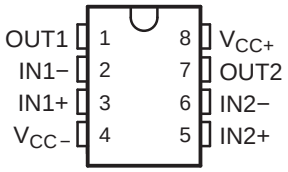
MC33078
DUAL HIGH-SPEED LOW-NOISE OPERATIONAL AMPLIFIER

SLLS633C – OCTOBER 2004 – REVISED NOVEMBER 2006

FEATURES

- **Dual-Supply Operation . . . ±5 V to ±18 V**
- **Low Noise Voltage . . . 4.5 nV/√Hz**
- **Low Input Offset Voltage . . . 0.15 mV**
- **Low Total Harmonic Distortion . . . 0.002%**
- **High Slew Rate . . . 7 V/μs**
- **High-Gain Bandwidth Product . . . 16 MHz**
- **High Open-Loop AC Gain . . . 800 at 20 kHz**
- **Large Output-Voltage Swing . . . 14.1 V to –14.6 V**
- **Excellent Gain and Phase Margins**

D (SOIC), DGK (MSOP), OR P (PDIP) PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

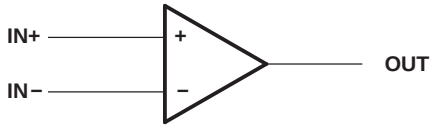
The MC33078 is a bipolar dual operational amplifier with high-performance specifications for use in quality audio and data-signal applications. This device operates over a wide range of single- and dual-supply voltages and offers low noise, high-gain bandwidth, and high slew rate. Additional features include low total harmonic distortion, excellent phase and gain margins, large output voltage swing with no deadband crossover distortion, and symmetrical sink/source performance.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
–40°C to 85°C	PDIP – P	Tube of 50	MC33078P	MC33078P
	SOIC – D	Tube of 75	MC33078D	M33078
		Reel of 2500	MC33078DR	
	VSSOP/MSOP – DGK	Reel of 2500	MC33078DGKR	MY_
		Reel of 250	MC33078DGKT	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) DGK: The actual top-side marking has one additional character that designates the assembly/test site.

SYMBOL (EACH AMPLIFIER)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC+}	Supply voltage(2)			18	V
V_{CC-}	Supply voltage(2)			–18	V
$V_{CC+} - V_{CC-}$	Supply voltage			36	V
	Input voltage, either input(2)(3)			V_{CC+} or V_{CC-}	V
	Input current(4)			±10	mA
	Duration of output short circuit(5)			Unlimited	
θ_{JA}	Package thermal impedance, junction to free air(6)(7)	D package		97	°C/W
		DGK package		172	
		P package		85	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
(4) Excessive input current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs, unless some limiting resistance is used.
(5) The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.
(6) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(7) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC-}	Supply voltage	–5	–18	V
V_{CC+}		5	18	
T_A	Operating free-air temperature range	–40	85	°C

Electrical Characteristics

V_{CC-} = –15 V, V_{CC+} = 15 V, T_A = 25°C (unless otherwise noted)

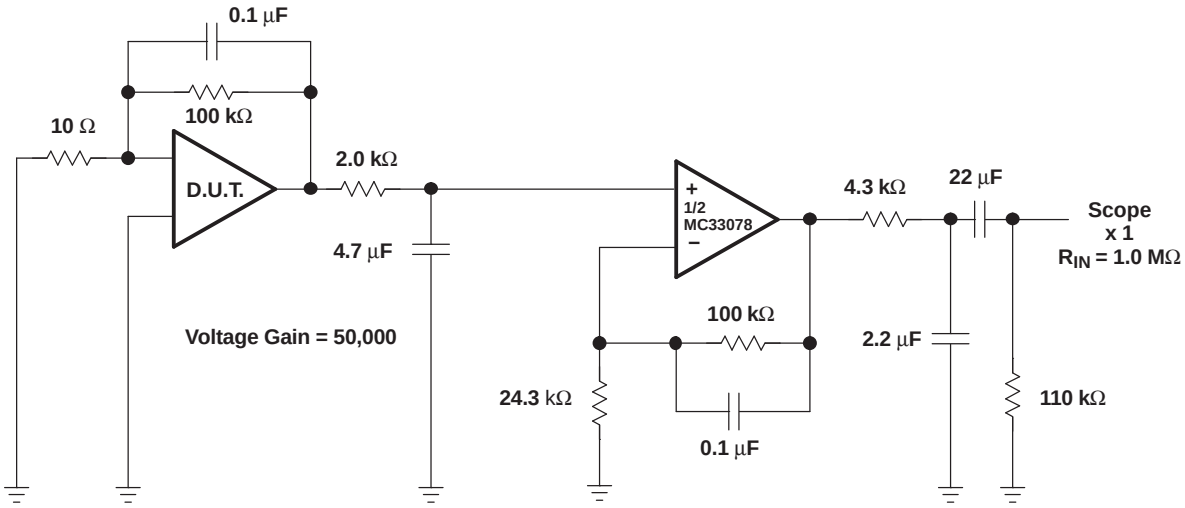
PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0, R_S = 10 Ω, V_{CM} = 0		T_A = 25°C		0.15	2	mV
				T_A = –40°C to 85°C			3	
αV_{IO}	Input offset voltage temperature coefficient	V_O = 0, R_S = 10 Ω, V_{CM} = 0		T_A = –40°C to 85°C		2		µV/°C
I_{IB}	Input bias current	V_O = 0, V_{CM} = 0		T_A = 25°C		300	750	nA
				T_A = –40°C to 85°C			800	
I_{IO}	Input offset current	V_O = 0, V_{CM} = 0		T_A = 25°C		25	150	nA
				T_A = –40°C to 85°C			175	
V_{ICR}	Common-mode input voltage range	ΔV_{IO} = 5 mV, V_O = 0			±13	±14		V
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2$ kΩ, V_O = ±10 V		T_A = 25°C	90	110		dB
				T_A = –40°C to 85°C	85			
V_{OM}	Maximum output voltage swing	V_{ID} = ±1 V	R_L = 600 Ω	V_{OM+}		10.7		V
				V_{OM-}		–11.9		
			R_L = 2k Ω	V_{OM+}	13.2	13.8		
				V_{OM-}	–13.2	–13.7		
			R_L = 10k Ω	V_{OM+}	13.5	14.1		
				V_{OM-}	–14	–14.6		
CMMR	Common-mode rejection ratio	V_{IN} = ±13 V			80	100		dB
k_{SVR} (1)	Supply-voltage rejection ratio	V_{CC+} = 5 V to 15 V, V_{CC-} = –5 V to –15 V			80	105		dB
I_{OS}	Output short-circuit current	$\|V_{ID}\|$ = 1 V, Output to GND		Source current	15	29		mA
				Sink current	–20	–37		
I_{CC}	Supply current (per channel)	V_O = 0		T_A = 25°C		2.05	2.5	mA
				T_A = –40°C to 85°C			2.75	

(1) Measured with $V_{CC\pm}$ differentially varied at the same time

Operating Characteristics

V_{CC-} = –15 V, V_{CC+} = 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	A_{VD} = 1, V_{IN} = –10 V to 10 V, R_L = 2 kΩ, C_L = 100 pF		5	7		V/µs
GBW	Gain bandwidth product	f = 100 kHz		10	16		MHz
B_1	Unity gain frequency	Open loop			9		MHz
G_m	Gain margin	R_L = 2 kΩ	C_L = 0 pF		–11		dB
			C_L = 100 pF		–6		
Φ_m	Phase margin	R_L = 2 kΩ	C_L = 0 pF		55		deg
			C_L = 100 pF		40		
	Amp-to-amp isolation	f = 20 Hz to 20 kHz			–120		dB
	Power bandwidth	V_O = 27 $V_{(PP)}$, R_L = 2 kΩ, THD ≤ 1%			120		kHz
THD	Total harmonic distortion	V_O = 3 V_{rms}, A_{VD} = 1, R_L = 2 kΩ, f = 20 Hz to 20 kHz			0.002		%
z_o	Open-loop output impedance	V_O = 0, f = 9 MHz			37		Ω
r_{id}	Differential input resistance	V_{CM} = 0			175		kΩ
C_{id}	Differential input capacitance	V_{CM} = 0			12		pF
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω			4.5		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz			0.5		pA/√Hz

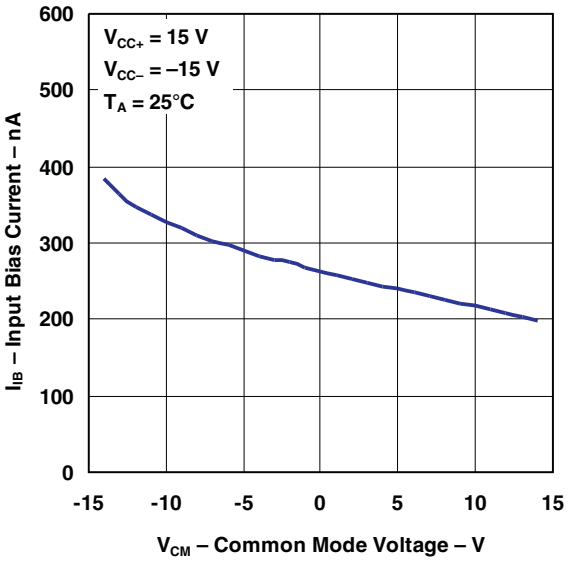


NOTE: All capacitors are non-polarized.

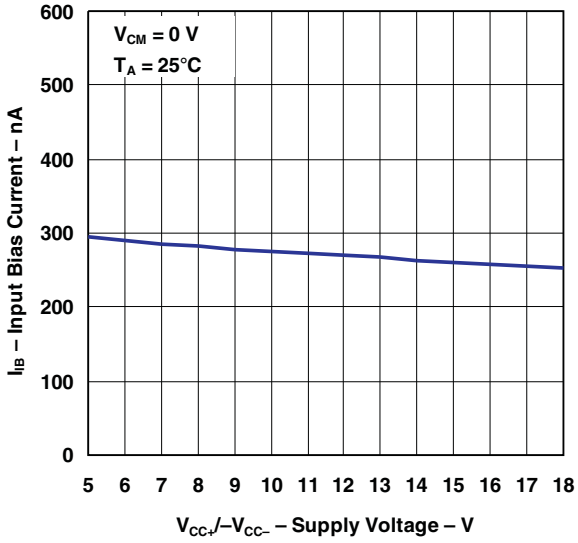
Figure 1. Voltage Noise Test Circuit (0.1 Hz to 10 Hz)

TYPICAL CHARACTERISTICS

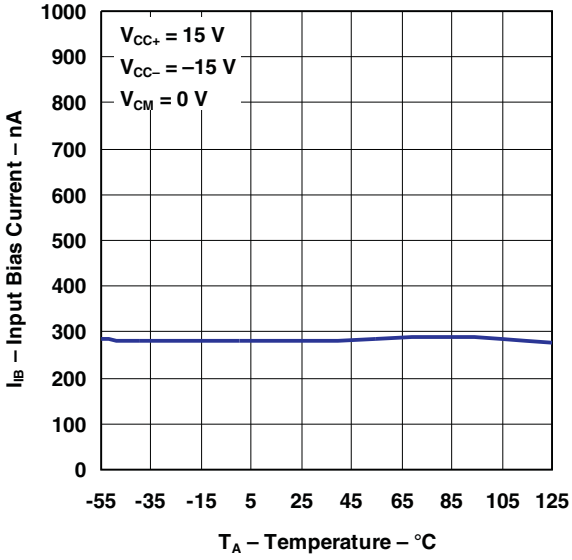
INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



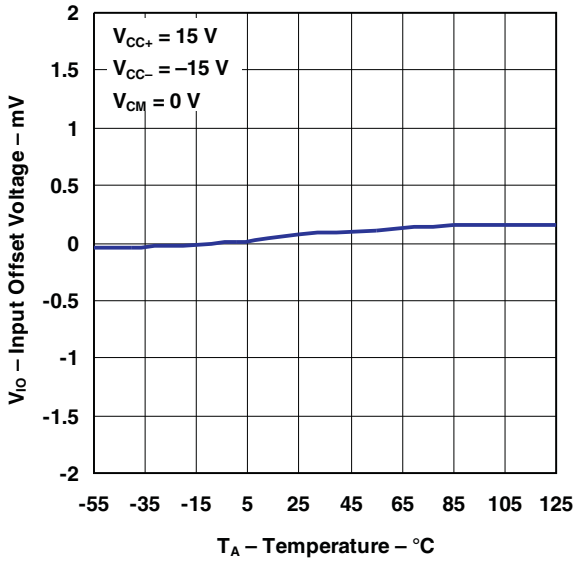
INPUT BIAS CURRENT vs SUPPLY VOLTAGE



INPUT BIAS CURRENT vs TEMPERATURE

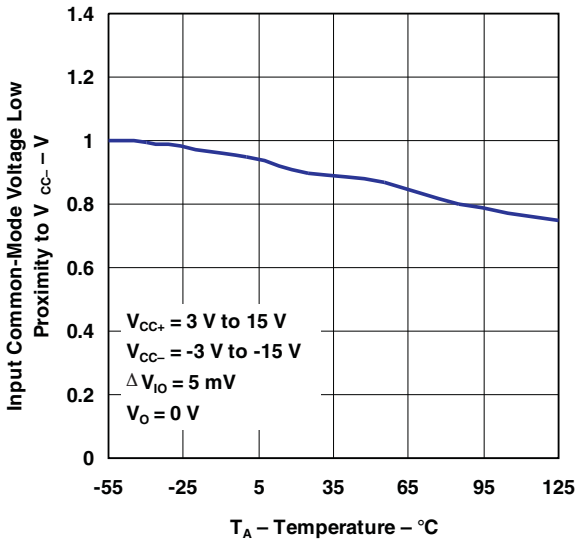


INPUT OFFSET VOLTAGE vs TEMPERATURE

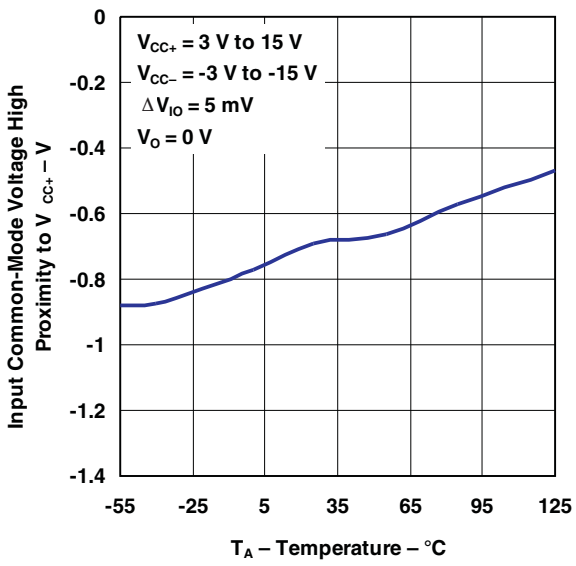


TYPICAL CHARACTERISTICS (continued)

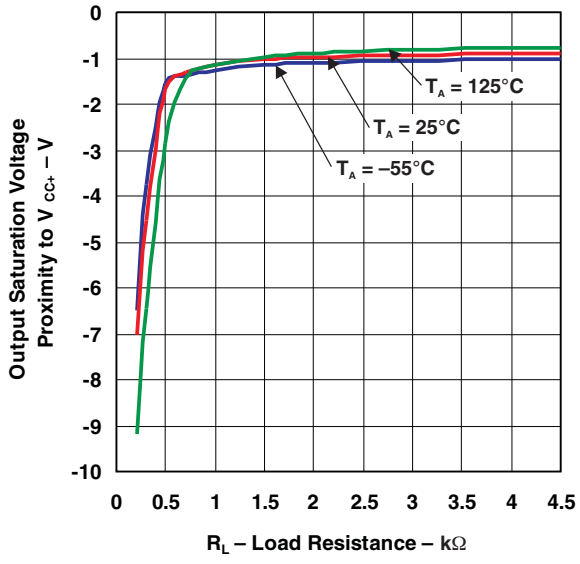
INPUT COMMON-MODE VOLTAGE LOW PROXIMITY TO V_{CC-} vs TEMPERATURE



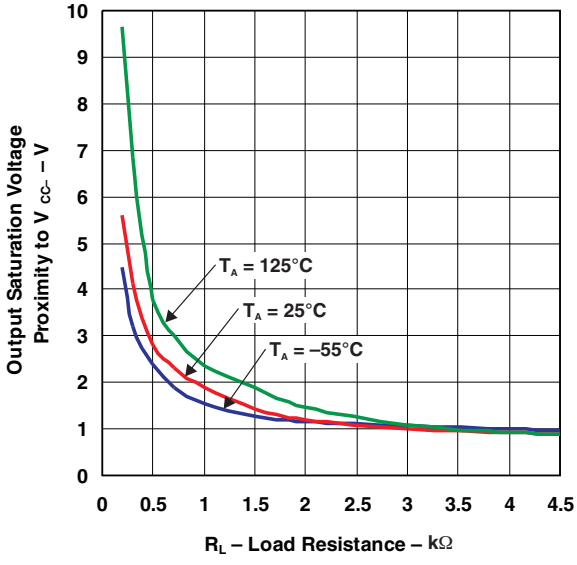
INPUT COMMON-MODE VOLTAGE HIGH PROXIMITY TO V_{CC+} vs TEMPERATURE



OUTPUT SATURATION VOLTAGE PROXIMITY TO V_{CC+} vs LOAD RESISTANCE

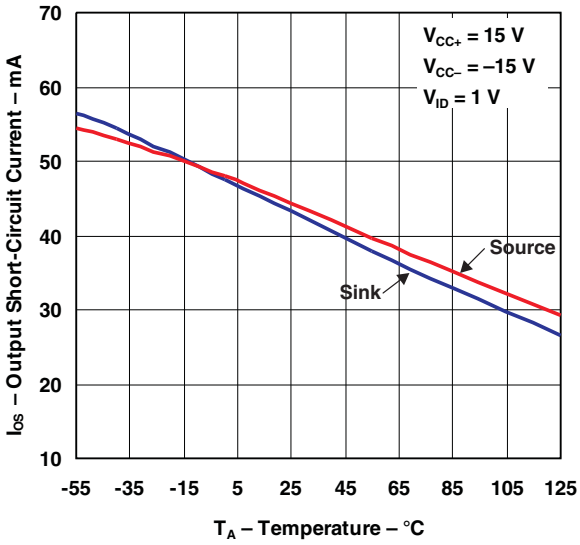


OUTPUT SATURATION VOLTAGE PROXIMITY TO V_{CC-} vs LOAD RESISTANCE

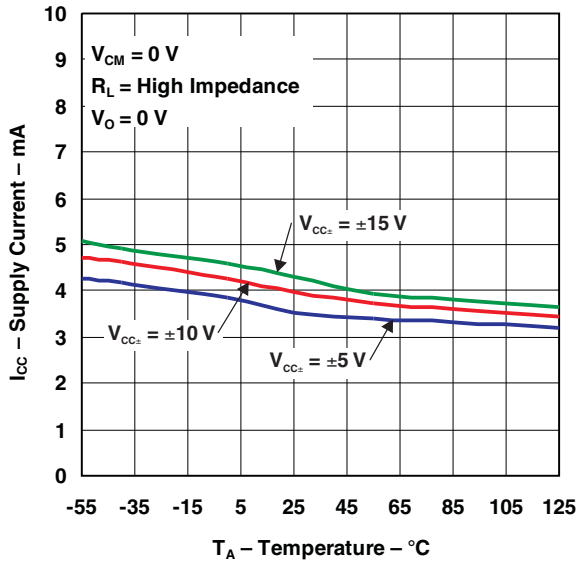


TYPICAL CHARACTERISTICS (continued)

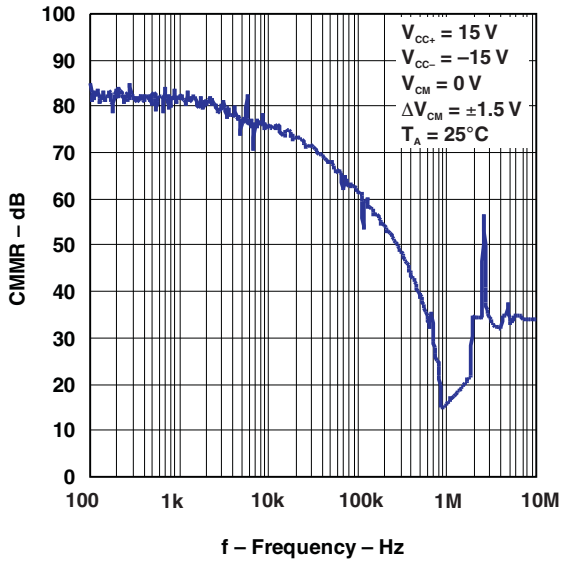
OUTPUT SHORT-CIRCUIT CURRENT vs TEMPERATURE



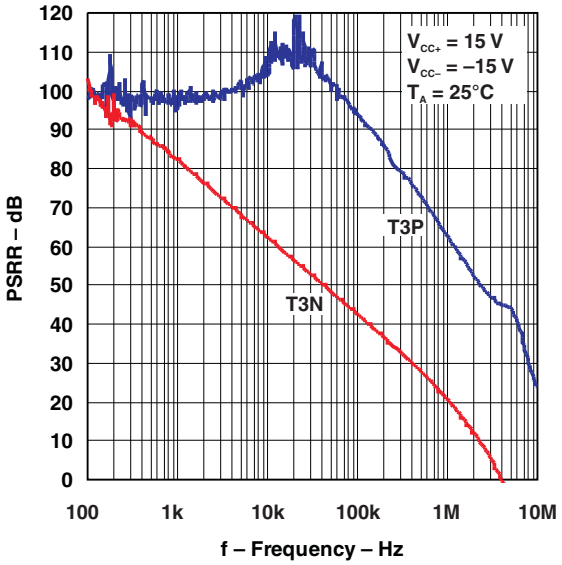
SUPPLY CURRENT vs TEMPERATURE



CMRR vs FREQUENCY

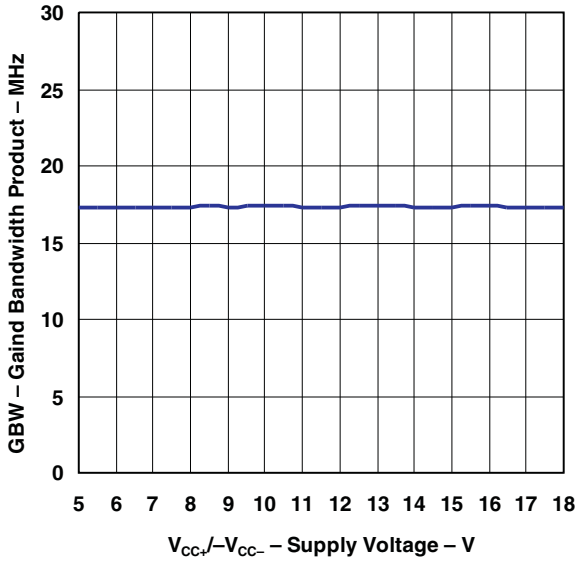


PSSR vs FREQUENCY

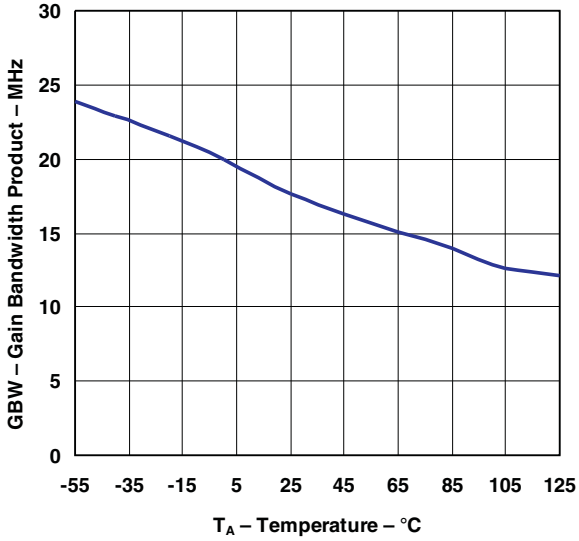


TYPICAL CHARACTERISTICS (continued)

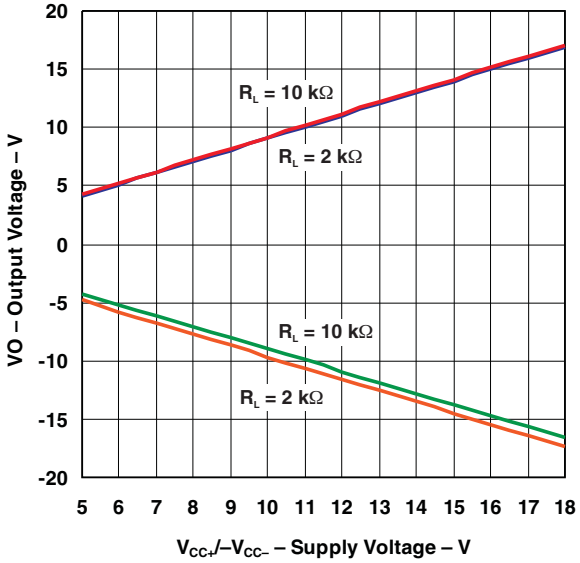
GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE



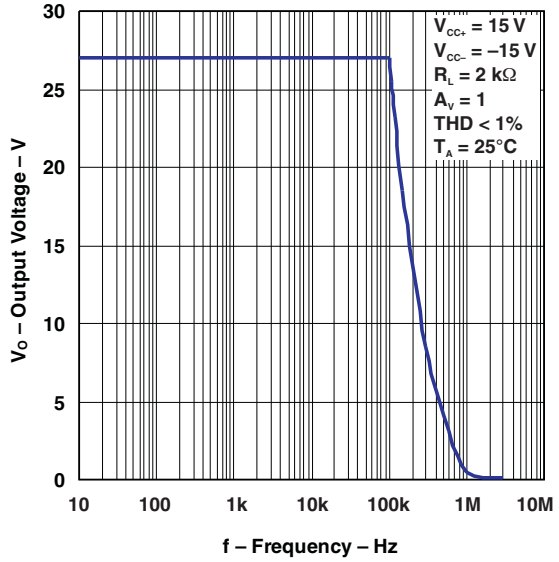
GAIN BANDWIDTH PRODUCT vs TEMPERATURE



OUTPUT VOLTAGE vs SUPPLY VOLTAGE

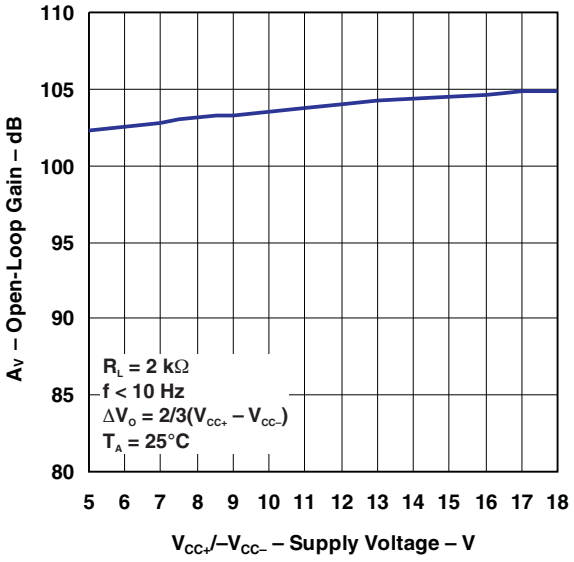


OUTPUT VOLTAGE vs FREQUENCY

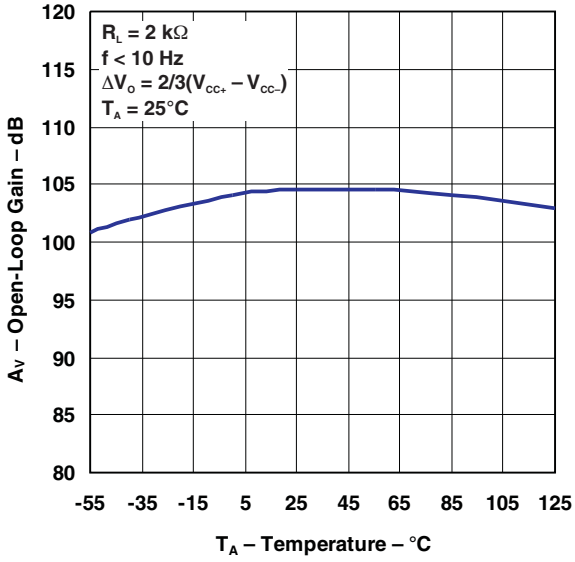


TYPICAL CHARACTERISTICS (continued)

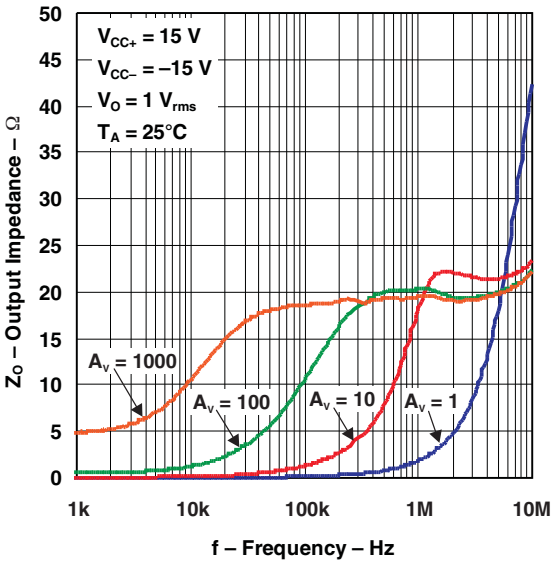
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



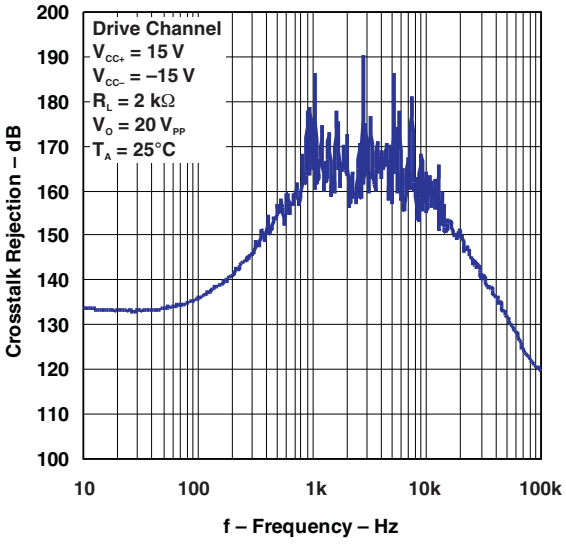
OPEN-LOOP GAIN vs TEMPERATURE



OUTPUT IMPEDANCE vs FREQUENCY

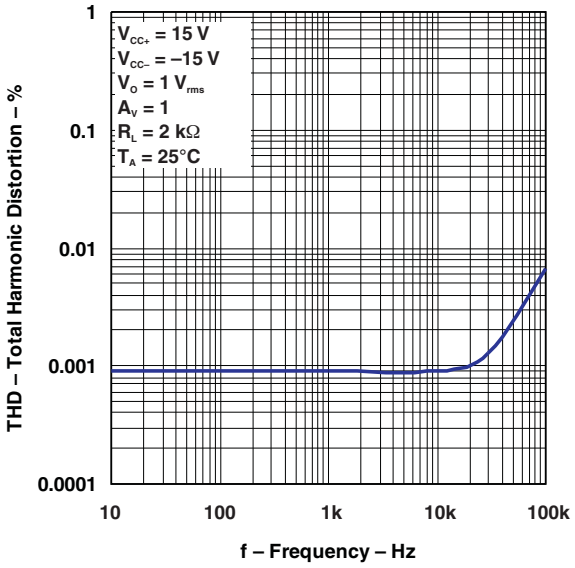


CROSSTALK REJECTION vs FREQUENCY

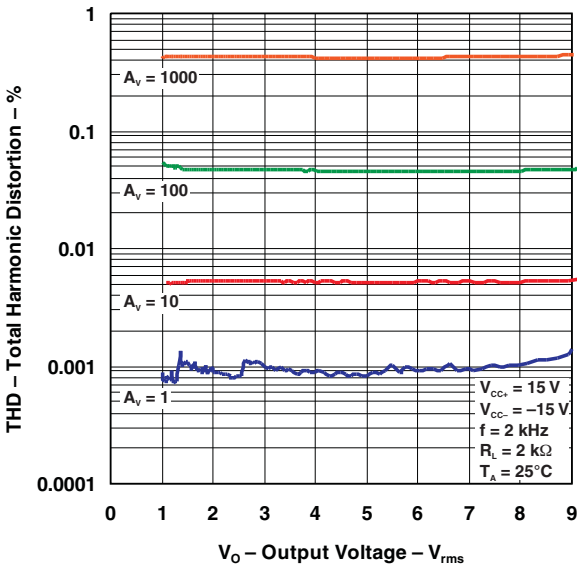


TYPICAL CHARACTERISTICS (continued)

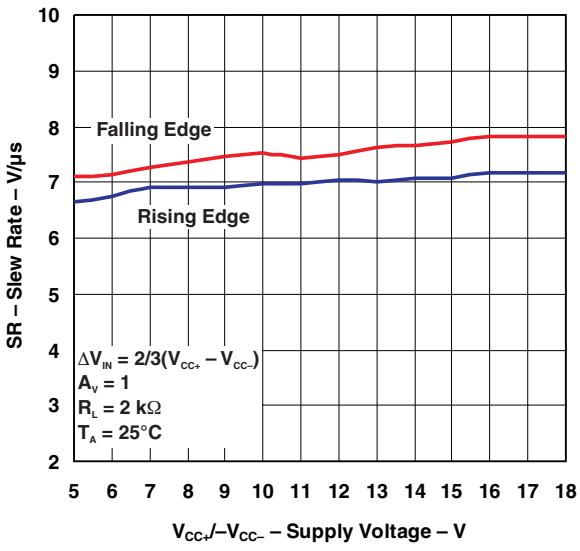
TOTAL HARMONIC DISTORTION vs FREQUENCY



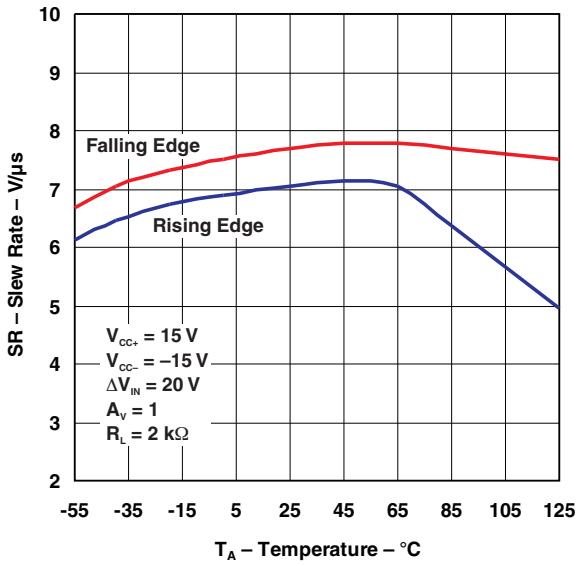
TOTAL HARMONIC DISTORTION vs OUTPUT VOLTAGE



SLEW RATE vs SUPPLY VOLTAGE

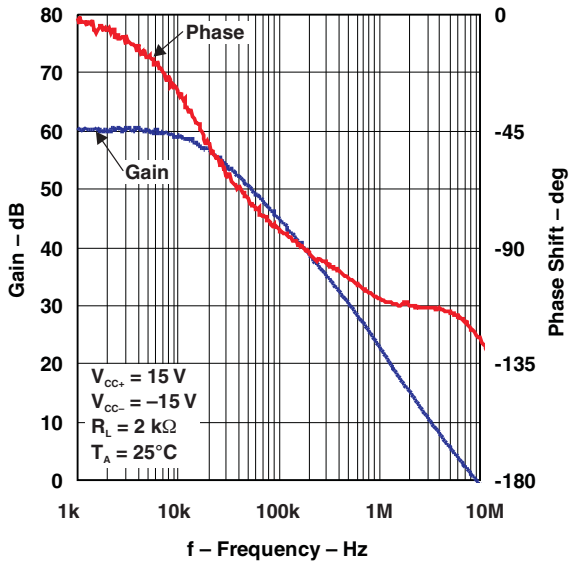


SLEW RATE vs TEMPERATURE

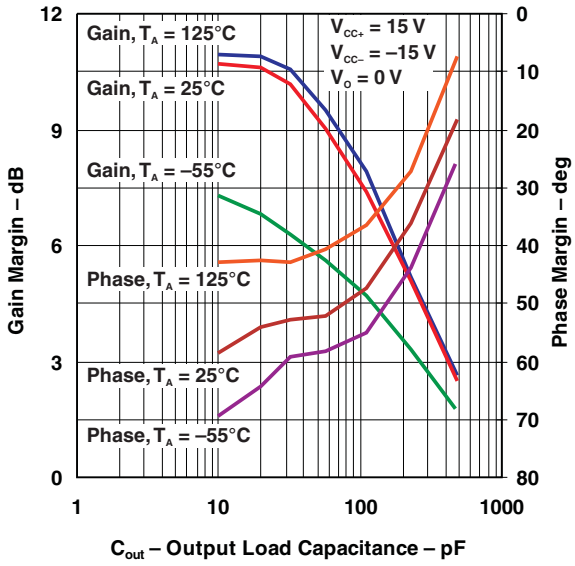


TYPICAL CHARACTERISTICS (continued)

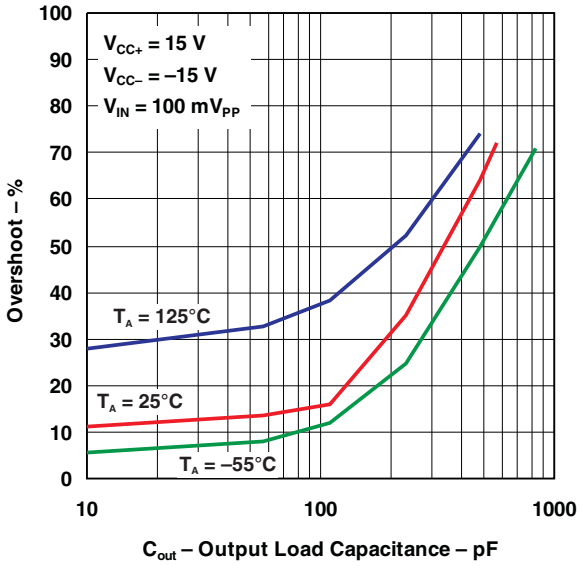
GAIN AND PHASE vs FREQUENCY



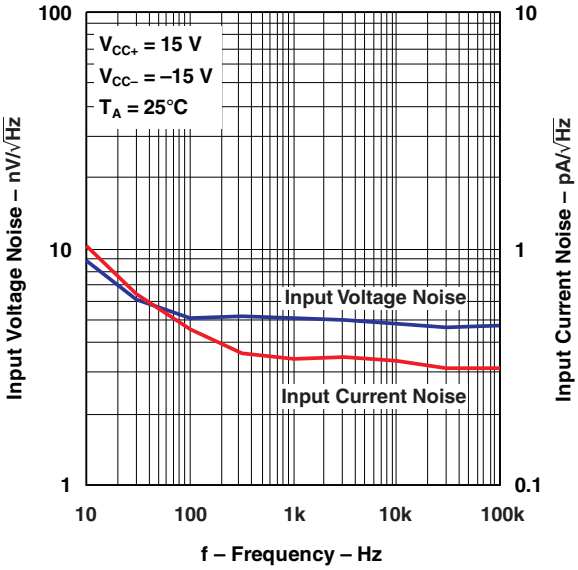
GAIN AND PHASE MARGIN vs OUTPUT LOAD CAPACITANCE



OVERSHOOT vs OUTPUT LOAD CAPACITANCE

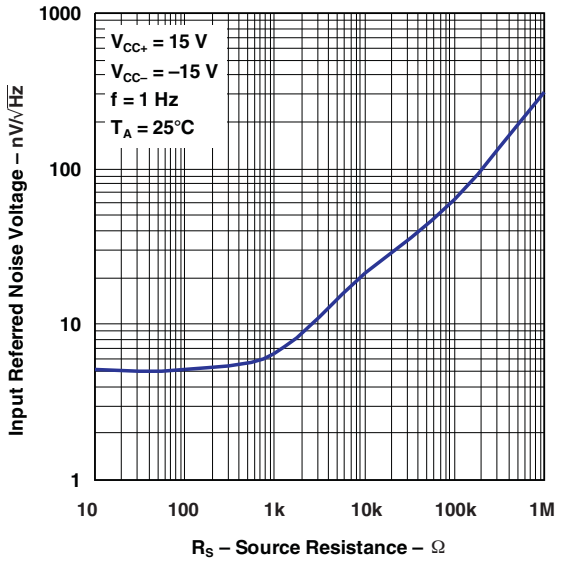


INPUT VOLTAGE AND CURRENT NOISE vs FREQUENCY

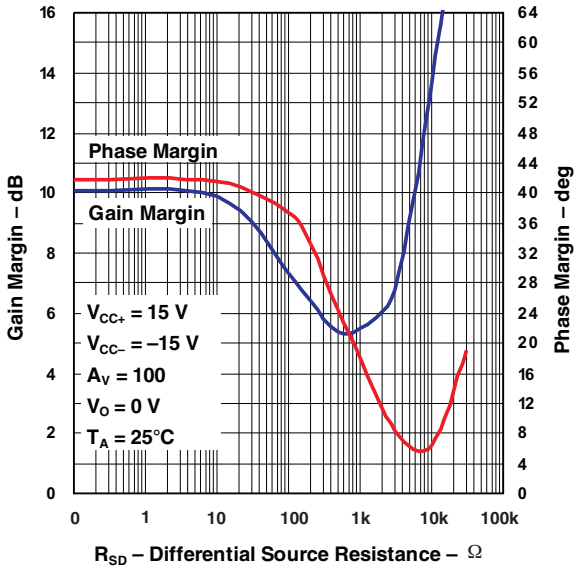


TYPICAL CHARACTERISTICS (continued)

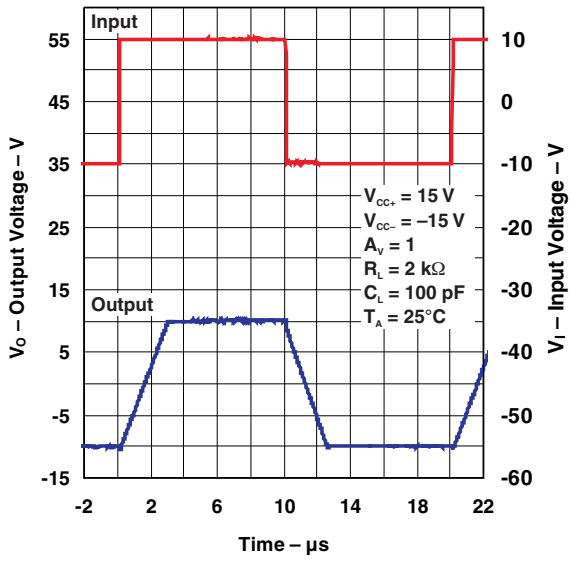
INPUT REFERRED NOISE VOLTAGE vs SOURCE RESISTANCE



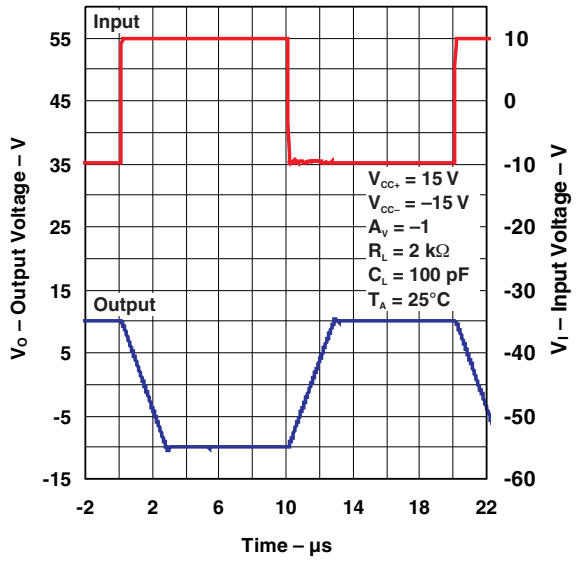
GAIN AND PHASE MARGIN vs DIFFERENTIAL SOURCE RESISTANCE



LARGE SIGNAL TRANSIENT RESPONSE (A_V = 1)

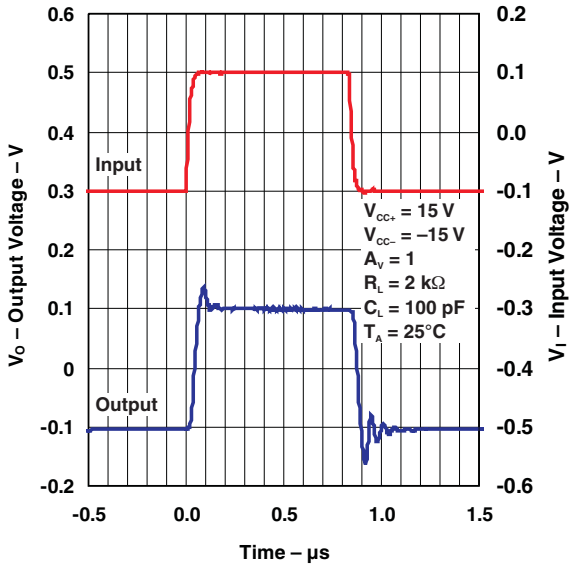


LARGE SIGNAL TRANSIENT RESPONSE (A_V = –1)

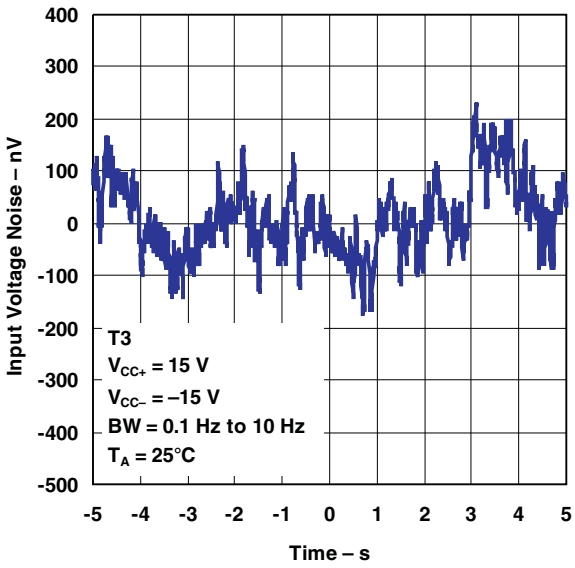


TYPICAL CHARACTERISTICS (continued)

SMALL SIGNAL TRANSIENT RESPONSE



LOW_FREQUENCY NOISE

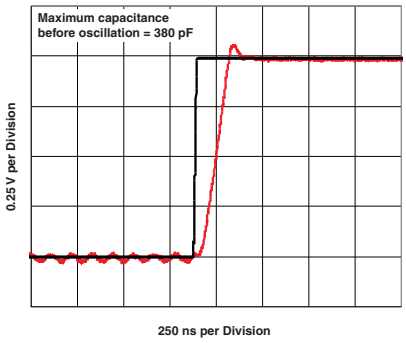


APPLICATION INFORMATION

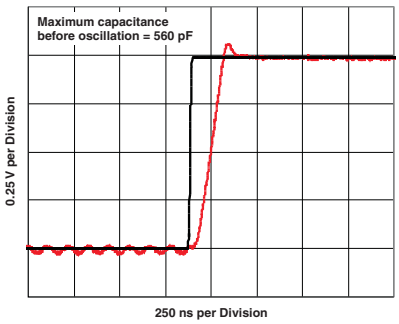
Output Characteristics

All operating characteristics are specified with 100-pF load capacitance. The MC33078 can drive higher capacitance loads. However, as the load capacitance increases, the resulting response pole occurs at lower frequencies, causing ringing, peaking, or oscillation. The value of the load capacitance at which oscillation occurs varies from lot to lot. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem (see Figure 2).

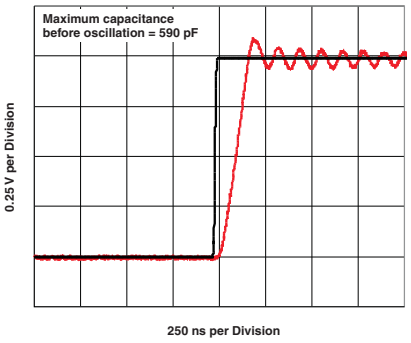
PULSE RESPONSE
(R_L = 600 Ω, C_L = 380 pF)



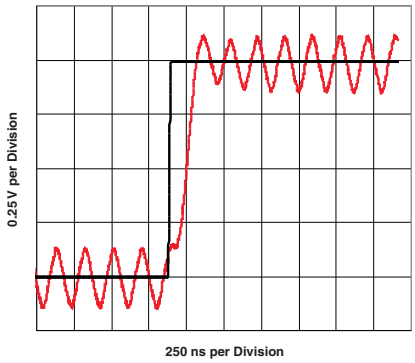
PULSE RESPONSE
(R_L = 2 kΩ, C_L = 560 pF)



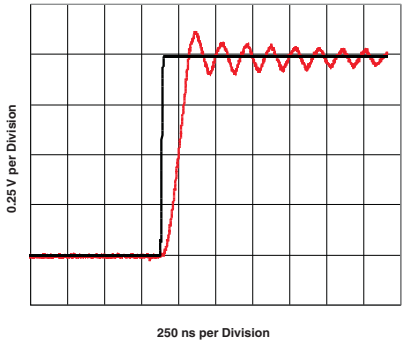
PULSE RESPONSE
(R_L = 10 kΩ, C_L = 590 pF)



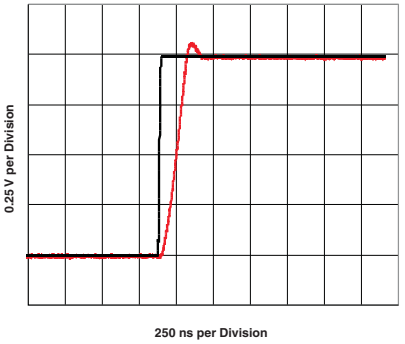
PULSE RESPONSE
(R_O = 0 Ω, C_O = 1000 pF, R_L = 2 kΩ)



PULSE RESPONSE
(R_O = 4 Ω, C_O = 1000 pF, R_L = 2 kΩ)



PULSE RESPONSE
(R_O = 35 Ω, C_O = 1000 pF, R_L = 2 kΩ)



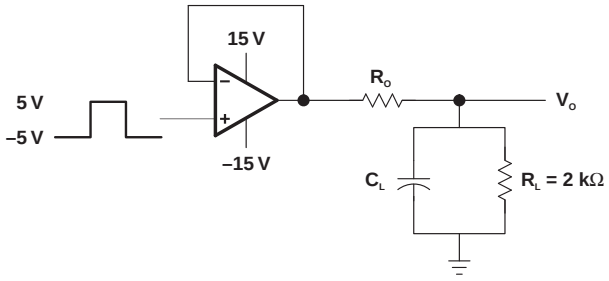


Figure 2. Output Characteristics

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MC33078D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	M33078
MC33078DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MYU
MC33078DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MYU
MC33078DGKR1G4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MYU
MC33078DGKR1G4.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MYU
MC33078DGKT	Obsolete	Production	VSSOP (DGK) | 8	-	-	Call TI	Call TI	-40 to 85	MYU
MC33078DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M33078
MC33078DR-NG	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M33078
MC33078DR-NG.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M33078
MC33078DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M33078
MC33078P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	MC33078P
MC33078P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	MC33078P

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

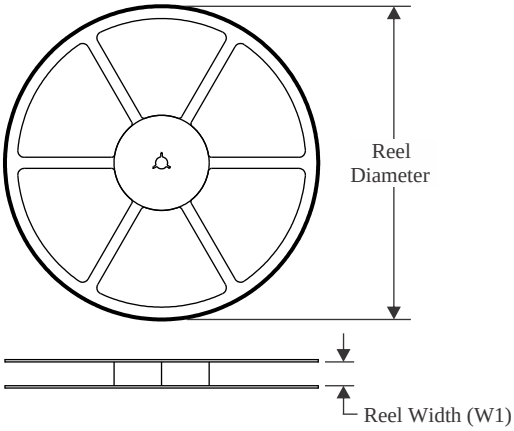
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

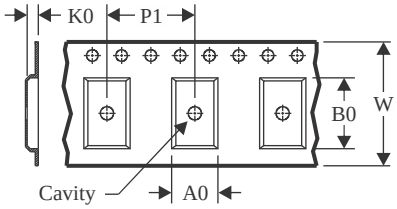
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

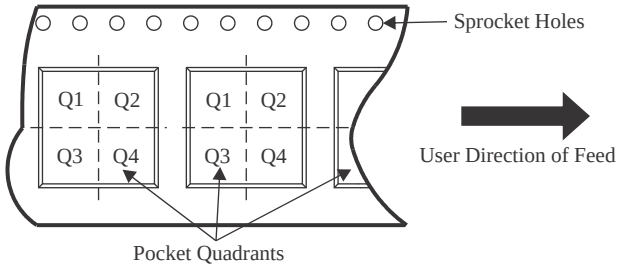


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

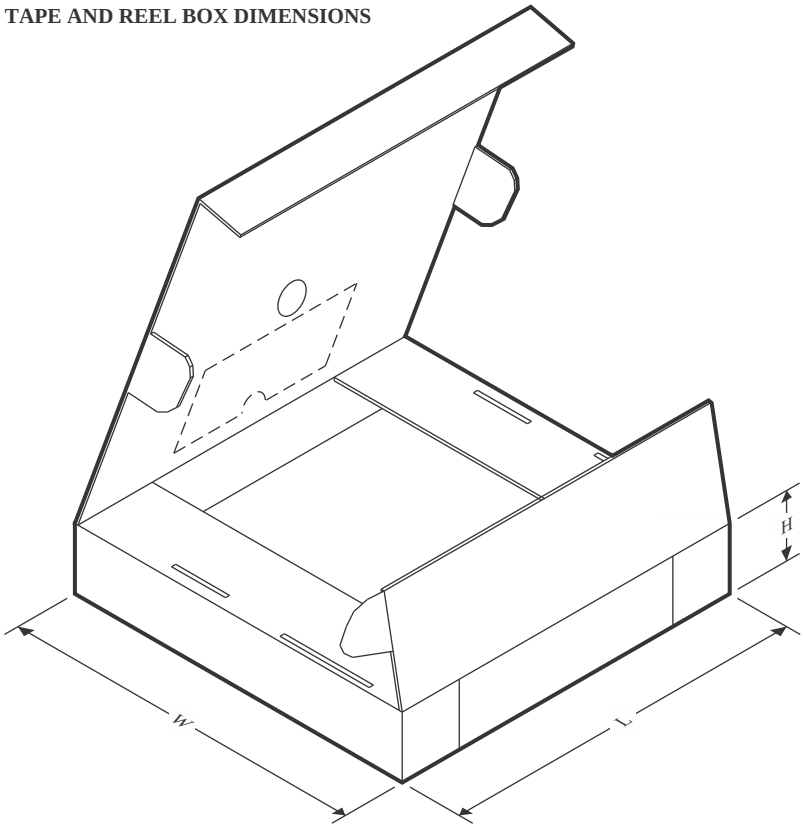
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MC33078DGKR	VSSOP	DGK	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
MC33078DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
MC33078DGKR1G4	VSSOP	DGK	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
MC33078DGKR1G4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
MC33078DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
MC33078DR-NG	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

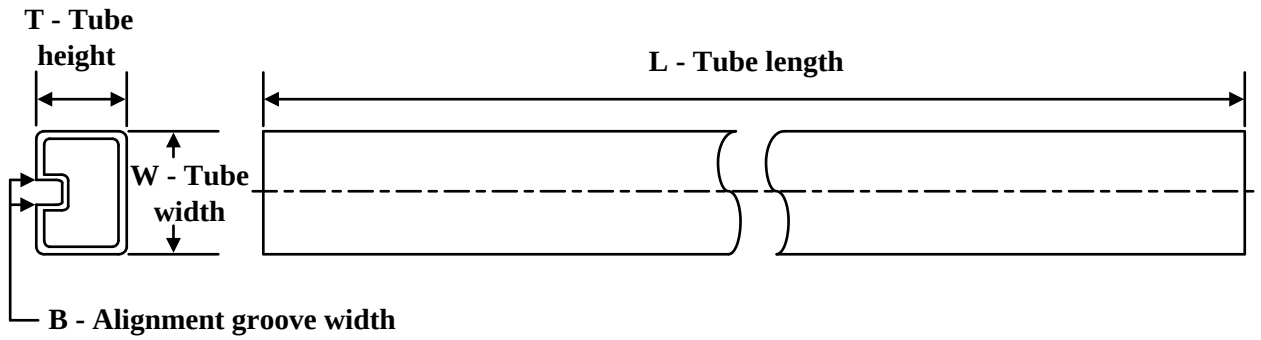
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MC33078DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
MC33078DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
MC33078DGKR1G4	VSSOP	DGK	8	2500	353.0	353.0	32.0
MC33078DGKR1G4	VSSOP	DGK	8	2500	353.0	353.0	32.0
MC33078DR	SOIC	D	8	2500	340.5	338.1	20.6
MC33078DR-NG	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

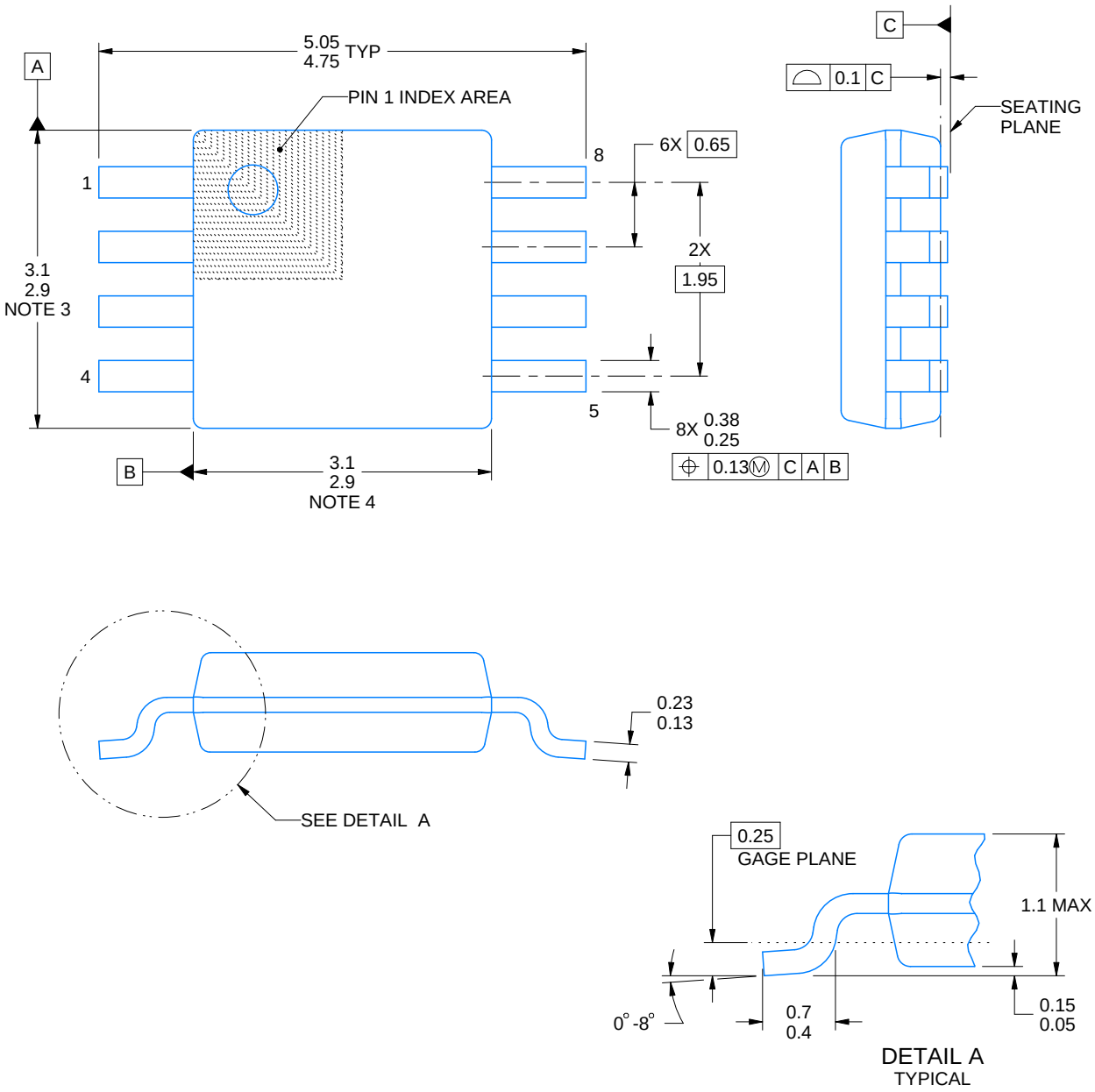
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MC33078P	P	PDIP	8	50	506	13.97	11230	4.32
MC33078P.A	P	PDIP	8	50	506	13.97	11230	4.32

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

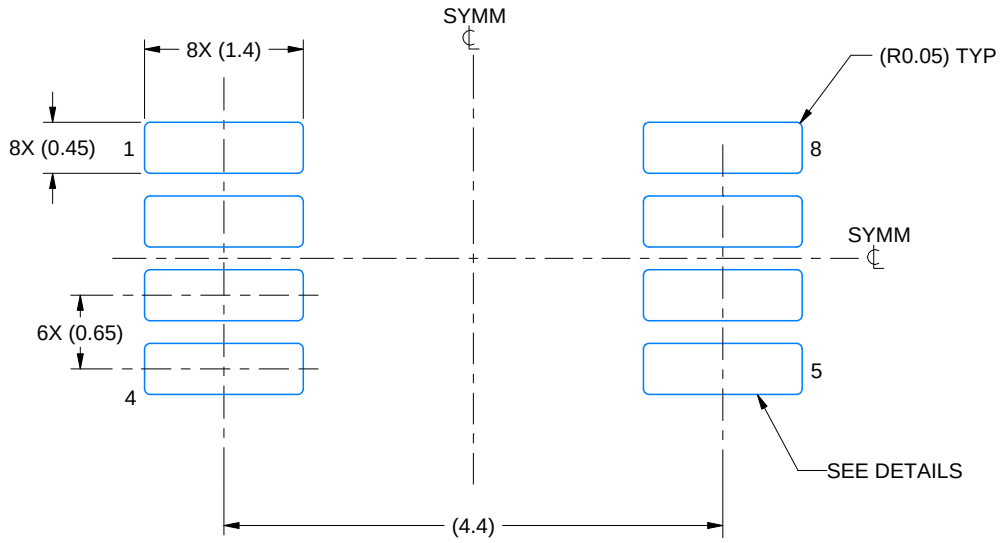
SMALL OUTLINE PACKAGE



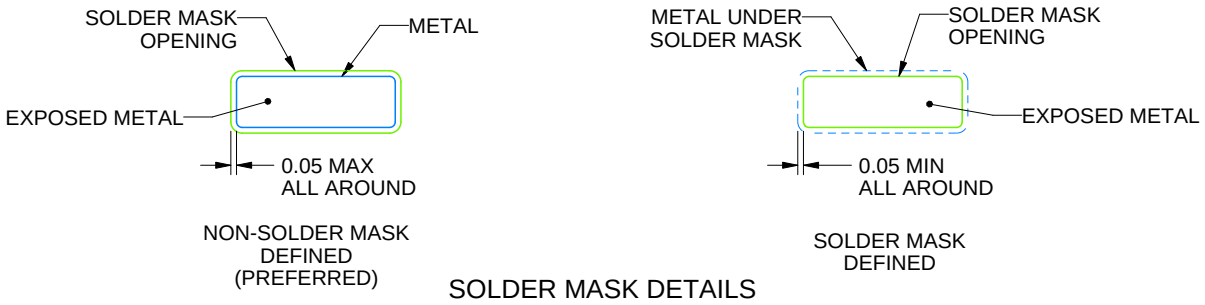
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

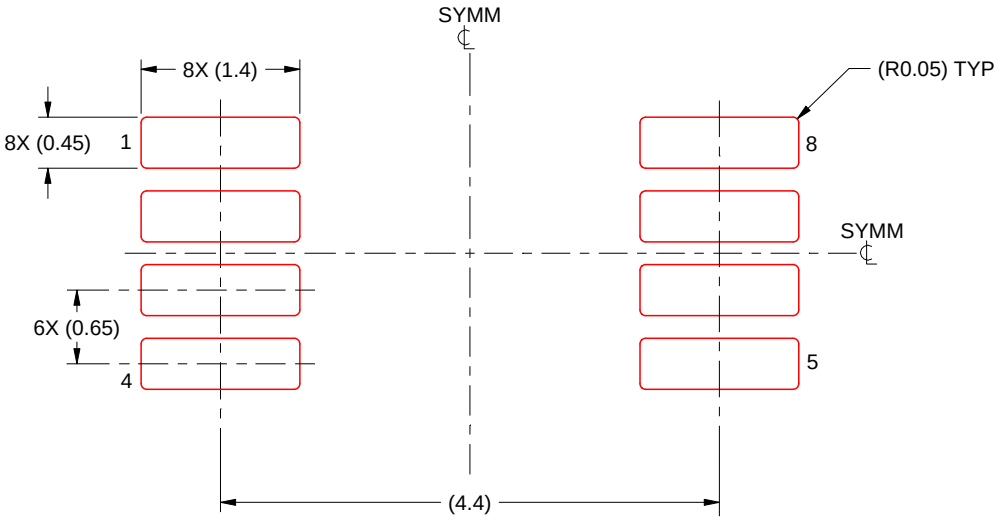


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

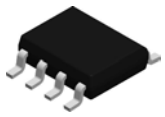


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

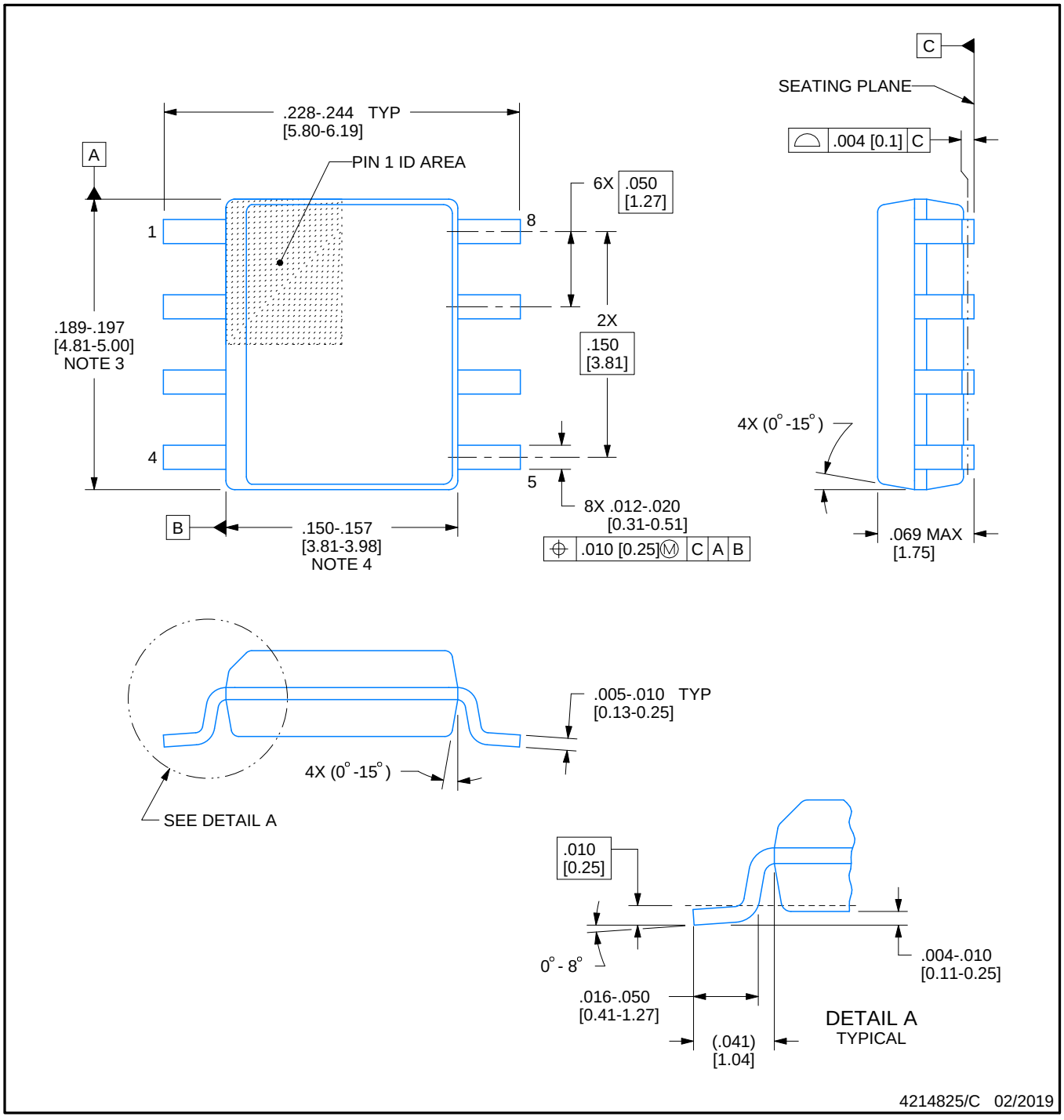


PACKAGE OUTLINE

D0008A

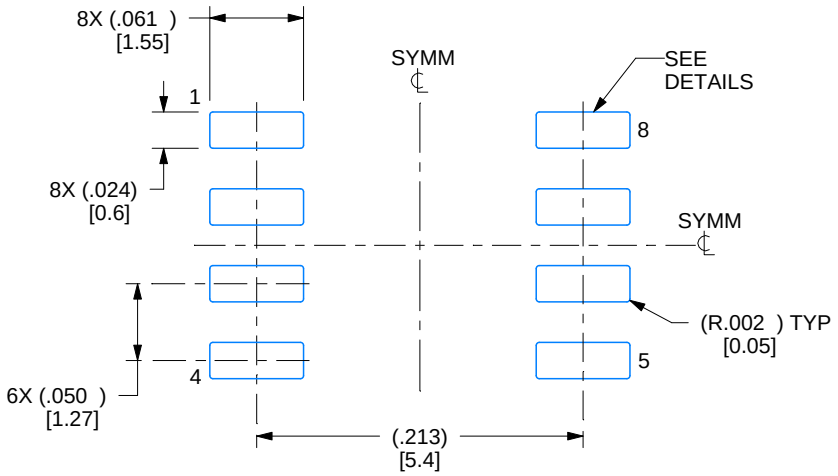
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

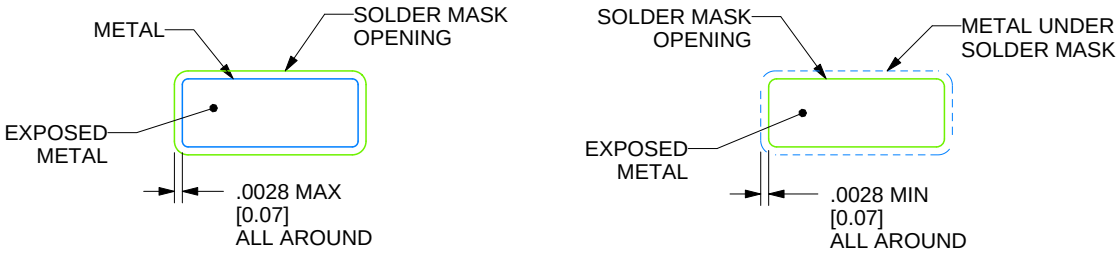


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

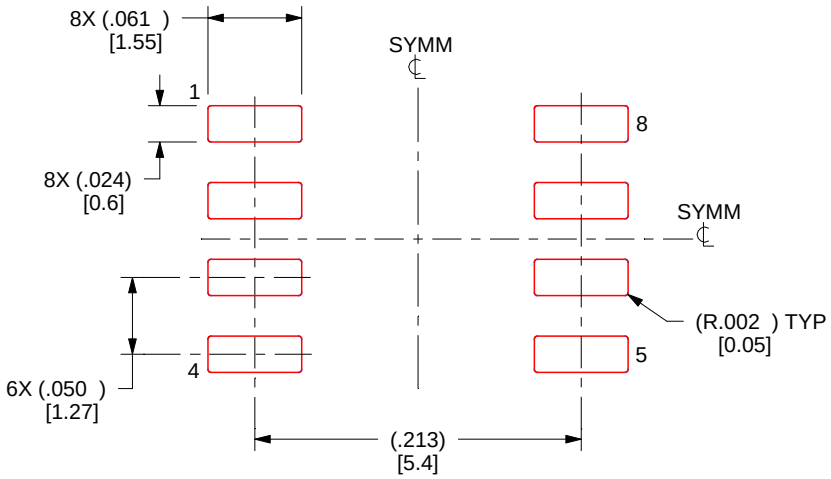
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



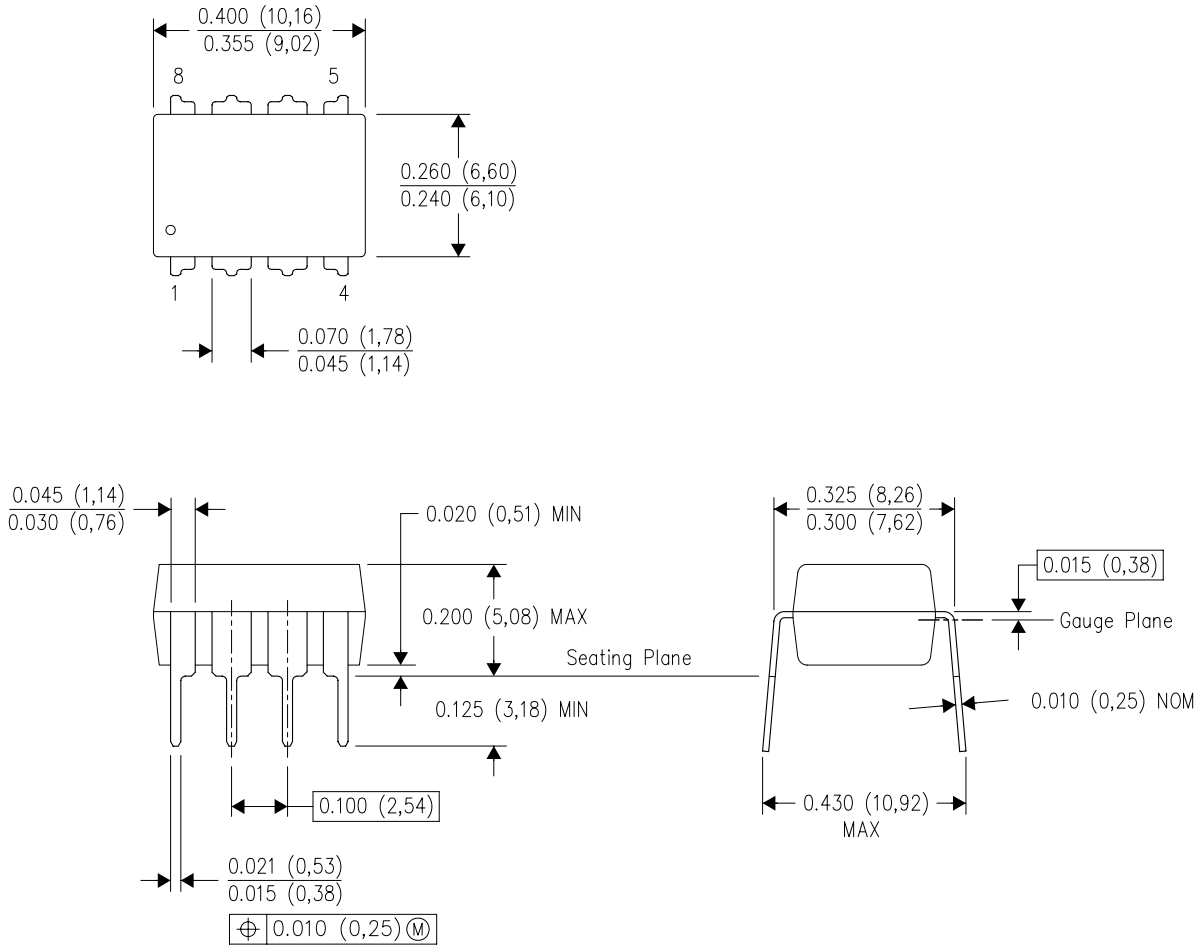
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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Last updated 10/2025