





3 Description





**LPV511** 

SNOSAG7D - AUGUST 2005 - REVISED AUGUST 2016

# LPV511 Micropower, Rail-to-Rail Input and Output Operational Amplifier

#### **Features**

Wide Supply Voltage Range: 2.7 V to 12 V

Slew Rate: 7.7 V/ms Supply Current: 880 nA

Output Short-Circuit Current: 1.35 mA

Rail-to-Rail Input

Rail-to-Rail Output: 100 mV from Rails Bandwidth ( $C_L = 50 \text{ pF}, R_L = 1 \text{ M}\Omega$ ): 27 kHz

Unity Gain Stable

### **Applications**

**Battery Powered Systems** 

Security Systems

Micropower Thermostats

Solar Powered Systems

Portable Instrumentation

Micropower Filters

Remote Sensor Amplifiers

The LPV511 is a micropower operational amplifier that operates from a voltage supply range as wide as 2.7 V to 12 V with ensured specifications at 3 V, 5 V, and 12 V. The ultra-low power LPV511 exhibits an excellent speed to power ratio, drawing only 880 nA of supply current with a bandwidth of 27 kHz. These specifications make the LPV511 an ideal choice for battery-powered systems that require long life through low supply current, such as instrumentation, sensor conditioning and battery current monitoring.

The LPV511 has an input range that includes both supply rails for ground and high-side battery sensing applications. The LPV511 output swings within 100 mV of either rail to maximize the signal's dynamic range in low supply applications. In addition, the output is capable of sourcing 650 µA of current when powered by a 12-V battery.

The LPV511 is fabricated on TI's advanced VIP50C process.

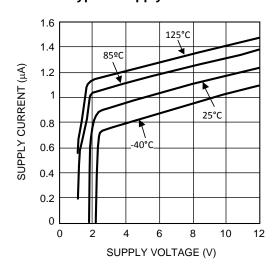
The LPV511 is available in the space-saving SC70 package, which makes it ideal for portable electronics with area-constrained PC boards.

#### Device Information<sup>(1)</sup>

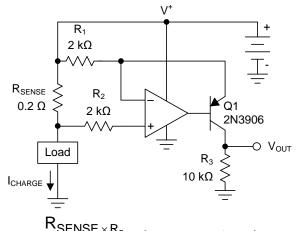
PART NUMBER	PACKAGE	BODY SIZE (NOM)		
LPV511	SC70 (5)	2.00 mm x 1.25 mm		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### **Typical Supply Current**



#### **High-Side Battery Current Sensor**



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### 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision C (March 2013) to Revision D

**Page** 

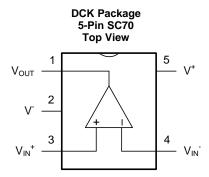
Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section
 Added Thermal Information table

### Changes from Revision B (March 2013) to Revision C

Page



# **5 Pin Configuration and Functions**



**Pin Functions** 

PIN		1/0	DESCRIPTION		
NO.	NAME	I/O	DESCRIPTION		
1	V <sub>OUT</sub>	0	Output		
2	V <sup>-</sup>	Р	Negative supply voltage		
3	V <sub>IN</sub> <sup>+</sup>	1	Noninverting input		
4	V <sub>IN</sub> <sup>-</sup>	1	Inverting input		
5	V <sup>+</sup>	Р	Positive supply voltage		

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### 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

	MIN	MAX	UNIT
V <sub>IN</sub> Differential		2.1	V
Supply voltage (V <sup>+</sup> - V <sup>-</sup> )	13.2		V
Voltage at input and output pins	V <sup>+</sup> + 0.3	V <sup>-</sup> - 0.3	V
Short-circuit duration	See <sup>(3)</sup>		
Junction temperature, T <sub>J</sub> <sup>(4)</sup>		150	°C
Storage temperature, T <sub>stg</sub>	-65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Output short-circuit duration is infinite for V<sup>+</sup> < 6 V at room temperature and below. For V<sup>+</sup> > 6 V, allowable short-circuit duration is 1.5 ms.
- (4) The maximum power dissipation is a function of  $T_{J(MAX)}$ ,  $R_{\theta JA}$ , and  $T_A$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(MAX)} T_A) / R_{\theta JA}$ . All numbers apply for packages soldered directly onto a PC board.

#### 6.2 ESD Ratings

			VALUE	UNIT
V	V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)(2)	±2000	V
V <sub>(ESD)</sub> EI		Machine model (MM) <sup>(3)</sup>	±200	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) Human Body Model: 1.5 kΩ in series with 100 pF.
- (3) Machine Model:  $0 \Omega$  in series with 200 pF.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Temperature <sup>(1)</sup>	-40	85	°C
Supply voltage (V <sup>+</sup> – V <sup>-</sup> )	2.7	12	V

<sup>(1)</sup> The maximum power dissipation is a function of  $T_{J(MAX)}$ ,  $R_{\theta JA}$ , and  $T_A$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$ . All numbers apply for packages soldered directly onto a PC board.

#### 6.4 Thermal Information

		LPV511	
	THERMAL METRIC <sup>(1)</sup>	DCK (SC70)	UNIT
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	278	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	105.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.4	°C/W
ΨЈТ	Junction-to-top characterization parameter	3	°C/W
ΨЈВ	Junction-to-board characterization parameter	55	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

 For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

Product Folder Links: LPV511



### 6.5 Electrical Characteristics: 3 V

Unless otherwise specified, all limits are specified for  $T_J = 25$ °C,  $V^+ = 3$  V,  $V^- = 0$  V,  $V_{CM} = V_O = V^+/2$ , and  $R_L = 100$  k $\Omega$  to V<sup>+</sup>/2. (1)

	PARAMETER	TEST CO	NDITIONS	MIN <sup>(2)</sup>	TYP <sup>(3)</sup>	MAX <sup>(2)</sup>	UNIT
.,	Lament affact confirms	T <sub>J</sub> = 25°C			±0.2	±3	
Vos	Input offset voltage	$T_J = -40$ °C to 85°C			±3.8	mV	
		T <sub>J</sub> = 25°C			±0.3		14/00
TC V <sub>OS</sub>	Input offset voltage drift <sup>(4)</sup>	$T_J = -40$ °C to 85°C				±15	μV/°C
		.,	T <sub>J</sub> = 25°C	-1000	-320		
	(5)	$V_{CM} = 0.5 \text{ V}$	$T_J = -40^{\circ}\text{C} \text{ to } 85^{\circ}\text{C}$	-1600			
I <sub>B</sub>	Input bias current <sup>(5)</sup>		T <sub>J</sub> = 25°C		110	800	pA
		$V_{CM} = 2.5 \text{ V}$	$T_{J} = -40^{\circ}\text{C to } 85^{\circ}\text{C}$			1900	
I <sub>OS</sub>	Input offset current		1 0		±10		pA
	'	V <sub>CM</sub> Stepped from 0 V to	T <sub>J</sub> = 25°C	77	100		•
		1.5 V	$T_{J} = -40^{\circ}\text{C to } 85^{\circ}\text{C}$	70			
CMRR		V <sub>CM</sub> Stepped from 2.4 V	T <sub>J</sub> = 25°C	75	115		
	Common mode rejection ratio	to 3 V	$T_{J} = -40^{\circ}\text{C to } 85^{\circ}\text{C}$	68			dB
		V <sub>CM</sub> Stepped from 0.5 V	T <sub>J</sub> = 25°C	60	80		
		to 2.5 V	$T_{J} = -40^{\circ}\text{C to } 85^{\circ}\text{C}$	56			
		V <sup>+</sup> = 2.7 V to 5 V,	$T_J = 25^{\circ}C$	72			
	Power supply rejection ratio	V = 2.7  V to 3 V, $V_{CM} = 0.5 \text{ V}$	$T_J = -40^{\circ}\text{C to } 85^{\circ}\text{C}$	68			
		\/+ - 3 \/ to 5 \/	$T_J = 25^{\circ}C$	76	115		
PSRR			$T_{J} = -40^{\circ}\text{C to } 85^{\circ}\text{C}$	72			dB
		V <sup>+</sup> = 5 V to 12 V, V <sub>CM</sub> = 0.5 V	$T_J = 25^{\circ}C$	84	117		
			$T_J = -40^{\circ}\text{C to } 85^{\circ}\text{C}$	80			
			$T_J = 25^{\circ}C$	-0.1		3.1	
CMVR	Input common-mode voltage	CMRR ≥ 50 dB	$T_J = -40^{\circ}\text{C to } 85^{\circ}\text{C}$	0		3	V
			$T_J = 25^{\circ}C$	75	105		
		Sinking, $V_0 = 2.5 \text{ V}$	$T_J = -40^{\circ}\text{C to } 85^{\circ}\text{C}$	70	100		
$A_{VOL}$	Large signal voltage gain		$T_{J} = 25^{\circ}C$	75	105		dB
		Sourcing, $V_O = 0.5 \text{ V}$	$T_J = -40^{\circ}\text{C to } 85^{\circ}\text{C}$	70	100		
			$T_J = 25^{\circ}C$	2.85	2.9		
	Output swing high	$V_{ID} = 100 \text{ mV}$	$T_J = -40^{\circ}\text{C to } 85^{\circ}\text{C}$	2.8	2.0		
$V_{O}$			$T_{J} = 25^{\circ}C$	2.0	100	150	V
	Output swing low	$V_{ID} = -100 \text{ mV}$	$T_J = -40^{\circ}\text{C to } 85^{\circ}\text{C}$		100	200	
		Sourcing	11 - 40 0 10 03 0				
	Outrout als and aircoit auror (6)	$V_{ID} = 100 \text{ mV}$			-500	-225	
I <sub>SC</sub>	Output short circuit current (6)	Sinking V <sub>ID</sub> = −100 mV		225	1350		μΑ
	0 1 /	T <sub>J</sub> = 25°C			0.88	1.2	
I <sub>S</sub>	Supply current	$T_{J} = -40^{\circ}\text{C to } 85^{\circ}\text{C}$				1.5	μA
	. (7)	$A_V = 1$ , $V_O$ ramps from	T <sub>J</sub> = 25°C	5.25	7.7		
SR	Slew rate <sup>(7)</sup>	ate <sup>(7)</sup> $A_V = 1$ , $V_O$ ramps from $0.5 \text{ V}$ to $2.5 \text{ V}$		3.10			V/ms

<sup>(1)</sup> Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

Product Folder Links: LPV511

Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.

<sup>(3)</sup> Typical values represent the most likely parametric norm at the time of characterization.

<sup>(4)</sup> Offset voltage drift is specified by design and/or characterization and is not tested in production. Offset voltage drift is determined by dividing the change in VOS at temperature extremes into the total temperature change.

Positive current corresponds to current flowing into the device.

The Short-Circuit Test is a momentary test. See Note 3 in Absolute Maximum Ratings.

Slew rate is the average of the rising and falling slew rates. (7)



### **Electrical Characteristics: 3 V (continued)**

Unless otherwise specified, all limits are specified for  $T_J = 25$  °C,  $V^+ = 3$  V,  $V^- = 0$  V,  $V_{CM} = V_O = V^+/2$ , and  $R_L = 100$  k $\Omega$  to  $V^+/2$ .

	PARAMETER	TEST CONDITIONS	MIN <sup>(2)</sup>	TYP <sup>(3)</sup>	MAX <sup>(2)</sup>	UNIT
GBW	Gain bandwidth product	$R_L = 1 M\Omega$ , $C_L = 50 pF$		27		kHz
	Phase margin	$R_L = 1 \text{ M}\Omega$ , $C_L = 50 \text{ pF}$		53		0
e <sub>n</sub>	Input-referred voltage noise	f = 100 Hz		320		nV/√ <del>Hz</del>
	land unformed accompant waits	f = 10 Hz		0.02		pA/√Hz
In	Input-referred current noise	f = 1 kHz		0.01		pavvnz

### 6.6 Electrical Characteristics: 5 V

Unless otherwise specified, all limits are specified for  $T_J = 25^{\circ}C$ ,  $V^+ = 5$  V,  $V^- = 0$  V,  $V_{CM} = V_O = V^+/2$ , and  $R_L = 100$  k $\Omega$  to  $V^+/2$ .

	PARAMETER	TEST CO	NDITIONS	MIN <sup>(2)</sup>	TYP <sup>(3)</sup>	MAX <sup>(2)</sup>	UNIT	
	$T_{\rm J} = 25^{\circ}{\rm C}$				±0.2	±3	\/	
Vos	input offset voltage	$T_J = -40$ °C to 85°C			±3.8	mV		
TOV	land offer to the second site (4)	T <sub>J</sub> = 25°C			±0.3			
TC V <sub>OS</sub>	Input offset voltage drift <sup>(4)</sup>	$T_J = -40$ °C to 85°C				±15	μV/°C	
İ		V - 0.5.V	$T_J = 25^{\circ}C$	-1000	-320			
	Input bias current <sup>(5)</sup>	$V_{CM} = 0.5 \text{ V}$	$T_J = -40$ °C to 85°C	-1600			pА	
I <sub>B</sub>	input bias current	V - 45 V	$T_J = 25^{\circ}C$		110	800	þΑ	
		V <sub>CM</sub> = 4.5 V	$T_J = -40$ °C to 85°C			1900		
Ios	Input offset current				±10		pА	
ĺ		V <sub>CM</sub> Stepped from	$T_J = 25^{\circ}C$	80	115			
	Common mode rejection ratio	0 V 1	0 V to 2.5 V	$T_J = -40$ °C to 85°C	73			
CMRR		V <sub>CM</sub> Stepped from	$T_J = 25^{\circ}C$	75	107		dB	
CIVIKK		4.4 to 5 V	$T_J = -40$ °C to 85°C	68				
		V <sub>CM</sub> Stepped from	$T_J = 25^{\circ}C$	65	87			
		0.5 to 4.5 V	$T_J = -40$ °C to 85°C	62				
		$V^{+} = 2.7 \text{ V to 5 V},$	$T_J = 25^{\circ}C$	72	114		İ	
		$V_{CM} = 0.5 \text{ V}$	$T_J = -40$ °C to 85°C	68				
PSRR	Power supply rejection ratio	$V^{+} = 3 V \text{ to } 5 V,$	$T_J = 25^{\circ}C$	76	115		dB	
FORK	Power Supply rejection ratio	$V_{CM} = 0.5 \text{ V}$	$T_J = -40$ °C to 85°C	72			uБ	
		$V^{+} = 5 V \text{ to } 12 V,$	$T_J = 25^{\circ}C$	84	117			
		$V_{CM} = 0.5 \text{ V}$	$T_J = -40$ °C to 85°C	80				
CMVR	Input common-mode voltage	CMRR ≥ 50 dB	$T_J = 25^{\circ}C$	0.1		5.1	V	
CIVIVK	input common-mode voitage	CIVIRR 2 50 UB	$T_J = -40$ °C to 85°C	0		5	V	
		Otalian V A5V	$T_J = 25^{\circ}C$	78	110		dB	
Δ	Large signal voltage gain	Sinking, $V_O = 4.5 \text{ V}$	$T_J = -40$ °C to 85°C	73				
A <sub>VOL</sub>	Large signal voltage galli		$T_J = 25^{\circ}C$	78	110			
<u> </u>		Sourcing, V <sub>O</sub> = 0.5 V	$T_J = -40$ °C to 85°C	73				

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<sup>(1)</sup> Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

<sup>(2)</sup> Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.

<sup>3)</sup> Typical values represent the most likely parametric norm at the time of characterization.

<sup>(4)</sup> Offset voltage drift is specified by design and/or characterization and is not tested in production. Offset voltage drift is determined by dividing the change in VOS at temperature extremes into the total temperature change.

<sup>(5)</sup> Positive current corresponds to current flowing into the device.



### **Electrical Characteristics: 5 V (continued)**

Unless otherwise specified, all limits are specified for  $T_J = 25^{\circ}C$ ,  $V^+ = 5$  V,  $V^- = 0$  V,  $V_{CM} = V_O = V^+/2$ , and  $R_L = 100$  k $\Omega$  to  $V^+/2$ .

	PARAMETER	TEST CON	IDITIONS	MIN <sup>(2)</sup>	TYP <sup>(3)</sup>	MAX <sup>(2)</sup>	UNIT
	Outside subject	\/ 100 m\/	$T_J = 25^{\circ}C$	4.8	4.89		V
.,	Output swing high	V <sub>ID</sub> = 100 mV	$T_J = -40$ °C to 85°C	4.75			V
Vo	Output outpa lou	\/ 100 m\/	T <sub>J</sub> = 25°C		110	200	mV
	Output swing low	V <sub>ID</sub> = −100 mV	$T_J = -40$ °C to 85°C			250	mv
	Output about airquit aurrant (6)	Sourcing to V <sup>-</sup> V <sub>ID</sub> = 100 mV			-550	-225	
I <sub>SC</sub>	Output short circuit current (6)	Sinking to V <sup>+</sup> V <sub>ID</sub> = −100 mV		225	1350		μΑ
	Complex compant	$T_J = 25^{\circ}C$			0.97	1.2	
I <sub>S</sub>	Supply current	$T_J = -40$ °C to 85°C				1.5	μA
SR	Slew rate <sup>(7)</sup>	$A_V = 1$ , $V_O$ ramps from	$T_J = 25^{\circ}C$	5.25	7.5		V/ms
SK	Siew fate 7	0.5 V to 4.5 V	$T_J = -40$ °C to 85°C	3.1			V/1115
GBW	Gain bandwidth product	$R_L = 1 M\Omega$ , $C_L = 50 pF$			27		kHz
	Phase margin	$R_L = 1 M\Omega$ , $C_L = 50 pF$			53		0
e <sub>n</sub>	Input-referred voltage noise	f = 100 Hz			320		nV/√ <del>Hz</del>
	lanut referred current noise	f = 10 Hz			0.02		- Λ / <sub>0</sub> /II=
In	Input-referred current noise	f = 1 kHz			0.01		pA/√Hz

<sup>(6)</sup> The Short-Circuit Test is a momentary test. See Note 3 in Absolute Maximum Ratings.

#### 6.7 Electrical Characteristics: 12 V

Unless otherwise specified, all limits are specified for  $T_J = 25^{\circ}C$ ,  $V^+ = 12$  V,  $V^- = 0$  V,  $V_{CM} = V_O = V^+/2$ , and  $R_L = 100$  k $\Omega$  to  $V^+/2$ . (1)

	PARAMETER	TEST C	ONDITIONS	MIN <sup>(2)</sup>	TYP (3)	MAX (2)	UNIT
V	Input offeet veltege	T <sub>J</sub> = 25°C			±0.2	±3	mV
Vos	Input offset voltage	$T_J = -40$ °C to 85°C				±3.8	IIIV
TC \/	land offer to the second of (4)	$T_J = 25^{\circ}C$			±0.3		\//00
IC V <sub>OS</sub>	Input offset voltage drift (4)	$T_J = -40$ °C to 85°C				±15	μV/°C
		V 05V	T <sub>J</sub> = 25°C	-1000	-320		
	Input bias current <sup>(5)</sup>	$V_{CM} = 0.5 \text{ V}$	$T_J = -40$ °C to 85°C	-1600			рА
IB		V <sub>CM</sub> = 11.5 V	T <sub>J</sub> = 25°C		110	800	
			$T_J = -40$ °C to 85°C			1900	
Ios	Input offset current				±10		рА
		V <sub>CM</sub> Stepped from	T <sub>J</sub> = 25°C	75	115		
		0 V to 6 V	$T_J = -40$ °C to 85°C	70			
CMDD	O	V <sub>CM</sub> Stepped from	T <sub>J</sub> = 25°C	75	110		٦D
CMRR	Common mode rejection ratio	11.4 V to 12 V	$T_J = -40$ °C to 85°C	68			dB
		V <sub>CM</sub> Stepped from 0.5 V to 11.5 V	$T_J = 25^{\circ}C$	70	97		
			$T_J = -40$ °C to 85°C	65			

<sup>(1)</sup> Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

<sup>(7)</sup> Slew rate is the average of the rising and falling slew rates.

<sup>(2)</sup> Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.

<sup>3)</sup> Typical values represent the most likely parametric norm at the time of characterization.

<sup>(4)</sup> Offset voltage drift is specified by design and/or characterization and is not tested in production. Offset voltage drift is determined by dividing the change in VOS at temperature extremes into the total temperature change.

<sup>(5)</sup> Positive current corresponds to current flowing into the device.



## **Electrical Characteristics: 12 V (continued)**

Unless otherwise specified, all limits are specified for  $T_J = 25^{\circ}C$ ,  $V^+ = 12$  V,  $V^- = 0$  V,  $V_{CM} = V_O = V^+/2$ , and  $R_L = 100$  k $\Omega$  to  $V^+/2$ .

PARAMETER		TEST CO	NDITIONS	MIN <sup>(2)</sup>	TYP (3)	MAX <sup>(2)</sup>	UNIT	
		$V^+ = 2.7 \text{ V to 5 V},$	$T_J = 25^{\circ}C$	72	114			
		$V_{CM} = 0.5 V$	$T_J = -40$ °C to 85°C	68				
DCDD	Dower cumply rejection ratio	$V^{+} = 3 V \text{ to } 5 V,$	T <sub>J</sub> = 25°C	76	115			
PSRR	Power supply rejection ratio	$V_{CM} = 0.5 \text{ V}$	$T_J = -40$ °C to 85°C	72				
		V <sup>+</sup> = 5 V to 12 V,	$T_J = 25^{\circ}C$	84	117			
		$V_{CM} = 0.5 \text{ V}$	$T_J = -40$ °C to 85°C	80				
CMVR	Input common-mode voltage	CMRR ≥ 50 dB	$T_J = 25^{\circ}C$	-0.1		12.1	V	
CIVIVR	input common-mode voitage	CIVIRR 2 50 QB	$T_J = -40$ °C to 85°C	0		12	V	
		Sinking V = 0.5 V	$T_J = 25^{\circ}C$	89	110			
۸	Large signal voltage gain	Sinking, $V_0 = 0.5 \text{ V}$	$T_J = -40$ °C to 85°C	84			dB	
A <sub>VOL</sub>		Sourcing, V <sub>O</sub> = 11.5 V	$T_J = 25^{\circ}C$	89	110			
			$T_J = -40$ °C to 85°C	84				
	Output swing high	V <sub>ID</sub> = 100 mV	$T_J = 25^{\circ}C$	11.8	11.85		V	
V		V <sub>ID</sub> = 100 IIIV	$T_J = -40$ °C to 85°C	11.72			V	
Vo	Output swing low	V <sub>ID</sub> = −100 mV	$T_J = 25^{\circ}C$		150	200	mV	
		VID = -100 111V			280	IIIV		
	(6)	Sourcing V <sub>ID</sub> = 100 mV		-650	-200	4		
I <sub>SC</sub>	Output short circuit current (6)	Sinking V <sub>ID</sub> = −100 mV		200	1300		μΑ	
	Complex assument	T <sub>J</sub> = 25°C			1.2	1.75		
I <sub>S</sub>	Supply current	$T_J = -40$ °C to 85°C				2.5	μA	
CD	Slew rate <sup>(7)</sup>	A 1/	5.25	7		\//		
SR	Siew rate (**)	$A_V = 1$ , $V_O$ ramped from	3.1			V/ms		
GBW	Gain bandwidth product	$R_L = 1 \text{ M}\Omega$ , $C_L = 50 \text{ pF}$		25		kHz		
	Phase margin	$R_L = 1 \text{ M}\Omega$ , $C_L = 50 \text{ pF}$		52		0		
e <sub>n</sub>	Input-referred voltage noise	f = 100 Hz			320		nV/√ <del>Hz</del>	
;	Input-referred current noise	f = 10 Hz		0.02		pA/√ <del>Hz</del>		
i <sub>n</sub>	input-referred current noise	f = 1 kHz			0.01		pA/ VHZ	

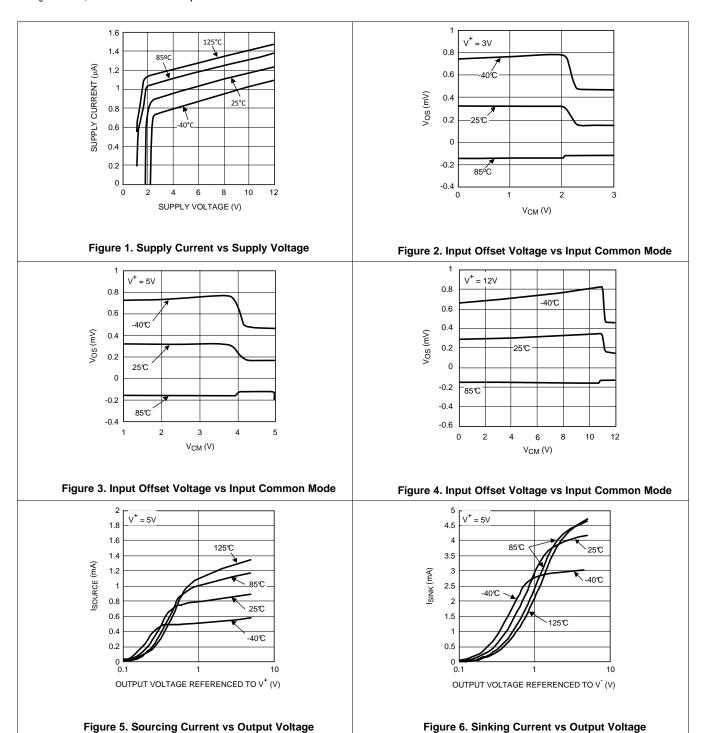
<sup>(6)</sup> The Short-Circuit Test is a momentary test. See Note 3 in *Absolute Maximum Ratings*.

<sup>(7)</sup> Slew rate is the average of the rising and falling slew rates.



### 6.8 Typical Characteristics

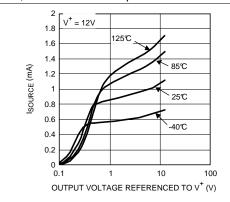
At  $T_J = 25$ °C, unless otherwise specified.



# TEXAS INSTRUMENTS

### **Typical Characteristics (continued)**

At  $T_J = 25$ °C, unless otherwise specified.



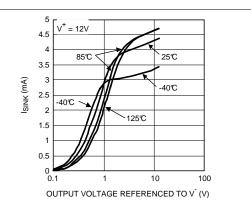
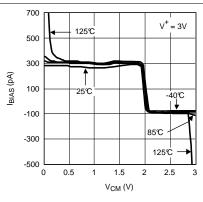


Figure 7. Sourcing Current vs Output Voltage

Figure 8. Sinking Current vs Output Voltage



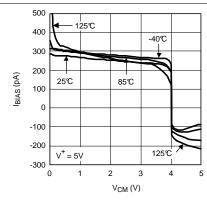
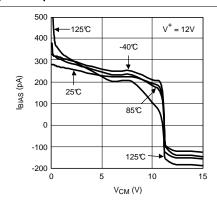


Figure 9. Input Bias Current vs Common Mode Voltage

Figure 10. Input Bias Current vs Common Mode Voltage



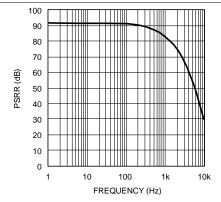


Figure 11. Input Bias Current vs Common Mode Voltage

Figure 12. PSRR vs Frequency



### **Typical Characteristics (continued)**

At  $T_J = 25$ °C, unless otherwise specified.

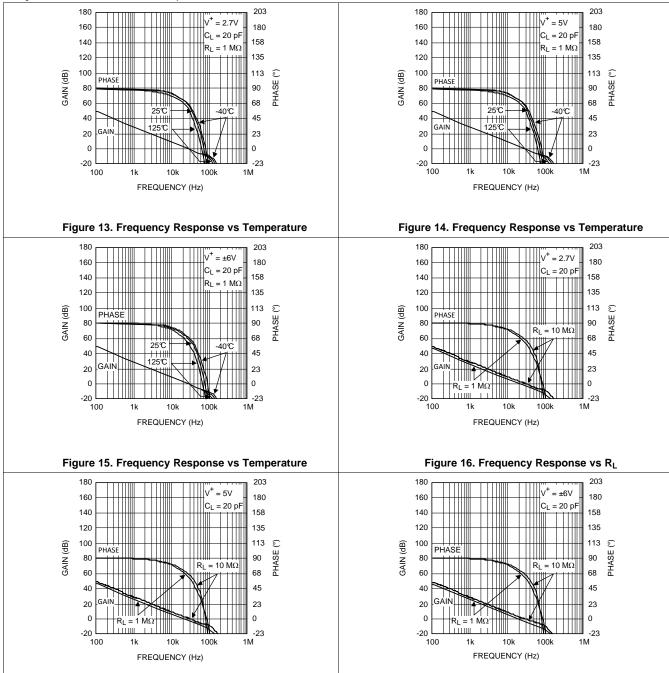


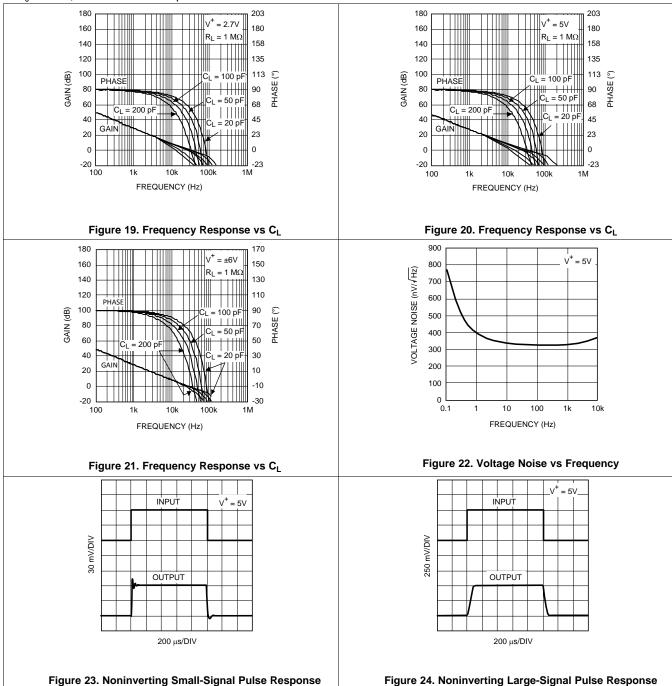
Figure 17. Frequency Response vs R<sub>L</sub>

Figure 18. Frequency Response vs R<sub>L</sub>



### **Typical Characteristics (continued)**

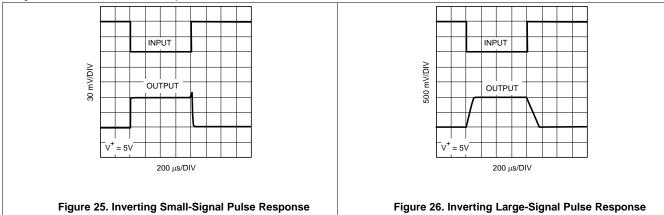
At  $T_J = 25$ °C, unless otherwise specified.





# **Typical Characteristics (continued)**

At  $T_J = 25$ °C, unless otherwise specified.



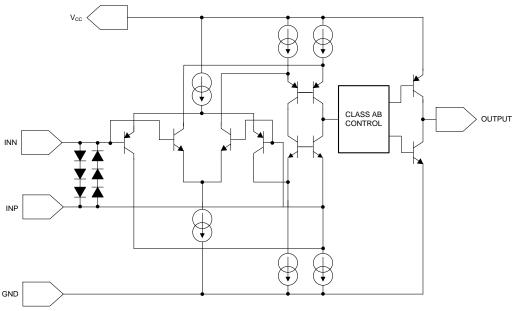


### 7 Detailed Description

#### 7.1 Overview

The LPV511 is a micropower operational amplifier that operates from a voltage supply range as wide as 2.7 V to 12 V with ensured specifications at 3 V, 5 V, and 12 V. The LPV511 exhibits an excellent speed-to-power ratio, drawing only 880 nA of supply current with a bandwidth of 27 kHz.

#### 7.2 Functional Block Diagram



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### 7.3 Feature Description

The LPV511 has a rail-to-rail input which provides more flexibility for the system designer. As can be seen from *Functional Block Diagram*, rail-to-rail input is achieved by using in parallel, one PNP differential pair and one NPN differential pair. When the common mode input voltage  $(V_{CM})$  is near  $V^+$ , the NPN pair is on and the PNP pair is off. When  $V_{CM}$  is near  $V^-$ , the NPN pair is off and the PNP pair is on. When  $V_{CM}$  is between  $V^+$  and  $V^-$ , internal logic decides how much current each differential pair will get. This special logic ensures stable and low distortion amplifier operation within the entire common mode voltage range.

#### 7.4 Device Functional Modes

#### 7.4.1 Input Stage

Because both input stages have their own offset voltage ( $V_{OS}$ ) characteristic, the offset voltage of the LPV511 becomes a function of  $V_{CM}$ .  $V_{OS}$  has a crossover point at 1 V below V<sup>+</sup>. See the  $V_{OS}$  vs  $V_{CM}$  curve in *Typical Characteristics*. Caution must be taken in situations where the input signal amplitude is comparable to the  $V_{OS}$  value and/or the design requires high accuracy. In these situations, it is necessary for the input signal to avoid the crossover point.

The input bias current,  $I_B$  will change in value and polarity as the input crosses the transition region. In addition, parameters such as PSRR and CMRR which involve the input offset voltage will also be affected by changes in  $V_{CM}$  across the differential pair transition region.

Differential input voltage is the difference in voltage between the noninverting (+) input and the inverting input (-) of the op amp. Due to the three series diodes across the two inputs, the absolute maximum differential input voltage is ±2.1 V. This may not be a problem to most conventional op amp designs; however, designers **must avoid using the LPV511 as a comparator**.



#### **Device Functional Modes (continued)**

#### 7.4.2 Output Stage

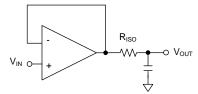
The LPV511 output voltage swing 100 mV from rails at 3-V supply, which provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The LPV511 maximum output voltage swing defines the maximum swing possible under a particular output load. The LPV511 output swings 110 mV from the rail at 5-V supply with an output load of 100 k $\Omega$ .

### 7.4.3 Driving Capacitive Load

The LPV511 is internally compensated for stable unity gain operation, with a 27-kHz typical gain bandwidth. However, the unity gain follower is the most sensitive configuration to capacitive load. Direct capacitive loading reduces the phase margin of the op amp. When the output is required to drive a large capacitive load, greater than 100 pF, a small series resistor at the output of the amplifier improves the phase margin (see Figure 27).

In Figure 27, the isolation resistor  $R_{ISO}$  and the load capacitor  $C_L$  form a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of  $R_{ISO}$ . The bigger the  $R_{ISO}$  resistor value, the more stable  $V_{OUT}$  will be. But the DC accuracy is degraded when the  $R_{ISO}$  gets bigger. If there were a load resistor in Figure 27, the output voltage would be divided by  $R_{ISO}$  and the load resistor.



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Figure 27. Resistive Isolation of Capacitive Load

Product Folder Links: LPV511



### Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

#### 8.1 Application Information

The LPV511 is fabricated with Texas Instrument's state-of-the-art VIP50C process.

### 8.2 Typical Applications

### 8.2.1 Battery Current Sensing

The rail-to-rail common mode input range and the very low guiescent current make the LPV511 ideal to use in high-side and low-side battery current sensing applications. The high-side current sensing circuit in Figure 28 is commonly used in a battery charger to monitor the charging current to prevent over charging. A sense resistor R<sub>SENSE</sub> is connected to the battery directly.

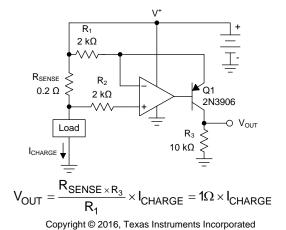


Figure 28. High Side Current Sensing

### 8.2.1.1 Design Requirements

The high-side current-sensing circuit (Figure 28) is commonly used in a battery charger to monitor charging current to prevent overcharging. A sense resistor RSENSE is connected to the battery directly. This system requires an op amp with rail-to-rail input. The LPV511 ideal for this application because its common-mode input range extends up to the positive supply.

#### 8.2.1.2 Detailed Design Procedure

As seen in Figure 28, the I<sub>CHARGE</sub> current flowing through sense resistor R<sub>SENSE</sub> develops a voltage drop equal to V<sub>SENSE</sub>. The voltage at the negative sense point will now be less than the positive sense point by an amount proportional to the V<sub>SENSE</sub> voltage.

The low-bias currents of the LPV511 cause little voltage drop through R2, so the negative input of the LPV551 amplifier is at essentially the same potential as the negative sense input.

The LPV511 will detect this voltage error between its inputs and servo the transistor base to conduct more current through Q1, increasing the voltage drop across R1 until the LPV511 inverting input matches the noninverting input. At this point, the voltage drop across R<sub>1</sub> now matches V<sub>SENSE</sub>.

I<sub>G</sub>, a current proportional to I<sub>CHARGE</sub>, will flow according to the following relation to:

$$I_{G} = V_{RSENSE} / R_{1} = (R_{SENSE} \times I_{CHARGE}) / R_{1}$$

$$\tag{1}$$

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### **Typical Applications (continued)**

I<sub>G</sub> also flows through the gain resistor R<sub>3</sub> developing a voltage drop equal to:

$$V_3 = I_G \times R_3 = (V_{RSENSE} / R_1) \times R_3 = ((R_{SENSE} \times I_{CHARGE}) / R_2) \times R_3$$

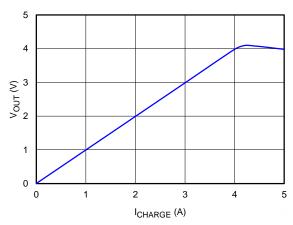
$$V_{OUT} = (R_{SENSE} \times I_{CHARGE}) \times G$$
(2)

where

$$\bullet \quad G = R_3 / R_1 \tag{3}$$

#### 8.2.1.3 Application Curve

Figure 29 shows the results of the example current sense circuit.



The error after 4 V where transistor Q1 runs out of headroom and saturates, limiting the upper output swing.

Figure 29. Current Sense Amplifier Results

#### 8.2.2 Summing Amplifier

The LPV511 operational amplifier is a perfect fit in a summing amplifier circuit because of the rail-to-rail input and output and the sub-micro Amp quiescent current. In this configuration, the amplifier outputs the sum of the three input voltages.

Equation 4 shows the ratio of the sum and the output voltage is defined using feedback and input resistors.

$$V_{OUT} = R_F \left( \frac{V_{REF} - V_1}{R_1} + \frac{V_{REF} - V_2}{R_2} + \frac{V_{REF} - V_3}{R_3} \right) + V_{REF}$$

$$(4)$$

$$V_1 \circ W_1 \circ W_2 \circ W_3 \circ W_4 \circ V_{OUT}$$

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Figure 30. Summing Amplifier Circuit

#### 8.3 Dos and Don'ts

Do properly bypass the power supplies.

Do add series resistence to the output when driving capacitive loads, particularly cables, Muxes and ADC inputs.

Do add series current limiting resistors and external Schottky clamp diodes if input voltage is expected to exceed the supplies. Limit the current to 1 mA or less (1  $k\Omega$  per volt).

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### 9 Power Supply Recommendations

The LPV80x is specified for operation from 1.6 V to 5.5 V (±0.8 V to ±2.75 V) over a -40°C to 125°C temperature range. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Electrical Characteristics: 3 V*.

#### **CAUTION**

Supply voltages larger than 13.2 V can permanently damage the device.

For proper operation, the power supplies bust be properly decoupled. For decoupling the supply lines it is suggested that 100 nF capacitors be placed as close as possible to the operational amplifier power supply pins. For single supply, place a capacitor between V<sup>+</sup> and V<sup>-</sup> supply leads. For dual supplies, place one capacitor between V<sup>+</sup> and ground, and one capacitor between V<sup>-</sup> and ground.

Low bandwidth nanopower devices do not have good high frequency (> 1 kHz) AC PSRR rejection against high-frequency switching supplies and other 1 kHz and above noise sources, so extra supply filtering is recommended if kilohertz or above noise is expected on the power supply lines.

### 10 Layout

### 10.1 Layout Guidelines

- The V<sup>+</sup> pin should be bypassed to ground with a low-ESR capacitor.
- The optimum placement is closest to the V<sup>+</sup> and ground pins.
- Take care to minimize the loop area formed by the bypass capacitor connection between V<sup>+</sup> and ground.
- The ground pin should be connected to the PCB ground plane at the pin of the device.
- The feedback components should be placed as close to the device as possible minimizing strays.

#### 10.2 Layout Example

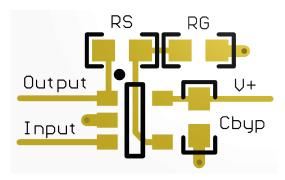


Figure 31. SOT-23 Layout Example



### 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Development Support

LPV511 PSPICE Model, http://www.ti.com/lit/zip/snom023

TINA-TI SPICE-Based Analog Simulation Program, http://www.ti.com/tool/tina-ti

DIP Adapter Evaluation Module, http://www.ti.com/tool/dip-adapter-evm

TI Universal Operational Amplifier Evaluation Module, http://www.ti.com/tool/opampevm

TI Filterpro Software, http://www.ti.com/tool/filterpro

### 11.2 Documentation Support

#### 11.2.1 Related Documentation

- Handbook of Operational Amplifier Applications (SBOA092)
- Compensate Transimpedance Amplifiers Intuitively (SBOA055)
- Circuit Board Layout Techniques (SLOA089)
- AN-1803 Design Considerations for a Transimpedance Amplifier (SNOA515)

### 11.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 11.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

#### 11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

#### 11.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: LPV511

www.ti.com 10-Nov-2025

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
LPV511MG/NOPB	Active	Production	SC70 (DCK)   5	1000   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A91
LPV511MG/NOPB.A	Active	Production	SC70 (DCK)   5	1000   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A91
LPV511MGX/NOPB	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A91
LPV511MGX/NOPB.A	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A91

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 5-Sep-2025

### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LPV511MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LPV511MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

**PACKAGE MATERIALS INFORMATION** 

www.ti.com 5-Sep-2025



### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LPV511MG/NOPB	SC70	DCK	5	1000	208.0	191.0	35.0
LPV511MGX/NOPB	SC70	DCK	5	3000	208.0	191.0	35.0



SMALL OUTLINE TRANSISTOR



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
  3. Reference JEDEC MO-203.

- 4. Support pin may differ or may not be present.5. Lead width does not comply with JEDEC.
- 6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 10. Board assembly site may have different recommendations for stencil design.



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