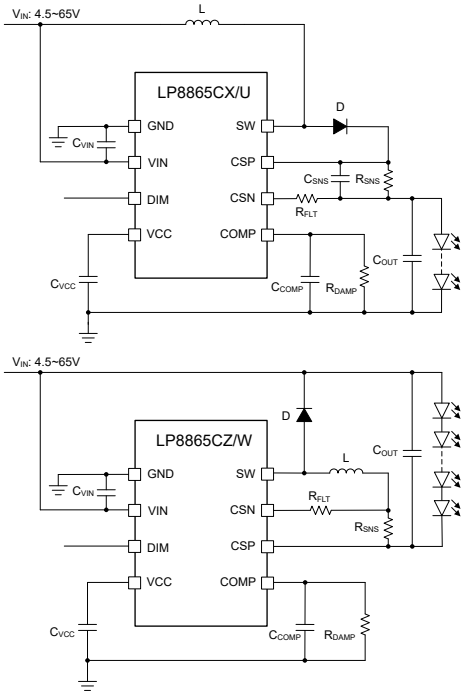
LP8865C-Q1 Low Cost Automotive Multi-Topology LED Driver

1 Features

- AEC-Q100 Qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Integrated MOSFET for buck, buck-boost and boost topology
  - Wide input voltage: 4.5V to 65V
  - Integrated typical 2.8A and 300mΩ MOSFET
  - 400kHz fixed switching frequency
- High precision power FET dimming
  - Analog dimming for U/V/W version
  - Fast PWM dimming for X/Y/Z version
- Full protection features:
  - LED open and short protection
  - Cycle-by-cycle current limit
  - Switching FET failure protection
  - Thermal shutdown

2 Applications

- Automotive infotainment
- Automotive instrument clusters
- Heads-up displays(HUD)
- Automotive lighting



Typical LED Driver Application Schematic

3 Description

The LP8865C-Q1 family is a low cost non-synchronous multi-topology solution with 4.5V to 65V wide input range. By integrating the low-side NMOS switch, the device is capable of driving LEDs with high power density and high efficiency. The family also supports common cathode connection and single layer PCB design. The switching frequency is fixed with 400kHz.

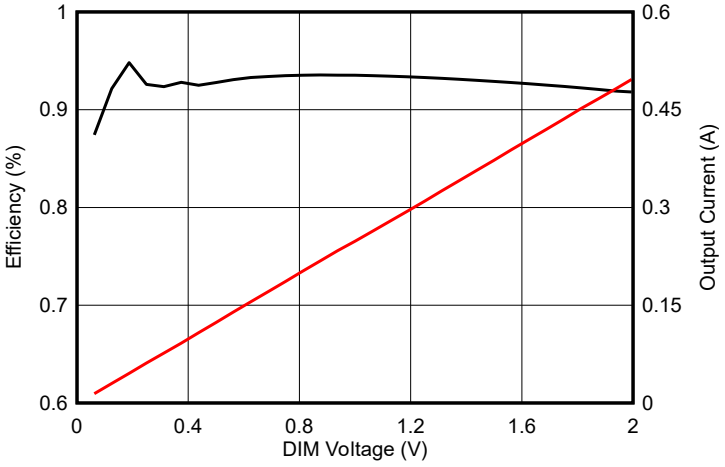
The LP8865C-Q1 family support PWM dimming by configuring through the DIM input pins by means of simple high and low signals or analog dimming by configuring through the DIM input pins by means of analog voltage signals. The device adopts an adaptive off-time current mode control along with smart and accurate sampling to enable fast PWM dimming and achieve high-dimming ratio.

The LP8865C-Q1 family also provides multiple systematic protections, including LED open and short, switching FET open and short, sense resistor open and short, and thermal shutdown.

Package Information

PART NUMBER	PACKAGE1	BODY SIZE (NOM)
LP8865C-Q1	HVSSOP (8)	3.0mm x 3.0mm

1. For all available packages, see the orderable addendum at the end of the data sheet.



Dimming Linearity and Efficiency

Table of Contents

4 Comparison Table

Part Number	Topology	Dimming Mode	Switching Frequency
LP8865CXQDGNRQ1	Boost	PWM Dimming	400kHz
LP8865CYQDGNRQ1	Buck-boost	PWM Dimming	400kHz
LP8865CZQDGNRQ1	Buck	PWM Dimming	400kHz
LP8865CUQDGNRQ1	Boost	Analog Dimming	400kHz
LP8865CVQDGNRQ1	Buck-boost	Analog Dimming	400kHz
LP8865CWQDGNRQ1	Buck	Analog Dimming	400kHz

5 Pin Configuration and Functions

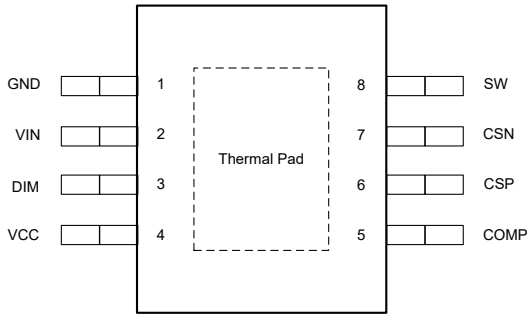


Figure 5-1. 8-Pin Buck HVSSOP Top View

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
No.	NAME		
1	GND	G	Ground pin.
2	VIN	P	Input power pin.
3	DIM	I	PWM dimming pin for X/Y/Z. Input PWM signal for PWM dimming. Analog dimming pin for U/V/W. Input analog signal for analog dimming.
4	VCC	P	Internal LDO output pin. Connect with a 16V, 1µF capacitor to GND.
5	COMP	I/O	Error-amilifier output. Connect capacitors to GND. Different capacitor values determine different softstart times and bandwidths.
6	CSP	I	LED current sense positive pin.
7	CSN	I	LED current sense negative pin.
8	SW	P	Switching node pin. Internally connected to the low-side MOSFET. Connect with the power inductor and the schottky diode.
Pad	Thermal Pad	NC	No connection.

1. I = Input, O = Output, P = Supply, G = Ground

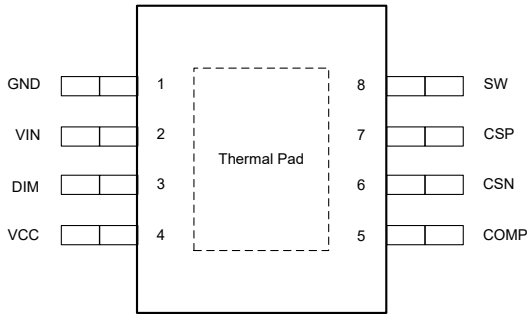


Figure 5-2. 8-Pin Boost/Buck-Boost HVSSOP Top View

Table 5-2. Pin Functions for boost/buck-boost topology

PIN		TYPE(1)	DESCRIPTION
VSON Package	NAME		
1	GND	G	Ground pin.
2	VIN	P	Input power pin.
3	DIM	I	PWM dimming pin for X/Y/Z. Input PWM signal for PWM dimming. Analog dimming pin for U/V/W. Input analog signal for analog dimming.
4	VCC	P	Internal LDO output pin. Connect with a 16V, 1µF capacitor to GND.
5	COMP	I/O	Error-amilifier output. Connect capacitors to GND. Different capacitor values determine different softstart times and bandwidths.
6	CSN	I	LED current sense negative pin.
7	CSP	I	LED current sense positive pin.
8	SW	P	Switching node pin. Internally connected to the low-side MOSFET. Connect with the power inductor and the schottky diode.
Pad	Thermal Pad	NC	No connection.

(1) I = Input, O = Output, P = Supply, G = Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage on pins VIN, CSP, CSN, SW		–0.3	65	V
Voltage on pins VCC, DIM, COMP		–0.3	5.5	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD classification level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C2a	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Supply voltage range	4.5	63	V
V_{SW}	Switching node voltage range	0	63	V
V_{CSP}, V_{CSN}	Sense common-mode voltage range	0	63	V
V_{VCC}	LDO output voltage range	0	5.3	V
V_{DIM}	Dimming voltage range	0	5	V
V_{COMP}	Compensation capacitor voltage range	0	5	V
T_A	Operating ambient temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LP8865C-Q1 HVSSOP 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics*application report, SPRA953.

6.5 Electrical Characteristics

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containingit. T_A = –40°C to +125°C, V_{IN} = 7V, (unlessotherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{VIN_UVLO}	V_{IN} undervoltage lockout	Rising V_{IN}	3.0	3.2	3.4	V
		Falling V_{IN}	2.8	3.0	3.2	V
	Hysteresis			0.2		V
I_{OFF}	PWM off quiesent current from V_{IN}	V_{DIM} = 0V, device enabled		1.0	1.3	mA
V_{VCC}	Internal LDO output voltage	I_{VCC} = 5mA	5.0	5.15	5.3	V
I_{VCC_LIM}	Internal LDO output current limit		15	20	26	mA
DIMMING						
V_{PWM_L}	DIM low-level input voltage (X/Y/Z version)				0.4	V
V_{PWM_H}	DIM high-level input voltage (X/Y/Z version)		1.2			V
$t_{PWM\_OUT\_ON}$	PWM output minimum on time (Z version)	Guaranteed by design			100	ns
$t_{PWM\_IN\_ON}$	PWM input minimum on time (Z version)	Guaranteed by design			100	ns
V_{ADIM}	DIM input voltage range (U/V/W version)		0		2.2	V
FEEDBACK AND ERROR AMPLIFIER						
$g_{M(ea)}$	Transconductance gain	V_{DIM} = 2V, $V_{CSP-CSN}$ = 200mV	205	265	325	µA/V
I_{COMP}	Source/sink current	V_{DIM} = 2V, $V_{CSP-CSN}$ = 200mV ± 200mV	±24	±40	±56	µA
V_{REF}	CSP-CSN pin voltage	V_{DIM} = 2V	191	200	209	mV
V_{REF}	CSP-CSN pin voltage	V_{DIM} = 0.2V	18.5	20	21.5	mV
$I_{LEAK\_CSP/N}$	CSP+CSN pin leakage current(Z/W Version)	V_{IN} = 60V, V_{DIM} = 2V			48	µA
$I_{LEAK\_CSP/N}$	CSP+CSN pin leakage current(Z/W Version)	V_{IN} = 60V, V_{DIM} = 0V			15	µA
$I_{LEAK\_CSP/N}$	CSP+CSN pin leakage current(X/Y/U/V Version)	V_{IN} = 60V, V_{DIM} = 2V			183	µA
$I_{LEAK\_CSP/N}$	CSP+CSN pin leakage current(X/Y/U/V Version)	V_{IN} = 60V, V_{DIM} = 0V			164	µA
POWER STAGE						
R_{DSON}	Switching FET on resistance	V_{IN} ≥ 5V		300		mΩ
t_{min_ON}	Switching FET minimum on time			140	160	ns
t_{min_OFF}	Switching FET minimum off time			140	160	ns
f_{SW}	Switching FET frequency		370	400	430	kHz
CURRENT LIMIT						
I_{LIM}	Switching FET cycle-by-cycle current limit (TPS922051)		2.8	3.2	3.6	A
THERMAL PROTECTION						
T_{TSD}	Thermal shutdown temperature			165		°C
	Hysteresis			15		°C

6.6 Typical Characteristics

V_{IN} = 12 V, LED count = 12, L = 33 µH, F_{SW} = 400 kHz, unless otherwise specified

6.6 Typical Characteristics (continued)

Figure 6-1. PWM Duty Cycle vs. CSP-CSN Voltage at 20kHz PWM

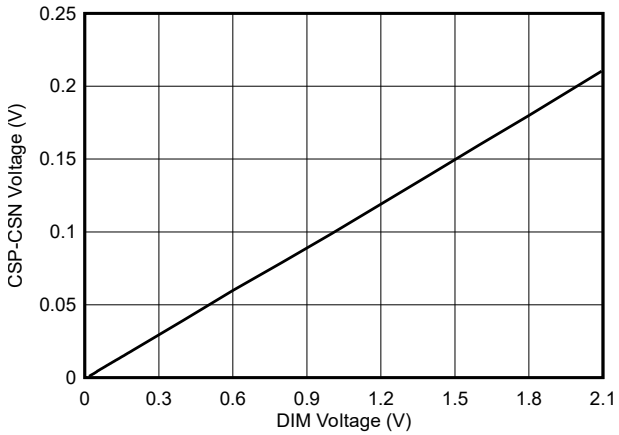


Figure 6-2. Analog Voltage vs. CSP-CSN Voltage

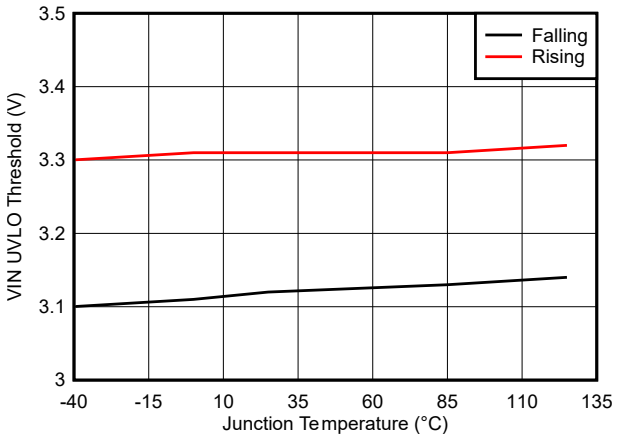


Figure 6-3. VIN UVLO Threshold vs. Junction Temperature

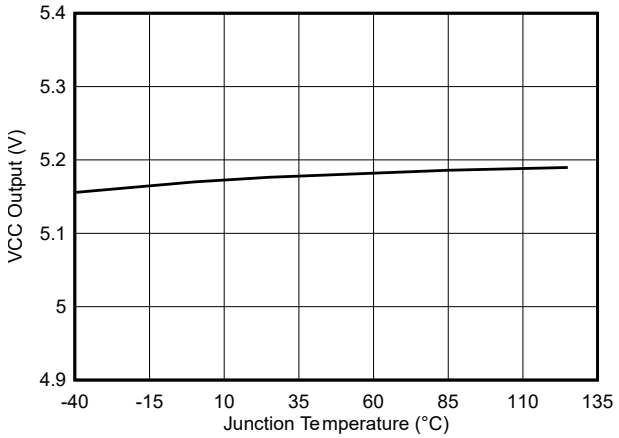


Figure 6-4. Internal LDO Output vs. Junction Temperature

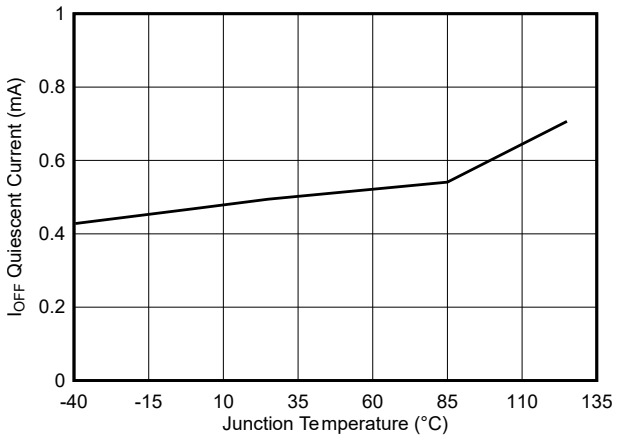


Figure 6-5. VIN Quiescent Current vs. Junction Temperature

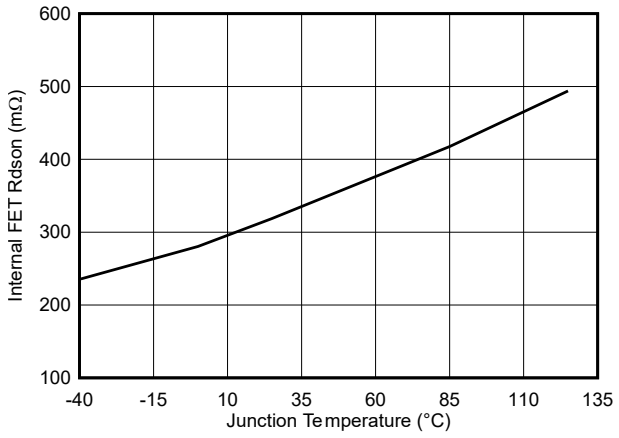


Figure 6-6. Switching FET Rdson vs. Junction Temperature

6.6 Typical Characteristics (continued)

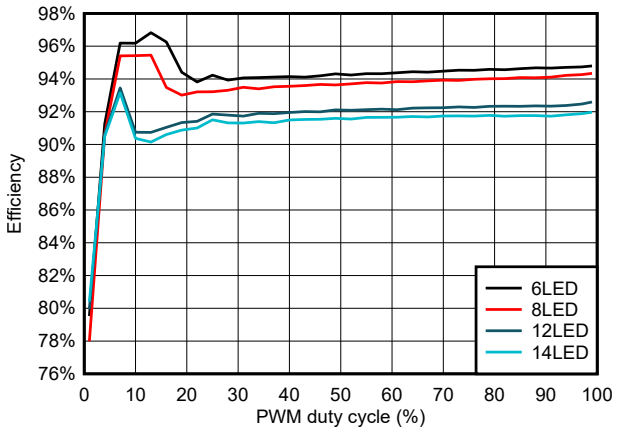


Figure 6-7. Boost PWM Dimming Efficiency at 13V Input Voltage, 0.5A Output Current, 20kHz PWM

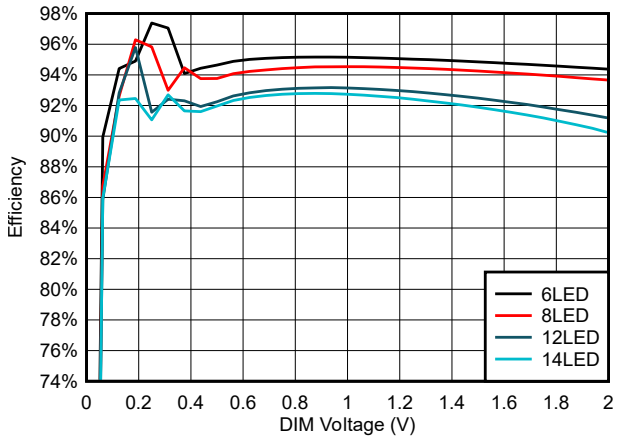


Figure 6-8. Boost Analog Dimming Efficiency at 13V Input Voltage, 0.5A Output Current

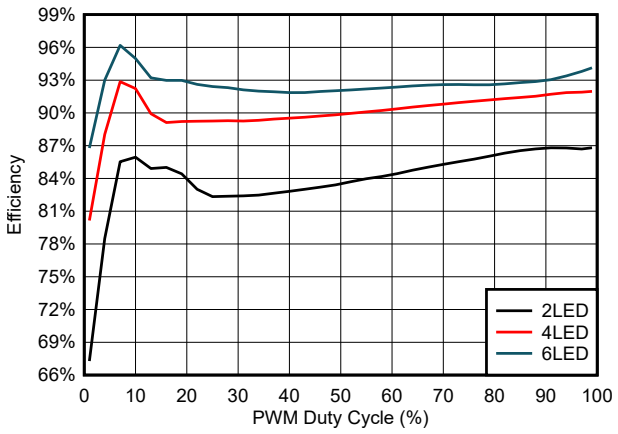


Figure 6-9. Buck PWM Dimming Efficiency at 24V Input Voltage, 2A Output Current, 20kHz PWM

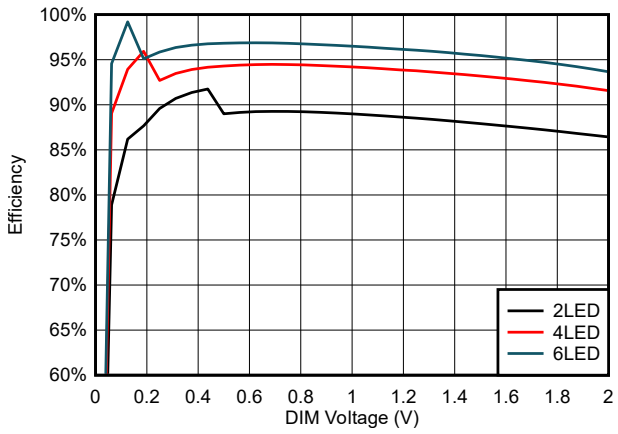


Figure 6-10. Buck Analog Dimming Efficiency at 24V Input Voltage, 2A Output Current

7 Detailed Description

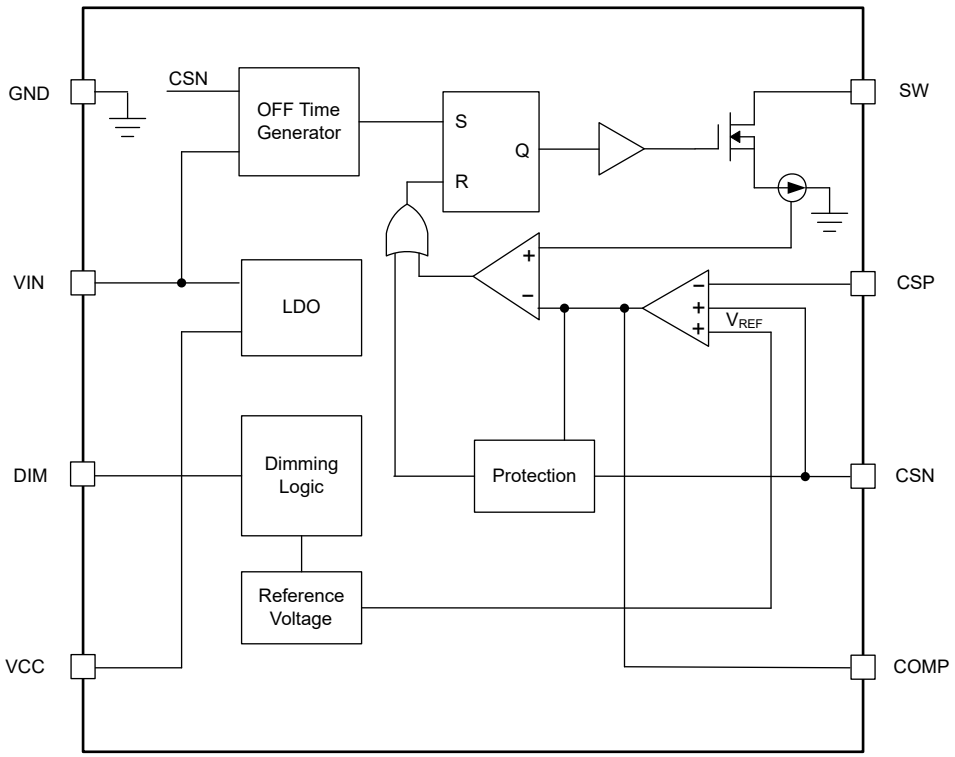
7.1 Overview

The LP8865C-Q1 family is a low cost non-synchronous multi-topology solution with 4.5V to 65V wide input range. By integrating the low-side NMOS switch, the device is capable of driving LEDs with high power density and high efficiency. The family also supports common cathode connection and single layer PCB design. The switching frequency is fixed with 400kHz.

The LP8865C-Q1XYZ option supports PWM dimming by configuring through the DIM input pins by means of simple high and low signals. The LP8865C-Q1U/V/W option supports analog dimming by configuring through the DIM input pins by means of analog voltage signals. The device adopts an adaptive off-time current mode control along with smart and accurate sampling to enable fast PWM dimming and achieve high dimming ratio.

The LP8865C-Q1 family also provides multiple systematic protections, including LED open and short, switching FET open and short, sense resistor open and short, and thermal shutdown.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adaptive Off-Time Current Mode Control

The LP8865C-Q1 family adopts an adaptive off-time current mode control to support fast transient response over a wide range of operation. The switching frequency is set at 400kHz.

For average output current regulation, the sensed voltage across the sensing resistor between the CSP and CSN pins is compared with the internal voltage reference, V_{REF} , through the error amplifier. The output of the error amplifier, V_{COMP}, passes through an external compensation network and is then compared with the peak current feedback at the PWM comparator. During each switching cycle, when the internal NMOS FET is turned on, the peak current is sensed through the internal FET. When the sensed value of peak current reaches V_{COMP} at the input of PWM comparator, the NMOS FET is turned off and the adaptive off-time counter starts counting. Once the adaptive off-time counter stops counting, the counter is reset until when the NMOS FET stays off. The counting off time is determined by the external resistor connected to the FSET pin and the input/output feed forward. Thus, the device is able to maintain a nearly constant switching frequency at steady state and regulate the output average current at a desired value.

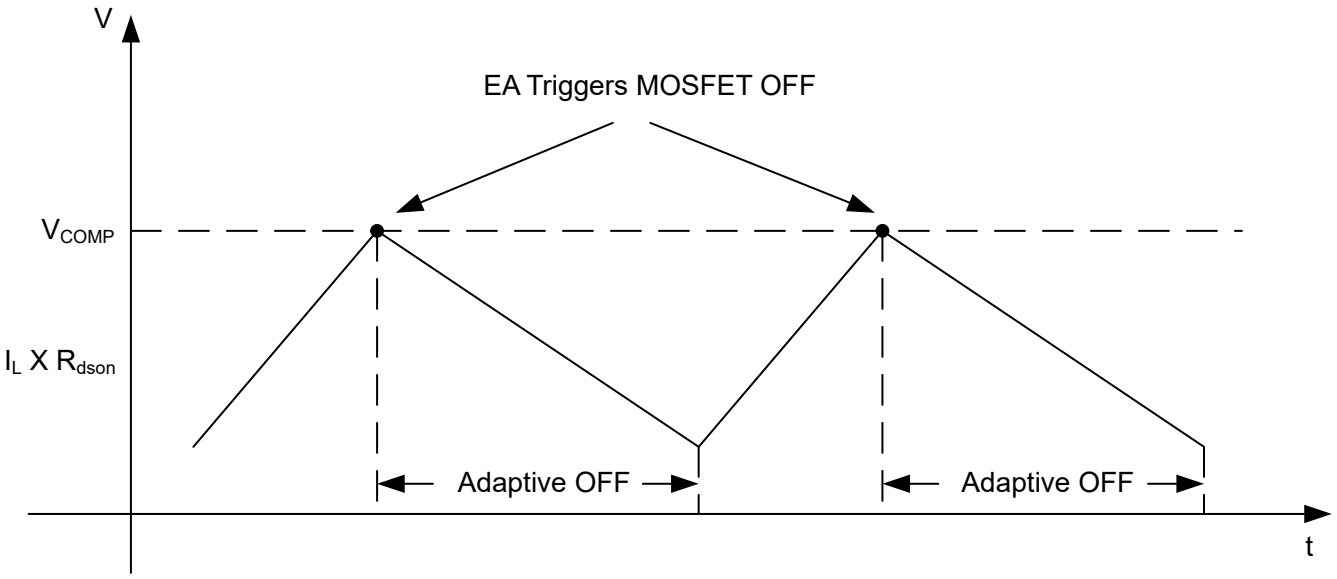


Figure 7-1. Adaptive Off-Time Current Mode Control Method

7.3.2 Setting LED Current

The output current of the LED is controlled with external resistor R_{sense} between CSP and CSN pins. R_{sense} value for the target current can be calculated using equation Equation 1. Noted that, to release IFD function and improve the accuracy of the output current in low duty cycle, the capacitor in parallel with sense resistor is required for boost and buck-boost topology. And it is optional for buck topology.

$$R_{SENSE} = \frac{V_{REF}}{I_{LED\_FS}} \quad (1)$$

where

- V_{REF} = 200mV
- R_{SENSE} is current setting resistor, mΩ
- I_{LED} is output current, A

For example, if R_{sense} is set to 100mΩ. I_{LED} will be 2A. A 100Ω R_{FLT} on CSN is needed to protect the CSP and CSN pin. An offset on V_{REF} need to be considered due to voltage drop on R_{FLT} with common-mode leakage current of CSP and CSN pins.

7.3.3 Internal Soft Start

The LP8865C-Q1 implements the internal soft-start function. Once VIN rises above V_{VIN_MIN}, the internal LDO starts to charge VCC capacitor. It takes approximately 800µs for VCC to rise above V_{VIN_UVLO} if a 1µF capacitor is connected to VCC pin. The POR is enabled right after VCC above V_{VIN_UVLO}. In this case, if using 1µF VCC capacitor, it is recommended to wait for 1ms to start dimming after VIN rises above V_{VIN_MIN}.

If DIM pin starts to rise or has the first PWM pulse appearing after VCC rises above V_{VIN_UVLO}, the device starts switching right away. For PWM dimming version, the initial PWM pulse can be as small as 50ns at DIM input pin to start dimming.

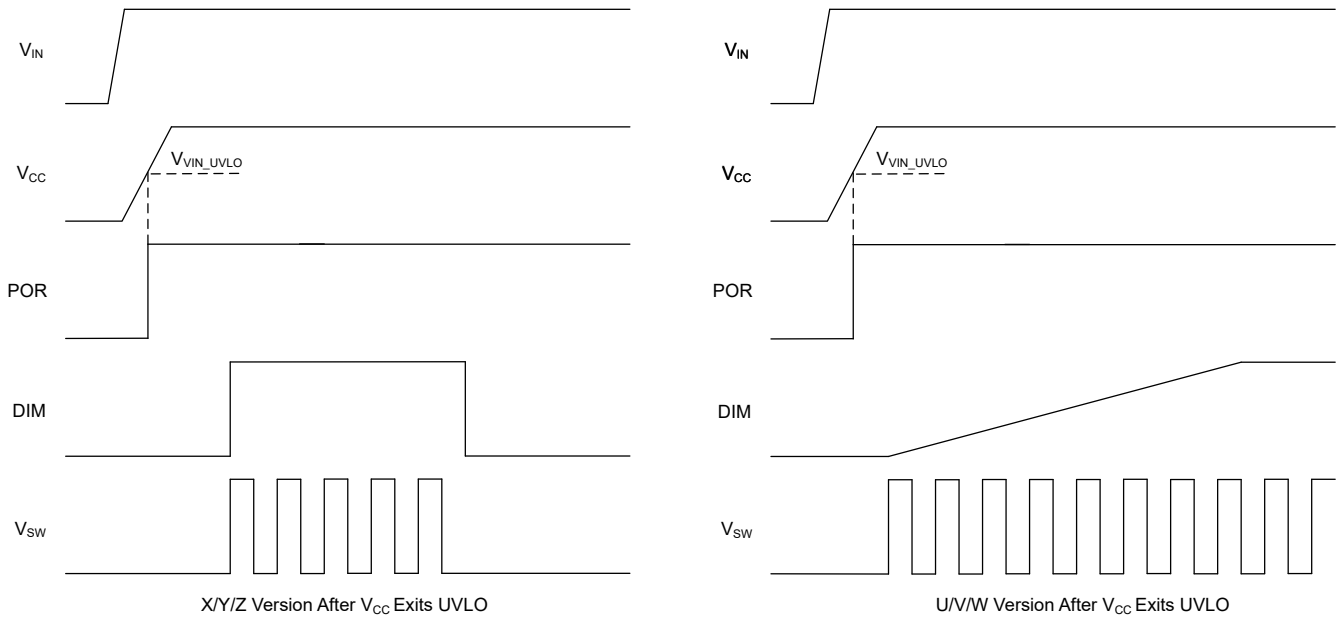


Figure 7-2. Startup Sequence

7.3.4 Dimming Mode

The LP8865C-Q1 X/Y/Z option supports PWM dimming mode. And LP8865C-Q1 U/V/W option supports analog dimming mode.

The configuration to dimming modes are shown as below:

Table 7-1. Dimming Mode Configuration

Dimming Mode	Part Number	DIM Pin
PWM Dimming	LP8865CX/Y/Z option	PWM signal
Analog Dimming	LP8865CU/V/W option	Analog signal

7.3.4.1 PWM dimming

The LP8865CX/Y/Z support PWM input signals with ultra narrow pulse width down to 50 ns for direct PWM dimming. The PWM dimming starts when the DIM input pin is configured by a PWM input signal.

When the PWM input signal at the DIM pin turns from low to high, the internal NMOS FET starts switching and the inductor current rises to the determined value set by sense resistor. The LED current is then regulated at the determined value as long as the PWM input signal stays high. When the PWM input signal turns from high to low, the internal FET is turned off causing the inductor current falling to zero. The internal FET maintains off and the LED current stays zero as long as the PWM input signal stays low.

7.3.4.2 Analog dimming

The LP8865CU/V/W support analog dimming which regulates the LED current through the analog input signal at the DIM pin.

The internal voltage reference, V_{REF}, starts to rise after the device exit UVLO. Once an analog voltage appears at the DIM pin, V_{REF} continues to increase until changing to the desired value in proportion to the analog voltage. V_{REF} is 200mV when the analog input signal at the DIM pin is 2V, for instance, and V_{REF} is 20mV when the analog input signal is 0.2V. V_{REF} is clamped at 220mV when the analog input signal at the DIM pin is higher than 2.2V. V_{REF} is 0V and the device stops switching when the analog input signal is lower than 10mV. The circuit is able to respond to the voltage change of the analog input signal with micro-seconds delay.

7.3.5 Fault Protection

The LP8865C-Q1 family is able to provide fault protections in many fault conditions, including LED open, LED short, LED short to GND, sense resistor open and short, internal switching FET open and short, and thermal shutdown. The fault criterion for different topology is shown in below.

Table 7-2. Protections in Buck topology

TYPE	CRITERION	BEHAVIOR
LED open load	V_{CSP} < 1V	The device keeps switching with minimum on time.
LED+ and LED- short circuit	V_{IN} - V_{CSP} < 100mV	The device keeps switching.
LED- short to GND	V_{CSP} < 1V for 100µs	The device keeps switching with minimum on time.
Sense-resistor open load	V_{CSP} - V_{CSN} > 300mV	The device stops switching and recovers when fault is removed.
Sense-resistor short circuit	COMP pin is clamped high	The device keeps switching under the cycle-by-cycle current limit.
Switching FET open	COMP pin is clamped high	The device keeps switching under the cycle-by-cycle current limit.
Switching FET short	V_{CSP} - V_{CSN} > 300mV	The device stops switching and recovers when fault is removed.
Thermal shutdown	T_J > T_{TSD}	The device stops switching and recovers when T_J falls below the hysteresis level.

Table 7-3. Protections in Boost / Buck-Boost topology

TYPE	CRITERION	BEHAVIOR
LED open load	V_{CSP} > 65 V	The device stops switching and recovers when fault is removed.
LED+ and LED- short circuit(Buck-Boost)	V_{CSN} - V_{IN} < 100 mV	The device keeps switching.
LED+ short to GND	V_{CSP} - V_{CSN} > 300 mV	The device stops switching and recovers when fault is removed.
Sense-resistor open load	V_{CSP} - V_{CSN} > 300mV	The device stops switching and recovers when fault is removed.
Sense-resistor short circuit	COMP pin is clamped high	The device keeps switching under the cycle-bycycle current limit.
Switching FET open	COMP pin is clamped high	The device keeps switching under the cycle-bycycle current limit.
Switching FET short	COMP pin is clamped high	The device keeps switching under the cycle-bycycle current limit.
Thermal shutdown	T_J > T_{TSD}	The device stops switching and recovers when T_J falls below the hysteresis level.

8 Application and Implementation

8.1 Application Information

LP8865C-Q1 can support buck / boost / buck-boost topology with different part number.

The LP8865C-Q1 X/U option is typically used as a boost converter, the LP8865C-Q1 Y/V option is typically used as a buck-boost converter and the LP8865C-Q1 Z/W option is typically used as a buck converter.

8.2 Typical Application

8.2.1 LP8865CUQDGNRQ1 12V Input, 1A Output, 8-piece WLED Driver With Analog Dimming

The LP8865CUQDGNRQ1 is typically used as a Boost converter with analog dimming to drive LEDs from an input from 4.5V to 63V range.

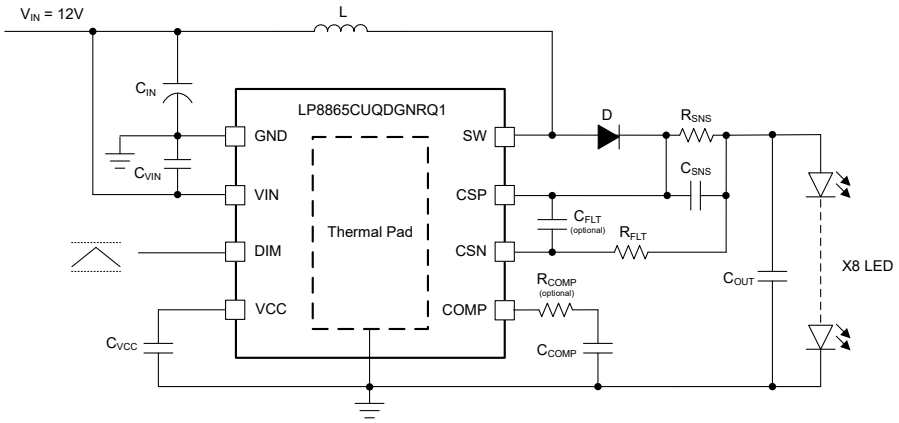


Figure 8-1. Typical Application for LP8865CUQDGNRQ1

8.2.1.1 Design Requirements

For this design example, use the parameters in the following table.

Table 8-1. Design Parameters

PARAMETER	VALUE
Input voltage	9V to 16V
LED string	8 LED
Output voltage	24V
Switching frequency	400kHz
Maximum LED current	0.5A
Inductor current ripple	40% of maximum inductor current
Dimming type	Analog version

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Inductor Selection

For this design, the input voltage is 9V to 16V. The output is 8 white LEDs in series and the inductor current ripple by requirement is less than 40% of maximum LED current. To choose a proper peak-to-peak inductor current ripple, the low-side FET current limit should not be violated when the converter works in no-load condition. This requires half of the peak-to-peak inductor current ripple to be lower than that limit. Another consideration is to ensure reasonable inductor core loss and copper loss caused by the peak-to-peak current ripple. Once this peak-to-peak inductor current ripple is chosen, use Equation 2 to calculate the recommended value of the inductor L.

$$L = \frac{V_{IN(min)} \times \left(V_{OUT} - V_{IN(min)}\right)}{V_{OUT} \times K_{IND} \times I_{L(max)} \times f_{SW}} \quad (2)$$

where

- K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum average LED current.
- $I_{L(max)}$ is the maximum average inductor current under minimum input voltage.
- f_{SW} is the switching frequency, 400kHz for this case.
- $V_{IN(min)}$ is the minimum input voltage.
- V_{OUT} is the sum of the voltage across LED load and the voltage across sense resistor.

With the chosen inductor value, the user can calculate the actual inductor current ripple using Equation 3.

$$I_{L(ripple)} = \frac{V_{IN(min)} \times \left(V_{OUT} - V_{IN(min)}\right)}{V_{OUT} \times L \times f_{SW}} \quad (3)$$

The design ratings of inductor RMS current and saturation current must be greater than those seen in the system requirement. This is to ensure no inductor overheat or saturation occurring. During power up, transient conditions or fault conditions, the inductor current may exceed its normal operating current and reach the current limit. Therefore, it is preferred to select a saturation current rating equal to or greater than the converter current limit. The peak-inductor-current and RMS current equations are shown in Equation 4 and Equation 5.

$$I_{L(peak)} = I_{L(max)} + \frac{I_{L(ripple)}}{2} \quad (4)$$

$$I_{L(rms)} = \sqrt{I_{L(max)}^{2} + \frac{I_{L(ripple)}^{2}}{2}} \quad (5)$$

In this design, $V_{IN(min)}$ = 9V, V_{OUT} = 24V, I_{LED} = 0.5A, f_{SW} = 400kHz, considering the efficiency as 0.9, $I_{L(min)}$ = 1.48A, choose K_{IND} = 0.4, the calculated inductance is 23.7µH. A 22µH inductor is chosen. With this inductor, the ripple, peak, and rms currents of the inductor are 0.64A, 1.80A, and 1.48A, respectively.

8.2.1.2.2 Input Capacitor Selection

An input capacitor is required to reduce the surge current drawn from the input supply and the switching noise coming from the device. Electrolytic capacitors are recommended for energy storage. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, it is recommended to place a 10µF ceramic capacitor along with a 0.1µF capacitor from VIN to PGND/AGND to provide high-frequency filtering. The input capacitor voltage rating must be greater than the maximum input voltage. Use Equation 6 to calculate the input ripple voltage, where ESR_{CIN} is the ESR of input capacitor, and K_{DR} is the derating coefficient of ceramic capacitance at the applied DC voltage.

$$V_{IN(ripple)} = \frac{I_{L(ripple)}}{8 \times K_{DR} \times C_{IN} \times f_{SW}} \quad (6)$$

In this design, a 33µF, 100V electrolytic capacitor, a 10µF, 100V X7R ceramic capacitor and a 0.1µF, 100V X7R ceramic capacitor are chosen, yielding around 40mV input ripple voltage.

8.2.1.2.3 Output Capacitor Selection

The output capacitor reduces the high-frequency current ripple through the LED string. Excessive current ripple increases the RMS current in the LED string, therefore increasing the LED temperature.

1. Calculate the total dynamic resistance of the LED string (R_{LED}) using the LED manufacturer's datasheet.

2. Calculate the required impedance of the output capacitor (Z_{OUT}) given the acceptable peak-to-peak ripple current through the LED string, $I_{LED(ripple)}$. $I_{L(ripple)}$ is the peak-to-peak inductor ripple current as calculated with the selected inductor.

3. Calculate the minimum effective output capacitance required.

4. Increase the output capacitance appropriately due to the derating effect of applied DC voltage.

See Equation 7, Equation 8, and Equation 9.

$$R_{LED} = \frac{\Delta V_F}{\Delta I_F} \times \#\ of\ LEDs \tag{7}$$

$$Z_{COUT} = \frac{R_{LED} \times I_{LED(ripple)}}{I_{L(max)} - I_{LED(ripple)}} \tag{8}$$

$$C_{COUT} = \frac{1}{2\pi \times f_{SW} \times Z_{COUT}} \tag{9}$$

Once the output capacitor is chosen, Equation 10 can be used to estimate the peak-to-peak ripple current through the LED string.

$$I_{LED(ripple)} = \frac{Z_{COUT} \times I_{L(max)}}{Z_{COUT} + R_{LED}} \tag{10}$$

Osram WLED is used here. The dynamic resistance of the LED is 1Ω at 0.5A forward current. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. In this design, three 10µF, 100V X7R ceramic capacitor and a 0.1µF, 100V X7R ceramic capacitor are chosen. The calculated ripple current of the LED is about 19.4mA.

8.2.1.2.4 Sense Resistor Selection

The maximum LED current is 0.5A at 100% PWM duty and the corresponding V_{REF} is 200mV. By using Equation 11, the sense resistance is calculated as 400mΩ. Note that the power consumption of the sense resistor is 100mW, requiring enough margin of the resistor's power rating in selection.

$$R_{SENSE} = \frac{V_{REF}}{I_{LED\_FS}} \tag{11}$$

In this design, a 100Ω resistor is recommended for RFLT at CSN pin to avoid noise injection and increase robustness. An optional 1nF, 50V X7R ceramic capacitor is chosen for CFLT across CSP-CSN pins to filter high-frequency noise of sense feedback. Using the equation below, a 10µF, 50V X7R ceramic capacitor is chosen for CSNS across RSNS to suppress the ac magnitude of sense feedback less than 200mV.

$$C_{SENSE} = \frac{0.25 \times I_{L(max)}}{200mV \times f_{SW}} \tag{12}$$

8.2.1.2.5 Other External Components Selection

For loop stability, it is recommended to select a 10nF, 10V X7R ceramic capacitor for C_{COMP} and an optional 100Ω resistor for R_{COMP}.

8.2.2 LP8865CYQDGNRQ1 24V Input, 0.5A Output, 4-piece WLED Driver With PWM Dimming

The LP8865CUQDGNRQ1 is typically used as a Buck-Boost converter with PWM dimming to drive LEDs from an input from 4.5V to 63V range.

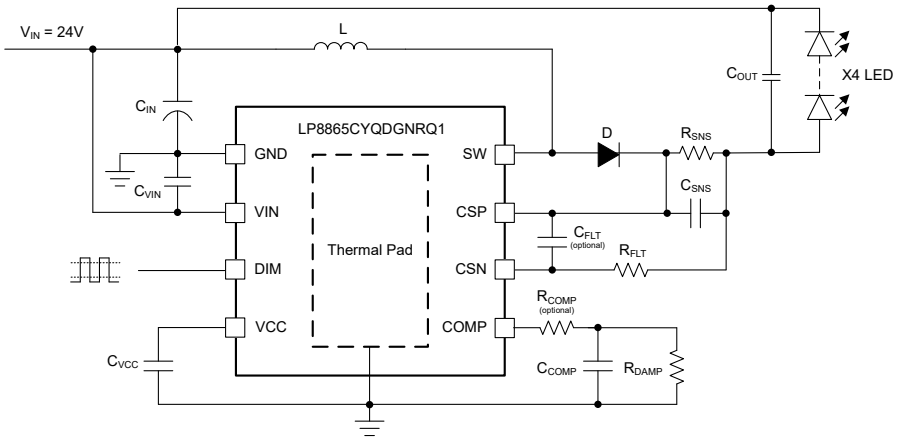


Figure 8-2. Typical Application for LP8865CYQDGNRQ1

8.2.2.1 Design Requirements

For this design example, use the parameters in the following table.

Table 8-2. Design Parameters

PARAMETER	VALUE
Input voltage range	9V -16V
LED string	5 LED
Output voltage	15V
Switching frequency	400kHz
Maximum LED current	0.5A
Inductor current ripple	40% of maximum inductor current
Dimming type	PWM version

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Inductor Selection

For this design, the input voltage is 9V to 16V. The output is 5 white LEDs in series and the inductor current ripple by requirement is less than 40% of maximum LED current. To choose a proper peak-to-peak inductor current ripple, the low-side FET current limit should not be violated when the converter works in no-load condition. This requires half of the peak-to-peak inductor current ripple to be lower than that limit. Another consideration is to ensure reasonable inductor core loss and copper loss caused by the peak-to-peak current ripple. Once this peak-to-peak inductor current ripple is chosen, use Equation 13 to calculate the recommended value of the inductor L.

$$L = \frac{V_{IN(min)} \times V_{OUT}}{\left(V_{OUT} + V_{IN(min)}\right) \times K_{IND} \times I_{L(max)} \times f_{SW}} \quad (13)$$

where

- K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum average LED current.
- $I_{L(max)}$ is the maximum average inductor current under minimum input voltage.
- f_{SW} is the switching frequency, 400kHz for this case.
- $V_{IN(min)}$ is the minimum input voltage.
- V_{OUT} is the sum of the voltage across LED load and the voltage across sense resistor.

With the chosen inductor value, the user can calculate the actual inductor current ripple using Equation 14.

$$I_{L(ripple)} = \frac{V_{IN(min)} \times V_{OUT}}{\left(V_{OUT} + V_{IN(min)}\right) \times L \times f_{SW}} \quad (14)$$

The design ratings of inductor RMS current and saturation current must be greater than those seen in the system requirement. This is to ensure no inductor overheat or saturation occurring. During power up, transient conditions or fault conditions, the inductor current may exceed its normal operating current and reach the current limit. Therefore, it is preferred to select a saturation current rating equal to or greater than the converter current limit. The peak-inductor-current and RMS current equations are shown in Equation 15 and Equation 16.

$$I_{L(peak)} = I_{L(max)} + \frac{I_{L(ripple)}}{2} \quad (15)$$

$$I_{L(rms)} = \sqrt{{I_{L(max)}}^2 + \frac{{I_{L(ripple)}}^2}{2}} \quad (16)$$

In this design, $V_{IN(min)}$ = 9V, V_{OUT} = 15V, I_{LED} = 0.5A, considering the efficiency as 0.8, $I_{L(max)}$ = 1.041A, f_{SW} = 400kHz, choose K_{IND} = 0.4, the calculated inductance is 33.75µH. A 33µH inductor is chosen. With this inductor, the ripple, peak, and rms currents of the inductor are 0.43A, 1.25A, and 1.04A, respectively.

8.2.2.2.2 Input Capacitor Selection

An input capacitor is required to reduce the surge current drawn from the input supply and the switching noise coming from the device. Electrolytic capacitors are recommended for energy storage. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, it is recommended to place a 10µF capacitor along with a 0.1µF capacitor from VIN to PGND/AGND to provide high-frequency filtering. The input capacitor voltage rating must be greater than the maximum input voltage. Use Equation 17 to calculate the input ripple voltage, where ESR_{CIN} is the ESR of input capacitor, and K_{DR} is the derating coefficient of ceramic capacitance at the applied DC voltage.

$$V_{IN(ripple)} = \frac{I_{L(ripple)}}{8 \times K_{DR} \times C_{IN} \times f_{SW}} \quad (17)$$

In this design, a 33µF, 100V electrolytic capacitor, a 10µF, 100V X7R ceramic capacitor and a 0.1µF, 100V X7R ceramic capacitor are chosen, yielding around 26mV input ripple voltage.

8.2.2.2.3 Output Capacitor Selection

The output capacitor reduces the high-frequency current ripple through the LED string. Excessive current ripple increases the RMS current in the LED string, therefore increasing the LED temperature.

1. Calculate the total dynamic resistance of the LED string (R_{LED}) using the LED manufacturer's datasheet.

2. Calculate the required impedance of the output capacitor (Z_{OUT}) given the acceptable peak-to-peak ripple current through the LED string, $I_{LED(ripple)}$, $I_{L(ripple)}$ is the peak-to-peak inductor ripple current as calculated with the selected inductor.

3. Calculate the minimum effective output capacitance required.

4. Increase the output capacitance appropriately due to the derating effect of applied DC voltage.

See Equation 18, Equation 19, and Equation 20.

$$R_{LED} = \frac{\Delta V_F}{\Delta I_F} \times \#\ of\ LEDs \tag{18}$$

$$Z_{COUT} = \frac{R_{LED} \times I_{LED(ripple)}}{I_{L(max)} - I_{LED(ripple)}} \tag{19}$$

$$C_{COUT} = \frac{1}{2\pi \times f_{SW} \times Z_{COUT}} \tag{20}$$

Once the output capacitor is chosen, Equation 21 can be used to estimate the peak-to-peak ripple current through the LED string.

$$I_{LED(ripple)} = \frac{Z_{COUT} \times I_{L(max)}}{Z_{COUT} + R_{LED}} \tag{21}$$

Osram WLED is used here. The dynamic resistance of the LED is 1Ω at 0.5A forward current. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. In this design, two 10µF, 100V X7R ceramic capacitor and a 0.1µF, 100V X7R ceramic capacitor are chosen. The calculated ripple current of the LED is about 20.3mA.

8.2.2.2.4 Sense Resistor Selection

The maximum LED current is 0.5A at 100% PWM duty and the corresponding V_{REF} is 200mV. By using Equation 22, the sense resistance is calculated as 400mΩ. Note that the power consumption of the sense resistor is 100mW, requiring enough margin of the resistor's power rating in selection.

$$R_{SENSE} = \frac{V_{REF}}{I_{LED\_FS}} \tag{22}$$

In this design, a 100Ω resistor is recommended for RFLT at CSN pin to avoid noise injection and increase robustness. An optional 1nF, 50V X7R ceramic capacitor is chosen for CFLT across CSP-CSN pins to filter high-frequency noise of sense feedback. Using the equation below, a 2.2µF, 50V X7R ceramic capacitor is chosen for CSNS to suppress the ac magnitude of sense feedback less than 200mV.

$$C_{SENSE} = \frac{0.25 \times I_{L(max)}}{200mV \times f_{SW}} \tag{23}$$

8.2.2.2.5 Other External Components Selection

For loop stability, it is recommended to select a 10nF, 10V X7R ceramic capacitor for C_{COMP} and an optional 100Ω resistor for R_{COMP}. A optional 10MΩ resistor is chosen for R_{DAMP} to suppress the overshoot current at rising edge of PWM on.

8.2.3 LP8865CWQDGNRQ1 24V Input, 2A Output, 4-piece WLED Driver With Analog Dimming

The LP8865CUQDGNRQ1 is typically used as a Buck converter with Analog dimming to drive LEDs from an input from 4.5V to 63V range.

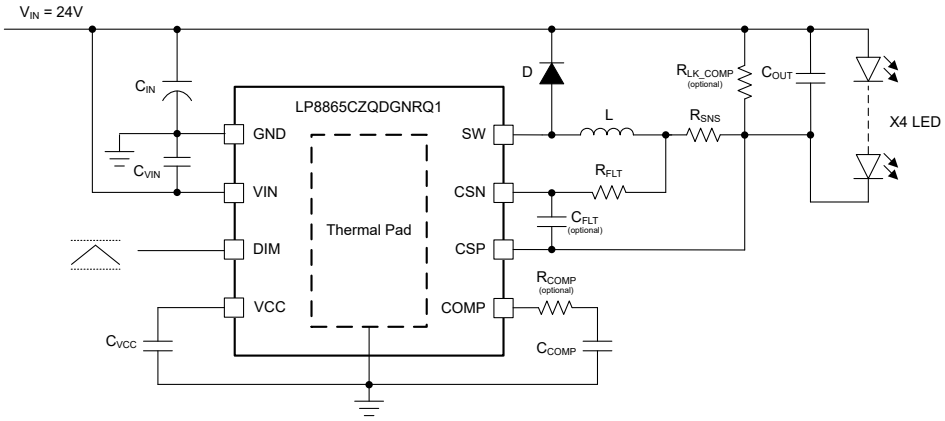


Figure 8-3. Typical Application for LP8865CUQDGNRQ1

8.2.3.1 Design Requirements

For this design example, use the parameters in the following table.

Table 8-3. Design Parameters

PARAMETER	VALUE
Input voltage range	9V -16V
LED string	1 LED
Output voltage	3V
Switching frequency	400kHz
Maximum LED current	2A
Inductor current ripple	40% of maximum inductor current
Dimming type	Analog version

8.2.3.2 Detailed Design Procedure

8.2.3.2.1 Inductor Selection

For this design, the input voltage is 9V to 16V. The output is single white LED and the inductor current ripple by requirement is less than 40% of maximum LED current. To choose a proper peak-to-peak inductor current ripple, the low-side FET current limit should not be violated when the converter works in no-load condition. This requires half of the peak-to-peak inductor current ripple to be lower than that limit. Another consideration is to ensure reasonable inductor core loss and copper loss caused by the peak-to-peak current ripple. Once this peak-to-peak inductor current ripple is chosen, use Equation 24 to calculate the recommended value of the inductor L.

$$L = \frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{V_{IN(max)} \times K_{IND} \times I_{L(max)} \times f_{SW}} \quad (24)$$

where

- K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum LED current.
- $I_{L(max)}$ is the maximum average inductor current, equal to the output current here.
- f_{SW} is the switching frequency.
- $V_{IN(max)}$ is the maximum input voltage.
- V_{OUT} is the sum of the voltage across LED load and the voltage across sense resistor.

With the chosen inductor value, the user can calculate the actual inductor current ripple using Equation 25.

$$I_{L(ripple)} = \frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{V_{IN(max)} \times L \times f_{SW}} \quad (25)$$

The design ratings of inductor RMS current and saturation current must be greater than those seen in the system requirement. This is to ensure no inductor overheat or saturation occurring. During power up, transient conditions or fault conditions, the inductor current may exceed its normal operating current and reach the current limit. Therefore, it is preferred to select a saturation current rating equal to or greater than the converter current limit. The peak-inductor-current and RMS current equations are shown in Equation 26and Equation 27.

$$I_{L(peak)} = I_{L(max)} + \frac{I_{L(ripple)}}{2} \quad (26)$$

$$I_{L(rms)} = \sqrt{I_{L(max)}^{2} + \frac{I_{L(ripple)}^{2}}{2}} \quad (27)$$

In this design, $V_{IN(max)}$ = 16V, V_{OUT} = 3V, I_{LED} = 2A, $I_{L(max)}$ = 2A, f_{SW} = 400kHz, choose K_{IND} = 0.4, the calculated inductance is 7.6µH. A 10µH inductor is chosen. With this inductor, the ripple, peak, and rms currents of the inductor are 0.61A, 2.3A, 2A, respectively.

8.2.3.2.2 Input Capacitor Selection

An input capacitor is required to reduce the surge current drawn from the input supply and the switching noise coming from the device. Electrolytic capacitors are recommended for energy storage. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, it is recommended to place a 10µF capacitor along with a 0.1µF capacitor from VIN to PGND/AGND to provide high-frequency filtering. The input capacitor voltage rating must be greater than the maximum input voltage. Use Equation 28 to calculate the input ripple voltage, where ESR_{CIN} is the ESR of input capacitor, and K_{DR} is the derating coefficient of ceramic capacitance at the applied DC voltage.

$$V_{IN(ripple)} = I_{L(max)} \times \left(\frac{V_{OUT}}{K_{DR} \times C_{IN} \times f_{SW} \times V_{IN(max)}} + ESR_{CIN}\right) \quad (28)$$

In this design, a 33µF, 100V electrolytic capacitor, two 22µF, 100V X7R ceramic capacitor and a 0.1µF, 100V X7R ceramic capacitor are chosen, yielding around 113mV input ripple voltage.

8.2.3.2.3 Output Capacitor Selection

The output capacitor reduces the high-frequency current ripple through the LED string. Excessive current ripple increases the RMS current in the LED string, therefore increasing the LED temperature.

1. Calculate the total dynamic resistance of the LED string (R_{LED}) using the LED manufacturer's datasheet.

2. Calculate the required impedance of the output capacitor (Z_{OUT}) given the acceptable peak-to-peak ripple current through the LED string, $I_{LED(ripple)}$. $I_{L(ripple)}$ is the peak-to-peak inductor ripple current as calculated with the selected inductor.

3. Calculate the minimum effective output capacitance required.

4. Increase the output capacitance appropriately due to the derating effect of applied DC voltage.

See Equation 29, Equation 30, and Equation 31.

$$R_{LED} = \frac{\Delta V_F}{\Delta I_F} \times \#\ of\ LEDs \tag{29}$$

$$Z_{COUT} = \frac{R_{LED} \times I_{LED(ripple)}}{I_{L(ripple)} - I_{LED(ripple)}} \tag{30}$$

$$C_{COUT} = \frac{1}{2\pi \times f_{SW} \times Z_{COUT}} \tag{31}$$

Once the output capacitor is chosen, Equation 32 can be used to estimate the peak-to-peak ripple current through the LED string.

$$I_{LED(ripple)} = \frac{Z_{COUT} \times I_{L(ripple)}}{Z_{COUT} + R_{LED}} \tag{32}$$

Osram WLED is used here. The dynamic resistance of the LED is 0.67Ω at 2A forward current. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. In this design, a 4.7µF, 100V X7R ceramic capacitor and a 0.1µF, 100V X7R ceramic capacitor are chosen. The calculated ripple current of the LED is about 68.4mA.

8.2.3.2.4 Sense Resistor Selection

The maximum LED current is 2A at 2V analog input and the corresponding V_{REF} is 200mV. By using Equation 33, the sense resistance is calculated as 100mΩ. Note that the power consumption of the sense resistor is 400mW, requiring enough margin of the resistor's power rating in selection.

$$R_{SENSE} = \frac{V_{REF}}{I_{LED\_FS}} \tag{33}$$

In this design, a 100Ω resistor is recommended for RFLT at CSN pin to avoid noise injection and increase robustness. An optional 1nF, 50V X7R ceramic capacitor is chosen for CFLT across CSP-CSN pins to filter high-frequency noise of sense feedback.

8.2.3.2.5 Other External Components Selection

In this design, a 0.1µF, 50V X7R ceramic capacitor is chosen for high-frequency filtering of sense feedback.

For loop stability, it is recommended to select a 1nF, 10V X7R ceramic capacitor for C_{COMP} and a 1kΩ resistor for R_{COMP}. A 1MΩ resistor is chosen for R_{DAMP} to suppress the overshoot current at rising edge of PWM on.

For loop stability, it is recommended to select a 1nF, 10V X7R ceramic capacitor for C_{COMP} and an optional 100Ω resistor for R_{COMP} . An optional resistor is chosen for R_{LK_COMP} to compensate the CSP+CSN common mode leakage current and avoid it passing through LEDs.

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply ranging between 4.5V and 63V. This input supply must be well regulated. The device requires an input capacitor to reduce the surge current drawn from the input supply and the switching noise from the device. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10µF capacitor is enough.

8.4 Layout

The LP8865C-Q1 requires a proper layout for optimal performance. The following section gives some guidelines to ensure a proper layout.

8.4.1 Layout Guidelines

Examples of a proper layout for boost topolgy, buck-boost topology and buck topology of LP8865C-Q1 family is shown below.

- Creating a large GND plane for good electrical and thermal performance is important.
- The VIN and GND traces should be as wide as possible to reduce trace impedance. Wide traces have the additional advantage of providing excellent heat dissipation.
- Thermal vias can be used to connect the top-side GND plane to additional printed-circuit board (PCB) layers for heat dissipation and grounding.
- The input capacitors must be located as close as possible to the IN pin and the GND pin.
- The VCC capacitor should be placed as close as possible to VCC pin to ensure stable LDO output voltage.
- The SW trace must be kept as short as possible to reduce parasitic inductance and thereby reduce transient voltage spikes. Short SW trace also reduces radiated noise and EMI.
- Do not allow switching current to flow under the device.
- The routing of CSN and CSP traces are recommended to be in parallel and kept as short as possible and placed away from the high-voltage switching trace and the ground shield.
- The compensation capacitor must be placed as close as possible to COMP pin so as to prevent oscillation and system instability.

8.4.2 Layout Example

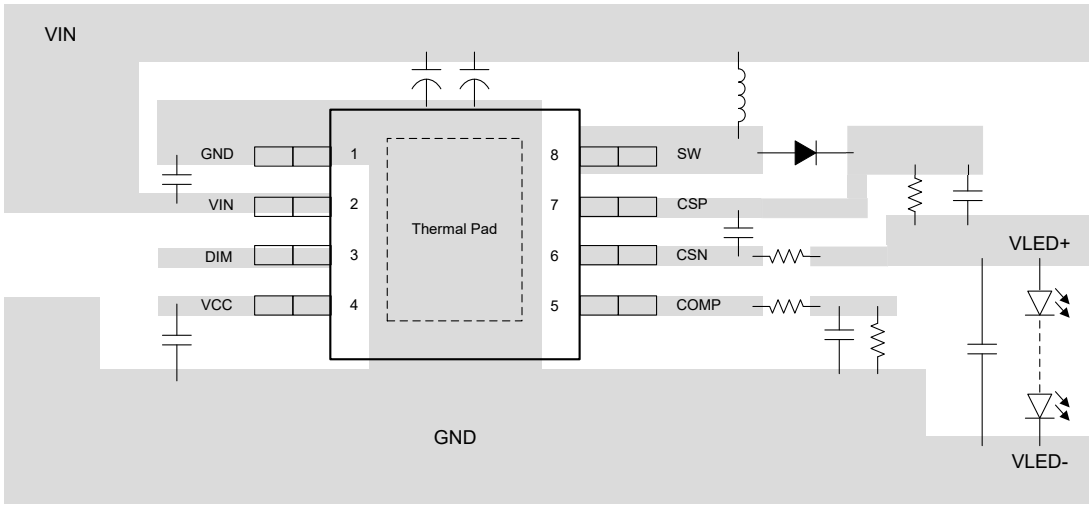


Figure 8-4. Boost Topology Top View Layout Example

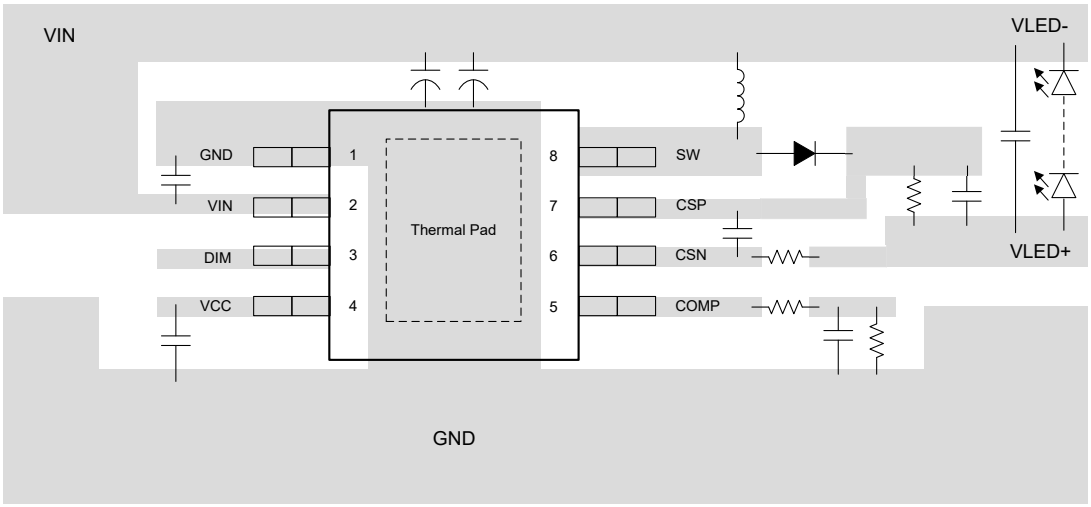


Figure 8-5. Buck-Boost Topology Top View Layout Example

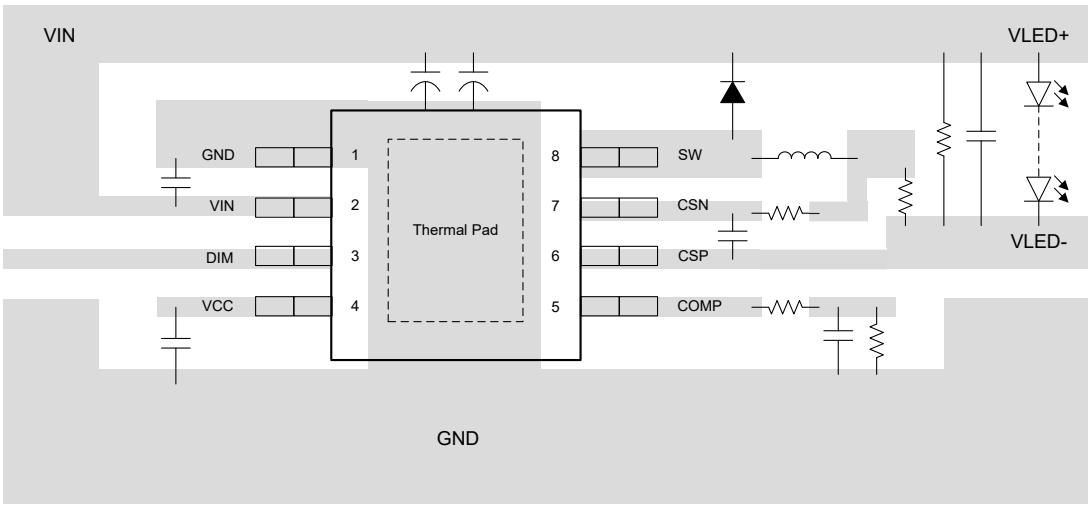


Figure 8-6. Buck Topology Top View Layout Example

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

DATE	REVISION	NOTES
May 2025	*	Initial release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated s. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP8865CUQDGNRQ1	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	FULL NIPDAU	Level-1-260C-UNLIM	-40 to 125	65CU
LP8865CVQDGNRQ1	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	FULL NIPDAU	Level-1-260C-UNLIM	-40 to 125	65CV
LP8865CWQDGNRQ1	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	FULL NIPDAU	Level-1-260C-UNLIM	-40 to 125	65CW
LP8865CXQDGNRQ1	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	FULL NIPDAU	Level-1-260C-UNLIM	-40 to 125	65CX
LP8865CYQDGNRQ1	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	FULL NIPDAU	Level-1-260C-UNLIM	-40 to 125	65CY
LP8865CZQDGNRQ1	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	FULL NIPDAU	Level-1-260C-UNLIM	-40 to 125	65CZ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

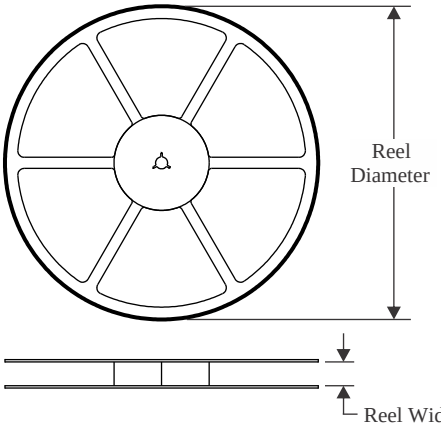
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

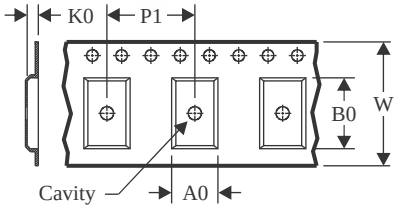
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

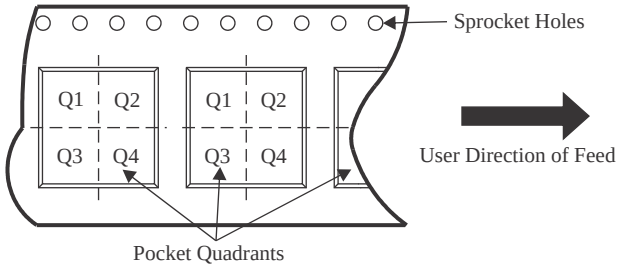


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

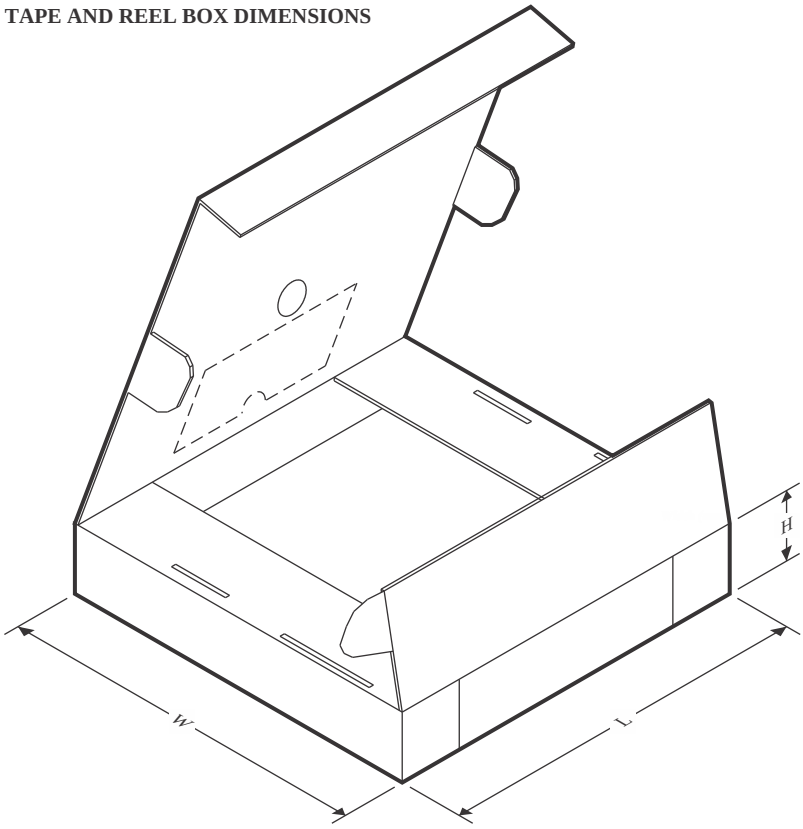
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8865CUQDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP8865CVQDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP8865CWQDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP8865CXQDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP8865CYQDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP8865CZQDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8865CUQDGNRQ1	HVSSOP	DGN	8	2500	353.0	353.0	32.0
LP8865CVQDGNRQ1	HVSSOP	DGN	8	2500	353.0	353.0	32.0
LP8865CWQDGNRQ1	HVSSOP	DGN	8	2500	353.0	353.0	32.0
LP8865CXQDGNRQ1	HVSSOP	DGN	8	2500	353.0	353.0	32.0
LP8865CYQDGNRQ1	HVSSOP	DGN	8	2500	353.0	353.0	32.0
LP8865CZQDGNRQ1	HVSSOP	DGN	8	2500	353.0	353.0	32.0

GENERIC PACKAGE VIEW

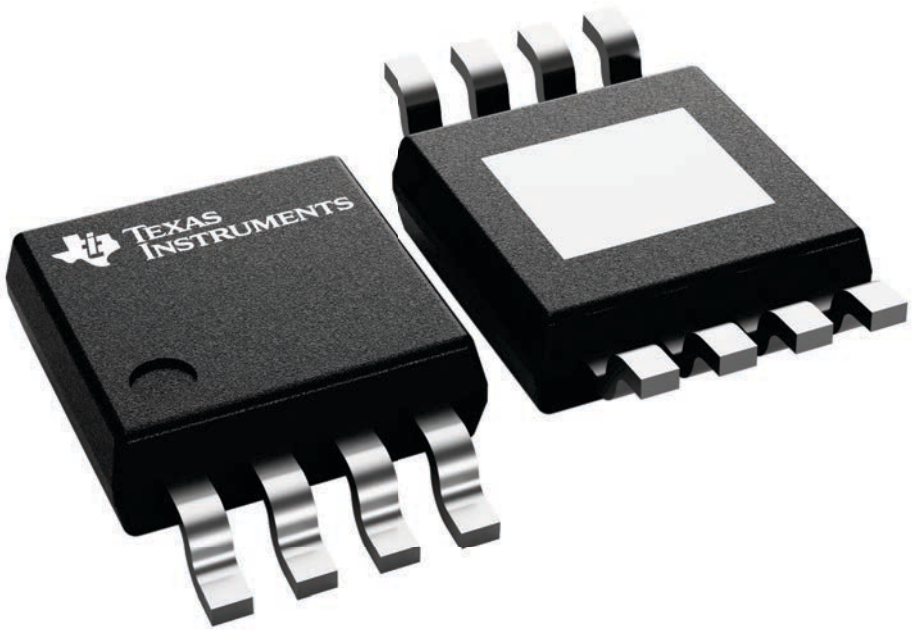
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

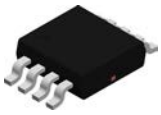
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B

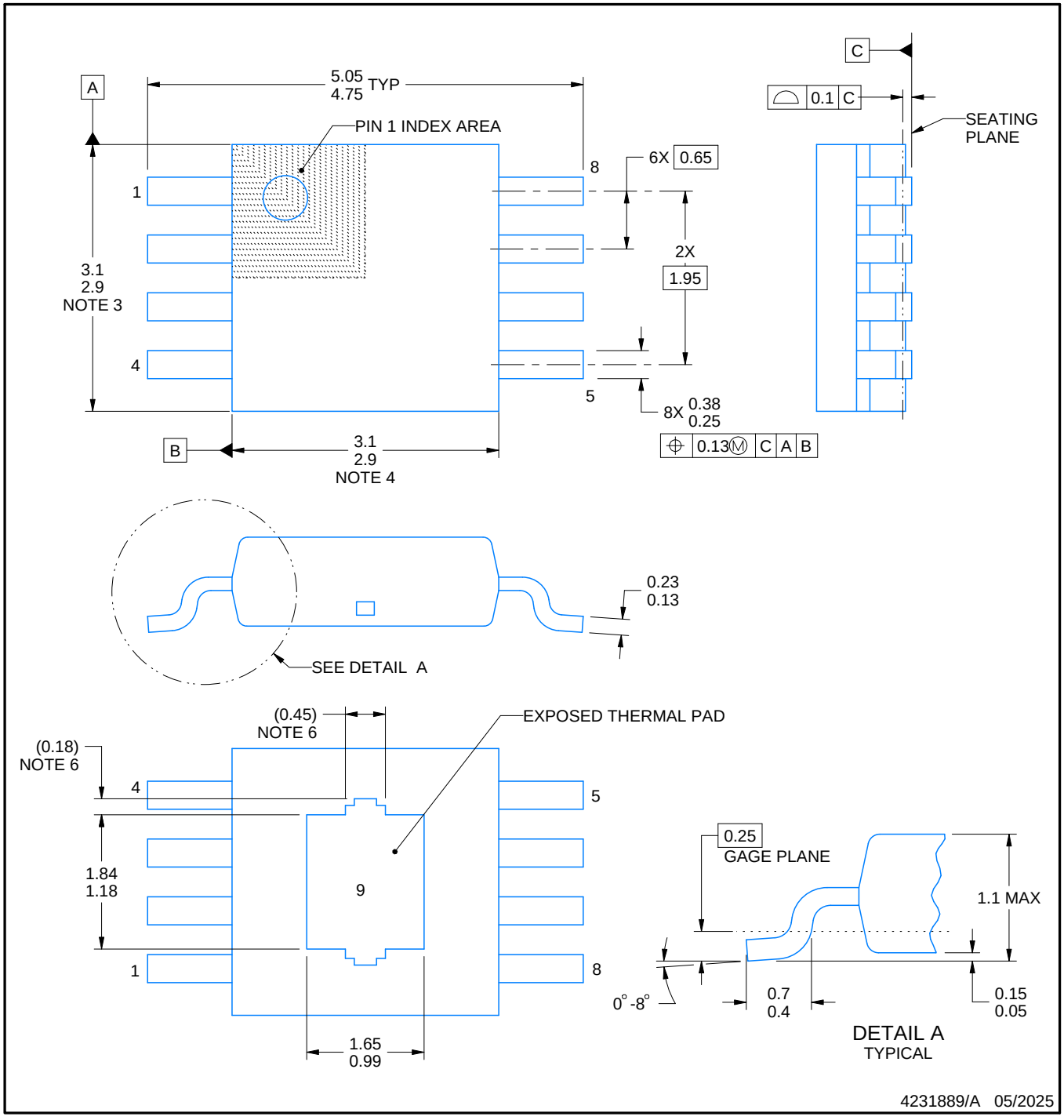
PACKAGE OUTLINE

DGN0008K



PowerPAD™ VSSOP - 1.1 mm max height

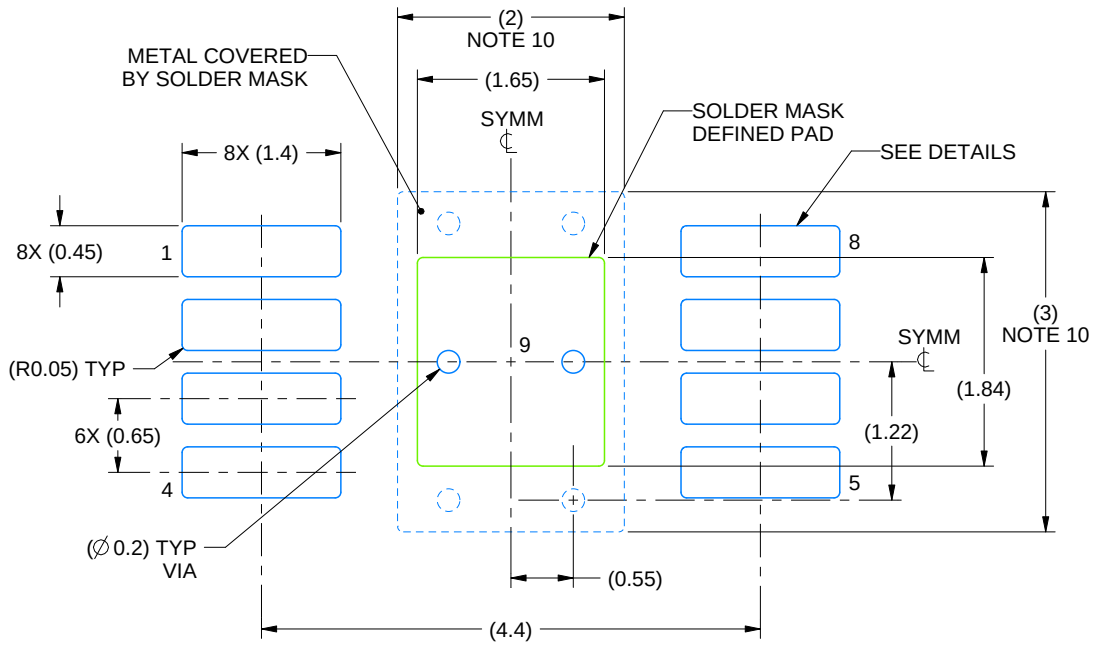
SMALL OUTLINE PACKAGE



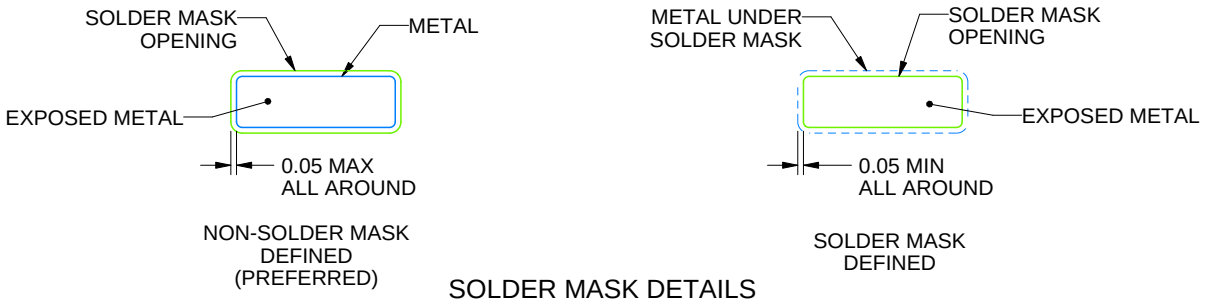
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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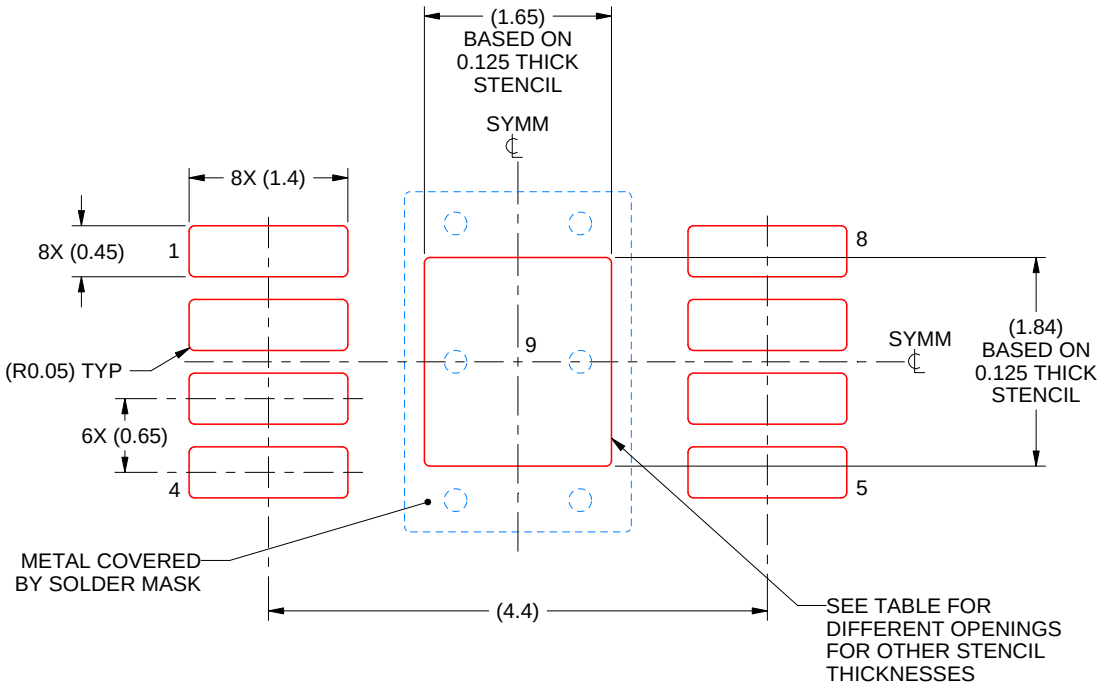
NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.84 X 2.06
0.125	1.65 X 1.84 (SHOWN)
0.15	1.51 X 1.68
0.175	1.39 X 1.56

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025