LP8774x-Q1 Three Buck Converters and 5-V Boost for AWR and IWR Radar Sensors

1 Features

- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature
- Functional safety-compliant device
  - Developed for functional safety applications
  - Documentation available to aid ISO 26262 functional safety system design up to ASIL-C / SIL-2
  - Input supply overvoltage and undervoltage monitoring
  - Regulator output overvoltage and undervoltage monitoring
  - Overvoltage and undervoltage monitoring for one external rail
  - Q&A watchdog
  - Level or PWM error signal monitor (ESM)
  - BIST and CRC
- Input voltage: 3.3V nominal (3V to 4V range)
- Three low-noise step-down DC/DC converters:
  - Output voltage: 0.9V to 1.9V, 0.8V (BUCK3), 0.82V (BUCK3)
  - Maximum output current: 3A/ 3A/ 3A
  - Switching frequency: 4.4MHz, 8.8MHz, and 17.6MHz
- 5V boost converter
  - Maximum output current: 350mA
- 150mA LDO
  - Output voltage 1.8V or 3.3V
- Output short-circuit and overload protection
- Input overvoltage protection (OVP) and undervoltage lockout (UVLO)
- Overtemperature warning and protection
- Serial peripheral interface (SPI)

2 Applications

- Short and medium range corner radar
- Long range front radar
- Ultra-short range radar
- Low ripple, low noise applications

3 Description

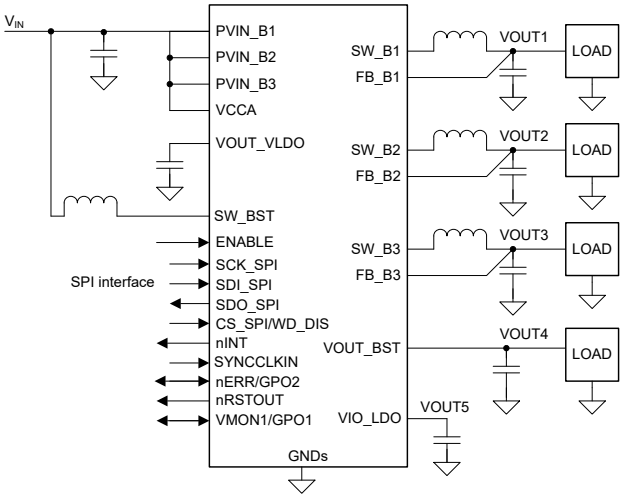
The LP8774x-Q1 device is designed to meet the power management requirements of the AWR and IWR MMICs in various automotive and industrial radar applications. The device has three step-down DC/DC converters, a 5V boost converter and a 1.8V or 3.3V LDO. The LDO is powered from the boost and intended for xWR I/O supply. An SPI serial interface and enable signals control the device.

The step-down DC/DC converters support programmable switching frequency of 4.4MHz, 8.8MHz, or 17.6MHz. High switching frequency and low noise across wide frequency range enable LDO-free power solution with minimal or no passive filtering. The high switching frequency improves thermals and transient settling for the MMIC RF rails. The device forces the switching clock into PWM mode for optimal RF performance and can also be synchronized to an external clock. The device supports remote voltage sensing to compensate IR drop between the regulator output and the point-of-load (POL) which improves the accuracy of the output voltage.

Package Information

PART NUMBER(1)	PACKAGE	PACKAGE SIZE(2)	BODY SIZE (NOM)
LP8774x-Q1	RXV (VQFN-HR, 28)	4.50mm × 5.00mm	4.50mm × 5.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application

Table of Contents

4 Description (continued)

The LP8774x-Q1 device supports programmable start-up and shutdown delays and sequences which are synchronized to the ENABLE signal. The sequences can also include GPO signals to control external regulators, load switches, and processor reset. The default settings for the device are programmed into nonvolatile memory (NVM). The device controls the output slew rate to minimize output voltage overshoot and in-rush current during device start-up.

This data sheet applies to the superset device, including all register settings, as was validated and covers the following generic part number LP8774x-Q1 with orderable part numbers **LP8774xyzzRXVR Q1**where:

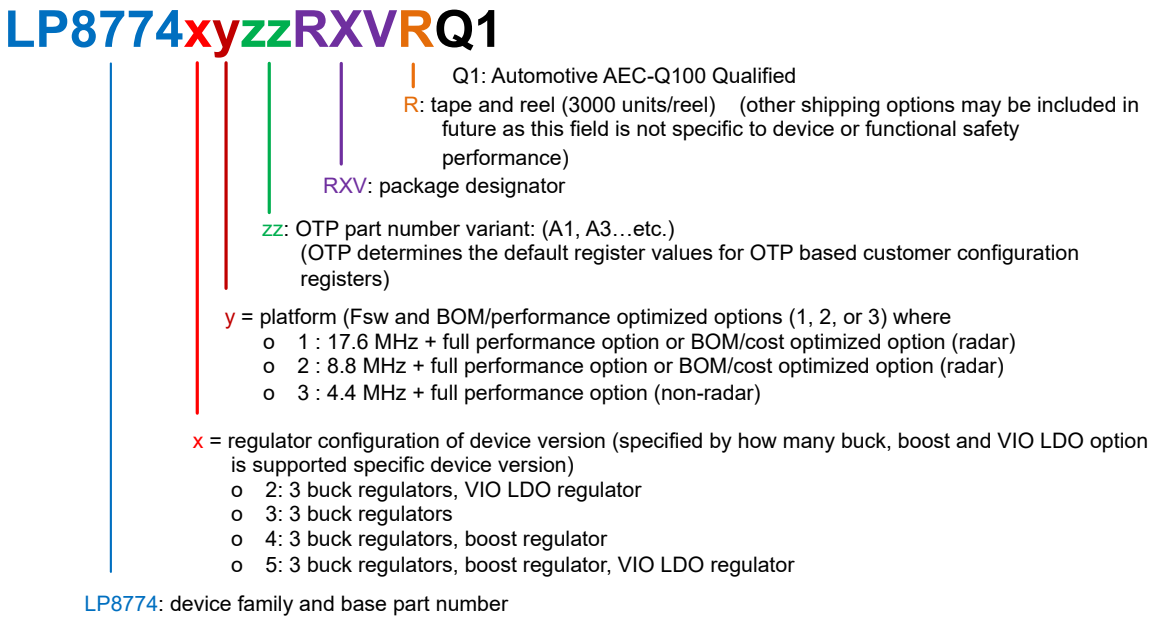


Figure 4-1. LP8774x-Q1 Orderable Part Numbers Scheme

5 Pin Configuration and Functions

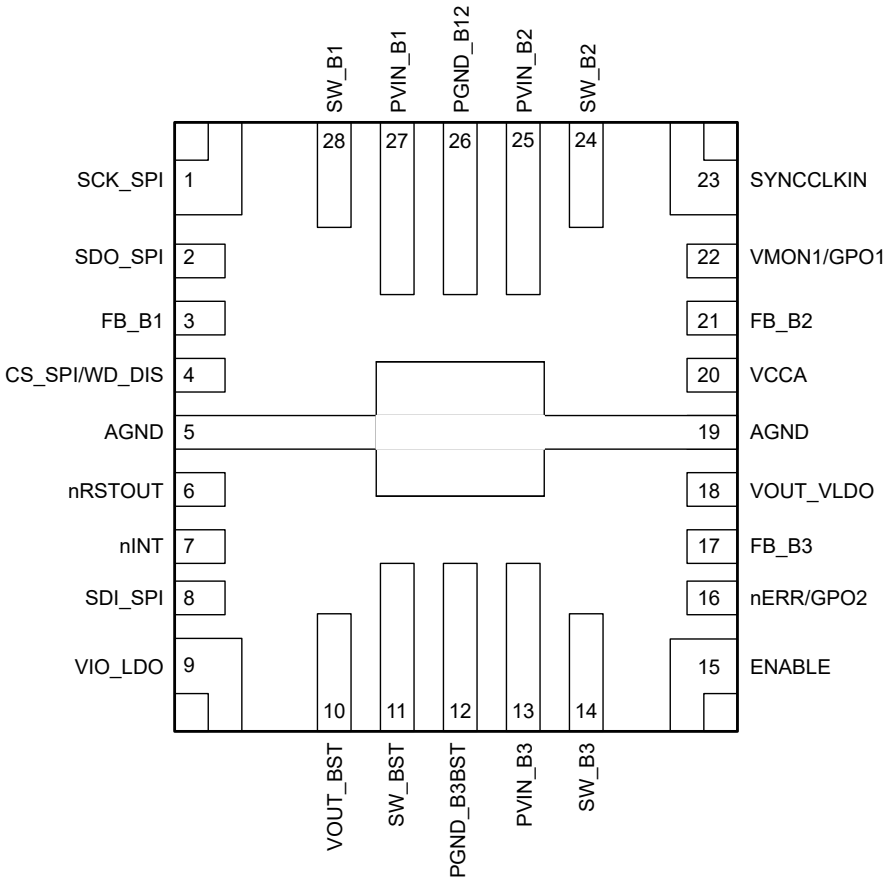


Figure 5-1. RXV Package, 28-Pin VQFN-HR (Top View)

Table 5-1. Pin Functions

PIN		I/O	TYPE	DESCRIPTION	CONNECTION IF NOT USED
NAME	NO.				
SCK_SPI	1	I	Digital	Clock signal for SPI interface.	Ground
SDO_SPI	2	O	Digital	Output data signal for SPI interface.	Floating
FB_B1	3	—	Analog	Output voltage feedback (positive) for BUCK1.	Ground
CS_SPI/ WD_DIS	4	I	Digital	Primary function: Chip select signal for SPI interface.	VCCA
		I	Digital	Alternative programmable function: Watchdog Deactivation Input.	Not applicable
AGND	5	—	Ground	Ground.	Ground
NRSTOUT	6	O	Digital	Reset output.	Floating
nINT	7	O	Digital	Interrupt output and CAN PHY control or both.	Floating
SDI_SPI	8	I	Digital	Input data signal for SPI interface.	Ground
VIO_LDO	9	—	Analog	IO supply from the internal LDO or from external source. LDO active: regulator filter node. LDO inactive: input for connecting to an external IO supply source, with input filtering capacitor placed.	Not applicable
VOUT_BST	10	—	Analog	BOOST active: BOOST output (internally connected as VIO_LDO input). BOOST inactive and VIO_LDO inactive: short with VIO_LDO. BOOST inactive and VIO_LDO active: input for connecting to an external supply used as VIO_LDO input.	External supply
SW_BST	11	—	Analog	When BOOST active: BOOST input. When BOOST inactive: short with VOUT_BST.	VOUT_BST

Table 5-1. Pin Functions (continued)

PIN		I/O	TYPE	DESCRIPTION	CONNECTION IF NOT USED
NAME	NO.				
PGND_B3BST	12	—	Ground	Power ground for BUCK3 and BOOST.	Ground
PVIN_B3	13	—	Power	Power input for BUCK3. The separate power pins PVIN_Bxx are not connected together internally – PVIN_Bxx and VCCA pins must be connected together in the application and be locally bypassed.	System supply
SW_B3	14	—	Analog	BUCK3 switch node.	Floating
ENABLE	15	I	Digital	Programmable ENABLE signal.	Not applicable
nERR/GPO2	16	I	Digital	Primary function: System MCU Error Monitoring Input.	Ground
		O	Digital	Alternative programmable function: General Purpose Output signal (GPO2).	Floating
		O	Digital	Alternative programmable function: Fault Communication Output signal (FAULT2).	Floating
FB_B3	17	—	Analog	Output voltage feedback (positive) for BUCK3.	Ground
VOUT_VLDO	18	—	Power	LDO regulator filter node. LDO is used for internal purposes. No external load allowed.	-
AGND	19	—	Ground	Ground.	Ground
VCCA	20	—	Power	Supply voltage for internal LDO. VCCA and PVIN_Bxx pins must be connected together in the application and be locally bypassed.	System supply
FB_B2	21	—	Analog	Output voltage feedback (positive) for BUCK2.	Ground
VMON1/ GPO1	22	—	Analog	Voltage monitoring input.	Ground
		O	Digital	Alternative programmable function: General Purpose Output signal (GPO1).	Floating
		O	Digital	Alternative programmable function: Fault Communication Output signal (FAULT1).	Floating
		O	Digital	Alternative programmable function: CAN PHY control (CAN_DIS).	Floating
SYNCCLKIN	23	I	Digital	External clock input.	Ground
SW_B2	24	—	Analog	BUCK2 switch node.	Floating
PVIN_B2	25	—	Power	Power input for BUCK2. The separate power pins PVIN_Bxx are not connected together internally – PVIN_Bxx and VCCA pins must be connected together in the application and be locally bypassed.	System supply
PGND_B12	26	—	Ground	Power ground for BUCK1 and BUCK2.	Ground
PVIN_B1	27	—	Power	Power input for BUCK1. The separate power pins PVIN_Bxx are not connected together internally – PVIN_Bxx and VCCA pins must be connected together in the application and be locally bypassed.	System supply
SW_B1	28	—	Analog	BUCK1 switch node.	Floating

6 Device and Documentation Support

6.1 Documentation Support

6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2022) to Revision B (June 2024)	Page
• Changed the Device Information table to the Packaging Information table	1
• Added Figure 4-1	3

Changes from Revision * (October 2021) to Revision A (November 2022)	Page
• Changed the document status from *Advance Information* to *Production Data*	1

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP877432A8RXVRQ1	Active	Production	VQFN-HR (RXV) | 28	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	LP8774 32A8-Q1
LP877432A8RXVRQ1.A	Active	Production	VQFN-HR (RXV) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8774 32A8-Q1
LP877442A9RXVRQ1	Active	Production	VQFN-HR (RXV) | 28	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	LP8774 42A9-Q1
LP877442A9RXVRQ1.A	Active	Production	VQFN-HR (RXV) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8774 42A9-Q1
LP87745101RXVRQ1	Active	Production	VQFN-HR (RXV) | 28	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	LP8774 5101-Q1
LP87745101RXVRQ1.A	Active	Production	VQFN-HR (RXV) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8774 5101-Q1
LP877451A1RXVRQ1	Active	Production	VQFN-HR (RXV) | 28	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	LP8774 51A1-Q1
LP877451A1RXVRQ1.A	Active	Production	VQFN-HR (RXV) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8774 51A1-Q1
LP877452A7RXVRQ1	Active	Production	VQFN-HR (RXV) | 28	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	LP8774 52A7-Q1
LP877452A7RXVRQ1.A	Active	Production	VQFN-HR (RXV) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8774 52A7-Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF LP87745-Q1 :

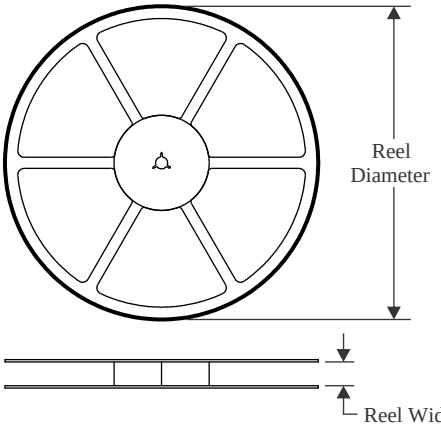
- Catalog : LP87745

NOTE: Qualified Version Definitions:

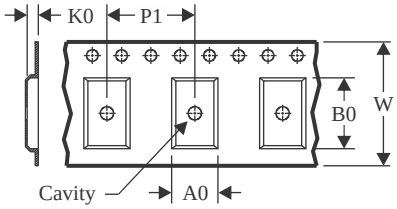
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

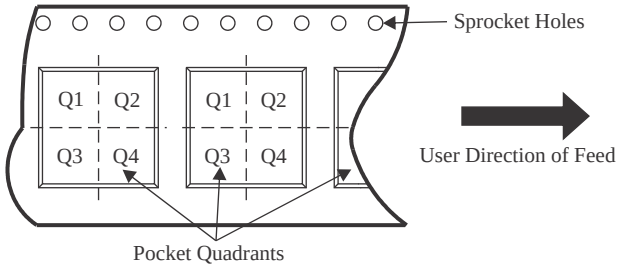


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

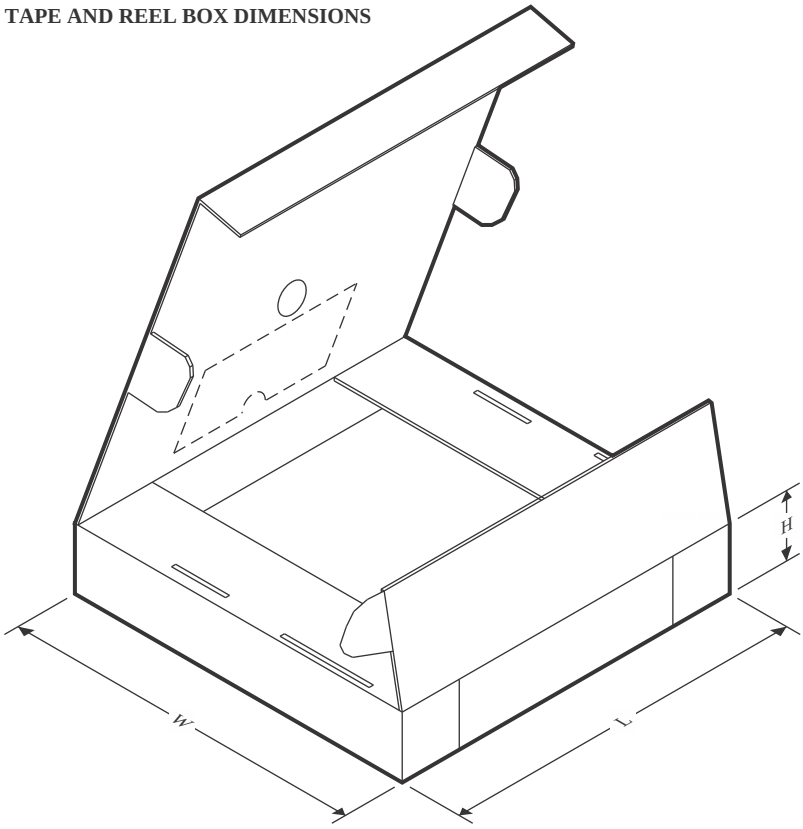
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP877432A8RXVRQ1	VQFN-HR	RXV	28	3000	330.0	12.4	4.8	5.3	1.15	8.0	12.0	Q1
LP877442A9RXVRQ1	VQFN-HR	RXV	28	3000	330.0	12.4	4.8	5.3	1.15	8.0	12.0	Q1
LP87745101RXVRQ1	VQFN-HR	RXV	28	3000	330.0	12.4	4.8	5.3	1.15	8.0	12.0	Q1
LP877451A1RXVRQ1	VQFN-HR	RXV	28	3000	330.0	12.4	4.8	5.3	1.15	8.0	12.0	Q1
LP877452A7RXVRQ1	VQFN-HR	RXV	28	3000	330.0	12.4	4.8	5.3	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP877432A8RXVRQ1	VQFN-HR	RXV	28	3000	367.0	367.0	35.0
LP877442A9RXVRQ1	VQFN-HR	RXV	28	3000	367.0	367.0	35.0
LP87745101RXVRQ1	VQFN-HR	RXV	28	3000	367.0	367.0	35.0
LP877451A1RXVRQ1	VQFN-HR	RXV	28	3000	367.0	367.0	35.0
LP877452A7RXVRQ1	VQFN-HR	RXV	28	3000	367.0	367.0	35.0

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