LP339

LP339 Ultra-Low Power Quad Comparator

Literature Number: SNOSBE0A

National Semiconductor

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LP339
Ultra-Low Power Quad Comparator

General Description

The LP339 consists of four independent voltage comparators designed specifically to operate from a single power supply and draw typically 60 µA of power supply drain current over a wide range of power supply voltages. Operation from split supplies is also possible and the ultra-low power supply drain current is independent of the power supply voltage. These comparators also feature a common-mode range which includes ground, even when operated from a single supply.

Applications include limit comparators, simple analog-to-digital converters, pulse, square and time delay generators; VCO's; multivibrators; high voltage logic gates. The LP339 was specifically designed to interface with the CMOS logic family. The ultra-low supply current makes the LP339 valuable in battery powered applications.

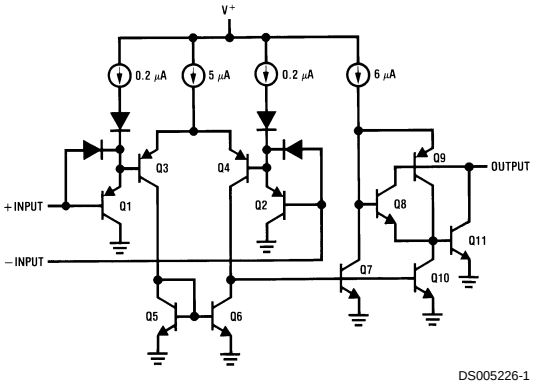
Advantages

- Ultra-low power supply drain suitable for battery applications
- Single supply operation
- Sensing at ground
- Compatible with CMOS logic family
- Pin-out identical to LM339

Features

- Ultra-low power supply current drain (60 µA)—independent of the supply voltage (75 µW/comparator at +5 V_{DC})
- Low input biasing current: 3 nA
- Low input offset current: ±0.5 nA
- Low input offset voltage: ±2 mV
- Input common-mode voltage includes ground
- Output voltage compatible with MOS and CMOS logic
- High output sink current capability (30 mA at V_O=2 V_{DC})
- Supply Input protected against reverse voltages

Schematic and Connection Diagrams



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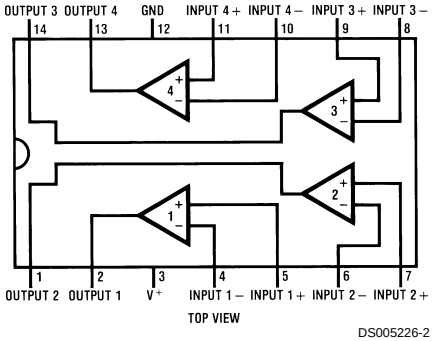

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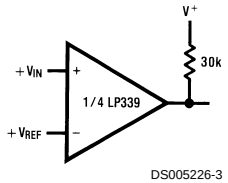
Order Number LP339M for S.O. Package
See NS Package Number M14A
Order Number LP339N for Dual-In-Line Package
See NS Package Number N14A

Typical Applications (V^+= 5.0 V_{DC})

Basic Comparator



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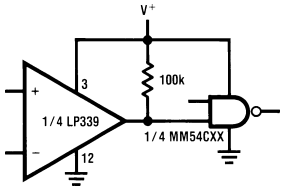
Driving CMOS



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	36 V_{DC} or ±18 V_{DC}
Differential Input Voltage	±36 V_{DC}
Input Voltage	−0.3 V_{DC} to 36 V_{DC}
Power Dissipation (Note 2)	
Molded DIP	570 mW
Output Short Circuit to GND (Note 3)	Continuous
Input Current V_{IN} < −0.3 V_{DC} (Note 4)	50 mA
Operating Temperature Range	0˚C to +70˚C
Storage Temperature Range	−65˚ to +150˚C
Soldering Information:	
Dual-In-Line Package (10 sec.)	+260˚C
S.O. Package:	
Vapor Phase (60 sec.)	+215˚C
Infrared (15 sec.)	+220˚C

See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.

Electrical Characteristics

(V+=5 V_{DC}) (Note 5)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage	T_A=25˚C (Note 10)		±2	±5	mV_{DC}
Input Bias Current	I_{IN}(+) or I_{IN}(−) with the Output in the Linear Range, T_A=25˚C (Note 6)		2.5	25	nA_{DC}
Input Offset Current	I_{IN}(+)−I_{IN}(−), T_A=25˚C		±0.5	±5	nA_{DC}
Input Common Mode Voltage Range	T_A=25˚C (Note 7)	0		V+−1.5	V_{DC}
Supply Current	R_L=Infinite on all Comparators, T_A=25˚C		60	100	μA_{DC}
Voltage Gain	V_O = 1 V_{DC} to 11 V_{DC}, R_L=15 kΩ, V^+=15 V_{DC}, T_A=25˚C		500		V/mV
Large Signal Response Time	V_{IN}=TTL Logic Swing, V_{REF}=1.4 V_{DC}, V_{RL}=5 V_{DC}, R_L=5.1 kΩ, T_A=25˚C		1.3		µSec
Response Time	V_{RL}=5 V_{DC}, R_L=5.1 kΩ, T_A=25˚C (Note 8)		8		µSec
Output Sink Current	V_{IN}(−)=1 V_{DC}, V_{IN}(+)=0, V_O=2 V_{DC}, T_A=25˚C (Note 12)	15	30		mA_{DC}
	V_O=0.4 V_{DC}	0.20	0.70		mA_{DC}
Output Leakage Current	V_{IN}(+)=1 V_{DC}, V_{IN}(−)=0, V_O=5 V_{DC}, T_A=25˚C		0.1		nA_{DC}
Input Offset Voltage	(Note 10)			±9	mV_{DC}
Input Offset Current	I_{IN}(+)−I_{IN}(−)		±1	±15	nA_{DC}
Input Bias Current	I_{IN}(+) or I_{IN}(−) with Output in Linear Range		4	40	nA_{DC}
Input Common Mode Voltage Range	Single Supply	0		V+−2.0	V_{DC}
Output Sink Current	V_{IN}(−)=1 V_{DC}, V_{IN}(+)=0, V_O=2 V_{DC}	10			mA_{DC}
Output Leakage Current	V_{IN}(+)=1 V_{DC}, V_{IN}(−)=0, V_O=30 V_{DC}			1.0	μA_{DC}
Differential Input Voltage	All $V_{IN'S}$≥0 V_{DC} (or V^- on split supplies) (Note 9)			36	V_{DC}

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: For elevated temperature operation, T_j max is 125˚C for the LP339. θ_{ja} (junction to ambient) is 175˚C/W for the LP339N and 120˚C/W for the LP339M when either device is soldered in a printed circuit board in a still air environment. The low bias dissipation and the “ON-OFF” characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

Note 3: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 50 mA.

Note 4: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input clamp diodes. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltage of the comparators to go to the V+ voltage level (or to ground for a large input overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which is negative, again returns to a value greater than −0.3 V_{DC} (T_A=25˚C).

Note 5: These specifications apply for V^+=5V_{DC} and 0˚C≤T_A≤70˚ C, unless otherwise stated. The temperature extremes are guaranteed but not 100% production tested. These parameters are not used to calculate outgoing AQL.

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or the input lines as long as the common-mode range is not exceeded.

Note 7: The input common-mode voltage or either input voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+−1.5V (T_A=25˚C), but either or both inputs can go to 30 V_{DC} without damage.

Note 8: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 1.3 µs can be obtained. See Typical Performance Characteristics section.

Electrical Characteristics (Continued)

Note 9: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3 V_{DC} (or 0.3 V_{DC} below the magnitude of the negative power supply, if used) at T_A=25˚C.

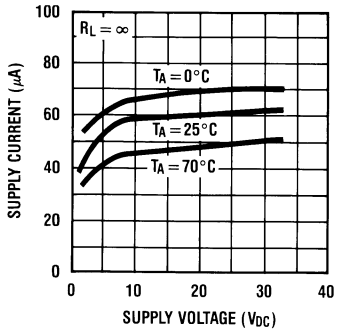
Note 10: At output switch point, V_O=1.4V, R_S=0Ω with V^+ from 5 V_{DC}; and over the full input common-mode range (0 V_{DC} to V^+−1.5 V_{DC}).

Note 11: For input signals that exceed V^+, only the overdriven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V maximum, and a limiting resistor should be used on all inputs that might exceed the positive supply.

Note 12: The output sink current is a function of the output voltage. The LP339 has a bi-modal output section which allows it to sink large currents via a Darlington connection at output voltages greater than approximately 1.5 V_{DC} and sink lower currents below this point. (See typical characteristics section and applications section).

Typical Performance Characteristics

Supply Current



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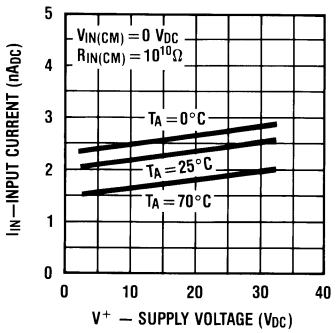
Input Current



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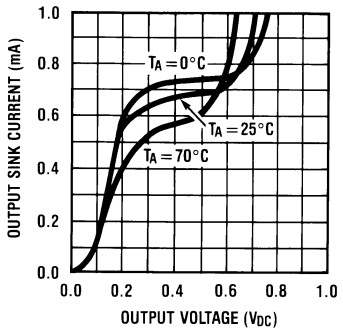
Output Sink Current



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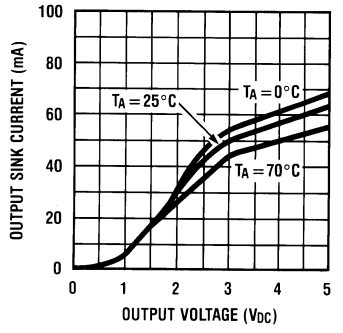
Output Sink Current



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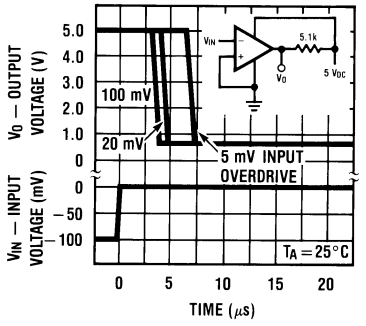
Response Times for Various Input Overdrives — Negative Transition



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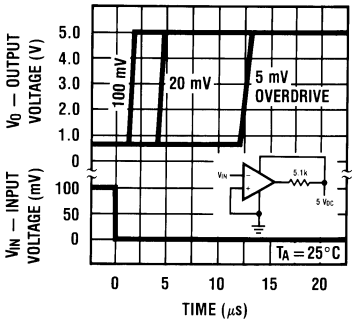
Response Times for Various Input Overdrives — Positive Transition



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Application Hints

All pins of any unused comparators should be tied to the negative supply.

The bias network of the LP339 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V_{DC} to 30 V_{DC}.

It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25˚C). An input clamp diode can be used as shown in the application section.

The output section of the LP339 has two distinct modes of operation-a Darlington mode and a grounded emitter mode. This unique drive circuit permits the LP339 to sink 30 mA at V_O=2 V_{DC} (Darlington mode) and 700 µA at V_O=0.4 V_{DC} (grounded emitter mode). *Figure 1* is a simplified schematic diagram of the LP339 output section.

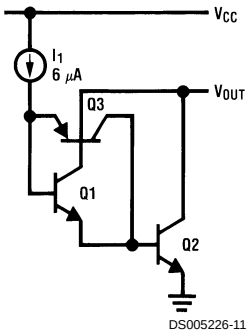


FIGURE 1.

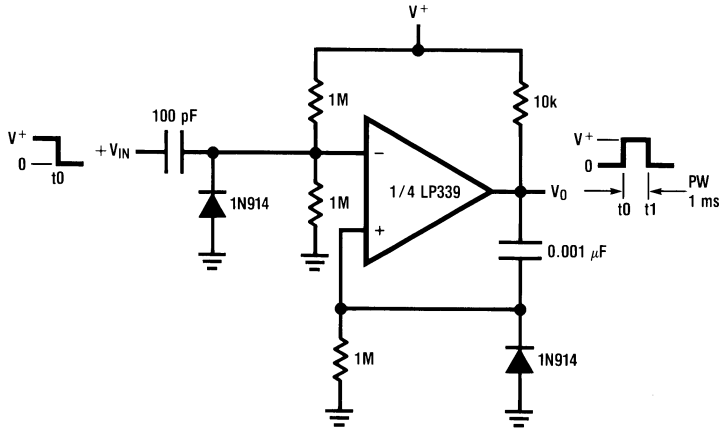
Notice that the output section is configured in a Darlington connection (ignoring Q3). Therefore, if the output voltage is held high enough (V_O≥1 V_{DC}), Q1 is not saturated and the output current is limited only by the product of the betas of Q1, Q2 and I1 (and the 60Ω R_{SAT} of Q2). The LP339 is thus capable of driving LED's, relays, etc. in this mode while maintaining an ultra-low power supply current of typically 60 µA.

If transistor Q3 were omitted, and the output voltage allowed to drop below about 0.8 V_{DC}, transistor Q1 would saturate and the output current would drop to zero. The circuit would, therefore, be unable to "pull" low current loads down to ground (or the negative supply, if used). Transistor Q3 has been included to bypass transistor Q1 under these conditions and apply the current I1 directly to the base of Q2. The output sink current is now approximately I1 times the beta of Q2 (700 µA at V_O=0.4 V_{DC}). The output of the LP339 exhibits a bi-modal characteristic with a smooth transition between modes. (See Output Sink Current graphs in Typical Performance Characteristics section.)

It is also important to note that in both cases the output is an uncommitted collector. Therefore, many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted power supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V+ terminal of the LP339 package.

Typical Applications (V^+=15 V_{DC})

One-Shot Multivibrator



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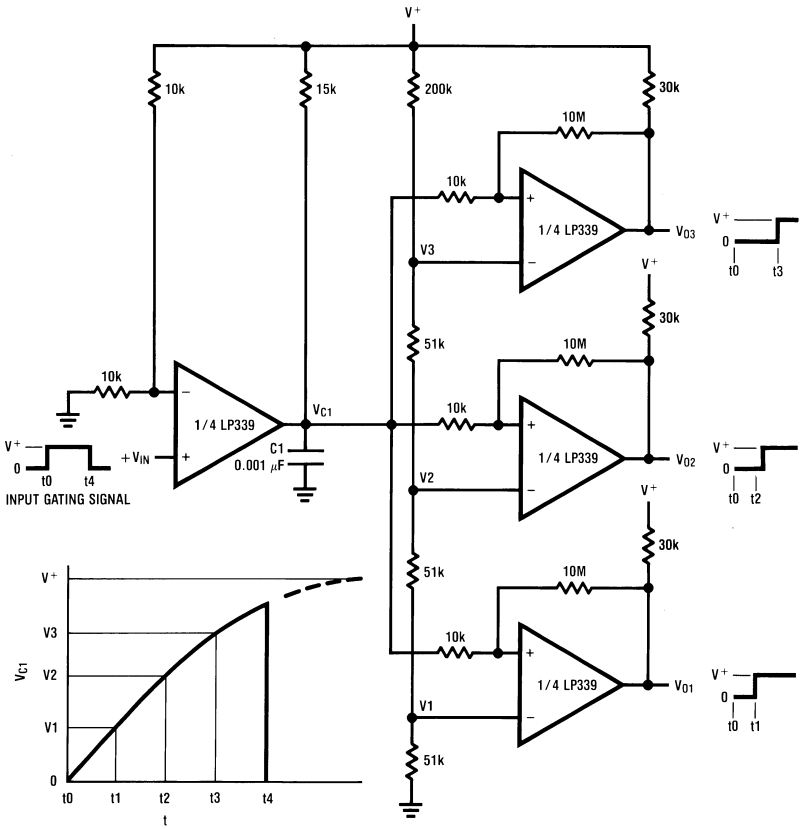
Time-Delay Generator



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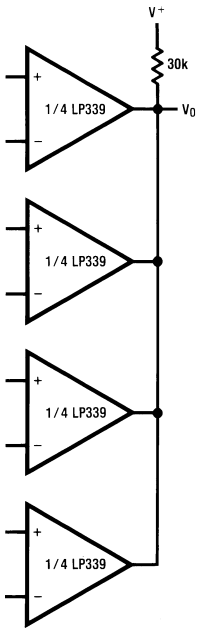
Typical Applications (V^+=15 V_{DC}) (Continued)

ORing the Outputs



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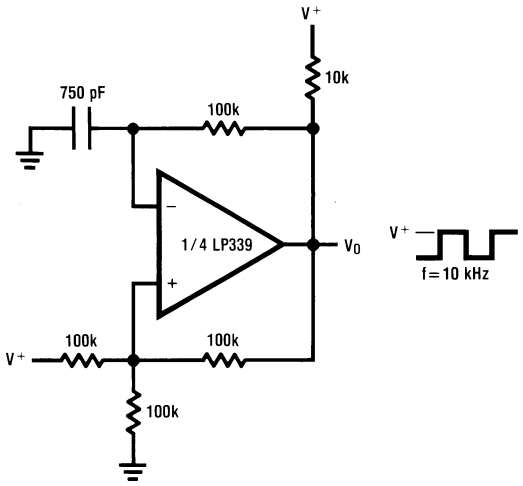
Squarewave Oscillator



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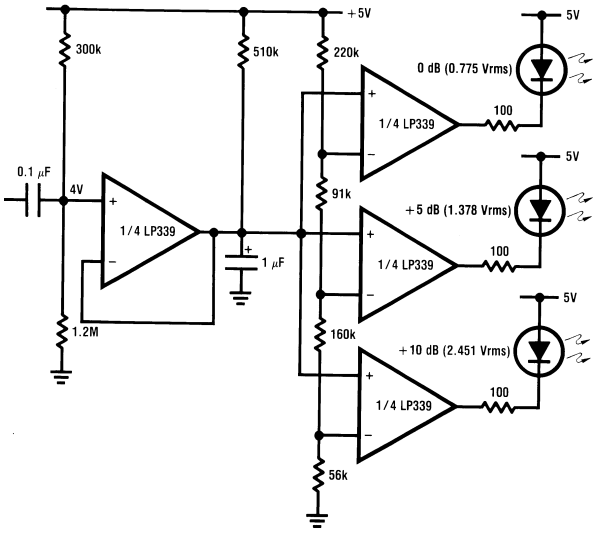
Typical Applications (V^+=15 V_{DC}) (Continued)

Three Level Audio Peak Indicator



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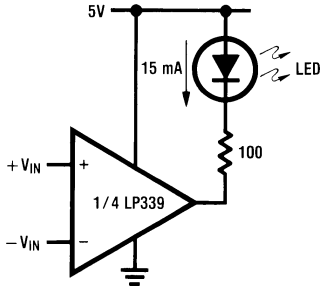
LED Driver



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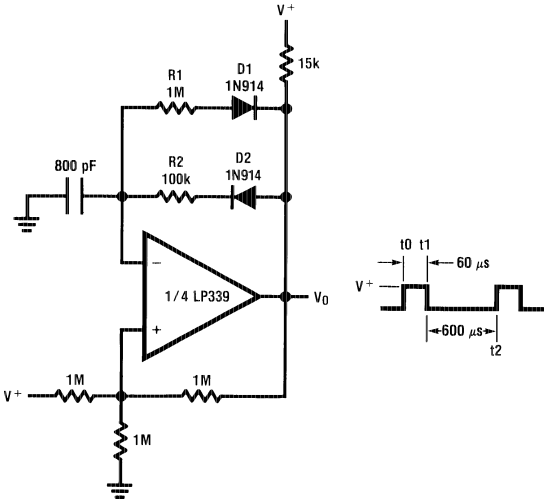
Pulse Generator



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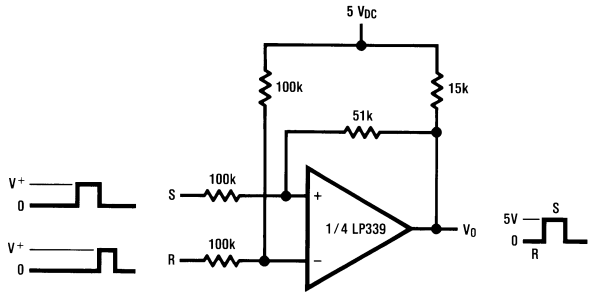
Typical Applications (V^+=15 V_{DC}) (Continued)

Bi-Stable Multivibrator



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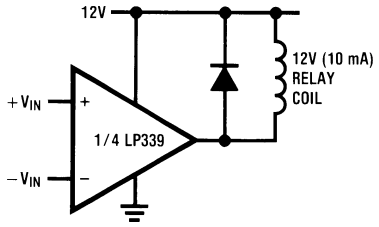
Relay Driver



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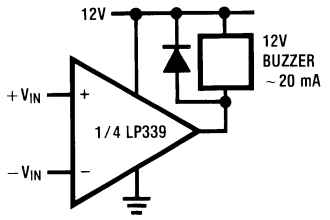
Buzzer Driver



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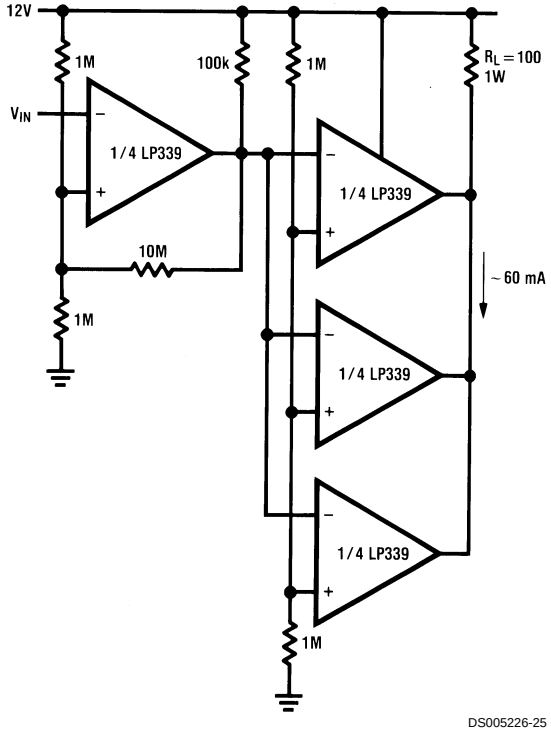
Comparator With 60 mA Sink Capability



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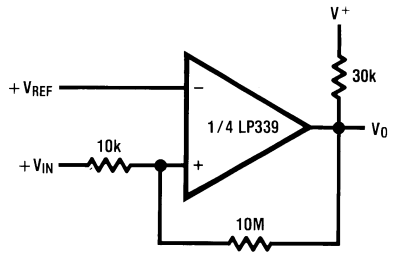
Typical Applications (V^+=15 V_{DC}) (Continued)

Non-Inverting Comparator with Hysteresis



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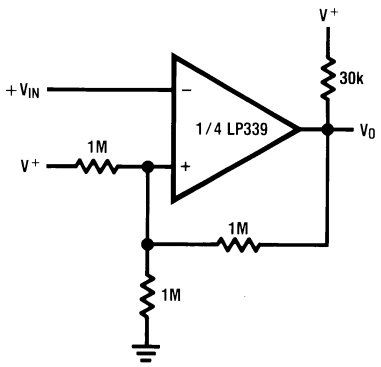
Inverting Comparator with Hysteresis



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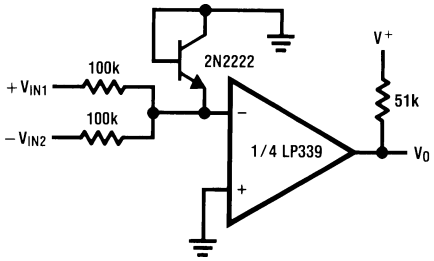
Comparing Input Voltages of Opposite Polarity



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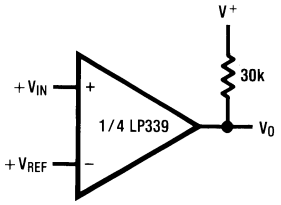
Basic Comparator



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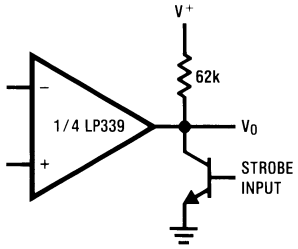
Output Strobing



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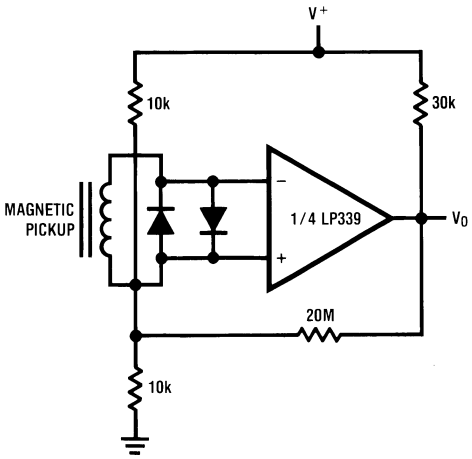
Transducer Amplifier



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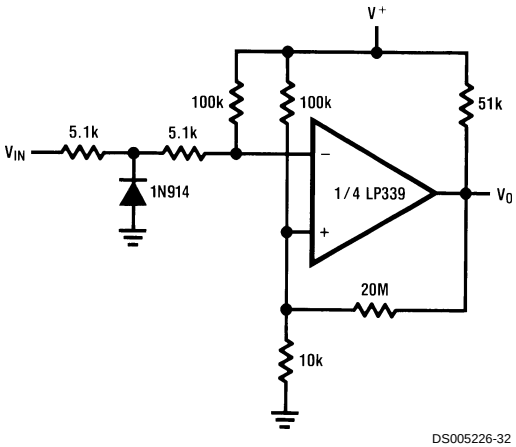
Zero Crossing Detector (Single Power Supply)



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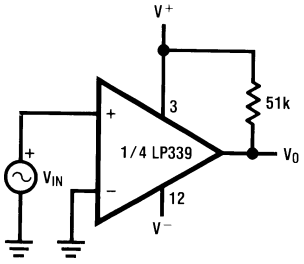
Typical Applications (V^+=15 V_{DC}) (Continued)

Split-Supply Applications
Zero Crossing Detector



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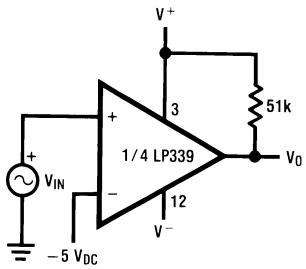
Comparator With a Negative Reference



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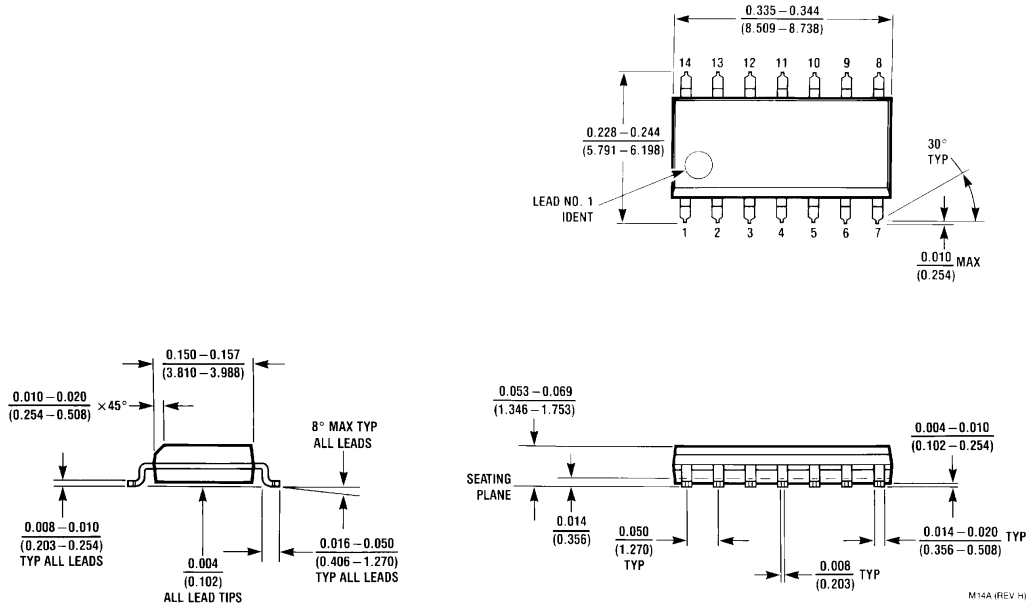
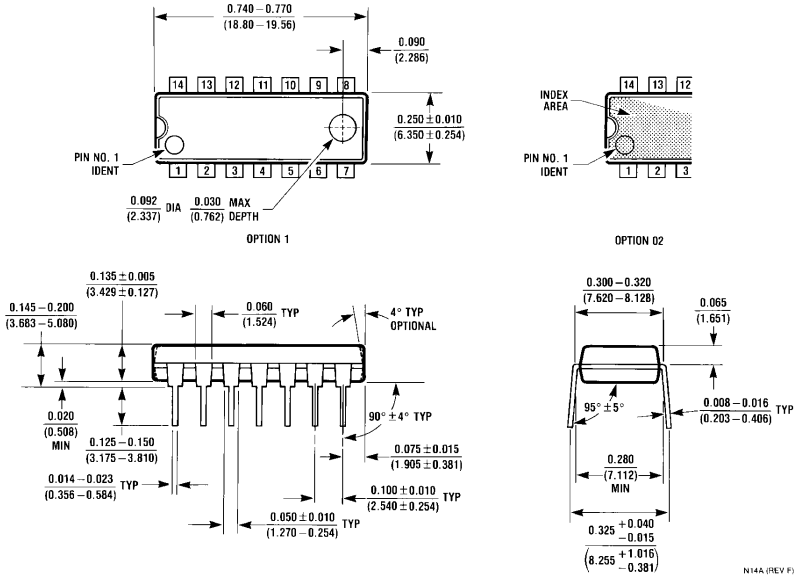
Physical Dimensions inches (millimeters) unless otherwise noted



S.O. Package (M)
Order Number LP339M or LP339MX
NS Package M14A



Molded Dual-In-Line Package (N)
Order Number LP339N
NS Package Number N14A

Notes

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP339M/NOPB	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LP339M
LP339M/NOPB.B	Active	Production	SOIC (D) | 14	55 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LP339M
LP339MX/NOPB	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LP339M
LP339MX/NOPB.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LP339M
LP339N/NOPB	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	0 to 70	LP339N
LP339N/NOPB.B	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	0 to 70	LP339N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

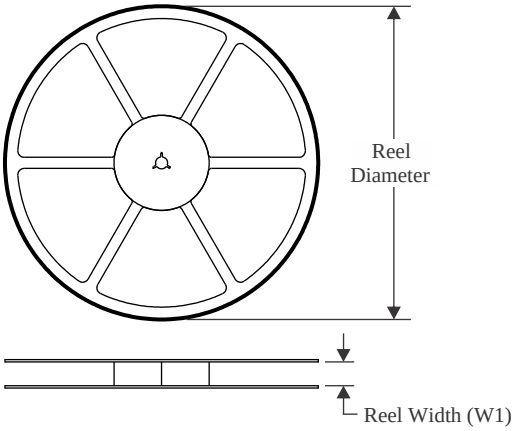
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

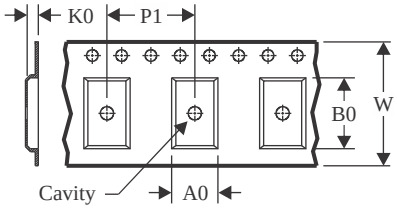
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

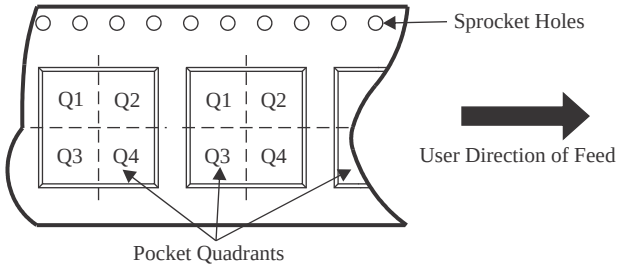


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

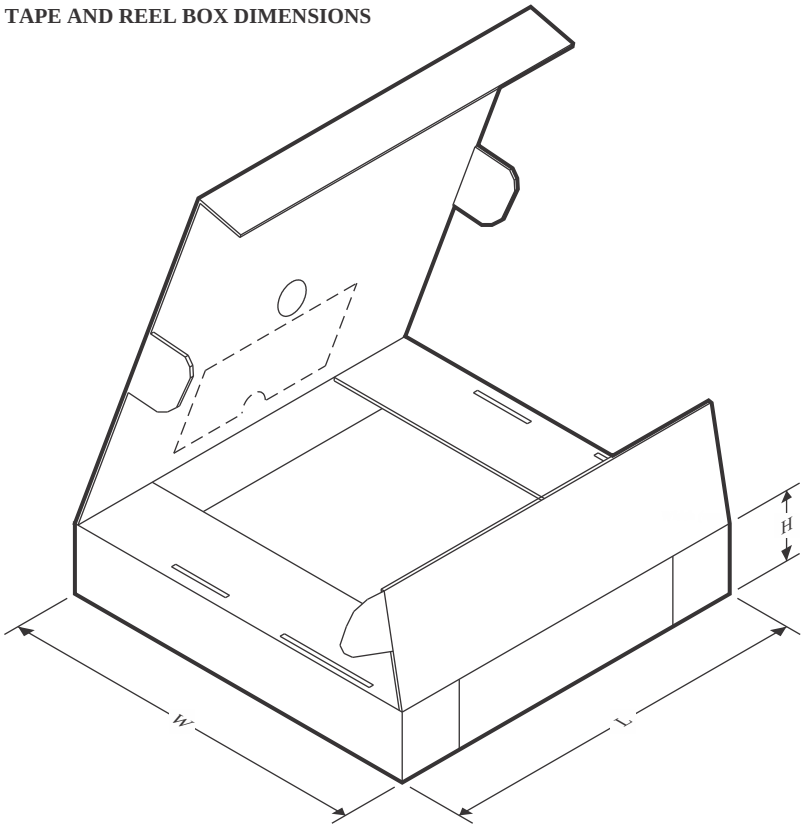
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP339MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

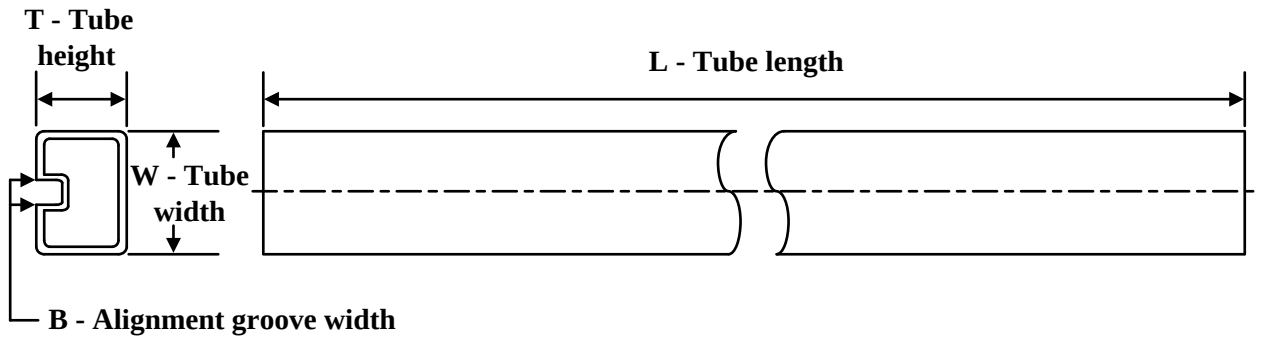
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP339MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP339M/NOPB	D	SOIC	14	55	495	8	4064	3.05
LP339M/NOPB.B	D	SOIC	14	55	495	8	4064	3.05
LP339N/NOPB	N	PDIP	14	25	502	14	11938	4.32
LP339N/NOPB.B	N	PDIP	14	25	502	14	11938	4.32

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