

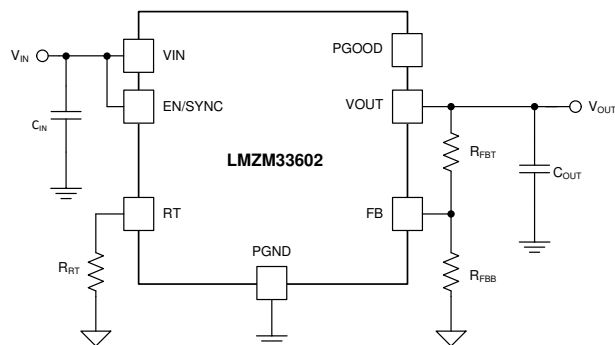
# LMZM33602 4-V to 36-V Input, 2-A Power Module in QFN Package

## 1 Features

- Complete integrated power solution
  - As few as four external components
  - Minimum solution size < 100 mm<sup>2</sup>
- 9-mm × 7-mm × 4-mm QFN package
  - All pins accessible from package perimeter
  - Pin compatible with 3-A LMZM33603
- Input voltage range: 4 V to 36 V
- Output voltage range: 1 V to 18 V
- Efficiencies up to 95%
- Adjustable switching frequency (200 kHz to 1.2 MHz)
- Allows synchronization to an external clock
- Power-good output
- Meets EN55011 class B radiated EMI standards
- Operating IC junction range: –40°C to +125°C
- Operating ambient range: –40°C to +105°C
- Create a custom design using the LMZM33602 with the [WEBENCH® Power Designer](#)

## 2 Applications

- [Factory and building automation](#)
- [Smart grid and energy](#)
- [Industrial](#)
- [Medical](#)
- [Defense](#)
- [Inverted output applications](#)



**Simplified Schematic**

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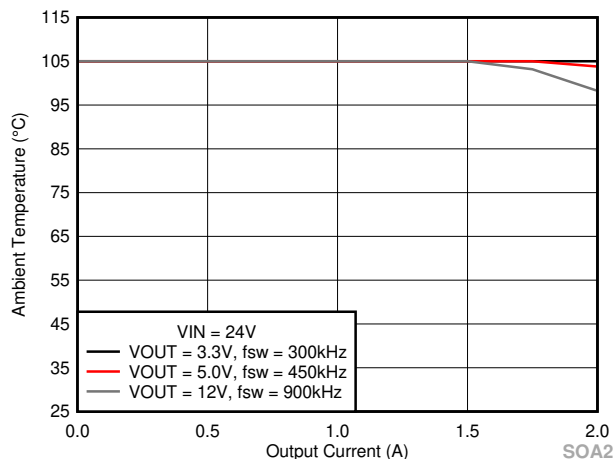
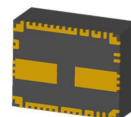
## 3 Description

The LMZM33602 power module is an easy-to-use integrated power solution that combines a 2-A, step-down, DC/DC converter with power MOSFETs, a shielded inductor, and passives into a low-profile package. This power solution requires as few as four external components and eliminates the loop compensation and magnetics part selection from the design process.

The 9-mm × 7-mm × 4-mm, 18-pin QFN package is easy to solder onto a printed circuit board and allows a compact, low-profile, point-of-load design. The full feature set, including power good, programmable UVLO, prebias start-up, overcurrent and overtemperature protections, make the LMZM33602 an excellent device for powering a wide range of applications.

### Device Information

| DEVICE NUMBER | PACKAGE  | BODY SIZE (NOM)   |
|---------------|----------|-------------------|
| LMZM33602     | QFN (18) | 9.00 mm × 7.00 mm |



**Safe Operating Area**



## Table of Contents

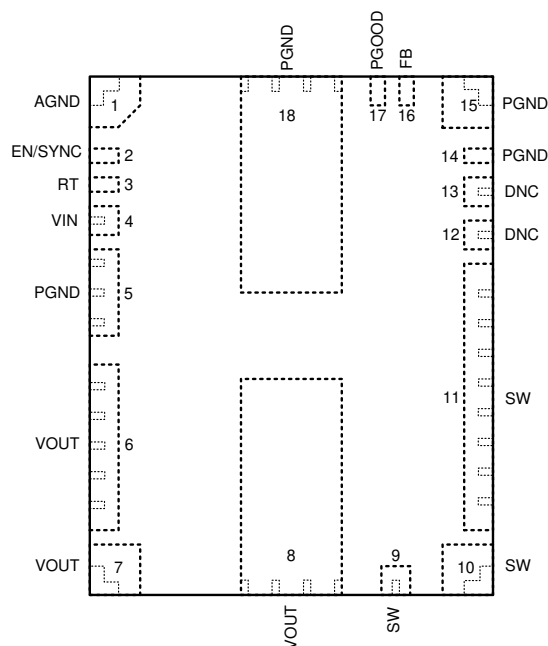
|                                                             |          |                                                          |           |
|-------------------------------------------------------------|----------|----------------------------------------------------------|-----------|
| <b>1 Features</b> .....                                     | <b>1</b> | <b>7 Detailed Description</b> .....                      | <b>10</b> |
| <b>2 Applications</b> .....                                 | <b>1</b> | 7.1 Overview.....                                        | 10        |
| <b>3 Description</b> .....                                  | <b>1</b> | 7.2 Functional Block Diagram.....                        | 10        |
| <b>4 Revision History</b> .....                             | <b>2</b> | 7.3 Feature Description.....                             | 11        |
| <b>5 Pin Configuration and Functions</b> .....              | <b>3</b> | 7.4 Device Functional Modes.....                         | 19        |
| Pin Functions.....                                          | 3        | <b>8 Application and Implementation</b> .....            | <b>20</b> |
| <b>6 Specifications</b> .....                               | <b>4</b> | 8.1 Application Information.....                         | 20        |
| 6.1 Absolute Maximum Ratings.....                           | 4        | 8.2 Typical Application.....                             | 20        |
| 6.2 ESD Ratings.....                                        | 4        | <b>9 Device and Documentation Support</b> .....          | <b>27</b> |
| 6.3 Recommended Operating Conditions.....                   | 4        | 9.1 Device Support.....                                  | 27        |
| 6.4 Thermal Information.....                                | 5        | 9.2 Documentation Support.....                           | 27        |
| 6.5 Electrical Characteristics.....                         | 5        | 9.3 Receiving Notification of Documentation Updates..... | 27        |
| 6.6 Switching Characteristics.....                          | 6        | 9.4 Support Resources.....                               | 27        |
| 6.7 Typical Characteristics ( $V_{IN} = 5\text{ V}$ ).....  | 7        | 9.5 Trademarks.....                                      | 27        |
| 6.8 Typical Characteristics ( $V_{IN} = 12\text{ V}$ )..... | 8        | 9.6 Electrostatic Discharge Caution.....                 | 27        |
| 6.9 Typical Characteristics ( $V_{IN} = 24\text{ V}$ )..... | 9        | 9.7 Glossary.....                                        | 27        |

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

|                                                                                                      |             |
|------------------------------------------------------------------------------------------------------|-------------|
| <b>Changes from Revision C (March 2018) to Revision D (August 2020)</b> .....                        | <b>Page</b> |
| • Updated the numbering format for tables, figures and cross-references throughout the document..... | 1           |
| • Updated Storage temperature range in <i>Absolute Maximum Ratings</i> .....                         | 4           |
| <b>Changes from Revision B (February 2018) to Revision C (March 2018)</b> .....                      | <b>Page</b> |
| • Added <i>Section 9.4</i> section.....                                                              | 24          |
| <b>Changes from Revision A (February 2018) to Revision B (February 2018)</b> .....                   | <b>Page</b> |
| • First release of production-data data sheet.....                                                   | 1           |
| <b>Changes from Revision * (December 2017) to Revision A (January 2018)</b> .....                    | <b>Page</b> |
| • Added new <i>Application</i> with link to SNVA800 app report; minor editorial updates.....         | 1           |
| • Added sentence re: inverting buck-boost topology to <i>Section 8.1</i> .....                       | 20          |

## 5 Pin Configuration and Functions



**Figure 5-1. RLR Package 18-Pin QFN Top View**

### Pin Functions

| PIN           |         | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|---------------|---------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NO.           | NAME    |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 1             | AGND    | G    | Analog ground. Zero voltage reference for internal references and logic. Do not connect this pin to PGND; the connection is made internal to the device. See the <a href="#">Section Layout</a> of the data sheet for a recommended layout.                                                                                                                                                                                                                                                                              |
| 2             | EN/SYNC | I    | EN - Enable input to regulator. High = On, Low = Off. Can be connected to VIN. Do not float. This pin can be used to set the input undervoltage lockout with two resistors. See <a href="#">Section 7.3.9</a> . SYNC - The internal oscillator can be synchronized to an external clock via AC-coupling. See <a href="#">Section 7.3.5</a> for details.                                                                                                                                                                  |
| 3             | RT      | I    | An external timing resistor connected between this pin and AGND adjusts the switching frequency of the device. If left open, the default switching frequency is 400 kHz.                                                                                                                                                                                                                                                                                                                                                 |
| 4             | VIN     | I    | Input supply voltage. Connect external input capacitors between this pin and PGND.                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 5, 14, 15, 18 | PGND    | G    | Power ground. This is the return current path for the power stage of the device. Connect pin 5 to the input source, the load, and to the bypass capacitors associated with VIN and VOUT using power ground planes on the PCB. <b>Pins 14 and 15 are not connected to PGND internal to the device and must be connected to PGND at pad 18.</b> Connect pad 18 to the power ground planes using multiple vias for good thermal performance. See <a href="#">Section Layout</a> of the data sheet for a recommended layout. |
| 6, 7, 8       | VOUT    | O    | Output voltage. These pins are connected to the internal output inductor. Connect these pins to the output load and connect external bypass capacitors between these pins and PGND.                                                                                                                                                                                                                                                                                                                                      |
| 9, 10, 11     | SW      | O    | Switch node. Connect these pins to a small copper island under the device for thermal relief. Do not place any external component on these pins or tie them to a pin of another function.                                                                                                                                                                                                                                                                                                                                |
| 12, 13        | DNC     | —    | Do not connect. <b>Each pin must be soldered to an isolated pad.</b> These pins connect to internal circuitry. Do not connect these pins to one another, AGND, PGND, or any other voltage.                                                                                                                                                                                                                                                                                                                               |
| 16            | FB      | I    | Feedback input. Connect the center point of the feedback resistor divider to this pin. Connect the upper resistor ( $R_{FBT}$ ) of the feedback divider to $V_{OUT}$ at the desired point of regulation. Connect the lower resistor ( $R_{FBB}$ ) of the feedback divider to AGND.                                                                                                                                                                                                                                       |
| 17            | PGOOD   | O    | Open drain output for power-good flag. Use a 10-k $\Omega$ to 100-k $\Omega$ pullup resistor to logic rail or other DC voltage no higher than 12 V.                                                                                                                                                                                                                                                                                                                                                                      |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating ambient temperature range (unless otherwise noted)<sup>(1)</sup>

|                                                                  |                                                        | MIN  | MAX                   | UNIT |
|------------------------------------------------------------------|--------------------------------------------------------|------|-----------------------|------|
| Input voltage                                                    | V <sub>IN</sub>                                        | −0.3 | 42                    | V    |
|                                                                  | EN/SYNC                                                | −5.5 | V <sub>IN</sub> + 0.3 | V    |
|                                                                  | PGOOD                                                  | −0.3 | 15                    | V    |
|                                                                  | FB, RT                                                 | −0.3 | 4.5                   | V    |
| Output voltage                                                   | SW                                                     | −1   | V <sub>IN</sub> + 0.3 | V    |
|                                                                  | SW (< 10-ns transients)                                | −5   | 42                    | V    |
|                                                                  | V <sub>OUT</sub>                                       | −0.3 | V <sub>IN</sub>       | V    |
| Sink current                                                     | PGOOD                                                  |      | 3                     | mA   |
| Mechanical shock                                                 | Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted |      | 500                   | G    |
| Mechanical vibration                                             | Mil-STD-883D, Method 2007.2, 20 to 2000 Hz             |      | 20                    | G    |
| Operating IC junction temperature, T <sub>J</sub> <sup>(2)</sup> |                                                        | −40  | 125                   | °C   |
| Operating ambient temperature, T <sub>A</sub> <sup>(2)</sup>     |                                                        | −40  | 105                   | °C   |
| Storage temperature, T <sub>stg</sub>                            |                                                        | −55  | 150                   | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The ambient temperature is the air temperature of the surrounding environment. The junction temperature is the temperature of the internal power IC when the device is powered. Operating below the maximum ambient temperature, as shown in the safe operating area (SOA) curves in the typical characteristics sections, ensures that the maximum junction temperature of any component inside the module is never exceeded.

### 6.2 ESD Ratings

|                    |                         |                                                                                | VALUE | UNIT |
|--------------------|-------------------------|--------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2500 | V    |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±750  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

Over operating ambient temperature range (unless otherwise noted)

|                                               | MIN              | MAX             | UNIT |
|-----------------------------------------------|------------------|-----------------|------|
| Input voltage, V <sub>IN</sub>                | 4 <sup>(1)</sup> | 36              | V    |
| Output voltage, V <sub>OUT</sub>              | 1                | 18              | V    |
| EN/SYNC voltage                               | −5               | V <sub>IN</sub> | V    |
| PGOOD pullup voltage, V <sub>PGOOD</sub>      | −0.3             | 12              | V    |
| PGOOD sink current, I <sub>PGOOD</sub>        |                  | 1               | mA   |
| Output current, I <sub>OUT</sub>              | 0                | 2               | A    |
| Operating ambient temperature, T <sub>A</sub> | −40              | 105             | °C   |

- (1) For output voltages ≤ 5 V, the recommended minimum V<sub>IN</sub> is 4 V or (V<sub>OUT</sub> + 1.5 V), whichever is greater. For output voltages > 5 V, the recommended minimum V<sub>IN</sub> is (1.3 × V<sub>OUT</sub>). See [Voltage Dropout](#) for information on voltage dropout.

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                                             | LMZM33602 | UNIT |
|-------------------------------|-------------------------------------------------------------|-----------|------|
|                               |                                                             | RLR (QFN) |      |
|                               |                                                             | 18 PINS   |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance <sup>(2)</sup>       | 18.9      | °C/W |
| $\psi_{JT}$                   | Junction-to-top characterization parameter <sup>(3)</sup>   | 2.0       | °C/W |
| $\psi_{JB}$                   | Junction-to-board characterization parameter <sup>(4)</sup> | 6.2       | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance,  $R_{\theta JA}$ , applies to devices soldered directly to a 63 mm × 63 mm, 4-layer PCB with 2 oz. copper and natural convection cooling. Additional airflow reduces  $R_{\theta JA}$ .
- (3) The junction-to-top board characterization parameter,  $\psi_{JT}$ , estimates the junction temperature,  $T_J$ , of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7).  $T_J = \psi_{JT} \times P_{dis} + T_T$ ; where  $P_{dis}$  is the power dissipated in the device and  $T_T$  is the temperature of the top of the device.
- (4) The junction-to-board characterization parameter,  $\psi_{JB}$ , estimates the junction temperature,  $T_J$ , of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7).  $T_J = \psi_{JB} \times P_{dis} + T_B$ ; where  $P_{dis}$  is the power dissipated in the device and  $T_B$  is the temperature of the board 1mm from the device.

## 6.5 Electrical Characteristics

Over –40°C to +105°C ambient temperature,  $V_{IN} = 24$  V,  $V_{OUT} = 5$  V,  $I_{OUT} = I_{OUT}$  maximum,  $f_{SW} = 450$  kHz (unless otherwise noted);  $C_{IN1} = 2 \times 4.7$ -μF, 50-V, 1210 ceramic;  $C_{IN2} = 100$ -μF, 50-V, electrolytic;  $C_{OUT} = 4 \times 22$ -μF, 25-V, 1210 ceramic. Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

| PARAMETER                                    |                                 | TEST CONDITIONS                                                                            | MIN                                   | TYP   | MAX   | UNIT |
|----------------------------------------------|---------------------------------|--------------------------------------------------------------------------------------------|---------------------------------------|-------|-------|------|
| <b>INPUT VOLTAGE (<math>V_{IN}</math>)</b>   |                                 |                                                                                            |                                       |       |       |      |
| $V_{IN}$                                     | Input voltage                   | Over $I_{OUT}$ range                                                                       | 4 <sup>(1)</sup>                      |       | 36    | V    |
| UVLO                                         | $V_{IN}$ undervoltage lockout   | $V_{IN}$ increasing                                                                        | 3.3                                   | 3.6   | 3.9   | V    |
|                                              |                                 | $V_{IN}$ decreasing                                                                        | 3                                     | 3.3   | 3.5   | V    |
| $I_{SHDN}$                                   | Shutdown supply current         | $V_{EN} = 0$ V, $V_{IN} = 12$ V                                                            |                                       | 2     | 4     | μA   |
| <b>OUTPUT VOLTAGE (<math>V_{OUT}</math>)</b> |                                 |                                                                                            |                                       |       |       |      |
| $V_{OUT(ADJ)}$                               | Output voltage adjust           | Over $I_{OUT}$ range                                                                       | 1                                     |       | 18    | V    |
| $V_{OUT(Ripple)}$                            | Output voltage ripple           | 20-MHz bandwidth                                                                           |                                       | 10    |       | mV   |
| <b>FEEDBACK</b>                              |                                 |                                                                                            |                                       |       |       |      |
| $V_{FB}$                                     | Feedback voltage <sup>(2)</sup> | $T_A = 25^\circ\text{C}$ , $I_{OUT} = 0$ A                                                 | 0.985                                 | 1     | 1.015 | V    |
|                                              |                                 | Over $V_{IN}$ range, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ , $I_{OUT} = 0$ A | 0.98                                  | 1     | 1.02  | V    |
|                                              | Load regulation                 | Over $I_{OUT}$ range, $T_A = 25^\circ\text{C}$                                             |                                       | 0.04% |       |      |
| $I_{FB}$                                     | Feedback leakage current        | $V_{FB} = 1$ V                                                                             |                                       | 10    |       | nA   |
| <b>CURRENT</b>                               |                                 |                                                                                            |                                       |       |       |      |
| $I_{OUT}$                                    | Output current                  | Natural convection, $T_A = 25^\circ\text{C}$                                               | 0                                     |       | 2     | A    |
|                                              | Overcurrent threshold           |                                                                                            |                                       | 3.6   |       | A    |
| <b>PERFORMANCE</b>                           |                                 |                                                                                            |                                       |       |       |      |
| $\eta$                                       | Efficiency                      | $V_{IN} = 24$ V,<br>$I_{OUT} = 1$ A                                                        | $V_{OUT} = 12$ V, $f_{SW} = 900$ kHz  | 94%   |       |      |
|                                              |                                 |                                                                                            | $V_{OUT} = 5$ V, $f_{SW} = 450$ kHz   | 90%   |       |      |
|                                              |                                 |                                                                                            | $V_{OUT} = 3.3$ V, $f_{SW} = 300$ kHz | 88%   |       |      |
|                                              |                                 | $V_{IN} = 12$ V,<br>$I_{OUT} = 1$ A                                                        | $V_{OUT} = 5$ V, $f_{SW} = 450$ kHz   | 93%   |       |      |
|                                              |                                 |                                                                                            | $V_{OUT} = 3.3$ V, $f_{SW} = 300$ kHz | 91%   |       |      |
|                                              |                                 |                                                                                            | $V_{OUT} = 2.5$ V, $f_{SW} = 250$ kHz | 89%   |       |      |
|                                              | Transient response              | 25% to 75%<br>load step<br>1 A/μs slew rate                                                | Over/undershoot                       | 90    |       | mV   |
|                                              |                                 |                                                                                            | Recovery time                         | 55    |       | μs   |

**LMZM33602**

SNVSAO4D – DECEMBER 2017 – REVISED AUGUST 2020

Over  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$  ambient temperature,  $V_{\text{IN}} = 24\text{ V}$ ,  $V_{\text{OUT}} = 5\text{ V}$ ,  $I_{\text{OUT}} = I_{\text{OUT}}$  maximum,  $f_{\text{sw}} = 450\text{ kHz}$  (unless otherwise noted);  $C_{\text{IN}1} = 2 \times 4.7\text{-}\mu\text{F}$ , 50-V, 1210 ceramic;  $C_{\text{IN}2} = 100\text{-}\mu\text{F}$ , 50-V, electrolytic;  $C_{\text{OUT}} = 4 \times 22\text{-}\mu\text{F}$ , 25-V, 1210 ceramic. Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

| PARAMETER           |                                         | TEST CONDITIONS                                            | MIN                | TYP               | MAX                | UNIT |
|---------------------|-----------------------------------------|------------------------------------------------------------|--------------------|-------------------|--------------------|------|
| SOFT START          |                                         |                                                            |                    |                   |                    |      |
| T <sub>SS</sub>     | Internal soft start time                |                                                            |                    | 6                 |                    | ms   |
| THERMAL             |                                         |                                                            |                    |                   |                    |      |
| T <sub>SHDN</sub>   | Thermal shutdown                        | Shutdown temperature                                       |                    | 170               |                    | °C   |
|                     |                                         | Hysteresis                                                 |                    | 15                |                    | °C   |
| ENABLE (EN)         |                                         |                                                            |                    |                   |                    |      |
| V <sub>EN-H</sub>   | EN rising threshold                     |                                                            | 1.4                | 1.55              | 1.7                | V    |
| V <sub>EN-HYS</sub> | EN hysteresis voltage                   |                                                            |                    | 0.4               |                    | V    |
| I <sub>EN</sub>     | EN Input leakage current                | V <sub>IN</sub> = 4 V to 36 V, V <sub>EN</sub> = 2 V       |                    | 10                | 100                | nA   |
|                     |                                         | V <sub>IN</sub> = 4 V to 36 V, V <sub>EN</sub> = 36 V      |                    |                   | 1                  | μA   |
| POWER GOOD (PGOOD)  |                                         |                                                            |                    |                   |                    |      |
| V <sub>PGOOD</sub>  | PGOOD thresholds                        | V <sub>OUT</sub> rising (good)                             | 92%                | 94%               | 96.5%              |      |
|                     |                                         | V <sub>OUT</sub> rising (fault)                            | 104%               | 107%              | 110%               |      |
|                     |                                         | V <sub>OUT</sub> falling hysteresis                        |                    | 1.5%              |                    |      |
|                     | Minimum V <sub>IN</sub> for valid PGOOD | 50-μA pullup, V <sub>EN</sub> = 0 V, T <sub>A</sub> = 25°C |                    |                   | 1.5                | V    |
|                     | PGOOD low voltage                       | 0.5-mA pullup, V <sub>EN</sub> = 0 V                       |                    |                   | 0.4                | V    |
| CAPACITANCE         |                                         |                                                            |                    |                   |                    |      |
| C <sub>IN</sub>     | External input capacitance              | Ceramic type                                               | 9.4 <sup>(3)</sup> |                   |                    | μF   |
|                     |                                         | Non-ceramic type                                           |                    | 47 <sup>(3)</sup> |                    | μF   |
| C <sub>OUT</sub>    | External output capacitance             |                                                            | min <sup>(4)</sup> |                   | max <sup>(5)</sup> | μF   |

- (1) See [Voltage Dropout](#) for information on voltage dropout.
- (2) The overall output voltage tolerance will be affected by the tolerance of the external  $R_{\text{FBT}}$  and  $R_{\text{FBB}}$  resistors.
- (3) A minimum of 9.4  $\mu\text{F}$  ( $2 \times 4.7\text{ }\mu\text{F}$ ) ceramic input capacitance is required for proper operation. An additional 47  $\mu\text{F}$  of bulk capacitance is recommended for applications with transient load requirements. See the [Input Capacitors](#) section of the datasheet for further guidance.
- (4) The minimum amount of required output capacitance varies depending on the output voltage (see [Output Capacitor Selection](#)). A minimum amount of ceramic output capacitance is required. Locate the capacitance close to the device. Adding additional ceramic or non-ceramic capacitance close to the load improves the response of the regulator to load transients.
- (5) The maximum allowable output capacitance varies depending on the output voltage (see [Output Capacitor Selection](#)).

## 6.6 Switching Characteristics

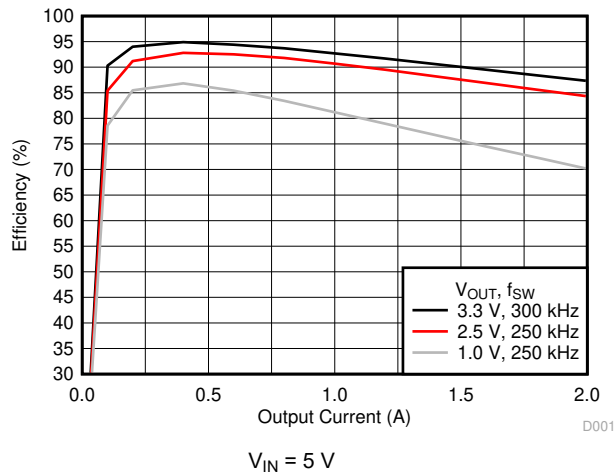
Over operating ambient temperature range (unless otherwise noted)

Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm, and are provided for reference only.

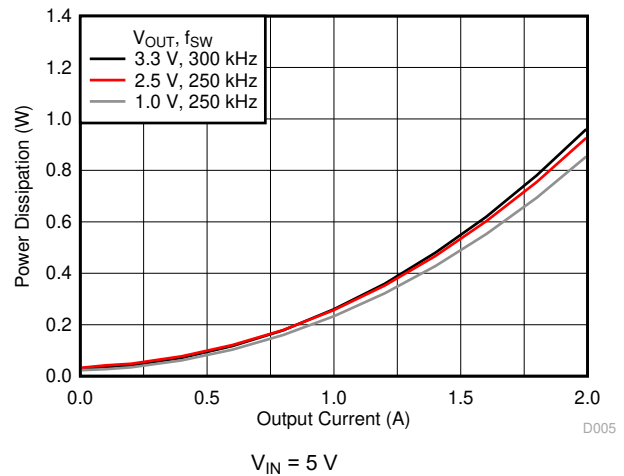
| PARAMETER                                           |                                                                       | TEST CONDITIONS | MIN | TYP | MAX  | UNIT |
|-----------------------------------------------------|-----------------------------------------------------------------------|-----------------|-----|-----|------|------|
| <b>FREQUENCY (RT) and SYNCHRONIZATION (EN/SYNC)</b> |                                                                       |                 |     |     |      |      |
| $f_{\text{sw}}$                                     | Default switching frequency                                           | RT pin = open   | 340 | 400 | 460  | kHz  |
|                                                     | Switching frequency range                                             |                 | 200 |     | 1200 | kHz  |
| $V_{\text{SYNC}}$                                   | Peak-to-peak amplitude of SYNC clock AC signal (measured at SYNC pin) |                 | 2.8 |     | 5.5  | V    |
| $T_{\text{S-MIN}}$                                  | Minimum SYNC ON/OFF time                                              |                 |     | 100 |      | ns   |

## 6.7 Typical Characteristics ( $V_{IN} = 5\text{ V}$ )

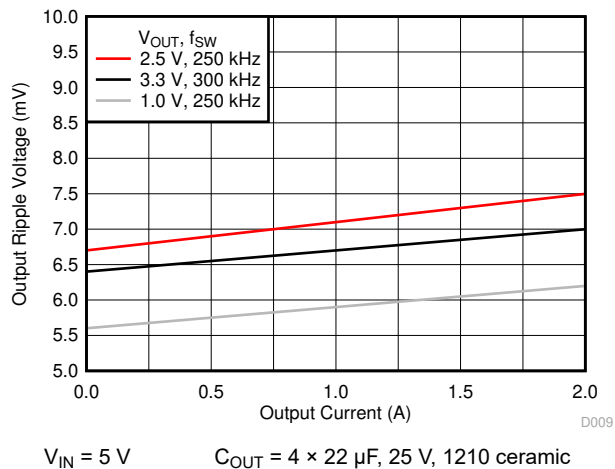
The typical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the device.



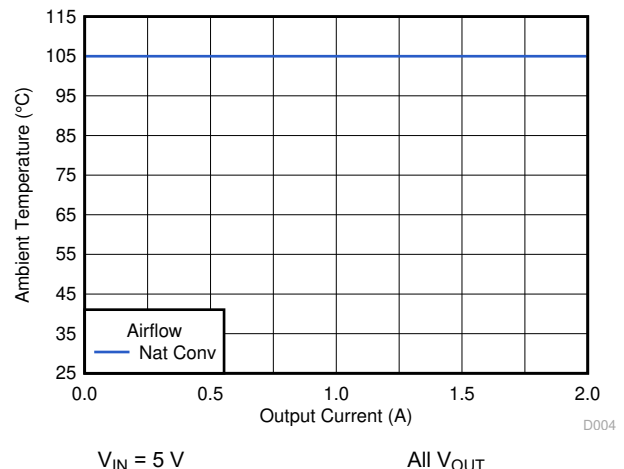
**Figure 6-1. Efficiency vs Output Current**



**Figure 6-2. Power Dissipation vs Output Current**



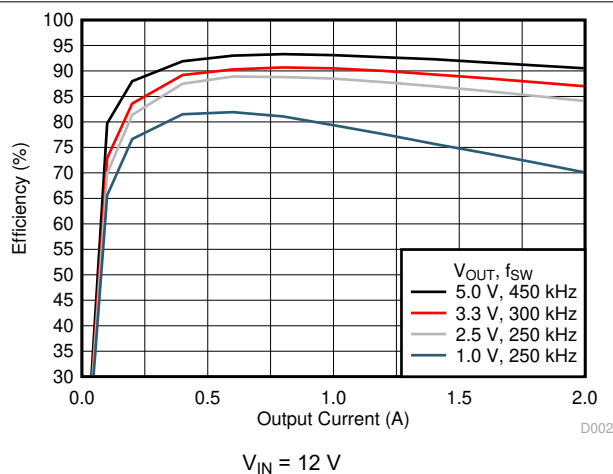
**Figure 6-3. Voltage Ripple vs Output Current**



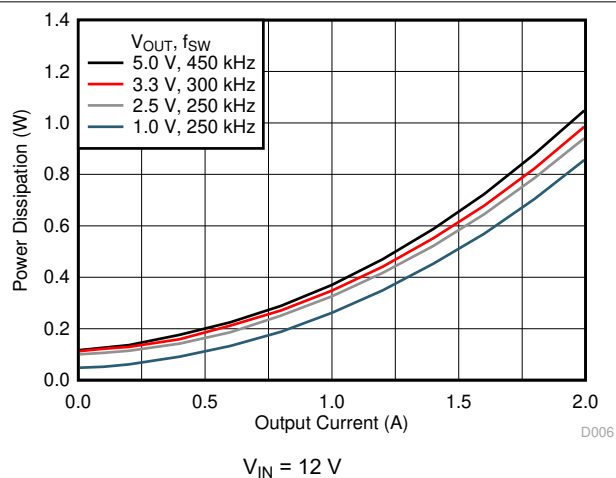
**Figure 6-4. Safe Operating Area**

## 6.8 Typical Characteristics ( $V_{IN} = 12\text{ V}$ )

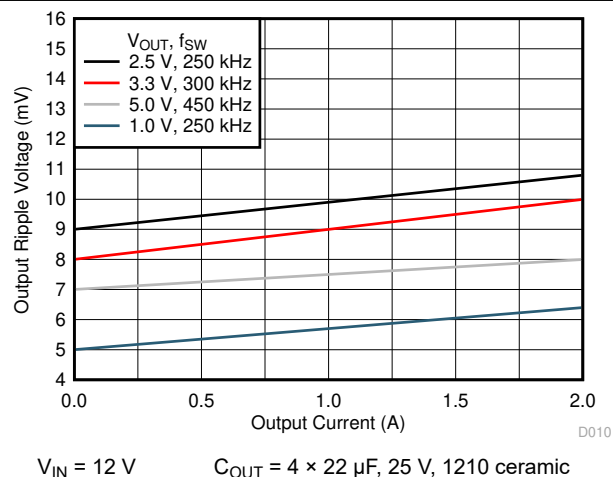
The typical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the device.



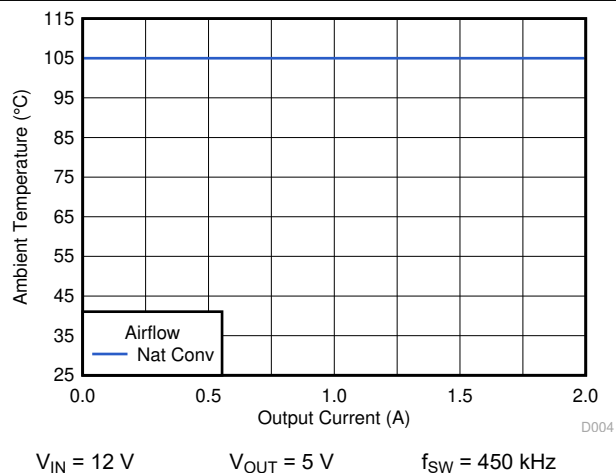
**Figure 6-5. Efficiency vs Output Current**



**Figure 6-6. Power Dissipation vs Output Current**



**Figure 6-7. Voltage Ripple vs Output Current**

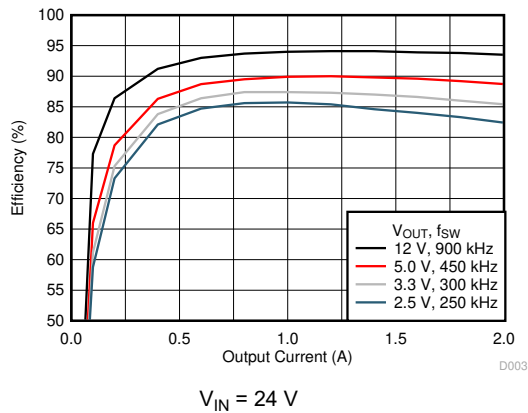


**Figure 6-8. Safe Operating Area**

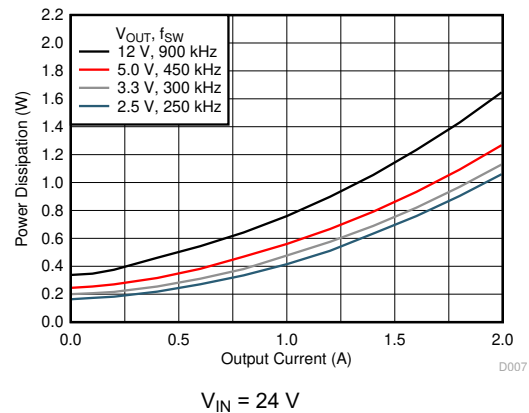


## 6.9 Typical Characteristics ( $V_{IN} = 24\text{ V}$ )

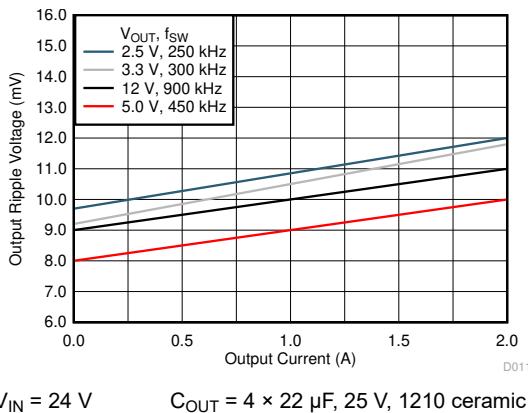
The typical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the device.



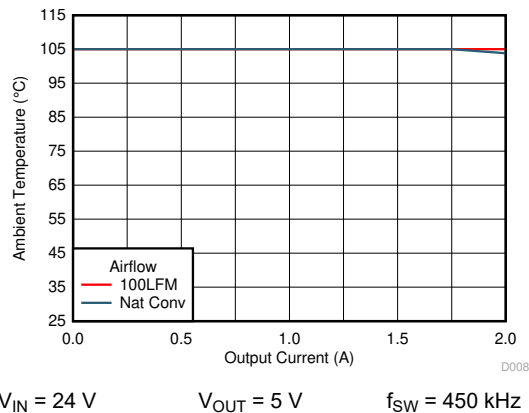
**Figure 6-9. Efficiency vs Output Current**



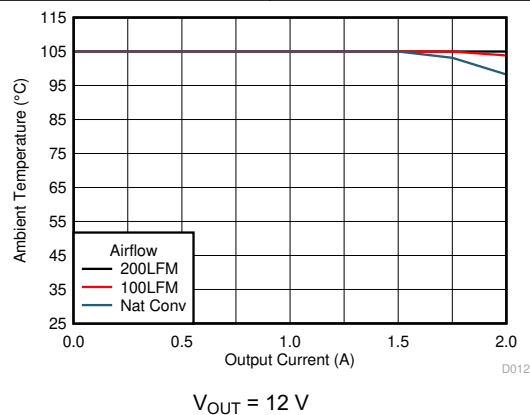
**Figure 6-10. Power Dissipation vs Output Current**



**Figure 6-11. Voltage Ripple vs Output Current**



**Figure 6-12. Safe Operating Area**



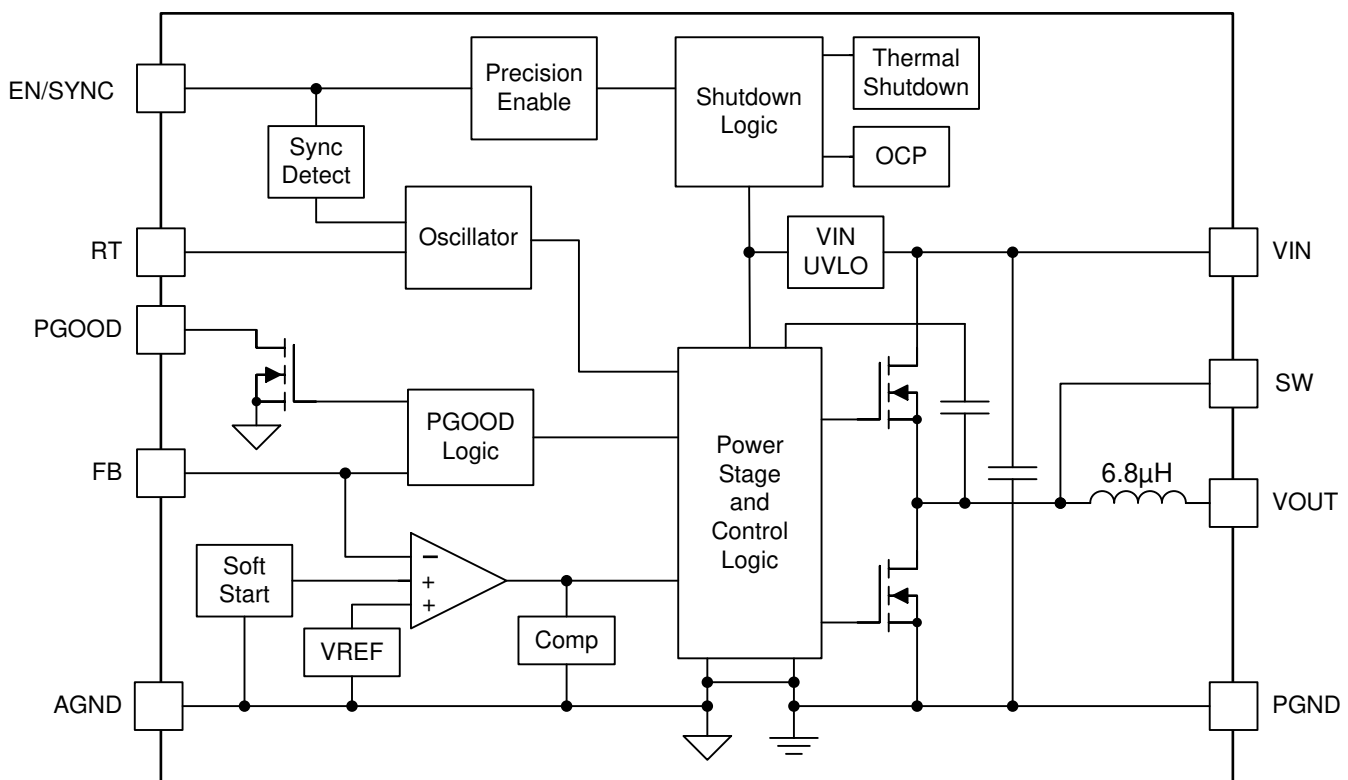
**Figure 6-13. Safe Operating Area**

## 7 Detailed Description

### 7.1 Overview

The LMZM33602 is a full-featured, 36-V input, 2-A, synchronous step-down converter with PWM, MOSFETs, shielded inductor, and control circuitry integrated into a low-profile, overmolded package. The device integration enables small designs, while providing the ability to adjust key parameters to meet specific design requirements. The LMZM33602 provides an output voltage range of 1 V to 18 V. An external resistor divider is used to adjust the output voltage to the desired value. The switching frequency can also be adjusted, by either an external resistor or a sync signal, which allows the LMZM33602 to accommodate a variety of input and output voltage conditions as well as optimize efficiency. The device provides accurate voltage regulation over a wide load range by using a precision internal voltage reference. Input undervoltage lockout is internally set at 3.6 V (typical), but can be adjusted upward using a resistor divider on the EN/SYNC pin of the device. The EN/SYNC pin can also be pulled low to put the device into standby mode to reduce input quiescent current. A power-good signal is provided to indicate when the output is within its nominal voltage range. Thermal shutdown and current limit features protect the device during an overload condition. An 18-pin, QFN package that includes exposed bottom pads provides a thermally enhanced solution for space-constrained applications.

### 7.2 Functional Block Diagram



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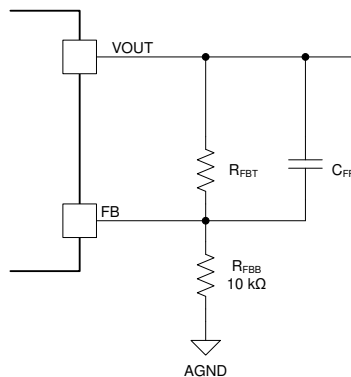
## 7.3 Feature Description

### 7.3.1 Adjusting the Output Voltage

A resistor divider connected to the FB pin (pin 16) programs the output voltage of the LMZM33602. The output voltage adjustment range is from 1 V to 18 V. [Figure 7-1](#) shows the feedback resistor connections for setting the output voltage. The recommended value of  $R_{FBB}$  is 10 k $\Omega$ . The value for  $R_{FBT}$  can be calculated using [Equation 1](#). Depending on the output voltage, a feedforward capacitor,  $C_{FF}$ , can be required for optimum transient performance. [Table 7-1](#) lists the standard external  $R_{FBT}$  and  $C_{FF}$  values for several output voltages between 2.5 V and 18 V. [Table 7-2](#) lists the values for output voltages below 2.5 V. Additionally, [Table 7-1](#) and [Table 7-2](#) include the recommended switching frequency ( $F_{SW}$ ), the frequency setting resistor ( $R_{RT}$ ), and the minimum and maximum output capacitance for each of the output voltages listed.

For designs with  $R_{FBB}$  other than 10 k $\Omega$ , adjust  $C_{FF}$  and  $R_{FBT}$  such that  $(C_{FF} \times R_{FBT})$  is unchanged and adjust  $R_{FBT}$  such that  $(R_{FBT} / R_{FBB})$  is unchanged.

$$R_{FBT} = 10 \times (V_{OUT} - 1)(k\Omega) \quad (1)$$



**Figure 7-1. Setting the Output Voltage**

**Table 7-1. Required Component Values ( $V_{OUT} \geq 2.5$  V)**

| $V_{OUT}$ (V) | $R_{FBT}$ (k $\Omega$ ) <sup>(3)</sup> | $C_{FF}$ (pF) | $f_{SW}$ (kHz) | $R_{RT}$ (k $\Omega$ ) | $C_{OUT(min)}$ ( $\mu$ F) <sup>(1)</sup> | $C_{OUT(max)}$ ( $\mu$ F) <sup>(2)</sup> |
|---------------|----------------------------------------|---------------|----------------|------------------------|------------------------------------------|------------------------------------------|
| 2.5           | 15.0                                   | 220           | 250            | 162                    | 150                                      | 400                                      |
| 3.3           | 23.2                                   | 150           | 300            | 133                    | 88                                       | 300                                      |
| 5             | 40.2                                   | 100           | 450            | 88.7                   | 66                                       | 200                                      |
| 6             | 49.9                                   | 68            | 550            | 71.5                   | 54                                       | 160                                      |
| 7.5           | 64.9                                   | 47            | 650            | 60.4                   | 40                                       | 130                                      |
| 9             | 80.6                                   | 47            | 700            | 56.2                   | 36                                       | 110                                      |
| 12            | 110                                    | open          | 900            | 44.2                   | 22                                       | 80                                       |
| 13.5          | 124                                    | open          | 1000           | 39.2                   | 22                                       | 75                                       |
| 15            | 140                                    | open          | 1100           | 35.7                   | 20                                       | 65                                       |
| 18            | 169                                    | open          | 1200           | 33.2                   | 16                                       | 55                                       |

- (1) For output voltages  $\geq 2.5$  V, the minimum required output capacitance must be comprised of **ceramic** type and account for DC bias and temperature derating.
- (2) The maximum output capacitance must include the required ceramic  $C_{OUT(min)}$ . Additional capacitance, may be ceramic type, low-ESR polymer type, or a combination of the two.
- (3)  $R_{FBB} = 10.0$  k $\Omega$

**Table 7-2. Required Component Values ( $V_{OUT} < 2.5$  V)**

| $V_{OUT}$ (V) | $R_{FBT}$ (k $\Omega$ ) <sup>(1)</sup> | $C_{FF}$ (pF) | $f_{SW}$ (kHz) | $R_{RT}$ (k $\Omega$ ) | $C_{OUT}$                                   |
|---------------|----------------------------------------|---------------|----------------|------------------------|---------------------------------------------|
| 1 to 2.5      | See <a href="#">Equation 1</a>         | open          | 250            | 162                    | 150- $\mu$ F ceramic + 470- $\mu$ F polymer |

- (1)  $R_{FBB} = 10$  k $\Omega$ . For  $V_{OUT} = 1$  V,  $R_{FBB} =$  open and  $R_{FBT} = 0$   $\Omega$ .

### 7.3.2 Feedforward Capacitor, $C_{FF}$

The LMZM33602 is internally compensated to be stable over the operating frequency and output voltage range. However, depending on the output voltage, an additional feedforward capacitor can be required. TI recommends an external feedforward capacitor,  $C_{FF}$ , be placed in parallel with the top resistor divider,  $R_{FBT}$  for optimum transient performance. The value for  $C_{FF}$  can be calculated using [Equation 2](#).

$$C_{FF} = \frac{1000}{4\pi \left( \frac{8.32}{V_{OUT} \times C_{OUT}} \right) \times R_{FBT}} \text{ (pF)} \quad (2)$$

where

- $C_{OUT}$  is the value after derating in  $\mu$ F
- $R_{FBT}$  is in k $\Omega$

Refer to [Table 7-1](#) for the recommended  $C_{FF}$  value for several output voltages.

### 7.3.3 Voltage Dropout

Voltage dropout is the difference between the input voltage and output voltage that is required to maintain output voltage regulation while providing the rated output current.

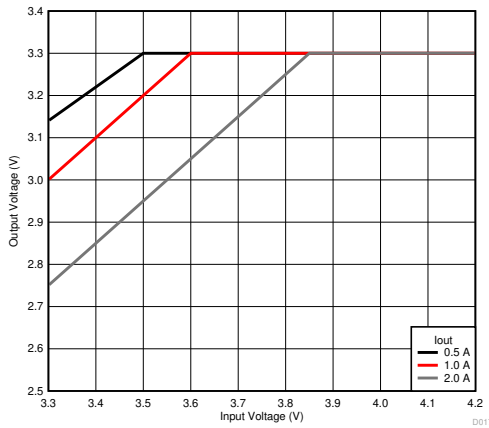
To ensure the LMZM33602 maintains output voltage regulation at the recommended switching frequency, over the operating temperature range, the following requirements apply:

For output voltages  $\leq 5$  V, the minimum  $V_{IN}$  is 4 V or ( $V_{OUT} + 1.5$  V), whichever is greater.

For output voltages  $> 5$  V, the minimum  $V_{IN}$  is ( $1.3 \times V_{OUT}$ ).

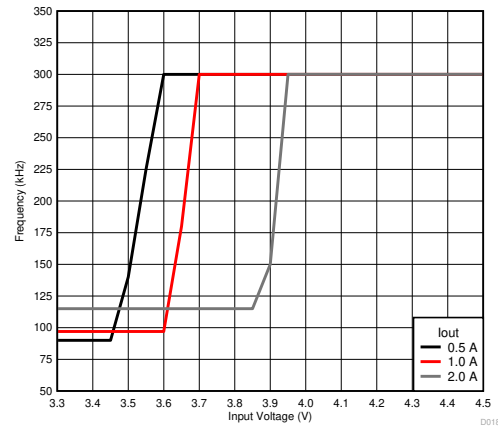
However, if fixed switching frequency operation is not required, the LMZM33602 operates in a frequency foldback mode when the dropout voltage is less than the recommendations above. Frequency foldback reduces the switching frequency to allow the output voltage to maintain regulation as input voltage decreases. [Figure 7-2](#) through [Figure 7-7](#) show typical dropout voltage and frequency foldback curves for 3.3-V, 5-V, and 12-V outputs

at  $T_A = 25^\circ\text{C}$ . (Note: As ambient temperature increases, dropout voltage and frequency foldback occur at higher input voltage.)



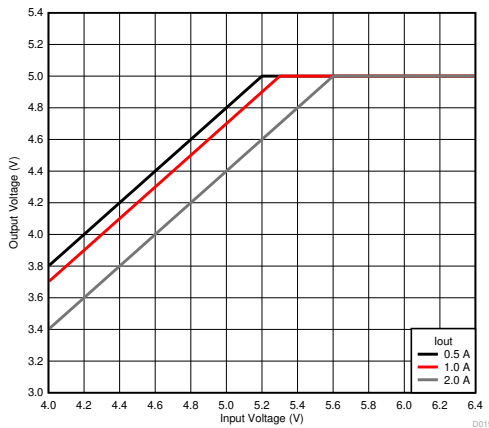
$V_{OUT} = 3.3\text{ V}$   $f_{SW} = 300\text{ kHz}$

**Figure 7-2. Voltage Dropout**



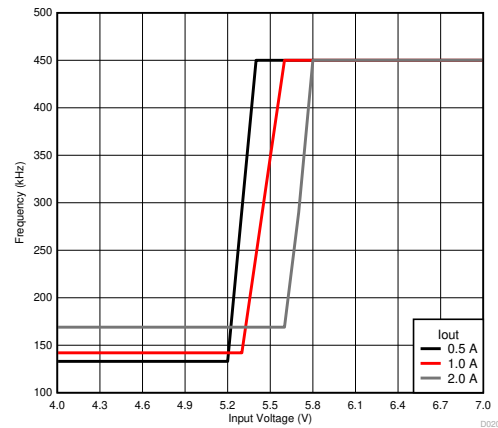
$V_{OUT} = 3.3\text{ V}$   $f_{SW} = 300\text{ kHz}$

**Figure 7-3. Frequency Foldback**



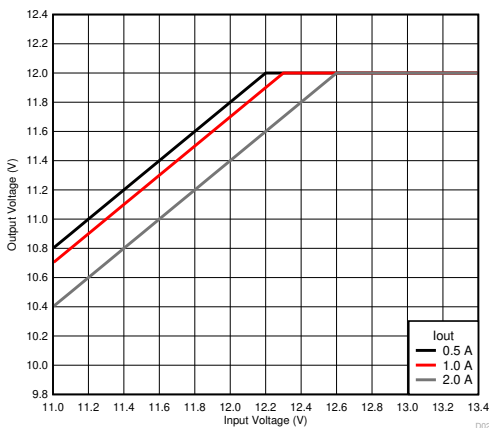
$V_{OUT} = 5\text{ V}$   $f_{SW} = 450\text{ kHz}$

**Figure 7-4. Voltage Dropout**



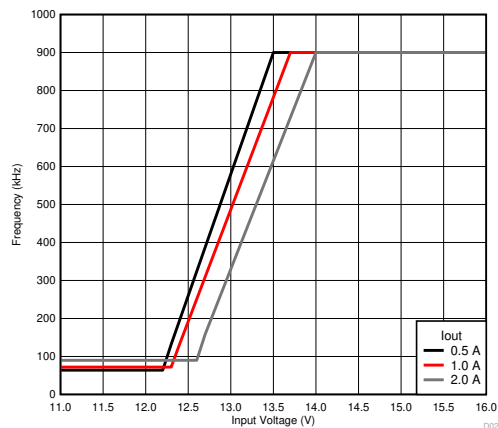
$V_{OUT} = 5\text{ V}$   $f_{SW} = 450\text{ kHz}$

**Figure 7-5. Frequency Foldback**



$V_{OUT} = 12\text{ V}$   $f_{SW} = 900\text{ kHz}$

**Figure 7-6. Voltage Dropout**



$V_{OUT} = 12\text{ V}$   $f_{SW} = 900\text{ kHz}$

**Figure 7-7. Frequency Foldback**

### 7.3.4 Switching Frequency (RT)

The switching frequency range of the LMZM33602 is 200 kHz to 1.2 MHz. The switching frequency can easily be set by connecting a resistor ( $R_{RT}$ ) between the RT pin and AGND. Additionally, the RT pin can be left floating and the LMZM33602 will operate at 400 kHz default switching frequency. Use Equation 3 to calculate the  $R_{RT}$  value for a desired frequency or simply select from Table 7-3.

The switching frequency must be selected based on the output voltage setting of the device and the operating input voltage. See Table 7-3 for  $R_{RT}$  resistor values and the allowable output voltage range for a given switching frequency for three common input voltages.

$$R_{RT} = \left( \frac{40200}{f_{sw} \text{ (kHz)}} \right) - 0.6 \text{ (k}\Omega\text{)} \quad (3)$$

**Table 7-3. Switching Frequency vs Output Voltage**

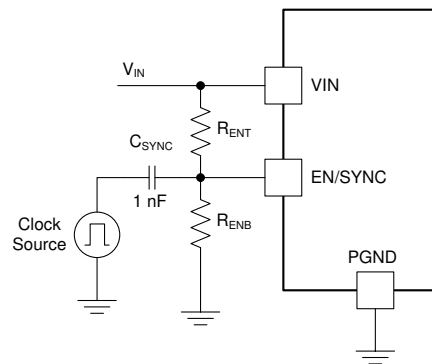
| SWITCHING<br>FREQUENCY<br>(kHz) | $R_{RT}$<br>RESISTOR<br>(k $\Omega$ ) | $V_{IN} = 5 \text{ V } (\pm 5\%)$ |     | $V_{IN} = 12 \text{ V } (\pm 5\%)$ |     | $V_{IN} = 24 \text{ V } (\pm 5\%)$ |      |
|---------------------------------|---------------------------------------|-----------------------------------|-----|------------------------------------|-----|------------------------------------|------|
|                                 |                                       | $V_{OUT} \text{ RANGE (V)}$       |     | $V_{OUT} \text{ RANGE (V)}$        |     | $V_{OUT} \text{ RANGE (V)}$        |      |
|                                 |                                       | MIN                               | MAX | MIN                                | MAX | MIN                                | MAX  |
| 200                             | 200                                   | 1                                 | 3.4 | 1                                  | 5.5 | 1                                  | 6.2  |
| 250                             | 158                                   | 1                                 | 3.5 | 1                                  | 6.2 | 1                                  | 10.6 |
| 300                             | 133                                   | 1                                 | 3.5 | 1                                  | 6.8 | 1                                  | 10.6 |
| 350                             | 113                                   | 1                                 | 3.5 | 1                                  | 7.4 | 1                                  | 10.7 |
| 400                             | 100 or<br>(RT pin<br>open)            | 1                                 | 3.5 | 1                                  | 7.9 | 1                                  | 11.4 |
| 450                             | 88.7                                  | 1                                 | 3.5 | 1                                  | 8.4 | 1.2                                | 12.1 |
| 500                             | 78.7                                  | 1                                 | 3.5 | 1                                  | 8.9 | 1.3                                | 12.8 |
| 550                             | 71.5                                  | 1                                 | 3.4 | 1                                  | 9.3 | 1.4                                | 13.4 |
| 600                             | 66.5                                  | 1                                 | 3.4 | 1                                  | 9.5 | 1.6                                | 14.1 |
| 650                             | 60.4                                  | 1                                 | 3.4 | 1                                  | 9.4 | 1.7                                | 14.6 |
| 700                             | 56.2                                  | 1                                 | 3.3 | 1                                  | 9.3 | 1.8                                | 15.2 |
| 750                             | 52.3                                  | 1                                 | 3.3 | 1                                  | 9.2 | 2.0                                | 15.8 |
| 800                             | 49.9                                  | 1                                 | 3.3 | 1                                  | 9.1 | 2.1                                | 16.3 |
| 850                             | 46.4                                  | 1                                 | 3.2 | 1.1                                | 9.0 | 2.2                                | 16.8 |
| 900                             | 44.2                                  | 1                                 | 3.2 | 1.2                                | 9.0 | 2.3                                | 17.3 |
| 950                             | 41.2                                  | 1                                 | 3.2 | 1.2                                | 8.9 | 2.5                                | 17.8 |
| 1000                            | 39.2                                  | 1                                 | 3.1 | 1.3                                | 8.8 | 2.6                                | 18   |
| 1050                            | 37.4                                  | 1                                 | 3.1 | 1.4                                | 8.7 | 2.7                                | 18   |
| 1100                            | 35.7                                  | 1                                 | 3.1 | 1.4                                | 8.6 | 2.9                                | 18   |
| 1150                            | 34.0                                  | 1                                 | 3   | 1.5                                | 8.5 | 3                                  | 18   |
| 1200                            | 33.2                                  | 1                                 | 3   | 1.6                                | 8.5 | 3.1                                | 18   |

### 7.3.5 Synchronization (SYNC)

The LMZM33602 switching frequency can also be synchronized to an external clock from 200 kHz to 1.2 MHz. To implement the synchronization feature, couple an AC signal to the EN/SYNC pin (pin 2) with a peak-to-peak amplitude of at least 2.8 V, not to exceed 5.5 V. The minimum SYNC clock ON and OFF time must be longer than 100ns. The AC signal must be coupled through a small capacitor (1 nF) as shown in Figure 7-8. R<sub>ENT</sub> is required for this synchronization circuit, but R<sub>ENB</sub> is not required if an external UVLO adjustment is not needed.

Before the external clock is present, or when a valid clock signal is removed, the device works in RT mode and the switching frequency is set by R<sub>RT</sub> resistor. Select R<sub>RT</sub> so that it sets the frequency close to the external synchronization frequency. When the external clock is present, the SYNC mode overrides the RT mode.

The synchronization frequency must be selected based on the output voltages of the devices being synchronized. Table 7-3 shows the allowable frequencies for a given range of output voltages. For the most efficient solution, always select the lowest allowable frequency.



**Figure 7-8. AC Coupled SYNC Signal**

### 7.3.6 Input Capacitors

The LMZM33602 requires a minimum input capacitance of 9.4  $\mu$ F ( $2 \times 4.7 \mu$ F) of ceramic type. High-quality, ceramic-type X5R or X7R capacitors with sufficient voltage rating are recommended. TI recommends an additional 100  $\mu$ F of non-ceramic capacitance for applications with transient load requirements. The voltage rating of input capacitors must be greater than the maximum input voltage.

**Table 7-4. Recommended Input Capacitors**

| VENDOR    | SERIES | PART NUMBER         | CAPACITOR CHARACTERISTICS |                                       |                                  |
|-----------|--------|---------------------|---------------------------|---------------------------------------|----------------------------------|
|           |        |                     | WORKING VOLTAGE (V)       | CAPACITANCE <sup>(2)</sup> ( $\mu$ F) | ESR <sup>(1)</sup> (m $\Omega$ ) |
| Murata    | X7R    | GRM32ER71H475KA88L  | 50                        | 4.7                                   | 2                                |
| TDK       | X5R    | C3225X5R1H106K250AB | 50                        | 10                                    | 3                                |
| Murata    | X7R    | GRM32ER71H106KA12   | 50                        | 10                                    | 2                                |
| TDK       | X7R    | C3225X7R1H106M250AB | 50                        | 10                                    | 3                                |
| Panasonic | ZA     | EEHZA1H101P         | 50                        | 100                                   | 28                               |

(1) Maximum ESR @ 100 kHz, 25°C.

(2) Standard capacitance values

### 7.3.7 Output Capacitors

The LMZM33602 minimum and maximum output capacitance listed in [Table 7-1](#) and [Table 7-2](#) represents the amount of *effective* capacitance. The effects of DC bias and temperature variation must be considered when using ceramic capacitance. For ceramic capacitors, the package size, voltage rating, and dielectric material will contribute to differences between the standard rated value and the actual effective value of the capacitance.

When adding additional capacitance, above  $C_{OUT(min)}$ , the capacitance can be ceramic type, low-ESR polymer type, or a combination of the two. See [Table 7-5](#) for a preferred list of output capacitors by vendor.

**Table 7-5. Recommended Output Capacitors**

| VENDOR    | SERIES | PART NUMBER <sup>(1)</sup> | CAPACITOR CHARACTERISTICS |                                 |                         |
|-----------|--------|----------------------------|---------------------------|---------------------------------|-------------------------|
|           |        |                            | WORKING VOLTAGE (V)       | CAPACITANCE <sup>(3)</sup> (μF) | ESR <sup>(2)</sup> (mΩ) |
| Murata    | X7R    | GRM32ER71E226KE15L         | 25                        | 22                              | 2                       |
| TDK       | X5R    | C3225X5R0J476K             | 6.3                       | 47                              | 2                       |
| Murata    | X5R    | GRM32ER61C476K             | 16                        | 47                              | 3                       |
| TDK       | X5R    | C3225X5R0J107M             | 6.3                       | 100                             | 2                       |
| Murata    | X5R    | GRM32ER60J107M             | 6.3                       | 100                             | 2                       |
| Murata    | X5R    | GRM32ER61A107M             | 10                        | 100                             | 2                       |
| Kemet     | X5R    | C1210C107M4PAC7800         | 16                        | 100                             | 2                       |
| Panasonic | POSCAP | 6TPE100MI                  | 6.3                       | 100                             | 18                      |
| Panasonic | POSCAP | 6TPE150MF                  | 6.3                       | 150                             | 15                      |
| Panasonic | POSCAP | 10TPF150ML                 | 10                        | 150                             | 15                      |
| Panasonic | POSCAP | 6TPF220M9L                 | 6.3                       | 220                             | 9                       |
| Panasonic | POSCAP | 6TPE220ML                  | 6.3                       | 220                             | 12                      |
| Panasonic | POSCAP | 4TPF330ML                  | 4                         | 330                             | 12                      |
| Panasonic | POSCAP | 6TPF330M9L                 | 6.3                       | 330                             | 9                       |
| Panasonic | POSCAP | 6TPE470MAZU                | 6.3                       | 470                             | 35                      |

- (1) **Capacitor Supplier Verification , RoHS, Lead-free and Material Details** Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
- (2) Maximum ESR @ 100 kHz, 25°C.
- (3) Standard capacitance values.



### 7.3.8 Output On/Off Enable (EN)

The voltage on the EN/SYNC pin provides electrical ON/OFF control of the device. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low quiescent current state.

The EN pin cannot be open circuit or floating. The simplest way to enable the operation of the LMZM33602 is to connect the EN pin to VIN directly as shown in Figure 7-9. This allows self-start-up of the LMZM33602 when VIN is within the operation range.

If an application requires controlling the EN pin, an external logic signal can be used to drive EN/SYNC pin as shown in Figure 7-10. Applications using an open drain/collector device to interface with this pin require a pullup resistor to a voltage above the enable threshold.

Figure 7-11 and Figure 7-12 show typical turn-ON and turn-OFF waveforms using the enable control.

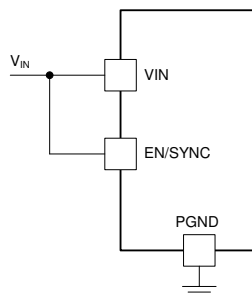


Figure 7-9. Enabling the Device

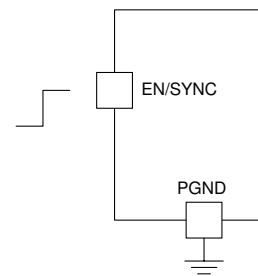


Figure 7-10. Typical Enable Control

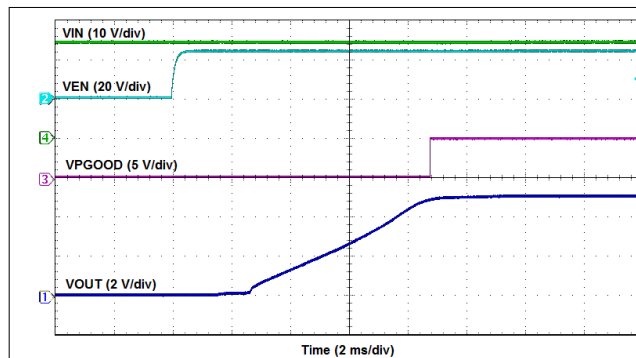


Figure 7-11. Enable Turn-ON

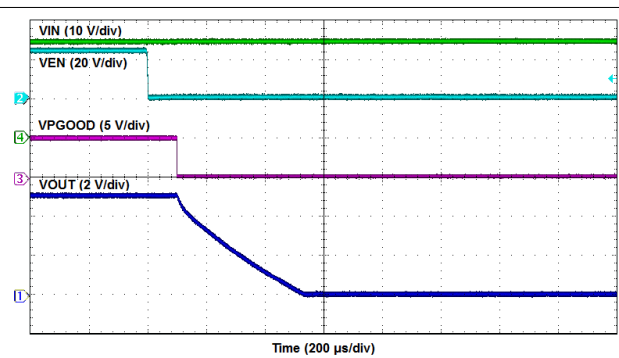


Figure 7-12. Enable Turn-OFF

### 7.3.9 Programmable Undervoltage Lockout (UVLO)

The LMZM33602 implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO rising threshold is 3.9 V (maximum) with a typical hysteresis of 300 mV.

If an application requires a higher UVLO threshold, a resistor divider can be placed on the EN/SYNC pin as shown in Figure 7-13. Table 7-6 lists recommended resistor values for  $R_{ENT}$  and  $R_{ENB}$  to adjust the ULVO voltage.

To ensure proper start-up and reduce input current surges, the UVLO threshold must be set to at least  $(V_{OUT} + 1.5 \text{ V})$  for output voltages  $\leq 5 \text{ V}$  and at least  $(1.3 \times V_{OUT})$  for output voltages  $> 5 \text{ V}$ . TI recommends to set the UVLO threshold to approximately 80% to 85% of the minimum expected input voltage.

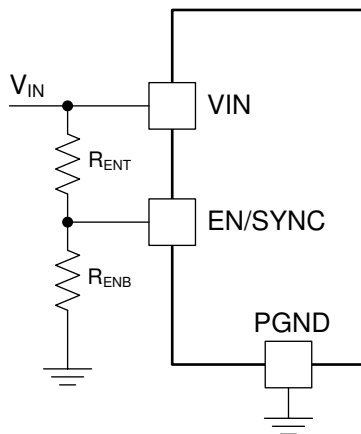


Figure 7-13. Adjustable UVLO

Table 7-6. Resistor Values for Adjusting UVLO

| VIN UVLO (V)            | 6.5  | 10   | 15   | 20   | 25   | 30   |
|-------------------------|------|------|------|------|------|------|
| $R_{ENT}$ (k $\Omega$ ) | 100  | 100  | 100  | 100  | 100  | 100  |
| $R_{ENB}$ (k $\Omega$ ) | 35.7 | 20.5 | 12.7 | 9.31 | 7.32 | 6.04 |

### 7.3.10 Power Good (PGOOD)

The LMZM33602 has a built-in power-good signal (PGOOD) which indicates whether the output voltage is within its regulation range. The PGOOD pin is an open-drain output that requires a pullup resistor to a nominal voltage source of 12 V or less. The maximum recommended PGOOD sink current is 1 mA. A typical pullup resistor value is between 10 k $\Omega$  and 100 k $\Omega$ .

Once the output voltage rises above 94% of the set voltage, the PGOOD pin rises to the pullup voltage level. The PGOOD pin is pulled low when the output voltage drops lower than 92.5% or rises higher than 107% of the nominal set voltage. See Figure 7-14 for typical power-good thresholds.

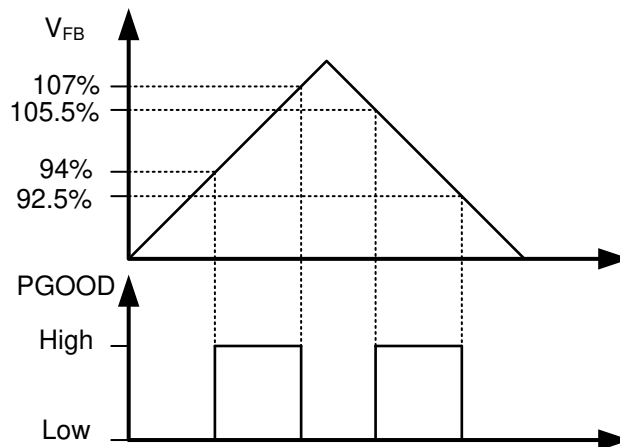
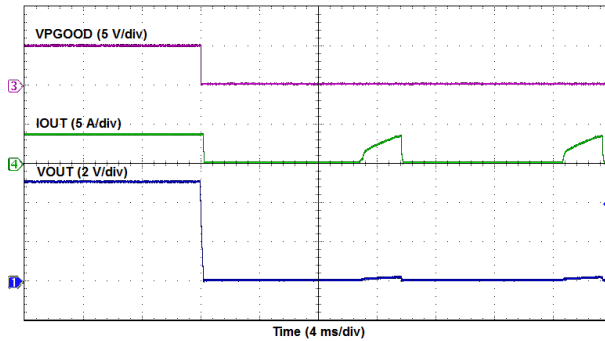


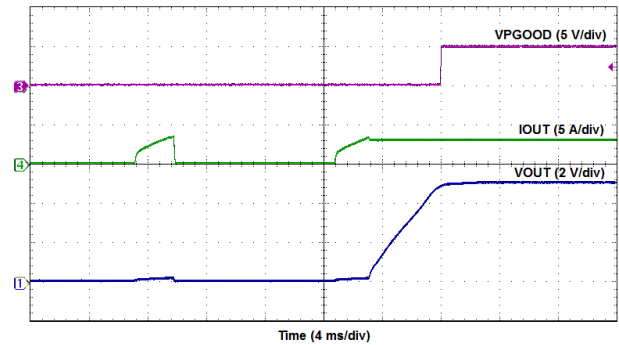
Figure 7-14. Power Good Flag

### 7.3.11 Overcurrent Protection (OCP)

The LMZM33602 is protected from overcurrent conditions. Hiccup mode is activated if a fault condition persists to prevent overheating. In hiccup mode, the regulator is shut down and kept off for 10 ms typical before the LMZM33602 tries to start again. If overcurrent or short-circuit fault condition still exist, hiccup repeats until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions, and prevents overheating and potential damage to the device. Once the fault is removed, the module automatically recovers and returns to normal operation as shown in Figure 7-16.



**Figure 7-15. Overcurrent Limiting**



**Figure 7-16. Removal of Overcurrent**

### 7.3.12 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 170°C typically. The device reinitiates the power up sequence when the junction temperature drops below 155°C typically.

## 7.4 Device Functional Modes

### 7.4.1 Active Mode

The LMZM33602 is in active mode when VIN is above the UVLO threshold and the EN/SYNC pin voltage is above the EN high threshold. The simplest way to enable the LMZM33602 is to connect the EN/SYNC pin to VIN. This allows self start-up of the LMZM33602 when the input voltage is in the operation range: 4 V to 36 V. In active mode, the LMZM33602 is in continuous conduction mode (CCM) with fixed switching frequency.

### 7.4.2 Shutdown Mode

The EN/SYNC pin provides electrical ON and OFF control for the LMZM33602. When the EN/SYNC pin voltage is below the EN low threshold, the device is in shutdown mode. In shutdown mode the standby current is 2  $\mu$ A typical. The LMZM33602 also employs input UVLO protection. If VIN is below the UVLO level, the output of the regulator is turned off.

## 8 Application and Implementation

### Note

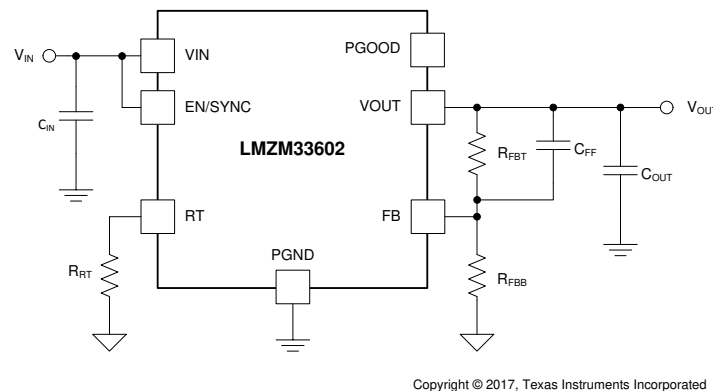
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The LMZM33602 is a synchronous, step-down, DC-DC power module. It is used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 2 A. The LMZM33602 can be configured in an inverting buck-boost (IBB) topology with the output voltage inverted or negative with respect to ground. For more details, see TI Application Report [Inverting Application for the LMZM33602/03](#). The following design procedure can be used to select components for the LMZM33602. Alternately, the WEBENCH® software may be used to generate complete designs. When generating a design, the WEBENCH® software utilizes an iterative design procedure and accesses comprehensive databases of components. See [www.ti.com](http://www.ti.com) for more details.

### 8.2 Typical Application

The LMZM33602 only requires a few external components to convert from a wide input voltage supply range to a wide range of output voltages. [Figure 8-1](#) shows a basic LMZM33602 schematic with only the minimum required components.



Copyright © 2017, Texas Instruments Incorporated

**Figure 8-1. LMZM33602 Typical Schematic**

#### 8.2.1 Design Requirements

For this design example, use the parameters listed in [Table 8-1](#) as the input parameters and follow the design procedures in [Section 8.2.2](#).

**Table 8-1. Design Example Parameters**

| DESIGN PARAMETER         | VALUE        |
|--------------------------|--------------|
| Input voltage $V_{IN}$   | 24 V typical |
| Output voltage $V_{OUT}$ | 5 V          |
| Output current rating    | 2 A          |
| Operating frequency      | 450 kHz      |

## 8.2.2 Detailed Design Procedure

### 8.2.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the LMZM33602 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ( $V_{IN}$ ), output voltage ( $V_{OUT}$ ), and output current ( $I_{OUT}$ ) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at [www.ti.com/WEBENCH](http://www.ti.com/WEBENCH).

### 8.2.2.2 Output Voltage Setpoint

The output voltage of the LMZM33602 device is externally adjustable using a resistor divider. The recommended value of  $R_{FBB}$  is 10.0 k $\Omega$ . The value for  $R_{FBT}$  can be selected from [Table 7-6](#) or calculated using [Equation 4](#):

$$R_{FBT} = 10 \times (V_{OUT} - 1)(k\Omega) \quad (4)$$

For the desired output voltage of 5.0 V, the formula yields a value of 40 k $\Omega$ . Choose the closest available value of 40.2 k $\Omega$  for  $R_{FBT}$ .

### 8.2.2.3 Feedforward Capacitor ( $C_{FF}$ )

TI recommends placing an external feedforward capacitor,  $C_{FF}$  in parallel with the top resistor divider,  $R_{FBT}$  for optimum transient performance. The value for  $C_{FF}$  can be calculated using [Equation 2](#) or selected from [Table 7-1](#). The recommended  $C_{FF}$  value for 5-V application is 100 pF.

### 8.2.2.4 Setting the Switching Frequency

The recommended switching frequency for a 5-V application is 450 kHz. To set the switching frequency to 450 kHz, a 88.7-k $\Omega$   $R_{RT}$  resistor is required.

### 8.2.2.5 Input Capacitors

The LMZM33602 requires a minimum input capacitance of 10  $\mu$ F (or  $2 \times 4.7 \mu$ F) ceramic type. High-quality ceramic type X5R or X7R capacitors with sufficient voltage rating are recommended. An additional 100  $\mu$ F of non-ceramic capacitance is recommended for applications with transient load requirements. The voltage rating of input capacitors must be greater than the maximum input voltage.

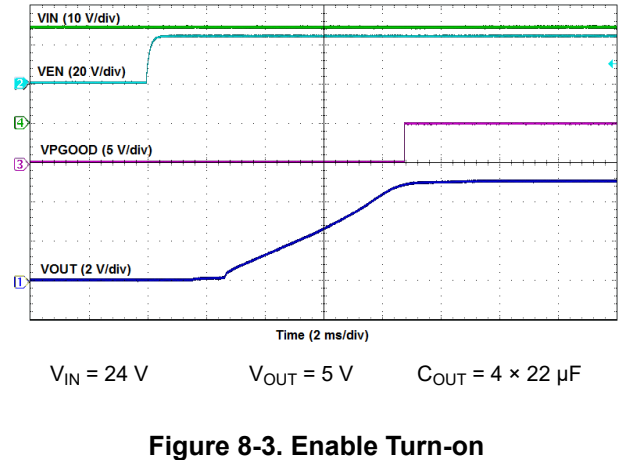
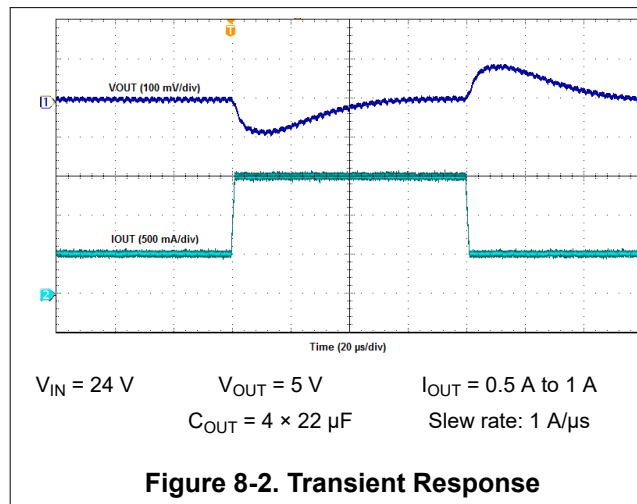
For this design, a 10- $\mu$ F, 50-V, ceramic capacitor was selected.

### 8.2.2.6 Output Capacitor Selection

The LMZM33602 requires a minimum amount of output capacitance for proper operation. The minimum amount of required output varies depending on the output voltage. See [Table 7-1](#) for the required output capacitance.

For this design example, four 22- $\mu$ F, 25-V ceramic capacitors are used.

### 8.2.2.7 Application Curves



### Power Supply Recommendations

The LMZM33602 is designed to operate from an input voltage supply range between 4 V and 36 V. This input supply must be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LMZM33602 supply voltage that can cause a false UVLO fault triggering and system reset.

If the input supply is located more than a few inches from the LMZM33602 additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The typical amount of bulk capacitance is a 100-μF electrolytic capacitor.

## Layout

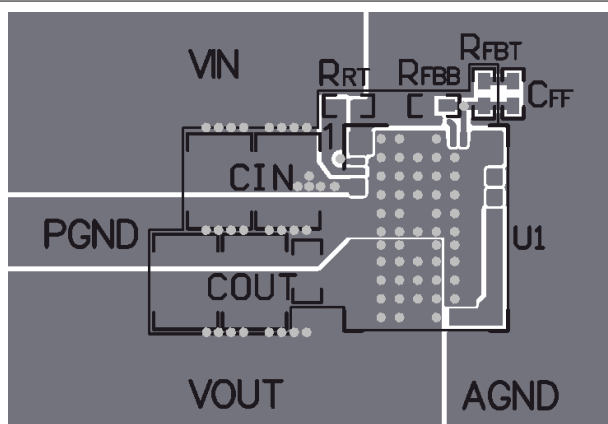
The performance of any switching power supply depends as much upon the layout of the PCB as the component selection. The following guidelines will help users design a PCB with the best power conversion performance, optimal thermal performance, and minimized generation of unwanted EMI.

### 9.1 Layout Guidelines

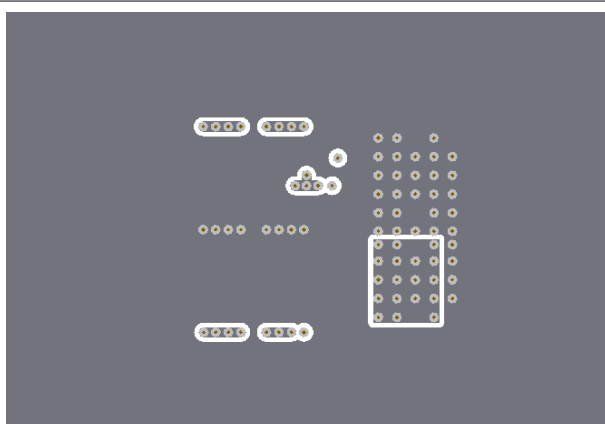
To achieve optimal electrical and thermal performance, an optimized PCB layout is required. [Figure 9-1](#) through [Figure 9-4](#) show a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- **Connect PGND pins 14 and 15 directly to pin 18 using thick copper traces.**
- Connect the SW pins together using a small copper island under the device for thermal relief.
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Keep AGND and PGND separate from one another.
- Place  $R_{FBT}$ ,  $R_{FBB}$ ,  $R_{RT}$ , and  $C_{FF}$  as close as possible to their respective pins.
- Use multiple vias to connect the power planes to internal layers.

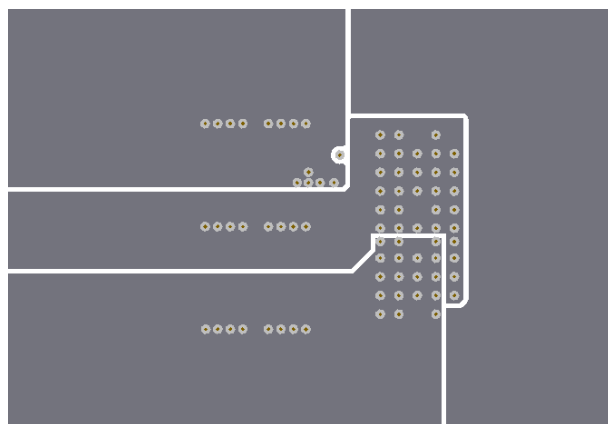
### 9.2 Layout Examples



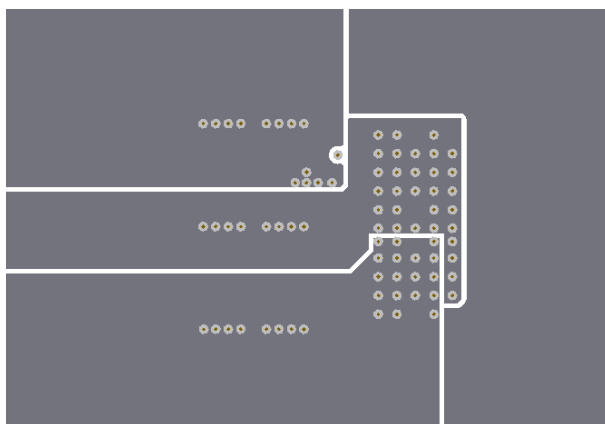
**Figure 9-1. Typical Top-Layer Layout**



**Figure 9-2. Typical Layer-2 Layout**



**Figure 9-3. Typical Layer 3 Layout**



**Figure 9-4. Typical Bottom-Layer Layout**

### 9.3 Theta JA versus PCB Area

The amount of PCB copper effects the thermal performance of the device. Figure 9-5 shows the effects of copper area on the junction-to-ambient thermal resistance ( $R_{\theta JA}$ ) of the LMZM33602. The junction-to-ambient thermal resistance is plotted for a 2-layer PCB and a 4-layer PCB with PCB area from 16 cm<sup>2</sup> to 49 cm<sup>2</sup>.

To determine the required copper area for an application:

1. Determine the maximum power dissipation of the device in the application by referencing the power dissipation graphs in [Section 6.7](#) to [Section 6.9](#).
2. Calculate the maximum  $\theta_{JA}$  using [Equation 5](#) and the maximum ambient temperature of the application.

$$\theta_{JA} = \frac{(125^{\circ}\text{C} - T_{A(\text{max})})}{P_{D(\text{max})}} \quad (^{\circ}\text{C}/\text{W}) \quad (5)$$

3. Reference [Figure 9-5](#) to determine the minimum required PCB area for the application conditions.

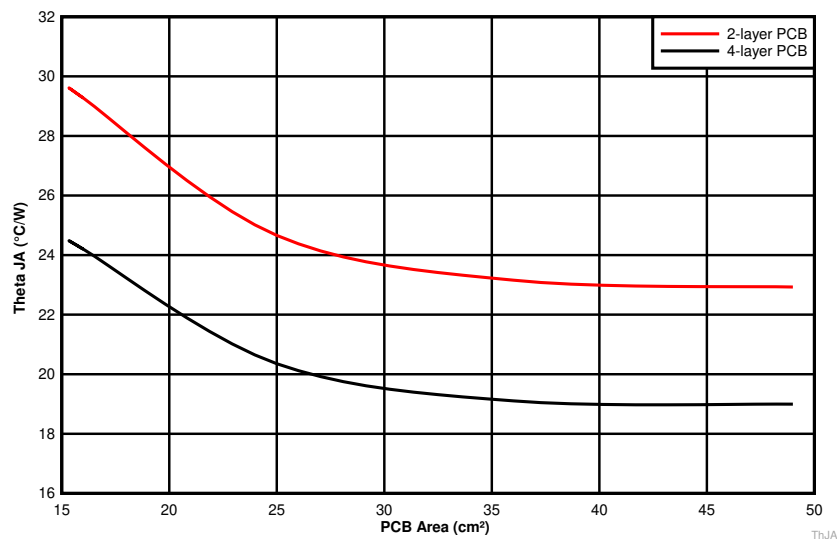


Figure 9-5.  $\theta_{JA}$  vs PCB Area

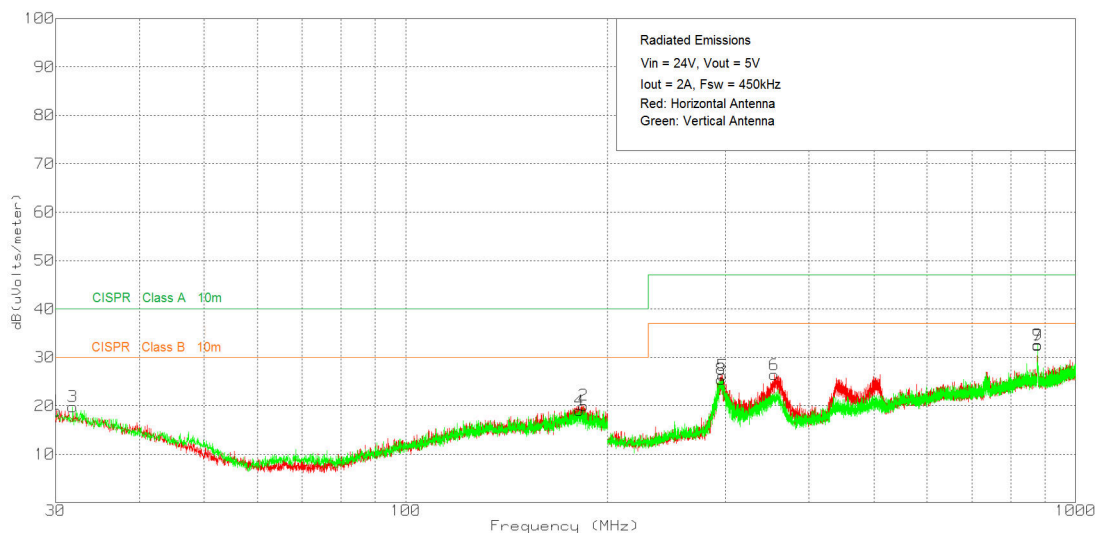
### 9.4 EMI

The LMZM33602 is compliant with EN55011 Class B radiated emissions. [Figure 9-6](#), [Figure 9-7](#), and [Figure 9-8](#) show typical examples of radiated emissions plots for the LMZM33602. The graphs include the plots of the antenna in the horizontal and vertical positions.

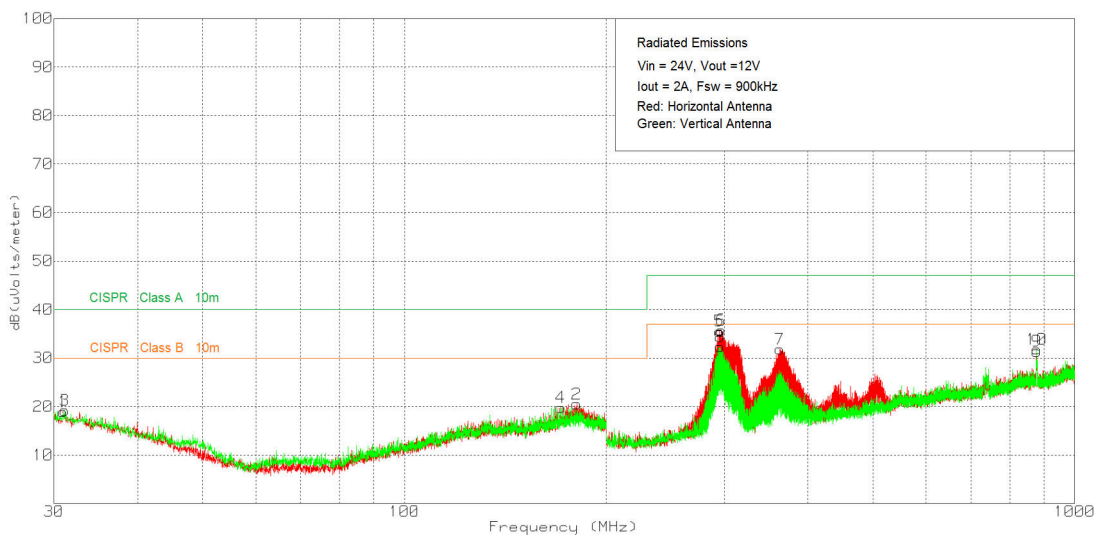
#### 9.4.1 EMI Plots

EMI plots were measured using the standard LMZM33602EVM with no input filter.

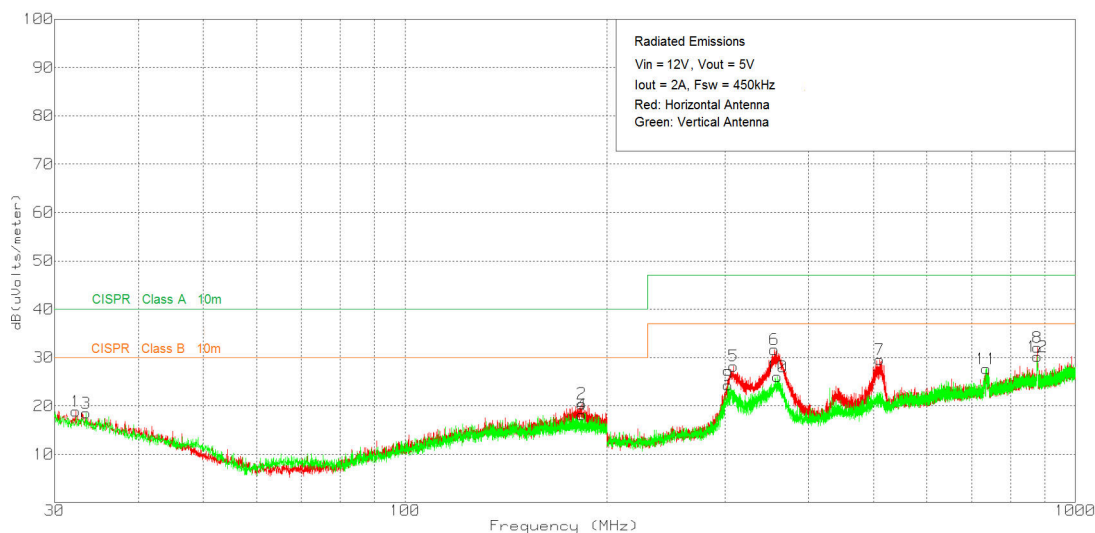




**Figure 9-6. Radiated Emissions 24-V Input, 5-V Output, 2-A Load (EN55011 Class B)**



**Figure 9-7. Radiated Emissions 24-V Input, 12-V Output, 2-A Load (EN55011 Class B)**



**Figure 9-8. Radiated Emissions 12-V Input, 5-V Output, 2-A Load (EN55011 Class B)**

## 9.5 Package Specifications

| LMZM33602                   |                                                                      | VALUE | UNIT  |
|-----------------------------|----------------------------------------------------------------------|-------|-------|
| Weight                      |                                                                      | 0.74  | grams |
| Flammability                | Meets UL 94 V-O                                                      |       |       |
| MTBF Calculated Reliability | Per Bellcore TR-332, 50% stress, $T_A = 40^{\circ}C$ , ground benign | 98.0  | MHrs  |

## 9 Device and Documentation Support

### 9.1 Device Support

#### 9.1.1 Development Support

##### 9.1.1.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the LMZM33602 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ( $V_{IN}$ ), output voltage ( $V_{OUT}$ ), and output current ( $I_{OUT}$ ) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

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Get more information about WEBENCH tools at [www.ti.com/WEBENCH](http://www.ti.com/WEBENCH).

### 9.2 Documentation Support

#### 9.2.1 Related Documentation

For related documentation see the following:

TI Application Report [Inverting Application for the LMZM33602/03](#)

### 9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 9.5 Trademarks

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WEBENCH® is a registered trademark of Texas Instruments.

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### 9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

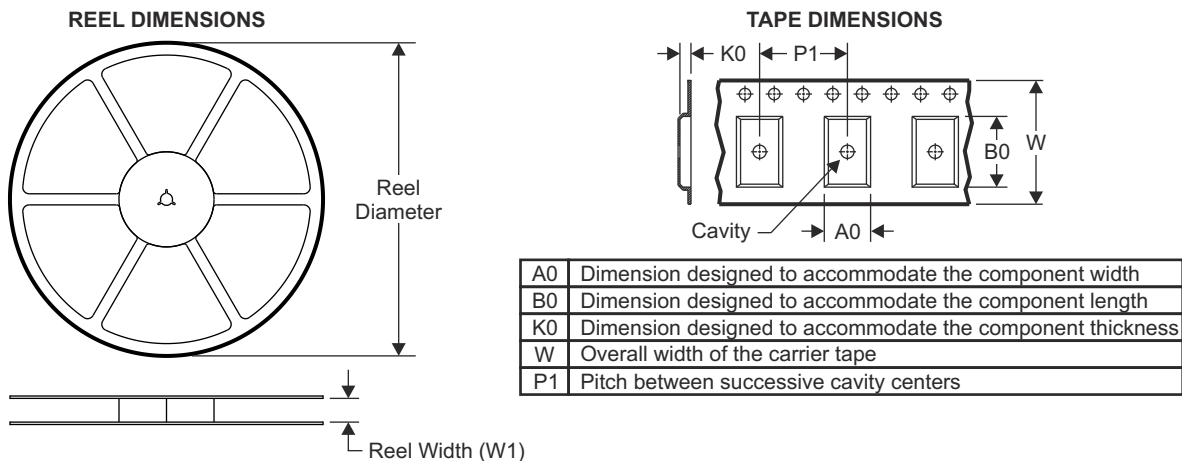
### 9.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

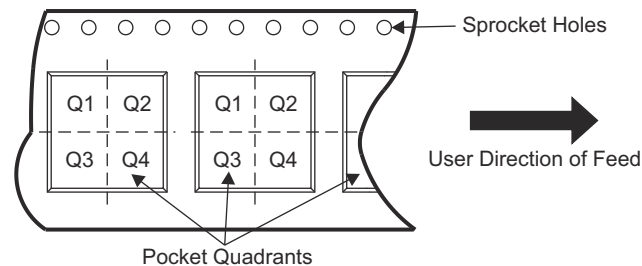
## Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 10.1 Tape and Reel Information

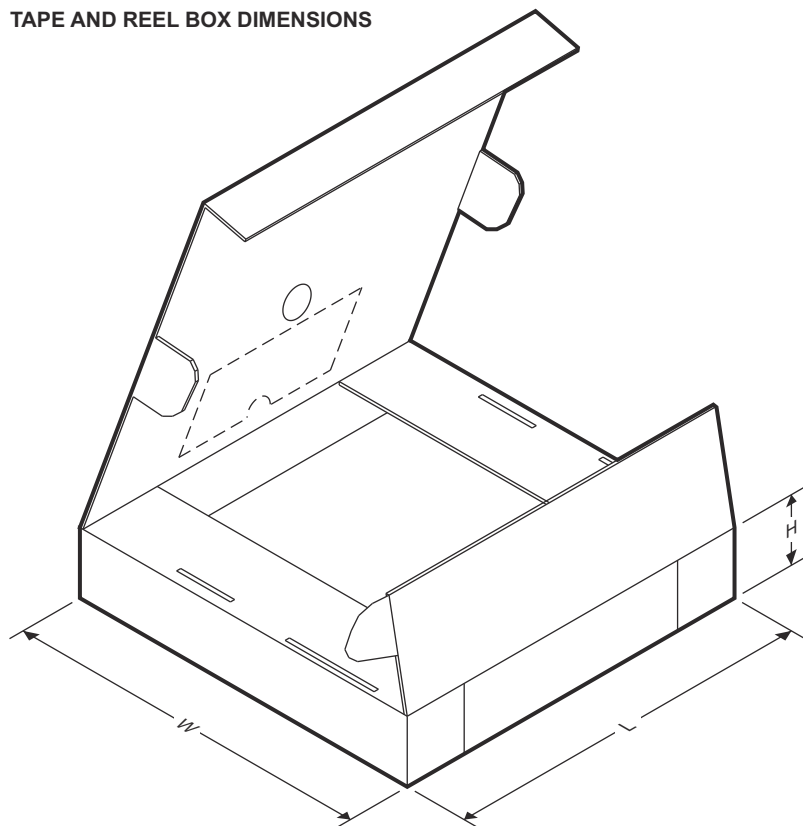


#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



| Device        | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMZM33602RLRR | B3QFN        | RLR             | 18   | 500 | 330.0              | 24.4               | 7.35    | 9.35    | 4.35    | 12.0    | 24.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**



| Device        | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|-----|-------------|------------|-------------|
| LMZM33602RLRR | B3QFN        | RLR             | 18   | 500 | 383.0       | 353.0      | 58.0        |

## PACKAGING INFORMATION

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">LMZM33602RLRR</a> | Active        | Production           | B3QFN (RLR)   18 | 500   LARGE T&R       | Yes         | NIPDAU                               | Level-3-250C-168 HR               | -40 to 105   | LMZM33602           |
| LMZM33602RLRR.A               | Active        | Production           | B3QFN (RLR)   18 | 500   LARGE T&R       | Yes         | NIPDAU                               | Level-3-250C-168 HR               | -40 to 105   | LMZM33602           |
| LMZM33602RLRR.B               | Active        | Production           | B3QFN (RLR)   18 | 500   LARGE T&R       | -           | Call TI                              | Call TI                           | -40 to 105   |                     |
| LMZM33602RLRRG4               | Active        | Production           | B3QFN (RLR)   18 | 500   LARGE T&R       | Yes         | NIPDAU                               | Level-3-250C-168 HR               | -40 to 105   | LMZM33602           |
| LMZM33602RLRRG4.A             | Active        | Production           | B3QFN (RLR)   18 | 500   LARGE T&R       | Yes         | NIPDAU                               | Level-3-250C-168 HR               | -40 to 105   | LMZM33602           |
| LMZM33602RLRRG4.B             | Active        | Production           | B3QFN (RLR)   18 | 500   LARGE T&R       | Yes         | NIPDAU                               | Level-3-250C-168 HR               | -40 to 105   | LMZM33602           |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

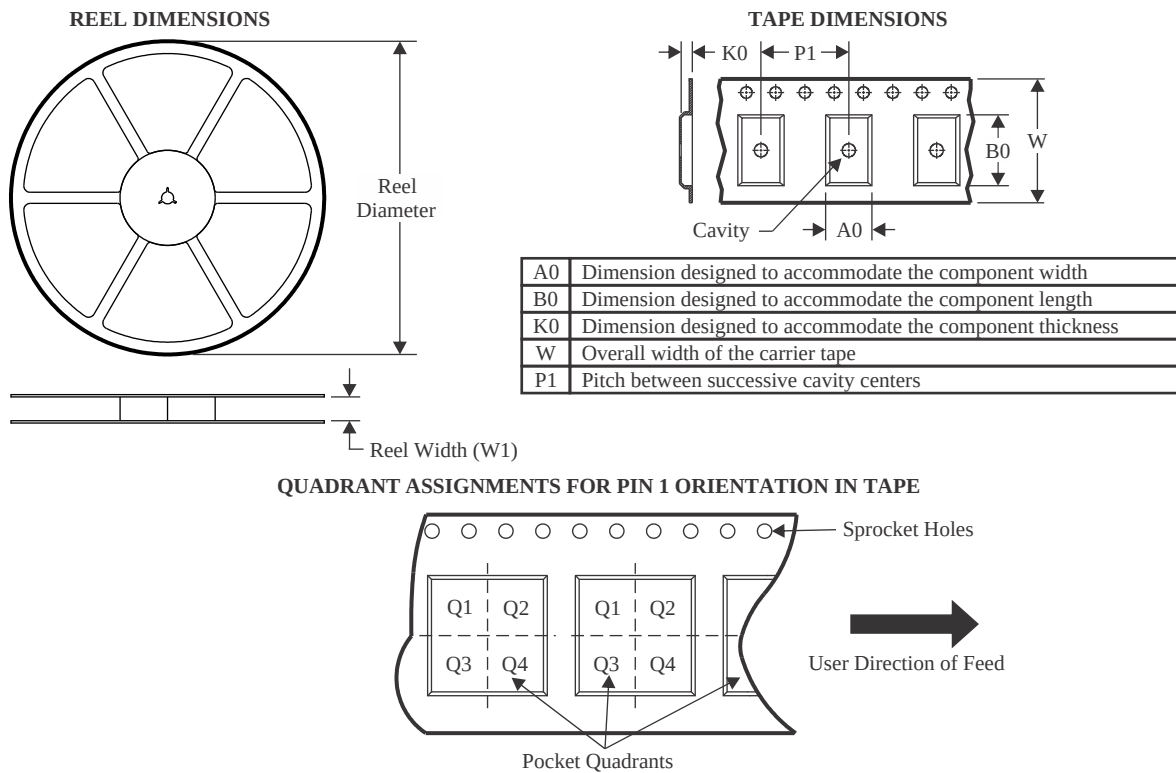
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION

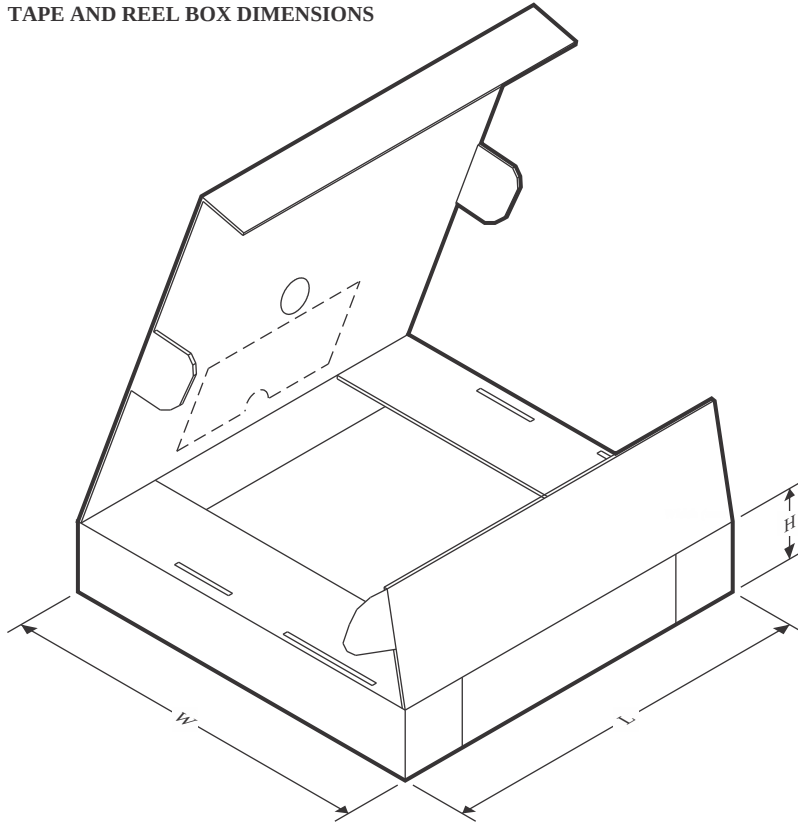


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMZM33602RLRR   | B3QFN        | RLR             | 18   | 500 | 330.0              | 24.4               | 7.35    | 9.35    | 4.35    | 12.0    | 24.0   | Q1            |
| LMZM33602RLRRG4 | B3QFN        | RLR             | 18   | 500 | 330.0              | 24.4               | 7.35    | 9.35    | 4.35    | 12.0    | 24.0   | Q1            |



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|-----|-------------|------------|-------------|
| LMZM33602RLRR   | B3QFN        | RLR             | 18   | 500 | 383.0       | 353.0      | 58.0        |
| LMZM33602RLRRG4 | B3QFN        | RLR             | 18   | 500 | 383.0       | 353.0      | 58.0        |

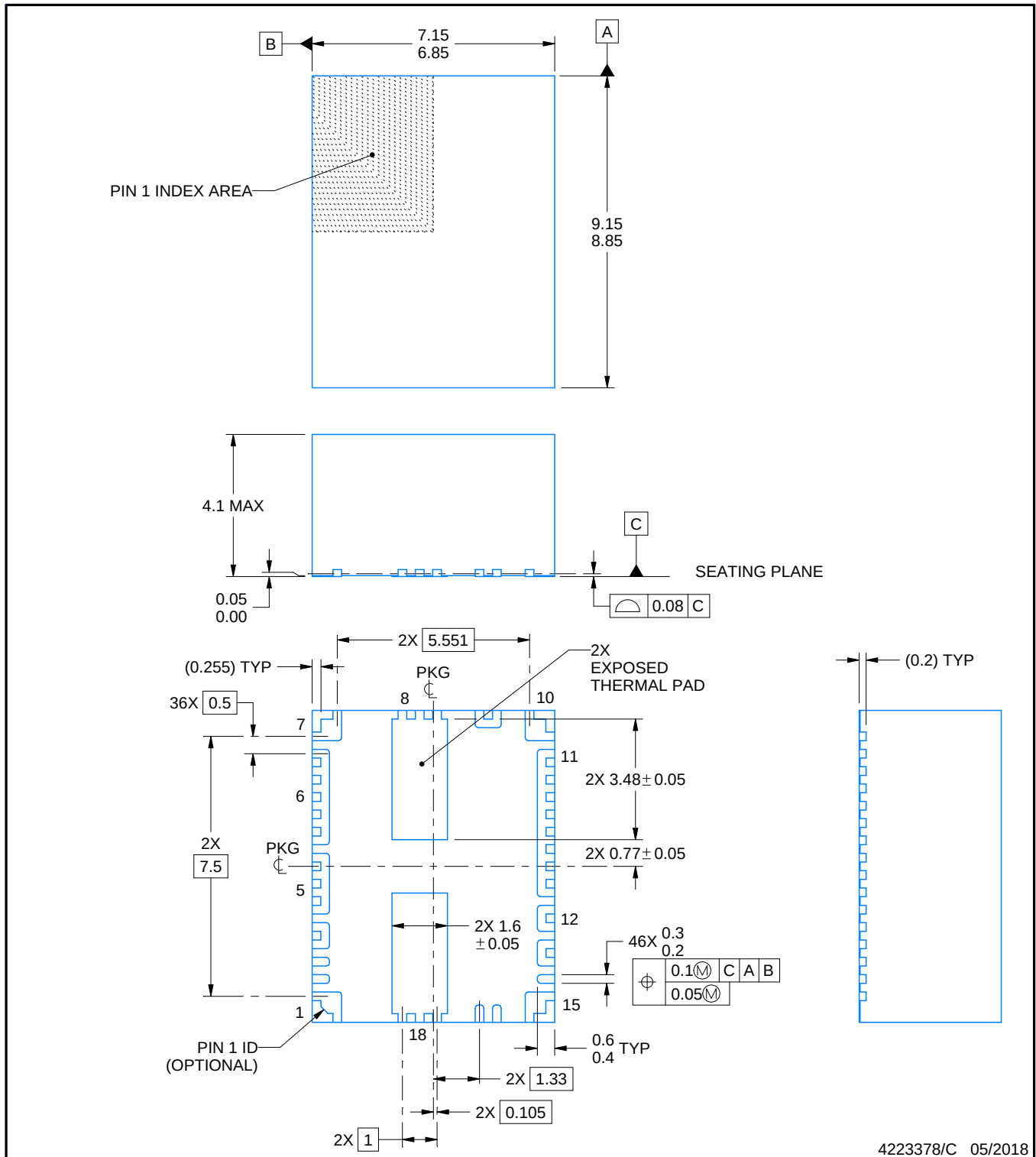
RLR0018A



## PACKAGE OUTLINE

B3QFN - 4.1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4223378/C 05/2018

### NOTES:

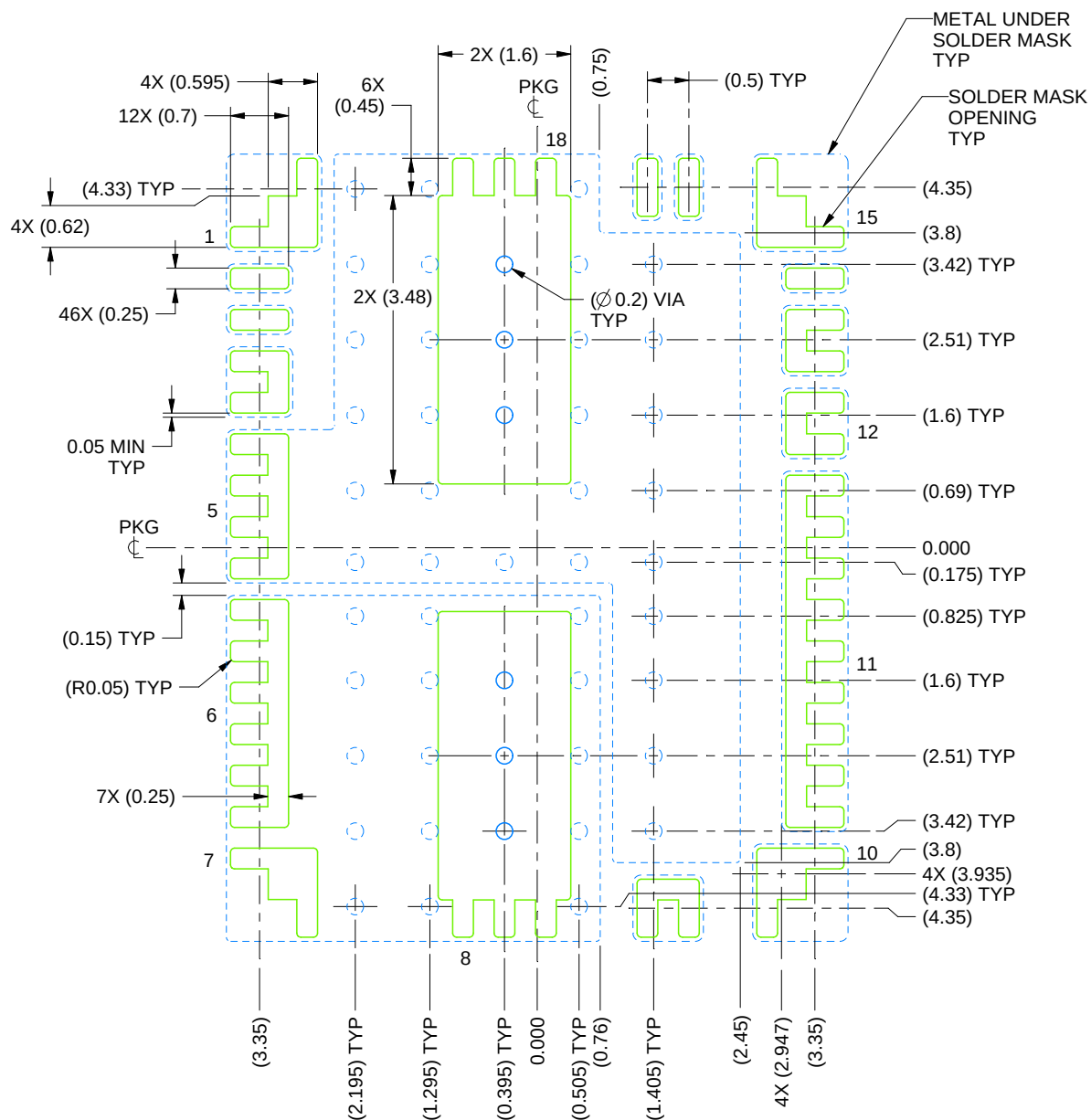
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

RLR0018A

B3QFN - 4.1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SOLDER MASK DEFINED  
SCALE: 12X

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NOTES: (continued)

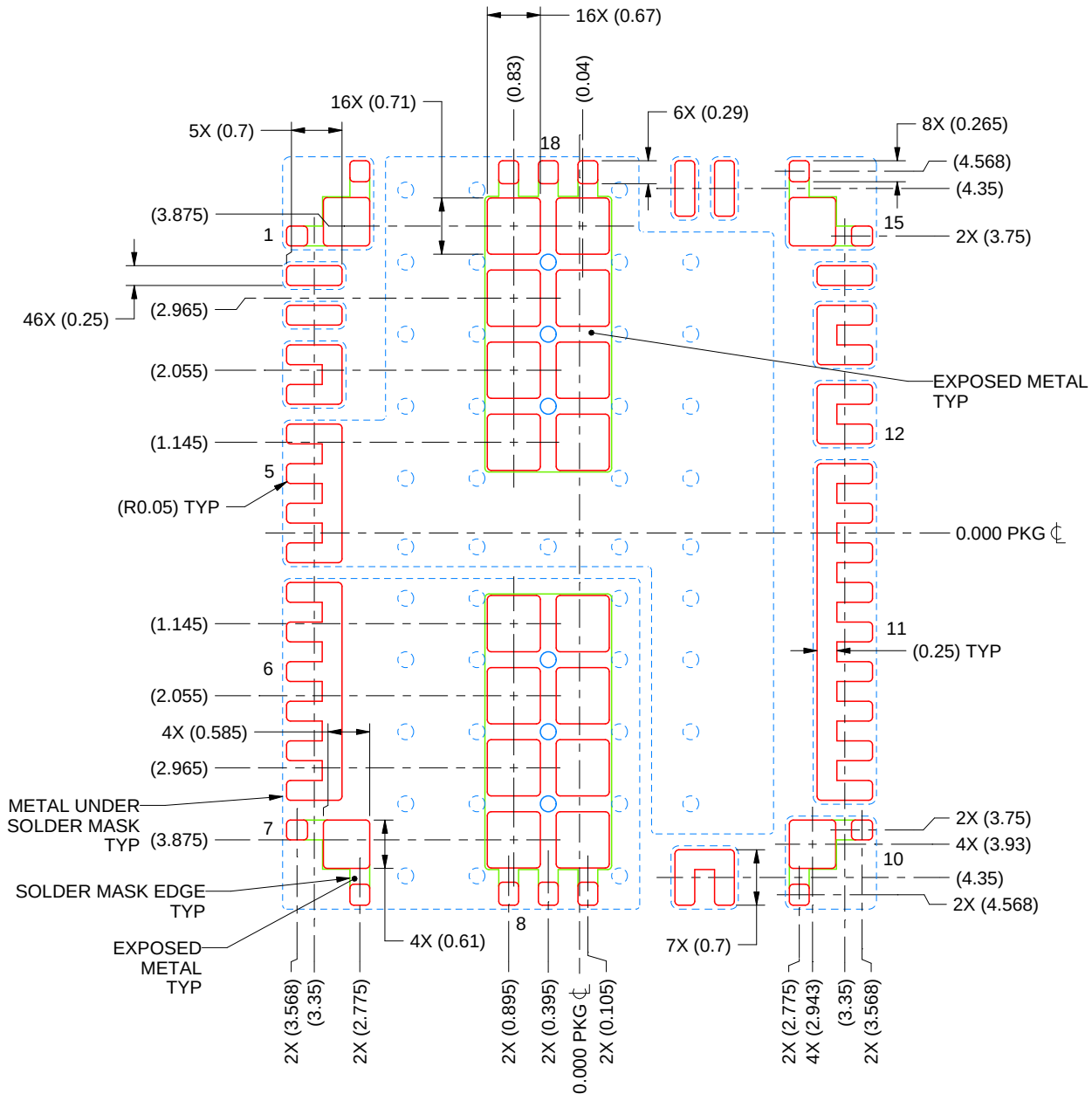
- This package designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RLR0018A

B3QFN - 4.1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 8 & 18:  
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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