LMV722-Q1 10-MHz Low-Noise, Low-Voltage Operational Amplifier

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Ambient Operating Temperature: –40°C to +125°C
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Power-Supply Voltage Range: 2.2 V to 5.5 V
- Low Supply Current: 905 µA/Amplifier at 2.2 V
- High Unity-Gain Bandwidth: 10 MHz
- Rail-to-Rail Output Swing
  - 600-Ω Load: 120 mV From Either Rail at 2.2 V
  - 2-kΩ Load: 50 mV From Either Rail at 2.2 V
- Input Common-Mode Voltage Range Includes Ground
- Input Voltage Noise: 10.5 nV/$\sqrt{Hz}$ at f = 1 kHz

2 Applications

- Infotainment
- Engine Control Unit
- Automotive Lighting
- Audio Signal Path

3 Description

The LMV722-Q1 device is a low-noise, low-voltage operational amplifier (op amp) that can be designed into a wide range of applications. The LMV722-Q1 has a unity-gain bandwidth of 10 MHz, slew rate of 5.25 V/µs, and good voltage and current noise performance.

The LMV722-Q1 is designed to provide optimal performance in low-voltage and low-noise systems such audio signal path or motor control applications. The device provides rail-to-rail output swing into heavy loads. The input common-mode voltage range includes ground and the maximum input offset voltage is 3.5 mV (over recommended temperature range) for the device. The capacitive load capability is also good at low supply voltages. The operating range is from 2.2 V to 5.5 V.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMV722-Q1	VSSOP	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

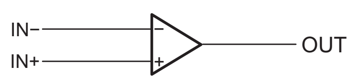


Table of Contents

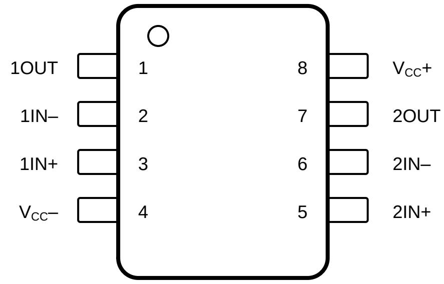
1 Features 1
2 Applications 1
3 Description 1
4 Revision History 2
5 Pin Configuration and Functions 3
6 Specifications 4
6.1 Absolute Maximum Ratings 4
6.2 ESD Ratings 4
6.3 Recommended Operating Conditions 4
6.4 Thermal Information 4
6.5 Electrical Characteristics V_{CC+} = 2.2 V 5
6.6 Electrical Characteristics V_{CC+} = 5 V 6
6.7 Typical Characteristics 7
7 Detailed Description 12
7.1 Overview 12
7.2 Functional Block Diagram 12
7.3 Feature Description 12
7.4 Device Functional Modes 12
8 Application and Implementation 13
8.1 Application Information 13
8.2 Typical Application 13
9 Power Supply Recommendations 15
9.1 Input and ESD Protection 15
10 Layout 16
10.1 Layout Guidelines 16
10.2 Layout Example 17
11 Device and Documentation Support 18
11.1 Documentation Support 18
11.2 Receiving Notification of Documentation Updates 18
11.3 Community Resources 18
11.4 Trademarks 18
11.5 Electrostatic Discharge Caution 18
11.6 Glossary 18
12 Mechanical, Packaging, and Orderable Information 18

4 Revision History

Changes from Original (June 2017) to Revision A	Page
• Changed body size from 4.90 mm to 3.00 mm	1
• CDM value changed from 100 V to 1000 V	4
• Updated *Layout Example* section	17

5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	1OUT	O	Output of amplifier 1
2	1IN–	I	Inverting input of amplifier 1
3	1IN+	I	Non-inverting input of amplifier 1
4	V_{CC}–	I	Negative power supply
5	2IN+	I	Non-inverting input of amplifier 2
6	2IN–	I	Inverting input of amplifier 2
7	2OUT	O	Output of amplifier 2
8	V_{CC}+	I	Positive power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
$V_{CC+} – V_{CC–}$	Supply voltage[2]	0	6	V
V_{ID}	Differential input voltage[3]		±Supply voltage	V
T_J	Operating virtual-junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
(3) Differential voltages are at IN+ with respect to IN−.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	2000	V
		Charged-device model (CDM), per AEC Q100-011	1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC+} – V_{CC–}$	Supply voltage	2.2	5.5	V
T_J	Operating ambient temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		LMV722-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	176.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	97.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	96.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics V_{CC+} = 2.2 V

V_{CC+} = 2.2 V, V_{CC-} = GND, V_{ICR} = V_{CC+}/2, V_O = V_{CC+}/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		T_J = 25°C		0.02	3	mV
			T_J = –40°C to +125°C			3.5	
TCV_{IO}	Input offset voltage average drift		T_J = 25°C		0.6		µV/°C
I_{IB}	Input bias current		T_J = 25°C		260		nA
I_{IO}	Input offset current		T_J = 25°C		25		nA
CMMR	Common-mode rejection ratio	V_{ICR} = 0 V to 1.3 V	T_J = 25°C	70	88		dB
			T_J = –40°C to +125°C	64			
PSRR	Power-supply rejection ratio	V_{CC+} = 2.2 V to 5 V V_O = 0, V_{ICR} = 0	T_J = 25°C	80	90		dB
			T_J = –40°C to +125°C	70			
V_{ICR}	Input common-mode voltage	CMRR ≥ 50 dB	T_J = 25°C		–0.3		V
			T_J = 25°C		1.3		
A_{VD}	Large-signal voltage gain	R_L = 600 Ω, V_O = 0.75 V to 2 V	T_J = 25°C	75	81		dB
			T_J = –40°C to +125°C	70			
		R_L = 2 kΩ, V_O = 0.5 V to 2.1 V	T_J = 25°C	75	84		
			T_J = –40°C to +125°C	70			
V_O	Output swing	R_L = 600 Ω to V_{CC+}/2	T_J = 25°C	2.090	2.125		V
			T_J = –40°C to +125°C	2.065			
			T_J = 25°C		0.071	0.120	
			T_J = –40°C to +125°C			0.145	
		R_L = 2 kΩ to V_{CC+}/2	T_J = 25°C	2.150	2.177		
			T_J = –40°C to +125°C	2.125			
			T_J = 25°C		0.056	0.080	
			T_J = –40°C to +125°C			0.105	
I_O	Output current	Sourcing, V_O = 0 V $V_{IN(diff)}$ = ±0.5 V	T_J = 25°C	10	14.9		mA
			T_J = –40°C to +125°C	5			
		Sinking, V_O = 2.2 V $V_{IN(diff)}$ = ±0.5 V	T_J = 25°C	10	17.6		
			T_J = –40°C to +125°C	5			
I_{CC}	Supply current		T_J = 25°C		1.81	2.4	mA
			T_J = –40°C to +125°C			2.6	
SR	Slew rate (1)		T_J = 25°C		4.9		V/µs
GBW	Gain bandwidth product		T_J = 25°C		10		MHz
Φ_m	Phase margin		T_J = 25°C		67.4		°
G_m	Gain margin		T_J = 25°C		–9.8		dB
V_n	Input-referred voltage noise	f = 1 kHz	T_J = 25°C		11		nV/√Hz
I_n	Input-referred current noise	f = 1 kHz	T_J = 25°C		0.3		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, AV = 1, R_L = 600 Ω, V_O = 500 mV_{pp}	T_J = 25°C		0.004%		

(1) Connected as voltage follower with 1-V step input. Number specified is the slower of the positive and negative slew rate.

6.6 Electrical Characteristics V_{CC+} = 5 V

V_{CC+} = 5 V, V_{CC-} = GND, V_{ICR} = V_{CC+}/2, V_O = V_{CC+}/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		T_J = 25°C		–0.08	3	mV
			T_J = –40°C to +125°C			3.5	
TCV_{IO}	Input offset voltage average drift		T_J = 25°C		0.6		µV/°C
I_{IB}	Input bias current		T_J = 25°C		260		nA
I_{IO}	Input offset current		T_J = 25°C		25		nA
CMMR	Common-mode rejection ratio	V_{ICR} = 0 V to 4.1 V	T_J = 25°C	80	89		dB
		V_{ICR} = 0 V to 4.1 V	T_J = –40°C to +125°C	75			
PSRR	Power-supply rejection ratio	V_{CC+} = 2.2 V to 5 V, V_O = 0, V_{ICR} = 0	T_J = 25°C	70	90		dB
		V_{CC+} = 2.2 V to 5 V, V_O = 0, V_{ICR} = 0	T_J = –40°C to +125°C	64			
V_{ICR}	Input common-mode voltage	CMRR ≥ 50 dB	T_J = 25°C		–0.3		V
			T_J = 25°C		4.1		
A_{VD}	Large-signal voltage gain	R_L = 600 Ω, V_O = 0.75 V to 4.8 V	T_J = 25°C	80	87		dB
			T_J = –40°C to +125°C	70			
		R_L = 2 kΩ, V_O = 0.7 V to 4.9 V	T_J = 25°C	80	94		
			T_J = –40°C to +125°C	70			
V_O	Output swing	R_L = 600 Ω to V_{CC+}/2	T_J = 25°C	4.84	4.882		V
			T_J = –40°C to +125°C	4.815			
			T_J = 25°C		0.134	0.19	
			T_J = –40°C to +125°C			0.215	
		R_L = 2 kΩ to V_{CC+}/2	T_J = 25°C	4.93	4.952		
			T_J = –40°C to +125°C	4.905			
			T_J = 25°C		0.076	0.11	
			T_J = –40°C to +125°C			0.135	
I_O	Output current	Sourcing, V_O = 0 V, $V_{IN(diff)}$ = ±0.5 V	T_J = 25°C	20	52.6		mA
			T_J = –40°C to +125°C	12			
		Sinking, V_O = 2.2 V, $V_{IN(diff)}$ = ±0.5 V	T_J = 25°C	15	23.7		
			T_J = –40°C to +125°C	8.5			
I_{CC}	Supply current		T_J = 25°C		2.01	2.4	mA
			T_J = –40°C to +125°C			2.8	
SR	Slew rate (1)		T_J = 25°C		5.25		V/µs
GBW	Gain bandwidth product		T_J = 25°C		10		MHz
Φ_m	Phase margin		T_J = 25°C		72		°
G_m	Gain margin		T_J = 25°C		–11		dB
V_n	Input-referred voltage noise	f = 1 kHz	T_J = 25°C		10.5		nV/√Hz
I_n	Input-referred current noise	f = 1 kHz	T_J = 25°C		0.2		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, AV = 1, R_L = 600 Ω, V_O = 500 mV_{pp}	T_J = 25°C		0.001%		

(1) Connected as voltage follower with 1-V step input. Number specified is the slower of the positive and negative slew rate.

6.7 Typical Characteristics

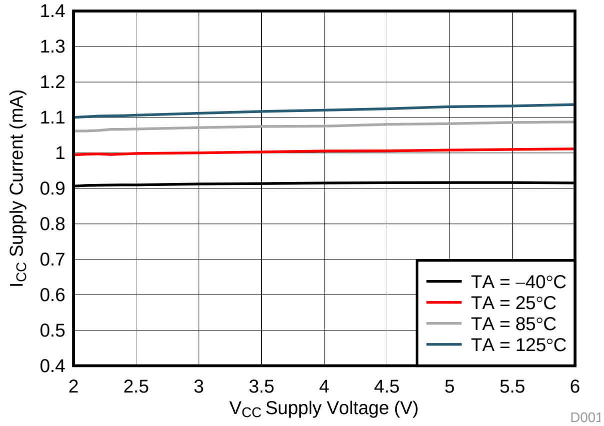


Figure 1. Supply Current vs Supply Voltage

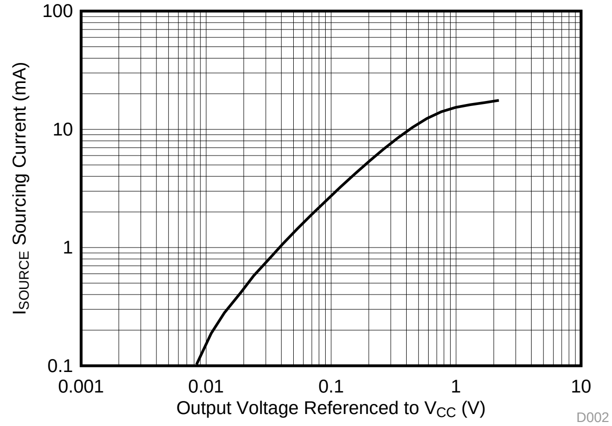


Figure 2. Sourcing Current vs Output Voltage

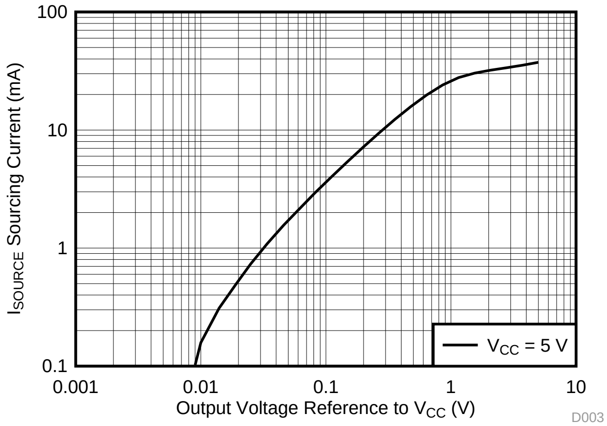
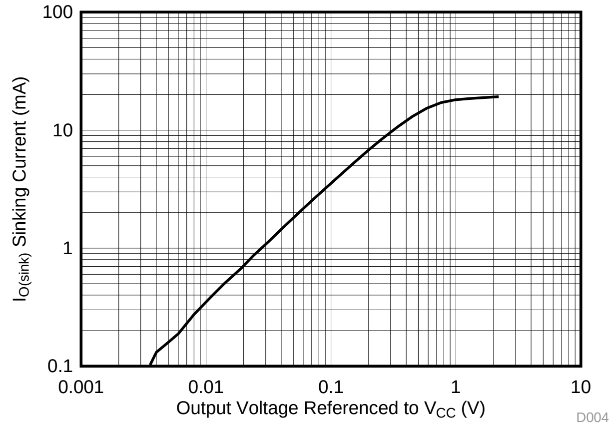


Figure 3. Sourcing Current vs Output Voltage



V_{CC} = 2.2 V

Figure 4. Sinking Current vs Output Voltage

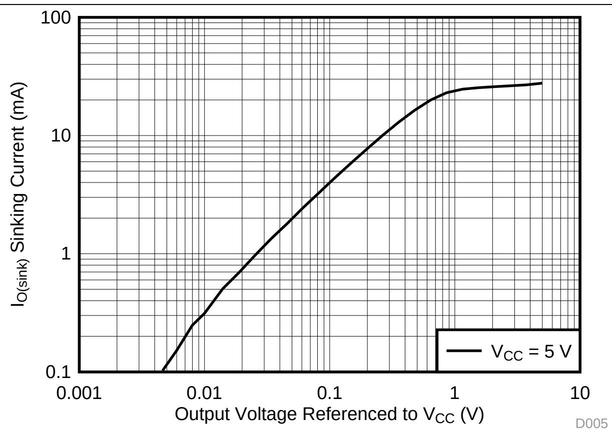


Figure 5. Sinking Current vs Output Voltage

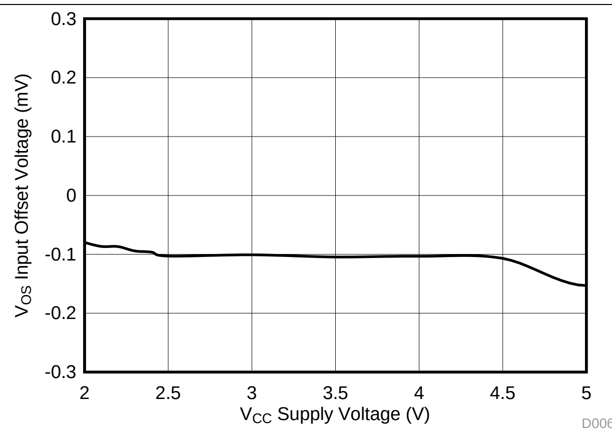


Figure 6. V_{IO} vs Supply Voltage

Typical Characteristics (continued)

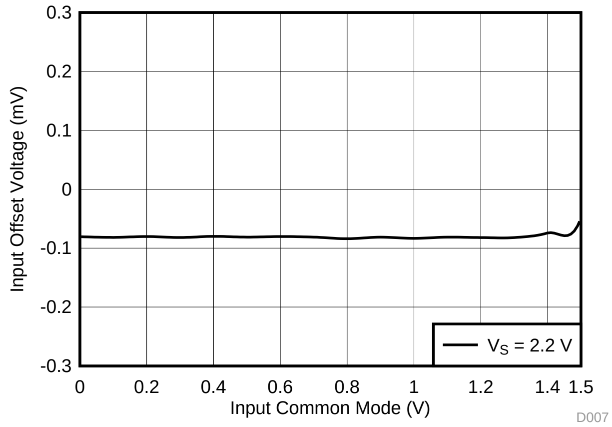


Figure 7. Input Offset Voltage vs Input Common-Mode Voltage

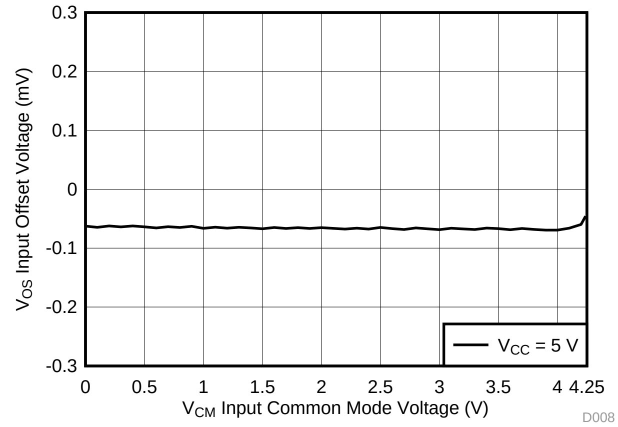


Figure 8. Input Offset Voltage vs Input Common-Mode Voltage

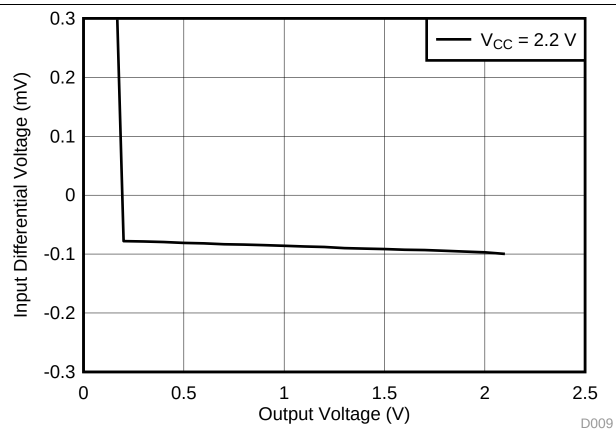


Figure 9. Input Voltage vs Output Voltage

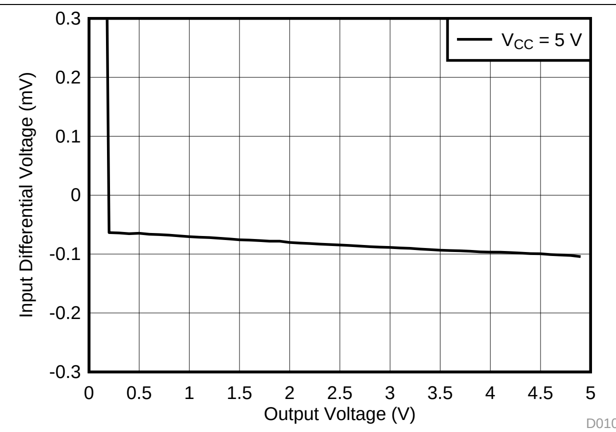


Figure 10. Input Voltage vs Output Voltage

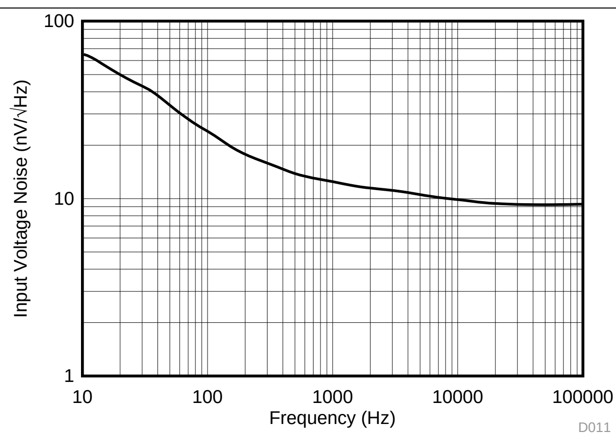


Figure 11. Input Voltage Noise vs Frequency

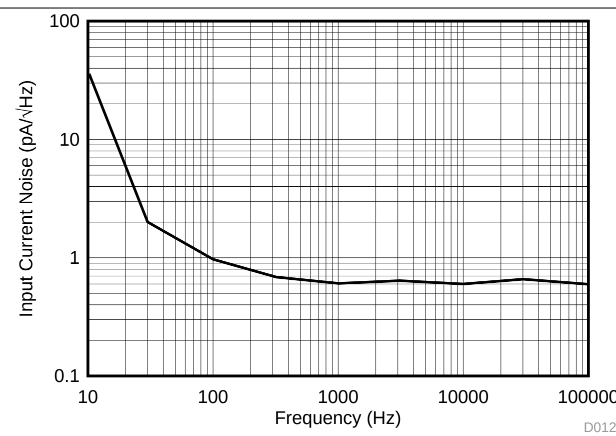


Figure 12. Input Current Noise vs Frequency

Typical Characteristics (continued)

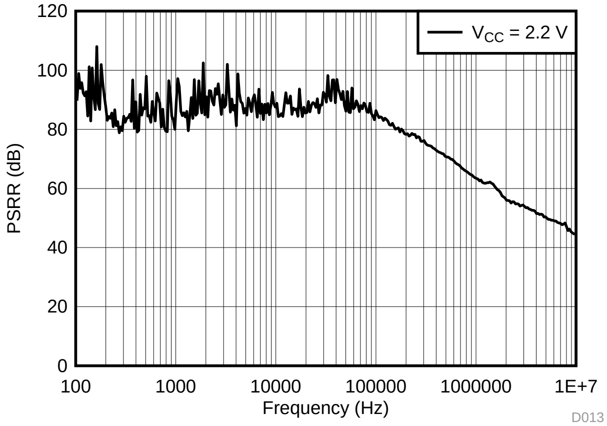
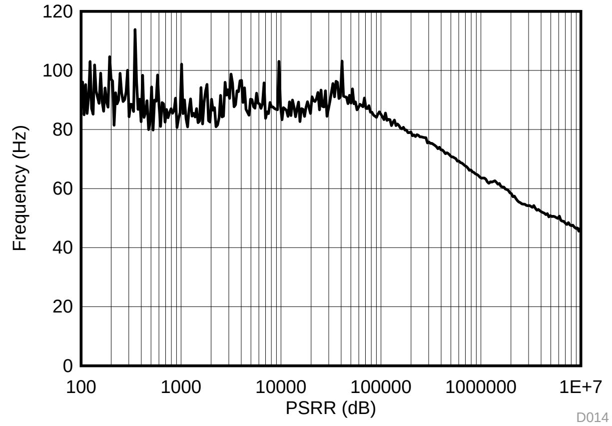
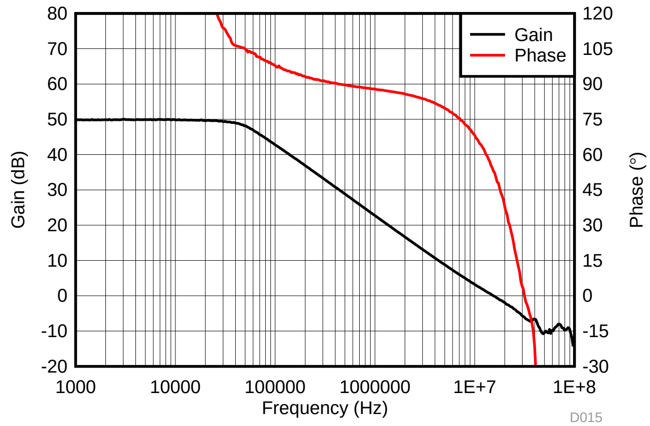


Figure 13. Psrr vs Frequency



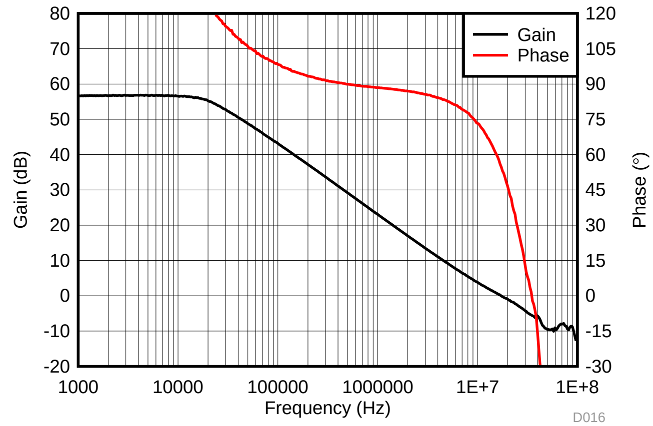
V_{CC} = 5 V

Figure 14. Psrr vs Frequency



V_{CC} = 2.2 V

Figure 15. Gain And Phase vs Frequency



V_{CC} = 5 V

Figure 16. Gain And Phase vs Frequency

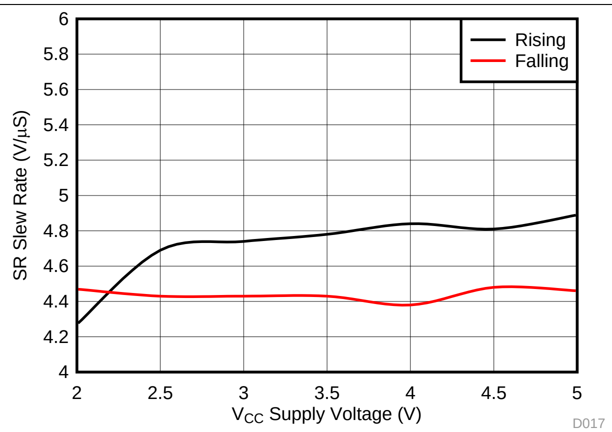
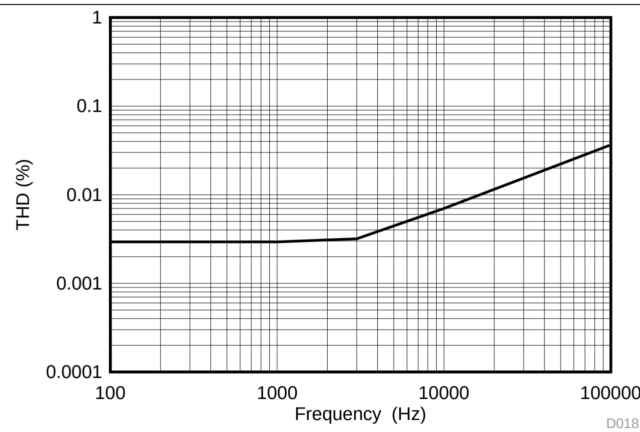


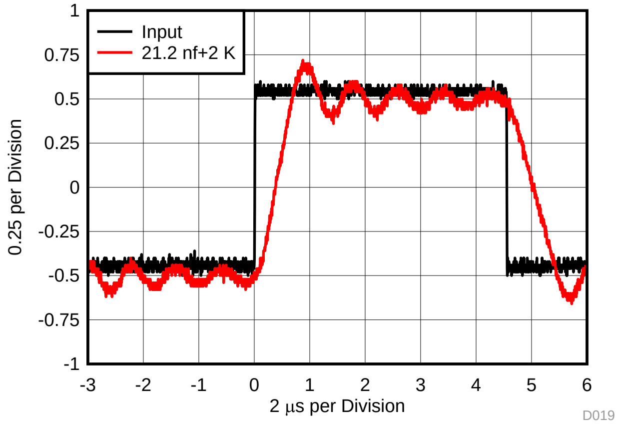
Figure 17. Slew Rate vs Supply Voltage



V_{CC} = 2.2 V

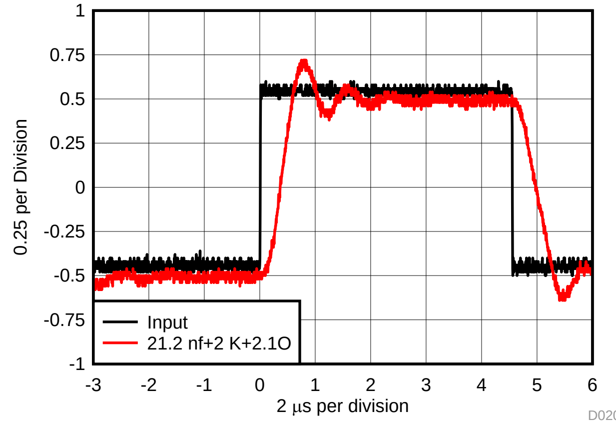
Figure 18. Thd vs Frequency

Typical Characteristics (continued)



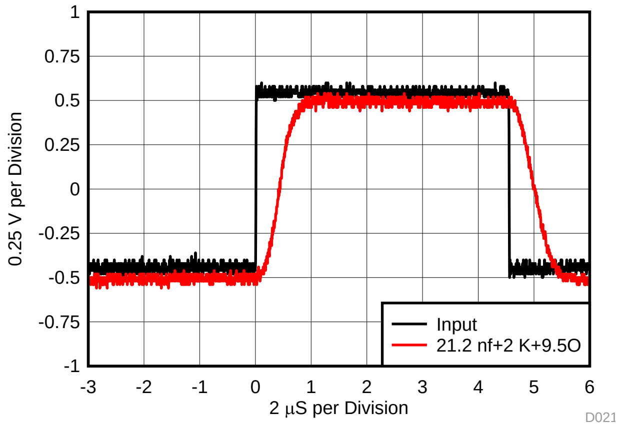
V_{CC} = 5 V, R_L = 2 kΩ, C_L = 21.2 nF, R_O = 0 Ω

Figure 19. Pulse Response



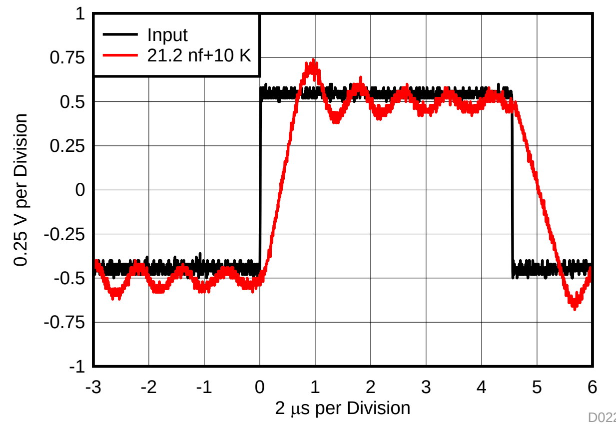
V_{CC} = 5 V, R_L = 2 kΩ, C_L = 21.2 nF, R_O = 2.1 Ω

Figure 20. Pulse Response



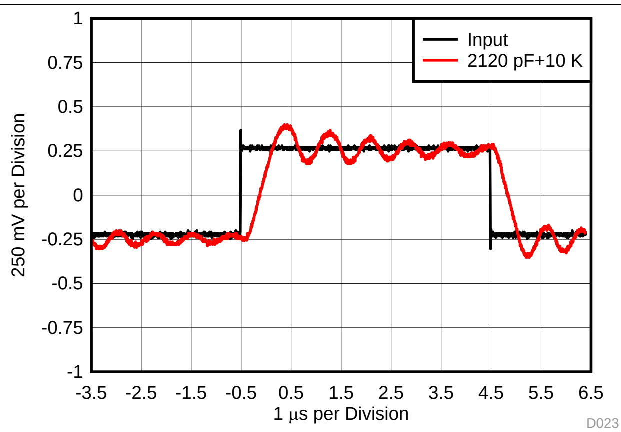
V_{CC} = 5 V, R_L = 2 kΩ, C_L = 21.2 nF, R_O = 9.5 Ω

Figure 21. Pulse Response



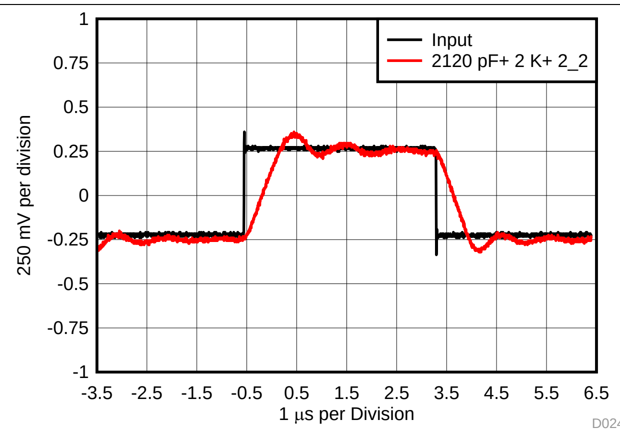
V_{CC} = 5 V, R_L = 10 kΩ, C_L = 21.2 nF, R_O = 0 Ω

Figure 22. Pulse Response



V_{CC} = 2.2 V, R_L = 10 kΩ, C_L = 2.12 nF, R_O = 0 Ω

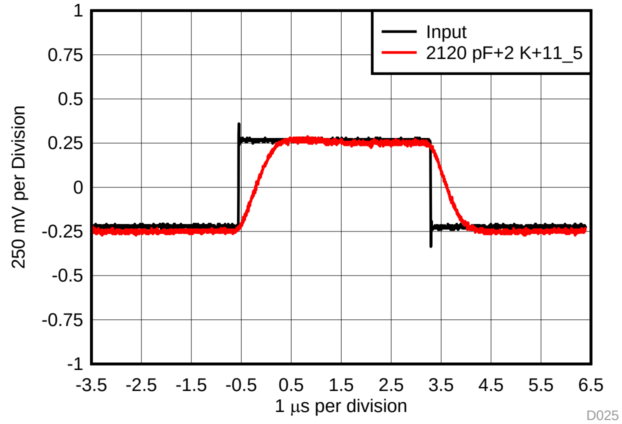
Figure 23. Pulse Response



V_{CC} = 2.2 V, R_L = 10 kΩ, C_L = 2.12 nF, R_O = 2.2 Ω

Figure 24. Pulse Response

Typical Characteristics (continued)



V_{CC} = 2.2 V, R_L = 10 kΩ, C_L = 2.12 nF, R_O = 11.5 Ω

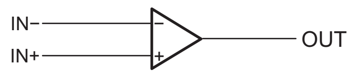
Figure 25. Pulse Response

7 Detailed Description

7.1 Overview

The LMV722-Q1 is a low-power, low-noise, rail-to-rail output op amp. This device is AEC-Q100 qualified for automotive applications. The LMV722-Q1 operates from a single 2.2 V to 5.5 V supply, is unity-gain stable, and is suitable for a wide range of general-purpose applications. The input common-mode voltage range includes ground. Rail-to-rail input and output swing significantly increases dynamic range in low-supply applications and makes applications suitable for driving sampling analog-to-digital converters (ADCs). The small footprints of the LMV722-Q1 package saves space on printed-circuit boards and enables good signal integrity and noise performance during the design of smaller electronic products, such as automotive head units.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Low Noise

The LMV722-Q1 device is a general-purpose op amp that provides low noise of 10.5 nV/√Hz and a wide bandwidth of 10 MHz. The low noise and wide bandwidth make the LMV722-Q1 device attractive for a variety of precision applications that require a good balance between cost and performance.

7.3.2 Rail-to-Rail Output

Rail-to-rail output swing provides maximum possible dynamic range at the output. This is particularly important when operating on low-supply voltages.

7.3.3 Input Includes Ground

This feature allows direct sensing near GND in a single-supply operation.

7.3.4 Signal Integrity

Signals pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, such as the 8-pin VSSOP (DGK), the LMV722-Q1 can be placed closer to the signal source; reducing noise pickup and increasing signal integrity.

7.4 Device Functional Modes

The only mode available for the LMV722-Q1 device is *on*.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMV722-Q1 features 10-MHz bandwidth and 5.25-V/µs slew rate providing good AC performance at very-low-power consumption. DC applications are well served with a very-low input noise voltage of 10.5 nV / $\sqrt{Hz}$ at 1 kHz, low input bias current, and a typical input offset voltage of 0.02 mV.

8.2 Typical Application

Figure 26 shows the LMV722-Q1 configured in a low-side current sensing application.

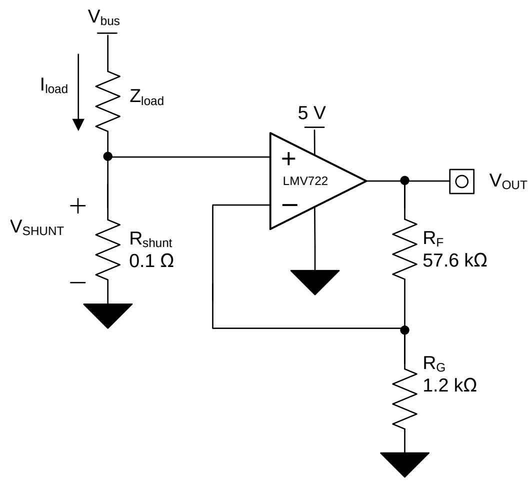


Figure 26. LMV722-Q1 in a Low-Side, Current-Sensing Application

8.2.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.9 V
- Maximum shunt voltage: 100 mV

Typical Application (continued)

8.2.2 Detailed Design Procedure

The transfer function of the circuit in Figure 26 is given in Equation 1

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using Equation 2.

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100mV}{1A} = 100m\Omega \quad (2)$$

Using Equation 2, R_{SHUNT} is calculated to be 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the LMV722-Q1 to produce an output voltage of roughly 0 V to 4.9 V. The gain needed by the LMV722-Q1 to produce the necessary output voltage is calculated using Equation 3:

$$Gain = \frac{(V_{OUT\_MAX} - V_{OUT\_MIN})}{(V_{IN\_MAX} - V_{IN\_MIN})} \quad (3)$$

Using Equation 3, the required gain is calculated to be 49 V/V, which is set with resistors R_F and R_G. Equation 4 is used to size the resistors, R_F and R_G, to set the gain of the LMV722-Q1 to 49 V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Choosing R_F as 57.6 kΩ and R_G as 1.2 kΩ provides a combination that equals roughly 49 V/V. Figure 27 shows the measured transfer function of the circuit shown in Figure 26.

8.2.3 Application Curve

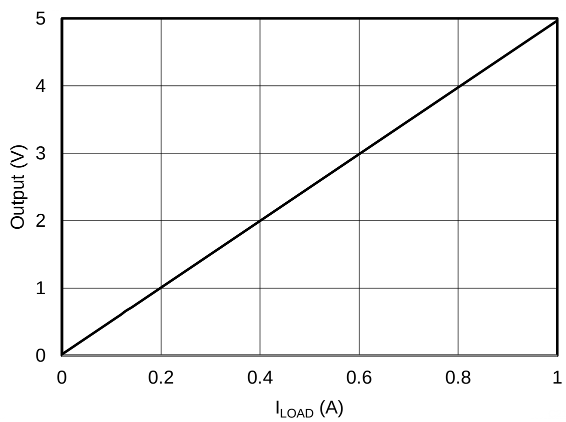


Figure 27. Low-Side, Current-Sense, Transfer Function

9 Power Supply Recommendations

The LMV722-Q1 series is specified for operation from 2.2 V to 5.5 V (±1.1 V to ±2.75 V); many specifications apply from –40°C to +125°C. The section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 6 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the section.

9.1 Input and ESD Protection

The LMV722-Q1 incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10-mA, as stated in the *Layout Guidelines* table. Figure 28 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

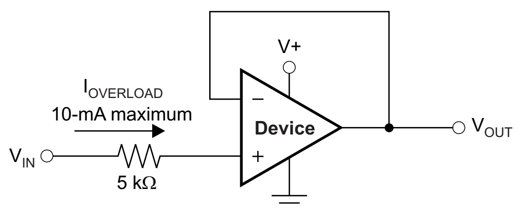


Figure 28. Input Current Protection

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information refer to, see *Circuit Board Layout Techniques*.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 30, keeping RF and RG close to the inverting input minimizes parasitic capacitance on the inverting input.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

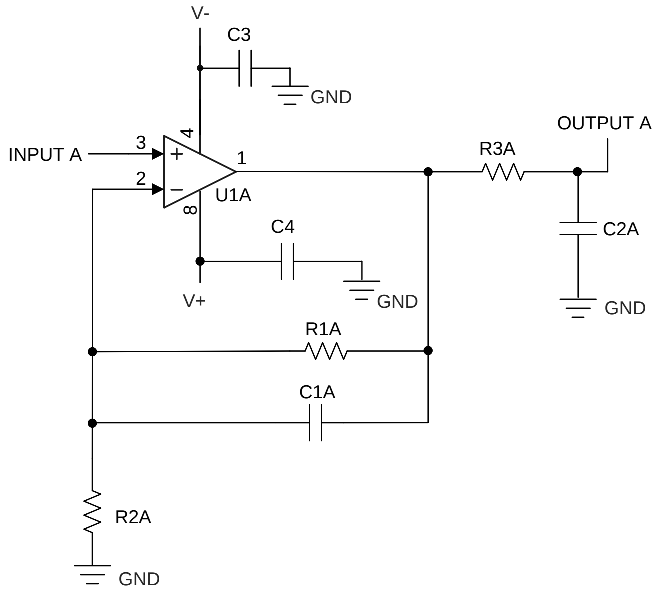


Figure 29. Schematic Representation for Figure 30

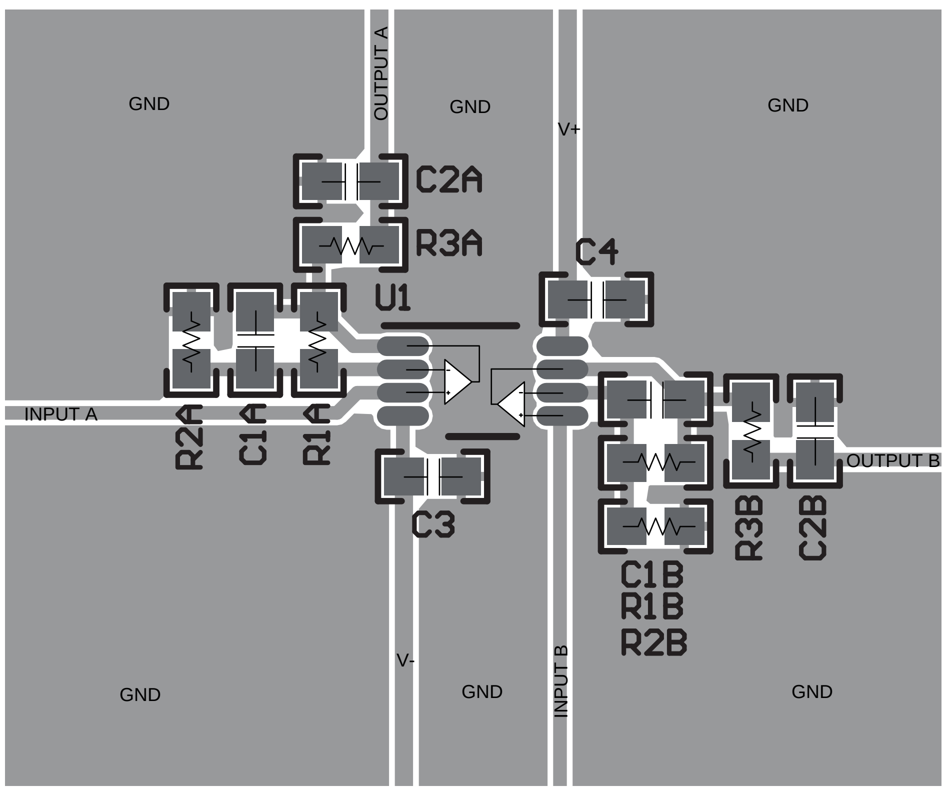


Figure 30. Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

Texas Instruments, *Circuit Board Layout Techniques*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMV722QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	R6EQ
LMV722QDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	R6EQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

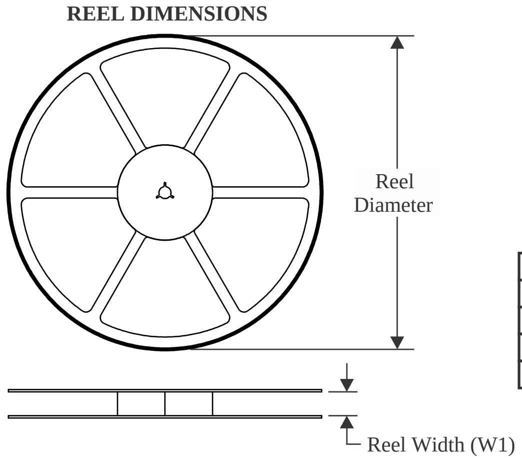
OTHER QUALIFIED VERSIONS OF LMV722-Q1 :

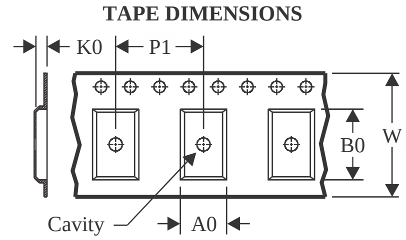
- Catalog : LMV722

NOTE: Qualified Version Definitions:

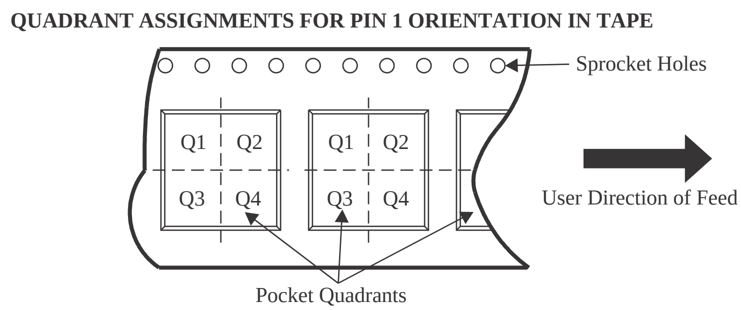
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION





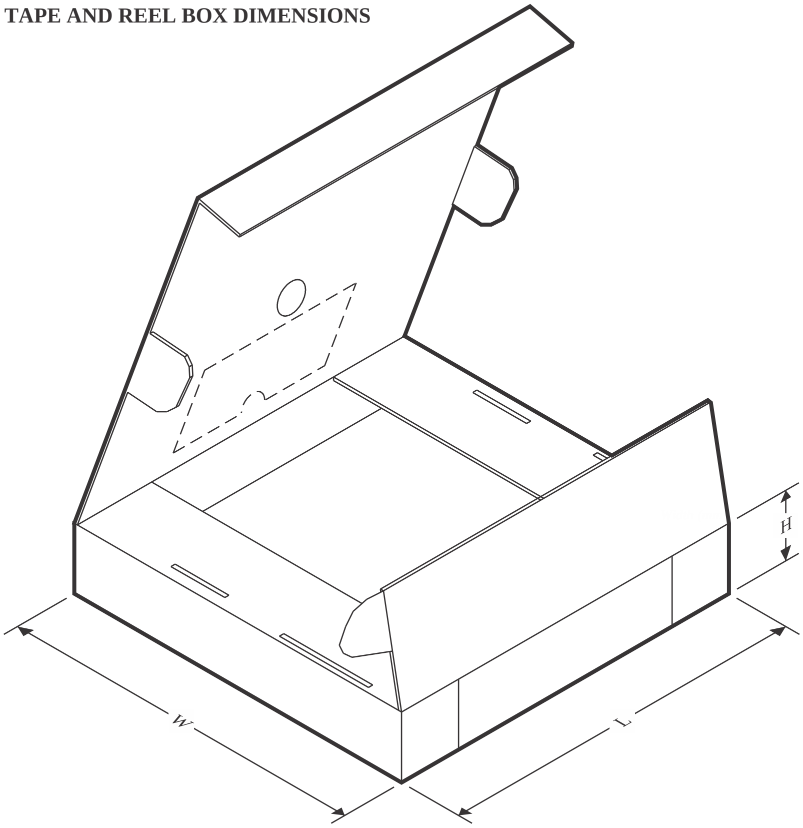
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

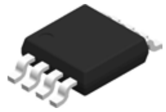
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV722QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

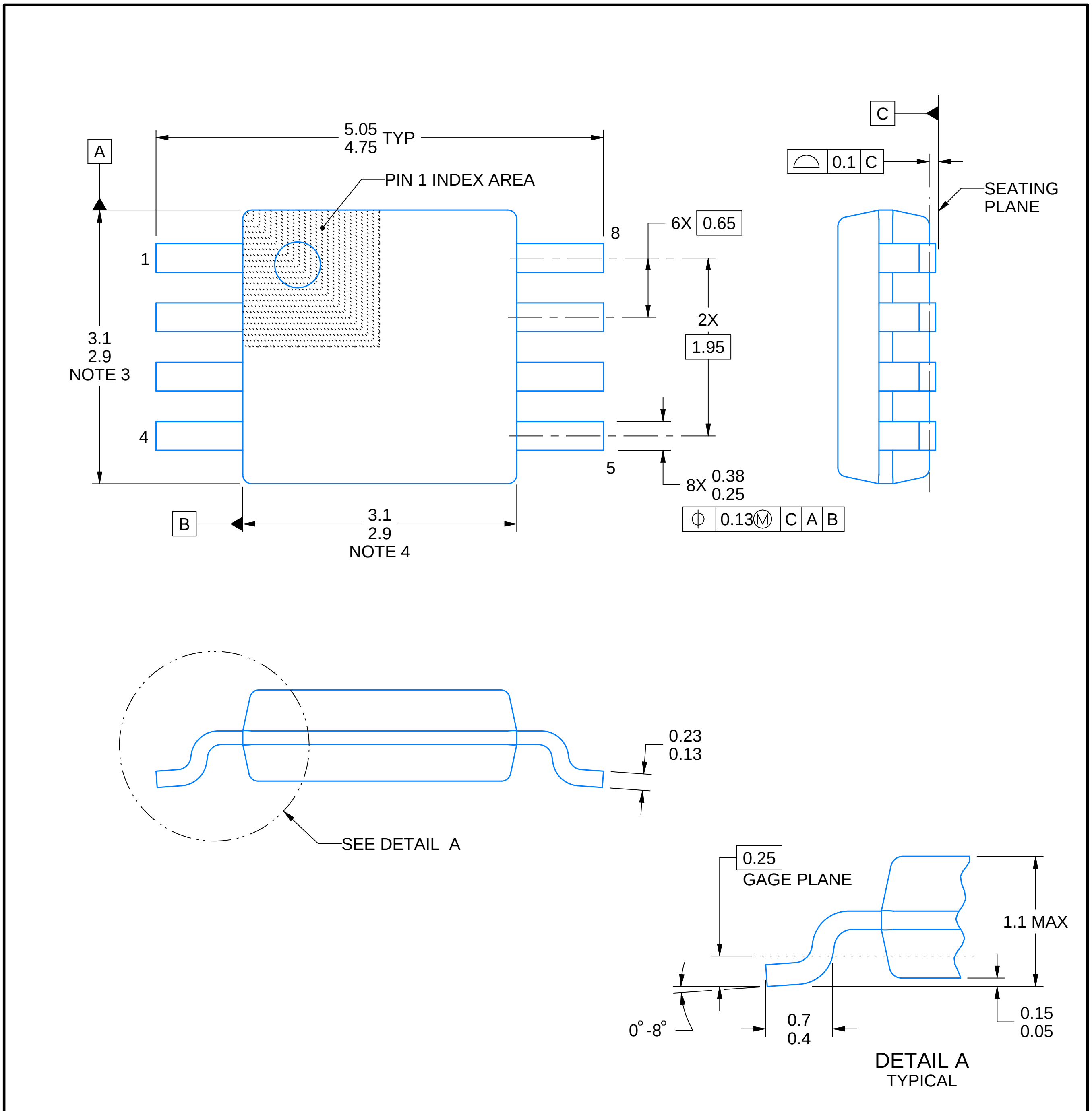
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV722QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0





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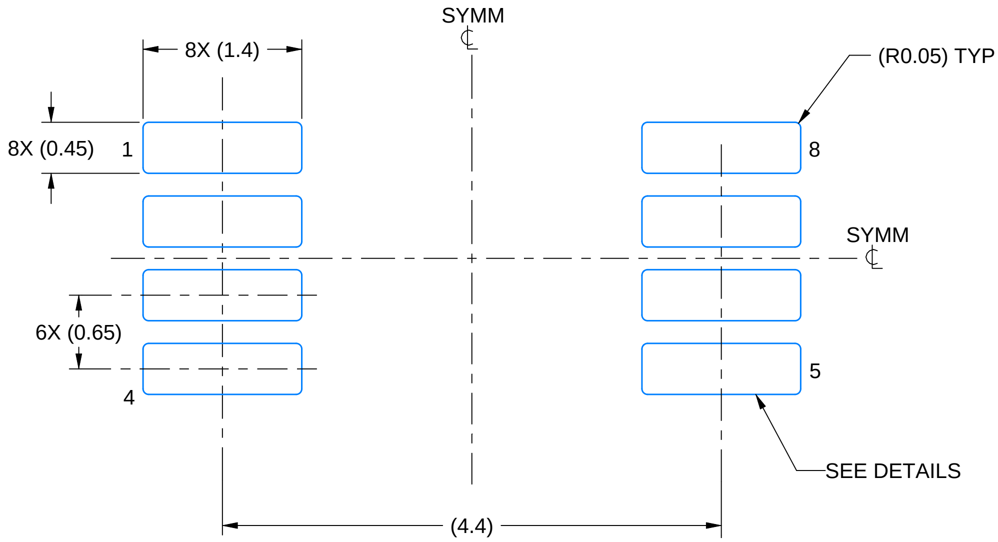
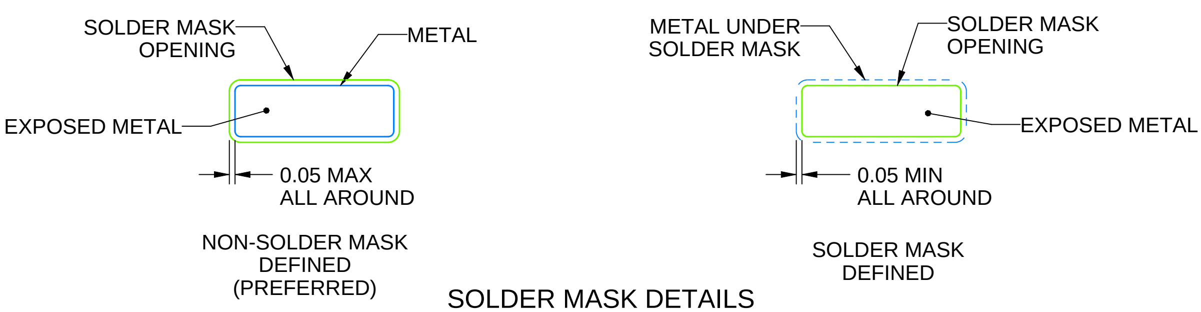
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

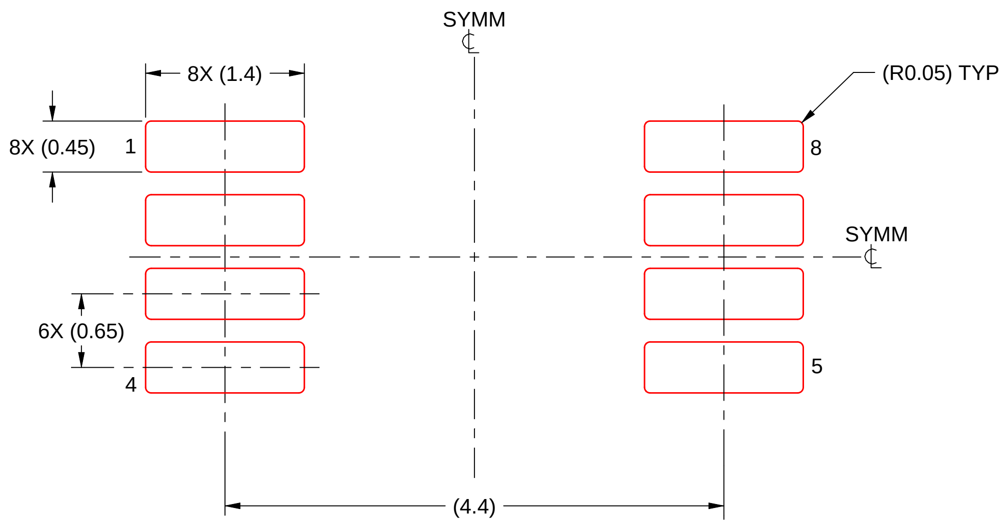


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.