LMV341-Q1, LMV344-Q1 Rail-to-Rail Output CMOS Operational Amplifiers

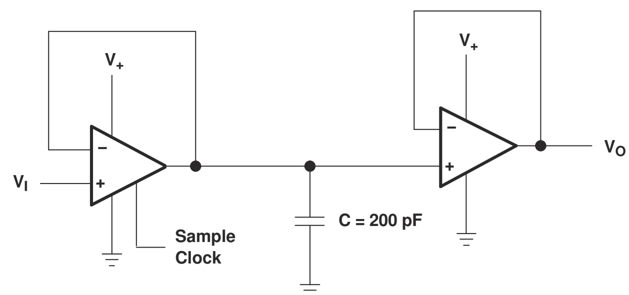
1 Features

- Qualified for Automotive Applications
- 2.7V and 5V Performance
- Rail-to-Rail Output Swing
- Input Bias Current: 1pA typical
- Input Offset Voltage: 0.25mV typical
- Low Supply Current: 100µA typical
- Gain Bandwidth: 1MHz typical
- Slew Rate: 1V/µs typical
- Turn-On Time From Shutdown: 5µs typical
- Input Referred Voltage Noise (at 10kHz): 20nV/√Hz

2 Description

The LMV341 and LMV344 devices are single and quad CMOS operational amplifiers, respectively, with low voltage, low power, and rail-to-rail output swing capabilities. The PMOS input stage offers an ultra-low input bias current of 1pA (typical) and an offset voltage of 0.25mV (typical). The single supply amplifier is designed specifically for low-voltage (2.7V to 5V) operation, with a wide common-mode input voltage range that typically extends from –0.2Vto 0.8V from the positive supply rail. Additional features are a 20nV/√ Hz voltage noise at 10kHz, 1MHz unity-gain bandwidth, 1V/µs slew rate, and 100µA current consumption per channel.

An extended industrial temperature range from –40°C to 125°C makes this device an excellent choice for automotive applications.



Application Circuit: Sample-and-Hold Circuit

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3 Device Comparison Table

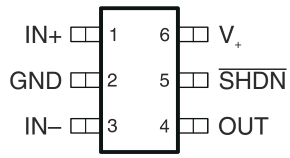
(1)

T_A	PACKAGE[2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING[3]
–40°C to 125°C	SC-70 – DCK	Reel of 3000	LMV341QDCKRQ1	RR_
	SOT-23 – DBV	Reel of 3000	LMV341QDBVRQ1	RCH_
	TSSOP – PW	Reel of 2000	LMV344IPWRQ1	LMV344Q

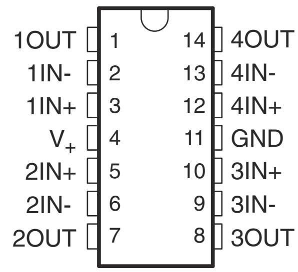
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) DBV/DCK: The actual top-side marking has one additional character that designates the wafer fab/assembly site.

4 Pin Configuration and Functions

LMV341
DBV OR DCK PACKAGE
(TOP VIEW)



LMV344
PW PACKAGE
(TOP VIEW)



5 Specifications

5.1 Absolute Maximum Ratings

(1)

over operating free-air temperature range (unless otherwise noted)

V_+	Supply voltage(2)		5.5V
V_{ID}	Differential input voltage(3)		±5.5V
V_I	Input voltage range (either input)		0 to 5.5V
θ_{JA}	Package thermal impedance(4) (5)	DBV package	165°C/W
		DCK package	259°C/W
		PW package	113°C/W
T_J	Operating virtual junction temperature		150°C
T_{stg}	Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values (except differential voltages and V_+ specified for the measurement of I_{OS}) are with respect to the network GND.
(3) Differential voltages are at IN+ with respect to IN−.
(4) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(5) The package thermal impedance is calculated in accordance with JESD 51-7.

5.2 Recommended Operating Conditions

		MIN	MAX	UNIT
V_+	Supply voltage (single-supply operation)	2.5	5.5	V
T_A	Operating free-air temperature	–40	125	°C

5.3 ESD Ratings

TEST CONDITIONS	TYP	UNIT
Human-Body Model (HBM)	2000	V
Machine Model (MM)	200	V

5.4 Electrical Characteristics 2.7V

V_+ = 2.7V, GND = 0V, V_{IC} = V_O = V_+/2, R_L > 1MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	LMV341			LMV344			UNIT
					MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
V_{IO}	Input offset voltage			25°C		0.25	4		0.25	4	mV
				Full range			4.5			4.5	
α_{VIO}	Average temperature coefficient of input offset voltage			Full range		1.7			1.7		μV/°C
I_{IB}	Input bias current			25°C		1	120		1	120	pA
				–40°C to 85°C			250			250	
				–40°C to 125°C			3			3	nA
I_{IO}	Input offset current			25°C		6.6			6.6		fA
CMRR	Common-mode rejection ratio	0 ≤ V_{ICR} ≤ 1.7V		25°C	40	80		56	80		dB
		0 ≤ V_{ICR} ≤ 1.6V		Full range	36			50			
k_{SVR}	Supply-voltage rejection ratio	2.7V ≤ V_+ ≤ 5V		25°C	45	82		65	82		dB
				Full range	60			60			
V_{ICR}	Common-mode input voltage range	CMRR ≥ 50dB		25°C	0	–0.2 to 1.9	1.7	0	–0.2 to 1.9	1.7	V
A_V	Large-signal voltage gain[2]	R_L = 10kΩ to 1.35V		25°C	73	113		78	113		dB
				Full range	66			70			
		R_L = 2kΩ to 1.35V		25°C	70	103		72	103		
				Full range	63			64			
V_O	Output swing (delta from supply rails)	R_L = 2kΩ to 1.35V	Low level	25°C		24	60		24	60	mV
				Full range			95			95	
			High level	25°C		26	60		26	60	
				Full range			95			95	
		R_L = 10kΩ to 1.35V	Low level	25°C		5	30		5	30	
				Full range			40			40	
			High level	25°C		5.3	30		5.3	30	
				Full range			40			40	
I_{CC}	Supply current (per channel)			25°C		100	170		150	200	μA
				Full range			230			230	
I_{OS}	Output short- circuit current	Sourcing		25°C	20	32		18	24		mA
		Sinking			15	24		15	24		
SR	Slew rate	R_L = 10kΩ[3]		25°C		1			1		V/μs
GBM	Unity-gain bandwidth	R_L = 10kΩ, C_L = 200pF		25°C		1			1		MHz
Φ_m	Phase margin	R_L = 100kΩ		25°C		72			72		deg
G_m	Gain margin	R_L = 100kΩ		25°C		20			20		dB
V_n	Equivalent input noise voltage	f = 1kHz		25°C		40			40		nV/√Hz
I_n	Equivalent input noise current	f = 1kHz		25°C		0.001			0.001		pA/√Hz
THD	Total harmonic distortion	f = 1kHz, A_V = 1, R_L = 600Ω, V_I = 1 V_{PP}		25°C		0.017			0.017		%

(1) Typical values represent the most likely parametric norm.
(2) GND + 0.2V ≤ V_O ≤ V_+ – 0.2V
(3) Connected as voltage follower with 2V_{PP} step input. Number specified is the slower of the positive and negative slew rates.

5.5 Shutdown Characteristics 2.7V

V_+ = 2.7V, GND = 0V, V_{IC} = V_O = $V_+/2$, R_L > 1MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{CC(SHDN)}$	Supply current in shutdown mode (per channel)	V_{SD} = 0V	25°C		0.045	1000	nA
			Full range			1.5	μA
$t_{(on)}$	Amplifier turn-on time		25°C		5		μs
V_{SD}	Shutdown pin voltage range	ON mode	25°C		1.7 to 2.7	2.4 to 2.7	V
		Shutdown mode			0 to 1	0 to 0.2	

5.6 Electrical Characteristics 5V

$V_+ = 5V$, GND = 0V, $V_{IC} = V_O = V_+/2$, $R_L > 1M\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	LMV341			LMV344			UNIT
					MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
V_{IO}	Input offset voltage			25°C		0.25	4		0.25	4	mV
				Full range			4.5			4.5	
α_{VIO}	Average temperature coefficient of input offset voltage			Full range		1.9			1.9		μV/°C
I_{IB}	Input bias current			25°C		1	200		1	200	pA
				–40°C to 85°C			375			375	
				–40°C to 125°C			5			5	nA
I_{IO}	Input offset current			25°C		6.6			6.6		fA
CMRR	Common-mode rejection ratio	$0 \le V_{ICR} \le 4V$		25°C	46	86		56	86		dB
		$0 \le V_{ICR} \le 3.9V$		Full range	47			50			
k_{SVR}	Supply-voltage rejection ratio	$2.7V \le V_+ \le 5V$		25°C	45	82		65	82		dB
				Full range	44			60			
V_{ICR}	Common-mode input voltage range	CMRR ≥ 50dB		25°C	0	–0.2 to 4.2	4	0	–0.2 to 4.2	4	V
A_V	Large-signal voltage gain[2]	$R_L = 10k\Omega$ to 2.5V		25°C	78	116		78	116		dB
				Full range	70			70			
		$R_L = 2k\Omega$ to 2.5V		25°C	72	107		72	107		
				Full range	64			64			
V_O	Output swing (delta from supply rails)	$R_L = 2k\Omega$ to 2.5V	Low level	25°C		32	67		32	60	mV
				Full range			95			95	
			High level	25°C		34	60		34	60	
				Full range			95			95	
		$R_L = 10k\Omega$ to 2.5V	Low level	25°C		7	30		7	30	
				Full range			45			40	
			High level	25°C		7	30		7	30	
				Full range			40			40	
I_{CC}	Supply current (per channel)			25°C		150	200		150	200	μA
				Full range			260			260	
I_{OS}	Output short-circuit current	Sourcing		25°C	85	113		70	90		mA
		Sinking			50	75		50	75		
SR	Slew rate	$R_L = 10k\Omega$[3]		25°C		1			1		V/μs
GBM	Unity-gain bandwidth	$R_L = 10k\Omega$, $C_L = 200pF$		25°C		1			1		MHz
Φ_m	Phase margin	$R_L = 100k\Omega$		25°C		70			70		deg
G_m	Gain margin	$R_L = 100k\Omega$		25°C		20			20		dB
V_n	Equivalent input noise voltage	f = 1kHz		25°C		39			39		$nV/\sqrt{Hz}$
I_n	Equivalent input noise current	f = 1kHz		25°C		0.001			0.001		$pA/\sqrt{Hz}$
THD	Total harmonic distortion	f = 1kHz, $A_V = 1$, $R_L = 600\Omega$, $V_I = 1\ V_{PP}$		25°C		0.012			0.012		%

(1) Typical values represent the most likely parametric norm.
(2) $GND + 0.2V \le V_O \le V_+ - 0.2V$
(3) Connected as voltage follower with $2V_{PP}$ step input. Number specified is the slower of the positive and negative slew rates.

5.7 Shutdown Characteristics 5V

V_+ = 5V, GND = 0V, V_{IC} = V_O = V_+/2, R_L > 1MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{CC(SHDN)}$	Supply current in shutdown mode (per channel)	V_{SD} = 0V	25°C		0.033	1	μA
			Full range			1.5	
$t_{(on)}$	Amplifier turn-on time		25°C		5		μs
V_{SD}	Shutdown pin voltage range	ON mode	25°C		3.1 to 5	4.5 to 5	V
		Shutdown mode			0 to 1	0 to 0.2	

6 Typical Characteristics

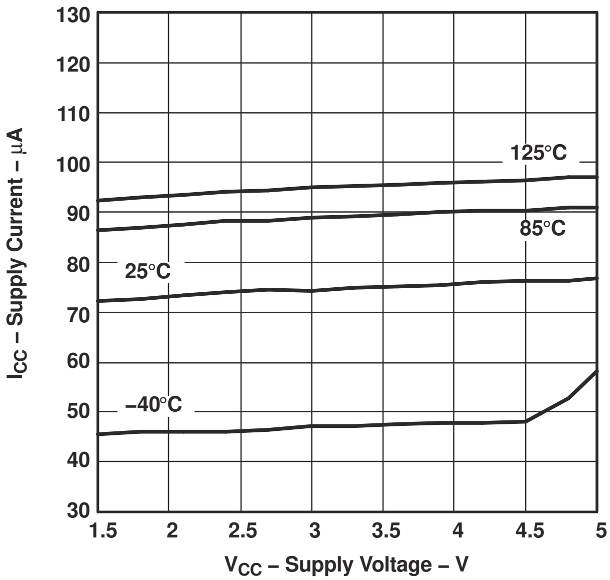


Figure 6-1. Supply Current vs Supply Voltage

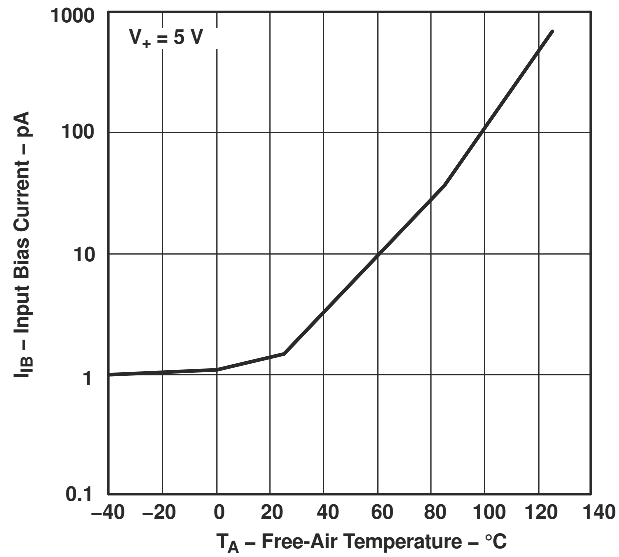


Figure 6-2. Input Bias Current vs Temperature

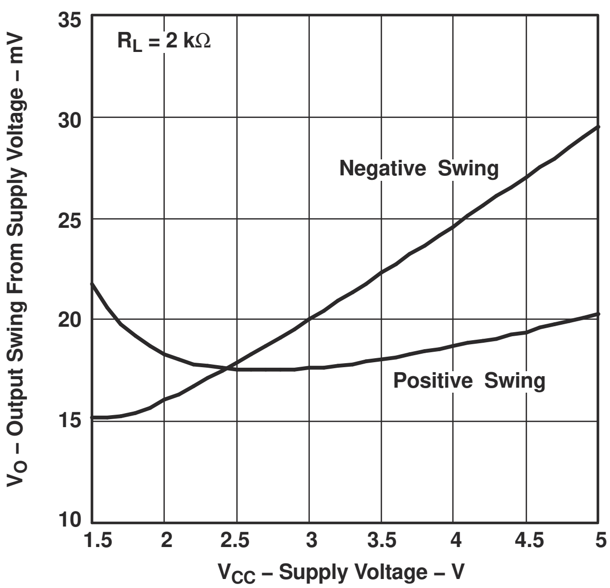


Figure 6-3. Output Voltage Swing vs Supply Voltage

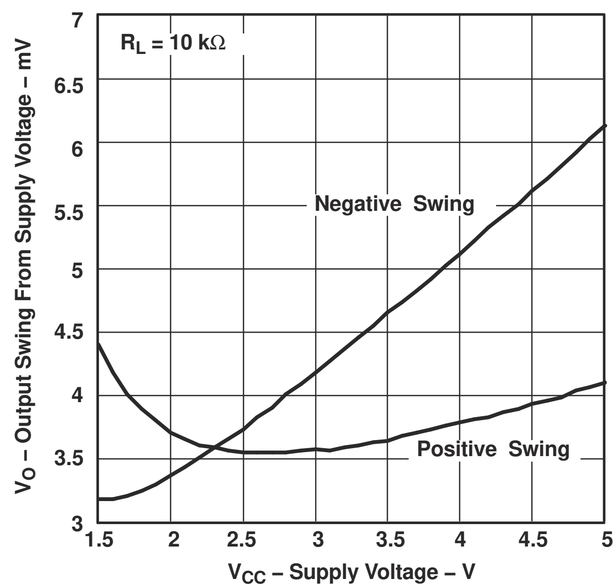


Figure 6-4. Output Voltage Swing vs Supply Voltage

6 Typical Characteristics (continued)

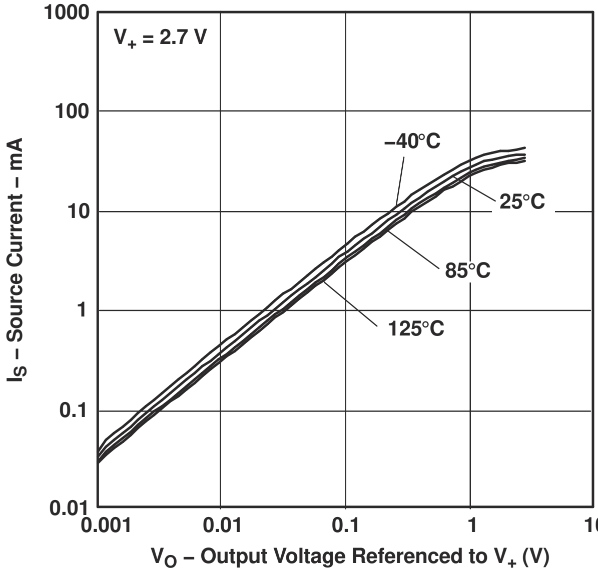


Figure 6-5. Source Current vs Output Voltage

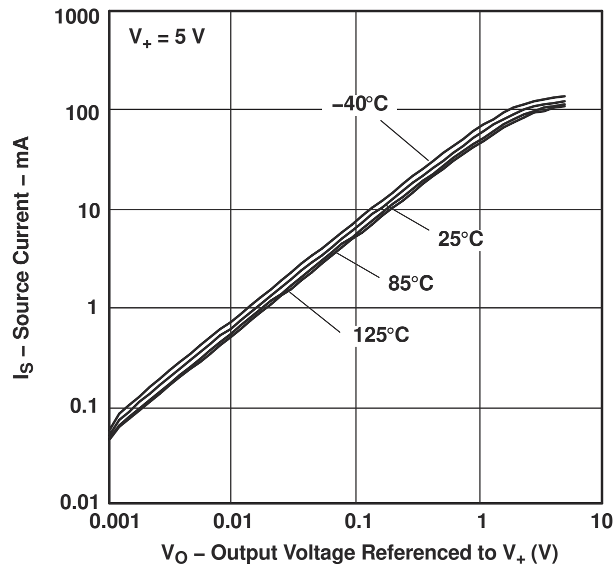


Figure 6-6. Source Current vs Output Voltage

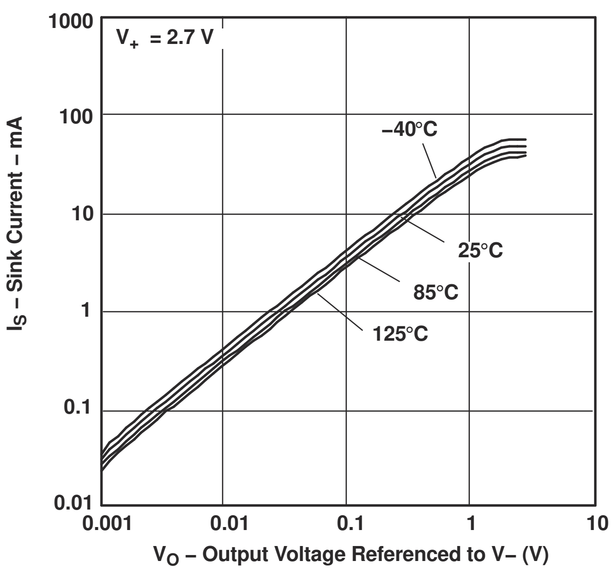


Figure 6-7. Sink Current vs Output Voltage

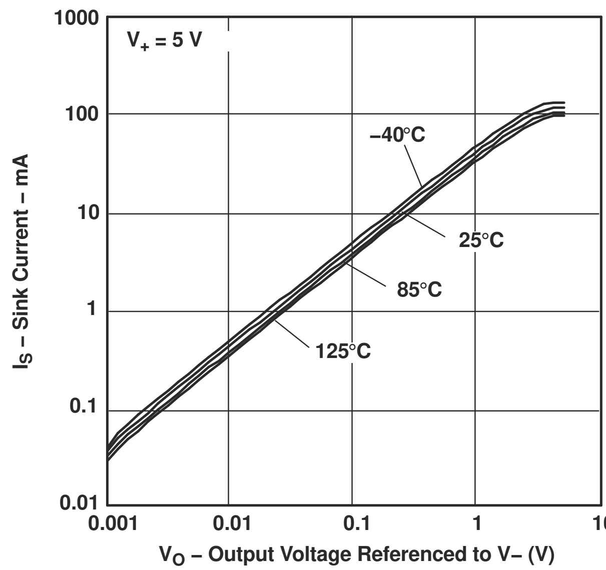


Figure 6-8. Sink Current vs Output Voltage

6 Typical Characteristics (continued)

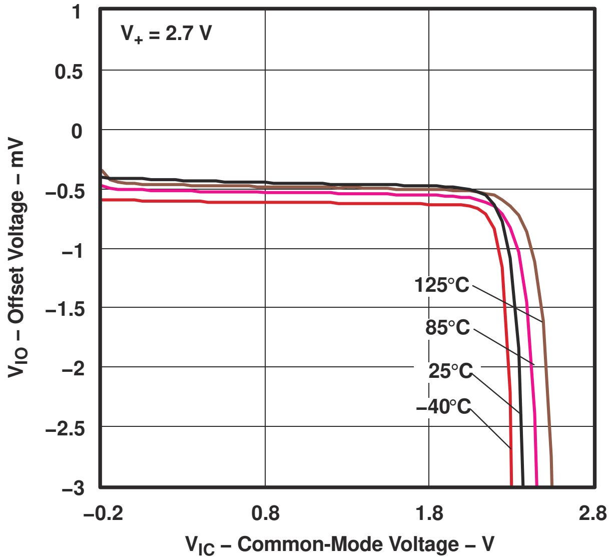


Figure 6-9. Offset Voltage vs Common-mode Voltage

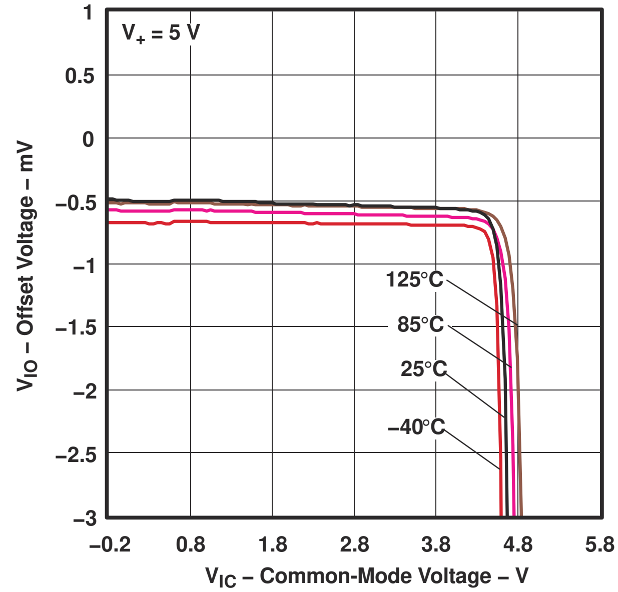


Figure 6-10. Offset Voltage vs Common-mode Voltage

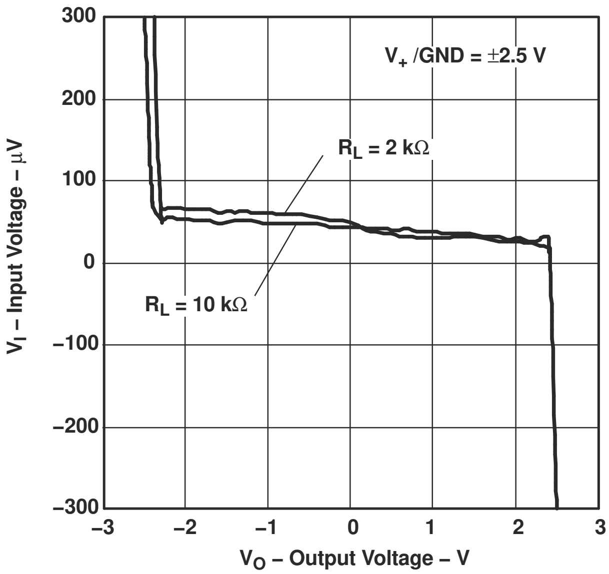


Figure 6-11. Input Voltage vs Output Voltage

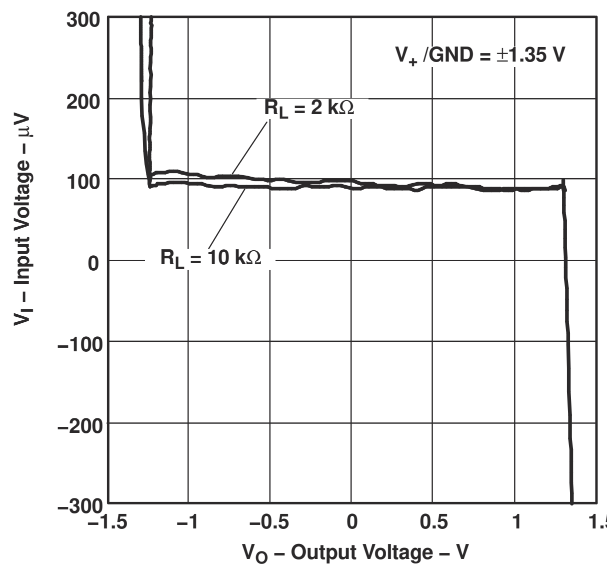


Figure 6-12. Input Voltage vs Output Voltage

6 Typical Characteristics (continued)

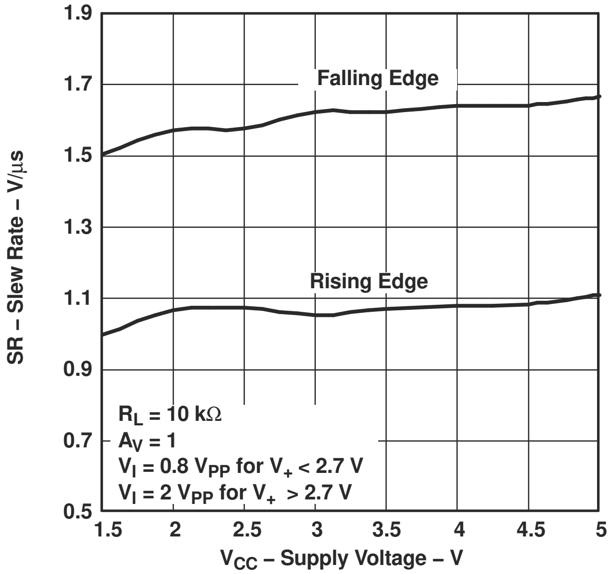


Figure 6-13. Slew Rate vs Supply Voltage

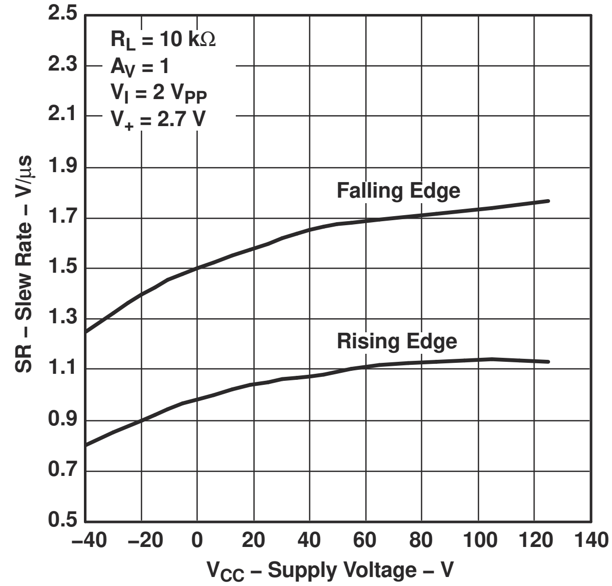


Figure 6-14. Slew Rate vs Temperature

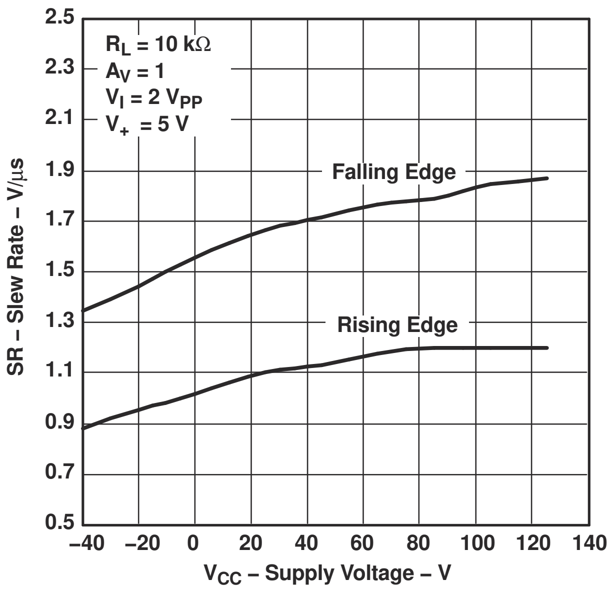


Figure 6-15. Slew Rate vs Temperature

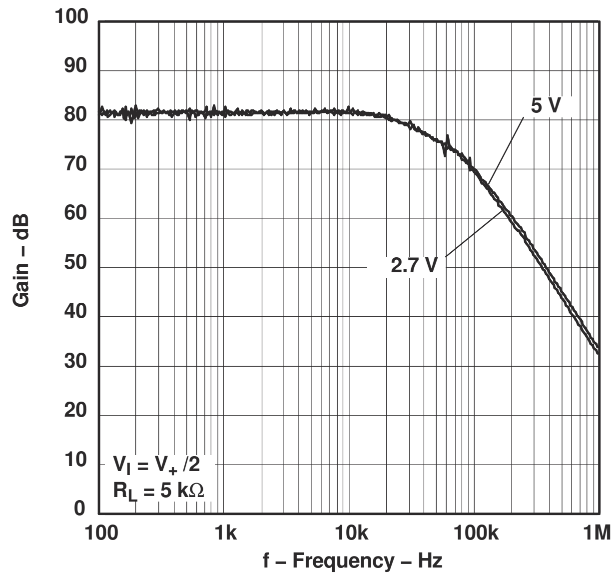


Figure 6-16. Cmrr vs Frequency

6 Typical Characteristics (continued)

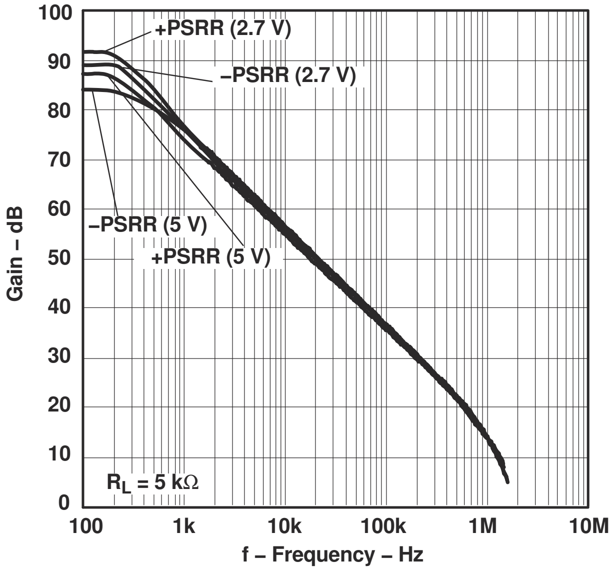


Figure 6-17. Psrr vs Frequency

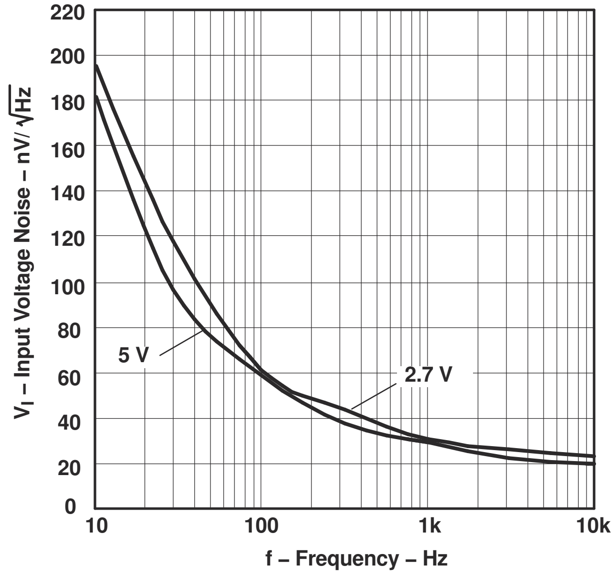


Figure 6-18. Input Voltage Noise vs Frequency

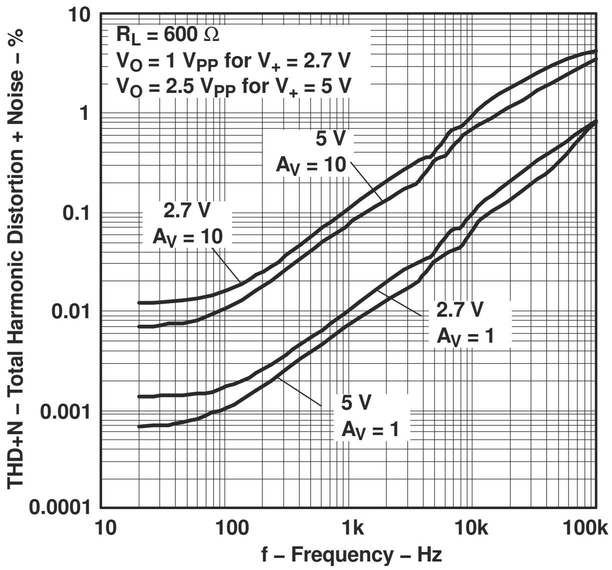


Figure 6-19. Total Harmonic Distortion + Noise vs Frequency

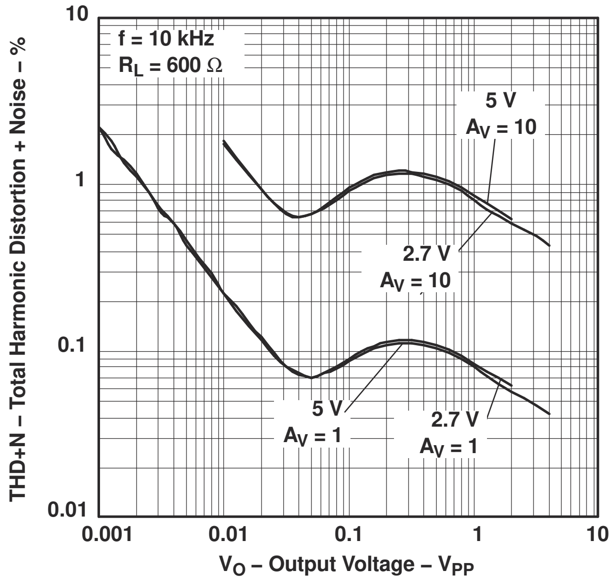


Figure 6-20. Total Harmonic Distortion + Noise vs Output Voltage

6 Typical Characteristics (continued)

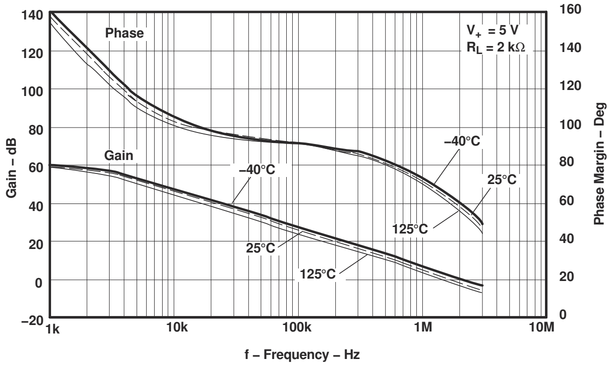


Figure 6-21. Gain And Phase Margin vs Frequency (t_a = –40°c, 25°c, 125°c)

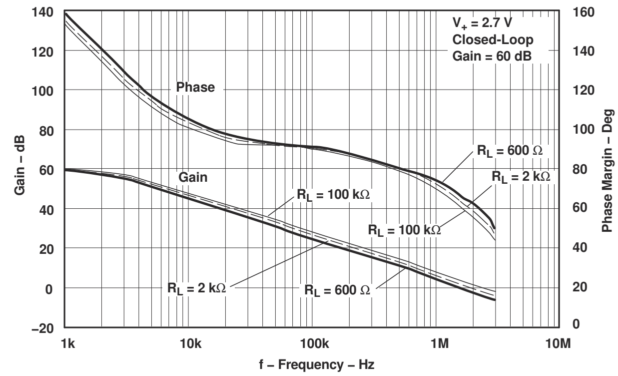


Figure 6-22. Gain And Phase Margin vs Frequency (r_l = 600ω, 2kω, 100kω)

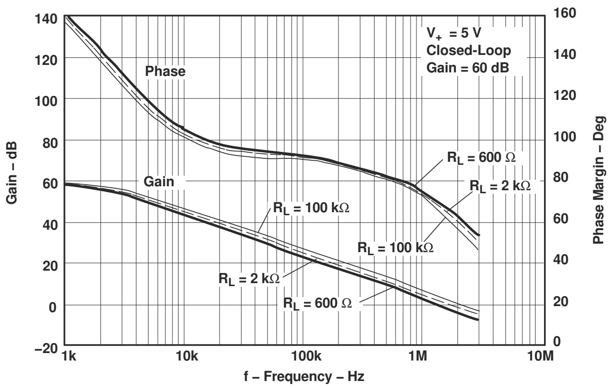


Figure 6-23. Gain And Phase Margin vs Frequency (r_l = 600ω, 2kω, 100kω)

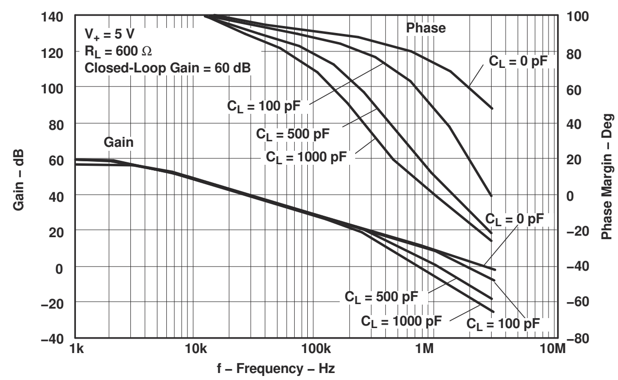


Figure 6-24. Gain And Phase Margin vs Frequency (c_l = 0pf, 100pf, 500pf, 1000pf)

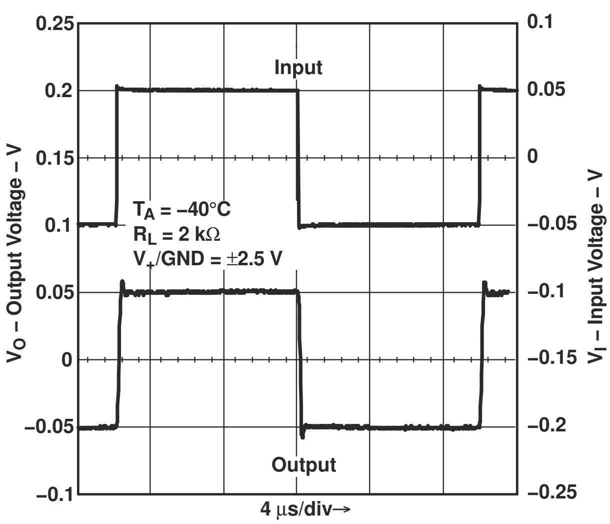


Figure 6-25. Small-Signal Noninverting Response

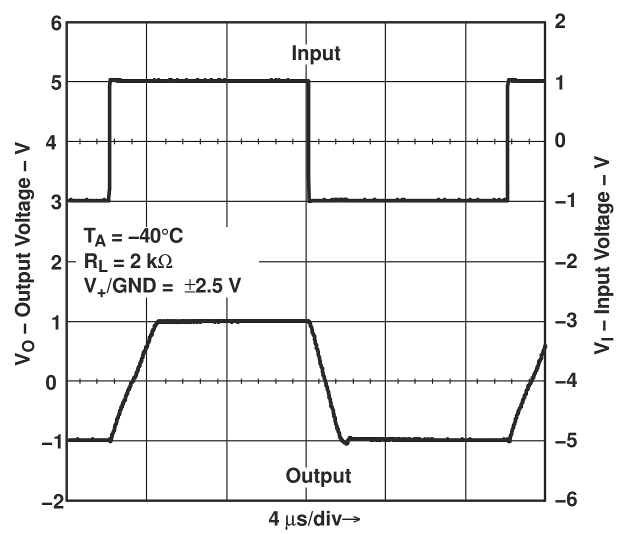


Figure 6-26. Large-Signal Noninverting Response

6 Typical Characteristics (continued)

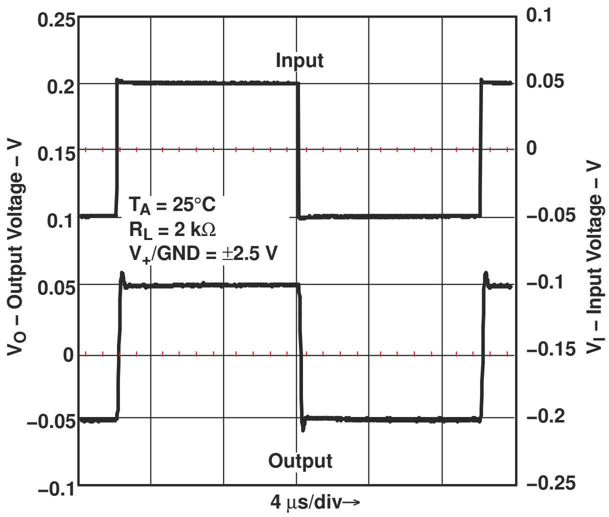


Figure 6-27. Small-Signal Noninverting Response

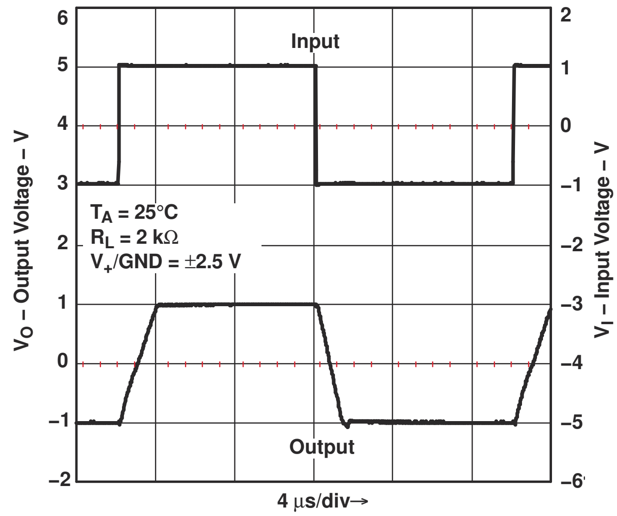


Figure 6-28. Large-Signal Noninverting Response

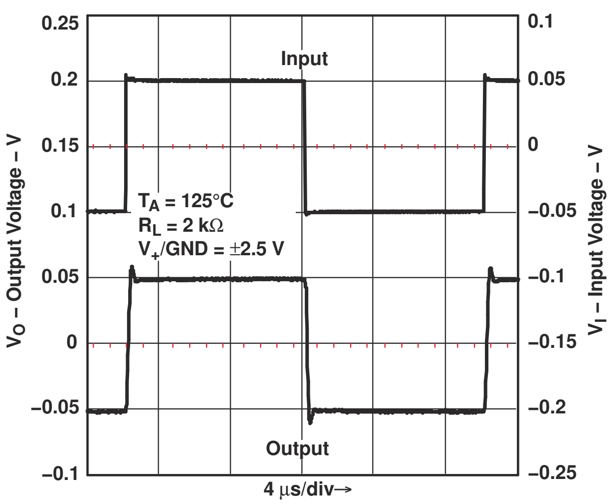


Figure 6-29. Small-Signal Noninverting Response

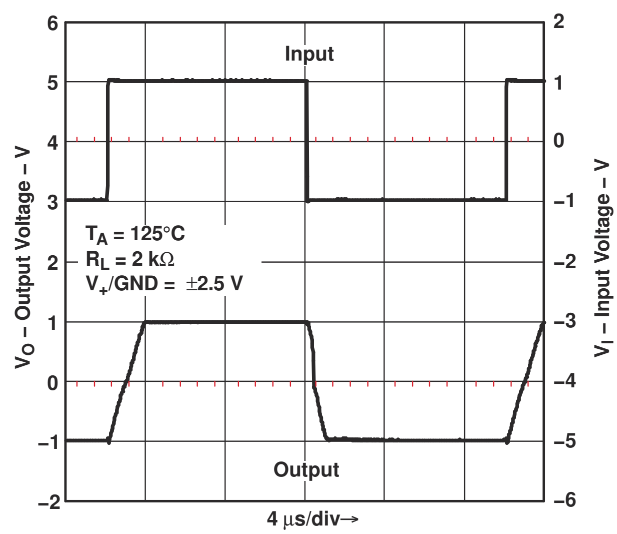


Figure 6-30. Large-Signal Noninverting Response

6 Typical Characteristics (continued)

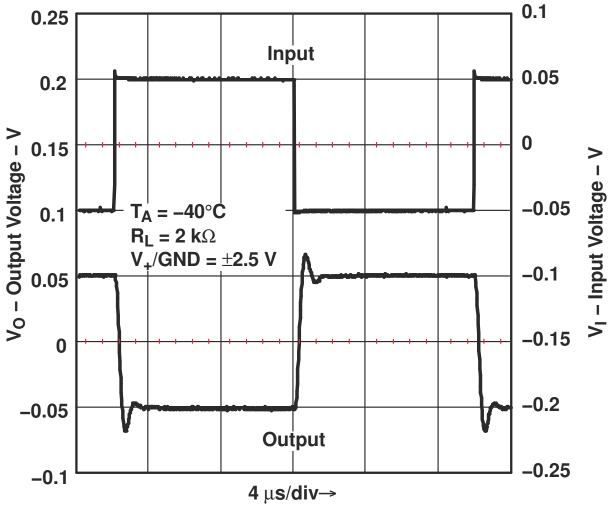


Figure 6-31. Small-Signal Inverting Response

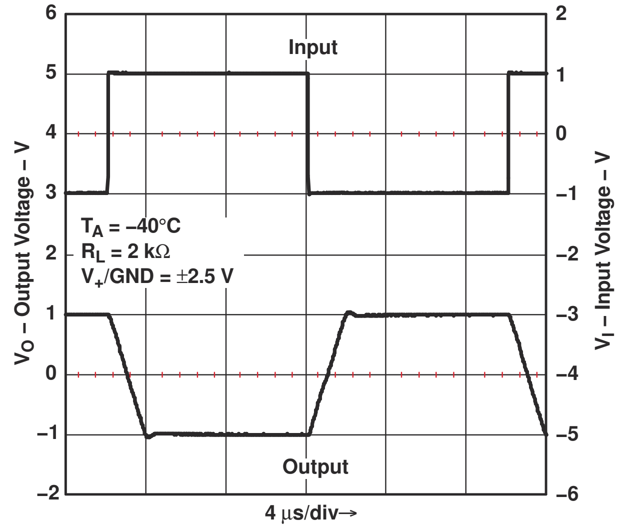


Figure 6-32. Large-Signal Inverting Response

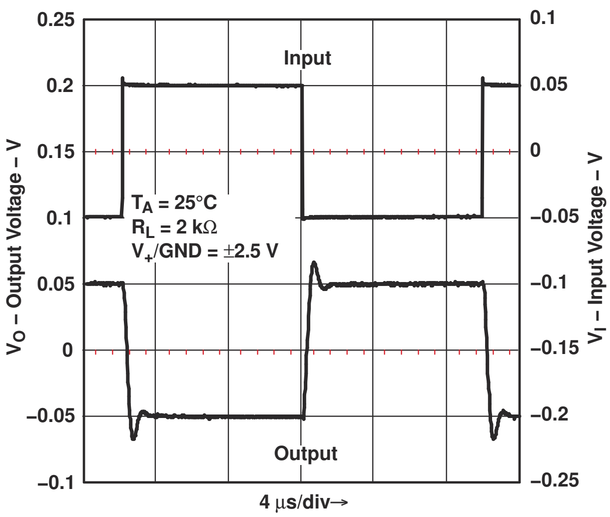


Figure 6-33. Small-Signal Inverting Response

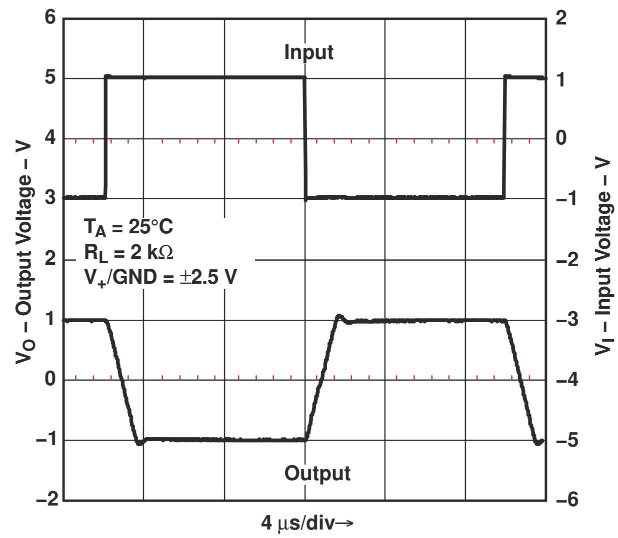


Figure 6-34. Large-Signal Inverting Response

6 Typical Characteristics (continued)

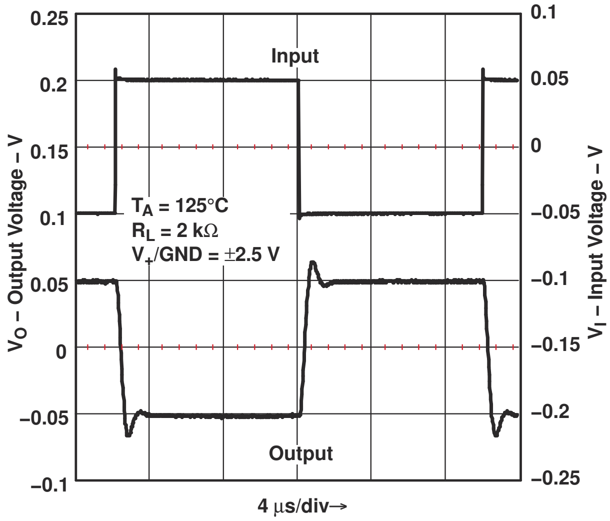


Figure 6-35. Small-Signal Inverting Response

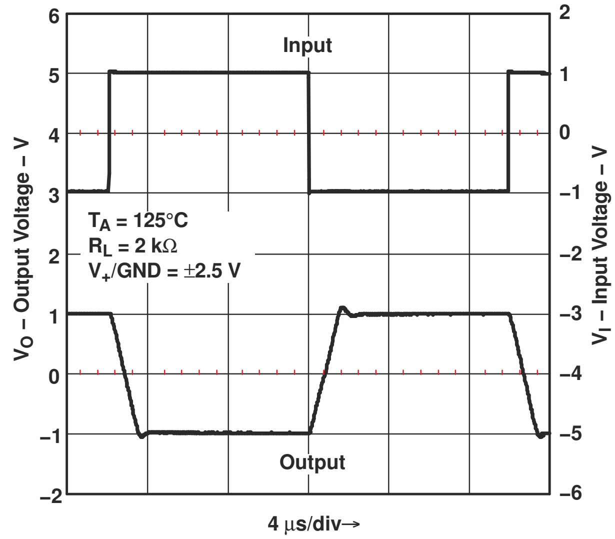


Figure 6-36. Large-Signal Inverting Response

7 Device and Documentation Support

7.1 Documentation Support

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2009) to Revision D (July 2025) — **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................. 1
- Changed supply current per channel specification at V+ = 2.7V from 100µA to 150µA (typical) and from 170µA to 200µA (maximum at 25°C)..6
- Changed recommended shutdown pin voltage range, shutdown mode specification at V+ = 2.7Vfrom 0 to 0.8V to 0 to 0.2V (maximum)..7
- Changed supply current per channel specification at V+ = 5V from 100µA to 150µA (typical)..........................8
- Changed recommended shutdown pin voltage range, shutdown mode specification at V+ = 5Vfrom 0 to 0.8V to 0 to 0.2V (maximum)..9

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMV341QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RCHE
LMV341QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RCHE
LMV341QDCKRQ1	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RRE
LMV341QDCKRQ1.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RRE
LMV341QDCKRQ1G4	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R4E, RRE)
LMV341QDCKRQ1G4.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R4E, RRE)
LMV344IPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV344Q
LMV344IPWRQ1.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV344Q

[1] **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMV341-Q1, LMV344-Q1 :

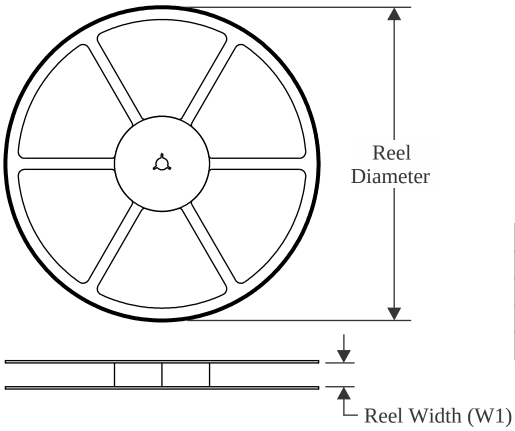
- Catalog : LMV341, LMV344

NOTE: Qualified Version Definitions:

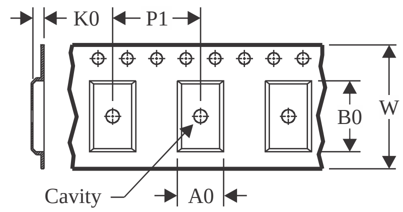
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

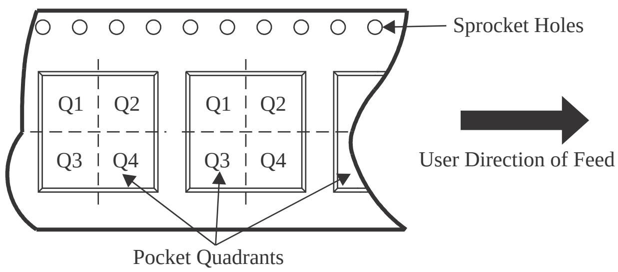


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

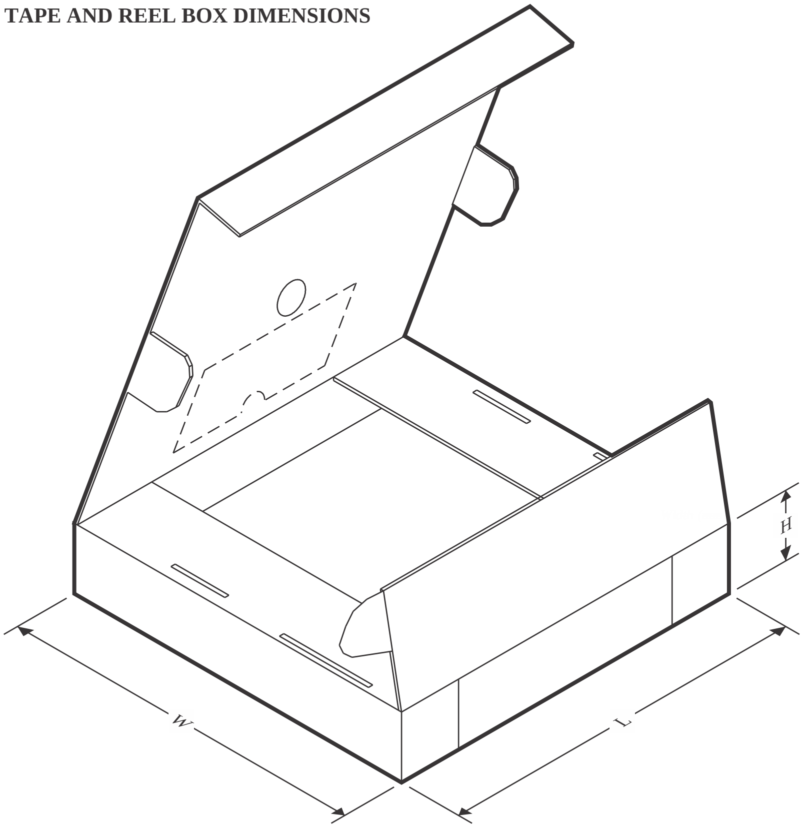
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

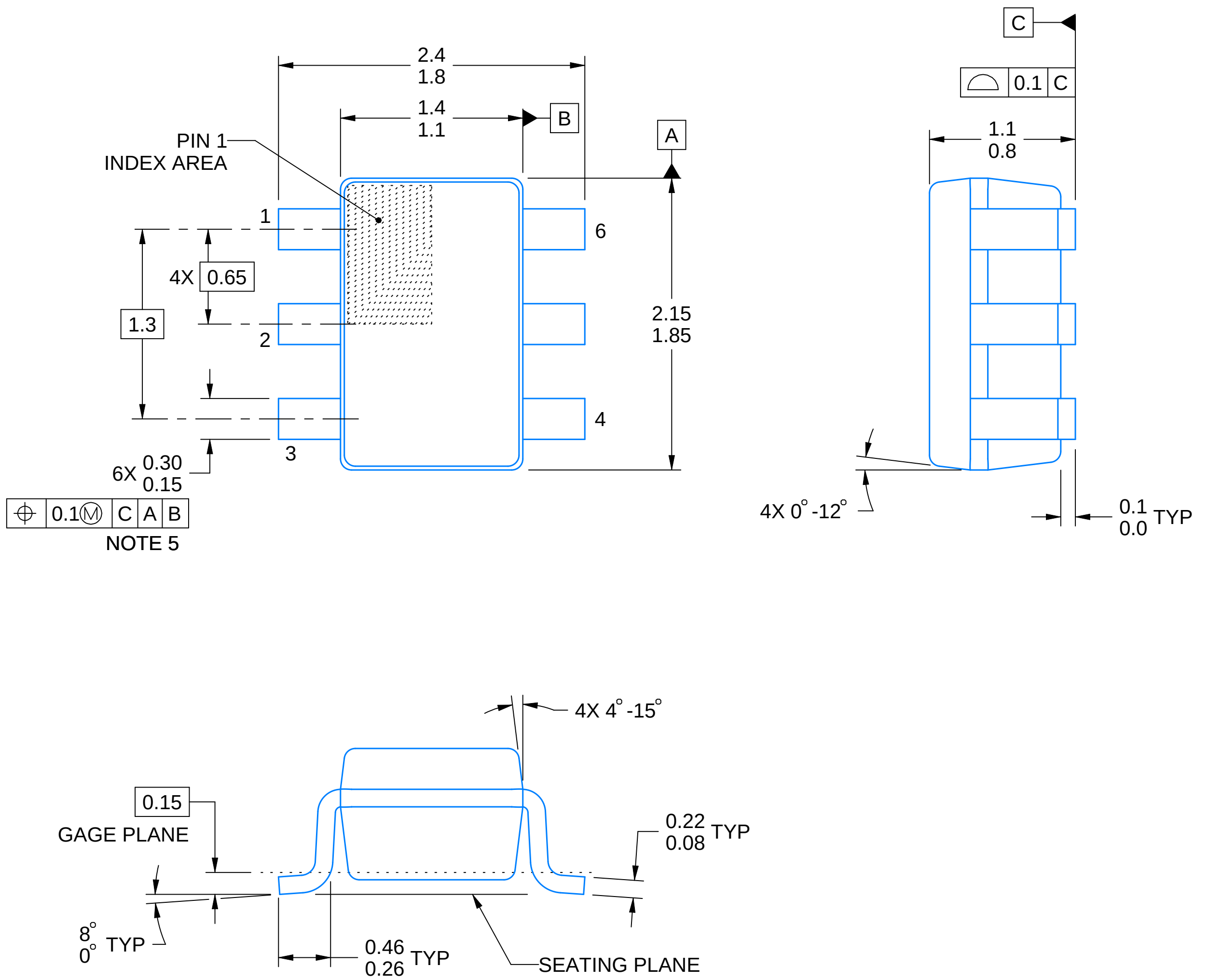
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV341QDBVRQ1	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV341QDCKRQ1	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
LMV341QDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
LMV341QDCKRQ1G4	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
LMV344IPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

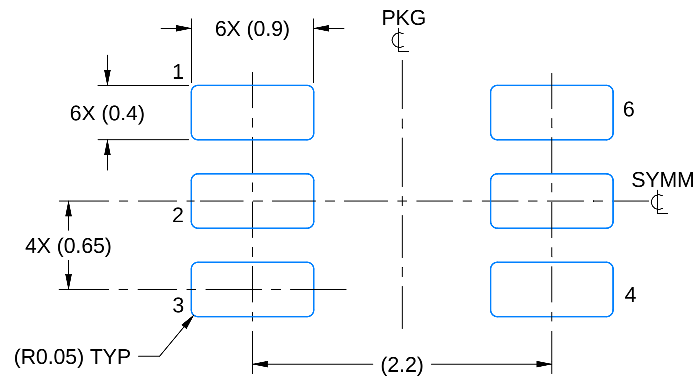
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV341QDBVRQ1	SOT-23	DBV	6	3000	200.0	183.0	25.0
LMV341QDCKRQ1	SC70	DCK	6	3000	200.0	183.0	25.0
LMV341QDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0
LMV341QDCKRQ1G4	SC70	DCK	6	3000	200.0	183.0	25.0
LMV344IPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0



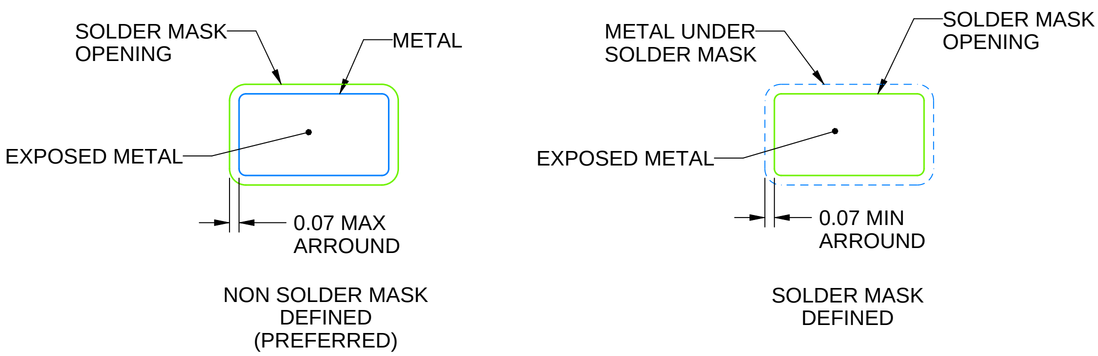
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

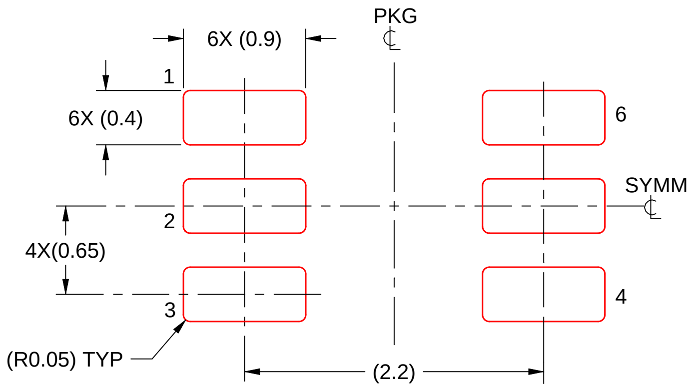


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

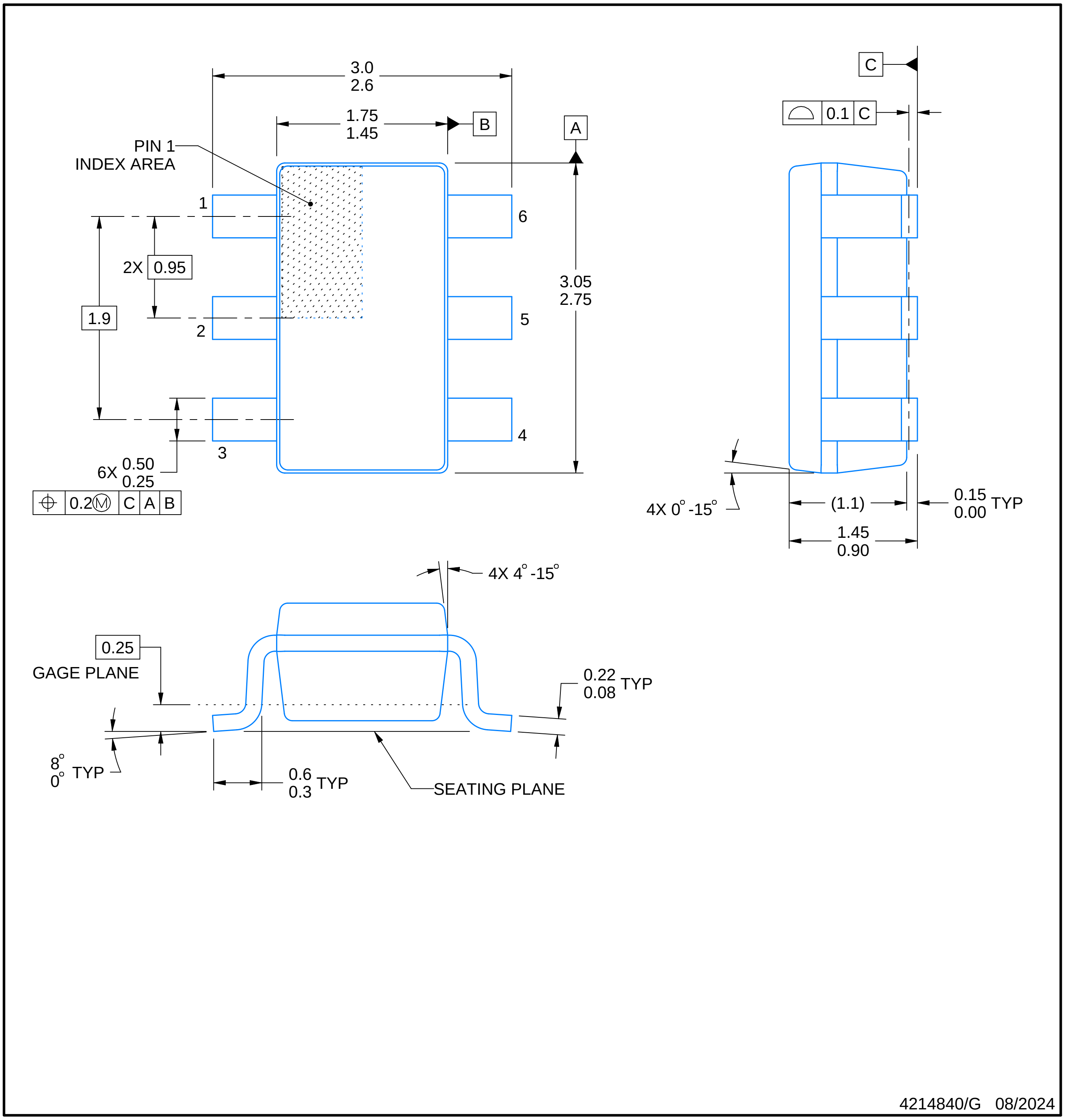


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

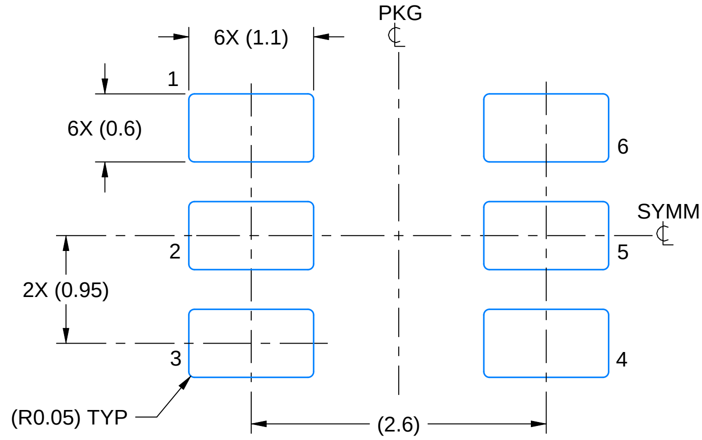
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

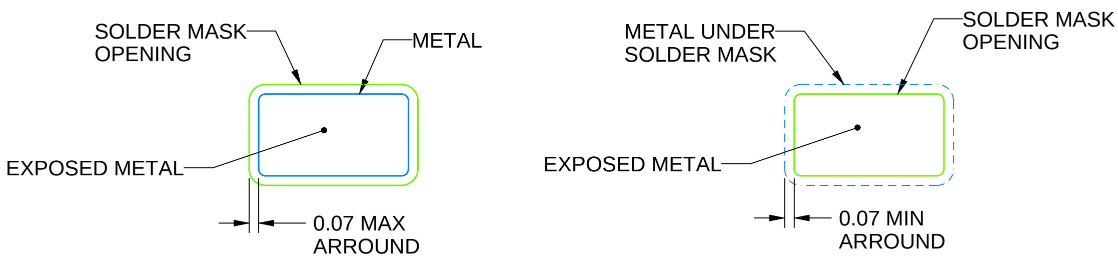


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)

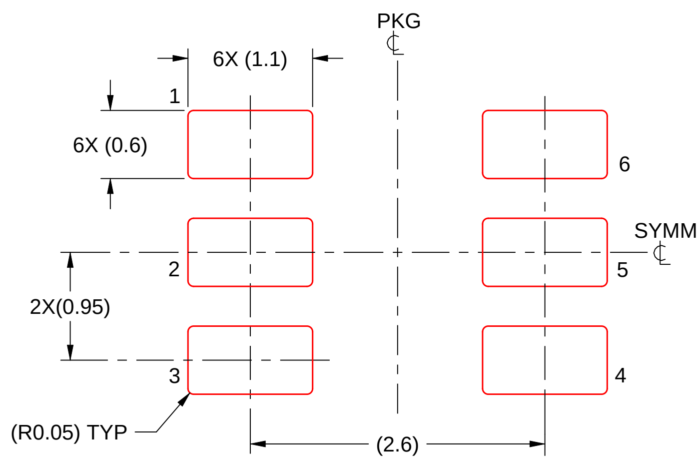
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

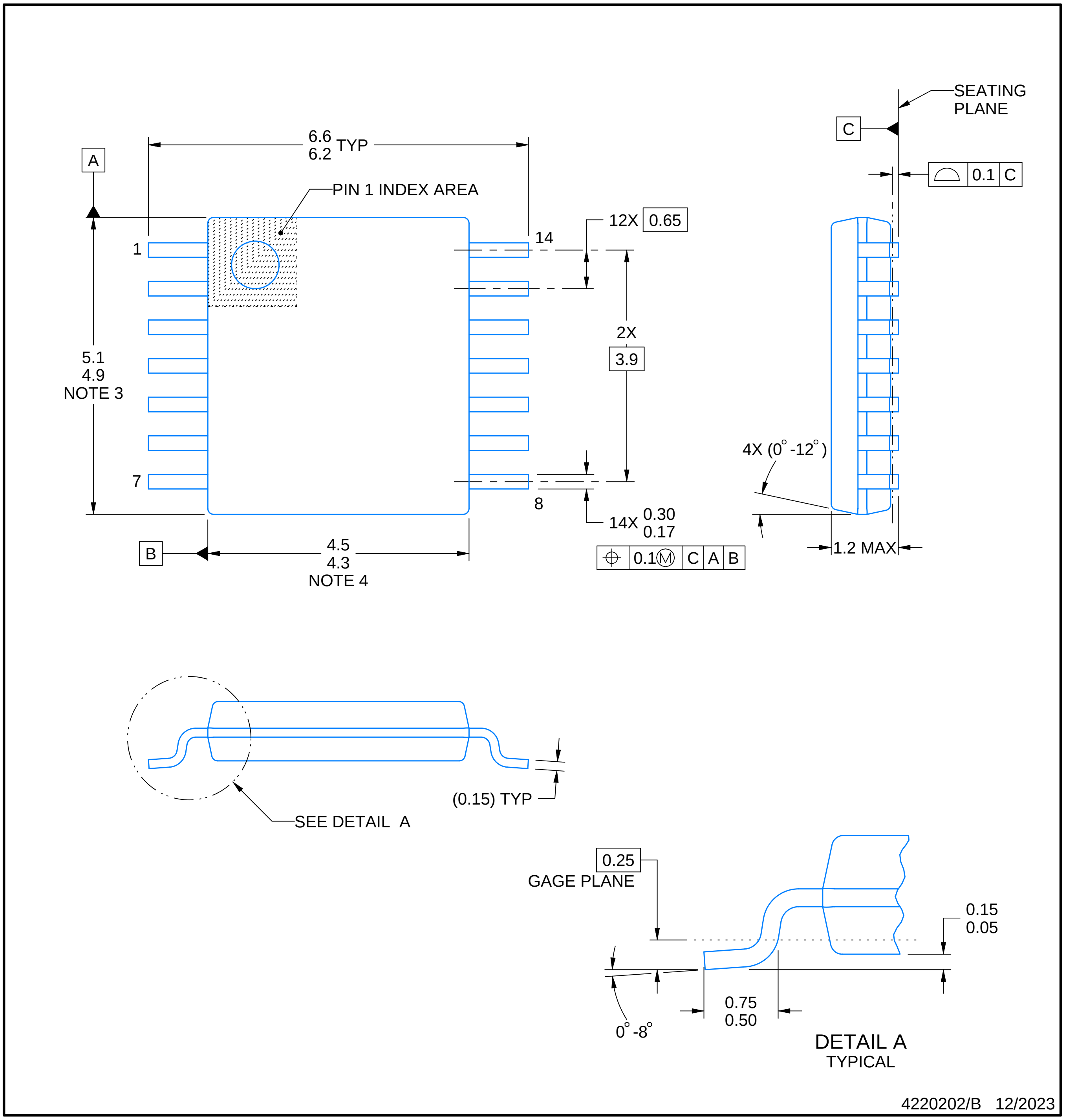


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

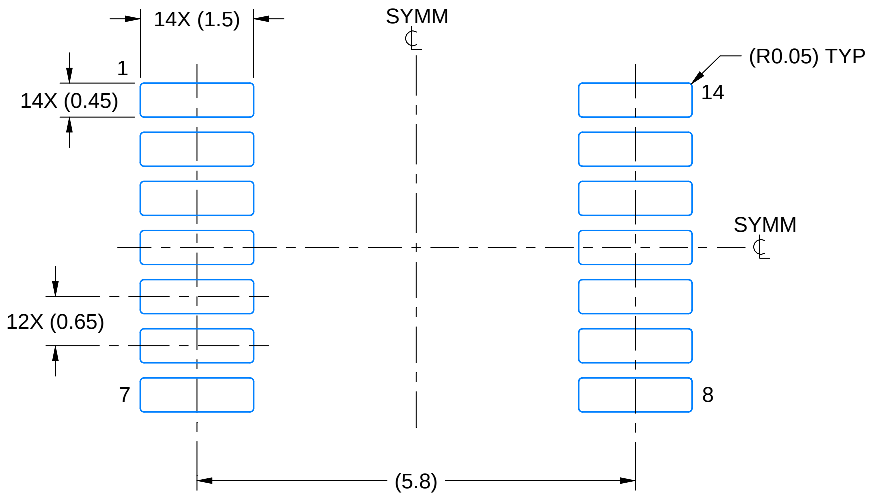
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

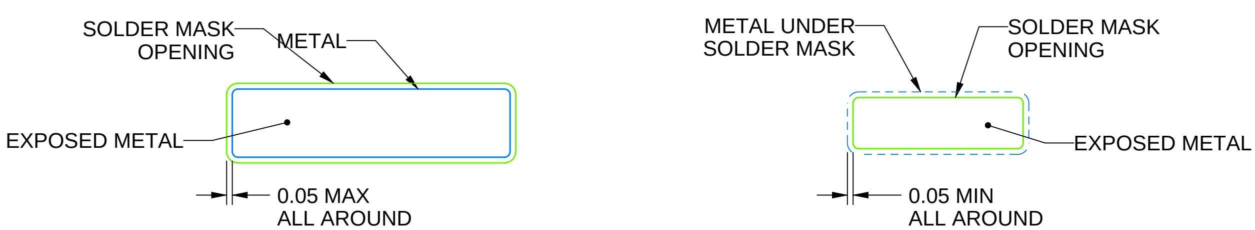


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

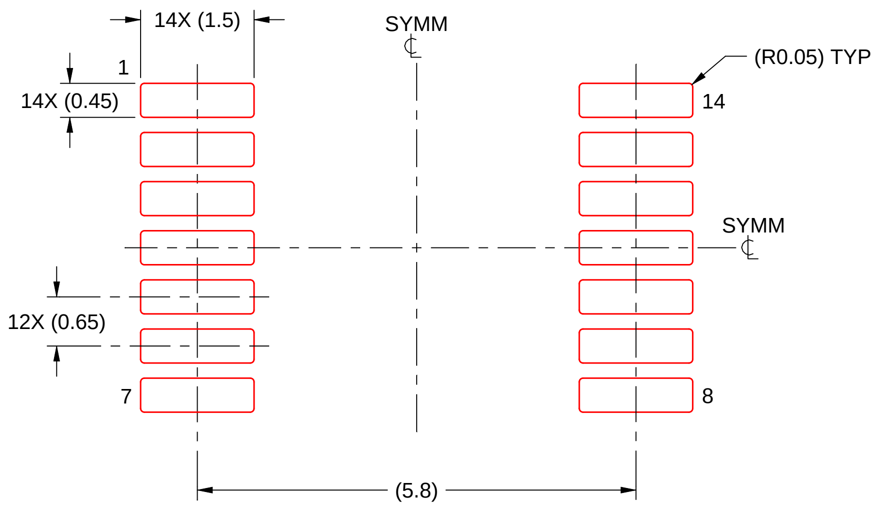


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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