

LMV34x Rail-to-Rail Output CMOS Operational Amplifiers With Shutdown

1 Features

- 2.7V and 5V performance
- Rail-to-rail output swing
- Input bias current:1pA (typical)
- Input offset voltage: 0.25mV (typical)
- Low supply current: 100µA (typical)
- Low shutdown current: 45pA (typical)
- Gain bandwidth of 1MHz (typical)
- Slew rate: 1V/µs (typical)
- Turn-on time from shutdown: 5µs (typical)
- Input referred voltage noise (at 10kHz): 20nV/√ Hz
- ESD protection exceeds JESD 22:
 - 2000V Human-Body Model (HBM)
 - 750V Charged-device model (CDM)

2 Applications

- Cordless and cellular phones
- Consumer electronics (laptops, PDAs)
- Audio preamplifiers for voice
- Portable, battery-powered electronic equipment
- Supply-current monitoring
- Battery monitoring
- **Buffers**
- **Filters**
- **Drivers**

3 Description

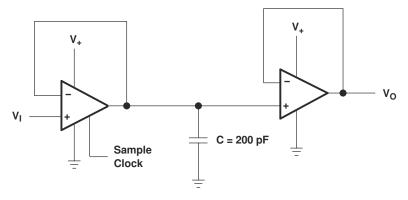
The LMV34x devices are single, dual, and quad CMOS operational amplifiers, respectively, with low voltage, low power, and rail-to-rail output swing capabilities. The PMOS input stage offers an ultralow input bias current of 1pA (typical) and an offset voltage of 0.25mV (typical). The single-supply amplifier is designed specifically for low-voltage (2.7V to 5V) operation, with a wide common-mode input voltage range that typically extends from -0.2V to 0.8V from the positive supply rail. The LMV341 (single) also offers a shutdown (SHDN) pin that can be used to disable the device. In shutdown mode, the supply current is reduced to 33nA (typical). Additional features of the family are a 20nV/√ Hz voltage noise at 10kHz, 1MHz unity-gain bandwidth, 1V/µs slew rate, and 100µA current consumption per channel.

Offered in both the SOT-23 and smaller SC70 packages, the LMV341 is suitable for the most spaceconstraint applications. The LMV342 dual device is offered in the standard SOIC and VSSOP packages. An extended industrial temperature range from -40°C to 125°C makes these devices suitable in a wide variety of commercial and industrial environments.

Package Information

PART NUMBER ⁽¹⁾	PACKAGE	BODY SIZE (NOM)						
LMV341IDCK	DCK (SC70, 6)	2.00mm × 1.25mm						
LMV341IDBV	DBV (SOT-23, 6)	2.90mm ×1.60mm						
LMV342ID	D (SOIC, 8)	4.90mm × 3.91mm						
LMV342IDGK	DGK (VSSOP, 8)	3.00mm × 3.00mm						
LMV344ID	D (SOIC, 14)	8.65mm × 3.91mm						
LMV344IPW	PW (TSSOP, 14)	5.00mm × 4.40mm						

For all available packages, see the orderable addendum at the end of the data sheet.



Sample-and-Hold Circuit



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4 Pin Configuration and Functions

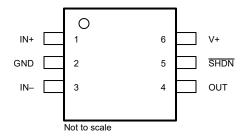


Figure 4-1. DBV or DCK Package, 6-Pin SOT-23 or SC70 (Top View)

Table 4-1. Pin Functions: LMV341

PIN		I/O	DESCRIPTION
NAME	SOT-23, SC70	1/0	DESCRIPTION
IN+	1	I	Noninverting input on channel 1
IN-	3	I	Inverting input on channel 1
OUT	4	0	Output on channel 1
GND	2	_	Ground
SHDN	5	I	Shutdown active low
V ₊	6	_	Positive power supply

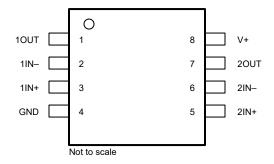


Figure 4-2. D or DGK Package, 8-Pin SOIC or VSSOP (Top View)

Table 4-2. Pin Functions: LMV342

PIN		I/O	DESCRIPTION			
NAME	SOIC, VSSOP	1/0	DESCRIPTION			
1IN+	3	I	Noninverting input on channel 1			
1IN-	2	I	nverting input on channel 1			
10UT	1	0	Output on channel 1			
2IN+	5	I	Noninverting input on channel 2			
2IN-	6	I	Inverting input on channel 2			
2OUT	7	0	Output on channel 2			
GND	4	_	Ground			
V ₊	8	_	Positive power supply			



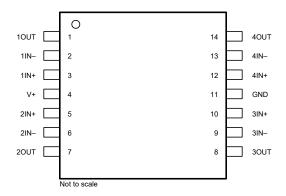


Figure 4-3. D or PW Package, 14-Pin SOIC or TSSOP (Top View)

Table 4-3. Pin Functions: LMV344

	PIN	1/0	DECORIDATION				
NAME	SOIC, TSSOP	I/O	DESCRIPTION				
1IN+	3	I	Noninverting input on channel 1				
1IN-	2	I	I Inverting input on channel 1				
10UT	1	0	Output on channel 1				
2IN+	5	I	I Noninverting input on channel 2				
2IN-	6	I	Inverting input on channel 2				
2OUT	7	0	Output on channel 2				
3IN+	10	I	Noninverting input on channel 3				
3IN-	9	I	Inverting input on channel 3				
3OUT	8	0	Output on channel 3				
4IN+	12	I	Noninverting input on channel 4				
4IN-	13	I	Inverting input on channel 4				
4OUT	14	0	Output on channel 4				
GND	11	_	Ground				
V ₊	4	_	Positive power supply				

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V ₊	Supply voltage ⁽²⁾	-0.3	5.5	V
V _{ID}	Differential input voltage ⁽³⁾		±5.5	V
VI	Input voltage (either input)	-0.3	5.5	V
Vo	Output voltage	-0.3	V _{CC} + 0.3	V
TJ	Operating virtual junction temperature		150	°C
T _{stg}	Storage temperature	-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

- (2) All voltage values (except differential voltages) are with respect to the network GND.
- (3) Differential voltages are at IN+ with respect to IN-.

5.2 ESD Ratings

			VALUE	UNIT
V	Electrostatic	trostatic Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾		V
V _(ESD)	discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±750	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V ₊	Supply voltage (single-supply operation)	2.5	5.5	V
T _A	Operating free-air temperature	-40	125	°C

5.4 Thermal Information

			LMV344	LMV341		LMV342	LMV344	
THERMAL METRIC(1)		D (SOIC)		DBV (SOT-23)			PW (TSSOP)	UNIT
		8 PINS	14 PINS	6 PINS	6 PINS	8 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance ^{(2) (3)}	123.9	88.7	193.4	196.8	192.3	118	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	70.2	49	145.6	82.4	78.2	46.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.1	43	44.1	95.2	112.6	59.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	25	16.9	34.1	1.8	15.2	5.1	°C/W
ΨЈВ	Junction-to-board characterization parameter	63.6	42.7	43.4	93.2	111.2	59.1	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

⁽²⁾ Maximum power dissipation is a function of T_J(max), R_{θ,JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_J(max) – T_A)/R_{θ,JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.

⁽³⁾ The package thermal impedance is calculated in accordance with JESD 51-7.



5.5 Electrical Characteristics: V₊ = 2.7V

 $\rm V_{+}$ = 2.7V, GND = 0V, $\rm V_{IC}$ = $\rm V_{O}$ = $\rm V_{+}/2,~R_{L}$ > 1M Ω (unless otherwise noted)

	PARAMETER	TEST CONDI	TIONS	T _A	MIN	TYP ⁽¹⁾	MAX	UNIT
.,				25°C		0.25	4	.,
V_{IO}	Input offset voltage			Full range			4.5	mV
α_{VIO}	Average temperature coefficient of input offset voltage			Full range		1.7		μV/°C
				25°C		1	120	^
I _{IB}	Input bias current			-40°C to 85°C			250	рA
				-40°C to 125°C			3	nA
I _{IO}	Input offset current			25°C		6.6		fA
CMDD	Common mode rejection ratio	0 ≤ V _{ICR} ≤ 1.7V		25°C	56	80		٩D
CMRR	Common-mode rejection ratio	0 ≤ V _{ICR} ≤ 1.6V		Full range	50	-		dB
l.	Cumply voltage rejection ratio	271/21/251/		25°C	65	82		٩D
k _{SVR}	Supply-voltage rejection ratio	2.7V ≤ V ₊ ≤ 5V		Full range	60			dB
	Canada in makasakan nanan	Lower range, CMRR ≥ 50dB		25°C		-0.2	0	
V_{ICR}	Common-mode input voltage range	Upper range, CMRR	≥ 50dB	25°C	1.7	1.9		V
		D 401:0 to 4.051/		25°C	78	113		
^	1	$R_L = 10k\Omega$ to 1.35V		Full range	70			dB
A_V	Large-signal voltage gain ⁽²⁾	$R_L = 2k\Omega$ to 1.35V		25°C	72	103		
				Full range	64			
		$R_L = 2k\Omega$ to 1.35V		25°C		24	60	-
			Low level	Full range			95	
			High level	25°C		26	60	
.,	Output swing			Full range			95	mV
V _O	(delta from supply rails)	R _L = 10kΩ to 1.35V	Low level	25°C		5	30	
				Full range			40	
			High level	25°C		5.3	30	
				Full range			40	
	Complete assessment (non-all-ann-all)			25°C		150	200	
I _{CC}	Supply current (per channel)			Full range			230	μA
		Sourcing	LMV341, LMV342		20	32		
los	Output short-circuit current	_	LMV344	25°C	18	24		mA
		Sinking	'		15	24		
SR	Slew rate	$R_L = 10k\Omega^{(3)}$		25°C		1		V/µs
GBM	Unity-gain bandwidth	$R_L = 10k\Omega, C_L = 200p$	F	25°C		1		MHz
Φ _m	Phase margin	R _L = 100kΩ		25°C		72		0
G _m	Gain margin	$R_L = 100k\Omega$		25°C		20		dB
V _n	Equivalent input noise voltage	f = 1kHz		25°C		40		nV/√ $\overline{\text{Hz}}$
In	Equivalent input noise current	f = 1kHz		25°C		0.001		pA/√ Hz
THD	Total harmonic distortion	$f = 1kHz$, $A_V = 1$, $R_L = 600Ω$, $V_I = 1$ V_{PF})	25°C		0.017%		

Typical values represent the most likely parametric norm.

Product Folder Links: LMV341 LMV342 LMV344

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GND + $0.2V \le V_0 \le V_+ - 0.2V$ (2)

Connected as voltage follower with 2V_{PP} step input. Number specified is the slower of the positive and negative slew rates.



5.6 Electrical Characteristics: V₊ = 5V

 V_{+} = 5V, GND = 0V, V_{IC} = V_{O} = $V_{+}/2,\,R_{L}$ > 1M Ω (unless otherwise noted)

	PARAMETER	TEST COND	TIONS	TA	MIN	TYP ⁽¹⁾	MAX	UNIT
\/	Input offeet volter:			25°C		0.25	4	mc\ /
V _{IO}	Input offset voltage			Full range			4.5	mV
α _{VIO}	Average temperature coefficient of input offset voltage			Full range		1.9		μV/°C
				25°C		1	200	^
I _{IB}	Input bias current			-40°C to 85°C			375	рA
				-40°C to 125°C			5	nA
I _{IO}	Input offset current			25°C		6.6		fA
CMDD	Common mode rejection ratio	0 ≤ V _{ICR} ≤ 4V		25°C	56	86		4D
CMRR	Common-mode rejection ratio	0 ≤ V _{ICR} ≤ 3.9V		Full range	50			dB
l,	Cumply voltage rejection ratio	271/21/251/		25°C	65	82		٩D
k _{SVR}	Supply-voltage rejection ratio	2.7V ≤ V ₊ ≤ 5V		Full range	60			dB
\/	Common-mode input	Lower range, CMRR ≥ 50dB		25°C		-0.2	0	V
V_{ICR}	voltage range	Upper range, CMRR	≥ 50dB	25°C	4	4.2		V
		D = 40k0 to 0.5V		25°C	78	116		
۸	Lama simal valtara main(2)	$R_L = 10k\Omega$ to 2.5V		Full range	70			- dB
A_V	Large-signal voltage gain ⁽²⁾	$R_L = 2k\Omega$ to 2.5V		25°C	72	107		
				Full range	64			
	Output swing	$R_L = 2k\Omega$ to 2.5V	111	25°C		32	60	
			Low level	Full range			95	mV
			High level	25°C		34	60	
				Full range			95	
V _O	(delta from supply rails)	$R_L = 10k\Omega$ to 2.5V	Low level	25°C		7	30	
				Full range			40	
			High level	25°C		7	30	
				Full range			40	
	Complete support (non-shape all)			25°C		150	200	
I _{CC}	Supply current (per channel)			Full range			260	μA
		Sourcing	LMV341, LMV342		85	113		
los	Output short-circuit current		LMV344	25°C	85	113		mA
		Sinking			50	75		
SR	Slew rate	$R_L = 10k\Omega^{(3)}$		25°C		1		V/µs
GBM	Unity-gain bandwidth	$R_L = 10k\Omega, C_L = 200p$	oF	25°C		1		MHz
Φ _m	Phase margin	$R_L = 100k\Omega$		25°C		70		0
G _m	Gain margin	$R_L = 100k\Omega$		25°C		20		dB
V _n	Equivalent input noise voltage	f = 1kHz		25°C		39		nV/√ Hz
I _n	Equivalent input noise current	f = 1kHz		25°C		0.001		pA/√ Hz
THD	Total harmonic distortion	$f = 1kHz, A_V = 1,$ $R_L = 600Ω, V_I = 1 V_P$	P	25°C		0.012%		

⁽¹⁾ Typical values represent the most likely parametric norm.

⁽²⁾ GND + $0.2V \le V_O \le V_+ - 0.2V$

³⁾ Connected as voltage follower with 2V_{PP} step input. Number specified is the slower of the positive and negative slew rates.



5.7 Shutdown Characteristics: V₊ = 2.7V

 V_{+} = 2.7V, GND = 0V, V_{IC} = V_{O} = $V_{+}/2$, R_{L} > 1M Ω (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
I _{CC(SHDN)}	Supply current in shutdown mode	V _{SD} = 0V	25°C		0.045	1000	nA
	Supply current in shutdown mode	V _{SD} - UV	Full range			1.5	μA
t _(on)	Amplifier turnon time		25°C		5		μs
V _{SD}	Personmended shutdown pin voltage range	ON mode	25°C	2.4		2.7	
	Recommended shutdown pin voltage range	Shutdown mode	25 C	0		0.2	V

5.8 Shutdown Characteristics: $V_+ = 5V$

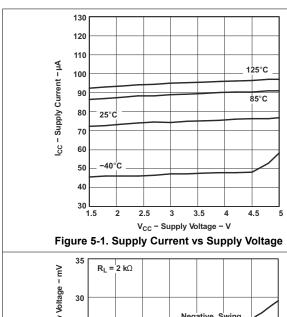
 V_{+} = 5V, GND = 0V, V_{IC} = V_{O} = $V_{+}/2$, R_{L} > 1M Ω (unless otherwise noted)

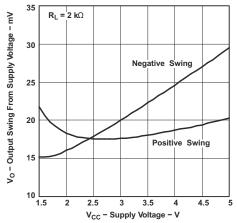
	PARAMETER	TEST CONDITIONS T _A		MIN	TYP	MAX	UNIT	
I _{CC(SHDN)}	Supply current in shutdown mode	\/ - 0\/	25°C		0.033	1	1	
	Supply current in shutdown mode	$V_{SD} = 0V$	Full range			1.5	μA	
t _(on)	Amplifier turnon time		25°C		5		μs	
V _{SD}	Pagammandad shutdawa pin yaltaga ranga	ON mode	25°C	4.5		5	\/	
	Recommended shutdown pin voltage range	Shutdown mode	23 0	0		0.2	· '	

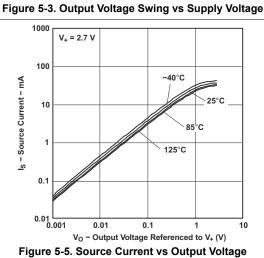
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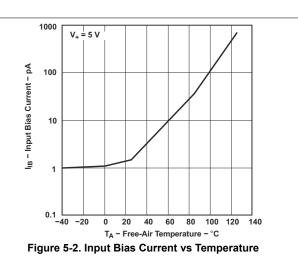


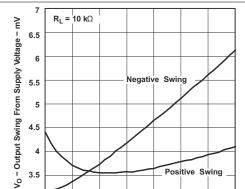
5.9 Typical Characteristics













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4.5

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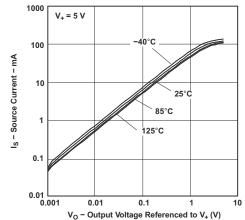
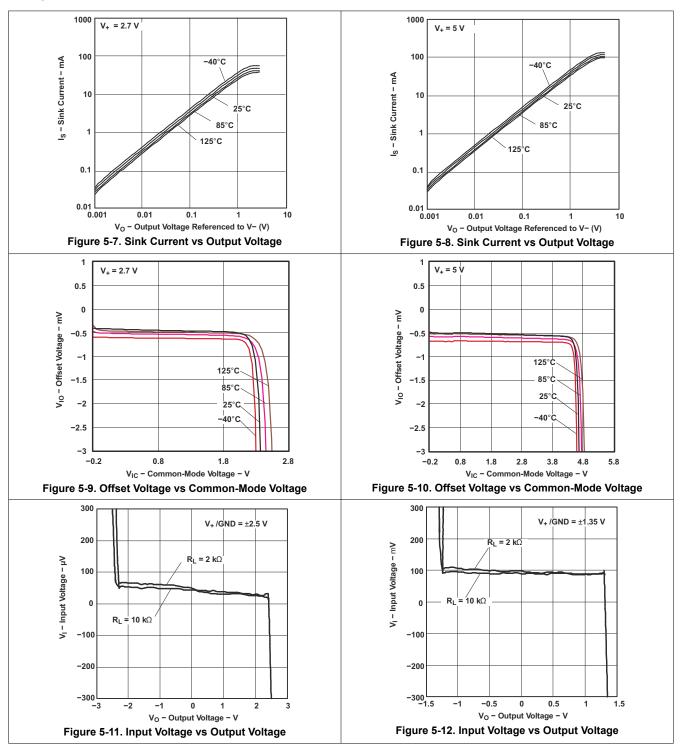
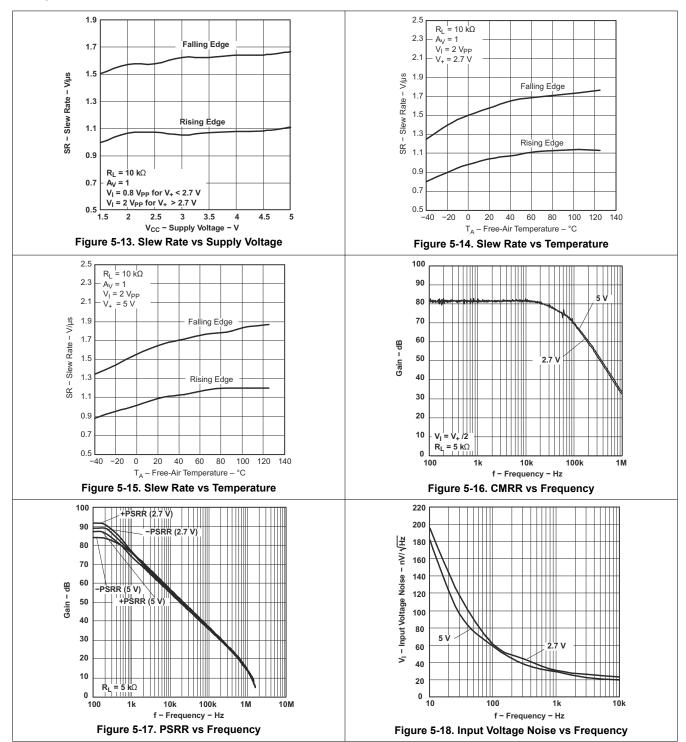


Figure 5-6. Source Current vs Output Voltage











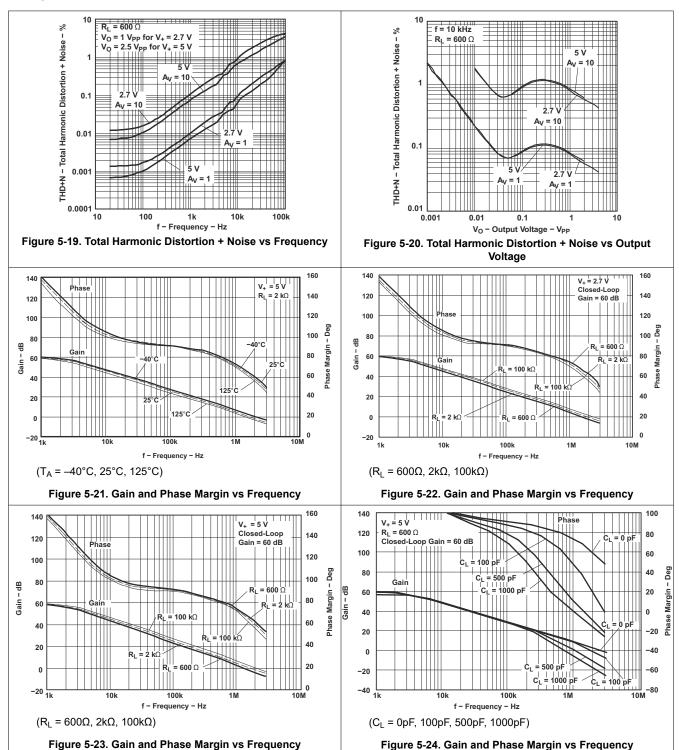
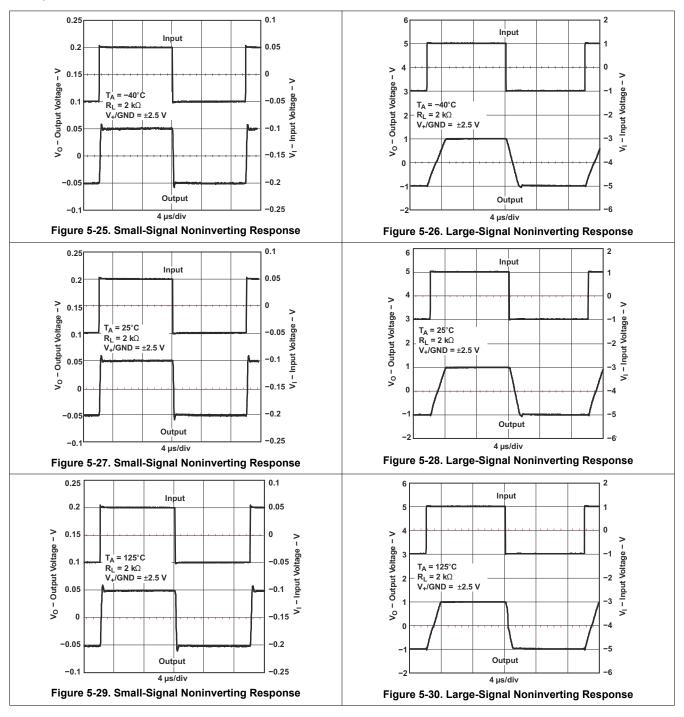
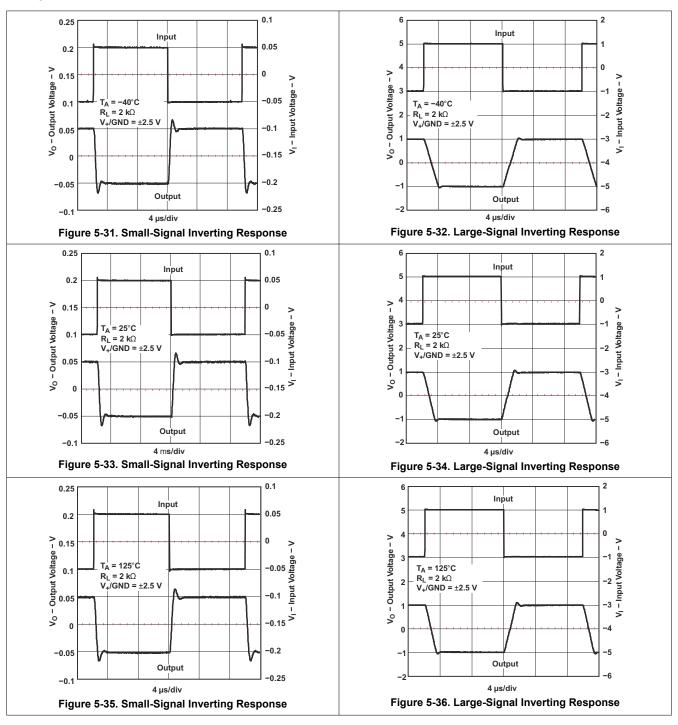


Figure 5-24. Gain and Phase Margin vs Frequency









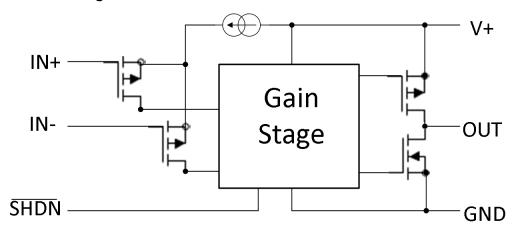


6 Detailed Description

6.1 Overview

The LMV34x devices are precision operational amplifiers with CMOS inputs for very low input bias current. Output is rail-to-rail and input common-mode includes ground. LMV341 has a shutdown mode for very low supply current.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 PMOS Input Stage

PMOS Input Stage supports a lower input range that includes ground. Upper range limit is $V_+ - 1V$.

6.3.2 CMOS Output Stage

The CMOS drain output topology allows rail-to-rail output swing.

6.3.3 Shutdown

LMV341 includes a shutdown pin. During shutdown, I_{CC} is nearly zero and the output becomes high impedance. The typical turnon time coming out of shutdown is $5\mu s$.

6.4 Device Functional Modes

The LMV34x devices have two modes of operation:

- Normal operation when SHDN pin is at V₊ level or the SHDN pin is not present
- Shutdown mode when SHDN is at GND level; I_{CC} is very low and output is high impedance.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

LMV34x devices have rail-to-rail output and input range from ground to VCC - 1V. CMOS inputs provide very low input current. Shutdown capability is an option in dual amplifier version. Operation from 2.5V to 5.5V is possible.

7.2 Typical Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

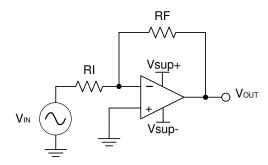


Figure 7-1. Application Schematic

7.2.1 Design Requirements

The supply voltage must be larger than the input voltage range and output range. For instance, this application scales a signal of ± 0.5 V to ± 1.8 V. Setting the supply at ± 2 V is sufficient to accommodate this application. The supplies can power up in any order; however, neither supply can be of opposite polarity relative to ground at any time; otherwise, a large current can flow though the input ESD diodes. To limit current in such an occurrence, TI highly recommends adding a series resistor to the grounded input. Vsup+ must be more positive than Vsup- at all times; otherwise, a large reverse supply current can flow.

7.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using Equation 1 and Equation 2.

$$A_{V} = \frac{VOUT}{VIN}$$
 (1)

$$A_{V} = \frac{1.8}{-0.5} = -3.6 \tag{2}$$

Once the desired gain is determined, choose a value for RI or RF. Choosing a value in the $k\Omega$ range is desirable because the amplifier circuit uses currents in the mA range. This makes sure the part does not draw too much current. For this example, choose $10k\Omega$ for RI, which means $36k\Omega$ is used for RF. This is determined by Equation 3.

$$A_{V} = -\frac{RF}{RI}$$
 (3)



7.2.3 Application Curve

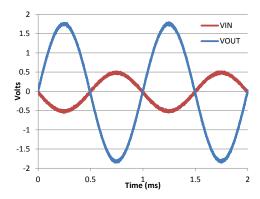


Figure 7-2. Input and Output Voltages of the Inverting Amplifier

8 Power Supply Recommendations

CAUTION

Supply voltages larger than 5.5V for a single supply can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

9 Layout

9.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the
 operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance
 power sources local to the analog circuitry.
 - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V₊ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, and pay attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Examples*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.



9.2 Layout Examples

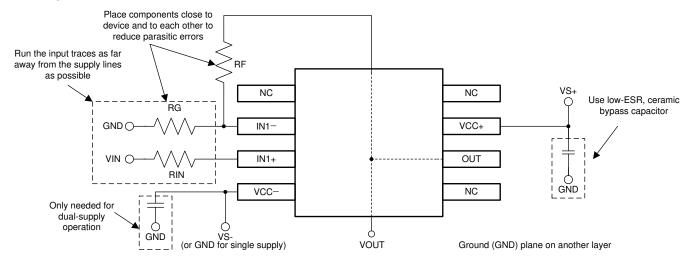


Figure 9-1. Operational Amplifier Layout for Noninverting Configuration

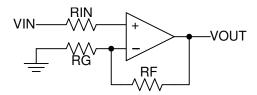


Figure 9-2. Operational Amplifier Schematic for Noninverting Configuration



10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on Notifications to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

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10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (May 2016) to Revision J (June 2025) Changed supply current per channel specification at V+ = 2.7V from 100µA to 150µA (typical) and from 170μA to 200μA (maximum at 25°C).......6 Changed supply current per channel specification at V+ = 5V from 100µA to 150µA (typical)......7 Changed recommended shutdown pin voltage range, shutdown mode specification at V+ = 2.7V from 0.8V to Changed recommended shutdown pin voltage range, shutdown mode specification at V+ = 5V from 0.8V to

Changes from Revision H (June 2012) to Revision I (May 2016) Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and

Page

Implementation section, Power Supply Recommendations section, Layout section, Device and

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
LMV341IDBVR	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(RC9A, RC9E, RC9S)
LMV341IDBVR.A	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(RC9A, RC9E, RC9S)
LMV341IDBVRE4	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	
LMV341IDBVRG4	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	
LMV341IDCKR	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	(R4A, R4E)
LMV341IDCKR.A	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	(R4A, R4E)
LMV341IDCKRG4	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R4A, R4E)
LMV341IDCKRG4.A	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R4A, R4E)
LMV342ID	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 125	MV342I
LMV342IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RPA
LMV342IDGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RPA
LMV342IDGKRG4	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	-	Call TI	Call TI	-40 to 125	
LMV342IDGKT	Preview	Production	VSSOP (DGK) 8	250 SMALL T&R	-	Call TI	Call TI	-40 to 125	
LMV342IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV342I
LMV342IDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV342I
LMV342IDRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	-	Call TI	Call TI	-40 to 125	
LMV344ID	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 125	LMV344I
LMV344IDR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV344I
LMV344IDR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV344I
LMV344IPW	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 125	MV344I
LMV344IPWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV344I
LMV344IPWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV344I
LMV344IPWRG4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	-	Call TI	Call TI	-40 to 125	

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

PACKAGE OPTION ADDENDUM

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- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF LMV341, LMV344:

Automotive: LMV341-Q1, LMV344-Q1

NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV341IDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
LMV341IDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
LMV341IDCKRG4	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
LMV342IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
LMV342IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV344IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV344IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LMV344IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV341IDBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
LMV341IDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
LMV341IDCKRG4	SC70	DCK	6	3000	202.0	201.0	28.0
LMV342IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LMV342IDR	SOIC	D	8	2500	353.0	353.0	32.0
LMV344IDR	SOIC	D	14	2500	353.0	353.0	32.0
LMV344IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
LMV344IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0





NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

- 4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- 5. Refernce JEDEC MO-178.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







NOTES:

PowerPAD is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-187.





NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
- 9. Size of metal pad may vary due to creepage requirement.





NOTES: (continued)

- 11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 12. Board assembly site may have different recommendations for stencil design.







NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

 4. Falls within JEDEC MO-203 variation AB.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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Last updated 10/2025