TEXAS INSTRUMENTS
LMR43606-Q1
SNVSCM5 – JANUARY 2024

LMR43606-Q1, 36V, 0.6A, Automotive Buck Converter With < 2.5µA I_Q at 150°C T_{JMAX} in 4mm² HotRod™ QFN

1 Features

- AEC-Q100-qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Greater than 85% efficiency at 1mA
- Miniature design size and low component cost
  - 2mm × 2mm HotRod™ package with wettable flanks
  - Internal compensation
- Designed for ultra-low EMI requirements
  - Spread spectrum reduces peak emissions
  - Pin selectable FPWM mode for constant frequency at light loads with MODE/SYNC pin
  - F_{SW} synchronization with MODE/SYNC pin
- Designed for automotive applications
  - –40°C to +150°C junction temperature range
  - Supports 42V automotive load dump
  - Supports 3-V_{IN} for automotive cold crank
  - Adjustable up to 95% of V_{IN}, 3.3V and 5V fixed V_{OUT} options available
- Designed for scalable power supplies
  - Adjustable F_{SW}: 200kHz to 2.2MHz (RT pin)
  - Pin compatible with:
    - LMR43610-Q1 (36V, 1A)
    - LMR36506-Q1 (65V, 600mA)
    - LMR36503-Q1 (65V, 300mA)

2 Applications

- Advanced driver assistance systems: radar ECU
- Infotainment and cluster: head unit, eCall
- Body electronics and lighting

3 Description

The LMR43606-Q1 is a small, 36V, 0.6A, synchronous step-down DC/DC converter in a 2mm × 2mm HotRod package. This easy-to-use converter supports a wide input voltage range of 3.0V to 36V with transients up to 42V.

The LMR43606-Q1 is specifically designed to meet low standby power requirements for always on, automotive applications. Auto mode enables frequency foldback when operating at light loads, allowing an unloaded current consumption of 1.5µA at 13.5V_{IN} and high light load efficiency. A seamless transition between PWM and PFM modes along with very low MOSFET ON resistances provide exceptional efficiency across the entire load range.

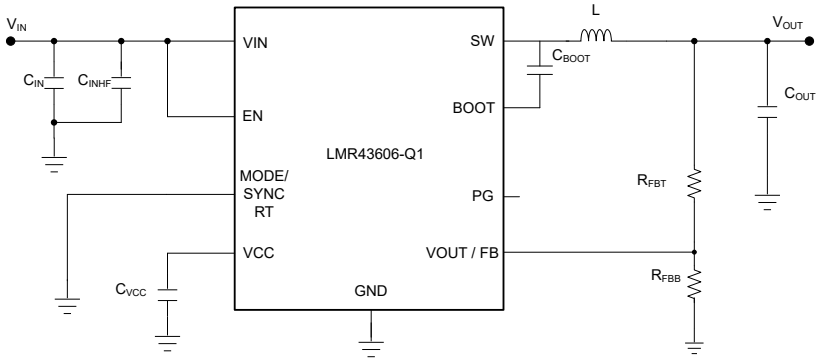
The control architecture and feature-set are designed for an ultra-small design size. The device uses peak current mode control to minimize output capacitance. The LMR43606-Q1 minimizes input filter size by using dual random spread spectrum, a low-EMI HotRod package, and an optimized pinout. The MODE/SYNC and RT pin variants can be used to set or synchronize the frequency between 200kHz and 2.2MHz to avoid noise sensitive frequency bands.

The rich feature set of the LMR43606-Q1 is designed to simplify implementation for a wide range of automotive end equipments.

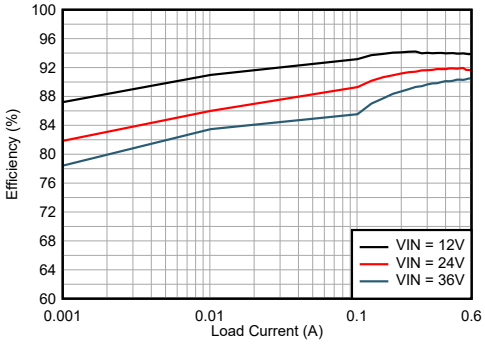
Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE(2)
LMR43606-Q1	RPE (VQFN-HR, 9)	2.00mm × 2.00mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic



Efficiency: V_{OUT} = 5V (Fixed), 400kHz

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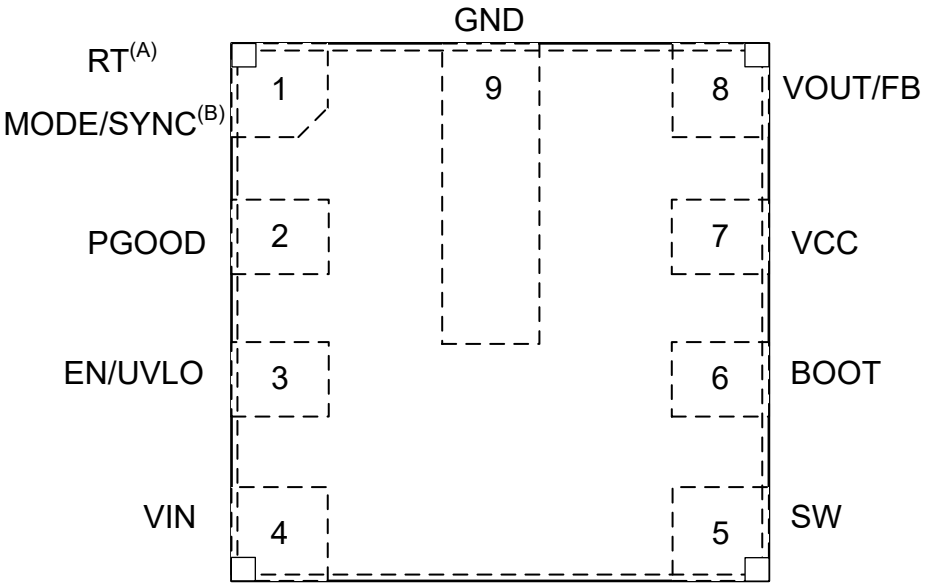
4 Device Comparison Table

ORDERABLE PART NUMBER (1)	OUTPUT CURRENT	OUTPUT VOLTAGE	EXTERNAL SYNC	F_{SW}	SPREAD SPECTRUM
LMR43606MSC3RPERQ1	0.6A	3.3V fixed / adjustable	Yes (PFM/FPWM selectable)	Fixed 2.2MHz	Yes
LMR43606MSC5RPERQ1	0.6A	5V fixed / adjustable	Yes (PFM/FPWM selectable)	Fixed 2.2MHz	Yes
LMR43606RS3RPERQ1	0.6A	3.3V fixed / adjustable	No (default PFM at light load)	Adjustable with RT resistor	Yes
LMR43606RS5RPERQ1	0.6A	5V fixed / adjustable	No (default PFM at light load)	Adjustable with RT resistor	Yes

(1) For more information on device orderable part numbers, see *Device Nomenclature*.

5 Pin Configuration and Functions



A. See Section 4 for more details. Pin 1 is factory-set for externally adjustable switching frequency RT variants only.
B. Pin 1 factory-set for fixed switching frequency MODE/SYNC variants only.

Figure 5-1. 9-Pin (2mm × 2mm) VQFN-HR RPE Package (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	RT or MODE/SYNC	A	For the RT variant, the switching frequency can be adjusted from 200kHz to 2.2MHz. For the MODE/SYNC variant, the switching frequency can operate in user-selectable PFM/FPWM mode and can be synchronized to an external clock. *Do not float this pin.*
2	PGOOD	A	Open-drain power-good flag output. Connect to a suitable voltage supply through a current limiting resistor. High = power OK, low = power bad. This pin goes low when EN = low. This pin can be open or grounded when not used.
3	EN/UVLO	A	Enable input to regulator. High = ON, low = OFF. Can be connected directly to VIN. *Do not float this pin.*
4	VIN	P	Input supply to regulator. Connect a high-quality bypass capacitor or capacitors directly to this pin and GND.
5	SW	P	Regulator switch node. Connect to power inductor.
6	BOOT	P	Bootstrap supply voltage for internal high-side driver. Connect a high-quality 100nF capacitor from this pin to the SW pin.
7	VCC	P	Internal LDO output. Used as supply to internal control circuits. Do not connect to external loads. Can be used as logic supply for power-good flag. Connect a high-quality 1µF capacitor from this pin to GND.
8	VOUT/FB	A	Fixed output options and adjustable output options are available with the VOUT/FB pin variant. Connect to the output voltage node for fixed VOUT. Connect to tap point of feedback voltage divider for adjustable VOUT. See Section 8.2.2.2.1 for how to select feedback resistor divider values. Check Section 4 for more details. *Do not float this pin.*
9	GND	G	Power ground terminal. Connect to system ground. Connect to C_{IN} with short, wide traces.
A = Analog, P = Power, G = Ground			

6 Specifications

6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range (1)

PARAMETER		MIN	MAX	UNIT
Voltages	VIN to GND	–0.3	42	V
Voltages	SW to GND	–0.3	V_{IN} + 0.3	V
Voltages	BOOT to SW	–0.3	5.5	V
Voltages	VCC to GND	–0.3	5.5	V
Voltages	VOUT/FB to GND	–0.3	16	V
Voltages	SYNC/MODE or RT to GND	–0.3	5.5	V
Voltages	PGOOD to GND	–0.3	20	V
Voltages	EN to GND	–0.3	42	V
Temperature	T_J, Junction temperature	–40	150	°C
Temperature	T_{stg}, Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002, HBD ESD Classification Level 2 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD clasiffication Level C5	±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage range for start-up	3.6	36	V
	Input voltage range after start-up	3.0	36	V
V_{OUT}	Output voltage range with adjustable output voltage setup	1	0.95 × VIN	V
I_{OUT}	LMR43606-Q1 continuous DC output current range	0	0.6	A
T_J	Operating junction temperature	–40	150	°C

6.4 Thermal Information

The value of $R_{\theta JA}$ in this table is only valid for comparison with other packages. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For example, a 4-layer PCB can achieve a $R_{\theta JA}$= 50°C/W.

THERMAL METRIC (1)		LMR43606-Q1 RPE (VQFN-HR) 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance for LMR43606MQ3EVM-2M	50	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise noted. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
V_{INMIN}	Input voltage rising threshold for start-up	Before start-up	3.2	3.35	3.5	V
	Input voltage falling threshold	Once operating	2.45	2.7	3	V
$I_{SD(VIN)}$	Shutdown quiescent current at VIN pin	EN = 0V		0.25	1	µA
$I_{QVIN(nonsw)}$	Non-switching input current; measured at VIN pin (1)	Fixed 5.0V V_{OUT}, $V_{VOUT/FB}$ = 5.25V		1.6	3	µA
$I_{QVIN(nonsw)}$	Non-switching input current; measured at VIN pin (1)	Fixed 3.3V V_{OUT}, $V_{VOUT/FB}$ = 3.47V		1.2	2.2	µA
ENABLE (EN PIN)						
$V_{EN-WAKE}$	EN wakeup threshold		0.5	0.7	1	V
$V_{EN-VOUT}$	Precision enable rising threshold for V_{OUT}		1.16	1.23	1.3	V
$V_{EN-HYST}$	Enable hysteresis below $V_{EN-VOUT}$		0.3	0.35	0.4	V
I_{LKG-EN}	Enable pin input leakage current	V_{EN} = V_{IN} = 13.5V		10		nA
INTERNAL LDO (VCC PIN)						
V_{CC}	VCC pin output voltage	V_{FB} = 0V, I_{VCC} = 1mA	3.1	3.3	3.45	V
VOLTAGE FEEDBACK (VOUT/FB PIN)						
V_{OUT}	Output voltage accuracy for fixed V_{OUT}	3.3V V_{OUT}, V_{IN} = 3.6V to 36V, FPWM mode	3.27	3.3	3.33	V
V_{OUT}	Output voltage accuracy for fixed V_{OUT}	5V V_{OUT}, V_{IN} = 5.5V to 36V, FPWM mode	4.94	5.00	5.06	V
V_{FB}	Internal reference voltage accuracy	V_{OUT} = 1V, V_{IN} = 3.0V to 36V, FPWM mode	0.99	1.00	1.01	V
$I_{FB(LKG)}$	FB input current	Adjustable configuration, FB = 1V		10		nA
CURRENT LIMITS						
$I_{PEAKMAX}$	High-side peak current limit	LMR43606-Q1	1.25	1.4	1.55	A
I_{VALMAX}	Low-side valley current limit	LMR43606-Q1	0.75	1	1.25	A
$I_{PEAKMIN}$	Minimum peak current limit	LMR43606-Q1, Auto mode	0.17	0.27	0.37	A
I_{NEGMIN}	Low-side valley current negative limit	LMR43606-Q1, FPWM mode	-0.9	-0.7	-0.5	A
I_{ZC}	Zero-cross current limit	Auto mode	30	80	135	mA
POWER GOOD (PGOOD PIN)						
PGD_{OV}	PGOOD upper threshold - rising	% of VOUT/FB (fixed or adj. output)	104	108	111	%

Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise noted. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PGD_{UV}	PGOOD upper threshold - falling	% of VOUT/FB (fixed or adj. output)	89	91	94.2	%
PGD_{HYST}	PGOOD recovery hysteresis for OV	% of VOUT/FB target regulation voltage	2	2.4	2.8	%
	PGOOD recovery hysteresis for UV	% of VOUT/FB target regulation voltage	1.1	3.3	5.9	%
$V_{PGD-VAL}$	Minimum V_{IN} for PGOOD function	V_{EN} = 0V, R_{PGD_PU} = 10kΩ			1.5	V
R_{PGD}	PGOOD ON resistance	V_{EN} = 3.3V, 200µA pullup current			100	Ω
R_{PGD}	PGOOD ON resistance	V_{EN} = 0V, 200µA pullup current			100	Ω
t_{RESET_FILTER}	PGOOD deglitch delay at falling edge		25	40	75	µs
t_{PGOOD_ACT}	Delay time to PGOOD high signal		1.35	2.5	4	ms
SOFT START						
t_{SS}	Time from first SW pulse to VOUT/FB at 90% of set point.		2	3.5	4.6	ms
t_{HICCUP}	Time in hiccup before retry soft start		30	50	75	ms
OSCILLATOR (SYNC/MODE PIN)						
t_{PULSE_H}	High duration needed to be recognized as a pulse		100			ns
t_{PULSE_L}	Low duration needed to be recognized as a pulse		100			ns
t_{SYNC}	High/Low level pulse maximum duration to be recognized as a valid clock signal				6	µs
t_{MODE}	Time at one level needed to indicate FPWM or Auto Mode		12.5			µs
f_{SYNC}	Frequency SYNC range		0.2		2.5	MHz
V_{MODE_L}	SYNC/MODE input voltage low level threshold				1	V
V_{MODE_H}	SYNC/MODE input voltage high level threshold		1.6			V
OSCILLATOR (RT PIN)						
$F_{SW(1MHz)}$	Switching frequency with Internal fixed 1 MHz setting	RT pin tie to V_{CC}	900	1000	1070	kHz
$F_{SW(2p2MHz)}$	Switching frequency with fixed 2.2 MHz	RT pin tied to GND	2100	2200	2300	kHz
$F_{SW(Adj)}$	Accuracy of external frequency, 400 kHz	R_{RT} = 39.2kΩ 0.1% resistor	340	400	460	kHz
SPREAD SPECTRUM						
DeltaFc	Frequency increase/decrease from spread spectrum of internal oscillator	DRSS		±4		%
SWITCH NODE						
t_{ON-MIN}	Minimum HS switch on-time	FPWM mode I_{OUT} = 1A, 2.2MHz fixed		65	75	ns
$t_{OFF-MIN}$	Minimum HS switch off-time			60	85	ns
t_{ON-MAX}	Maximum HS switch on-time	HS timeout in dropout	6	9	13	µs
POWER STAGE						
V_{BOOT_UVLO}	Voltage on BOOT pin compared to SW which will turnoff high-side switch			2.1		V
$R_{DSON-HS}$	High-side MOSFET on-resistance	Load = 1A		132	260	mΩ
$R_{DSON-LS}$	Low-side MOSFET on-resistance	Load = 1A		75	140	mΩ

(1) This is the current used by the device open loop. It does not represent the total input current of the system when in regulation.

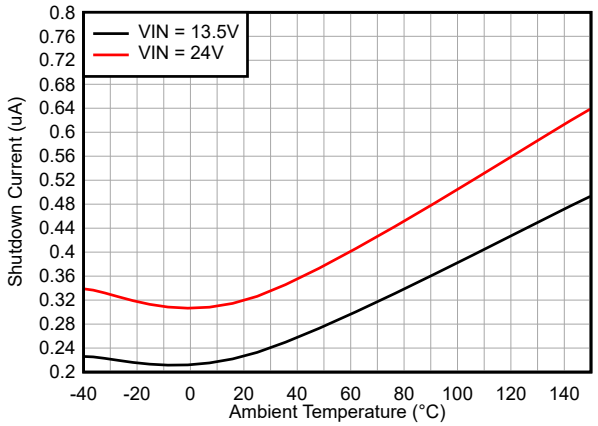
6.6 System Characteristics

The following specifications apply only to the typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40°C to 150°C. These specifications are not ensured by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{QVIN}	Input current to V_{IN}	V_{IN} = 13.5V, Fixed 3.3V V_{OUT}, I_{OUT} = 0A, Auto mode		1.5		µA
		V_{IN} = 13.5V, Fixed 5V V_{OUT}, I_{OUT} = 0A, Auto mode		2		µA
POWER STAGE						
V_{DROP1}	Input to output voltage differential to maintain V_{OUT} regulation ≥ 95%, with frequency foldback	V_{OUT} = 3.3V, fixed 2.2MHz, I_{OUT} = 0.6A		0.2		V
		V_{OUT} = 5V, fixed 2.2MHz, I_{OUT} = 0.6A		0.2		V
V_{DROP2}	Input to output voltage differential to maintain V_{OUT} regulation ≥ 95% and F_{SW} ≥ 1.85MHz	V_{OUT} = 3.3V, fixed 2.2MHz, I_{OUT} = 0.6A		0.7		V
	Input to output voltage differential to maintain V_{OUT} regulation ≥ 95% and F_{SW} ≥ 1.85MHz	V_{OUT} = 5V, fixed 2.2MHz trim, I_{OUT} = 0.6A		0.9		V
D_{MAX}	Maximum switch duty cycle	V_{OUT} =5V, while in frequency fold-back, I_{OUT} = 0.6A		98		%
		F_{sw} = 1.85MHz, V_{OUT} = 5.0V, I_{OUT} = 0.6A		87		%
$R_{FBPARA(min)}$	Minimum value of the parallel feedback resistors: R_{FBT}//R_{FBB}			5		kΩ
PROTECTION						
$T_{SD(trip)}$	Thermal shutdown temperature	Shutdown temperature	158	168	186	°C
$T_{SD(hyst)}$	Thermal shutdown temperature	Recovery temperature		15	20	°C

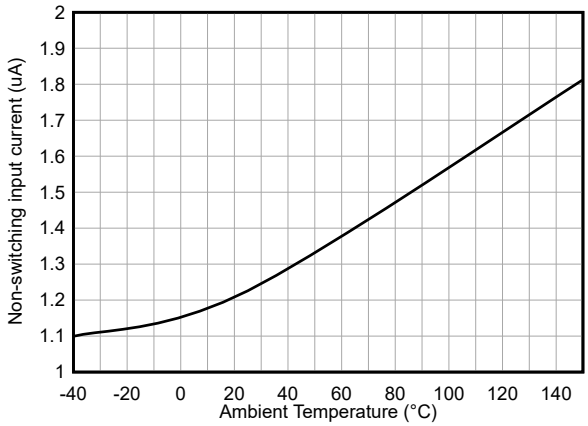
6.7 Typical Characteristics

Unless otherwise specified, the following conditions apply: T_A = 25°C, V_{IN} = 13.5V



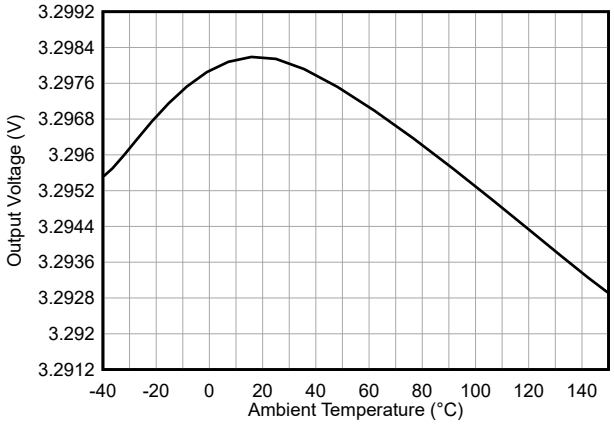
V_{OUT} = 3.3V fixed

Figure 6-1. Shutdown Current Versus Temperature



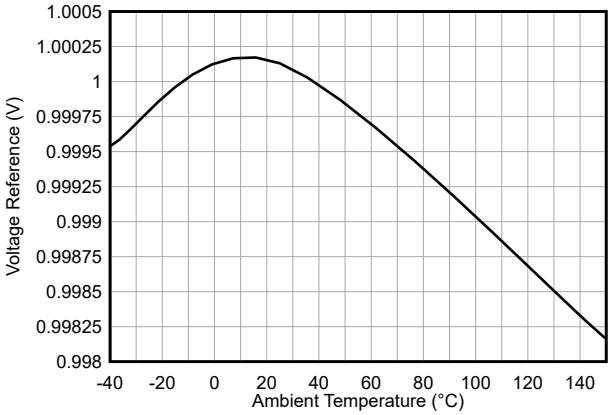
V_{OUT} = 3.3V fixed

Figure 6-2. Nonswitching Input Current ($I_{QVIN(nonsw)}$) Versus Temperature



V_{OUT} = 3.3V fixed

Figure 6-3. Output Voltage Accuracy Versus Temperature



V_{OUT} = adjustable

Figure 6-4. Feedback Voltage Accuracy Versus Temperature

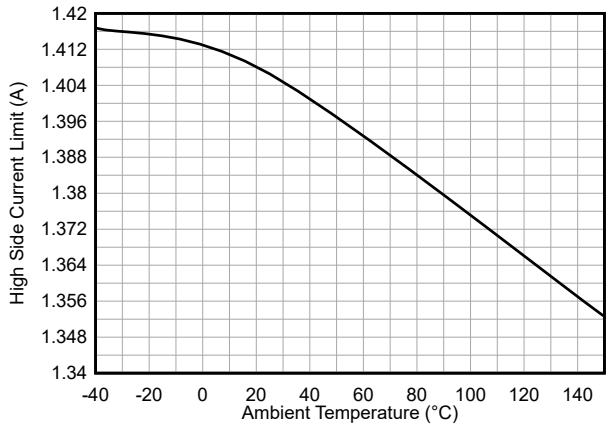


Figure 6-5. High Side MOSFET Current Limit Versus Temperature

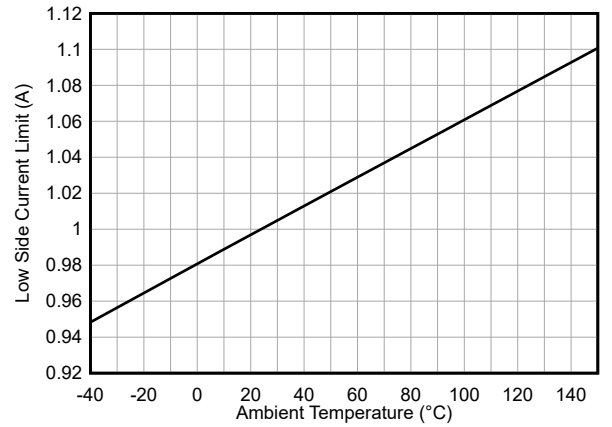


Figure 6-6. Low Side MOSFET Current Limit Versus Temperature

7 Detailed Description

7.1 Overview

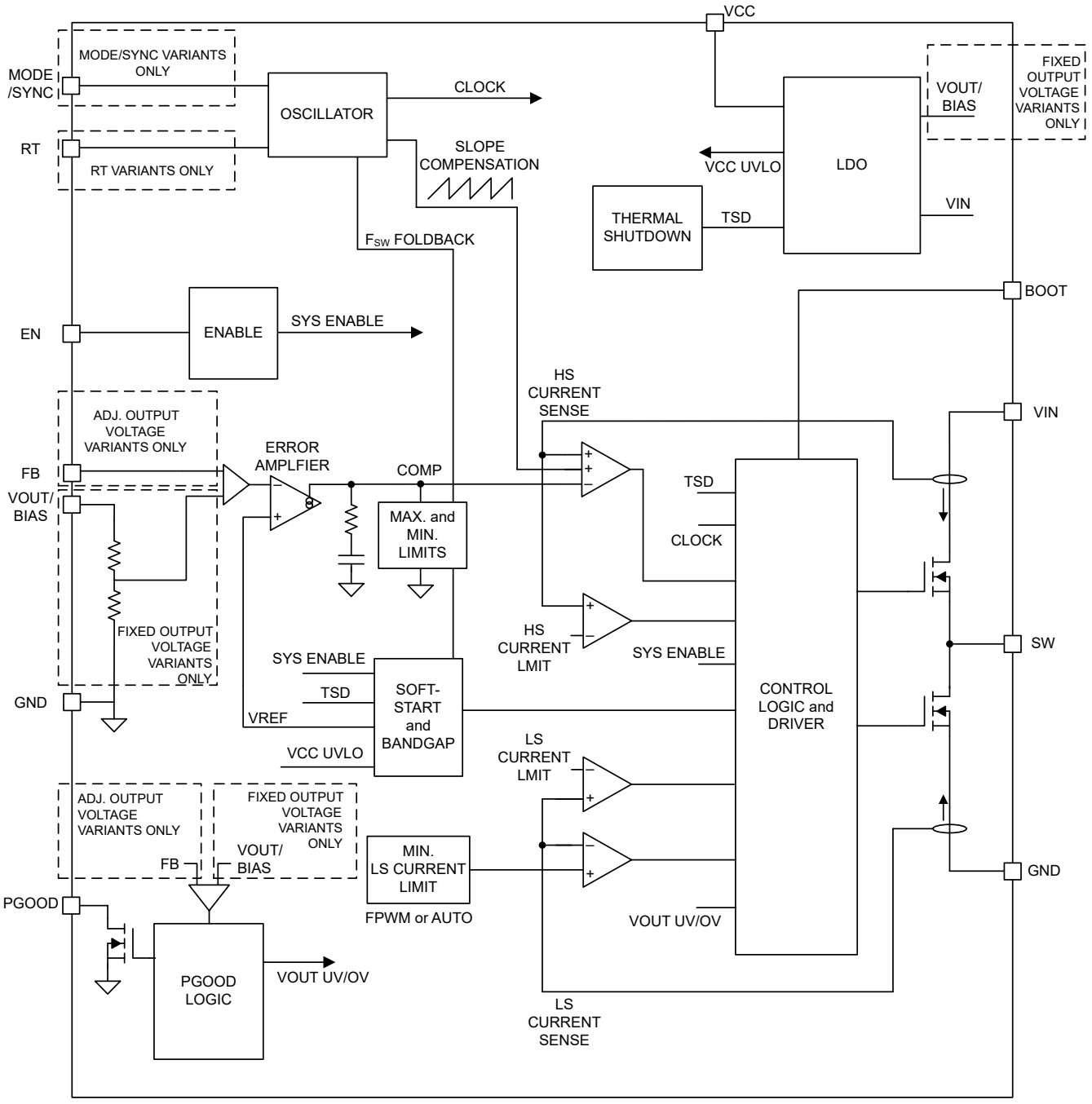
The LMR43606-Q1 is a wide input, low-quiescent current, high-performance regulator that can operate over a wide range of duty ratio and switching frequencies, including sub-AM band at 400kHz and above AM band at 2.2MHz. During wide input transients, if the minimum on time or the minimum off time cannot support the desired duty ratio at the higher switching frequency settings, the switching frequency is reduced automatically, allowing the LMR43606-Q1 to maintain the output voltage regulation. With an internally compensated design optimized for minimal output capacitors, the system design process with the LMR43606-Q1 is simplified significantly compared to other buck regulators available in the market.

The LMR43606-Q1 is designed to minimize external component cost and design size while operating in all demanding automotive environments. The LMR43606-Q1 family includes variants that can be set up to operate over a wide switching frequency range, from 200kHz to 2.2MHz, with the correct resistor selection from the RT pin to ground. To further reduce system cost, the PGOOD output feature with built-in delayed release allows the elimination of the reset supervisor in many applications.

The LMR43606-Q1-Q1 family is designed to reduce EMI/EMC emissions. The design includes a dual random spread spectrum switching frequency dithering scheme, has no bond-wire flip-chip on the lead (HotRod) package, and is available with the MODE/SYNC feature (select variants), allowing synchronization to an external clock, when available. Together, these features eliminate the need for any common-mode choke or shielding or any elaborate input filter design scheme, greatly reducing the complexity and cost of the EMI/EMC mitigation measures.

The LMR43606-Q1 comes in an ultra-small, 2mm × 2mm QFN package with wettable flanks, allowing for quick optical inspection along with specially designed corner anchor pins for reliable board level solder connections.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable, Start-Up, and Shutdown

Voltage at the EN pin controls the start-up or remote shutdown of the LMR43606-Q1 family of devices. The part stays shut down as long as the EN pin voltage is less than $V_{EN-WAKE}$ = 0.5V. During shutdown, the input current drawn by the device typically drops down to 0.25µA (V_{IN} = 13.5V). With the voltage at the EN pin greater than $V_{EN-WAKE}$, the device enters device standby mode and the internal LDO powers up to generate VCC. As the EN voltage increases further, approaching $V_{EN-VOUT}$, the device finally starts to switch, entering start-up mode with a soft start. During the device shutdown process, when the EN input voltage measures less than ($V_{EN-VOUT}$ – $V_{EN-HYST}$), the regulator stops switching and re-enters device standby mode. Any further decrease in the EN pin voltage, below $V_{EN-WAKE}$, and the device is then firmly shut down. The high-voltage compliant EN input pin can be connected directly to the V_{IN} input pin if remote precision control is not needed. The EN input pin must not be allowed to float. The various EN threshold parameters and their values are listed in Section 6.5. Figure 7-2 shows the precision enable behavior and shows a typical remote EN start-up waveform in an application. After the EN goes high, after a delay of about 1ms, the output voltage begins to rise with a soft start and reaches close to the final value in about 3.5ms (t_{ss}). After a delay of about 2.5ms (t_{PGOOD_ACT}), the PGOOD flag goes high. During start-up, the device is not allowed to enter FPWM mode until the soft-start time has elapsed. This time is measured from the rising edge of EN. Check Section 8.2.2.9 for component selection.

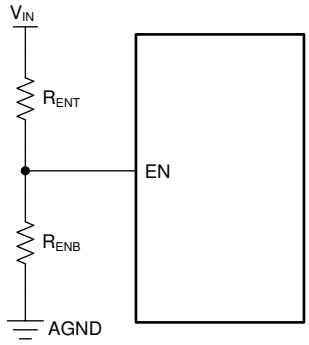


Figure 7-1. VIN UVLO Using the EN Pin

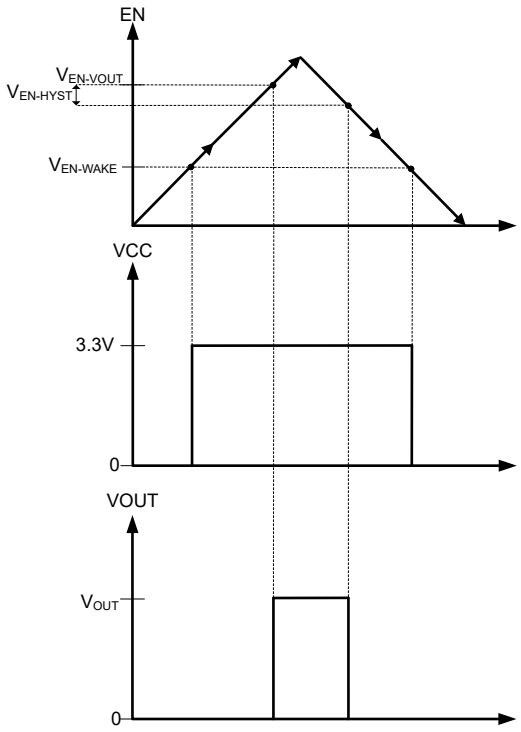


Figure 7-2. Precision Enable Behavior

7.3.2 External CLK SYNC (With MODE/SYNC)

Synchronizing the operation of multiple regulators in a single system, resulting in a well-defined system level performance is often desirable. The select variants in the LMR43606-Q1 with the MODE/SYNC pin allow the power designer to synchronize the device to a common external clock. The LMR43606-Q1 implements an in-phase locking scheme, where the rising edge of the clock signal, provided to the MODE/SYNC pin of the LMR43606-Q1, corresponds to the turning on of the high-side device. The external clock synchronization is implemented using a phase locked loop (PLL), eliminating any large glitches. The external clock fed into the LMR43606-Q1 replaces the internal free-running clock, but does not affect any frequency foldback operation. Output voltage continues to be well-regulated. The device remains in FPWM mode and operates in CCM for light loads when synchronization input is provided.

The MODE/SYNC input pin in the LMR43606-Q1 can operate in one of three selectable modes:

- Auto mode: Pulse frequency modulation (PFM) operation is enabled during light load and diode emulation prevents reverse current through the inductor. See Section 7.4.3.2 for more details.
- FPWM mode: In FPWM mode, diode emulation is disabled, allowing current to flow backwards through the inductor. This allows operation at full frequency even without load current. See Section 7.4.3.3 for more details.
- SYNC mode: The internal clock locks to an external signal applied to the MODE/SYNC pin. As long as output voltage can be regulated at full frequency and is not limited by minimum off time or minimum on time, clock frequency is matched to the frequency of the signal applied to the MODE/SYNC pin. While the device is in SYNC mode, the device operates as though in FPWM mode: diode emulation is disabled, allowing the frequency applied to the MODE/SYNC pin to be matched without a load.

7.3.2.1 Pulse-Dependent MODE/SYNC Pin Control

Most systems that require more than a single mode of operation from the LMR43606-Q1 are controlled by digital circuitry such as a microprocessor. These systems can generate dynamic signals easily but have difficulty generating multi-level signals. Pulse-dependent MODE/SYNC pin control is useful with these systems. To initiate pulse-dependent MODE/SYNC pin control, a valid sync signal must be applied. Table 7-1 shows a summary of the pulse dependent mode selection settings.

Table 7-1. Pulse-Dependent Mode Selection Settings

MODE/SYNC INPUT	MODE
> V_{MODE_H}	FPWM with spread spectrum factory setting
< V_{MODE_L}	Auto mode with spread spectrum factory setting
Synchronization Clock	SYNC mode

Figure 7-3 shows the transition between auto mode and FPWM mode while in pulse-dependent MODE/SYNC control. The LMR43606-Q1 transitions to a new mode of operation after the time, t_{MODE}. Figure 7-3 and Figure 7-4 show the details.

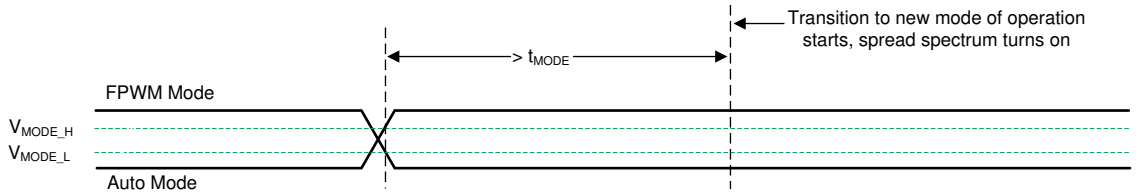


Figure 7-3. Transition from Auto Mode and FPWM Mode

If MODE/SYNC voltage remains constant longer than t_{MODE}, the LMR43606-Q1 enters either auto mode or FPWM mode with spread spectrum turned on (if factory setting is enabled) and MODE/SYNC continues to operate in pulse-dependent scheme.

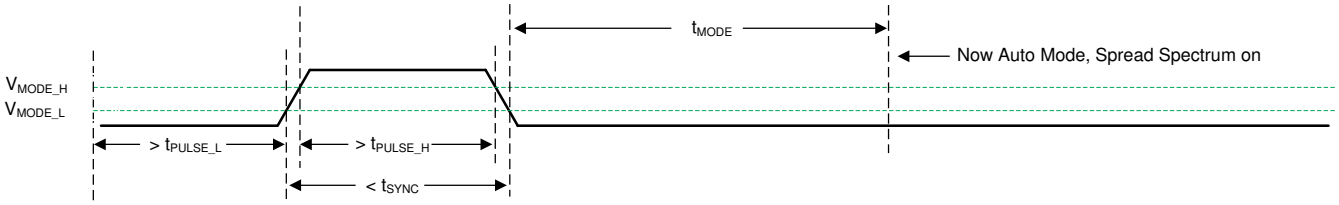


Figure 7-4. Transition from SYNC Mode to Auto Mode

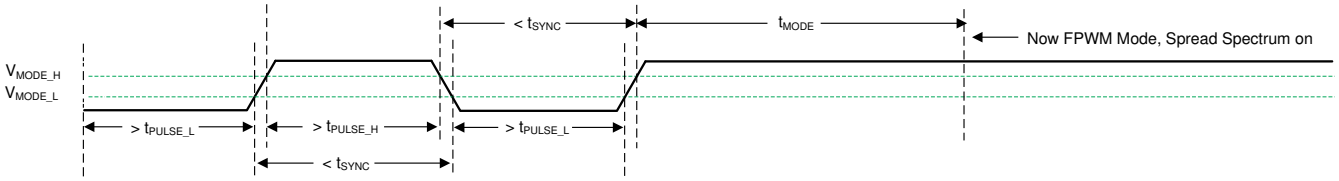


Figure 7-5. Transition from SYNC Mode to FPWM Mode

7.3.3 Adjustable Switching Frequency (with RT)

The select variants in the LMR43606-Q1 family with the RT pin allow the power designers to set any desired operating frequency between 200kHz and 2.2MHz in the applications. See Figure 7-6 to determine the resistor value needed for the desired switching frequency. The RT pin and the MODE/SYNC pin variants share the same pin location. The power supply designer can either use the RT pin variant and adjust the switching frequency of operation as warranted by the application or use the MODE/SYNC variant and synchronize to an external clock signal. See Table 7-2 for selection on programming the RT pin.

Table 7-2. RT Pin Setting

RT INPUT	SWITCHING FREQUENCY
VCC	1MHz
GND	2.2MHz
RT resistor to GND	Adjustable according to Figure 7-6
Float (not recommended)	No switching

Use Equation 1 to calculate the value of RT for a desired frequency.

$$RT = \frac{18286}{Fsw^{1.021}} \quad (1)$$

where

- RT is the frequency setting resistor value (kΩ).
- F_{SW} is the switching frequency.

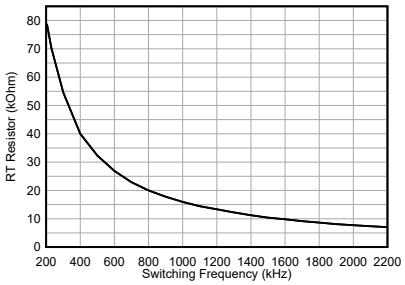


Figure 7-6. RT Values vs Frequency

7.3.4 Power-Good Output Operation

Use the power-good feature using the PGOOD pin of the LMR43606-Q1 to reset a system microprocessor whenever the output voltage is out of regulation. This open-drain output remains low under device fault conditions, such as current limit and thermal shutdown, as well as during normal start-up. A glitch filter prevents false flag operation for any short duration excursions in the output voltage, such as during line and load transients. Output voltage excursions lasting less than t_{RESET_FILTER} do not trip the power-good flag. Power-good operation can best be understood in reference to Figure 7-7. Table 7-3 gives a more detailed breakdown of the PGOOD operation. Here, $V_{PGD_{UV}}$ is defined as the PGD_{UV} scaled version of V_{OUT} (target regulated output voltage) and $V_{PGD_{HYST}}$ as the PGD_{HYST} scaled version of V_{OUT}, where both PGD_{UV} and PGD_{HYST} are listed in Section 6.5. During the initial power up, a total delay of 6ms (typical) is encountered from the time $V_{EN-VOUT}$ is triggered to the time that the power-good is flagged high. This delay only occurs during the device start-up and is not encountered during any other normal operation of the power-good function. When EN is pulled low, the power-good flag output is also forced low. With EN low, power-good remains valid as long as the input voltage ($V_{PGD-VAL}$ is ≥ 1.5V (maximum)).

The power-good output scheme consists of an open-drain n-channel MOSFET, which requires an external pullup resistor connected to a suitable logic supply. It can also be pulled up to either V_{CC} or V_{OUT} through an appropriate resistor, as desired. If this function is not needed, the PGOOD pin can be open or grounded. Limit the current into this pin to ≤ 4mA.

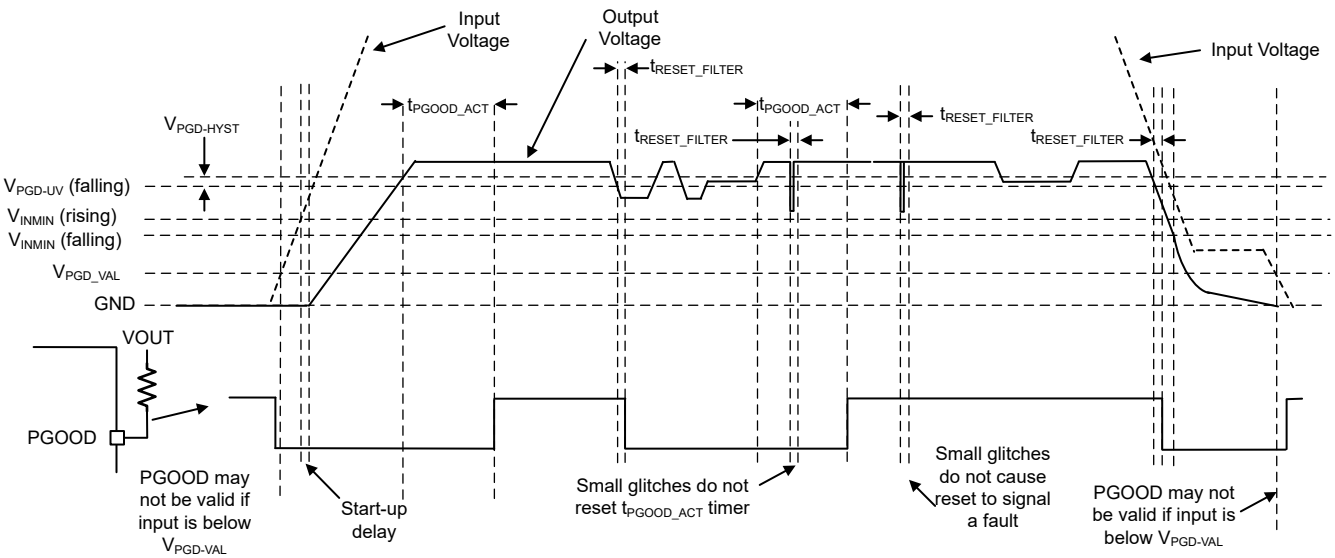


Figure 7-7. Power-Good Operation (OV Events Not Included)

Table 7-3. Fault Conditions for PGOOD (Pull Low)

FAULT CONDITION INITIATED	FAULT CONDITION ENDS (AFTER WHICH t_{PGOOD_ACT} MUST PASS BEFORE PGOOD OUTPUT IS RELEASED)
$V_{OUT} < V_{PGD_{UV}}$ AND $t > t_{RESET\_FILTER}$	Output voltage in regulation: $V_{PGD_{UV}} + V_{PGD_{HYST}} < V_{OUT} < V_{PGD_{OV}} - V_{PGD_{HYST}}$
$V_{OUT} > V_{PGD_{OV}}$ AND $t > t_{RESET\_FILTER}$	Output voltage in regulation
$T_J > T_{SD(trip)}$	$T_J < T_{SD(trip)} - T_{SD(hyst)}$ *and* output voltage in regulation
$EN < V_{EN-VOUT} - V_{EN-HYST}$	$EN > V_{EN-VOUT}$ *and* output voltage in regulation

7.3.5 Internal LDO, VCC, and VOUT/FB Input

The LMR43606-Q1 uses the internal LDO output and the VCC pin for all internal power supply. The VCC pin draws power either from the V_{IN} (in adjustable output variants) or the VOUT/FB (in fixed-output variants). In the fixed output variants, after the LMR43606-Q1 is active but has yet to regulate, the VCC rail continues to draw power from the input voltage, V_{IN}, until the VOUT/FB voltage reaches > 3.3V (or when the device has reached steady-state regulation post the soft start). The VCC rail typically measures 3.3V in both adjustable and fixed output variants. During start-up, VCC momentarily exceeds the normal operating voltage, then drops to the normal operating voltage.

7.3.6 Bootstrap Voltage and $V_{BOOT-UVLO}$ (BOOT Terminal)

The high-side switch driver circuit requires a bias voltage higher than VIN to make sure the HS switch is turned ON. The capacitor connected between BOOT and SW works as a charge pump to boost voltage on the BOOT terminal to (SW+VCC). The boot diode is integrated on the LMR43606-Q1 die to minimize physical design size. TI recommends a 100nF capacitor rated for 10V or higher for CBOOT. The BOOT rail has a UVLO setting. This UVLO has a threshold of $V_{BOOT-UVLO}$ and is typically set at 2.1V. If the CBOOT capacitor is not charged above this voltage with respect to the SW pin, then the part initiates a charging sequence, turning on the low-side switch before attempting to turn on the high-side device.

7.3.7 Output Voltage Selection

In the LMR43606-Q1 family, an adjustable output or fixed output voltage option is configurable for every device variant (see Section 4). For an adjustable output, the user needs an external resistor divider connection between the output voltage node, the device FB pin, and the system GND, as shown in Figure 7-8. The adjustable output voltage operation uses a 1V internal reference voltage. Refer to section Section 8.2.2.2.1 for more details on how to adjust the output voltage.

When using the fixed-output configuration from the LMR43606-Q1 family, simply connect the FB pin (identified as VOUT/FB pin for fixed-output variants in the rest of the data sheet) to the system output voltage node. See Section 4 for more details.

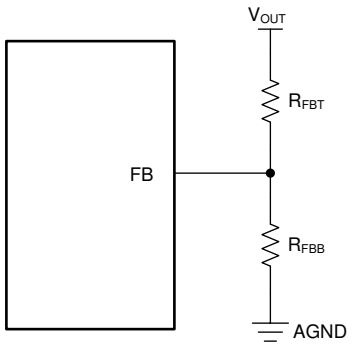


Figure 7-8. Setting Output Voltage for Adjustable Output Variant

In an adjustable output voltage configuration, an addition feedforward capacitor, C_{FF}, in parallel with the R_{FBT}, can be used to optimize the phase margin and transient response. See Section 8.2.2.8 for more details. No additional resistor divider or feedforward capacitor is needed in fixed-output variants.

7.3.8 Spread Spectrum

Spread spectrum eliminates peak emissions at specific frequencies by spreading these peaks across a wider range of frequencies than a part with fixed-frequency operation. The LMR43606-Q1 implements a modulation pattern designed to reduce low frequency-conducted emissions from the first few harmonics of the switching frequency. The pattern can also help reduce the higher harmonics that are more difficult to filter, which can fall in the FM band. These harmonics often couple to the environment through electric fields around the switch node and inductor. The LMR43606-Q1 uses a spread of frequencies which can spread energy smoothly across the FM and TV bands. The device implements dual random spread spectrum (DRSS). DRSS is a combination of a triangular frequency spreading pattern and pseudorandom frequency hopping. The combination allows the spread spectrum to be very effective at spreading the energy at the following:

- Fundamental switching harmonic with slow triangular pattern
- High frequency harmonics with additional pseudo-random jumps at the switching frequency

The advantage of DRSS is the equivalent harmonic attenuation in the upper frequencies with a smaller fundamental frequency deviation. This advantage reduces the amount of input current and output voltage ripple that is introduced at the modulating frequency. Additionally, the LMR43606-Q1 also allows the user to further reduce the output voltage ripple caused by the spread spectrum modulating pattern.

The spread spectrum is only available while the clock of the device is free running at the natural frequency. Any of the following conditions overrides spread spectrum, turning spread spectrum off:

- The clock is slowed due to operation at low-input voltage – this is operation in dropout.
- The clock is slowed under light load in auto mode. Note that if you are operating in FPWM mode, spread spectrum can be active, even if there is no load.
- The clock is slowed due to high input to output voltage ratio. This mode of operation is expected if on time reaches minimum on time. See the Section 6.5.
- The clock is synchronized with an external clock.

7.3.9 Soft Start and Recovery from Dropout

When designing with the LMR43606-Q1, consider slow rise in output voltage due to recovery from dropout and soft start as a two separate operating conditions, as shown in Figure 7-9 and Figure 7-10. Soft start is triggered by any of the following conditions:

- Power is applied to the VIN pin of the device, releasing undervoltage lockout.
- EN is used to turn on the device.
- Recovery from shutdown due to overtemperature protection

After soft start is triggered, the IC takes the following actions:

- The reference used by the IC to regulate output voltage is slowly ramped up. The net result is that output voltage, if previously 0V, takes t_{SS} to reach 90% of the desired value.
- Operating mode is set to auto mode of operation, activating the diode emulation mode for the low-side MOSFET. This action allows start-up without pulling the output low. This is true even when there is a voltage already present at the output during a prebias start-up.

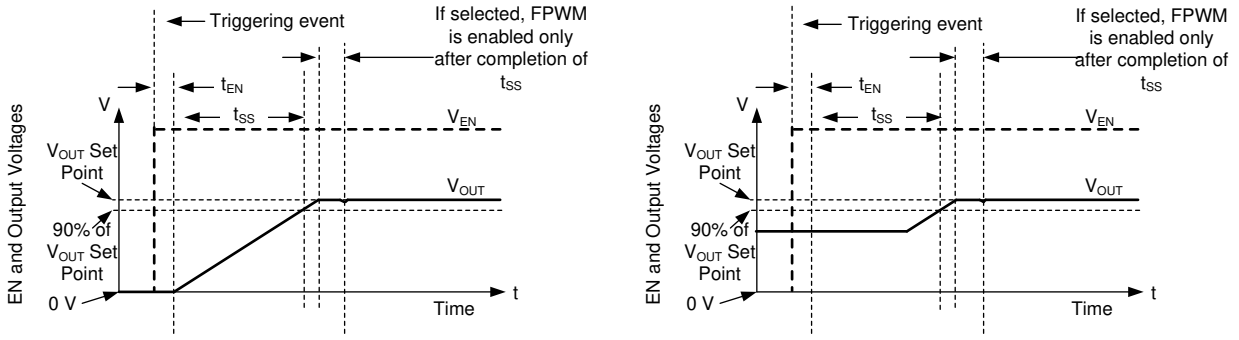


Figure 7-9. Soft Start With and Without Prebias Voltage

7.3.9.1 Recovery from Dropout

Any time the output voltage falls more than a few percent, output voltage ramps up slowly. This condition, called graceful recovery from dropout in this document, differs from soft start in two important ways:

- The reference voltage is set to approximately 1% above what is needed to achieve the existing output voltage.
- If the device is set to FPWM, the device continues to operate in that mode during the recovery from dropout. If output voltage were to suddenly be pulled up by an external supply, the LMR43606-Q1 can pull down on the output. Note that all protections that are present during normal operation are in place, preventing any catastrophic failure if output is shorted to a high voltage or ground.

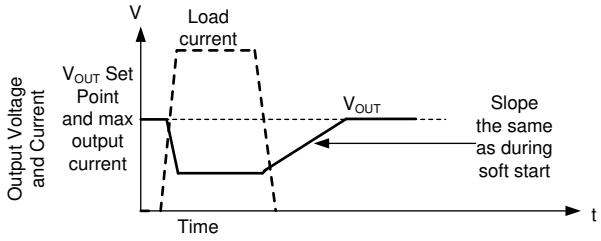


Figure 7-10. Recovery from Dropout

Whether output voltage falls due to high load or low input voltage, after the condition that causes output to fall below the set point is removed, the output climbs at the same speed as during start-up. shows an example of this behavior.

7.3.10 Current Limit and Short Circuit

The LMR43606-Q1 incorporates both peak and valley inductor current limit to provide protection to the device from overloads and short circuits and limit the maximum output current. Valley current limit prevents inductor current runaway during short circuits on the output, while both peak and valley limits work together to limit the maximum output current of the converter. Cycle-by-cycle current limit is used for overloads, while hiccup mode is used for sustained short circuits. Finally, a zero current detector is used on the low-side power MOSFET to implement diode emulation (DEM) at light loads. The typical value of this current limit is found under the I_{ZC} in Section 6.5.

When the device is overloaded, the valley of the inductor current can not reach below I_{VALMAX} (see the Electrical Characteristics table) before the next clock cycle. When this event occurs, the valley current limit control skips that cycle, causing the switching frequency to drop. Further overload causes the switching frequency to continue to drop, and the inductor ripple current to increase. When the peak of the inductor current reaches the high-side current limit, $I_{PEAKMAX}$ (see Section 6.5), the switch duty cycle is reduced and the output voltage falls out of regulation. This action represents the maximum output current from the converter and is given approximately by Equation 2:

$$I_{OUT}\Big|_{max} = \frac{I_{PEAKMAX} + I_{VALMAX}}{2} \quad (2)$$

If, during current limit, the voltage on the FB input falls below about 0.4V due to a short circuit, the device enters into hiccup mode. In this mode, the device stops switching for t_{HICCUP} (see Section 6.5), or about 94ms and then goes through a normal restart with soft start. If the short-circuit condition remains, the device runs in current limit for about 20ms (typical) and then shuts down again. This cycle repeats as long as the short-circuit-condition persists. This mode of operation helps reduce the temperature rise of the device during a hard short on the output. The output current is greatly reduced during hiccup mode. After the output short is removed and the hiccup delay is passed, the output voltage recovers normally.

7.3.11 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the internal switches when the device junction temperature exceeds 168°C (typical). Thermal shutdown does not trigger below 158°C (minimum). After thermal shutdown occurs, hysteresis prevents the part from switching until the junction temperature drops to approximately 153°C (typical). When the junction temperature falls below 153°C (typical), the LMR43606-Q1 attempts another soft start.

While the LMR43606-Q1 is shut down due to high junction temperature, power continues to be provided to VCC. To prevent overheating due to a short circuit applied to VCC, the LDO that provides power for VCC has reduced current limit while the part is disabled due to high junction temperature. The LDO only provides a few milliamperes during thermal shutdown.

7.3.12 Input Supply Current

The LMR43606-Q1 is designed to have very low input supply current when regulating light loads. This design is achieved by powering much of the internal circuitry from the output. The VOUT/FB pin in the fixed-output voltage variants is the input to the LDO that powers the majority of the control circuits. By connecting the VOUT/FB input pin to the output node of the regulator, a small amount of current is drawn from the output. This current is reduced at the input by the ratio of V_{OUT} / V_{IN} as described in Equation 3.

$$I_{QVIN} = I_Q + I_{EN} + I_{BIAS} \times \frac{V_{OUT}}{\eta_{eff} \times V_{IN}} \quad (3)$$

where

- I_{QVIN} is the total standby (switching) current consumed by the operating (switching) buck converter when unloaded.
- I_Q is the current drawn from the V_{IN} terminal.
- I_{EN} is current drawn by the EN terminal. Include this current if EN is connected to VIN. Check I_{LKG-EN} in Section 6.5 for I_{EN}.
- I_{BIAS} is bias current drawn by the BIAS LDO.
- η_{eff} is the light-load efficiency of the buck converter with I_{QVIN} removed from the input current of the buck converter. η_{eff} = 0.8 is a conservative value that can be used under normal operating conditions.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control of the device. When the EN pin voltage is below 0.7V (typical), both the converter and the internal LDO have no output voltage and the part is in shutdown mode. In shutdown mode, the quiescent current drops to typically 250nA.

7.4.2 Standby Mode

The internal LDO has a lower EN threshold than the output of the converter. When the EN pin voltage is above 1V (maximum) and below the precision enable threshold for the output voltage, the internal LDO regulates the VCC voltage at 3.3V typical. The internal power MOSFETs of the SW node remain off unless the voltage on EN pin goes above the precision enable threshold. The LMR43606-Q1 also employs UVLO protection.

7.4.3 Active Mode

The LMR43606-Q1 is in active mode whenever the EN pin is above $V_{EN-VOUT}$, V_{IN} is high enough to satisfy V_{INMIN}, and no other fault conditions are present. The simplest way to enable the operation is to connect the EN pin to V_{IN}, which allows self start-up when the applied input voltage exceeds the minimum V_{INMIN}.

In active mode, depending on the load current, input voltage, and output voltage, the LMR43606-Q1 is in one of five modes:

- Continuous conduction mode (CCM) with fixed switching frequency when load current is above half of the inductor current ripple
- Auto mode - Light Load Operation: PFM when switching frequency is decreased at very light load
- FPWM mode - Light Load Operation: Continuous conduction mode (CCM) when the load current is lower than half of the inductor current ripple
- Minimum on time: At high input voltage and low output voltages, the switching frequency is reduced to maintain regulation
- Dropout mode: When switching frequency is reduced to minimize voltage dropout

7.4.3.1 CCM Mode

The following operating description of the LMR43606-Q1 refers to Section 7.2 and to the waveforms in Figure 7-11. In CCM, the LMR43606-Q1 supplies a regulated output voltage by turning on the internal high-side (HS) and low-side (LS) switches with varying duty cycle (D). During the HS switch on time, the SW pin voltage, V_{SW}, swings up to approximately V_{IN}, and the inductor current, i_L, increases with a linear slope. The HS switch is turned off by the control logic. During the HS switch off time, t_{OFF}, the LS switch is turned on. Inductor current discharges through the LS switch, which forces the V_{SW} to swing below ground by the voltage drop across the LS switch. The converter loop adjusts the duty cycle to maintain a constant output voltage. D is defined by the on time of the HS switch over the switching period:

$$D = T_{ON} / T_{SW} \quad (4)$$

In an ideal buck converter where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage:

$$D = V_{OUT} / V_{IN} \quad (5)$$

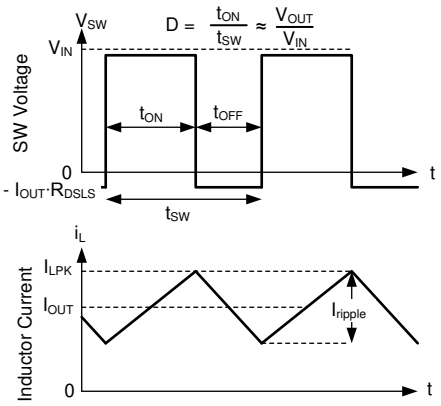


Figure 7-11. SW Voltage and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

7.4.3.2 Auto Mode – Light-Load Operation

The LMR43606-Q1 can have two behaviors while lightly loaded. One behavior, called auto mode operation, allows for seamless transition between normal current mode operation while heavily loaded and highly efficient light-load operation. The other behavior, called FPWM mode, maintains full frequency even when unloaded. Which mode the LMR43606-Q1 operates in depends on which variant from this family is selected. Note that all parts operate in FPWM mode when synchronizing frequency to an external signal.

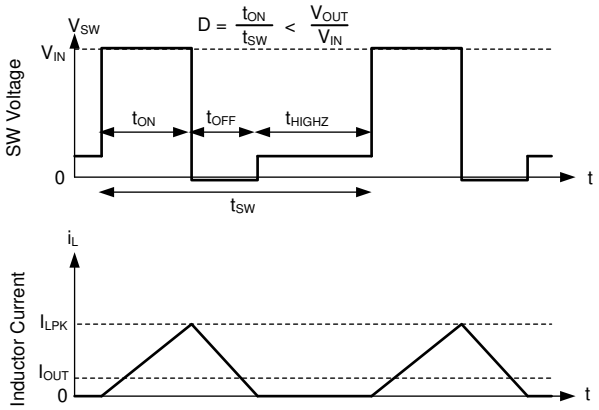
The light-load operation is employed in the LMR43606-Q1 only in auto mode. The light load operation employs two techniques to improve efficiency:

- Diode emulation, which allows DCM operation (see Figure 7-12)
- Frequency reduction (ee Figure 7-12)

Note that while these two features operate together to improve light load efficiency, these features operate independently.

7.4.3.2.1 Diode Emulation

Diode emulation prevents reverse current through the inductor which requires a lower frequency needed to regulate given a fixed peak inductor current. Diode emulation also limits ripple current as frequency is reduced. With a fixed peak current, as output current is reduced to zero, frequency must be reduced to near zero to maintain regulation.



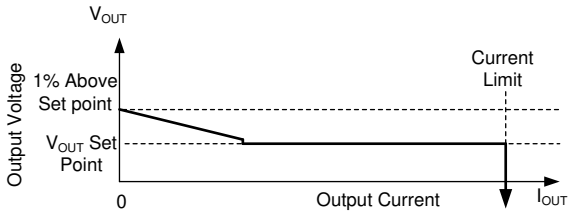
In auto mode, the low-side device is turned off after the SW node current is near zero. As a result, after output current is less than half of what inductor ripple can be in CCM, the part operates in DCM which is equivalent to the statement that diode emulation is active.

Figure 7-12. PFM Operation

The LMR43606-Q1 has a minimum peak inductor current setting (see $I_{PEAKMIN}$ in Section 6.5) while in auto mode. After current is reduced to a low value with fixed input voltage, on time is constant. Regulation is then achieved by adjusting frequency. This mode of operation is called PFM mode regulation.

7.4.3.2.2 Frequency Reduction

The LMR43606-Q1 reduces frequency whenever output voltage is high. This function is enabled whenever the internal error amplifier compensation output, COMP, an internal signal, is low and there is an offset between the regulation set point of VOUT/FB and the voltage applied to VOUT/FB. The net effect is that there is larger output impedance while lightly loaded in auto mode than in normal operation. Output voltage must be approximately 1% high when the part is completely unloaded.



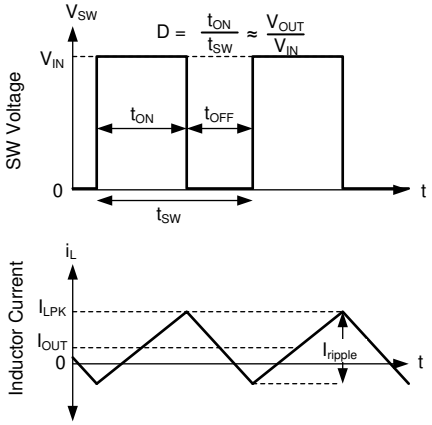
In auto mode, after the output current drops below approximately 1/10th the rated current of the part, output resistance increases so that output voltage is 1% high while the buck is completely unloaded.

Figure 7-13. Steady State Output Voltage Versus Output Current in Auto Mode

In PFM operation, a small DC positive offset is required on the output voltage to activate the PFM detector. The lower the frequency in PFM, the more DC offset is needed on V_{OUT}. If the DC offset on V_{OUT} is not acceptable, a dummy load at V_{OUT} or FPWM mode can be used to reduce or eliminate this offset.

7.4.3.3 FPWM Mode – Light-Load Operation

In FPWM mode, frequency is maintained while lightly loaded. To maintain frequency, a limited reverse current is allowed to flow through the inductor. Reverse current is limited by reverse current limit circuitry. See Section 6.5 for reverse current limit values.



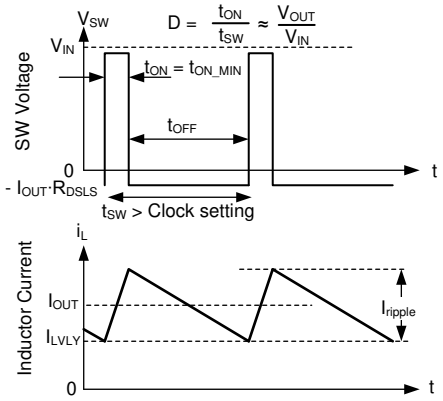
In FPWM mode, Continuous Conduction (CCM) is possible even if I_{OUT} is less than half of I_{ripple}.

Figure 7-14. FPWM Mode Operation

For all devices, in FPWM mode, frequency reduction is still available if output voltage is high enough to command minimum on time even while lightly loaded, allowing good behavior during faults which involve output being pulled up.

7.4.3.4 Minimum On-Time (High Input Voltage) Operation

The LMR43606-Q1 continues to regulate output voltage even if the input-to-output voltage ratio requires an on time less than the minimum on time of the chip with a given clock setting. This event is accomplished using valley current control. At all times, the compensation circuit dictates both a maximum peak inductor current and a maximum valley inductor current. If for any reason, valley current is exceeded, the clock cycle is extended until valley current falls below that determined by the compensation circuit. If the converter is not operating in current limit, the maximum valley current is set above the peak inductor current, preventing valley control from being used unless there is a failure to regulate using peak current only. If the input-to-output voltage ratio is too high, such that the inductor current peak value exceeds the peak command dictated by compensation, the high-side device cannot be turned off quickly enough to regulate output voltage. As a result, the compensation circuit reduces both peak and valley current. After a low enough current is selected by the compensation circuit, valley current matches that being commanded by the compensation circuit. Under these conditions, the low-side device is kept on and the next clock cycle is prevented from starting until inductor current drops below the desired valley current. Since on time is fixed at the minimum value, this type of operation resembles that of a device using a Constant On-Time (COT) control scheme; see Figure 7-15.

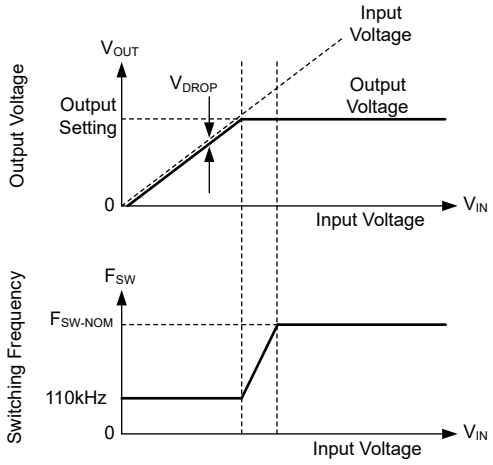


In valley control mode, minimum inductor current is regulated, not peak inductor current.

Figure 7-15. Valley Current Mode Operation

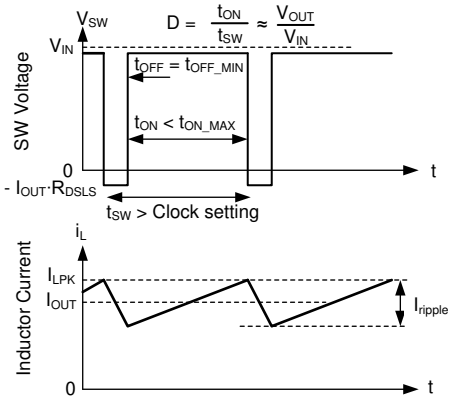
7.4.3.5 Dropout

Dropout operation is defined as any input-to-output voltage ratio that requires frequency to drop to achieve the required duty cycle. At a given clock frequency, duty cycle is limited by minimum off time. After this limit is reached as shown in Figure 7-17 if clock frequency was to be maintained, the output voltage falls. Instead of allowing the output voltage to drop, the LMR43606-Q1 extends the high-side switch on time past the end of the clock cycle until the needed peak inductor current is achieved. The clock is allowed to start a new cycle once peak inductor current is achieved or after a predetermined maximum on time, t_{ON-MAX}, of approximately 9µs passes. As a result, after the needed duty cycle cannot be achieved at the selected clock frequency due to the existence of a minimum off time, frequency drops to maintain regulation. As shown in Figure 7-16, if input voltage is low enough so that output voltage cannot be regulated even with an on time of t_{ON-MAX}, output voltage drops to slightly below the input voltage by V_{DROP}. For additional information on recovery from dropout, refer to Figure 7-10.



Output voltage and frequency versus input voltage: If there is little difference between input voltage and output voltage setting, the IC reduces frequency to maintain regulation. If input voltage is too low to provide the desired output voltage at approximately 110kHz, input voltage tracks output voltage.

Figure 7-16. Frequency and Output Voltage in Dropout



Switching waveforms while in dropout. Inductor current takes longer than a normal clock to reach the desired peak value. As a result, frequency drops. This frequency drop is limited by t_{ON-MAX}.

Figure 7-17. Dropout Waveforms

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

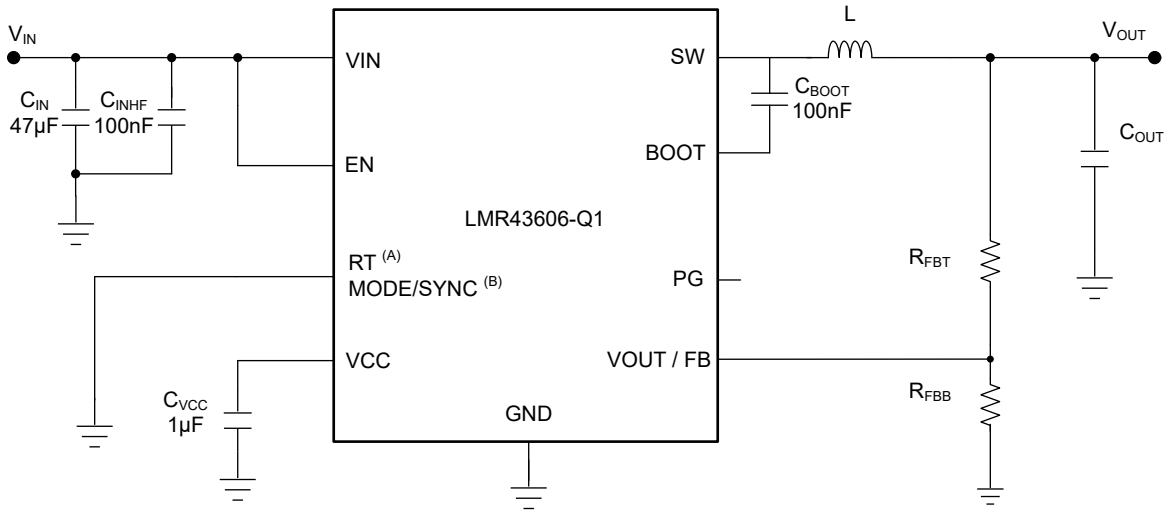
The LMR43606-Q1 step-down DC-to-DC converter is typically used to convert a higher DC voltage to a lower DC voltage. LMR43606-Q1 supports a maximum output current of 0.6A. The following design procedure can be used to select components for the LMR43606-Q1.

Note

All of the capacitance values given in the following application information refer to *effective* values unless otherwise stated. The *effective* value is defined as the actual capacitance under DC bias and temperature, not the rated or nameplate values. Use high-quality, low-ESR, ceramic capacitors with an X7R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under DC bias the capacitance drops considerably. Large case sizes and higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank must be made to make sure that the minimum value of *effective* capacitance is provided.

8.2 Typical Application

Figure 8-1 shows a typical application circuit for the LMR43606-Q1. This device is designed to function over a wide range of external components and system parameters. However, the internal compensation is designed for a certain range of external inductance and output capacitance. As a quick-start guide, provide typical component values for a range of the most common output voltages.



A. The RT pin is factory-set for externally adjustable switching frequency RT variants only. Tying this pin to GND results in 2.2MHz switching frequency. See Section 7.3.3 for details.

B. The MODE/SYNC pin is factory-set for fixed frequency MODE/SYNC variants only. Tying this pin to GND results in AUTO mode. See Section 7.3.2 for details.

Figure 8-1. Example Application Circuit

Table 8-1. Typical External Component Values for Adjustable Output LMR43606-Q1

f_{SW} (1) (2) (kHz)	V_{OUT} (V)	L (µH)	NOMINAL C_{OUT} (RATED CAPACITANCE)	R_{FBT} (3) (kΩ)	R_{FBB} (kΩ)	C_{IN}	C_{BOOT}	C_{VCC}
400	3.3	33	3 × 22µF	33.2	14.3	4.7µF + 1 × 100nF	100nF	1µF
2200	3.3	4.7	1 × 22µF	33.2	14.3	4.7µF + 1 × 100nF	100nF	1µF
400	5	47	3 × 22µF	49.9	12.4	4.7µF + 1 × 100nF	100nF	1µF
2200	5	5.6	1 × 22µF	49.9	12.4	4.7µF + 1 × 100nF	100nF	1µF

(1) Inductor values are calculated based on typical V_{IN} = 12V.
(2) The switching frequencies listed here can be achieved in a number of ways depending on the device variant. For RT devices see Section 7.3.3. For MODE/SYNC devices see Section 7.3.2.
(3) For R_{FBT} and R_{FBB} values outside the range stated above, see Section 8.2.2.2.1.

Table 8-2. Typical External Component Values for Fixed Output LMR43606-Q1

f_{SW} (kHz)	V_{OUT} (V)	L (µH)	NOMINAL C_{OUT} (RATED CAPACITANCE)	R_{FBT} (kΩ)	R_{FBB} (kΩ)	C_{IN}	C_{BOOT}	C_{VCC}
400	3.3	33	3 × 22µF	0	DNP	4.7µF + 1 × 100nF	100nF	1µF
2200	3.3	4.7	1 × 22µF	0	DNP	4.7µF + 1 × 100nF	100nF	1µF
400	5	47	3 × 22µF	0	DNP	4.7µF + 1 × 100nF	100nF	1µF
2200	5	5.6	1 × 22µF	0	DNP	4.7µF + 1 × 100nF	100nF	1µF

8.2.1 Design Requirements

Section 8.2.2 provides a detailed design procedure based on Table 8-3.

Table 8-3. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	12V, (4V to 36V)
Output voltage	3.3V
Maximum output current	0A to 2A
Switching frequency	2200kHz

8.2.2 Detailed Design Procedure

The following design procedure applies to Figure 8-1 and Table 8-2.

8.2.2.1 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall design size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows the use of smaller inductors and output capacitors, hence, a more compact design. For this example, 2200kHz is used.

8.2.2.2 Setting the Output Voltage

The VOUT/FB pin of the device can be either connected directly to the output capacitor or the mid point of a feedback resistor divider. When connected directly to the output capacitor, the device operates as a fixed output option. The 3.3V or 5V fixed output options are factory trimmed and are unique to a specific device. See Section 4 for the selection of fixed output voltage versions.

8.2.2.2.1 FB for Adjustable Output

If other voltages are desired, the VOUT/FB pin can be connected to a feedback resistor divider network to set the output voltage. The divider network is comprised of R_{FBT} and R_{FBB}, and closes the loop between the output voltage and the converter. The converter regulates the output voltage by holding the voltage on the FB pin equal to the internal reference voltage, V_{REF}. The converter determines whether fixed output voltage or adjustable output voltage is required by sensing the resistance of the feedback path during start-up. To make that the converter regulates to the desired output voltage, the typical minimum value for the parallel combination of R_{FBT} and R_{FBB} is 5kΩ while the typical maximum value is 10kΩ as shown in Equation 6. Equation 7 can be used as a starting point to determine the value of R_{FBT}. Reference Table 8-4 for a list of acceptable resistor values for various output voltages.

$$5\ k\Omega\ <\ R_{FBT}||R_{FBB}\ \leq 10\ k\Omega \tag{6}$$

$$R_{FBT} \leq 10\ k\Omega \times \frac{V_{OUT}}{1\ V} \tag{7}$$

Table 8-4. Recommended Feedback Resistor Values for Various Output Voltages

V_{OUT} (V)	R_{FBT} (1) (kΩ)	R_{FBB} (kΩ)
2.5	24.9	16.5
3.3	33.2	14.3
5	49.9	12.4
6	60.4	12.1
9	90.9	11.3

(1) R_{FBT} and R_{FBB} based on 1% standard resistor values.

For this 3.3V example, the user can choose the *LMR43606MSC3RPERQ1* and connect the VOUT/FB pin directly to the output capacitor.

8.2.2.3 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current. Note that when selecting the ripple current for applications with much smaller maximum load than the maximum available from the device, use the maximum device current. Equation 8 can be used to determine the value of inductance. The constant K is the percentage of inductor current ripple. For this example, choose K = 0.4 and find an inductance of L = 4.53µH. Select the standard value of 4.7µH.

$$L = \frac{(V_{IN} - V_{OUT})}{f_{SW} \times K \times I_{OUTmax}} \times \frac{V_{OUT}}{V_{IN}} \quad (8)$$

Ideally, the saturation current rating of the inductor is at least as large as the high-side switch current limit, $I_{PEAKMAX}$ (see Section 6.5). This size makes sure that the inductor does not saturate, even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, I_{VALMAX}, is designed to reduce the risk of current runaway, a saturated inductor can cause the current to rise to high values very rapidly. This event can lead to component damage. Do not allow the inductor to saturate. Inductors with a ferrite core material have very *hard* saturation characteristics, but usually have lower core losses than powdered iron cores. Powered iron cores exhibit a *soft* saturation, allowing some relaxation in the current rating of the inductor. However, powered iron cores have more core losses at frequencies above about 1MHz. In any case, the inductor saturation current must not be less than the maximum peak inductor current at full load.

The maximum inductance is limited by the minimum current ripple for the current mode control to perform correctly. As a rule, the minimum inductor ripple current must be no less than about 10% of the device maximum rated current under nominal conditions.

8.2.2.4 Output Capacitor Selection

The current mode control scheme of the LMR43606-Q1 devices allows operation over a wide range of output capacitance. The output capacitor bank is usually limited by the load transient requirements and stability rather than the output voltage ripple. Refer to Table 8-1 for typical output capacitor value for 3.3V and 5V output voltages. Based on Table 8-1, for a 3.3V output design, choose the recommended 2 × 22µF ceramic output capacitor for this example. For other designs with other output voltages, WEBENCH can be used as a starting point for selecting the value of output capacitor.

In practice, the output capacitor has the most influence on the transient response and loop-phase margin. Load transient testing and bode plots are the best way to validate any given design and must always be completed before the application goes into production. In addition to the required output capacitance, a small ceramic capacitor placed on the output can help reduce high-frequency noise. Small-case size ceramic capacitors in the range of 1nF to 100nF can be very helpful in reducing spikes on the output caused by inductor and board parasitics.

Limit the maximum value of total output capacitance to about 10 times the design value, or 1000µF, whichever is smaller. Large values of output capacitance can adversely affect the start-up behavior of the regulator as well as the loop stability. If values larger than noted here must be used, then a careful study of start-up at full load and loop stability must be performed.

8.2.2.5 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum ceramic capacitance of 4.7µF is required on the input of the LMR43606-Q1. This must be rated for at least the maximum input voltage that the application requires, preferably twice the maximum input voltage. This capacitance can be increased to help reduce input voltage ripple and maintain the input voltage during load transients. In addition, a small case size 100nF ceramic capacitor must be used at the input, as close a possible to the regulator. In the case of the LMR43606MQ3EVM-2M this capacitor is placed approximately 0.4mm away from the regulator. This placement

provides a high frequency bypass for the control circuits internal to the device. For this example, a 4.7µF, 50V, X7R (or better) ceramic capacitor is chosen. The 100nF must also be rated at 50V with an X7R dielectric.

Using an electrolytic capacitor on the input in parallel with the ceramics is often desirable. This statement is especially true if long leads or traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitor or capacitors. The approximate RMS value of this current can be calculated from Equation 9 and must be checked against the manufacturer maximum ratings.

$$I_{RMS} \cong \frac{I_{OUT}}{2} \tag{9}$$

8.2.2.6 C_{BOOT}

The LMR43606-Q1 requires a bootstrap capacitor connected between the BOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. A high-quality ceramic capacitor of 100nF and at least 16V is required.

8.2.2.7 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the regulator. This output requires a 1µF, 16V ceramic capacitor connected from VCC to GND for proper operation. In general, this output must not be loaded with any external circuitry. However, this output can be used to supply the pullup for the power-good function (see Section 7.3.4). A value in the range of 10kΩ to 100kΩ is a good choice in this case. The nominal output voltage on VCC is 3.3V; see Section 6.5 for limits.

8.2.2.8 C_{FF} Selection

In some cases, a feedforward capacitor can be used across R_{FBT} to improve the load transient response or improve the loop-phase margin. *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feedforward Capacitor* application report is helpful when experimenting with a feedforward capacitor.

Due to the nature of the feedback detect circuitry, the value of C_{FF} must be limited to make sure that the desired output voltage is established when configuring for adjustable output voltages. Follow Equation 10 to make sure C_{FF} remains below the maximum value.

$$C_{FF} < C_{OUT} \times \frac{\sqrt{V_{OUT}}}{1.2\ M\Omega} \tag{10}$$

8.2.2.9 External UVLO

In some cases, an input UVLO level different than that provided internal to the device is needed. This level can be accomplished by using the circuit shown in Figure 8-2. The input voltage at which the device turns on is designated as V_{ON} while the turn-off voltage is V_{OFF}. First, a value for R_{ENB} is chosen in the range of 10kΩ to 100kΩ, then Equation 11 and Equation 12 are used to calculate R_{ENT} and V_{OFF} respectively.

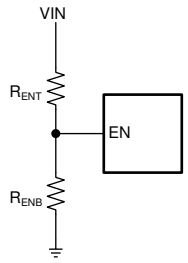


Figure 8-2. Setup for External UVLO Application

$$R_{ENT} = \left(\frac{V_{ON}}{V_{EN-VOUT}} - 1\right) \times R_{ENB} \quad (11)$$

$$V_{OFF} = V_{ON} \times \left(1 - \frac{V_{EN-HYS}}{V_{EN-VOUT}}\right) \quad (12)$$

where

- V_{ON} is the V_{IN} turn-on voltage.
- V_{OFF} is the V_{IN} turn-off voltage.

8.2.2.10 Maximum Ambient Temperature

As with any power conversion device, the LMR43606-Q1 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the ambient temperature, the power loss, and the effective thermal resistance, $R_{\theta JA}$, of the device, and PCB combination. The maximum junction temperature for the LMR43606-Q1 must be limited to 150°C. This limit establishes a limit on the maximum device power dissipation and, therefore, the load current. Equation 13 shows the relationships between the important parameters. Seeing that larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current is easy. The converter efficiency can be estimated by using the curves provided in this data sheet. If the desired operating conditions cannot be found in one of the curves, interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. For more information reference *Semiconductor and IC Package Thermal Metrics* application report.

$$I_{OUT}\Big|_{MAX} = \frac{\left(T_J - T_A\right)}{R_{\theta JA}} \times \frac{\eta}{(1-\eta)} \times \frac{1}{V_{OUT}} \quad (13)$$

where

- η is the efficiency.

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature and flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

Use Equation 14 to estimate the IC junction temperature for a given operating condition.

$$T_J \cong T_A + R_{\theta JA} \times IC\ Power\ Loss \quad (14)$$

where

- T_J is the IC junction temperature (ºC).
- T_A is the ambient temperature (ºC).
- $R_{\theta JA}$ is the thermal resistance (ºC/W).
- IC power loss is the power loss for the IC (W).

The IC Power loss mentioned above is the overall power loss minus the loss that comes from the inductor DC resistance. The overall power loss can be approximated by using WEBENCH for a specific operating condition and temperature.

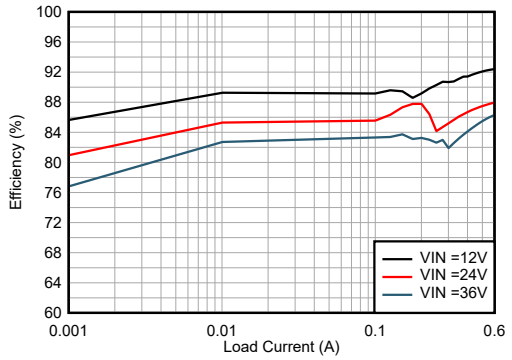
Use the following resources as guides to optimal thermal PCB design and estimating $R_{\theta JA}$ for a given application environment:

- *Thermal Design by Insight not Hindsight* application report
- *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages* application report

- *Semiconductor and IC Package Thermal Metrics* application report
- *Thermal Design Made Simple with LM43603 and LM43602* application report
- *PowerPAD™ Thermally Enhanced Package* application report
- *PowerPAD™ Made Easy* application report
- *Using New Thermal Metrics* application report
- *PCB Thermal Calculator*

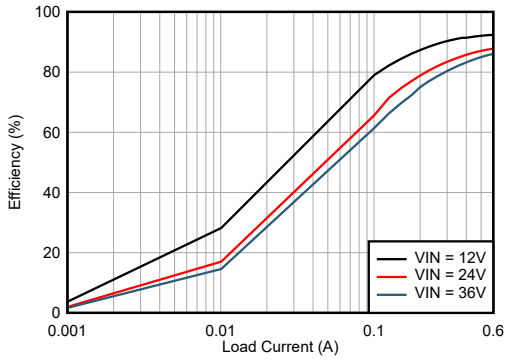
8.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 12V, T_A = 25°C.



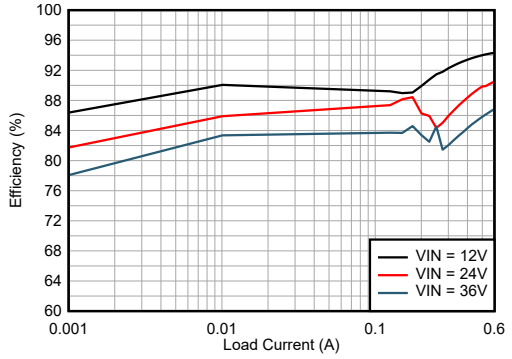
LMR43606MSC3 V_{OUT} = 3.3V 2.2MHz (AUTO) Fixed

Figure 8-3. Efficiency



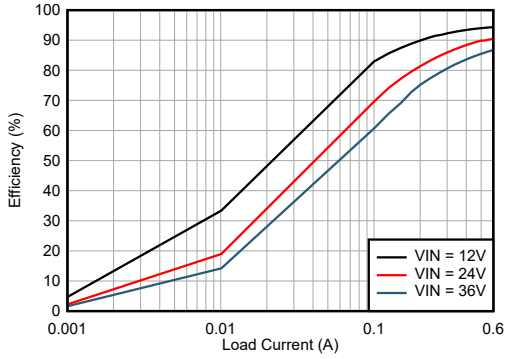
LMR43606MSC3 V_{OUT} = 3.3V 2.2MHz (FPWM) Fixed

Figure 8-4. Efficiency



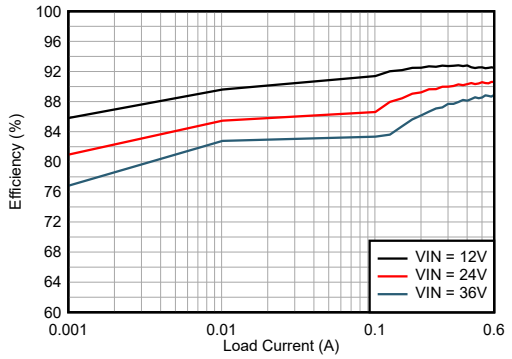
LMR43606MSC5 V_{OUT} = 5V 2.2MHz (AUTO) Fixed

Figure 8-5. Efficiency



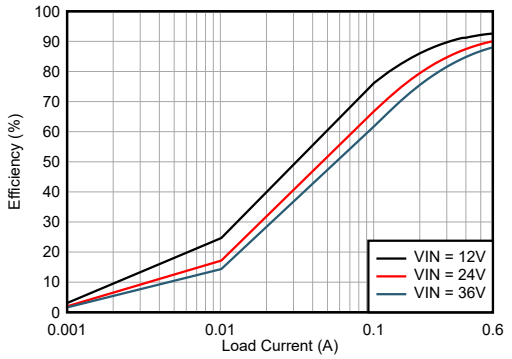
LMR43606MSC5 V_{OUT} = 5V 2.2MHz (FPWM) Fixed

Figure 8-6. Efficiency



LMR43606RS3 V_{OUT} = 3.3V 400kHz (AUTO) Fixed

Figure 8-7. Efficiency

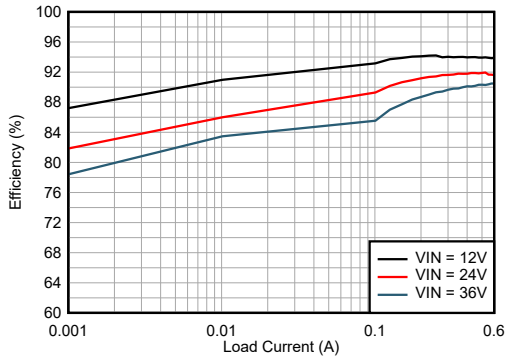


LMR43606MSC3 V_{OUT} = 3.3V 400kHz (FPWM) Fixed

Figure 8-8. Efficiency

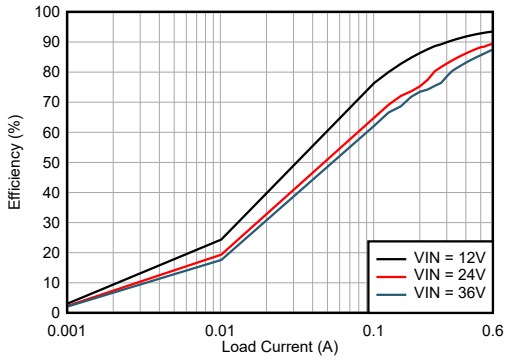
8.2.3 Application Curves (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 12V, T_A = 25°C.



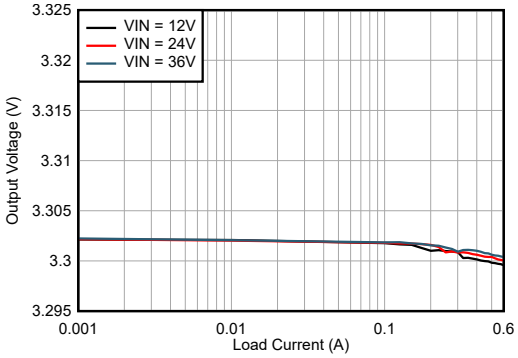
LMR43606RS5 V_{OUT} = 5V Fixed 400kHz (AUTO)

Figure 8-9. Efficiency



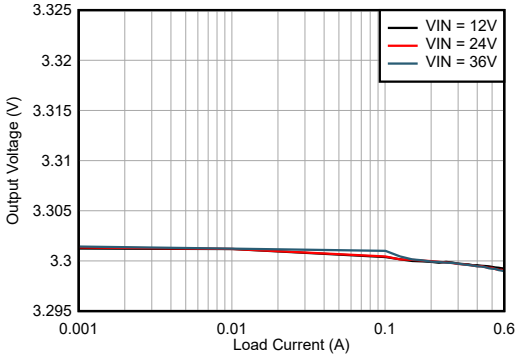
LMR43606MSC5 V_{OUT} = 5V Fixed 400kHz (FPWM)

Figure 8-10. Efficiency



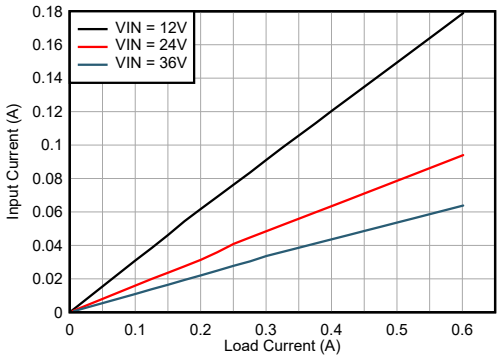
LMR43606MSC3 V_{OUT} = 3.3V Fixed 2.2MHz (AUTO)

Figure 8-11. Line and Load Regulation



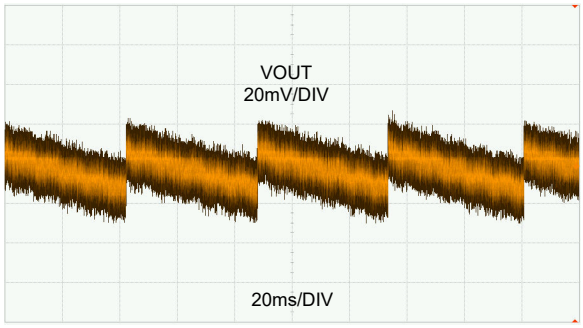
LMR43606MSC3 V_{OUT} = 3.3V Fixed 400kHz (AUTO)

Figure 8-12. Line and Load Regulation



LMR43606MSC3 V_{OUT} = 3.3V Fixed 2.2MHz (AUTO)

Figure 8-13. Input Current vs. Load Current

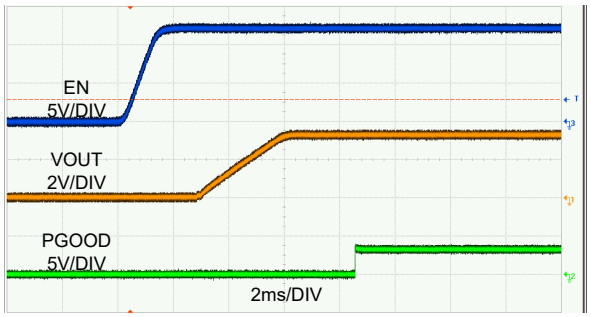


LMR43606MSC3 V_{OUT} = 3.3V Fixed 2.2MHz (AUTO)

Figure 8-14. No Load Output Voltage Ripple

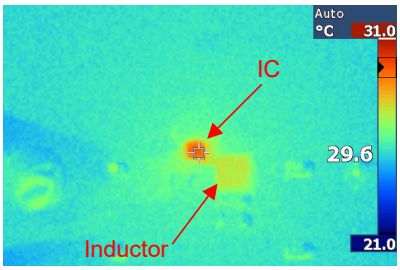
8.2.3 Application Curves (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 12V, T_A = 25°C.



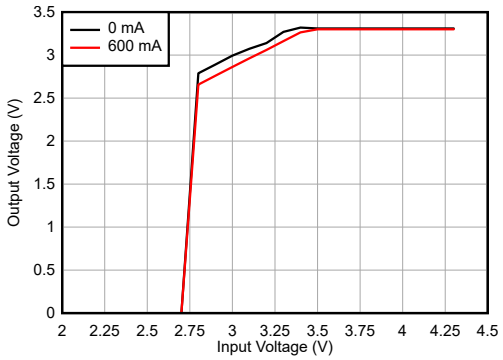
LMR43606MSC3 V_{OUT} = 3.3V fixed 2.2MHz (AUTO)

Figure 8-15. Start Up



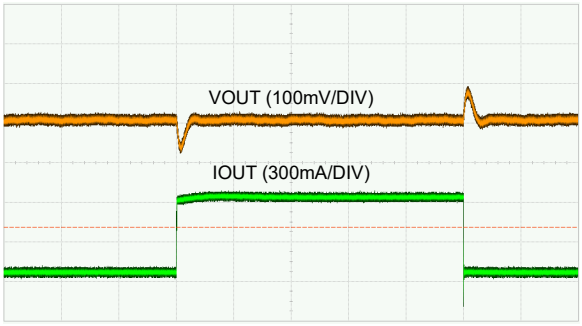
LMR43606MSC3 V_{OUT} = 3.3V $12V_{IN}$, 600mA, 2.2MHz (AUTO)
Fixed 3.3 V_{OUT}

Figure 8-16. EVM Thermal Performance



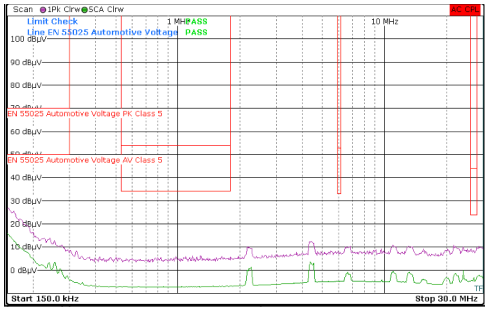
LMR43606MSC3 V_{OUT} = 3.3V 2.2MHz (AUTO)
Fixed

Figure 8-17. Dropout



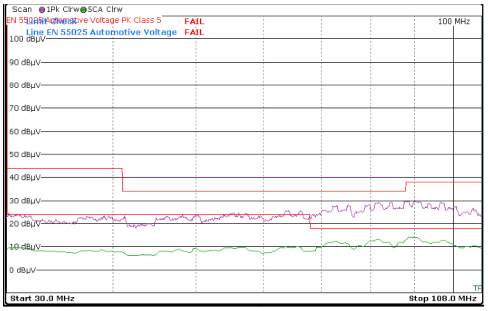
LMR43606MSC3 V_{OUT} = 3.3V 2.2MHz (FPWM)
60 mA to 600mA,1A/µs Fixed

Figure 8-18. Load Transient



V_{IN} = 13.5V V_{OUT} = 3.3V Fixed f_{SW} = 2.2MHz Load = 0.6A

Figure 8-19. Typical CISPR 25 Conducted EMI 150kHz – 30MHz
Purple: Peak Detect, Green: Average Detect

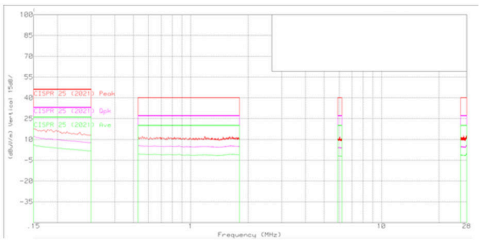


V_{IN} = 13.5V V_{OUT} = 3.3V Fixed f_{SW} = 2.2MHz Load = 0.6A

Figure 8-20. Typical CISPR 25 Conducted EMI 30MHz – 108MHz
Purple: Peak Detect, Green: Average Detect

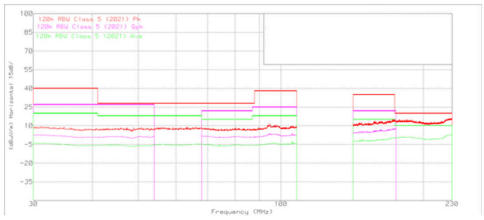
8.2.3 Application Curves (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 12V, T_A = 25°C.



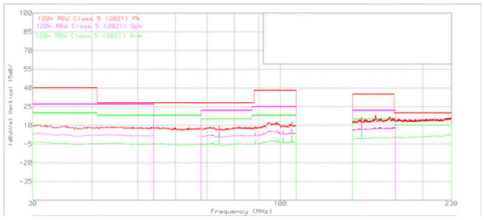
V_{IN} = 13.5V | V_{OUT} = 3.3V Fixed | f_{SW} = 2.2MHz Load = 0.6A

Figure 8-21. Typical CISPR 25 Radiated EMI 150kHz – 30MHz Rod Antenna Red: Peak Detect, Green: Average Detect



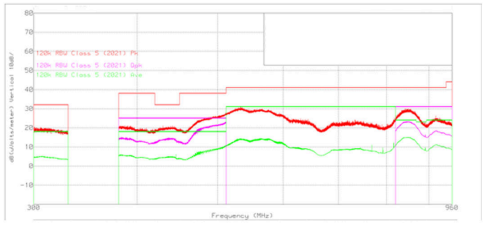
V_{IN} = 13.5V | V_{OUT} = 3.3V Fixed | f_{SW} = 2.2MHz Load = 0.6A

Figure 8-22. Typical CISPR 25 Radiated EMI 30MHz – 230MHz Vertical Bicon Antenna Red: Peak Detect, Green: Average Detect



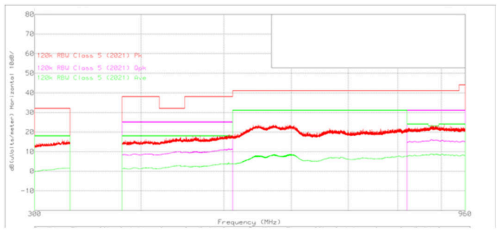
V_{IN} = 13.5V | V_{OUT} = 3.3V Fixed | f_{SW} = 2.2MHz Load = 0.6A

Figure 8-23. Typical CISPR 25 Radiated EMI 30MHz – 230MHz Horizontal Bicon Antenna Red: Peak Detect, Green: Average Detect



V_{IN} = 13.5V | V_{OUT} = 3.3V Fixed | f_{SW} = 2.2MHz Load = 0.6A

Figure 8-24. Typical CISPR 25 Radiated EMI 300MHz – 1GHz Vertical Log Antenna Red: Peak Detect, Green: Average Detect

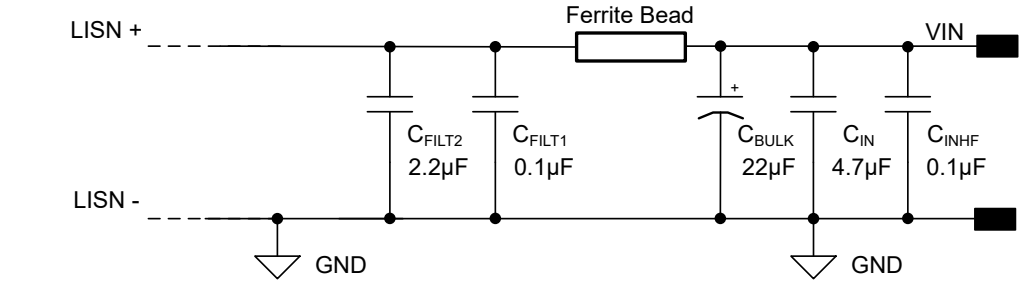


V_{IN} = 13.5V | V_{OUT} = 3.3V Fixed | f_{SW} = 2.2MHz Load = 0.6A

Figure 8-25. Typical CISPR 25 Radiated EMI 300MHz – 1GHz Horizontal Log Antenna Red: Peak Detect, Green: Average Detect

8.2.3 Application Curves (continued)

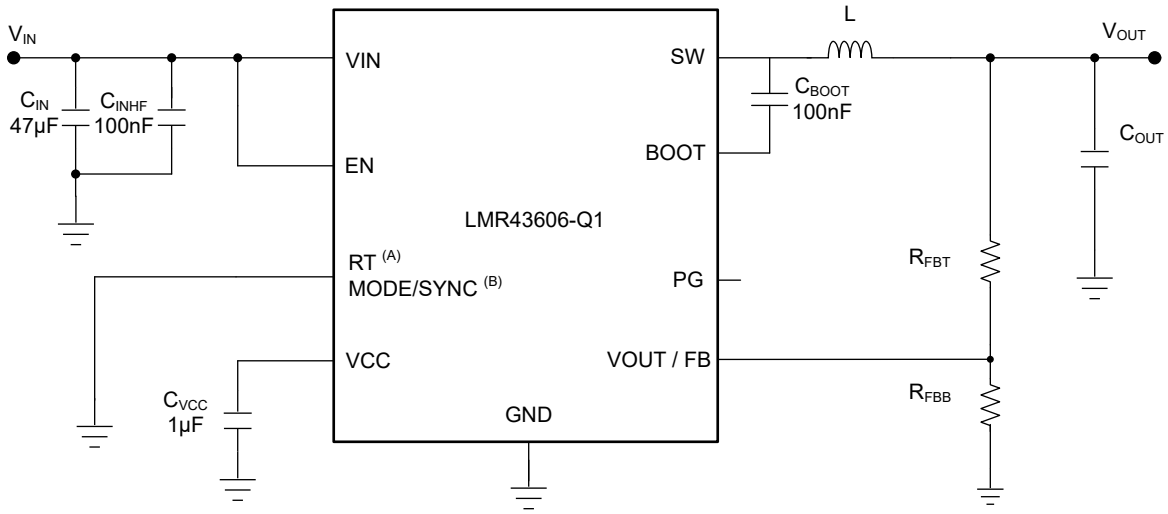
Unless otherwise specified the following conditions apply: V_{IN} = 12V, T_A = 25°C.



Ferrite Bead Part Number: FBMH3225HM601NT

Alternate Ferrite Bead Part Number: FBMH3225HM102N

Figure 8-26. Typical Input EMI Filter



A. The RT pin is factory-set for externally adjustable switching frequency RT variants only. Tying this pin to GND results in 2.2MHz switching frequency. See Section 7.3.3 for details.

B. The MODE/SYNC pin is factory-set for fixed frequency MODE/SYNC variants only. Tying this pin to GND results in auto mode. See Section 7.3.2 for details.

Figure 8-27. Example Application Circuit

Table 8-5. BOM for Typical Application Curves

U1	f_{SW}	V_{OUT}	L	NOMINAL C_{OUT} (RATED CAPACITANCE)	RFBT	RFBB	CFF
LMR43606MSC3RPERQ1	2200kHz	3.3V Fixed	5.6µH, 31mΩ	2 × 22µF	0Ω	DNP	DNP

8.3 Best Design Practices

- Do not exceed the *Absolute Maximum Ratings*.
- Do not exceed the *Recommended Operating Conditions*.
- Do not exceed the *ESD Ratings*.
- Do not allow the EN input to float.
- Do not allow the output voltage to exceed the input voltage, nor go below ground.
- Follow all the guidelines and suggestions found in this data sheet before committing the design to production. TI application engineers are ready to help critique design and PCB layout to help make the project a success.

8.4 Power Supply Recommendations

The characteristics of the input supply must be compatible with Section 6 found in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with Equation 15.

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (15)$$

where

- η is the efficiency.

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an underdamped resonant circuit, resulting in overvoltage transients at the input to the regulator. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip can cause the regulator to momentarily shut down and reset. The best way to solve these kind of issues is to limit the distance from the input supply to the regulator or plan to use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors help dampen the input resonant circuit and reduce any overshoots. A value in the range of 20µF to 100µF is usually sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This action can lead to instability, as well as some of the effects mentioned above, unless designed carefully. The *AN-2162 Simple Success With Conducted EMI From DC/DC Converters* application report provides helpful suggestions when designing an input filter for any switching regulator.

In some cases, a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a *snap-back* characteristic (thyristor type). TI does not recommend the use of a device with this type of characteristic. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow can damage the device.

8.5 Layout

8.5.1 Layout Guidelines

The PCB layout of any DC/DC converter is critical to the best performance of the design. Poor PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, to a great extent, the EMI performance of the regulator is dependent on the PCB layout. In a buck converter, the most critical PCB feature is the loop formed by the input capacitor or capacitors and power ground, as shown in Figure 8-28. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the converter. Because of this, the traces in this loop must be wide and short, and the loop area as small as possible to

reduce the parasitic inductance. Figure 8-29 shows a recommended layout for the critical components of the LMR43606-Q1.

- *Place the input capacitors as close as possible to the VIN and GND terminals.*
- *Place bypass capacitor for VCC close to the VCC pin.* This capacitor must be placed close to the device and routed with short, wide traces to the VCC and GND pins.
- *Use wide traces for the C_{BOOT} capacitor.* Place C_{BOOT} close to the device with short/wide traces to the BOOT and SW pins.
- *Place the feedback divider as close as possible to the FB pin of the device.* Place R_{FBB}, R_{FBT}, and C_{FF}, if used, physically close to the device. The connections to FB and GND must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, the latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
- *Use at least one ground plane in one of the middle layers.* This plane acts as a noise shield and as a heat dissipation path.
- *Provide wide paths for VIN, VOUT, and GND.* Making these paths as wide and direct as possible reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
- *Provide enough PCB area for proper heat-sinking.* As stated in Section 8.2.2.10, enough copper area must be used to make sure of e a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. The top and bottom PCB layers must be made with two ounce copper and no less than one ounce. If the PCB design uses multiple copper layers (recommended), these thermal vias can also be connected to the inner layer heat-spreading ground planes.
- *Keep the switch area small.* Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time, the total area of this node must be minimized to help reduce radiated EMI.

See the following PCB layout resources for additional important guidelines:

- *Layout Guidelines for Switching Power Supplies* application report
- *Simple Switcher PCB Layout Guidelines* application report
- *Construction Your Power Supply- Layout Considerations* seminar
- *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x* application report

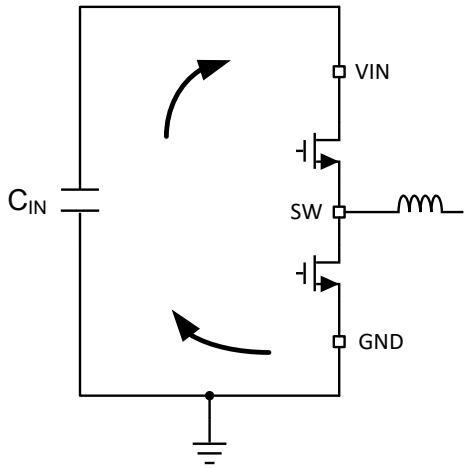


Figure 8-28. Current Loops With Fast Edges

8.5.1.1 Ground and Thermal Considerations

As previously mentioned, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces as well as a quiet reference potential for the control circuitry. Connect the GND pin to the ground planes using vias next to the bypass capacitors. The GND trace, as well as the VIN and SW traces, must be constrained to one side of the ground planes. The other side of the ground plane contains much less noise; use for sensitive routes.

TI recommends providing adequate device heat-sinking by having enough copper near the GND pin. See Figure 8-29 for example layout. Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top as: 2 oz / 1 oz / 1 oz / 2 oz. A four-layer board with enough copper thickness, and proper layout, provides low current conduction impedance, proper shielding and lower thermal resistance.

8.5.2 Layout Example

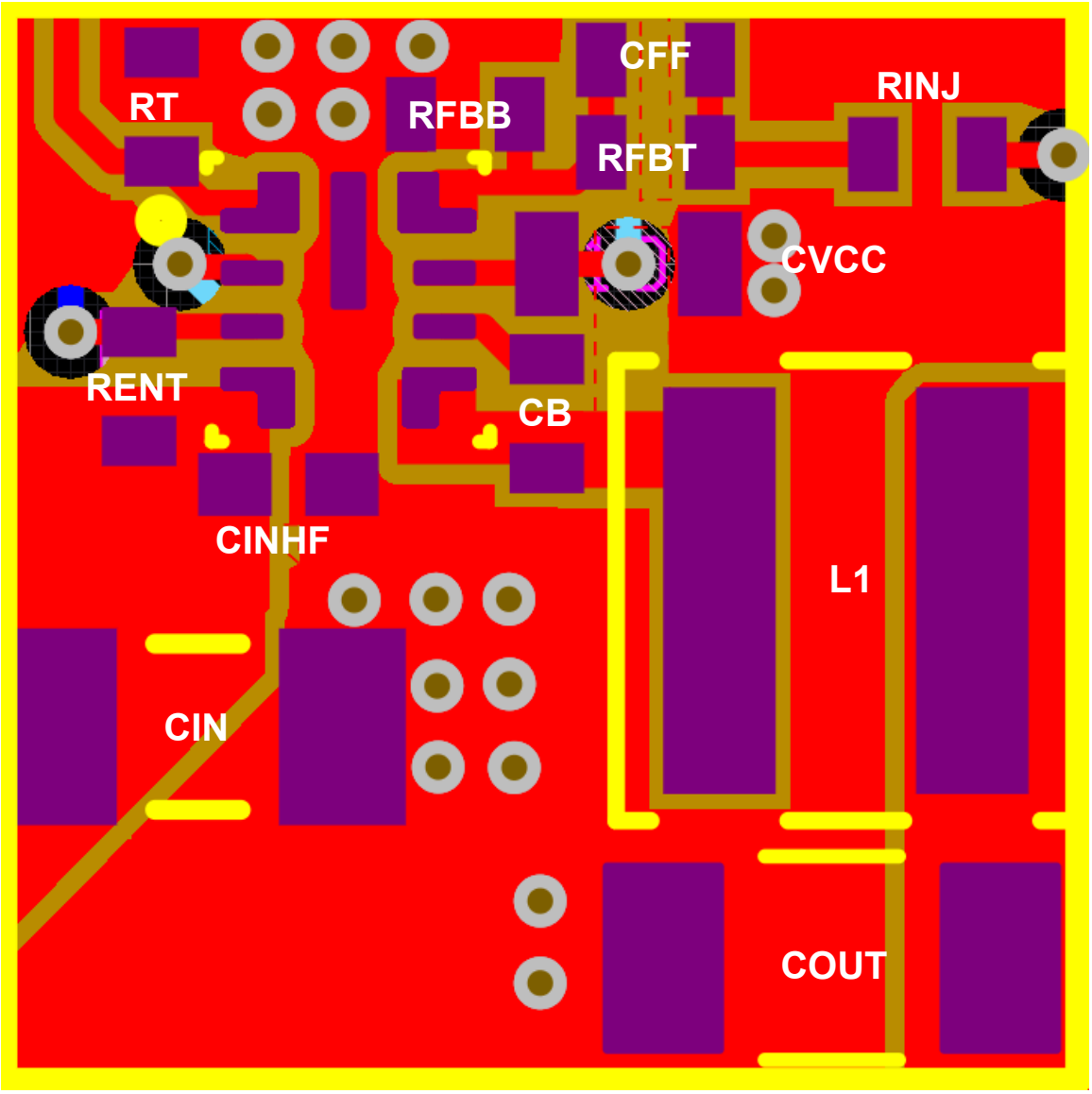


Figure 8-29. Example Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.1.2 Device Nomenclature

Figure 9-1 shows the device naming nomenclature of the LMR43606-Q1-Q1. See Section 4 for the availability of each variant. Contact TI sales representatives or on TI's E2E™ support forum for detail and availability of other options; minimum order quantities apply.

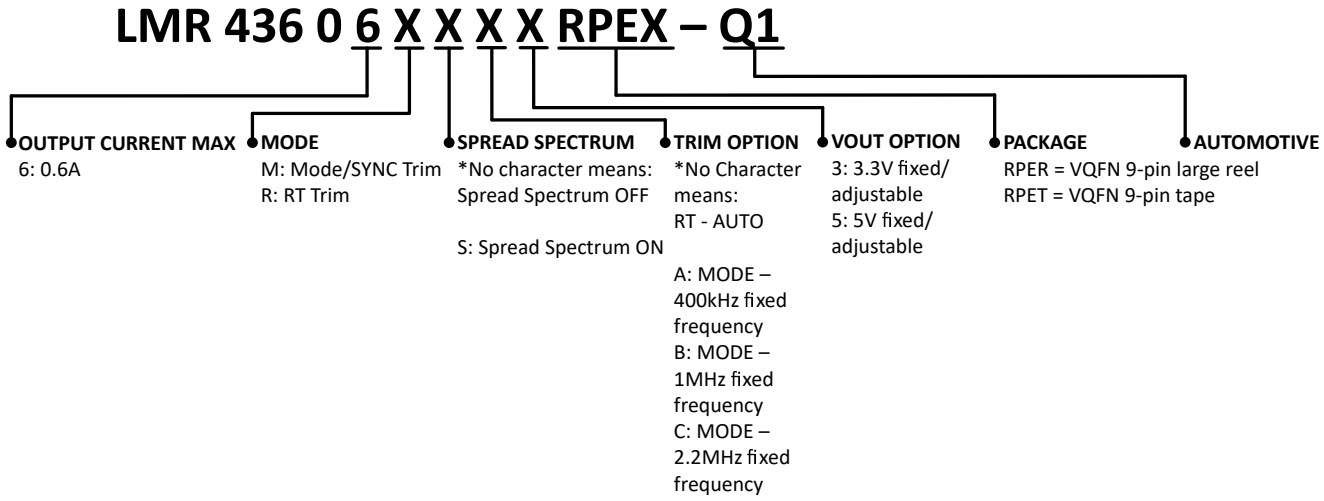


Figure 9-1. Device Naming Nomenclature

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feedforward Capacitor* application report
- Texas Instruments, *Thermal Design by Insight not Hindsight* application report
- Texas Instruments, *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *Thermal Design Made Simple with LM43603 and LM43602* application report
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package Application Report*
- Texas Instruments, *PowerPAD™ Made Easy* application report
- Texas Instruments, *Using New Thermal Metrics* application report
- Texas Instruments, *Layout Guidelines for Switching Power Supplies* application report
- Texas Instruments, *Simple Switcher PCB Layout Guidelines* application report
- Texas Instruments, *Construction Your Power Supply- Layout Considerations* seminar
- Texas Instruments, *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x* application report
- Texas Instruments, *AN-2162 Simple Success With Conducted EMI From DC/DC Converters* application report

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

HotRod™, PowerPAD™, and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMR43606MSC3RPERQ1	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	6M3Q
LMR43606MSC3RPERQ1.A	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	6M3Q
LMR43606MSC5RPERQ1	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	6M5Q
LMR43606MSC5RPERQ1.A	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	6M5Q
LMR43606RS3RPERQ1	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	6R3Q
LMR43606RS3RPERQ1.A	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	6R3Q
LMR43606RS5RPERQ1	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	6R5Q
LMR43606RS5RPERQ1.A	Active	Production	VQFN-HR (RPE) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	6R5Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

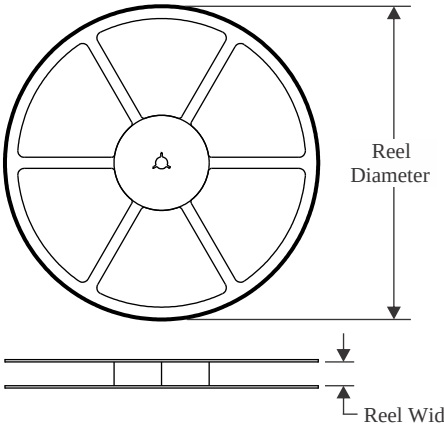
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

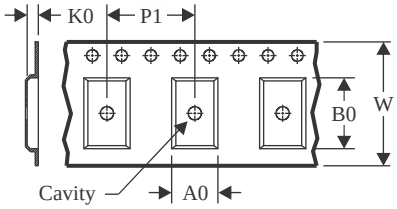
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

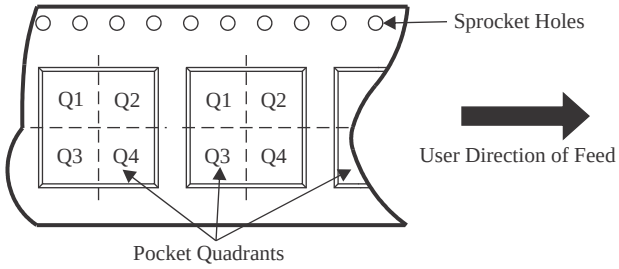


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

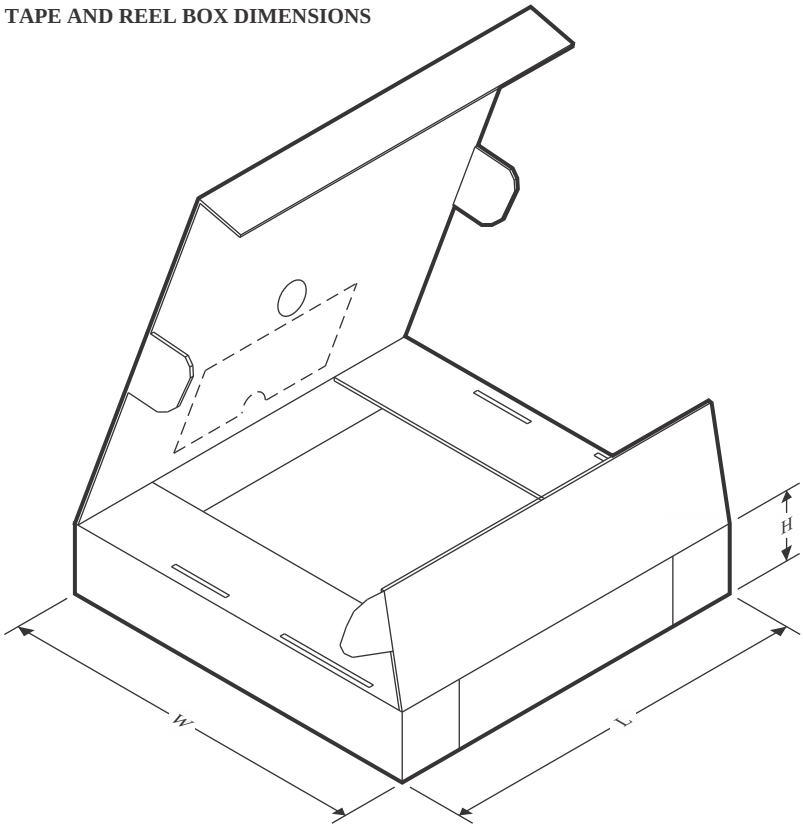
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR43606MSC3RPERQ1	VQFN-HR	RPE	9	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
LMR43606MSC5RPERQ1	VQFN-HR	RPE	9	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
LMR43606RS3RPERQ1	VQFN-HR	RPE	9	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
LMR43606RS5RPERQ1	VQFN-HR	RPE	9	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR43606MSC3RPERQ1	VQFN-HR	RPE	9	3000	213.0	191.0	35.0
LMR43606MSC5RPERQ1	VQFN-HR	RPE	9	3000	213.0	191.0	35.0
LMR43606RS3RPERQ1	VQFN-HR	RPE	9	3000	213.0	191.0	35.0
LMR43606RS5RPERQ1	VQFN-HR	RPE	9	3000	213.0	191.0	35.0

GENERIC PACKAGE VIEW

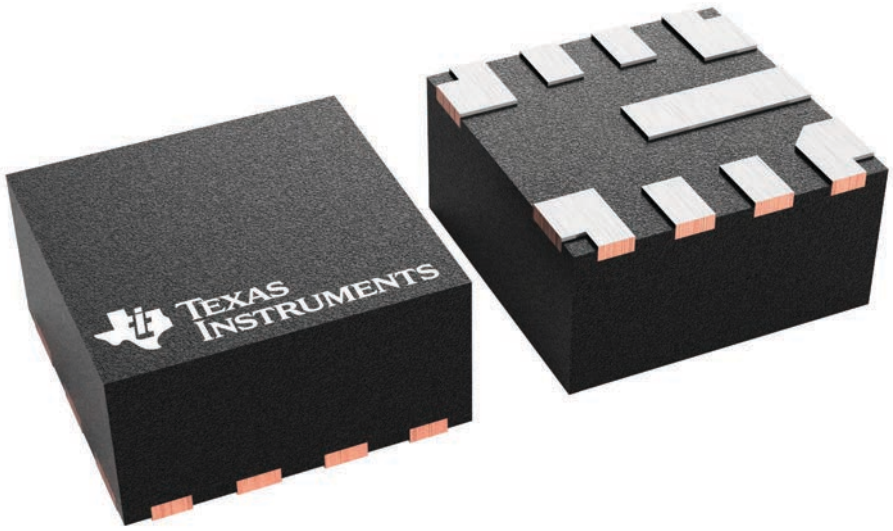
RPE 9

VQFN-HR - 1.0 mm max height

2 x 2, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



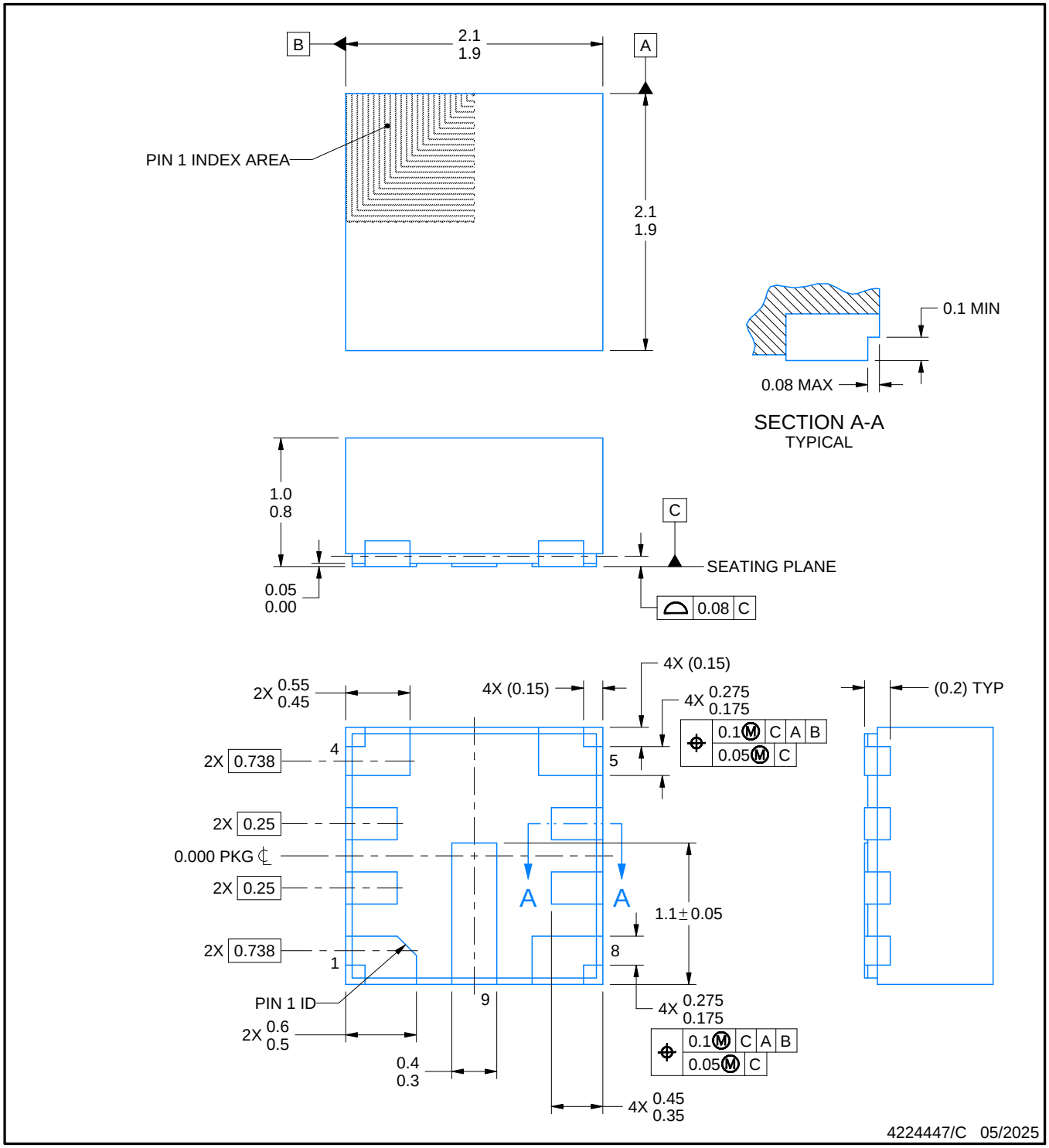
4227057/A

PACKAGE OUTLINE

RPE0009A

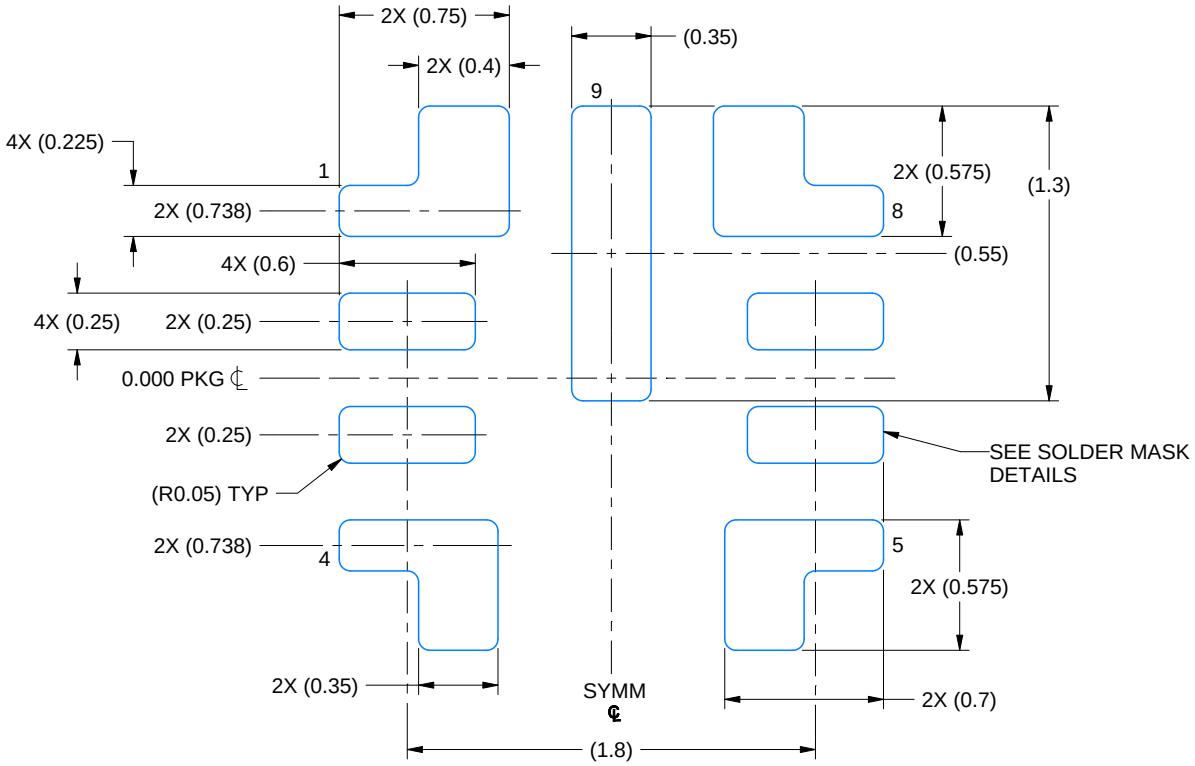
VQFN-HR - 1.0 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

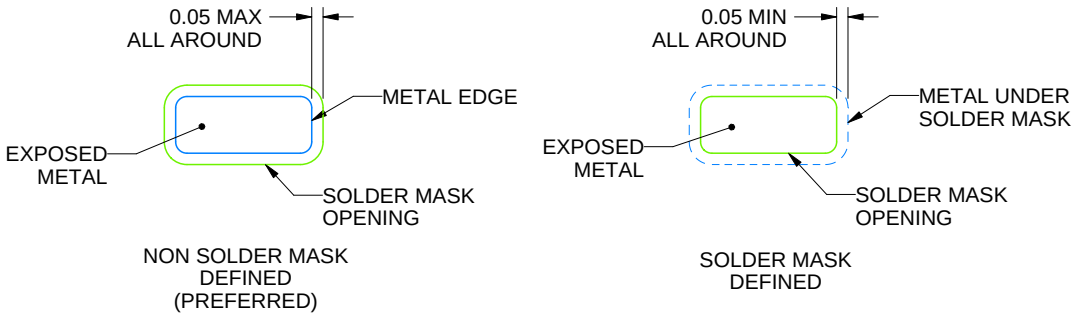


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

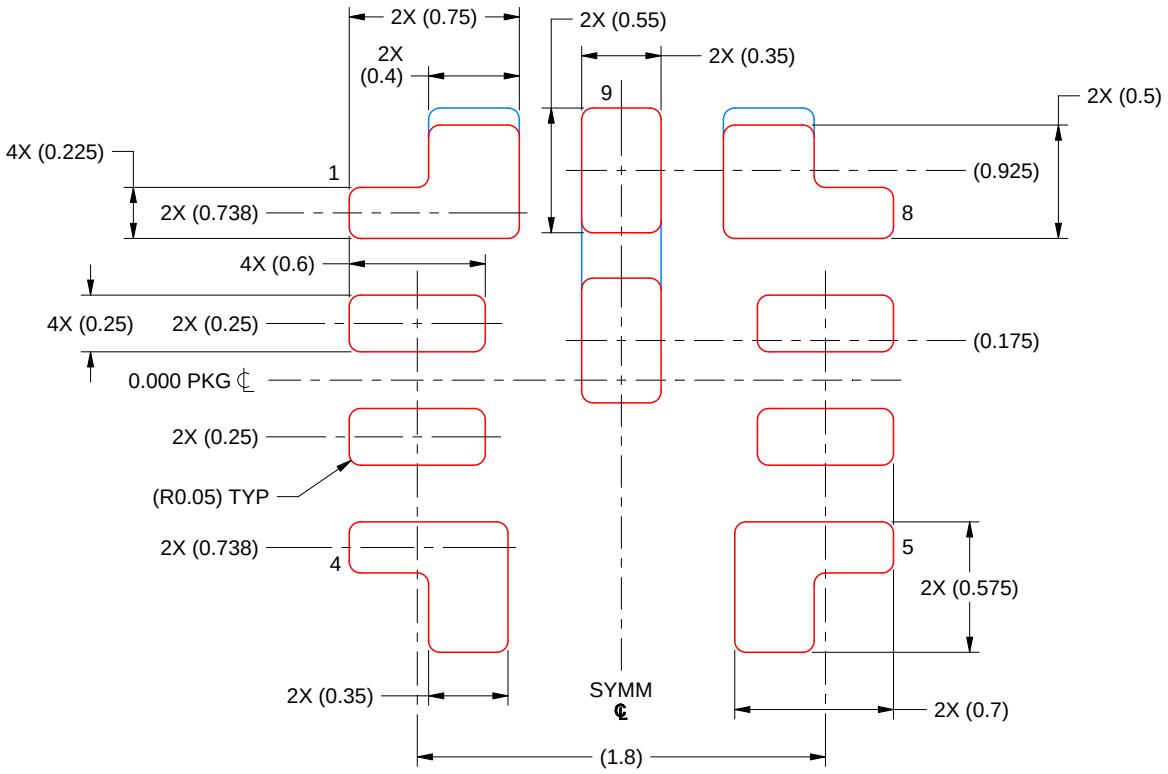


SOLDER MASK DETAILS

4224447/C 05/2025

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

PADS 1 & 8:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 9:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

DWG_NO:5/REV:5 MM_YYYY:5

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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