











SNAS517E - NOVEMBER 2011 - REVISED SEPTEMBER 2015

LMP91050

# LMP91050 Configurable AFE for Nondispersive Infrared (NDIR) Sensing Applications

#### **Features**

- Programmable Gain Amplifier
- Dark Signal Offset Cancellation
- Supports External Filtering
- Common-Mode Generator and 8-Bit DAC
- **Key Specifications** 
  - Programmable Gain 167 to 7986 V/V
  - Low Noise (0.1 to 10 Hz) 0.1 µVRMS
  - Gain Drift 100 ppm/°C (Maximum)
  - Phase Delay Drift 500 ns (Maximum)
  - Power Supply Voltage Range 2.7 to 5.5 V

## Applications

- **NDIR Sensing**
- **Demand Control Ventilation**
- **Building Monitoring**
- CO2 Cabin Control Automotive
- Alcohol Detection Automotive
- Industrial Safety and Security
- GHG and Freons Detection Platforms

## 3 Description

The LMP91050 device is a programmable integrated Sensor Analog Front End (AFE) optimized for thermopile sensors, as typically used in NDIR applications. It provides a complete signal path solution between a sensor and microcontroller that generates an output voltage proportional to the thermopile voltage. The programmability of the LMP91050 enables it to support multiple thermopile sensors with a single design as opposed to the multiple discrete solutions.

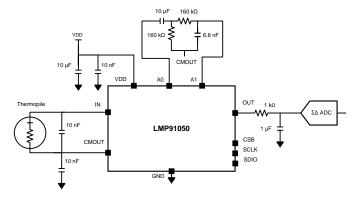
The LMP91050 features a programmable gain amplifier (PGA), dark phase offset cancellation, and an adjustable common-mode generator (1.15 V or 2.59 V) which increases output dynamic range. The PGA offers a low-gain range of 167 V/V to 1335 V/V plus a high-gain range of 1002 V/V to 7986 V/V which enables the user to use thermopiles with different sensitivities. The PGA is highlighted by low-gain drift (100 ppm/°C), output offset drift (1.2 mV/°C at G = 1002 V/V), phase delay drift (500 ns) and noise specifications (0.1  $\mu V_{RMS}$  0.1 to 10Hz).

## Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)		
LMP91050	VSSOP (10)	3.00 mm × 3.00 mm		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

## Typical Application Circuit



Configurable AFE for NDIR



## **Table of Contents**

1	Features 1		8.3 Feature Description	12
2	Applications 1		8.4 Device Functional Modes	14
3	Description 1		8.5 Programming	14
4	Revision History2		8.6 Register Maps	16
5	Description (continued)3	9	Application and Implementation	18
6	Pin Configuration and Functions		9.1 Application Information	18
-	_		9.2 Typical Application	18
7	Specifications	10	Power Supply Recommendations	21
	7.2 ESD Ratings	11	Layout	21
	7.3 Recommended Operating Conditions		11.1 Layout Guidelines	21
	7.4 Thermal Information		11.2 Layout Example	21
	7.5 Electrical Characteristics	12	Device and Documentation Support	22
	7.6 SPI Interface		12.1 Community Resources	22
	7.7 Timing Characteristics		12.2 Trademarks	22
	7.8 Typical Characteristics		12.3 Electrostatic Discharge Caution	22
8	Detailed Description		12.4 Glossary	
•	8.1 Overview	13	Mechanical, Packaging, and Orderable	20
	8.2 Functional Block Diagram		Information	22

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

## Changes from Revision D (March 2013) to Revision E

Page

Product Folder Links: LMP91050

## Changes from Revision C (April 2012) to Revision D

Page

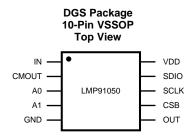


## 5 Description (continued)

The offset cancellation circuitry compensates for the *dark signal* by adding an equal and opposite offset to the input of the second stage, thus removing the original offset from the output signal. This offset cancellation circuitry allows optimized usage of the ADC full scale and relaxes ADC resolution requirements.

The LMP91050 allows extra signal filtering (high-pass, lowpass or bandpass) through dedicated pins A0 and A1, in order to remove out of band noise. The user can program through the on board SPI interface. Available in a small form factor 10-pin package, the LMP91050 operates from -40 to 105°C.

## 6 Pin Configuration and Functions



**Pin Functions** 

PIN		TYPE	DESCRIPTION		
NO.	NAME	ITPE	DESCRIPTION		
1	IN	Analog Input	Signal Input		
2	CMOUT	Analog Output	Common-Mode Voltage Output		
3	A0	Analog Output	First Stage Output		
4	A1	Analog Input	Second Stage Input		
5	GND	Power	Ground		
6	OUT	Analog Output	Signal Output, reference to the same potential as CMOUT		
7	CSB	Digital Input	Chip Select, active low		
8	SCLK	Digital Input	Interface Clock		
9	SDIO	Digital Input / Output	Serial Data Input / Output		
10	VDD	Power	Positive Supply		

## 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)(3)

	MIN	MAX	UNIT
Supply Voltage (VDD)	-0.3	6	V
Voltage at Any Pin	-0.3	VDD + 0.3	V
Input Current at Any Pin		5	mA
Junction Temperature <sup>(4)</sup>		150	°C
Storage Temperature, T <sub>stq</sub>	-65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) For soldering specifications: see product folder at www.ti.com and SNOA549.
- (4) The maximum power dissipation is a function of TJ(MAX), θJA, and the ambient temperature, TA. The maximum allowable power dissipation at any ambient temperature is PDMAX = (TJ(MAX) TA)/ θJA All numbers apply for packages soldered directly onto a PC board.



## 7.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1250	V
		Machine Model	±250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
Supply Voltage	2.7	5.5	V
Junction Temperature (2)	-40	105	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The maximum power dissipation is a function of  $T_{J(MAX)}$ ,  $\theta_{JA}$ , and the ambient temperature, TA. The maximum allowable power dissipation at any ambient temperature is  $P_{DMAX} = (T_{J(MAX)} T_A)/\theta_{JA}$  All numbers apply for packages soldered directly onto a PC board.

#### 7.4 Thermal Information

		LMP91050	
	THERMAL METRIC <sup>(1)</sup>		UNIT
		10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	176	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

#### 7.5 Electrical Characteristics

The following specifications apply for VDD = 3.3 V, VCM = 1.15 V, unless otherwise specified. All other limits apply to  $T_A = T_J = +25^{\circ}C$ . (1)

	PARAMETER	TEST CONDITIONS	MIN <sup>(2)</sup>	TYP <sup>(3)</sup>	MAX <sup>(2)</sup>	UNIT
POWER	SUPPLY		1			
VDD	Supply voltage		2.7	3.3	5.5	V
IDD	Supply current	All analog block ON	3.1	3.7	4.2	mA
	Power-down supply current	All analog block OFF	45	85	121	μΑ
OFFSET	CANCELLATION (OFFSET DAG	<del>(</del> )				
	Resolution			256		steps
	LSB	All gains		33.8		mV
	DNL		-1		2	LSB
	Error	Output referred offset error, all gains		±100		mV
	Offset adjust range	Output referred, all gains	0.2		VDD - 0.2	V
	DAC settling time			480		μs
PROGRA	AMMABLE GAIN AMPLIFIER (PO	GA) 1ST STAGE, $R_L = 10 \text{ k}\Omega$ , $C_L = 15 \text{ pF}$			<u> </u>	
				5		
IBIAS	Bias current	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$			200	рΑ

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T<sub>J</sub> = T<sub>A</sub>. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T<sub>J</sub> > T<sub>A</sub>. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
- (2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
- (3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.



## **Electrical Characteristics (continued)**

The following specifications apply for VDD = 3.3 V, VCM = 1.15 V, unless otherwise specified. All other limits apply to  $T_A = T_J = +25^{\circ}C.^{(1)}$ 

	PARAMETER	TEST CONDITIONS	MIN <sup>(2)</sup>	TYP <sup>(3)</sup>	MAX <sup>(2)</sup>	UNIT
VINMAX _HGM	Max input signal high-gain mode	Referenced to CMOUT voltage, it refers to the maximum voltage at the IN pin		±2		mV
VINMAX _LGM	Max input signal low-gain mode	before clipping; It includes dark voltage of the thermopile and signal voltage.		±12		mV
VOS	Input offset voltage			-165		μV
G _HGM	Gain high-gain mode			250		V/V
G_LGM	Gain low-gain mode			42		V/V
GE	Gain error	Both HGM and LGM		2.5%		
VOUT	Output voltage range		0.5		VDD - 0.5	V
PhDly	Phase delay	1-mV input step signal, HGM, V <sub>OUT</sub> measured at Vdd/2		6		μs
TCPhDly	Phase delay variation with temperature	1-mV input step signal, HGM, V <sub>OUT</sub> measured at Vdd/2,		416		ns
SSBW	Small signal bandwidth	Vin = 1mVpp, Gain = 250 V/V		18		kHz
Cin	Input capacitance			100		pF
PROGRAI	MABLE GAIN AMPLIFIER (PG	A) 2ND STAGE, $R_S = 1 \text{ k}\Omega$ , $C_L = 1 \mu\text{F}$			<u>,                                    </u>	
VINMAX	Max input signal	GAIN = 4 V/V		1.65		V
VINMIN	Min input signal			0.82		V
G	Gain	Programmable in 4 steps	4		32	V/V
GE	Gain error	Any gain		2.5		%
VOUT	Output voltage range		0.2		VDD - 0.2	V
PhDly	Phase delay	100-mV input sine 35-kHz signal, Gain = 8, V <sub>OUT</sub> measured at 1.65 V, R <sub>L</sub> = 10 kΩ		1		μs
TCPhDly	Phase delay variation with temperature	250-mV input step signal, Gain = 8, V <sub>OUT</sub> measured at Vdd/2		84		ns
SSBW	Small signal bandwidth	Gain = 32 V/V		360		kHz
Cin	Input capacitance			5		pF
CLOAD, OUT	OUT pin load capacitance	Series RC		1		μF
RLOAD, OUT	OUT pin load resistance	Series RC		1		kΩ
COMBINE	D AMPLIFIER CHAIN SPECIFIC	ATION				
en	Input-referred noise density	Combination of both current and voltage noise, with a 86kΩ source impedance at 5Hz, Gain = 7986		30		nV/√ <del>Hz</del>
	Input-referred integrated noise	Combination of both current and voltage noise, with a 86kΩ source impedance 0.1Hz to 10Hz, Gain = 7986		0.1	0.12 <sup>(4)</sup>	μVrms
		PGA1 GAIN = 42, PGA2 GAIN = 4		167		
		PGA1 GAIN = 42, PGA2 GAIN = 8		335		
		PGA1 GAIN = 42, PGA2 GAIN = 16		669		
0	Onin	PGA1 GAIN = 42, PGA2 GAIN = 32		1335		1/0/
G	Gain	PGA1 GAIN = 250, PGA2 GAIN = 4		1002		V/V
		PGA1 GAIN = 250, PGA2 GAIN = 8		2004		
		PGA1 GAIN = 250, PGA2 GAIN = 16		4003		
		PGA1 GAIN = 250, PGA2 GAIN = 32		7986		
GE	Gain error	Any gain		5%		
		<u> </u>				

<sup>(4)</sup> Specified by design and characterization. Not tested on shipped production material.

Submit Documentation Feedback



## **Electrical Characteristics (continued)**

The following specifications apply for VDD = 3.3 V, VCM = 1.15 V, unless otherwise specified. All other limits apply to  $T_A = T_J = +25^{\circ}C.^{(1)}$ 

	PARAMETER	TEST CONDITIONS	MIN <sup>(2)</sup>	TYP <sup>(3)</sup>	MAX <sup>(2)</sup>	UNIT
TCCGE	Gain temp coefficient (5)	$T_A = -40$ °C to +85°C			100	ppm/°C
PSRR	Power supply rejection ratio	DC, 3-V to 3.6-V supply, gain = 1002 V/V	90	110		dB
PhDly	Phase delay	1-mV input step signal, Gain = 1002, V <sub>OUT</sub> measured at Vdd/2		9		μs
TCPhDly	Phase delay variation with temperature <sup>(6)</sup>	1-mV input step signal, Gain=1002, V <sub>OUT</sub> measured at Vdd/2, T <sub>A</sub> = -40°C to +85°C			500	ns
		Gain = 167 V/V, T <sub>A</sub> = -40°C to +85°C	-0.525		0.525	
	OS Output offset voltage temperature drift <sup>(5)</sup>	Gain = 335 V/V, $T_A = -40^{\circ}\text{C}$ to +85°C	-0.6		0.6	mV/°C
		Gain = 669 V/V, $T_A = -40^{\circ}\text{C}$ to +85°C	-0.9		0.9	
TCVOS		Gain = 1335 V/V, $T_A = -40$ °C to +85°C	-1.5		1.5	
10005		Gain = 1002 V/V, $T_A = -40^{\circ}\text{C}$ to +85°C	-1.2		1.2	
		Gain = 2004 V/V, $T_A = -40$ °C to +85°C	-1.9		1.9	
		Gain = 4003 V/V, $T_A = -40$ °C to +85°C	-3.7		3.7	
		Gain = $7986V/V$ , $T_A = -40$ °C to $+85$ °C	-7.1		7.1	
COMMON	-MODE GENERATOR					
VCM	Common-mode voltage	Programmable, see Common-Mode Generation		1.15 or 2.59		V
	VCM accuracy			2%		
CLOAD	CMOut load capacitance			10		nF

<sup>(5)</sup> TCCGE and TCVOS are calculated by taking the largest slope between -40°C and 25°C linear interpolation and 25°C and 85°C linear interpolation.

## 7.6 SPI Interface

The following specifications apply for VDD = 3.3 V, VCM = 1.15 V,  $C_L$  = 15 pF, unless otherwise specified. All other limits apply to  $T_A = T_J = +25$ °C. (1)

	PARAMETER	TEST CONDITIONS	MIN <sup>(2)</sup>	TYP <sup>(3)</sup> MAX <sup>(2)</sup>	UNIT
$V_{IH}$	Logic input high		0.7 × VDD		V
$V_{IL}$	Logic input low			0.8	V
$V_{OH}$	Logic output high		2.6		V
$V_{OL}$	Logic output low			0.4	V
111 1/111	Input digital lackage current		-100	100	~ ^
IIH/IIL	Input digital leakage current	$T_A = -40$ °C to +85°C	-200	200	nA

<sup>(1)</sup> Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T<sub>J</sub> = T<sub>A</sub>. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T<sub>J</sub> > T<sub>A</sub>. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

#### 7.7 Timing Characteristics

The following specifications apply for VDD = 3.3 V, VCM = 1.15 V,  $C_L$  = 15 pF, unless otherwise specified. All other limits apply to  $T_A = T_J = +25$ °C. (1)

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T<sub>J</sub> = T<sub>A</sub>. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T<sub>J</sub> > T<sub>A</sub>. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

<sup>(6)</sup> TCPhDly is largest change in phase delay between -40°C and 25°C measurements and 25°C and 85°C measurements.

<sup>(2)</sup> Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

<sup>(3)</sup> Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.



## **Timing Characteristics (continued)**

The following specifications apply for VDD = 3.3 V, VCM = 1.15 V,  $C_L$  = 15 pF, unless otherwise specified. All other limits apply to  $T_A = T_J = +25$ °C.<sup>(1)</sup>

	PARAMETER	TEST CONDITIONS	MIN <sup>(2)</sup>	TYP <sup>(3)</sup>	MAX <sup>(2)</sup>	UNIT
t <sub>WU</sub>	Wake-up time			1		ms
f <sub>SCLK</sub>	Serial clock frequency				10	MHz
t <sub>PH</sub>	SCLK pulse width high		0.4 / f <sub>SCLK</sub>			ns
t <sub>PL</sub>	SCLK pulse width low		0.4 / f <sub>SCLK</sub>			ns
t <sub>CSS</sub>	CSB set-up time		10			ns
t <sub>CSH</sub>	CSB hold time		10			ns
t <sub>SU</sub>	SDI set-up time prior to rise edge of SCLK		10			ns
t <sub>SH</sub>	SDI hold time prior to rise edge of SCLK		10			ns
t <sub>DOD1</sub>	SDO disable time after rise edge of CSB				45	ns
t <sub>DOD2</sub>	SDO disable time after 16 <sup>th</sup> rise edge of SCLK				45	ns
t <sub>DOE</sub>	SDO enable time from the fall edge of 8 <sup>th</sup> SCLK				35	ns
t <sub>DOA</sub>	SDO access time after the fall edge of SCLK				35	ns
t <sub>DOH</sub>	SDO hold time after the fall edge of SCLK		5			ns
t <sub>DOR</sub>	SDO rise time			5		ns
t <sub>DOF</sub>	SDO fall time			5		ns

- (2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
- (3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

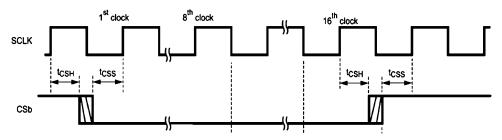


Figure 1. SPI Timing Diagram

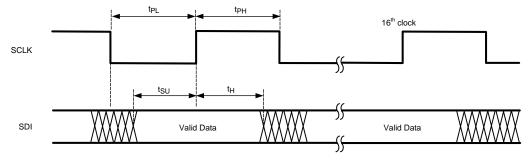


Figure 2. SPI Set-Up Hold Time



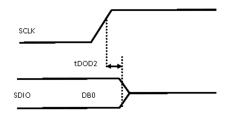


Figure 3. SDO Disable Time After 16<sup>th</sup> Rise Edge of SCLK

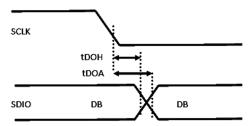


Figure 4. SDO Access Time ( $t_{DOA}$ ) and SDO Hold Time ( $t_{DOH}$ ) After the Fall Edge of SCLK

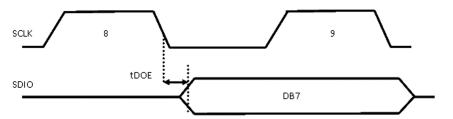


Figure 5. SDO Enable Time from the Fall Edge of  $8^{th}$  SCLK

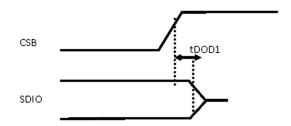


Figure 6. SDO Disable Time after Rise Edge of CSB

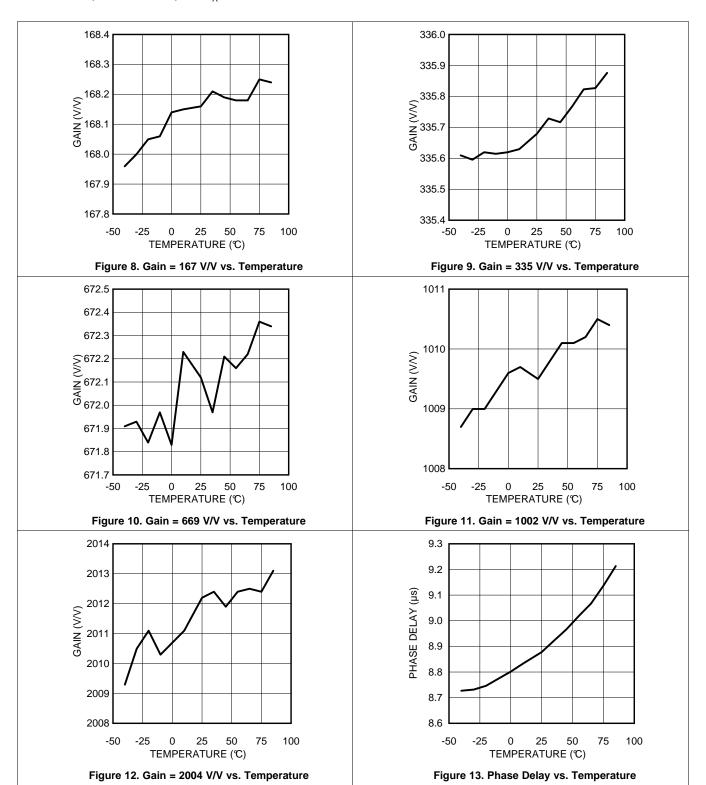


Figure 7. SDO Rise and Fall Times



## 7.8 Typical Characteristics

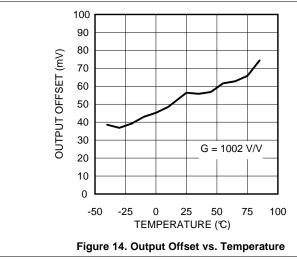
VDD = +3.3 V, VCM = 1.15 V, and  $T_A$  = 25°C unless otherwise noted



# TEXAS INSTRUMENTS

## **Typical Characteristics (continued)**

VDD = +3.3 V, VCM = 1.15 V, and  $T_A = 25$ °C unless otherwise noted



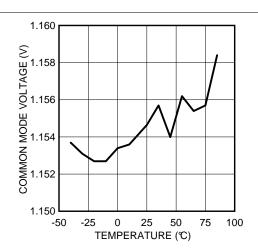


Figure 15. Common-Mode Voltage vs. Temperature

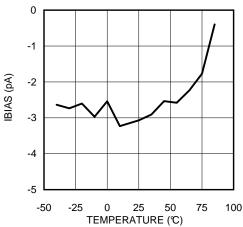


Figure 16. Input Bias Current vs. Temperature

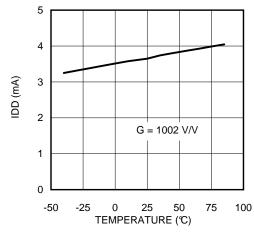
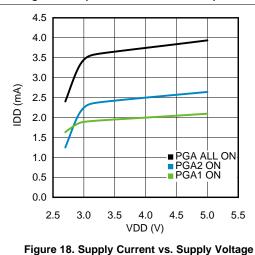


Figure 17. Supply Current vs. Temperature





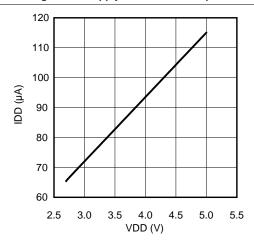


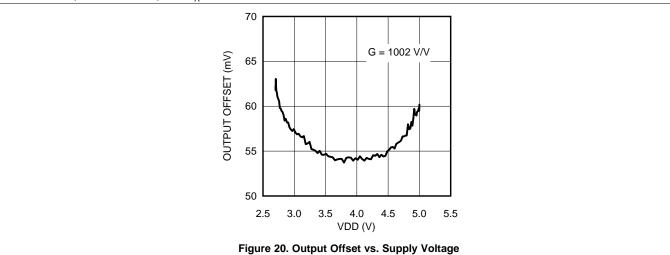
Figure 19. Power-Down Supply Current vs. Supply Voltage

Submit Documentation Feedback



## **Typical Characteristics (continued)**

VDD = +3.3 V, VCM = 1.15 V, and  $T_A = 25$ °C unless otherwise noted





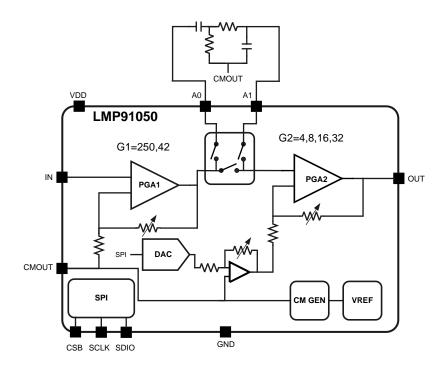
## 8 Detailed Description

#### 8.1 Overview

The input channel of the LMP91050 features two programmable gain stages that give the user flexibility in optimizing the system gain. Access to the inter-stage connection between the gain blocks also allows the inclusion of appropriate filtering if needed. The internal DAC allows the DC offset of the output voltage to be adjusted independently of the common-mode voltage supplied to the sensor, enabling the sampled signal to be centered within the ADC full-scale input range.

The following paragraphs discuss the LMP91050's features in more detail.

## 8.2 Functional Block Diagram



#### 8.3 Feature Description

## 8.3.1 Programmable Gain Amplifier

The LMP91050 offers two programmable gain modes (low or high) with four programmable gain settings each. The purpose of the gain mode is to enable thermopiles with larger dark voltage levels. All gain settings are accessible through bits GAIN1 and GAIN2[1:0]. The low-gain mode has a range of 167 V/V to 1335 V/V while the high-gain mode has a range of 1002 V/V to 7986 V/V. The PGA is referenced to the internally generated VCM. Input signal, referenced to this VCM voltage, should be within ±2 mV (see VINMAX\_HGM specification) in high-gain mode. In the low gain mode the first stage will provide a gain of 42 V/V instead of 250 V/V, thus allowing a larger maximum input signal up to ±12 mV (VINMAX\_LGM).

Table 1. Gain Modes

BIT SYMBOL	GAIN
CAINIA	0: 250 (default)
GAIN1	1: 42



## **Feature Description (continued)**

**Table 1. Gain Modes (continued)** 

BIT SYMBOL	GAIN					
	00: 4 (default)					
CAING [4:0]	01: 8					
GAIN2 [1:0]	10: 16					
	11: 32					

#### 8.3.2 External Filter

The LMP91050 offers two different measurement modes selectable through EXT\_FILT bit. EXT\_FILT bit is present in the Device configuration register and is programmable through SPI.

**Table 2. Measurement Modes** 

BIT SYMBOL	MEASUREMENT MODE
EXT_FILT	0: The signal from the thermopile is being processed by the internal PGAs, without additional external decoupling or filtering (default).
	1: The signal from the thermopile is being processed by the first internal PGA and fed to the A0 pin. An external low pass, high pass or band pass filter can be connected through pins A0, A1.

An external filter can be applied when EXT\_FILT = 1. A typical band pass filter is shown in the picture below. Resistor and capacitor can be connected to the CMOUT pin of the LMP91050 as shown. Discrete component values have been added for reference.

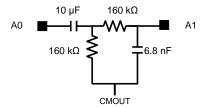


Figure 21. Typical Bandpass Filter

#### 8.3.3 Offset Adjust

Procedure of the offset adjust is to first measure the *dark signal*, program the DAC to adjust, and then measure in a second cycle the residual of the dark signal for further signal manipulation within the  $\mu$ C. The signal source is expected to have an offset component (dark signal) larger than the actual signal. During the *dark phase*, the time when no light is detected by the sensor, the  $\mu$ C can program LMP91050 internal DAC to compensate for a measured offset. A low output offset voltage temperature drift (TCVOS) ensures system accuracy over temperature. See Figure 22 below which plots the maximum TCVOS allowed over a given temperature drift in order to achieve n bit system accuracy.

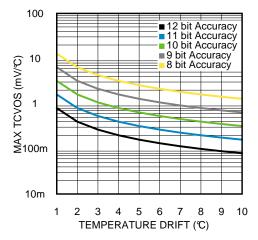


Figure 22. System Accuracy vs. TCVOS and Temperature Drift

#### 8.3.4 Common-Mode Generation

As the offset of the sensor is bipolar, there is a need to supply a VCM to the sensor. This can be programmed as 1.15 V or 2.59 V (approximately mid rail of 3.3-V or 5-V supply). TI does not recommend to use 2.59-V VCM with a 3.3-V supply

#### 8.3.5 CSB

Chip Select is a active-low signal. CSB needs to be asserted throughout a transaction. That is, CSB should not pulse between the Instruction Byte and the Data Byte of a single transaction.

#### **NOTE**

CSB de-assertion always terminates an on-going transaction, if it is not already complete. Likewise, CSB assertion will always bring the device into a state, ready for next transaction, regardless of the termination status of a previous transaction.

CSB may be permanently tied low for a 2-wire SPI communication protocol.

#### 8.3.5.1 SCLK

SCLK can idle High or Low for a write transaction. However, for a READ transaction, SCLK must idle high. SCLK features a Schmitt-triggered input and although it has hysterisis, TI recommends to keep SCLK as clean as possible to prevent glitches from inadvertently spoiling the SPI frame.

#### 8.4 Device Functional Modes

To read the registers of the LMP91050, the SDIO mode enable register must be written using a special sequence, as described in the SDIO Mode section. During the reading process, the analog OUT pin is still active, as normal. There are no other special modes for the device.

## 8.5 Programming

#### 8.5.1 SPI Interface

An SPI interface is available in order to program the device parameters like PGA gain of two stages, enabling external filter, enabling power for PGAs, offset adjust and common-mode (VCM) voltage.

#### 8.5.1.1 Interface Pins

The Serial Interface consists of SDIO (Serial Data Input / Output), SCLK (Serial Interface Clock) and CSB (Chip Select Bar). The serial interface is write-only by default. Read operations are supported after unlocking the SDIO\_MODE\_PASSWD. This is discussed in detail later in the document.



## **Programming (continued)**

#### 8.5.1.2 Communication Protocol

Communication on the SPI normally involves Write and Read transactions. Write transaction consists of single Write Command Byte, followed by single Data byte. The following figure shows the SPI Interface Protocol for write transaction.

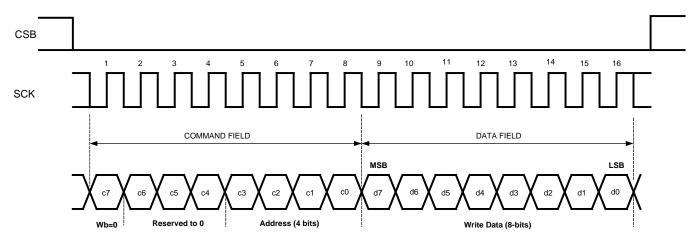
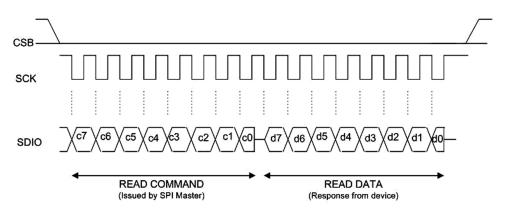


Figure 23. SPI Interface Protocol

For Read transactions, user first needs to write into a SDIO mode enable register for enabling the SPI read mode. Once the device is enabled for Reading, the data is driven out on the SDIO pin during the Data field of the Read Transaction. SDIO pin is designed as a bidirectional pin for this purpose. Figure 24 shows the Read transaction. The sequence of commands that need to be issued by the SPI Master to enable SPI read mode is shown in Figure 25.

#### READ TRANSACTION

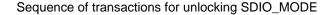


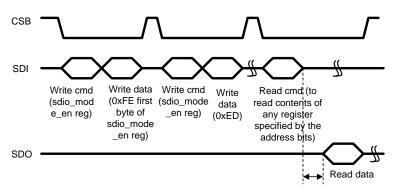
Note: Read command is issued by the SPI Master, who after issuing the c0 (LSBit of the command byte) bit should relinquish the data line (high-Z) after meeting the hold timing(10ns) and stop SCK idling high.

Figure 24. Read Transaction



## **Programming (continued)**





Bus turnaround time = half cycle

#### Note

- 1. Once the SDIO\_mode is unlocked. The user can read as many registers as long as nothing else is written to sdio mode en register to disturb the state of SDIO mode
- 2. The separate signals SDI and SDO are given in the figure for the sake of understanding. However, only one signal SDIO exists in the design

Figure 25. Enable SDIO Mode for Reading SPI Registers

## 8.5.1.3 Registers Organization

Configuring the device is achieved using Write of the designated registers in the device. All the registers are organized into individually addressable byte-long registers that have a unique address. The format of the Write/Read instruction is as shown below.

Table 3. Write / Read Instruction Format

Bit[7]	Bit[6:4]	Bit[3:0]			
0 : Write Instruction	Decemined to 0	Address			
1 : Read Instruction	Reserved to 0	Address			

## 8.6 Register Maps

This section describes the programmable registers and the associated programming sequence, if any, for the device. Table 4 shows the summary listing of all the registers that are available to the user and their power-up values.

**Table 4. Register Descriptions** 

Title	Address (Hex)	Туре	Power-up/Reset Value (Hex)	
Dovice Configuration	0.40	Read-Write	0v0	
Device Configuration	0x0	(Read allowed in SDIO Mode)	0x0	
DAC Configuration	04	Read-Write	020	
DAC Configuration	0x1	(Read allowed in SDIO Mode)	0x80	
SDIO Mode Enable	O Mode Enable 0xF Write-o		0x0	



## 8.6.1 Device Configuration

Table 5. Device Configuration Register (Address 0x0)

Bit	Bit Symbol	Description						
7	RESERVED	Reserved to 0.						
		00: PGA1 OFF PGA2 OFF (default)						
[6.5]	ΓN	01: PGA1 OFF, PGA2 ON						
[6:5]	EN	10: PGA1 ON, PGA2 OFF						
		11: PGA1 ON, PGA2 ON						
4	EVT EUT	0: PGA1 to PGA2 direct (default)						
4	EXT_FILT	1: PGA1 to PGA2 via external filter						
2	CMNI MODE	0 : 1.15V (default)						
3	CMN_MODE	1:2.59V						
	] GAIN2	00: 4 (default)						
[0.4]		01: 8						
[2:1]		10: 16						
		11: 32						
0	CAINIA	0: 250 (default)						
0	GAIN1	1: 42						

## 8.6.2 DAC Configuration

The output DC level will shift according to the formula Vout\_shift = -33.8mV \* (NDAC - 128).

Table 6. DAC Configuration Register (Address 0x1)

Bit	Bit Symbol	Description					
[7:0]	NDAC	128 (0x80): Vout_shift = -33.8mV * (128 - 128) = 0mV (default)					

## 8.6.3 SDIO Mode

Write-only

Table 7. SDIO Mode Enable Register (Address 0xf)

Bit	Bit Symbol	Description
[7.0]	CDIO MODE EN	To enter SDIO Mode, write the successive sequence 0xFE and 0xED.
[7:0]	SDIO_MODE_EN	Write anything other than this sequence to get out of mode.



## 9 Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

Figure 26 shows a typical NDIR sensing circuit with a bandpass filter with a high frequency cutoff of approximately 100 Hz. The lowpass filter at the output has a cutoff of approximately 110 Hz.

## 9.2 Typical Application

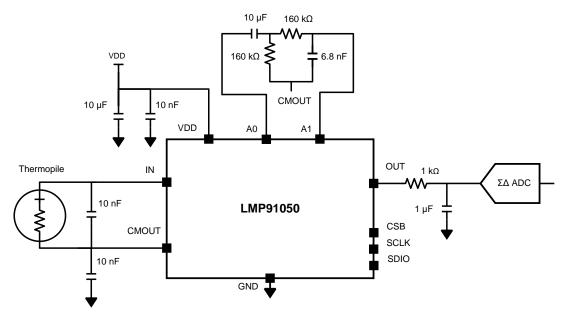


Figure 26. Typical NDIR Sensing Application Circuit

#### 9.2.1 Design Requirements

The design requirements for using the LMP91050 in an application basically include the following:

- Determine the characteristics of the thermopile and the appropriate gain and common mode voltage that will maximize the dynamic range of the sensor. Consult the manufacturer's data sheet.
- Selecting an analog-to-digital converter that supports the needed resolution and update rate.
- Determining the bandwidth of the inter-stage low-pass filter to limit the noise imposed on the signal
- An SPI interface to a microcontroller or other logic device is required in order to configure the LMP91050.

## 9.2.2 Detailed Design Procedure

The basic design procedure is as follows:

- Select the appropriate inter-stage bandpass filter bandwidth. Note that the common mode voltage (CMOUT) is connected to both the thermopile and the bandpass filter, as shown in Figure 26.
- TI recommends that a lowpass filter be inserted between the OUT pin and the input to the ADC, to further reduce noise on the signal and prevent aliasing.
- Power supply bypassing as shown in figure 32 is recommended.
- Based on the thermopile characteristics, select the common-mode voltage and gain to be programmed into the LMP91050. CMOUT should be selected to center the expected dynamic range of the thermopile within the full scale range of the ADC to the best extent possible. The gain should be selected to maximize the

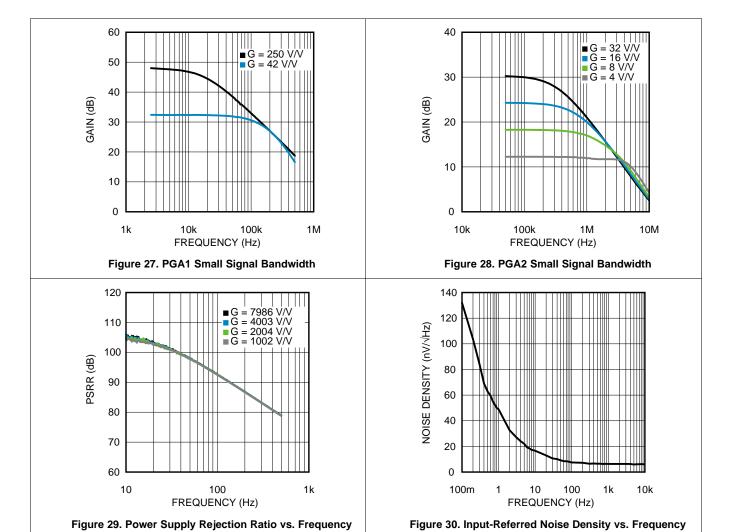


## **Typical Application (continued)**

signal range at the ADC input, but should allow some headroom below full scale to prevent clipping. The gain should also compensate, if possible, for any loss due to the filters in the signal path.

The internal DAC can be programmed to further optimize the signal range on the OUT pin. See Offset Adjust
for further information.

## 9.2.3 Application Curves

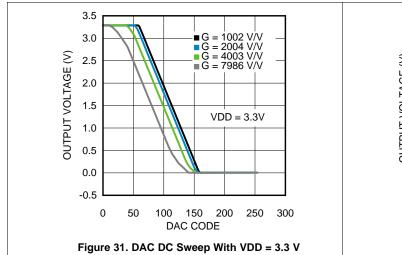


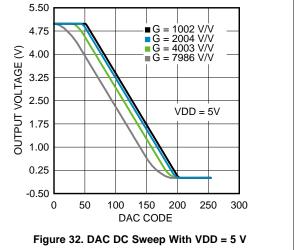
Copyright © 2011–2015, Texas Instruments Incorporated

Submit Documentation Feedback



# **Typical Application (continued)**







## 10 Power Supply Recommendations

Because the LMP91050 is used in a sampled data system, care must be taken to maintain power supply noise below an acceptable level, which will depend on the requirements of the application. In all cases, follow the manufacturer's design recommendations for the power conditioning device used in the system. The LMP91050 offers excellent power supply rejection over a wide range of frequencies, but adequate power supply bypassing should always be used (see Figure 26). If using a switching supply, additional filtering may be required particularly if the switcher harmonics fall within the passband of the filters used in the system. Ensure that the selected power conditioning device is capable of sourcing the current required by the LMP91050.

#### 11 Layout

## 11.1 Layout Guidelines

Figure 33 shows a layout example for the LMP91050. All components should be placed as close as possible to the device, especially the bypass capacitors to VDD (CBypass1 and CBypass2).

## 11.2 Layout Example

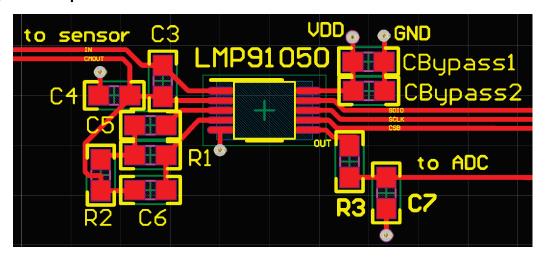


Figure 33. LMP91050 Layout Example

Product Folder Links: LMP91050

Copyright © 2011-2015, Texas Instruments Incorporated



## 12 Device and Documentation Support

## 12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 12.2 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

## 12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.4 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com 10-Nov-2025

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
LMP91050MM/NOPB	Obsolete	Production	VSSOP (DGS)   10	-	-	Call TI	Call TI	-40 to 105	AN8A
LMP91050MME/NOPB	Obsolete	Production	VSSOP (DGS)   10	-	-	Call TI	Call TI	-40 to 105	AN8A
LMP91050MMX/NOPB	Active	Production	VSSOP (DGS)   10	3500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	AN8A
LMP91050MMX/NOPB.A	Active	Production	VSSOP (DGS)   10	3500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	AN8A

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 20-Feb-2024

## TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP91050MMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

# PACKAGE MATERIALS INFORMATION

www.ti.com 20-Feb-2024



## \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
LMP91050MMX/NOPB	VSSOP	DGS	10	3500	356.0	356.0	35.0	



SMALL OUTLINE PACKAGE



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-187, variation BA.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025