LMC7111 Tiny CMOS Operational Amplifier With Rail-to-Rail Input and Output

1 Features

- Tiny 5-pin SOT-23 package saves space
- Very wide common-mode input range
- Specified at 2.7V, 5V, and 10V
- Typical supply current 25µA at 5V
- 50kHz gain-bandwidth at 5V
- Similar to popular LMC6462
- Output to within 20mV of supply rail at 100kΩ load
- Good capacitive load drive

2 Applications

- Mobile communications
- Portable computing
- Current sensing for battery chargers
- Voltage reference buffering
- Sensor interface
- Stable bias for GaAs RF amps

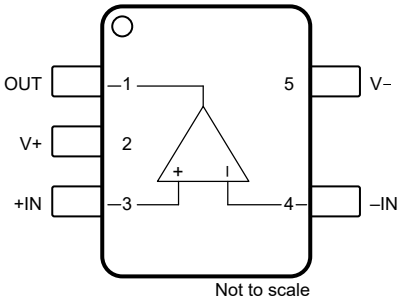
3 Description

The LMC7111 is a micropower CMOS operational amplifier available in the space-saving SOT-23 package. This package makes the LMC7111 an excellent choice for space- and weight-critical designs. The wide common-mode input range enables the design of battery-monitoring circuits that sense signals greater than the V+ supply. The main benefits of the tiny package are most apparent in small, portable, electronic devices, such as mobile phones, pagers, and portable computers. The tiny amplifiers can be placed on a board where needed, simplifying board layout.

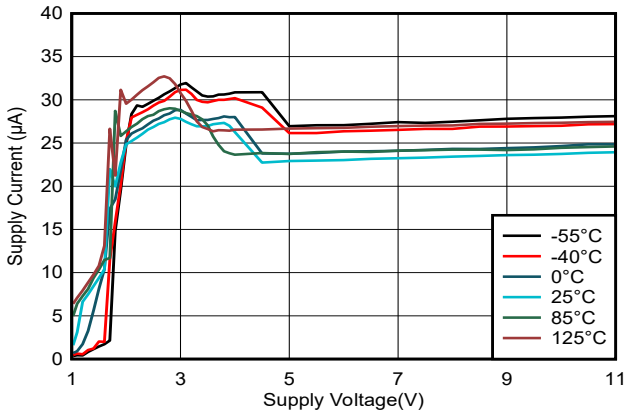
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LM7111	DBV (SOT-23, 5)	2.9mm × 2.8mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



DBV Package, 5-Pin SOT-23 (Top View)



Supply Current vs Supply Voltage

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Pin Configuration and Functions....2
5 Specifications....3
5.1 Absolute Maximum Ratings....3
5.2 ESD Ratings....3
5.3 Recommended Operating Conditions....3
5.4 Thermal Information....3
5.5 Electrical Characteristics for V_S = 2.7V or ±1.35V....4
5.6 Electrical Characteristics for V_S = 5V or ±2.5V....5
5.7 Electrical Characteristics for V_S = 10V or ±5V....6
5.8 Typical Characteristics....7
5.9 Typical Characteristics: 2.7V....7
5.10 Typical Characteristics: 3V....8
5.11 Typical Characteristics: 5V....9
5.12 Typical Characteristics: 10V....13
6 Detailed Description....15
6.1 Feature Description....15
7 Application and Implementation....16
7.1 Application Information....16
7.2 Typical Application....18
8 Device and Documentation Support....19
8.1 Device Support....19
8.2 Receiving Notification of Documentation Updates....19
8.3 Support Resources....19
8.4 Trademarks....19
8.5 Electrostatic Discharge Caution....19
8.6 Glossary....19
9 Revision History....19
10 Mechanical, Packaging, and Orderable Information....20

4 Pin Configuration and Functions

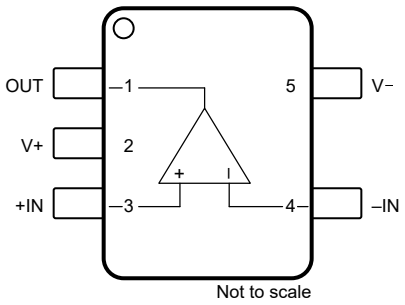


Figure 4-1. DBV Package, 5-Pin SOT-23 (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OUT	Output	Output
2	V+	Power	Positive supply
3	+IN	Input	Noninverting input
4	−IN	Input	Inverting input
5	V−	Power	Negative supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Differential input voltage		±Supply voltage	V
V_S	Supply voltage, V_S = (V+) – (V–)		11	V
	Voltage at input/output pin	(V–) – 0.3	(V+) + 0.3	V
	Current at input pin		±5	mA
I_{SC}	Output short circuit(2)		±30	mA
	Supply pin current		30	mA
	Lead temperature (soldering, 10s)		260	°C
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature(3)		150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Applies to both single-supply and split-supply operation. Continuous short operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$ and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly into a printed circuit board (PCB).

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	2.5		11	V
T_J	Junction temperature	–40		85	°C

5.4 Thermal Information

THERMAL METRIC(1)		LMC7111 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	325	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics for V_S = 2.7V or ±1.35V

at T_A = +25°C, V+ = 2.7V, V– = 0V, V_{CM} = V_O = V+ / 2, and R_L > 1MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±0.9	±7	mV
		T_J = –40°C to +85°C				±9	
dV_{OS}/dT	Input offset voltage drift				±10		µV/°C
PSRR	Power-supply rejection ratio	Positive 2.7V < V+ < 5V, V– = 0V		55	60		dB
			T_J = –40°C to +85°C	50			
		Negative 2.7V < V+ < 5V, V+ = 0V		55	60		
			T_J = –40°C to +85°C	50			
INPUT BIAS CURRENT							
I_B	Input bias current (1)				±0.1	±1	pA
		T_J = –40°C to +85°C				±20	
I_{OS}	Input offset current (1)				±0.01	±0.5	pA
		T_J = –40°C to +85°C				±10	
INPUT VOLTAGE							
V_{CM}	Input common-mode voltage	To positive rail CMRR ≥ 47dB		2.7	2.8		V
			T_J = –40°C to +85°C	2.25			
		To negative rail CMRR ≥ 41dB			–0.10	0.0	
			T_J = –40°C to +85°C			0.40	
		To positive rail CMRR ≥ 47dB, V+ = 3V		3.0	3.2		
			T_J = –40°C to +85°C	2.8			
		To negative rail, CMRR > 47dB, V+ = 3V			–0.25	0.0	
		To positive rail CMRR ≥ 47dB, V+ = 3.3V		3.4	3.5		
			T_J = –40°C to +85°C	3.2			
		To negative rail CMRR ≥ 47dB, V+ = 3.3V			–0.25	–0.10	
			T_J = –40°C to +85°C			0.0	
INPUT IMPEDANCE							
R_{IN}	Input resistance				> 10		TΩ
C_{IN}	Input capacitance	Common mode			3		pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	Sourcing			400		V/mV
		Sinking			150		
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				40		kHz
SR	Slew rate				0.015		V/µs
OUTPUT							
V_O	Voltage output swing	Positive rail R_L = 100kΩ		2.68	2.69		V
			T_J = –40°C to +85°C	2.40			
		Negative rail R_L = 100kΩ			0.10	0.20	
			T_J = –40°C to +85°C			0.08	
		Positive rail R_L = 10kΩ		2.60	2.65		
			T_J = –40°C to +85°C	2.40			
		Negative rail R_L = 10kΩ			0.03	0.10	
			T_J = –40°C to +85°C			0.3	
I_{SC}	Short-circuit current	Sourcing (V_O = 0V) and sinking (V_O = 2.7V)		1	7		mA
			T_J = –40°C to +85°C	0.7			
POWER SUPPLY							
I_Q	Quiescent current per amplifier				20	50	µA
		T_J = –40°C to +85°C				65	

(1) Input bias current specified by design and processing.

5.6 Electrical Characteristics for V_S = 5V or ±2.5V

at T_A = +25°C, V+ = 5V, V– = 0V, V_{CM} = V_O = V_S / 2, and R_L > 1MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±0.9		mV
dV_{OS}/dT	Input offset voltage drift	T_J = –40°C to +85°C			2		µV/°C
PSRR	Power-supply rejection ratio	Positive, 5V < V+ < 10V, V– = 0V		60	85		dB
		Negative, –5V < V– < –10V, V+ = 0V		60	85		
INPUT BIAS CURRENT							
I_B	Input bias current (1)				±0.1	±1	pA
		T_J = –40°C to +85°C				±20	
I_{OS}	Input offset current (1)				±.01	±0.5	pA
		T_J = –40°C to +85°C				±10	
NOISE							
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range	To positive rail CMRR ≥ 50dB		5.20	5.25		V
			T_J = –40°C to +85°C	5.0			
		To negative rail CMRR ≥ 50dB			–0.3	–0.2	
			T_J = –40°C to +85°C			0.0	
CMRR	Common-mode rejection ratio	0V < V_{CM} < 5V		60	85		dB
INPUT IMPEDANCE							
R_{IN}	Input resistance				>10		TΩ
C_{IN}	Common mode input capacitance				3		pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	Sourcing			500		V/mV
		Sinking			200		
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				50		kHz
SR	Slew rate	Voltage follower with 1V step input, R_L = 100kΩ to 1.5V, f = 1kHz, V_O = $1V_{PP}$		0.010	0.027		V/µs
OUTPUT							
V_O	Voltage output swing	R_L = 100kΩ	Positive rail	4.98	4.99		V
			Negative rail		0.01	0.02	
		R_L = 10kΩ	Positive rail	4.9	4.98		
			Negative rail		0.02	0.1	
I_{SC}	Short-circuit current	Sourcing V_O = 0V		5	7		mA
			T_J = –40°C to +85°C	3.5			
		Sinking V_O = 3V		5	7		
			T_J = –40°C to +85°C	3.5			
POWER SUPPLY							
I_Q	Quiescent current per amplifier				25		µA

(1) Input bias current specified by design and processing.

5.7 Electrical Characteristics for V_S = 10V or ±5V

at T_A = +25°C, V+ = 10V, V- = 0V, V_{CM} = V_O = V+ / 2, and R_L > 1MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±0.9	±7	mV
		T_J = –40°C to +85°C				±9	
dV_{OS}/dT	Input offset voltage drift	T_J = –40°C to +85°C			2		µV/°C
PSRR	Power supply rejection ratio	Positive 5V < V_S < 10V, V– = 0V, V_O = 2.5V			80		dB
		Negative –5V < V_S < –10V, V+ = 0V, V_O = 2.5V			80		
INPUT BIAS CURRENT							
I_B	Input bias current (1)				±0.1	±1	pA
		T_J = –40°C to +85°C				±20	
I_{OS}	Input offset current (1)				±0.01	±0.5	pA
		T_J = –40°C to +85°C				±10	
NOISE							
e_n	Input voltage noise density	f = 1kHz, V_{CM} = 1V			110		nV/√Hz
i_n	Input current noise density	f = 1kHz			0.03		pA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range	To positive rail CMRR ≥ 50dB		10.15	10.2		V
			T_J = –40°C to +85°C	10.0			
		To negative rail CMRR ≥ 50dB			–0.2	–0.15	
			T_J = –40°C to +85°C			0.0	
INPUT IMPEDANCE							
R_{IN}	Input resistance				>10		TΩ
C_{IN}	Common mode input capacitance				3		pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	R_L = 100kΩ	Sourcing		500		V/mV
			Sinking		200		
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				50		kHz
SR	Slew rate	Voltage follower with 1V step input, R_L = 100kΩ to 5V, f = 1kHz, V_O = $2V_{PP}$			0.03		V/µs
G_M	Gain margin				15		dB
θ_m	Phase margin				50		°
OUTPUT							
V_O	Voltage output swing	R_L = 100kΩ	Positive rail,	9.98	9.99		V
			Negative rail		0.01	0.02	
		R_L = 10kΩ	Positive rail	9.90	9.98		
			Negative rail		0.02	0.1	
I_{SC}	Short-circuit current	Sourcing V_O = 0V		25	20		mA
			T_J = –40°C to +85°C	7			
		Sinking V_O = 10V		30	20		
			T_J = –40°C to +85°C	7			
POWER SUPPLY							
I_Q	Quiescent current per amplifier				25	60	µA
		T_J = –40°C to +85°C				75	

(1) Input bias current specified by design and processing.

5.8 Typical Characteristics

at T_A = 25°C (unless otherwise specified)

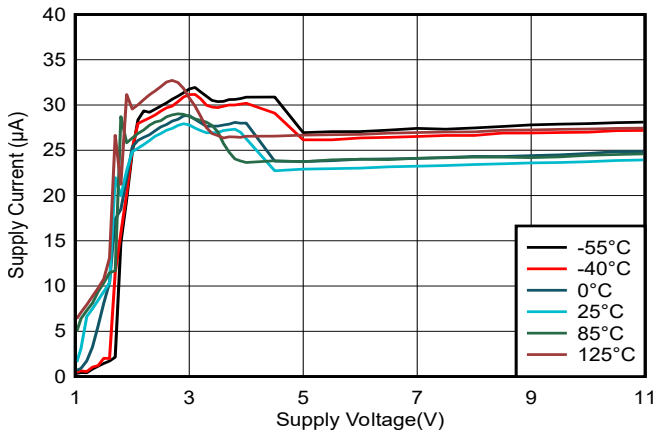


Figure 5-1. Supply Current vs Supply Voltage

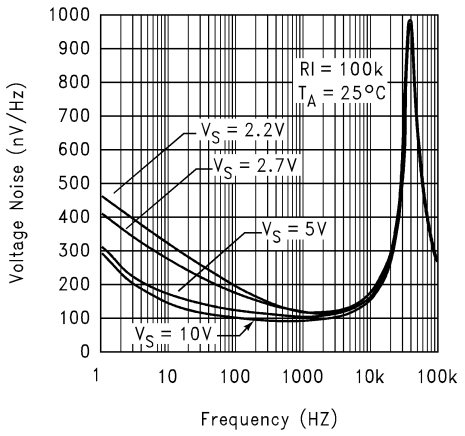


Figure 5-2. Voltage Noise vs Frequency

5.9 Typical Characteristics: 2.7V

at T_A = 25°C (unless otherwise specified)

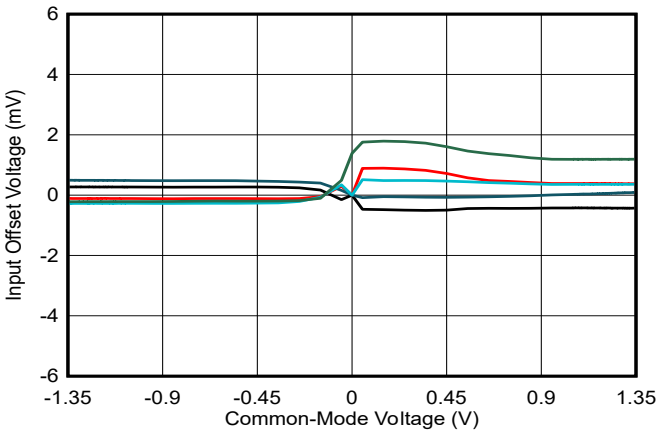


Figure 5-3. Offset Voltage vs Common-Mode Voltage at 2.7V

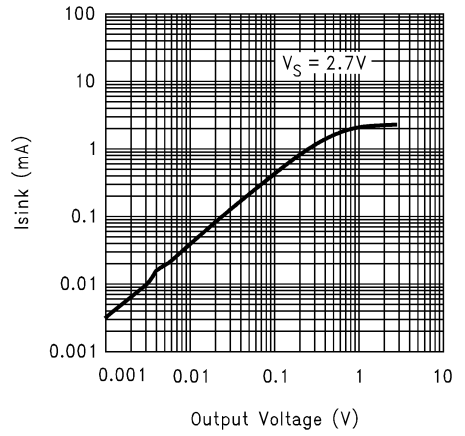


Figure 5-4. Sinking Output vs Output Voltage

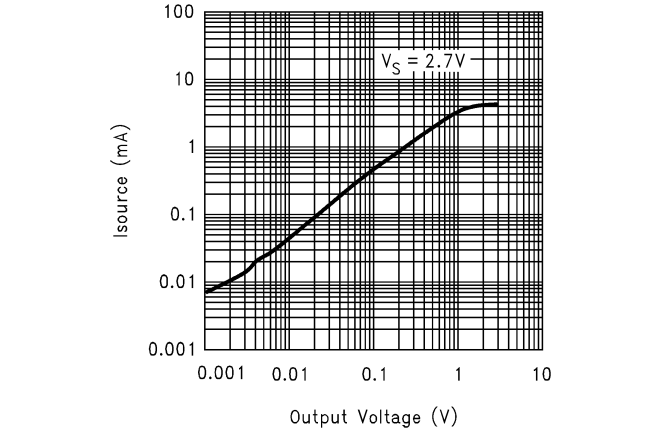


Figure 5-5. Sourcing Output vs Output Voltage

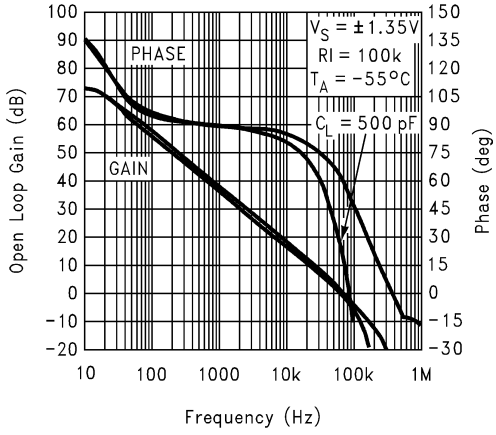


Figure 5-6. Gain and Phase vs Capacitive Load at 2.7V

5.9 Typical Characteristics: 2.7V (continued)

at T_A = 25°C (unless otherwise specified)

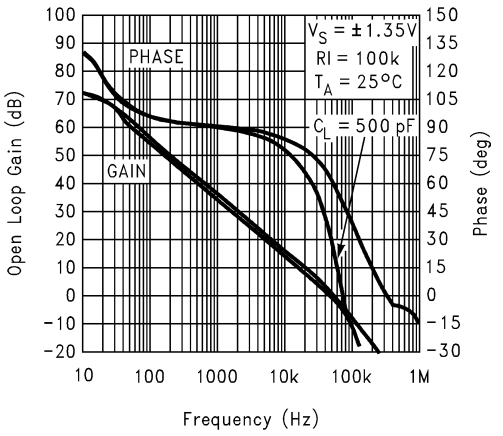


Figure 5-7. Gain and Phase vs Capacitive Load at 2.7V

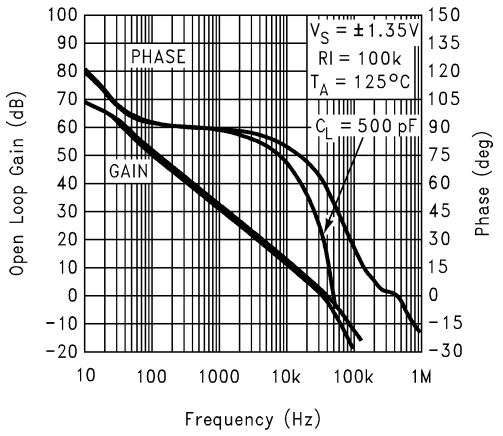


Figure 5-8. Gain and Phase vs Capacitive Load at 2.7V

5.10 Typical Characteristics: 3V

at T_A = 25°C (unless otherwise specified)

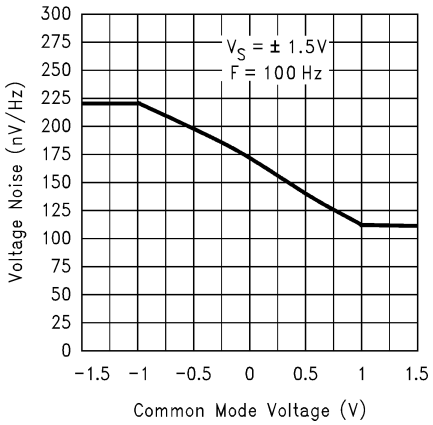


Figure 5-9. Voltage Noise vs Common-Mode Voltage at 3V

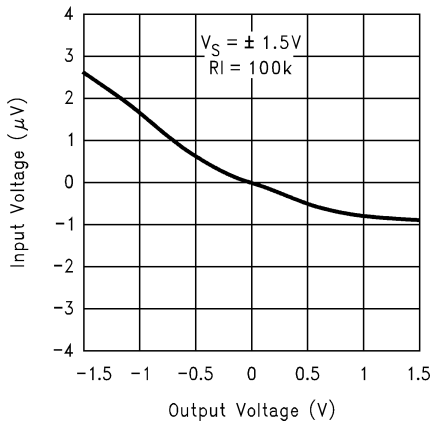


Figure 5-10. Output Voltage vs Input Voltage at 3V

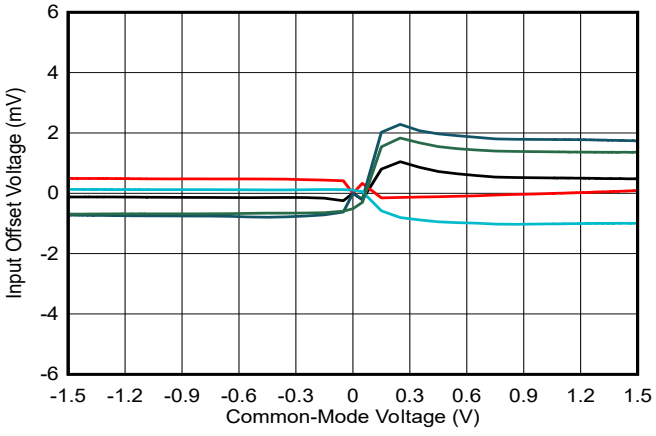


Figure 5-11. Offset Voltage vs Common-Mode Voltage at 3V

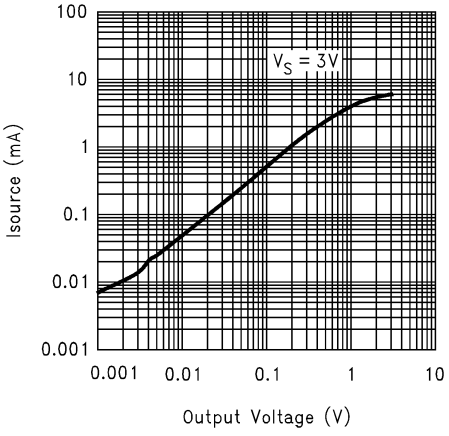


Figure 5-12. Sourcing Output vs Output Voltage

5.10 Typical Characteristics: 3V (continued)

at T_A = 25°C (unless otherwise specified)

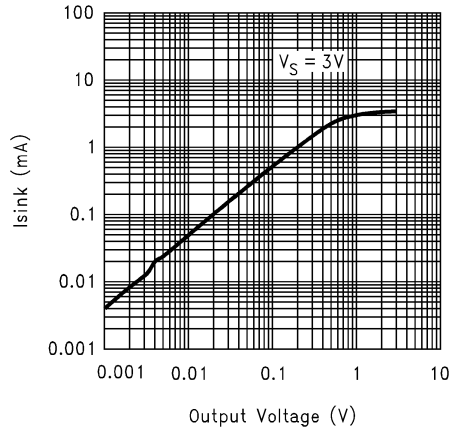


Figure 5-13. Sinking Output vs Output Voltage

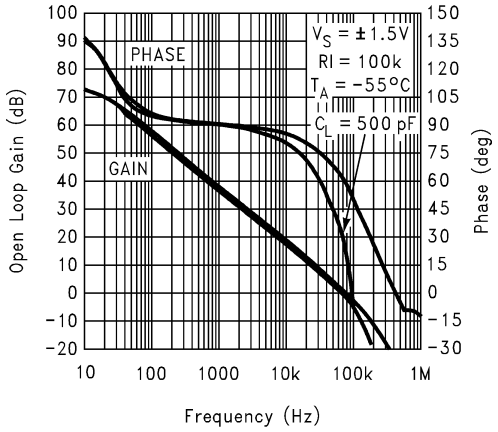


Figure 5-14. Gain and Phase vs Capacitive Load at 3V

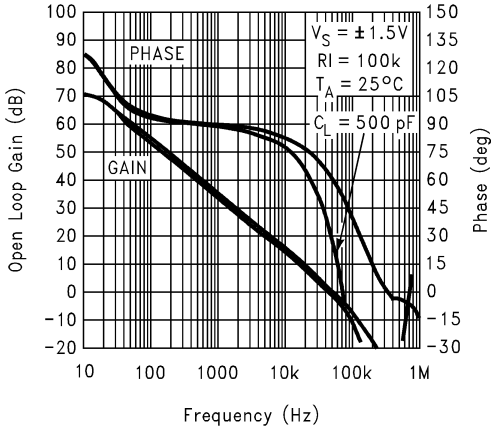


Figure 5-15. Gain and Phase vs Capacitive Load at 3V

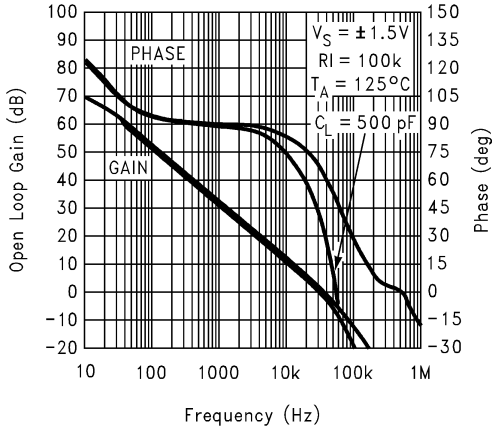


Figure 5-16. Gain and Phase vs Capacitive Load at 3V

5.11 Typical Characteristics: 5V

at T_A = 25°C (unless otherwise specified)

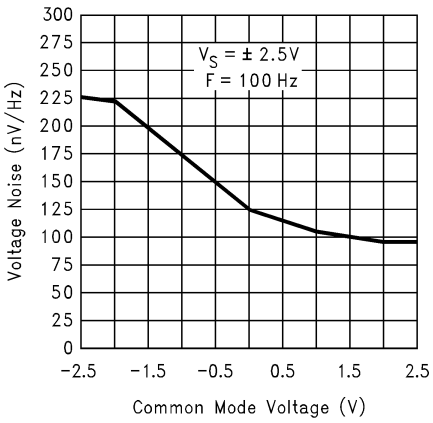


Figure 5-17. Voltage Noise vs Common-Mode Voltage at 5V

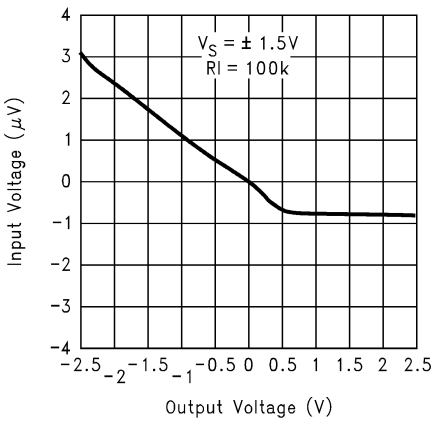


Figure 5-18. Output Voltage vs Input Voltage at 5V

5.11 Typical Characteristics: 5V (continued)

at T_A = 25°C (unless otherwise specified)

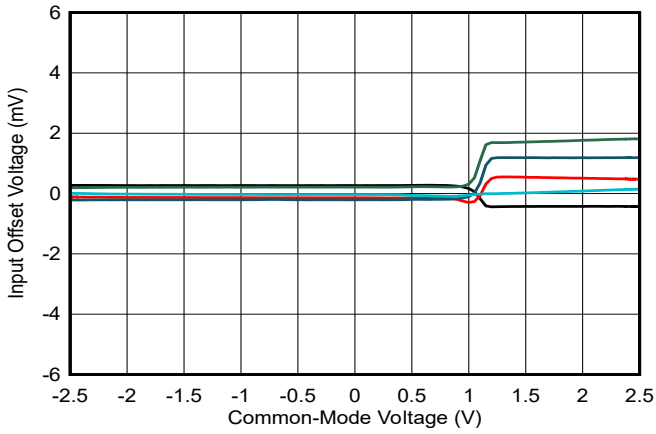


Figure 5-19. Offset Voltage vs Common-Mode Voltage at 5V

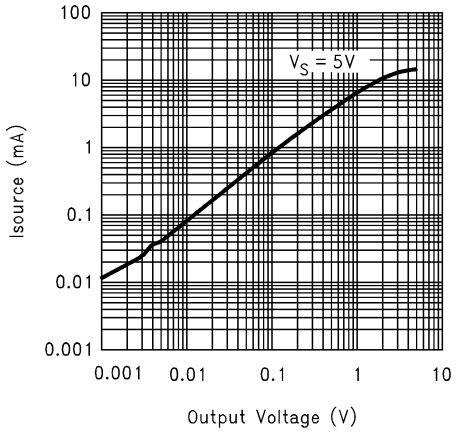


Figure 5-20. Sourcing Output vs Output Voltage

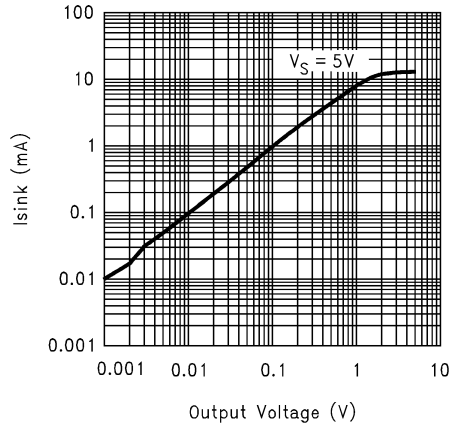


Figure 5-21. Sinking Output vs Output Voltage

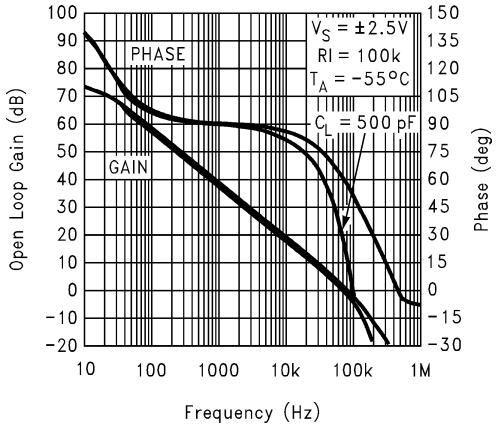


Figure 5-22. Gain and Phase vs Capacitive Load at 5V

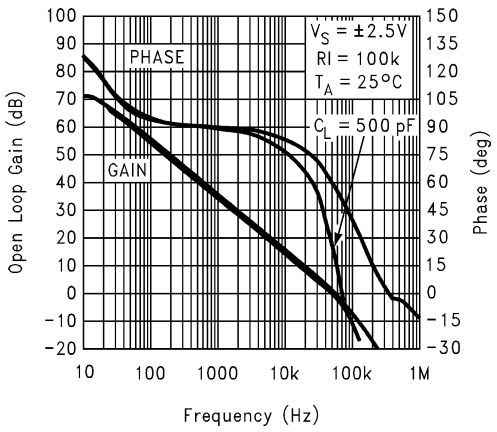


Figure 5-23. Gain and Phase vs Capacitive Load at 5V

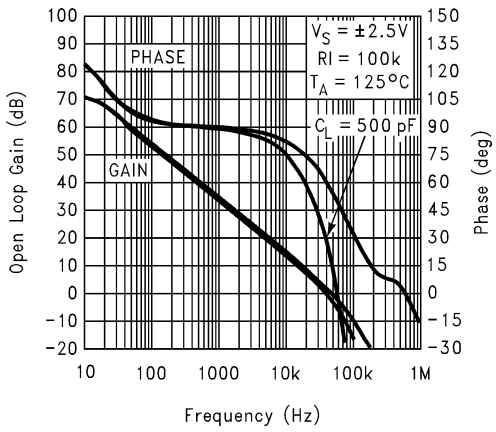


Figure 5-24. Gain and Phase vs Capacitive Load at 5V

5.11 Typical Characteristics: 5V (continued)

at T_A = 25°C (unless otherwise specified)

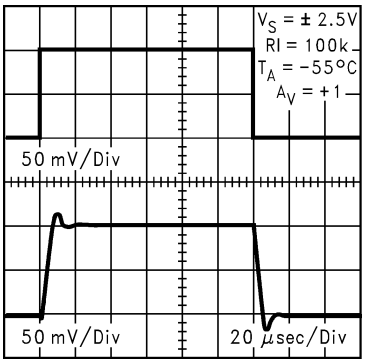


Figure 5-25. Noninverting Small-Signal Pulse Response at 5V

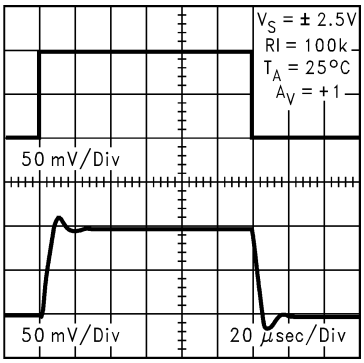


Figure 5-26. Noninverting Small-Signal Pulse Response at 5V

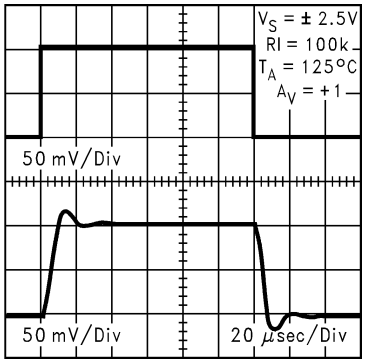


Figure 5-27. Noninverting Small-Signal Pulse Response at 5V

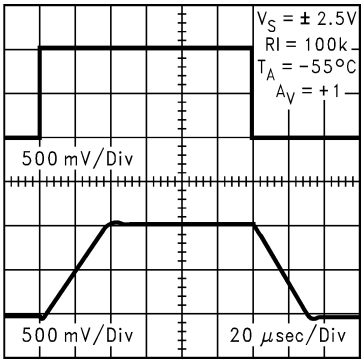


Figure 5-28. Noninverting Large-Signal Pulse Response at 5V

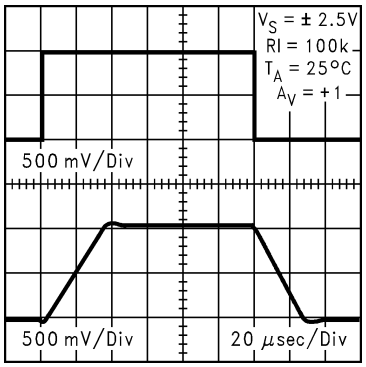


Figure 5-29. Noninverting Large-Signal Pulse Response at 5V

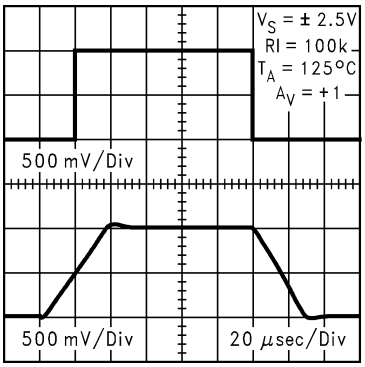


Figure 5-30. Noninverting Large-Signal Pulse Response at 5V

5.11 Typical Characteristics: 5V (continued)

at T_A = 25°C (unless otherwise specified)

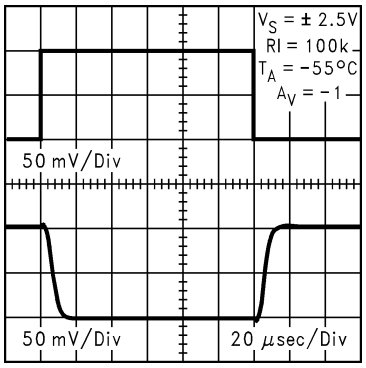


Figure 5-31. Inverting Small-Signal Pulse Response at 5V

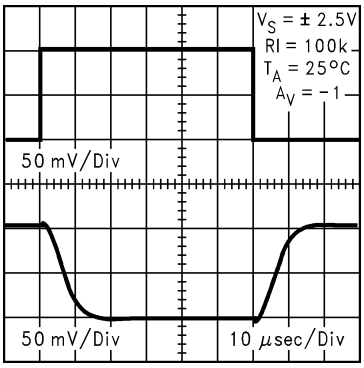


Figure 5-32. Inverting Small-Signal Pulse Response at 5V

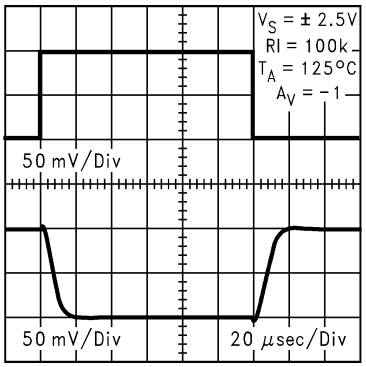


Figure 5-33. Inverting Small-Signal Pulse Response at 5V

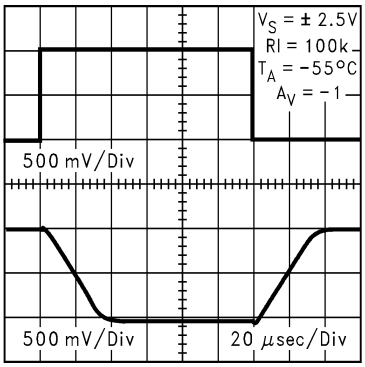


Figure 5-34. Inverting Large-Signal Pulse Response at 5V

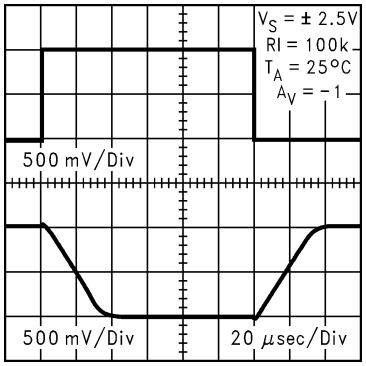


Figure 5-35. Inverting Large-Signal Pulse Response at 5V

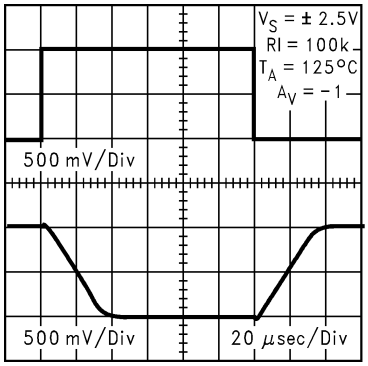


Figure 5-36. Inverting Large-Signal Pulse Response at 5V

5.12 Typical Characteristics: 10V

at T_A = 25°C (unless otherwise specified)

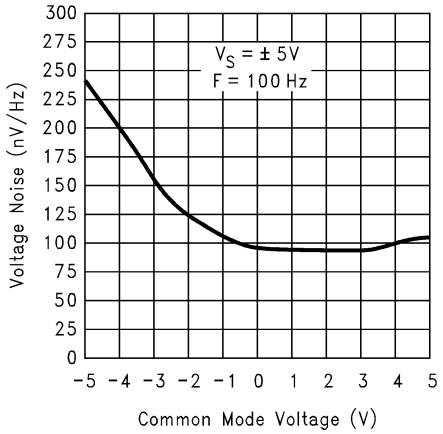


Figure 5-37. Voltage Noise vs Common-Mode Voltage at 10V

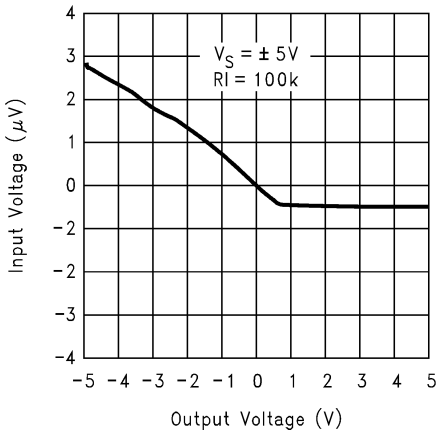


Figure 5-38. Output Voltage vs Input Voltage at 10V

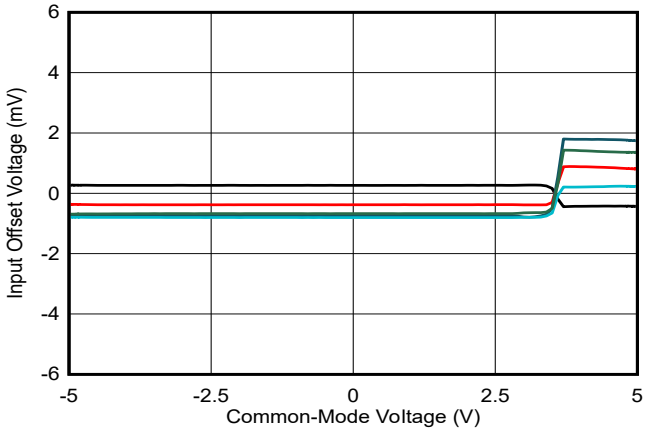


Figure 5-39. Offset Voltage vs Common-Mode Voltage at 10V

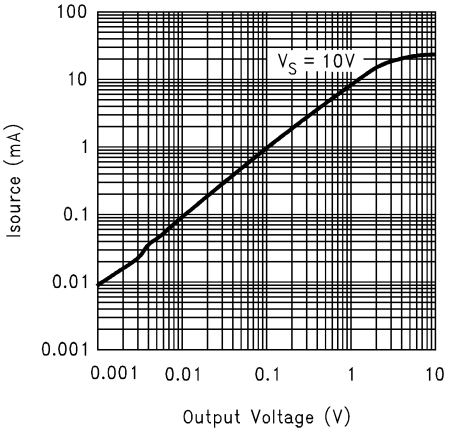


Figure 5-40. Sourcing Output vs Output Voltage

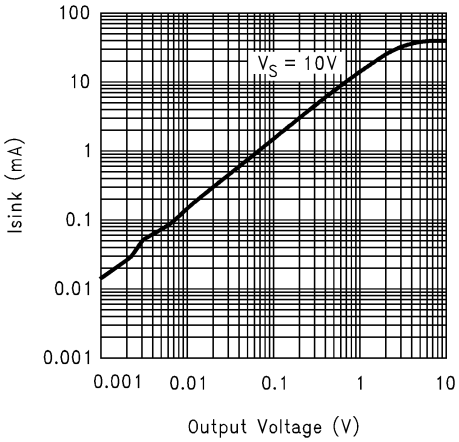


Figure 5-41. Sinking Output vs Output Voltage

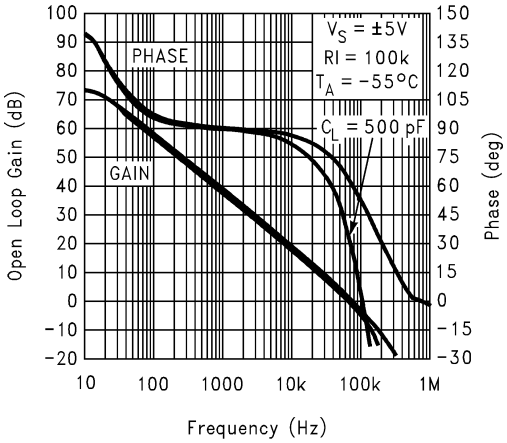


Figure 5-42. Gain and Phase vs Capacitive Load at 10V

5.12 Typical Characteristics: 10V (continued)

at T_A = 25°C (unless otherwise specified)

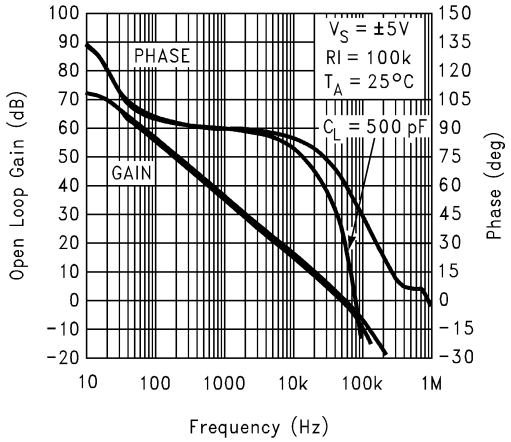


Figure 5-43. Gain and Phase vs Capacitive Load at 10V

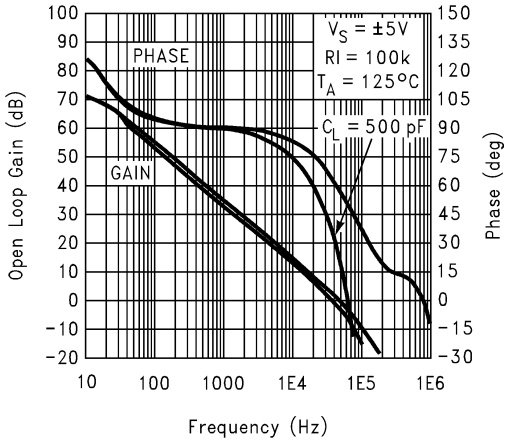


Figure 5-44. Gain and Phase vs Capacitive Load at 10V

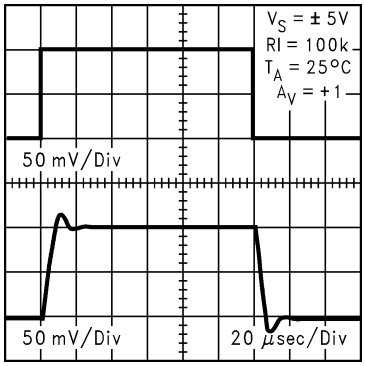


Figure 5-45. Noninverting Small-Signal Pulse Response at 10V

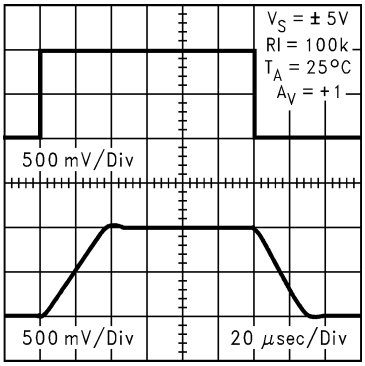


Figure 5-46. Noninverting Large-Signal Pulse Response at 10V

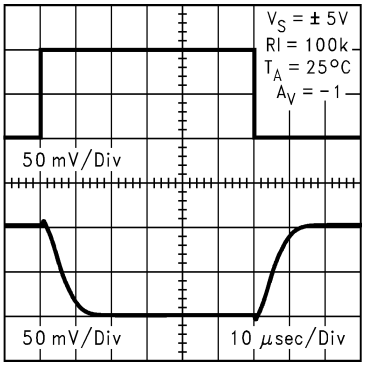


Figure 5-47. Inverting Small-Signal Pulse Response at 10V

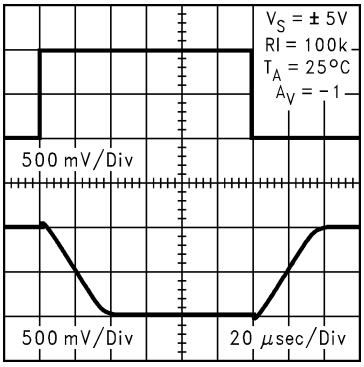


Figure 5-48. Inverting Large-Signal Pulse Response at 10V

6 Detailed Description

6.1 Feature Description

6.1.1 Benefits of the LMC7111 Tiny Amp

6.1.1.1 Size

The small footprint of the SOT-23-5 packaged tiny amplifier, (0.12in × 0.118in, 3.05mm × 3mm) saves space on printed circuit boards, and enable the design of smaller electronic products. Many customers prefer smaller and lighter products because the designs can contribute to overall weight reduction in applications.

6.1.1.2 Height

The height (0.056 inches, 1.43mm) of the tiny amplifier makes the device an excellent choice for use in a wide range of circuit boards in which a thin profile is required.

6.1.1.3 Signal Integrity

Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the Tiny amp can be placed closer to the signal source, reducing noise pickup and increasing signal integrity. The Tiny amp can also be placed next to the signal destination, such as a buffer for the reference of an analog to digital converter.

6.1.1.4 Simplified Board Layout

The tiny amplifier can simplify board layout in several ways. Avoid long PCB traces by correctly placing amplifiers instead of routing signals to a dual or quad device. By using multiple tiny amplifiers instead of duals or quads, complex signal routing and possibly crosstalk can be reduced.

6.1.1.5 Low Supply Current

The typical 25µA supply current of the LMC7111 extends battery life in portable applications, and can allow for the reduction of battery size in some applications.

6.1.1.6 Wide Voltage Range

The LMC7111 is characterized at 2.7V, 3V, 3.3V, 5V and 10V. Performance data is provided at these popular voltages. This wide voltage range makes the LMC7111 a good choice for devices where the voltage can vary over the life of the batteries.

6.1.2 Input Common-Mode Voltage Range

The LMC7111 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage.

The absolute maximum input voltage is 300mV beyond either rail at room temperature. Voltages greatly exceeding this maximum rating can cause excessive current to flow in or out of the input pins, adversely affecting reliability.

Applications that exceed this rating must externally limit the maximum input current to ±5mA with an input resistor as shown in Figure 6-1.

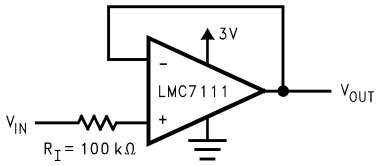


Figure 6-1. R_I Input Current Protection for Voltages Exceeding the Supply Voltage

6.1.3 Output Swing

The LMC71111 output goes to within 100mV of either power supply rail for a 10kΩ load, and to 20mV of the rail for a 100kΩ load. This feature makes the LMC7111 useful to drive transistors connected to the same power supply. By going very close to the supply, the LMC7111 can turn the transistors all the way on or off.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Capacitive Load Tolerance

The LMC7111 can typically directly drive a 300pF load with V_S = 10V at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in Figure 7-1. This simple technique is useful for isolating the capacitive input of multiplexers and A/D converters.

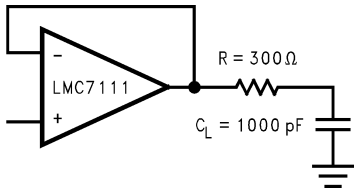


Figure 7-1. Resistive Isolation of a 330pF Capacitive Load

7.1.2 Compensating for Input Capacitance When Using Large-Value Feedback Resistors

When using very large value feedback resistors, (usually > 500kΩ) the large feed back resistance can react with the input capacitance due to transducers, photodiodes, and circuit board parasitics to reduce phase margins.

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in Figure 7-2), C_f is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \quad (1)$$

or

$$R_1 C_{IN} \leq R_2 C_f \quad (2)$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance can be larger or smaller than that of a breadboard, so the actual optimum value for $C_F$can be different. Check C_F values on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

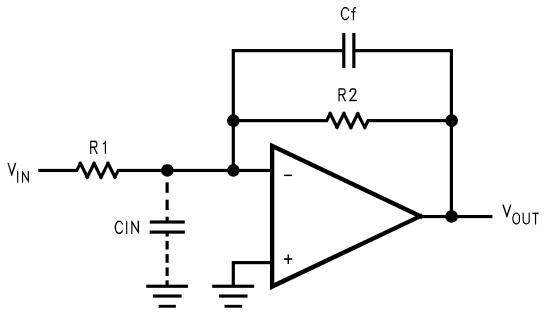


Figure 7-2. Canceling the Effect of Input Capacitance

7.1.3 Dual and Quad Devices With Similar Performance

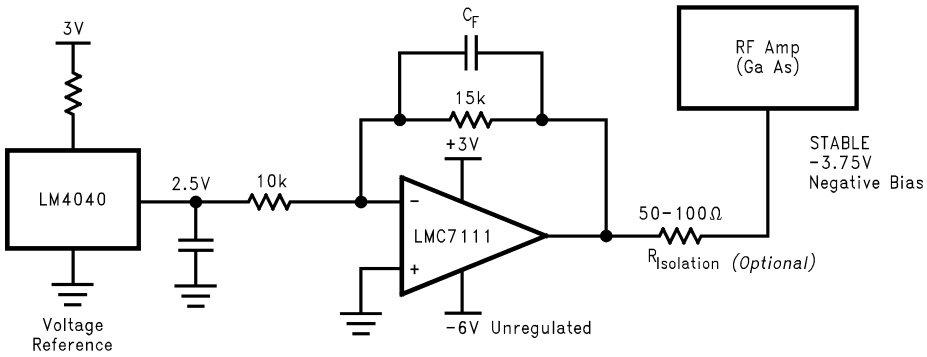
The dual LMC6462 and quad LMC6464 devices achieve performance similar to the LMC7111. Both devices are available in both conventional through-hole and surface-mount packaging. See also the LMC646x data sheet for details.

7.2 Typical Application

7.2.1 Biasing GaAs RF Amplifiers

The capacitive load capability, low current draw, and small size of the SOT-23 LMC7111 make this device a good choice for providing a stable negative bias to other integrated circuits.

The very small size of the LMC7111 and the LM4040 reference take up very little board space.



Note: C_F and $R_{isolation}$ prevent oscillations when driving capacitive loads.

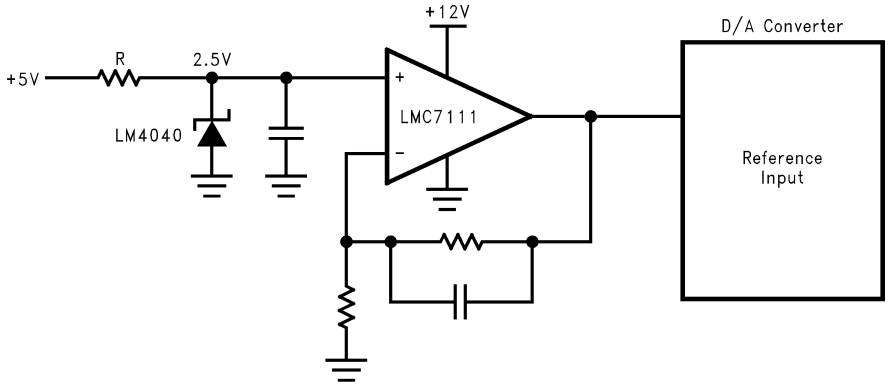
Figure 7-3. Stable Negative Bias

7.2.2 Reference Buffer for Analog-to-Digital Converters

The LMC7111 can be used as a voltage reference buffer for an analog-to-digital converter (ADC). This configuration works best for ADCs with the reference input is a static load, such as dual slope integrating ADCs. Converters with a reference input that is a dynamic load (the reference current changes with time) can require a faster device, such as the LMC7101 or the LMC7131.

The small size of the LMC7111 allows this device to be placed close to the reference input. The low supply current (25µA typical) saves power.

For ADC reference inputs that require higher accuracy and lower offset voltage, see the LMC646x data sheet. The LMC6462 has performance similar to the LMC7111. The LMC6462 is available in two grades with reduced input voltage offset.



8 Device and Documentation Support

8.1 Device Support

8.1.1 Spice Macromodel

A SPICE macromodel is available for the LMC7111. This model includes simulation of:

- Input common-mode voltage range
- Frequency and transient response
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions and many more characteristics as listed on the macro model disk. Visit the LMC7111 product page on http://www.ti.com for the spice model.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (March 2013) to Revision F (January 2025)	Page
• Updated pin diagram for SOT-23 and pin names in *Pin Configurations and Functions*	2
• Deleted PDIP package information in *Pin Configuration and Functions*	2
• Updated parameter names and table format in all *Electrical Characteristics*	4
• Deleted reference to AI version in all *Electrical Characteristics*	4
• Updated dV_{OS}/dT from 2µV/°C to 10µV/°C	4
• Changed V_{CM} test condition from CMRR ≥ 50dB to CMRR ≥ 47dB	4
• Changed V_{CM} test condition for negative rail for V_S= 2.7V from CMRR ≥ 50dB to CMRR ≥ 41dB	4
• Changed I_{SC} MIN from 30mA to 25mA	6

Changes from Revision D (March 2013) to Revision E (March 2013)	Page
• Changed layout of National Data Sheet to TI format	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMC7111BIM5/NOPB	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 85	A01B
LMC7111BIM5X/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A01B
LMC7111BIM5X/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A01B
LMC7111BIM5X/NOPB.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A01B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

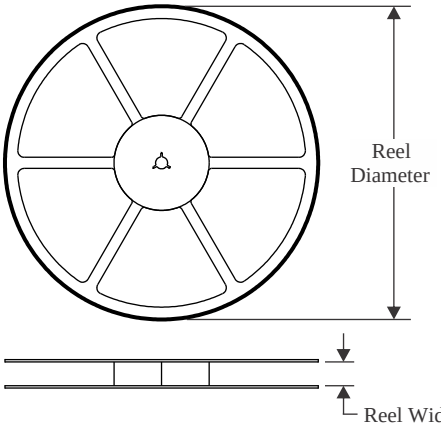
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

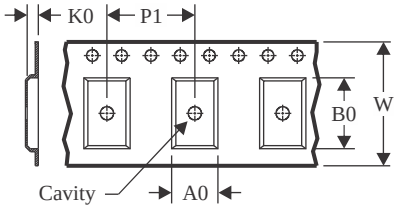
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

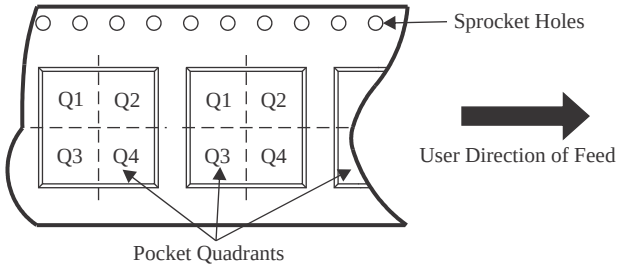


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

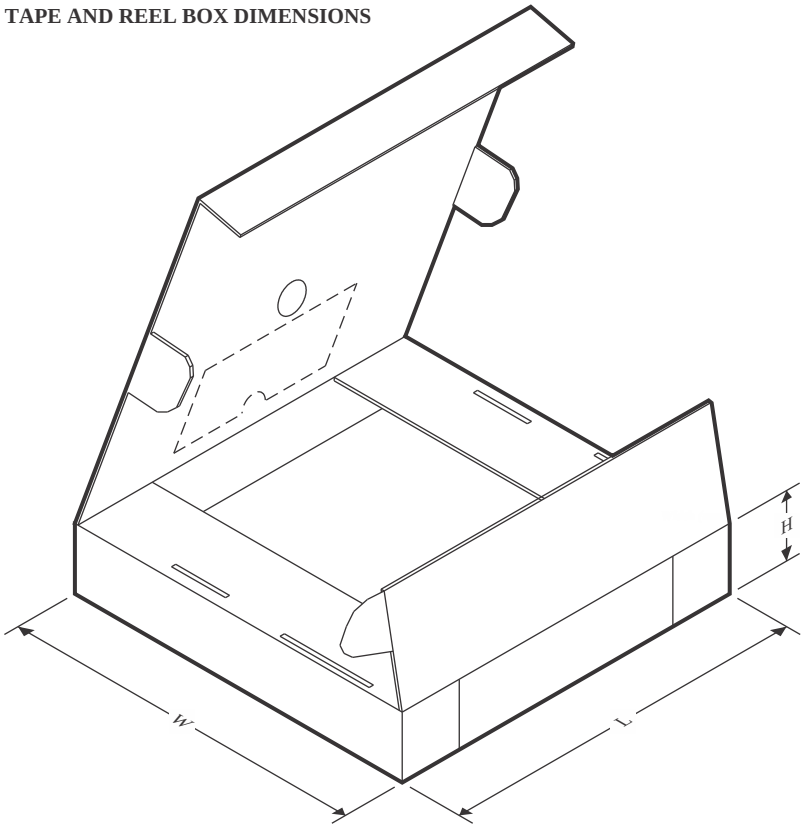
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC7111BIM5X/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

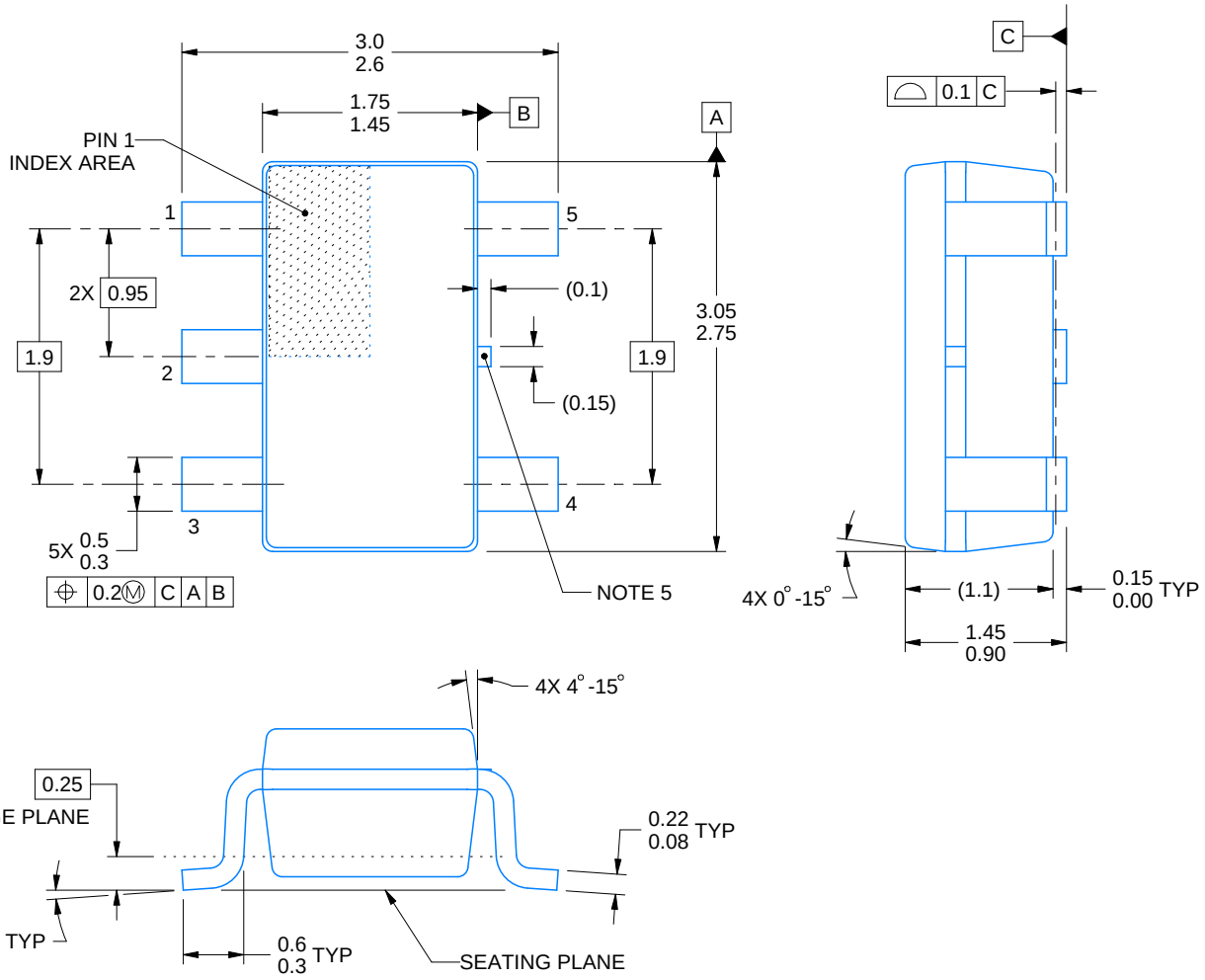
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC7111BIM5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

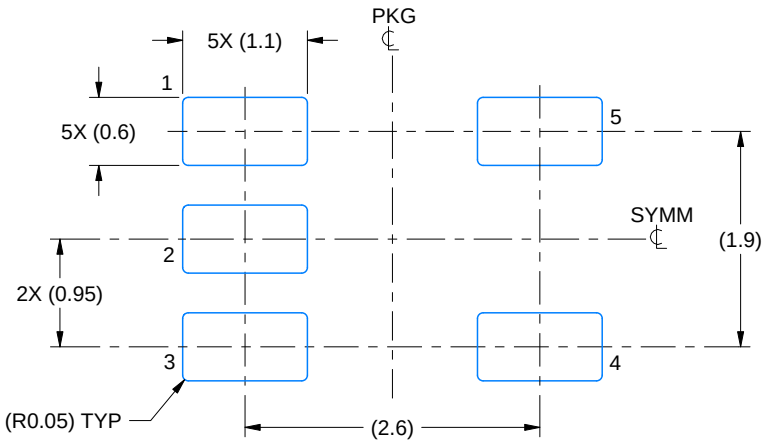
SMALL OUTLINE TRANSISTOR



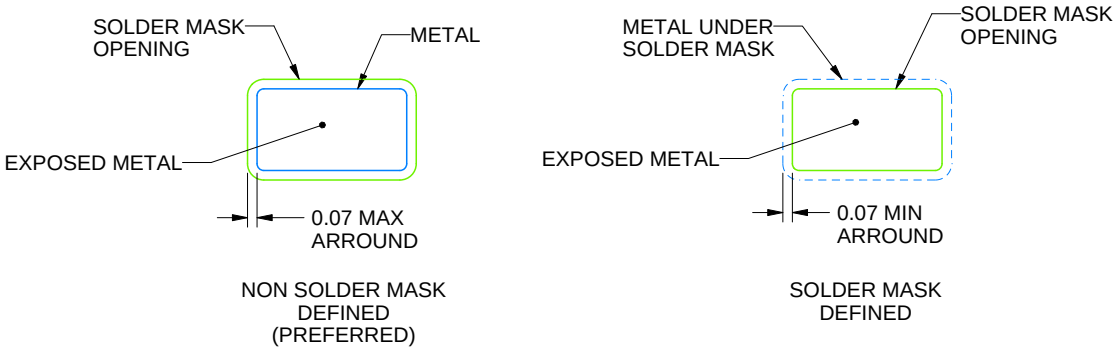
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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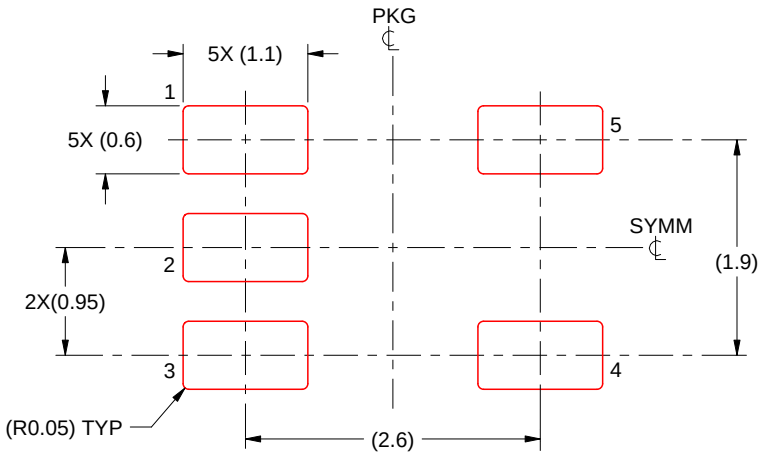
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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