

# LMC7101Q-Q1 Automotive, Tiny, Low-Power Operational Amplifier With Rail-to-Rail Input and Output

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $T_A$
- Tiny 5-Pin SOT-23 package saves space; typical circuit layouts take half the space of 8-pin SOIC designs
- Specified for 2.7V, 3V, 5V, 15V supplies
- Typical supply current 0.5mA at 5V
- Typical total harmonic distortion of 0.01% at 5V
- 1MHz gain bandwidth
- Similar to popular LMC6482 and LMC6484
- Rail-to-rail input and output

## 2 Applications

- Mobile communications
- Notebooks and PDAs
- Battery-powered products
- Sensor interface
- Automotive applications

## 3 Description

The LMC7101Q-Q1 device is a high-performance, automotive, CMOS operational amplifier available in a space-saving, 5-pin, SOT-23 tiny package. This design makes the LMC7101Q-Q1 an excellent choice for space- and weight-critical designs. The performance is similar to the single amplifier of the LMC6482 and LMC6484, with rail-to-rail input and output, high open-loop gain, low distortion, and low-supply currents.

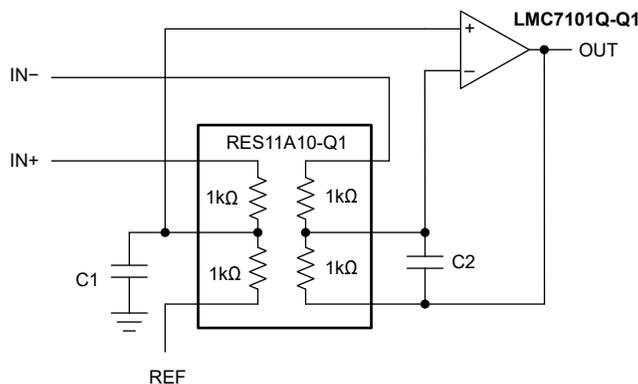
The main benefits of the tiny package are most apparent in space-constrained applications. The tiny amplifiers can be placed on a board where needed, thus simplifying board layout.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
LMC7101Q-Q1	DBV (SOT-23, 5)	2.9mm × 2.8mm

(1) For more information, see [Section 10](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



**Difference Amplifier Application With RES11A-Q1**



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## 4 Pin Configuration and Functions

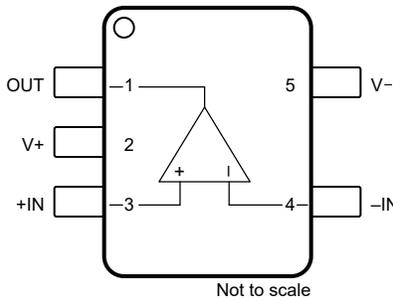


Figure 4-1. DBV Package, 5-Pin SOT-23 (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OUT	Output	Output
2	V+	Power	Positive supply
3	+IN	Input	Noninverting input
4	-IN	Input	Inverting input
5	V-	Power	Negative supply

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup> <sup>(2)</sup>

		MIN	MAX	UNIT
	Difference Input voltage		±Supply voltage	V
	Voltage at input and output pins	(V-) – 0.3	(V+) + 0.3	V
V <sub>S</sub>	Supply voltage, V <sub>S</sub> = (V+) – (V-)		16	V
	Current at input pin	-5	5	mA
	Current at output pin <sup>(3)</sup>	-35	35	mA
	Current at power supply pin		35	mA
	Lead temperature (soldering, 10s)		260	°C
T <sub>J</sub>	Junction temperature <sup>(4)</sup>		150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) If Military/Aerospace specified devices are required, contact the TI Sales Office or Distributors for availability and specifications.
- (3) Applies to both single-supply and split-supply operation. Continuous short operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C
- (4) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, R<sub>θJA</sub> and T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> – T<sub>A</sub>) / R<sub>θJA</sub>. All numbers apply for packages soldered directly into a PC board.

### 5.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>S</sub>	Supply voltage, V <sub>S</sub> = (V+) – (V-)	2.7		15.5	V
T <sub>A</sub>	Ambient temperature	-40		125	°C

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LMC7101Q-Q1	UNIT
		DBV (SOT-23)	
		5 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	193.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case(top) thermal resistance	128.5	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	88.9	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	66.8	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	88.6	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case(bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Electrical Characteristics for $V_S = 2.7V$ or $\pm 1.35V$

at  $T_A = 25^\circ C$ ,  $V_+ = 2.7V$ ,  $V_- = 0V$ ,  $V_{CM} = V_{OUT} = V_+ / 2$ , and  $R_L = 1M\Omega$  connected to  $V_+ / 2$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>OFFSET VOLTAGE</b>							
$V_{OS}$	Input offset voltage			$\pm 0.11$	$\pm 9$	mV	
$dV_{OS}/dT$	Input offset voltage drift	$T_A = -40^\circ C$ to $+125^\circ C$		1		$\mu V/^\circ C$	
PSRR	Power-supply rejection ratio	$V_+ = 1.35V$ to $1.65V$ , $V_- = -1.35V$ to $-1.65V$ , $V_{CM} = 0V$	45	60		dB	
<b>INPUT BIAS CURRENT</b>							
$I_B$	Input bias current	$T_A = -40^\circ C$ to $+125^\circ C$		$\pm 1$	$\pm 1000$	pA	
$I_{OS}$	Input offset current	$T_A = -40^\circ C$ to $+125^\circ C$		$\pm 0.5$	$\pm 2000$	pA	
<b>INPUT VOLTAGE</b>							
$V_{CM}$	Common-mode voltage	For $CMRR \geq 47dB$	Positive 2.7	3		V	
			Negative	0	0		
CMRR	Common-mode rejection	$0V \leq V_{CM} \leq 2.7V$	47	70		dB	
<b>INPUT IMPEDANCE</b>							
$R_{IN}$	Input resistance			$> 1$		$T\Omega$	
$C_{IN}$	Common-mode input capacitance			3		pF	
<b>FREQUENCY RESPONSE</b>							
GBW	Gain bandwidth product			0.6		MHz	
SR	Slew rate <sup>(1)</sup>	$V_+ = 15V$ , $10V$ step, $G = 1$ , $R_L = 100k\Omega$ to $7.5V$ , $V_{OUT} = 10V_{PP}$ , $f = 1kHz$		0.7		V/ $\mu s$	
<b>OUTPUT</b>							
$V_O$	Voltage output swing	Positive rail	$R_L = 2k\Omega$	2.15	2.45	V	
			$R_L = 10k\Omega$	2.64	2.68		
		Negative rail	$R_L = 2k\Omega$		0.25		0.5
			$R_L = 10k\Omega$		0.025		0.06
<b>POWER SUPPLY</b>							
$I_Q$	Quiescent current per amplifier	$T_A = -40^\circ C$ to $+125^\circ C$		500	810	$\mu A$	
				500	950		

(1) Number specified is the slower of the positive and negative slew rates.

## 5.6 Electrical Characteristics for $V_S = 3V$ or $\pm 1.5V$

at  $T_A = 25^\circ\text{C}$ ,  $V_+ = 3V$ ,  $V_- = 0V$ ,  $V_{CM} = 1.5V$ ,  $V_{OUT} = V_+ / 2$ , and  $R_L = 1M\Omega$  connected to  $V_+ / 2$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>OFFSET VOLTAGE</b>							
$V_{OS}$	Input offset voltage			$\pm 0.11$	$\pm 7$	mV	
$dV_{OS}/dT$	Input offset voltage drift	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		1		$\mu\text{V}/^\circ\text{C}$	
PSRR	Power-supply rejection ratio	$V_+ = 1.5V$ to $7.5V$ , $V_- = -1.5V$ to $-7.5V$ , $V_{OUT} = V_{CM} = 0V$	60	80		dB	
<b>INPUT BIAS CURRENT</b>							
$I_B$	Input bias current	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		$\pm 1$	$\pm 1000$	pA	
$I_{OS}$	Input offset current	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		$\pm 0.5$	$\pm 2000$	pA	
<b>INPUT VOLTAGE</b>							
$V_{CM}$	Input common-mode voltage	For $CMRR \geq 47\text{dB}$	Positive 3	3.3		V	
			Negative	0	0		
CMRR	Common-mode rejection	$0V \leq V_{CM} \leq 3V$	47	70		dB	
<b>INPUT IMPEDANCE</b>							
$R_{IN}$	Input resistance			$> 1$		$T\Omega$	
$C_{IN}$	Common-mode input capacitance			3		pF	
<b>OUTPUT</b>							
$V_O$	Voltage output swing	Positive rail	$R_L = 2k\Omega$	2.6	2.8	V	
			$R_L = 600\Omega$	2.5	2.7		
		Negative rail	$R_L = 2k\Omega$		0.2		0.4
			$R_L = 600\Omega$		0.37		0.6
<b>POWER SUPPLY</b>							
$I_Q$	Quiescent current per amplifier	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		500	810	$\mu\text{A}$	
				500	950		

## 5.7 Electrical Characteristics for $V_S = 5V$ or $\pm 2.5V$

 at  $T_A = 25^\circ\text{C}$ ,  $V_+ = 5V$ ,  $V_- = 0V$ ,  $V_{CM} = 1.5V$ ,  $V_{OUT} = V_+ / 2$ , and  $R_L = 1M\Omega$  connected to  $V_+ / 2$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>OFFSET VOLTAGE</b>							
$V_{OS}$	Input offset voltage			$\pm 0.11$	$\pm 7$	mV	
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		$\pm 0.11$	$\pm 9$		
$dV_{OS}/dT$	Input offset voltage drift	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		1		$\mu\text{V}/^\circ\text{C}$	
PSRR	Power supply rejection ratio	Positive $V_+ = 5V$ to $15V$ $V_- = 0V$ , $V_{OUT} = 1.5V$	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	65	82	dB	
				62	82		
		Negative $V_+ = -5V$ to $-15V$ $V_- = 0V$ , $V_{OUT} = -1.5V$	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	65	82		
				62	82		
<b>INPUT BIAS CURRENT</b>							
$I_B$	Input bias current			$\pm 1$		pA	
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			$\pm 1000$		
$I_{OS}$	Input offset current			$\pm 0.5$		pA	
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			$\pm 2000$		
<b>NOISE</b>							
THD	Total harmonic distortion	$f = 10\text{kHz}$ , $G = -2V/V$ , $R_L = 10\text{k}\Omega$ , $V_{OUT} = 4V_{pp}$		0.01		%	
<b>INPUT VOLTAGE</b>							
$V_{CM}$	Input common-mode voltage	To positive rail CMRR > 50dB	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	5.2	5.3	V	
				4.8	5.3		
		To negative rail CMRR > 50dB	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		-0.3		-0.2
					-0.3		0.2
CMRR	Common-mode rejection ratio	$0V \leq V_{CM} \leq 5V$		52	75	dB	
		$0.2V \leq V_{CM} \leq 4.8V$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		51	74		
<b>INPUT IMPEDANCE</b>							
$R_{IN}$	Input resistance			> 1		$\text{T}\Omega$	
$C_{IN}$	Input capacitance			3		pF	
<b>FREQUENCY RESPONSE</b>							
GBW	Gain bandwidth product			1		MHz	
SR	Slew rate			1		$\text{V}/\mu\text{s}$	
<b>OUTPUT</b>							
$V_O$	Voltage output swing	Positive rail $R_L = 2\text{k}\Omega$	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	4.7	4.9	V	
				4.54	4.9		
		Negative rail $R_L = 2\text{k}\Omega$	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		0.1		0.18
					0.1		0.28
		Positive rail $R_L = 600\Omega$	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	4.5	4.7		
				4.28	4.7		
		Negative rail $R_L = 600\Omega$	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		0.3		0.5
					0.3		0.8
$I_{SC}$	Short-circuit current	Sourcing $V_{OUT} = 0V$	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	16	24	mA	
				9	24		
		Sinking $V_{OUT} = 5V$	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	11	19		
				5.8	19		
<b>POWER SUPPLY</b>							
$I_Q$	Quiescent current per amplifier			0.5	0.85	mA	
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			0.5		1

## 5.8 Electrical Characteristics for $V_S = 15V$ or $\pm 7.5V$

at  $T_A = 25^\circ\text{C}$ ,  $V_+ = 15V$ ,  $V_- = 0V$ ,  $V_{CM} = 1.5V$ ,  $V_{OUT} = V_+ / 2$ , and  $R_L = 1M\Omega$  connected to  $V_+ / 2$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>OFFSET VOLTAGE</b>							
$V_{OS}$	Input offset voltage			$\pm 0.26$		mV	
$dV_{OS}/dT$	Input offset voltage drift	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		1		$\mu\text{V}/^\circ\text{C}$	
PSRR	Power-supply rejection ratio	Positive $V_+ = 5V$ to $15V$ , $V_- = 0V$ , $V_{OUT} = 1.5V$		62	82	dB	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	60	82		
		Negative $V_+ = -5V$ to $-15V$ , $V_- = 0V$ , $V_{OUT} = -1.5V$		65	82		
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	62	82		
<b>INPUT BIAS CURRENT</b>							
$I_B$	Input bias current			$\pm 1$		pA	
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			$\pm 1000$		
$I_{OS}$	Input offset current			$\pm 0.5$		pA	
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			$\pm 2000$		
<b>NOISE</b>							
$e_n$	Input voltage noise density	$f = 1\text{kHz}$ , $V_{CM} = 1V$		37		$\text{nV}/\sqrt{\text{Hz}}$	
$i_n$	Input current noise density	$f = 1\text{kHz}$		6.8		$\text{fA}/\sqrt{\text{Hz}}$	
THD	Total harmonic distortion	$f = 1\text{kHz}$ , $G = -2V/V$ , $R_L = 10\text{k}\Omega$ , $V_{OUT} = 8.5V_{pp}$		0.01		%	
<b>INPUT VOLTAGE</b>							
$V_{CM}$	Input common-mode voltage	To positive rail $V_+ = 15V$ , $\text{CMRR} > 50\text{dB}$		15.2	15.3	V	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	14.8	15.3		
		To negative rail $V_+ = 15V$ , $\text{CMRR} > 50\text{dB}$			-0.3		-0.2
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		-0.3		0.2
CMRR	Common-mode rejection ratio	$0V \leq V_{CM} \leq 15V$		62	82	dB	
		$0.2V \leq V_{CM} \leq 14.8V$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		60	82		
<b>INPUT IMPEDANCE</b>							
$R_{IN}$	Input resistance			$> 1$		$T\Omega$	
$C_{IN}$	Input capacitance			3		pF	
<b>OPEN-LOOP GAIN</b>							
$A_{OL}$	Open-loop voltage gain	Sourcing $7.5V < V_O < 12.5V$ , $V_{CM} = 1.5V$ $R_L = 2\text{k}\Omega$ to $7.5V$		80	340	V/mV	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	30	340		
		Sinking $2.5V < V_O < 7.5V$ , $V_{CM} = 1.5V$ $R_L = 2\text{k}\Omega$ to $7.5V$		15	24		
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	4	24		
		Sourcing, $V_{CM} = 1.5V$ , $7.5V < V_O < 12.5V$ , $R_L = 600\Omega$		34	300		
		Sinking, $V_{CM} = 1.5V$ , $2.5V < V_O < 7.5V$ , $R_L = 600\Omega$		6	15		

## 5.8 Electrical Characteristics for $V_S = 15V$ or $\pm 7.5V$ (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_+ = 15V$ ,  $V_- = 0V$ ,  $V_{CM} = 1.5V$ ,  $V_{OUT} = V_+ / 2$ , and  $R_L = 1M\Omega$  connected to  $V_+ / 2$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>FREQUENCY RESPONSE</b>							
GBW	Gain bandwidth product			1.1		MHz	
SR	Slew rate <sup>(1)</sup>	10V step, $R_L = 100k\Omega$ to 7.5V $V_{OUT} = 10V_{PP}$ , $f = 1kHz$		0.5	1.1	V/ $\mu$ s	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	0.4	1.1		
$\theta_m$	Phase margin			45		$^\circ$	
$G_m$	Gain margin			10		dB	
<b>OUTPUT</b>							
$V_O$	Voltage output swing	Positive rail $R_L = 2k\Omega$		14.4	14.7	V	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	14.2	14.7		
		Negative rail $R_L = 2k\Omega$			0.16		0.32
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		0.16		0.45
		Positive rail $R_L = 600\Omega$		13.4	14.1		
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	12.85	14.1		
Negative rail $R_L = 600\Omega$			0.5	1			
	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		0.5	1.5			
$I_{SC}$	Short-circuit current <sup>(2)</sup>	Sourcing $V_{OUT} = 0V$		30	50	mA	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	20	50		
		Sinking $V_{OUT} = 12V$		30	50		
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	20	50		
<b>POWER SUPPLY</b>							
$I_Q$	Quiescent current per amplifier			0.8	1.5	mA	
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		0.8	1.75		

(1) Number specified is the slower of the positive and negative slew rates.

(2) Do not short circuit output to  $V_+$  when  $V_+$  is greater than 12V or reliability can be adversely affected.

### 5.9 Typical Characteristics for $V_S = 2.7V$

at  $V_+ = 2.7V$ ,  $V_- = 0V$ , and  $T_A = 25^\circ C$  (unless otherwise specified)

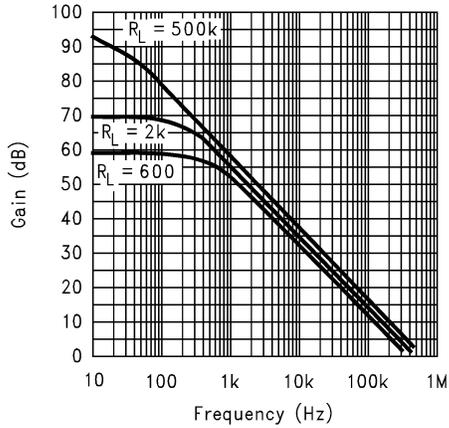


Figure 5-1. Open-Loop Frequency Response

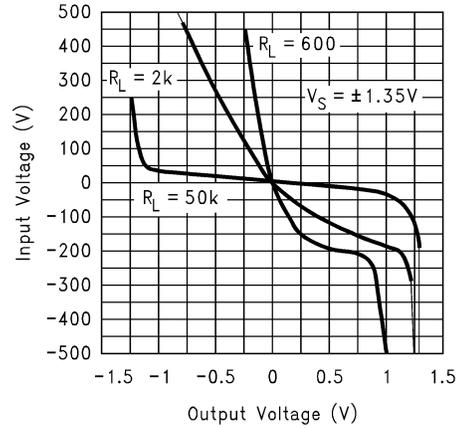


Figure 5-2. Input Voltage vs Output Voltage

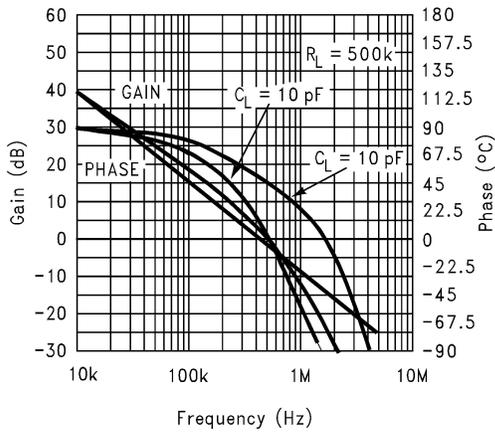


Figure 5-3. Gain and Phase vs Capacitance Load

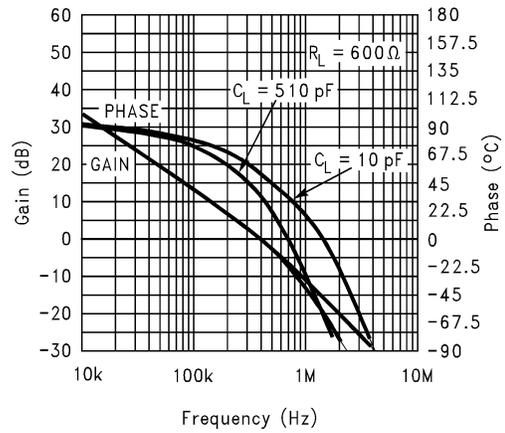


Figure 5-4. Gain and Phase vs Capacitance Load

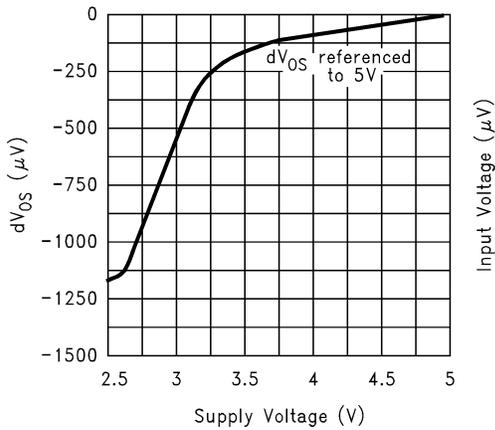


Figure 5-5.  $dV_{OS}$  vs Supply Voltage

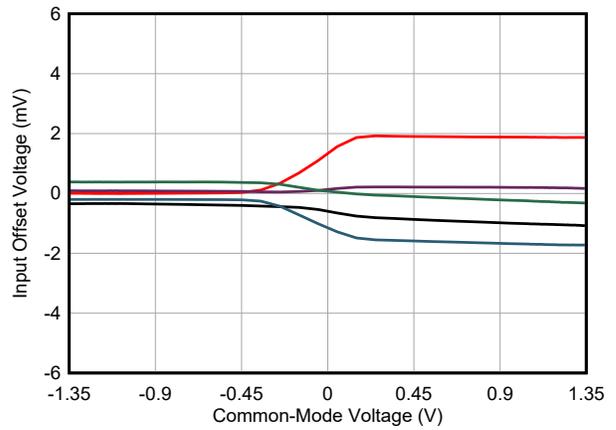
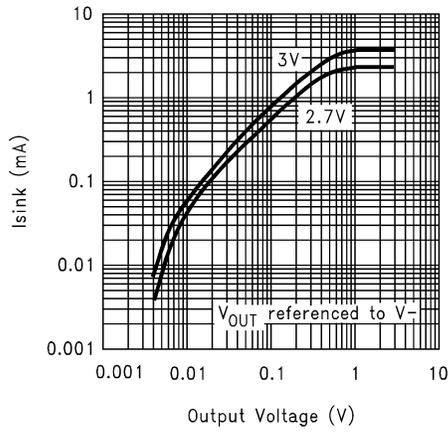


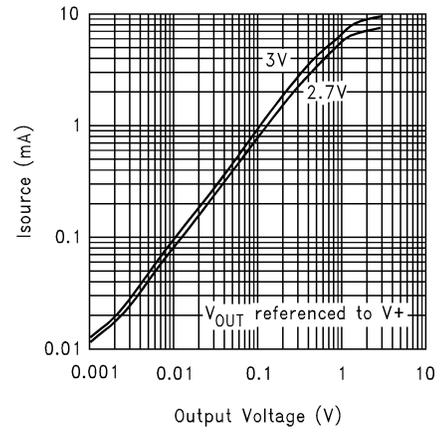
Figure 5-6. Input Offset Voltage vs Common-Mode Voltage

### 5.9 Typical Characteristics for $V_S = 2.7V$ (continued)

at  $V_+ = 2.7V$ ,  $V_- = 0V$ , and  $T_A = 25^\circ C$  (unless otherwise specified)



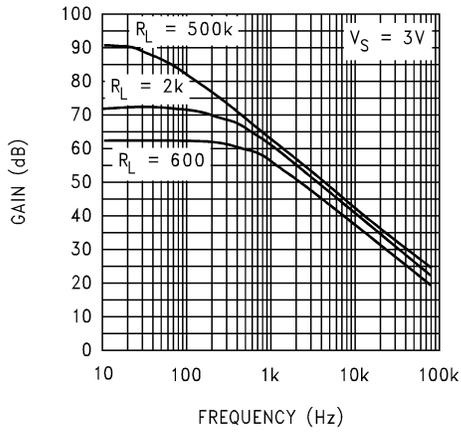
**Figure 5-7. Sinking Current vs Output Voltage**



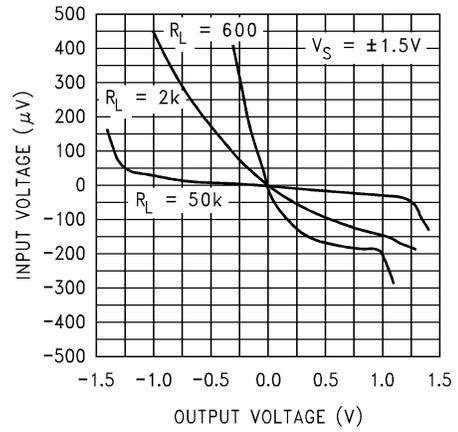
**Figure 5-8. Sourcing Current vs Output Voltage**

### 5.10 Typical Characteristics for $V_S = 3V$

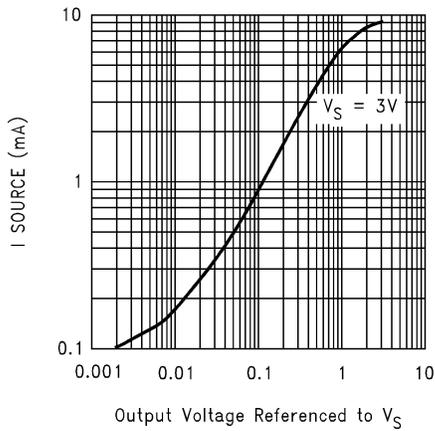
at  $V_+ = 3V$ ,  $V_- = 0V$ , and  $T_A = 25^\circ C$  (unless otherwise specified)



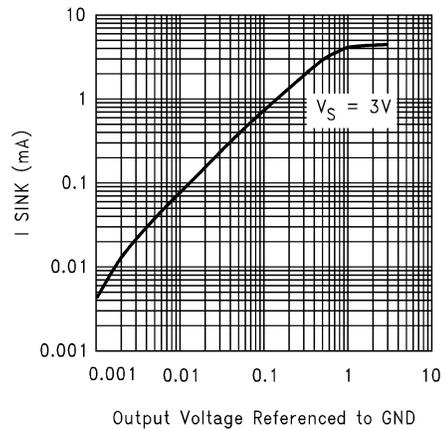
**Figure 5-9. Open-Loop Frequency Response**



**Figure 5-10. Input Voltage vs Output Voltage**



**Figure 5-11. Sourcing Current vs Output Voltage**



**Figure 5-12. Sinking Current vs Output Voltage**

### 5.11 Typical Characteristics for $V_S = 5V$

at  $V_+ = 5V$ ,  $V_- = 0V$ , and  $T_A = 25^\circ C$  (unless otherwise specified)

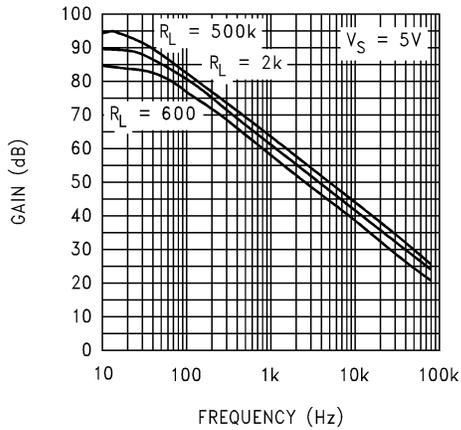


Figure 5-13. Open-Loop Frequency Response

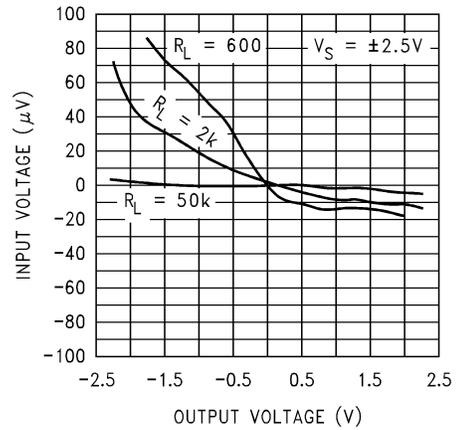


Figure 5-14. Input Voltage vs Output Voltage

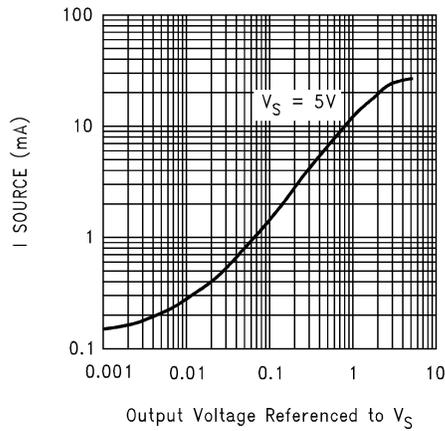


Figure 5-15. Sourcing Current vs Output Voltage

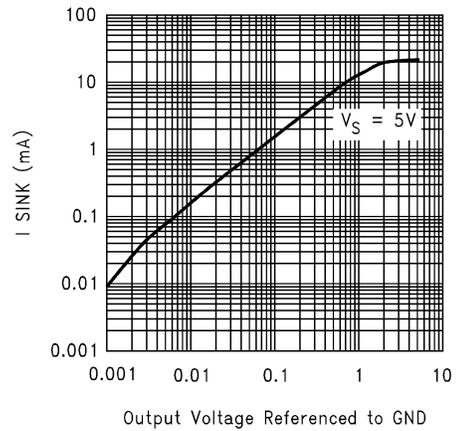


Figure 5-16. Sinking Current vs Output Voltage

### 5.12 Typical Characteristics for $V_S = 15V$

at  $V_+ = 15V$ ,  $V_- = 0V$ , and  $T_A = 25^\circ C$  (unless otherwise specified)

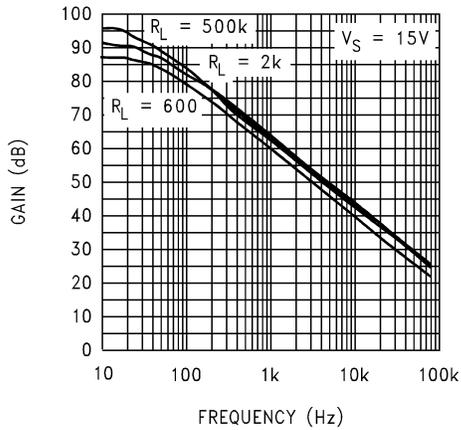


Figure 5-17. Open-Loop Frequency Response

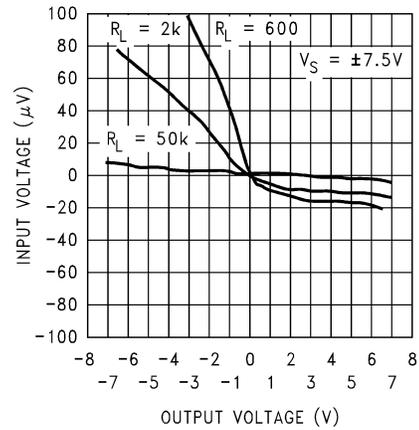


Figure 5-18. Input Voltage vs Output Voltage

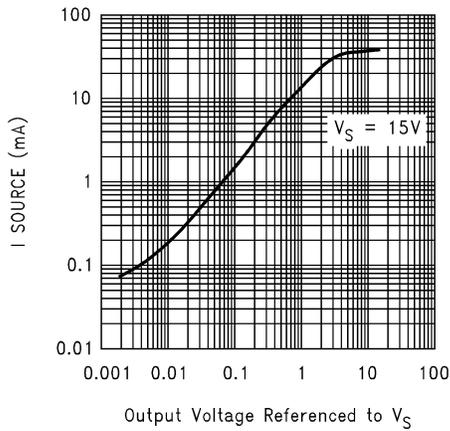


Figure 5-19. Sourcing Current vs Output Voltage

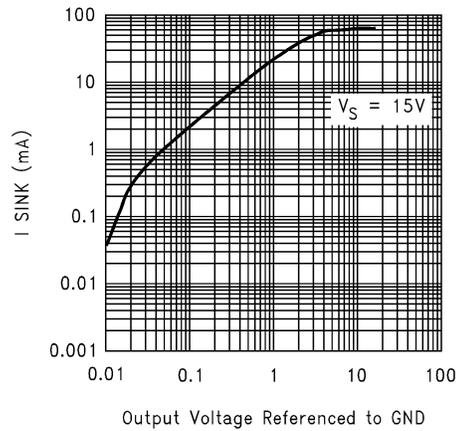


Figure 5-20. Sinking Current vs Output Voltage

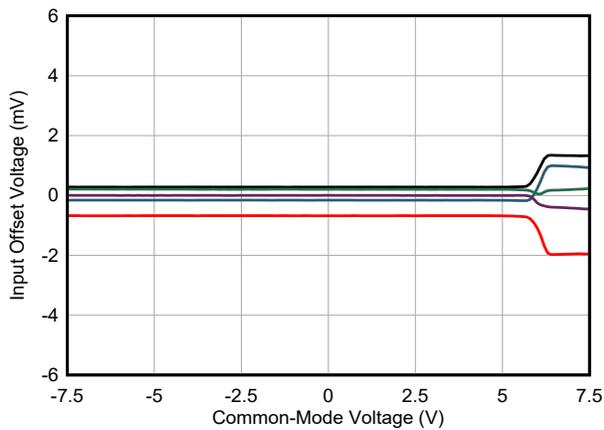


Figure 5-21. Input Offset Voltage vs Common-Mode Voltage

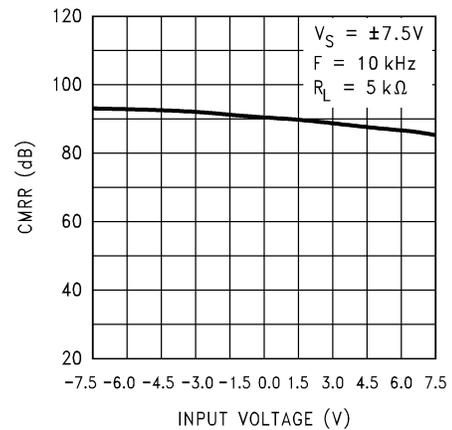


Figure 5-22. CMRR vs Input Voltage

### 5.12 Typical Characteristics for $V_S = 15V$ (continued)

at  $V_+ = 15V$ ,  $V_- = 0V$ , and  $T_A = 25^\circ C$  (unless otherwise specified)

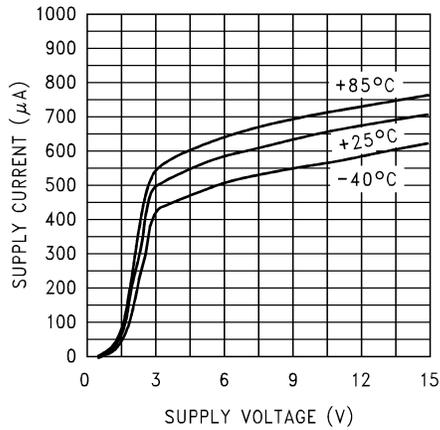


Figure 5-23. Supply Current vs Supply Voltage

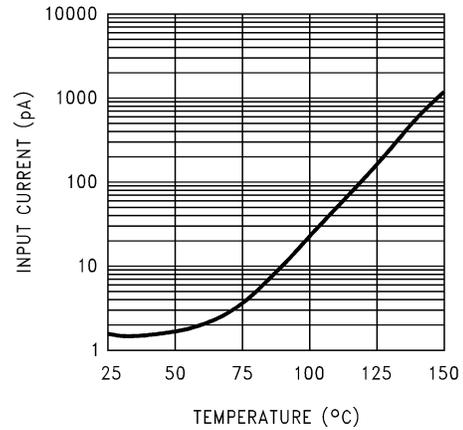


Figure 5-24. Input Current vs Temperature

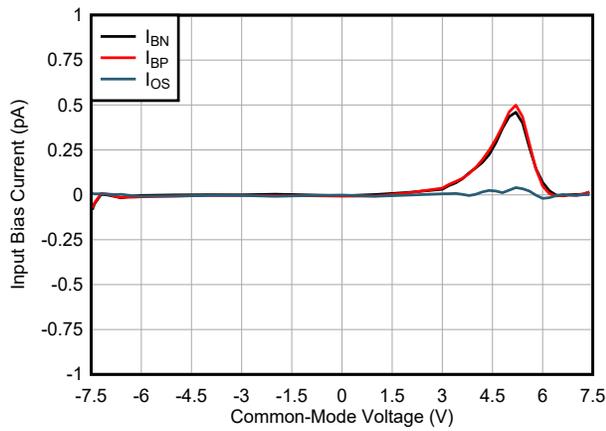


Figure 5-25. Input Bias Current vs Common-Mode Voltage

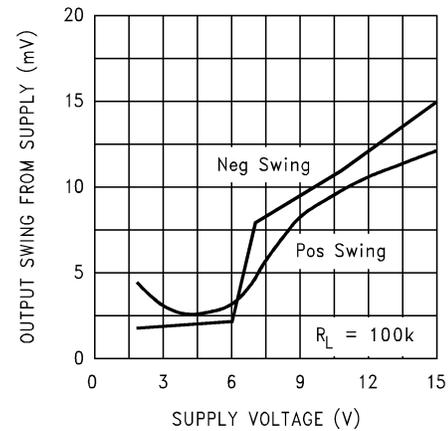


Figure 5-26. Output Voltage Swing vs Supply Voltage

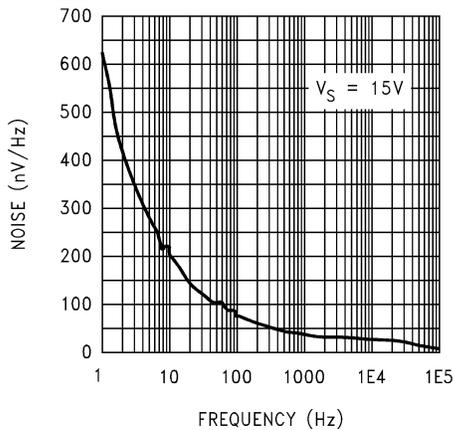


Figure 5-27. Input Voltage Noise vs Frequency

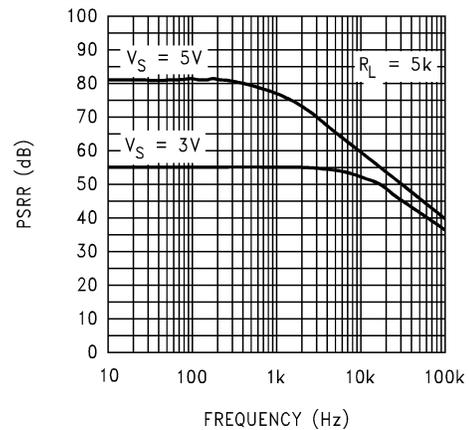
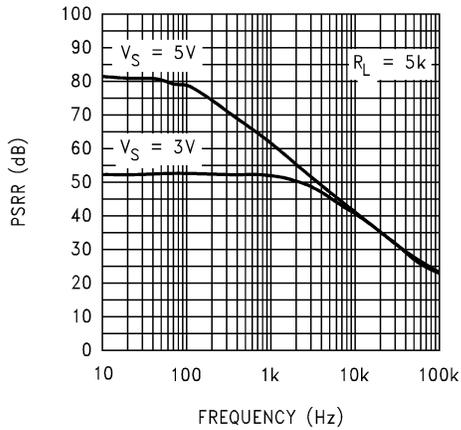


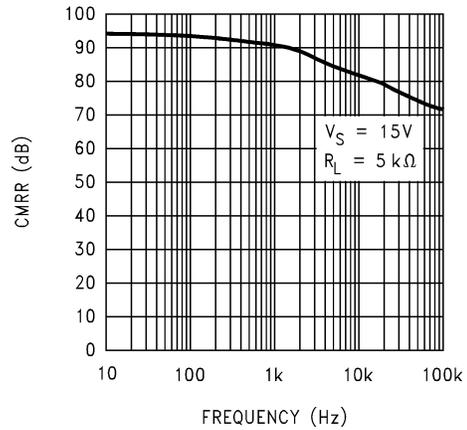
Figure 5-28. Positive PSRR vs Frequency

### 5.12 Typical Characteristics for $V_S = 15V$ (continued)

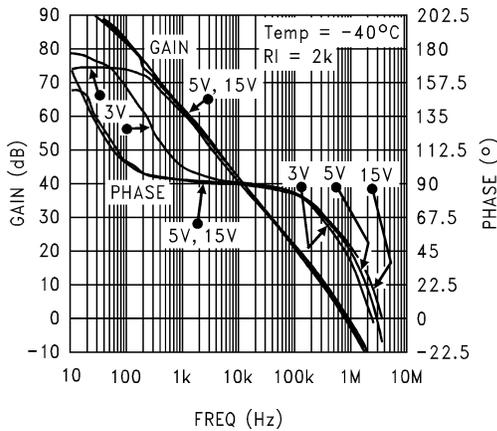
at  $V_+ = 15V$ ,  $V_- = 0V$ , and  $T_A = 25^\circ C$  (unless otherwise specified)



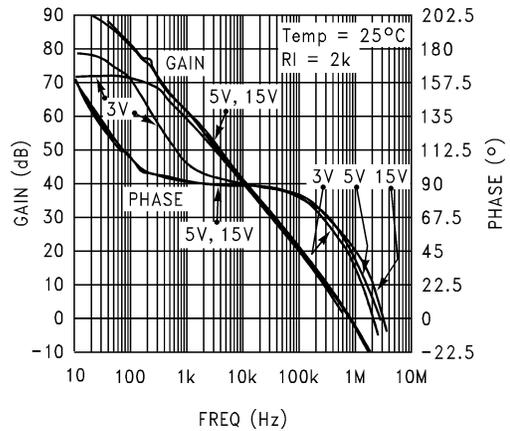
**Figure 5-29. Negative PSRR vs Frequency**



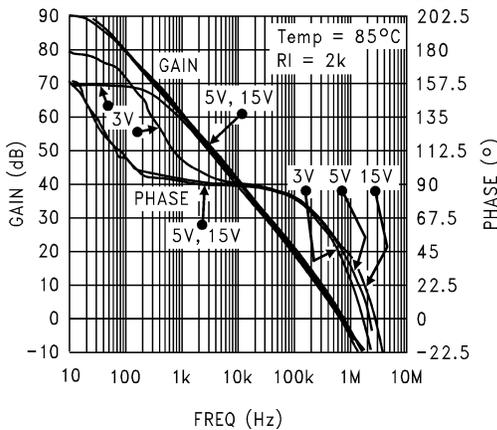
**Figure 5-30. CMRR vs Frequency**



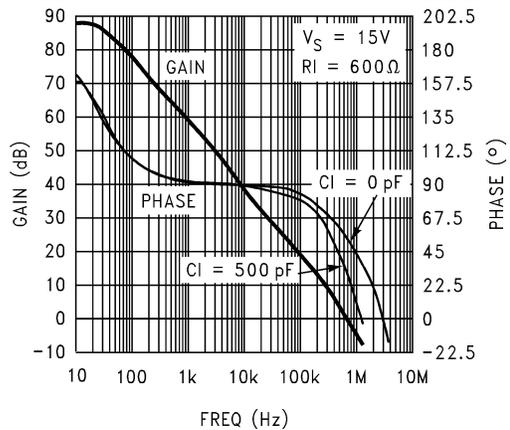
**Figure 5-31. Open-Loop Frequency Response at  $-40^\circ C$**



**Figure 5-32. Open-Loop Frequency Response at  $25^\circ C$**



**Figure 5-33. Open-Loop Frequency Response at  $85^\circ C$**



**Figure 5-34. Gain and Phase vs Capacitive Load**

### 5.12 Typical Characteristics for $V_S = 15V$ (continued)

at  $V_+ = 15V$ ,  $V_- = 0V$ , and  $T_A = 25^\circ C$  (unless otherwise specified)

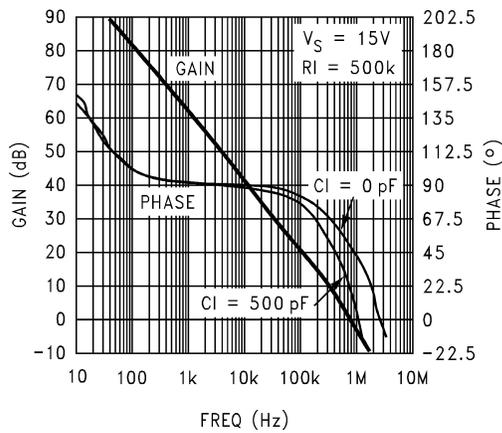


Figure 5-35. Gain and Phase vs Capacitive Load

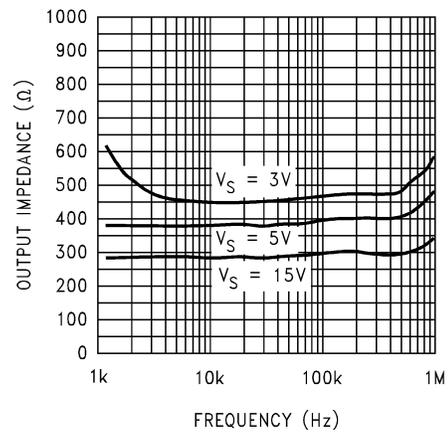


Figure 5-36. Output Impedance vs Frequency

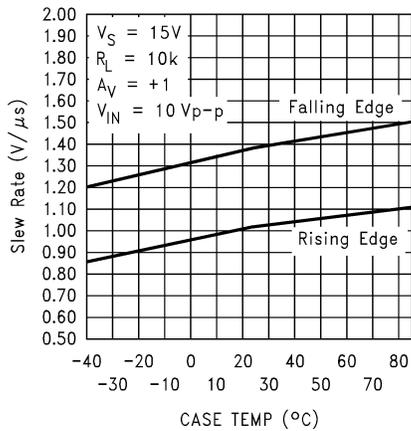


Figure 5-37. Slew Rate vs Temperature

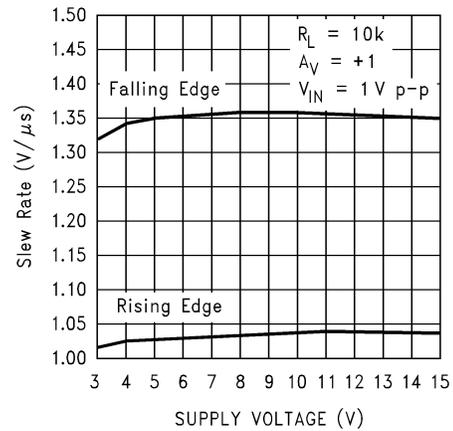


Figure 5-38. Slew Rate vs Supply Voltage

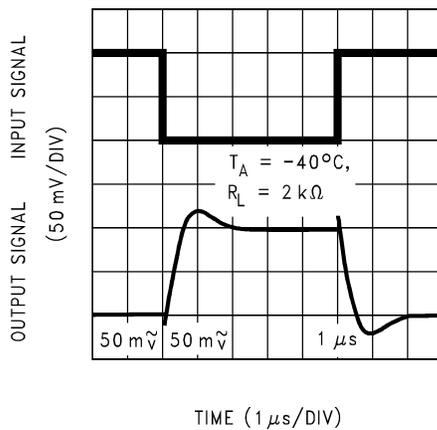


Figure 5-39. Inverting Small-Signal Pulse Response

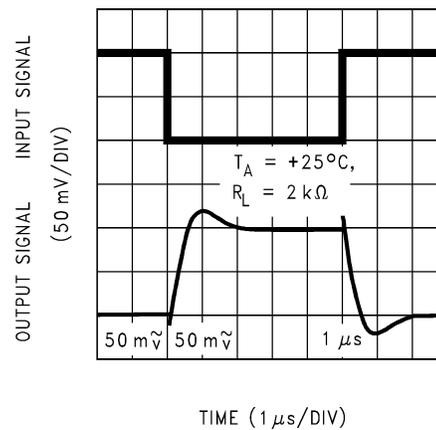
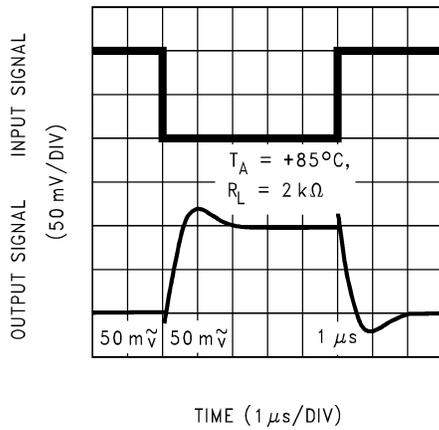


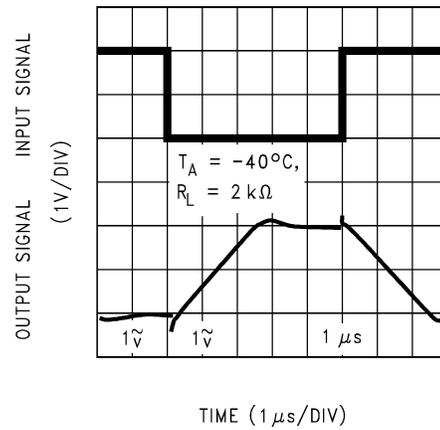
Figure 5-40. Inverting Small-Signal Pulse Response

### 5.12 Typical Characteristics for $V_S = 15V$ (continued)

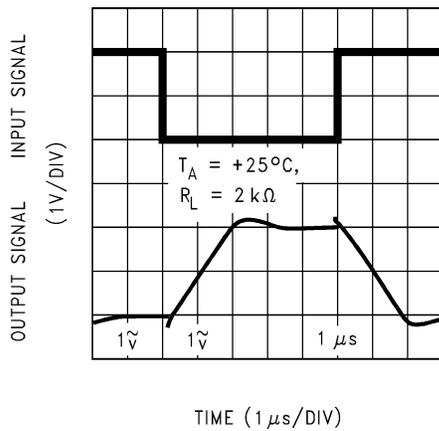
at  $V_+ = 15V$ ,  $V_- = 0V$ , and  $T_A = 25^\circ C$  (unless otherwise specified)



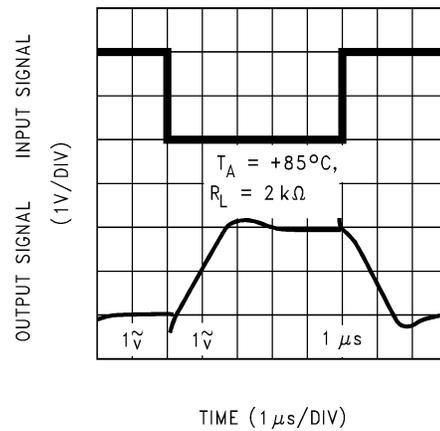
**Figure 5-41. Inverting Small-Signal Pulse Response**



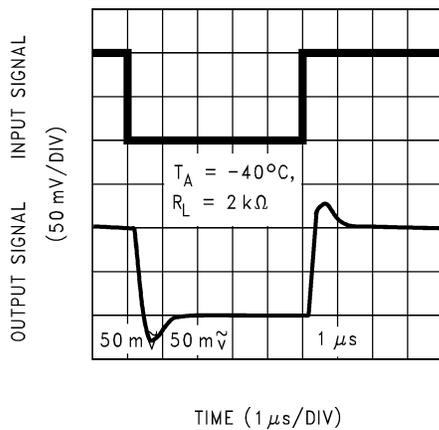
**Figure 5-42. Inverting Large-Signal Pulse Response**



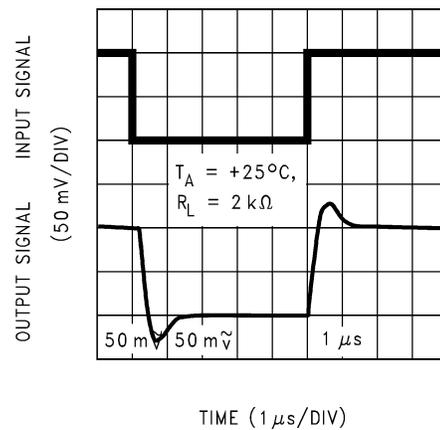
**Figure 5-43. Inverting Large-Signal Pulse Response**



**Figure 5-44. Inverting Large-Signal Pulse Response**



**Figure 5-45. Noninverting Small-Signal Pulse Response**



**Figure 5-46. Noninverting Small-Signal Pulse Response**

### 5.12 Typical Characteristics for $V_S = 15V$ (continued)

at  $V_+ = 15V$ ,  $V_- = 0V$ , and  $T_A = 25^\circ C$  (unless otherwise specified)

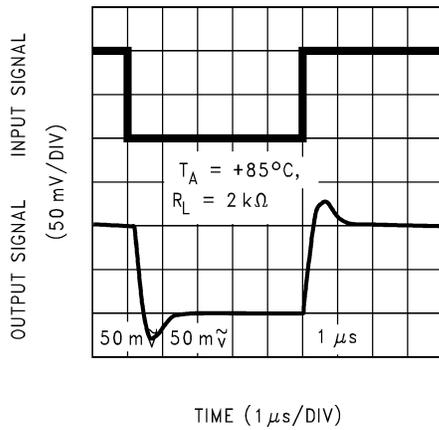


Figure 5-47. Noninverting Small-Signal Pulse Response

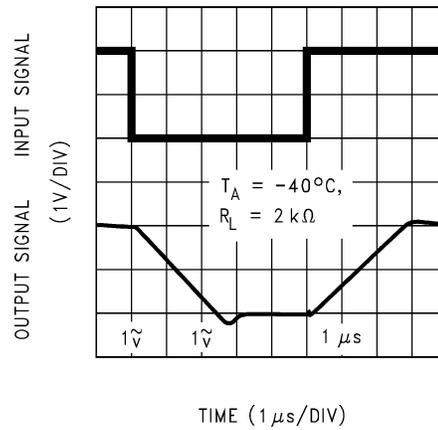


Figure 5-48. Noninverting Large-Signal Pulse Response

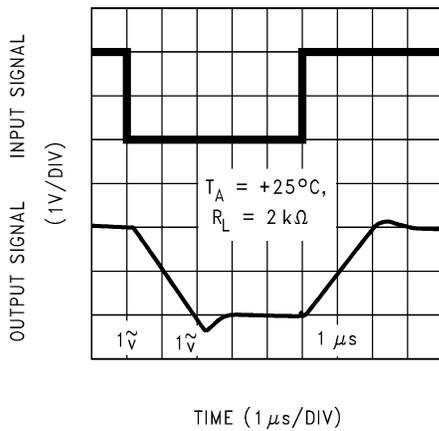


Figure 5-49. Noninverting Large-Signal Pulse Response

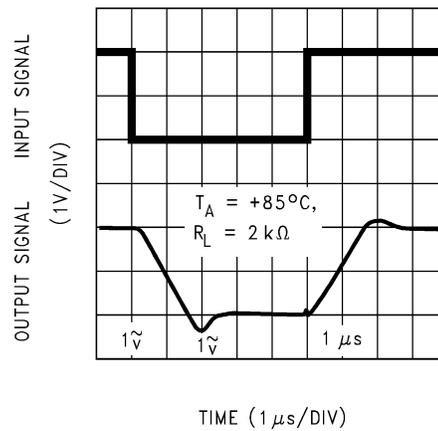


Figure 5-50. Noninverting Large-Signal Pulse Response

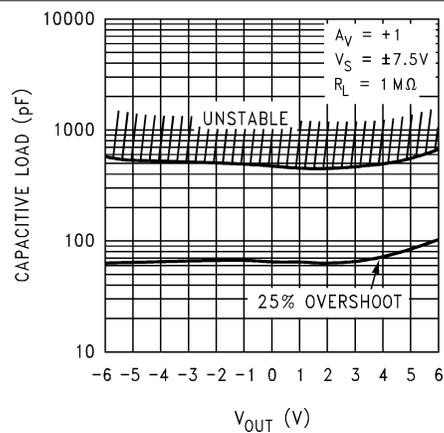


Figure 5-51. Stability vs Capacitive Load

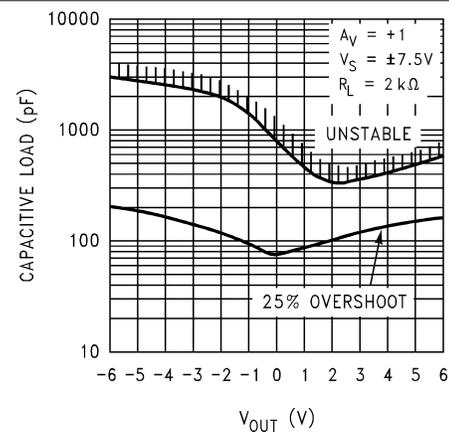
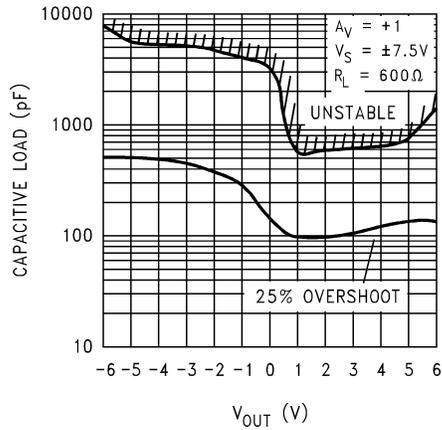


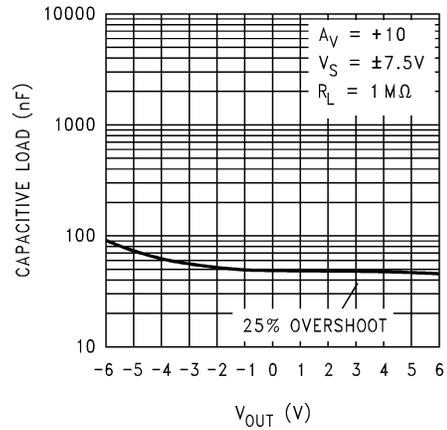
Figure 5-52. Stability vs Capacitive Load

### 5.12 Typical Characteristics for $V_S = 15V$ (continued)

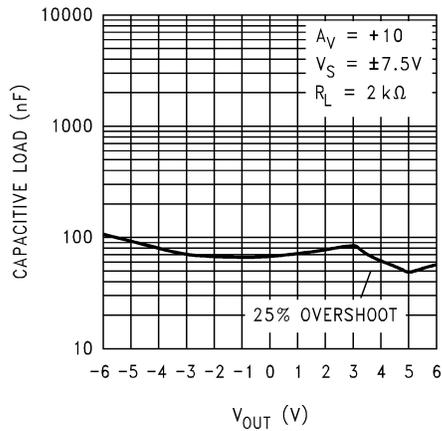
at  $V_+ = 15V$ ,  $V_- = 0V$ , and  $T_A = 25^\circ C$  (unless otherwise specified)



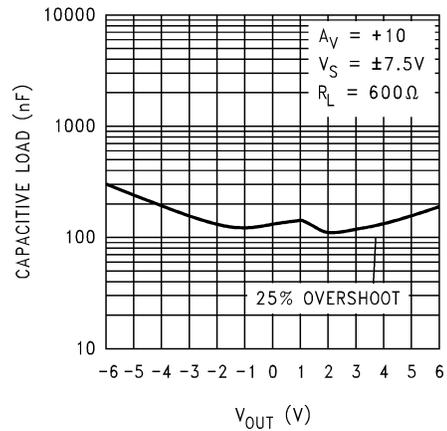
**Figure 5-53. Stability vs Capacitive Load**



**Figure 5-54. Stability vs Capacitive Load**



**Figure 5-55. Stability vs Capacitive Load**



**Figure 5-56. Stability vs Capacitive Load**

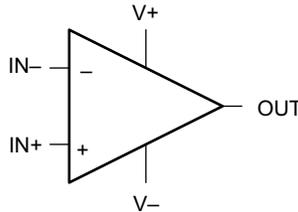
## 6 Detailed Description

### 6.1 Overview

The LMC7101Q-Q1 is a single-channel, low-power operational amplifier available in a space-saving SOT-23 package, offering rail-to-rail input and output operation across a wide range of power-supply configurations.

The LMC7101Q-Q1 is also available in a commercial-grade variant, see LMC7101.

### 6.2 Functional Block Diagram



### 6.3 Feature Description

#### 6.3.1 Benefits of the LMC7101 Tiny Amplifier

##### 6.3.1.1 Size

The small footprint of the SOT-23-5 packaged tiny amplifier, (0.12in × 0.118in, 3.05mm × 3mm) saves space on printed circuit boards, and enable the design of smaller electronic products. Many customers prefer smaller and lighter products because the designs can contribute to overall weight reduction in vehicles.

##### 6.3.1.2 Height

The 0.056 inches (1.43mm) height of the tiny LMC7101Q-Q1 amplifier makes the device an excellent choice for use in a wide range of circuit boards in which a thin profile is required.

##### 6.3.1.3 Signal Integrity

Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the tiny amplifier can be placed closer to the signal source, thus reducing noise pickup and increasing signal integrity. The tiny amplifier can also be placed next to the signal destination, such as a buffer, for the reference of an analog-to-digital converter.

##### 6.3.1.4 Simplified Board Layout

The tiny LMC7101Q-Q1 amplifier can simplify board layout in several ways. Avoid long PCB traces by correctly placing amplifiers instead of routing signals to a dual or quad device. By using multiple tiny amplifiers instead of duals or quads, complex signal routing and possibly crosstalk can be reduced.

##### 6.3.1.5 Low THD

The high open-loop gain of the LMC7101Q-Q1 amplifier helps to achieve very low audio distortion—typically 0.01% at 10kHz with a 10kΩ load at 5V supplies. This makes the tiny amplifier an excellent choice for automotive audio and low-frequency signal-processing applications.

##### 6.3.1.6 Low Supply Current

The typical 0.5mA supply current of the LMC7101Q-Q1 can help improve thermal performance on high density circuit boards, and can allow the reduction of the overall board size in some applications.

##### 6.3.1.7 Wide Voltage Range

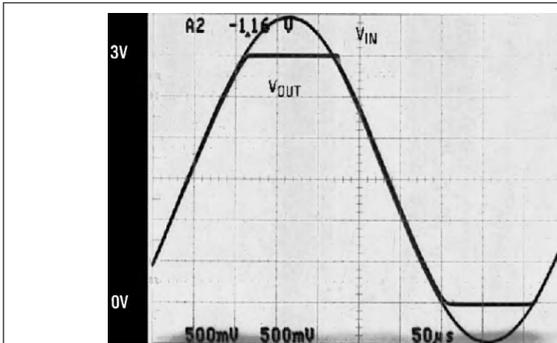
The LMC7101 is characterized at 15V, 5V and 3V. Performance data is provided at these popular voltages. This wide voltage range makes the LMC7101Q-Q1 a good choice for devices where the supply voltage can vary.

## 6.4 Device Functional Modes

### 6.4.1 Input Common-Mode Voltage Range

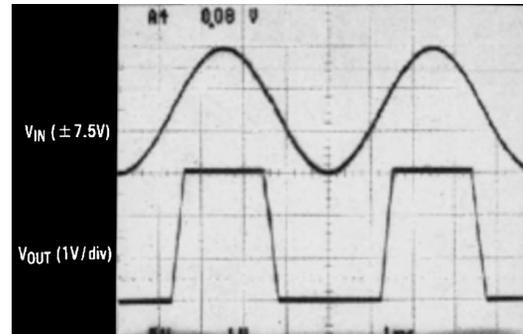
The LMC7101Q-Q1 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. [Figure 6-1](#) shows an input voltage exceeding both supplies with no resulting phase inversion of the output.

The absolute maximum input voltage is 300mV beyond either rail at room temperature. Voltages greatly exceeding this maximum rating, as in [Figure 6-2](#), can cause excessive current to flow in or out of the input pins, thus adversely affecting reliability.



The input voltage signal exceeds the amplifier power supply voltage with no output phase inversion.

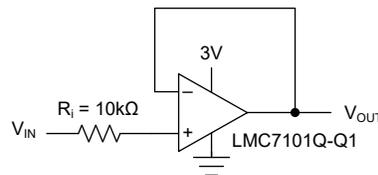
**Figure 6-1. Input Voltage**



The  $\pm 7.5\text{V}$  input signal greatly exceeds the 3V supply in [Figure 6-3](#) causing no phase inversion due to  $R_i$ .

**Figure 6-2. Input Signal**

Applications that exceed this rating must externally limit the maximum input current to  $\pm 5\text{mA}$  with an input resistor as shown in [Figure 6-3](#).



**Figure 6-3.  $R_i$  Input Current Protection for Voltages Exceeding the Supply Voltage**

## 7 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Application Information

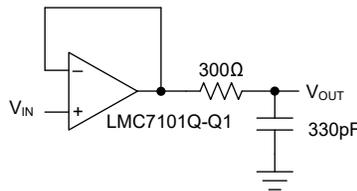
#### 7.1.1 Rail-to-Rail Output

The approximate output resistance of the LMC7101Q-Q1 is  $180\Omega$  sourcing and  $130\Omega$  sinking at  $V_S = 3V$  and  $110\Omega$  sourcing and  $80\Omega$  sinking at  $V_S = 5V$ . Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

#### 7.1.2 Capacitive Load Tolerance

The LMC7101Q-Q1 can typically directly drive a  $100pF$  load with  $V_S = 15V$  at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of operational amplifiers. The combination of the output impedance and the capacitive load of the operational amplifier induces phase lag, which results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in [Figure 7-1](#). This simple technique is useful for isolating the capacitive input of multiplexers and A/D converters.



**Figure 7-1. Resistive Isolation of a 330pF Capacitive Load**

### 7.1.3 Compensating for Input Capacitance When Using Large Value Feedback Resistors

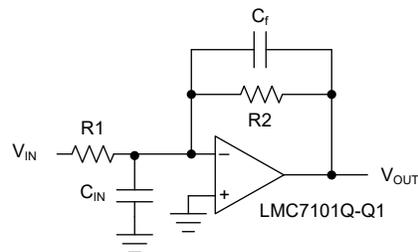
When using very large value feedback resistors, (usually >500 kΩ) the large feedback resistance can react with the input capacitance due to transducers, photo diodes, and circuit board parasitics to reduce phase margins.

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in [Figure 7-2](#)),  $C_f$  is first estimated by [Equation 1](#) and [Equation 2](#), which typically provides significant overcompensation.

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \quad (1)$$

$$2\pi R_1 C_{IN} \leq 2\pi R_2 C_f \quad (2)$$

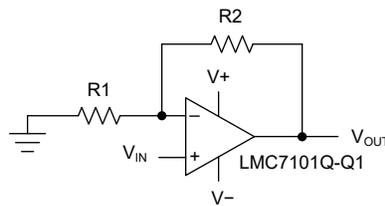
Printed circuit board stray capacitance can be larger or smaller than that of a breadboard, so the actual optimum value for  $C_f$  can be different. The values of  $C_f$  must be checked on the actual circuit.



**Figure 7-2. Canceling the Effect of Input Capacitance**

## 7.2 Typical Application

[Figure 7-3](#) shows a high input impedance noninverting circuit. This circuit gives a closed-loop gain equal to the ratio of the sum of  $R_1$  and  $R_2$  to  $R_1$  and a closed-loop 3dB bandwidth equal to the amplifier unity-gain frequency divided by the closed-loop gain. This design has the benefit of a very high input impedance, which is equal to the differential input impedance multiplied by loop gain (open loop gain / closed loop gain). In dc-coupled applications, input impedance is not as important as input current and the voltage drop across the source resistance. The amplifier output can go into saturation if the input is allowed to float, which can be important if the amplifier must be switched from source to source.



**Figure 7-3. Example Application**

### 7.2.1 Design Requirements

For this example application, the supply voltage is 5V, and  $100 \times \pm 5\%$  of noninverting gain is necessary. The signal input impedance is approximately 10k $\Omega$ .

### 7.2.2 Detailed Design Procedure

Use the equation for a noninverting amplifier configuration;  $G = 1 + R_2 / R_1$ , set  $R_1$  to 10k $\Omega$ , and  $R_2$  to  $99 \times R_1$ , which is 990k $\Omega$ . Replacing the 990k $\Omega$  resistor with a more readily available 1M $\Omega$  resistor results in a gain of 101, which is within the desired gain tolerance. The gain-frequency characteristic of the amplifier and the feedback network must be such that oscillation does not occur. To meet this condition, the phase shift through amplifier and feedback network must never exceed 180° for any frequency where the gain of the amplifier and the feedback network is greater than unity. In practical applications, the phase shift must not approach 180° because this is the situation of conditional stability. The most critical case occurs when the attenuation of the feedback network is zero.

### 7.2.3 Application Curve

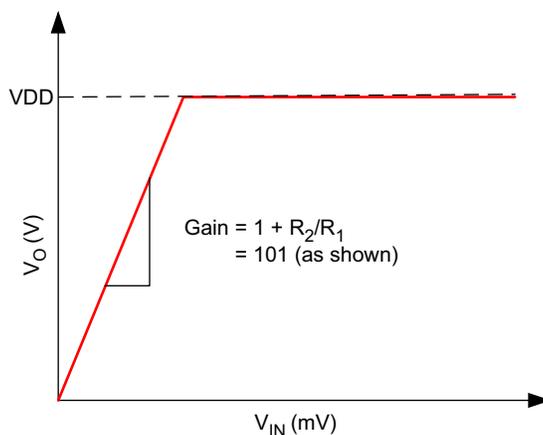


Figure 7-4. Output Response

### 7.3 Power Supply Recommendations

For proper operation, the power supplies must be decoupled. For supply decoupling, TI recommends placing 10nF to 1μF capacitors as close as possible to the operational-amplifier power supply pins. For single supply configurations, place a capacitor between the V+ and V- supply pins. For dual supply configurations, place one capacitor between V+ and ground, and place a second capacitor between V- and ground. Bypass capacitors must have a low ESR of less than 0.1Ω.

### 7.4 Layout

#### 7.4.1 Layout Guidelines

Care must be taken to minimize the loop area formed by the bypass capacitor connection between supply pins and ground. A ground plane underneath the device is recommended; any bypass components to ground must have a nearby via to the ground plane. The optimum bypass capacitor placement is closest to the corresponding supply pin. Use of thicker traces from the bypass capacitors to the corresponding supply pins can lower the power-supply inductance and provide a more stable power supply.

The feedback components must be placed as close as possible to the device to minimize stray parasitics.

#### 7.4.2 Layout Example

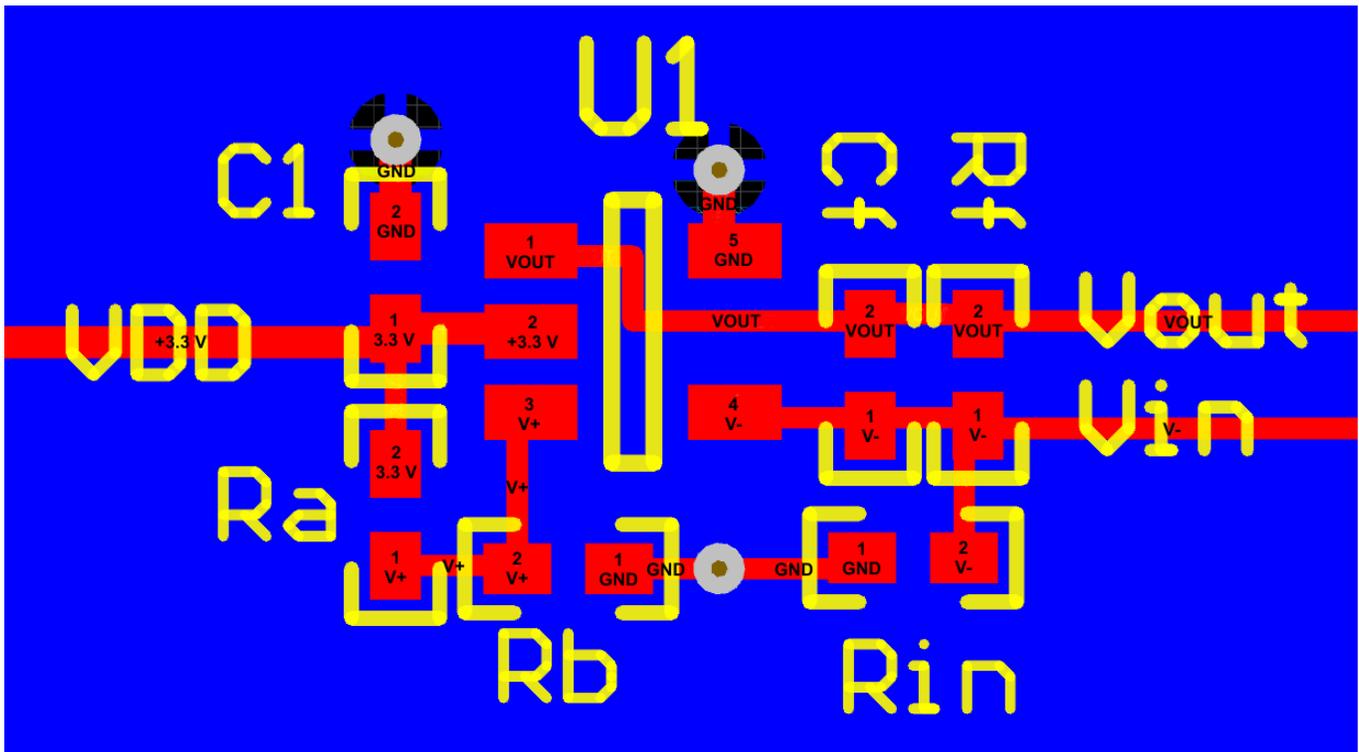


Figure 7-5. LMC7101Q-Q1 Example Layout

## 8 Device and Documentation Support

### 8.1 Documentation Support

#### 8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [LMC66x CMOS Dual Operational Amplifiers data sheet](#)
- Texas Instruments, [RES11A Matched, Thin-Film Resistor Dividers With 1kΩ Inputs data sheet](#)

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 8.4 Trademarks

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### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (September 2015) to Revision H (January 2025)	Page
• Moved LMC7101 commercial device into new SBOSAL2 data sheet.....	1
• Updated <i>Features</i> .....	1
• Updated <i>Description</i> .....	1
• Updated pin diagram figure and pin names in <i>Pin Configuration and Functions</i> .....	2
• Deleted Machine model (MM) from <i>ESD Ratings</i> .....	3
• Changed temperature test conditions from junction temperature, $T_J$ to ambient temperature, $T_A$ throughout...3	3
• Updated <i>Thermal Information</i> .....	3
• Updated formatting across all <i>Electrical Characteristics</i> .....	4
• Updated parameter names to be consistent with modern data sheets.....	4
• Added missing input offset voltage drift temperature condition in all <i>Electrical Characteristics</i> .....	4
• Updated temperature range conditions in input bias current and input offset current in all Electrical Characteristics.....	4
• Changed input common-mode voltage condition from $CMRR \geq 50\text{dB}$ to $CMRR \geq 47\text{dB}$ .....	4
• Changed $CMRR$ MIN from 50dB to 47dB.....	4
• Deleted footnotes 1 and 2 in all <i>Electrical Characteristics</i> .....	4

• Changed input common-mode voltage condition from CMRR > 50dB to CMRR > 47dB.....	5
• Changed CMRR MIN from 60dB to 47dB and TYP from 74dB to 70dB .....	5
• Changed CMRR MIN from 60dB to 52dB and TYP from 82dB to 75dB.....	6
• Changed CMRR MIN for T <sub>A</sub> = –40°C to +125°C from 60dB to 51dB and TYP from 82dB to 74dB.....	6
• Changed input common-mode voltage test condition from (V+) = 5V to (V+) = 15V.....	7
• Changed CMRR MIN from 65dB to 62dB.....	7
• Deleted Figures 6, 11, 14, 17, 20, 23, and 37.....	9
• Added Figure 5-6.....	9
• Added Figures 5-21 and 5-25.....	13
• Updated description text in <i>Size</i> .....	20
• Updated Figure 7-3, <i>Example Application</i> to show correct noninverting circuit.....	23

<b>Changes from Revision F (March 2013) to Revision G (September 2015)</b>	<b>Page</b>
• Added <i>Pin Configuration and Functions, ESD Ratings, Feature Description, Device Functional Modes, Application and Implementation, Power Supply Recommendations, Layout, Device and Documentation Support, and Mechanical, Packaging, and Orderable Information</i> sections.....	1

<b>Changes from Revision E (March 2013) to Revision F (March 2013)</b>	<b>Page</b>
• Changed layout of National Semiconductor Data Sheet to TI format.....	23

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">LMC7101QM5/NOPB</a>	Obsolete	Production	SOT-23 (DBV)   5	-	-	Call TI	Call TI	-40 to 125	AT6A
<a href="#">LMC7101QM5X/NOPB</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	Call TI   Sn	Level-1-260C-UNLIM	-40 to 125	AT6A
LMC7101QM5X/NOPB.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	AT6A
LMC7101QM5X/NOPB.B	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	AT6A

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

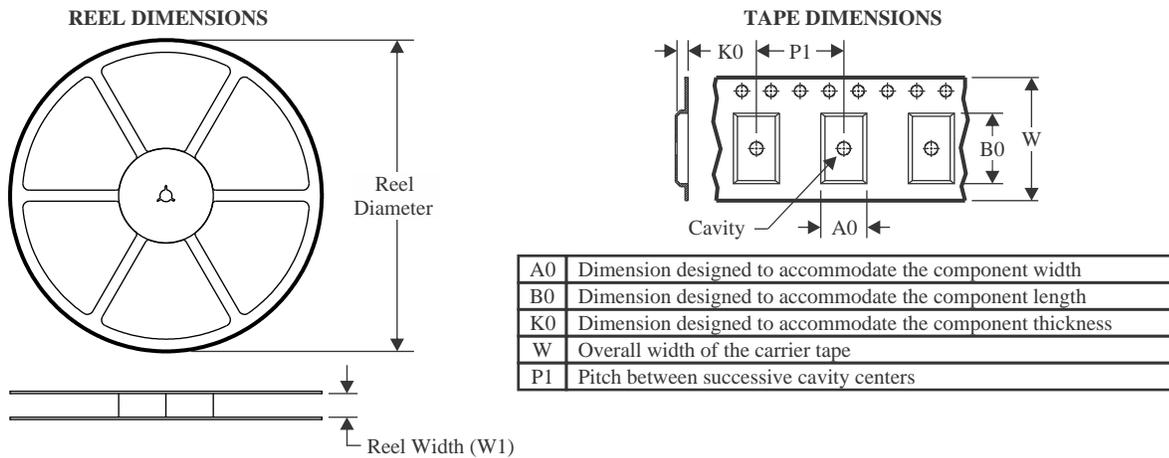
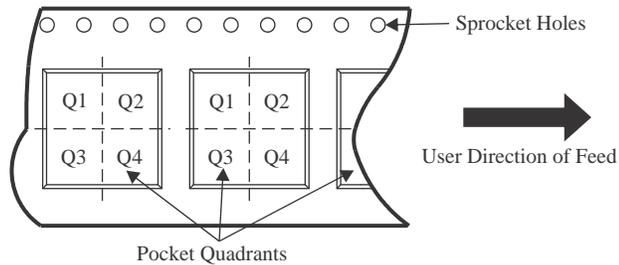
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

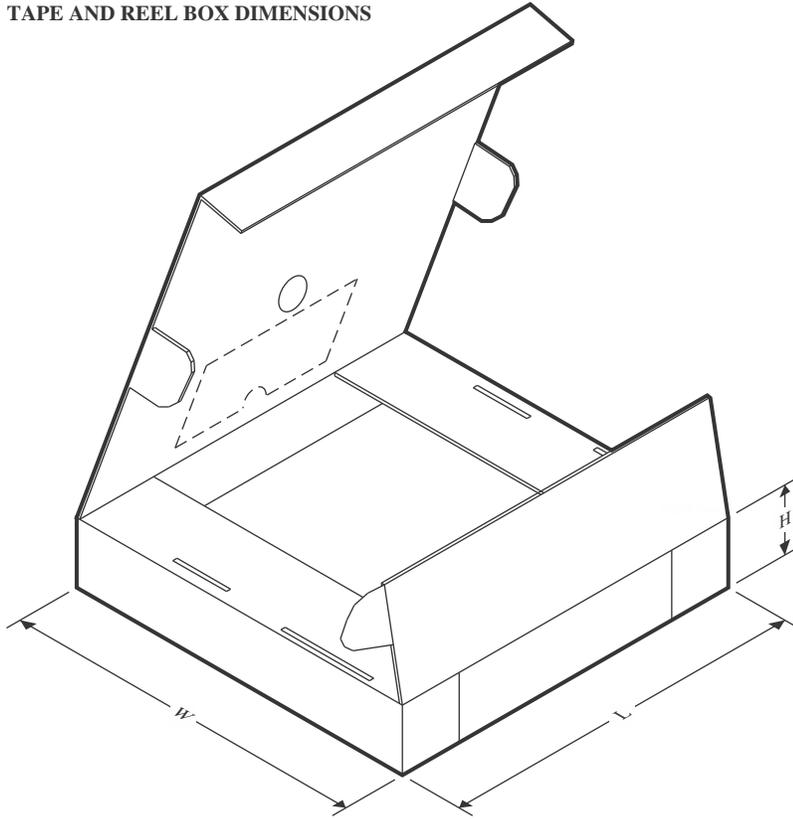
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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC7101QM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC7101QM5X/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0

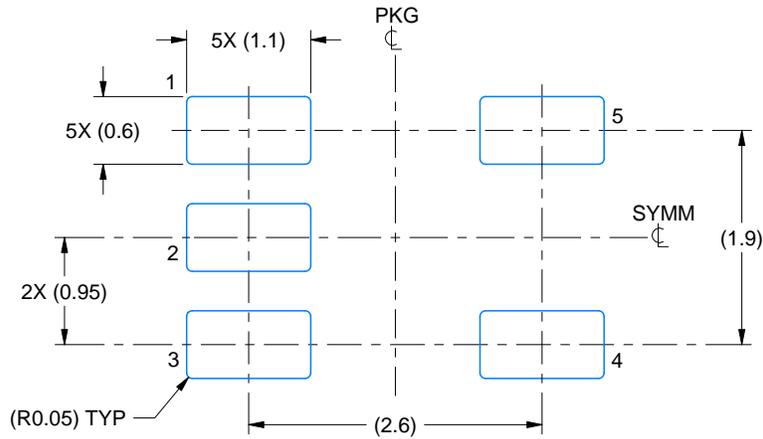


# EXAMPLE BOARD LAYOUT

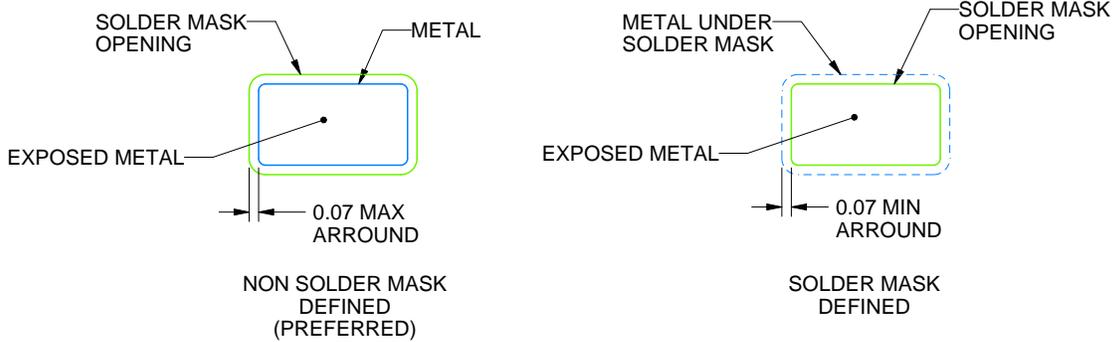
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

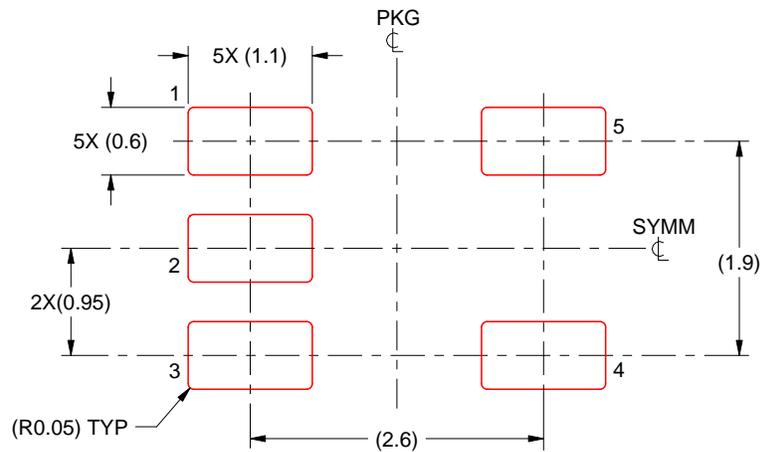
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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