

LMC7101 Tiny, Low-Power Operational Amplifier With Rail-to-Rail Input and Output

1 Features

- Tiny 5-Pin SOT-23 package saves space; typical circuit layouts take half the space of 8-pin SOIC designs
- Specified for 2.7V, 3V, 5V, and 15V supplies
- Typical supply current 0.5mA at 5V
- Typical total harmonic distortion of 0.01% at 5V
- 1MHz gain bandwidth
- Specified to industrial temperature: -40°C to +85°C
- Similar to popular LMC6482 and LMC6484
- Rail-to-rail input and output

2 Applications

- Mobile communications
- Notebooks and PDAs
- Battery-powered products
- Sensor interface
- Automotive applications

3 Description

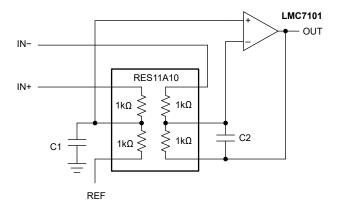
The LMC7101 device is a high-performance, automotive, CMOS operational amplifier available in a space-saving, 5-pin, SOT-23 tiny package. This design makes the LMC7101 an excellent choice for space- and weight-critical designs. The performance is similar to the single amplifier of the LMC6482 and LMC6484, with rail-to-rail input and output, high openloop gain, low distortion, and low-supply currents.

The main benefits of the tiny package are most apparent in small, portable electronic devices, such as mobile phones, pagers, notebook computers, personal digital assistants, and PCMCIA cards. The tiny amplifiers can be placed on a board where needed, thus simplifying board layout.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾		
LMC7101	DBV (SOT-23, 5)	2.9mm × 2.8mm		

- For more information, see Section 10.
- The package size (length × width) is a nominal value and includes pins, where applicable.



Difference Amplifier Application With RES11A



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4 Pin Configuration and Functions

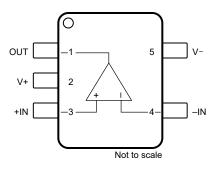


Figure 4-1. DBV Package, 5-Pin SOT-23 (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME	1175	DESCRIP HON
1	OUT	Output	Output
2	V+	Power	Positive supply
3	+IN	Input	Noninverting input
4	-IN	Input	Inverting input
5	V-	Power	Negative supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

	3 1 3 (MIN	MAX	UNIT
	Difference Input voltage		±Supply voltage	V
	Voltage at input and output pins	(V-) - 0.3	(V+) + 0.3	V
Vs	Supply voltage, $V_S = (V+) - (V-)$		16	V
	Current at input pin	-5	5	mA
	Current at output pin ⁽³⁾	-35	35	mA
	Current at power supply pin		35	mA
	Lead temperature (soldering, 10s)		260	°C
T _J	Junction temperature ⁽⁴⁾		150	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) If Military/Aerospace specified devices are required, contact the TI Sales Office or Distributors for availability and specifications.
- (3) Applies to both single-supply and split-supply operation. Continuous short operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C
- (4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$ and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly into a PC board.

5.2 ESD Ratings

			VALUE	UNIT
.,	Electrostatio discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000	V
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	\ \ \

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM MAX	UNIT
Vs	Supply voltage, $V_S = (V+) - (V-)$	2.7	15.5	V
T _J	Junction temperature	-40	85	°C

5.4 Thermal Information

		LMC7101			
	THERMAL METRIC ⁽¹⁾	DBV (SOT)	UNIT		
		5 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.5	°C/W		
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	128.5	°C/W		
$R_{\theta JB}$	Junction-to-board thermal resistance	88.9	°C/W		
Ψлт	Junction-to-top characterization parameter	66.8	°C/W		
Ψ_{JB}	Junction-to-board characterization parameter	88.6	°C/W		
R _{0JC(bot)}	Junction-to-case(bottom) thermal resistance	N/A	°C/W		

(1) For information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.



5.5 Electrical Characteristics for $V_S = \pm 1.35V$ or 2.7V

at T_J = 25°C, V+ = 2.7V, V- = 0V, V_{CM} = V_{OUT} = V+ / 2, and R_L > 1M Ω connected to V+ / 2 (unless otherwise noted)

	PARAMETER	TE	EST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET	VOLTAGE						
.,	l	LMC7101A			±0.11	±6	\/
V _{OS}	Input offset voltage	LMC7101B			±0.11	±9	mV
dV _{OS} /dT	Input offset voltage drift	$T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$			1		μV/°C
PSRR	Power-supply rejection ratio	V+ = 1.35V to 1.65V, V- =	= -1.35V to -1.65V, V _{CM} = 0V	45	60		dB
INPUT B	IAS CURRENT					<u> </u>	
I _B	Input bias current	$T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$			±1	±64	pА
I _{OS}	Input offset current	T _J = -40°C to +85°C			±0.5	±32	pA
INPUT V	OLTAGE		,				
.,	Input common-mode	F OMDD > 47-ID	Positive	2.7	3		V
V _{CM}	voltage	For CMRR ≥ 47dB	Negative		0	0	V
CMRR	Common-mode rejection	0V ≤ V _{CM} ≤ 2.7V	'	47	70		dB
INPUT IN	IPEDANCE		,				
R _{IN}	Input resistance				> 1		ΤΩ
C _{IN}	Common-mode input capacitance				3		pF
FREQUE	NCY RESPONSE		,			'	
GBW	Gain bandwidth product				0.6		MHz
SR	Slew rate ⁽¹⁾	(V+) = 15V, 10V step, R _L :	= 100kΩ to 7.5V, V _{OUT} = 10V _{PP} , f = 1kHz		0.7		V/µs
OUTPUT		<u> </u>					
		Positive rail	$R_L = 2k\Omega$	2.15	2.45		
.,	\/- \tau	Positive rail	$R_L = 10k\Omega$	2.64	2.68		
Vo	Voltage output swing	Negative rail	$R_L = 2k\Omega$		0.25	0.5	V
			$R_L = 10k\Omega$		0.025	0.06	
POWER	SUPPLY		·				
I.	Quiescent current per				500	810	^
IQ	amplifier	$T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$			500	950	μA

⁽¹⁾ Number specified is the slower of the positive and negative slew rates.



5.6 Electrical Characteristics for $V_S = \pm 1.5V$ or 3V

at T_J = 25°C, V+ = 3V, V- = 0V, V_{CM} = V_{OUT} = V+ / 2, and R_L = 1M Ω connected to V+ / 2 (unless otherwise noted)

	PARAMETER	TES	T CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET	VOLTAGE			•			
V _{OS} Input offset voltage		LMC7101A			±0.11	±3	mV
V _{OS}	input offset voltage	LMC7101B	LMC7101B		±0.11	±7	mv
dV _{OS} /dT	Input offset voltage drift	$T_J = -40$ °C to +85°C			1		μV/°C
	Power-supply rejection	V+ = 1.5V to 7.5V	LMC7101A	68	80		
PSRR	ratio	V = -1.5V to -7.5V $V_{OUT} = V_{CM} = 0V$	LMC7101B	60	80		dB
INPUT BI	IAS CURRENT						
I _B	Input bias current	$T_J = -40$ °C to +85°C			±1	±64	pA
Ios	Input offset current	$T_J = -40$ °C to +85°C			±0.5	±32	pA
INPUT V	OLTAGE						
\/	Input common-mode voltage		Positive	3	3.3		V
V _{CM}			Negative		0	0	V
CMRR	Common-mode rejection	$0V \le V_{CM} \le 3V$		47	70		dB
INPUT IM	IPEDANCE			,		-	
R _{IN}	Input resistance				> 1		TΩ
C _{IN}	Common-mode input capacitance				3		pF
ОИТРИТ						1	
		D 37	$R_L = 2k\Omega$	2.6	2.8		
.,		Positive rail	$R_L = 600\Omega$	2.5	2.7		.,
Vo	Voltage output swing	N14:	$R_L = 2k\Omega$		0.2	0.4	V
		Negative rail	R _L = 600Ω		0.37	0.6	
POWER	SUPPLY	<u>'</u>	'	<u>'</u>		'	
	Quiescent current per				500	810	
IQ	amplifier	$T_J = -40$ °C to +85°C			500	950	μA

Product Folder Links: LMC7101

5



5.7 Electrical Characteristics for $V_S = \pm 2.5V$ or 5V

at T_J = 25°C, V+ = 5V, V- = 0V, V_{CM} = V_{OUT} = V+ / 2, and R_L = 1M Ω connected to V+ / 2 (unless otherwise noted)

<u> </u>	PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET	VOLTAGE						
					±0.11	±3	
√ _{os}		LMC7101A	T _J = -40°C to +85°C		±0.11	±5	
V _{OS}	Input offset voltage				±0.11	±7	mV
PSRR PSRR POS NPUT BIA B OS NPUT VOI CMRR NPUT IMP RIN CIN		LMC7101B	$T_{.1} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$		±0.11	±9	
dV _{OS} /dT	Input offset voltage drift	T _J = -40°C to +85°C	J		1	-	μV/°C
	1 3	J	LMC7101A	70	82		
		Positive	LMC7101B	65	82		
PSRR		V+ = 5V to 15V V- = 0V, V _{OUT} = 1.5V	LMC7101A T _J = -40°C to +85°C	65	82		
	Power-supply rejection		LMC7101B T _J = -40°C to +85°C	62	82		
PSRR	ratio		LMC7101A	70	82		dB
		Negative	LMC7101B	65	82		
		V+ = -5V to -15V V- = 0V, V _{OUT} = -1.5V	LMC7101A T _J = -40°C to +85°C	65	82		
			LMC7101B T _J = -40°C to +85°C	62	82		
INPUT B	IAS CURRENT		,			"	
					±1		
I _B	Input bias current $T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$					±64	рA
					±0.5	±64	
los	Input offset current	$T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$				±32	рA
NOISE	"					1	
THD	Total harmonic distortion	f = 10kHz, G = -2V/V, R _L = 1	0 kΩ, $V_{OUT} = 4V_{pp}$		0.01		%
INPUT V	OLTAGE					1	
		To positive rail		5.2	5.3		
.,	Input common-mode	CMRR > 50dB	$T_J = -40$ °C to +85°C	5	5.3		.,
V _{CM}	voltage	To negative rail			-0.3	-0.2	V
		CMRR > 50dB	$T_J = -40$ °C to +85°C		-0.3	0	
01.100	Common-mode rejection	0)/ 1)/ 15//		52	75		i.
CMRR	ratio	$0V \le V_{CM} \le 5V$	$T_J = -40$ °C to +85°C	51	74		dB
INPUT IN	//PEDANCE		1			1	
R _{IN}	Input resistance				> 1		ТΩ
C _{IN}	Input capacitance				3		pF
FREQUE	NCY RESPONSE	•			,	<u>'</u>	
GBW	Gain bandwidth product				1		MHz
SR	Slew rate				1		V/µs

5.7 Electrical Characteristics for $V_S = \pm 2.5V$ or 5V (continued)

 $\underline{\text{at T}_{\text{J}} = 25^{\circ}\text{C, V+} = 5\text{V, V-} = 0\text{V, V}_{\text{CM}} = \text{V}_{\text{OUT}} = \text{V+} \text{/} 2, \text{ and R}_{\text{L}} = 1\text{M}\Omega \text{ connected to V+} \text{/} 2 \text{ (unless otherwise noted)}$

	PARAMETER	TI	EST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPU	Т						
V _O		Positive rail		4.7	4.9		
		$R_L = 2k\Omega$	$T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	4.6	4.9		
		Negative rail			0.1	0.18	
	Valtage entrut entire	$R_L = 2k\Omega$	$T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$		0.1	0.24	V
	voltage output swing	/oltage output swing		4.5	4.7		V
			$T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	4.24	4.7		
					0.3	0.5	
			$T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$		0.3	0.65	
		Sourcing		16	24		
	Short-circuit current	V _{OUT} = 0V	$T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	11	24		A
I _{SC}	Short-circuit current	Sinking		11	19		mA
		V _{OUT} = 5V	$T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	7.5	19		
POWER	R SUPPLY				,		
1.	Quiescent current per				0.5	0.85	
IQ	amplifier	$T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$			0.5	1	mA



5.8 Electrical Characteristics for $V_S = \pm 7.5V$ or 15V

at T_J = 25°C, V+ = 15V, V- = 0V, V_{CM} = V_{OUT} = V+ / 2, and R_L = 1M Ω connected to V+ / 2 (unless otherwise noted)

	PARAMETER	TEST CO	NDITIONS	MIN	TYP	MAX	UNIT
OFFSET	VOLTAGE						
V _{OS}	Input offset voltage				±0.26		mV
dV _{OS} /dT	Input offset voltage drift	$T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$			1		μV/°C
			LMC7101A	70	82		
		Positive	LMC7101B	65	82		
		V+ = 5V to 15V V- = 0V, V _{OUT} = 1.5V	LMC7101A T _J = -40°C to +85°C	65	82		
PSRR	Power-supply rejection		LMC7101B T _J = -40°C to +85°C	60	82		٦D
FORK	ratio		LMC7101A	70	82		dB
		Negative	LMC7101B	65	82		
		V+ = -5V to -15V V- = 0V, V _{OUT} = -1.5V	LMC7101A T _J = -40°C to +85°C	65	82		
			LMC7101B T _J = -40°C to +85°C	62	82		
INPUT BI	AS CURRENT						
	Innut hing gurrant	land him a summer			±1		- ^
I _B	Input bias current	$T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$					pA
	l				±0.5		^
los	Input offset current $T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$					±32	рA
NOISE	1	-		-		'	
e _n	Input voltage noise density	f = 1kHz, V _{CM} = 1V			37		nV/√ Hz
i _n	Input current noise density	f = 1kHz			6.8		fA/√ Hz
THD	Total harmonic distortion	$f = 10kHz, G = -2V/V, R_L = 10k\Omega$	o, V _{OUT} = 8.5V _{pp}		0.01		%
INPUT VO	DLTAGE					'	
		To positive rail		15.2	15.3		
.,	Input common-mode CMRR > 50dB		$T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	15	15.3		.,
V _{CM}	voltage	To negative rail			-0.3	-0.2	V
		CMRR > 50dB	$T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$		-0.3	0	
01100	Common-mode rejection	01/ -1/ -1/51/		62	82		···
CMRR	ratio	0V ≤ V _{CM} ≤15V	$T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	60	82		dB
INPUT IM	PEDANCE		1				
R _{IN}	Input resistance				> 1		ΤΩ
C _{IN}	Input capacitance				3		pF
OPEN-LO	OOP GAIN						
		Sourcing 7.5V < V _O < 12.5V, V _{CM} = 1.5V		80	340		
		$R_L = 2k\Omega$ to 7.5V	$T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	40	340		
•	0	Sinking		15	24		
A _{OL}	Open-loop voltage gain	$2.5V < V_O < 7.5V, V_{CM} = 1.5V$ R _L = $2k\Omega$ to $7.5V$	$T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	10	24		V/mV
		Sourcing, V _{CM} = 1.5V, 7.5V < V _O	< 12.5V, R _L = 600Ω	34	300		
		Sinking, V _{CM} = 1.5V, 2.5V < V _O <	7.5V, R _L = 600Ω	6	15		

5.8 Electrical Characteristics for $V_S = \pm 7.5V$ or 15V (continued)

at $T_J = 25$ °C, V+ = 15V, V- = 0V, $V_{CM} = V_{OUT} = V + / 2$, and $R_L = 1M\Omega$ connected to V+ / 2 (unless otherwise noted)

	PARAMETER	TEST	CONDITIONS	MIN	TYP	MAX	UNIT	
FREQU	ENCY RESPONSE							
GBW	Gain bandwidth product				1.1		MHz	
SR	- (4)	V _S = 15V, 10V step,		0.5	1.1			
	Slew rate ⁽¹⁾	R_L = 100kΩ to 7.5V V _{OUT} = 10V _{PP} , f = 1kHz	$T_{J} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	0.4	1.1		V/µs	
θ_{m}	Phase margin				45		۰	
G _m	Gain margin				10		dB	
OUTPU	Т							
		Positive rail		14.4	14.7			
	Voltage output swing	$R_L = 2k\Omega$	$T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	14.2	14.7		V	
		$\begin{array}{c} \text{Negative rail} \\ \text{R}_{L} = 2k\Omega \\ \\ \text{positive rail} \\ \text{R}_{L} = 600\Omega \end{array}$			0.16	0.32		
V			$T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$		0.16	0.45		
Vo				13.4	14.1			
			$T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	13	14.1			
		Negative rail			0.5	1	ī	
		$R_L = 600\Omega$	$T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$		0.5	1.3		
	01 1 1 1 (2)	Sourcing		30	50			
		nort-circuit current ⁽²⁾ Vout = 0V Sinking	$T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	20	50		ma A	
I _{SC}	Short-Gircuit Gurrentte			30	50		mA	
		V _{OUT} = 12V	$T_J = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	20 50				
POWER	R SUPPLY	<u> </u>	·					
	Quiescent current per				0.8	1.5	m۸	
IQ	amplifier	$T_J = -40$ °C to +85°C	$T_{J} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$			1.71	mA	

⁽¹⁾ Number specified is the slower of the positive and negative slew rates.

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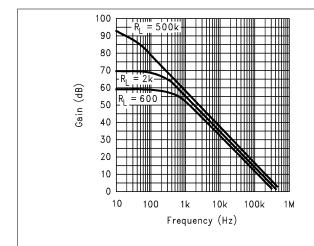
Product Folder Links: LMC7101

⁽²⁾ Do not short circuit output to V+ when V+ is greater than 12V or reliability can be adversely affected.



5.9 Typical Characteristics for $V_S = 2.7V$

at V+ = 2.7V, V- = 0V, and T_A = 25°C (unless otherwise specified)

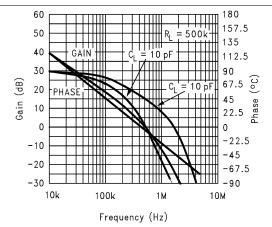


A COUTPUT Voltage (V)

500

Figure 5-1. Open-Loop Frequency Response

Figure 5-2. Input Voltage vs Output Voltage



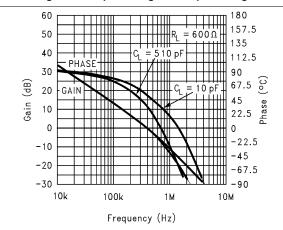
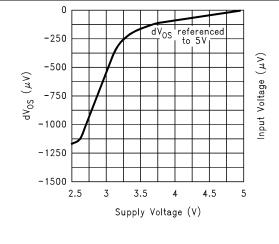


Figure 5-3. Gain and Phase vs Capacitance Load

Figure 5-4. Gain and Phase vs Capacitance Load



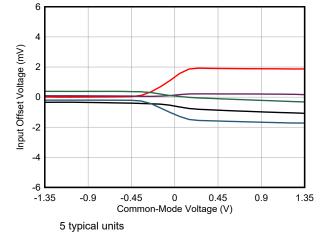
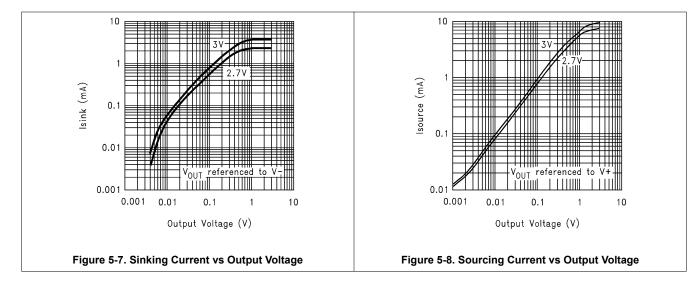


Figure 5-5. dV_{OS} vs Supply Voltage Figure 5-6. Input Offset Voltage vs Common-Mode Voltage



at V+ = 2.7V, V $_-$ = 0V, and T_A = 25°C (unless otherwise specified)





5.10 Typical Characteristics for $V_S = 3V$

at V+ = 3V, V- = 0V, and T_A = 25°C (unless otherwise specified)

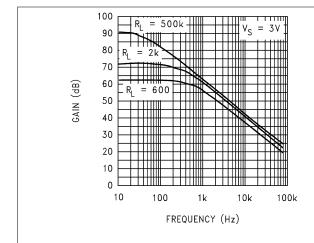


Figure 5-9. Open-Loop Frequency Response

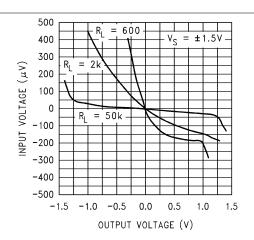


Figure 5-10. Input Voltage vs Output Voltage

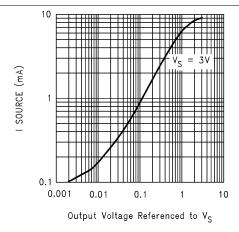


Figure 5-11. Sourcing Current vs Output Voltage

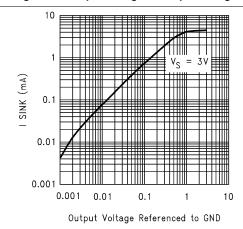


Figure 5-12. Sinking Current vs Output Voltage

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5.11 Typical Characteristics for $V_S = 5V$

at V+ = 5V, V- = 0V, and T_A = 25°C (unless otherwise specified)

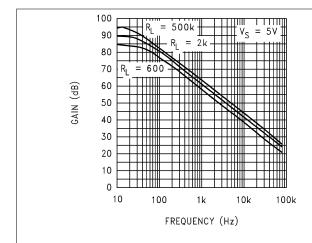


Figure 5-13. Open-Loop Frequency Response

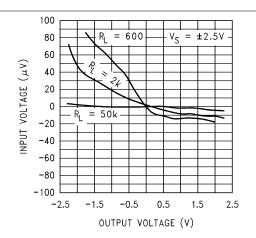


Figure 5-14. Input Voltage vs Output Voltage

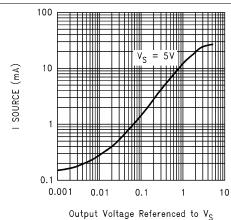


Figure 5-15. Sourcing Current vs Output Voltage

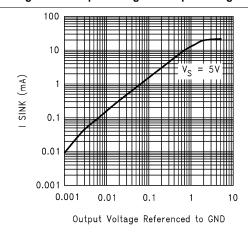


Figure 5-16. Sinking Current vs Output Voltage



5.12 Typical Characteristics for $V_S = 15V$

at V+ = 15V, V- = 0V, and T_A = 25°C (unless otherwise specified)

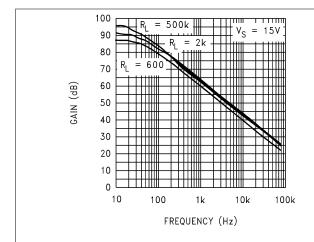


Figure 5-17. Open-Loop Frequency Response

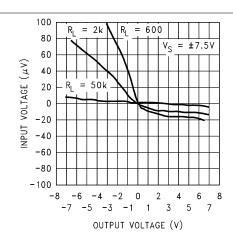


Figure 5-18. Input Voltage vs Output Voltage

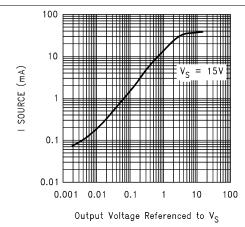


Figure 5-19. Sourcing Current vs Output Voltage

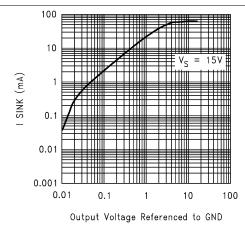
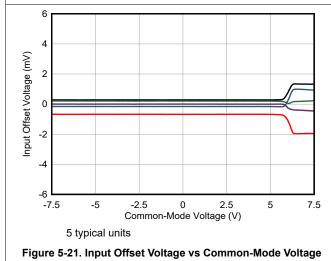


Figure 5-20. Sinking Current vs Output Voltage



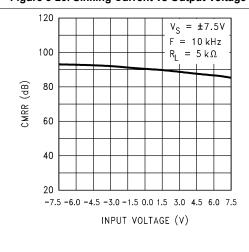


Figure 5-22. CMRR vs Input Voltage

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at V+ = 15V, V- = 0V, and T_A = 25°C (unless otherwise specified)

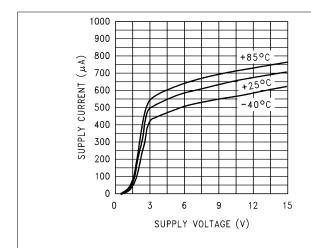


Figure 5-23. Supply Current vs Supply Voltage

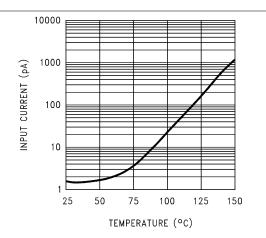


Figure 5-24. Input Current vs Temperature

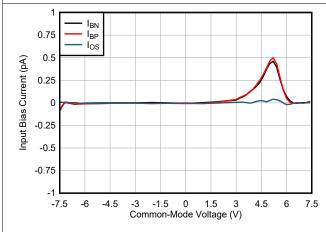


Figure 5-25. Input Bias Current vs Common-Mode Voltage

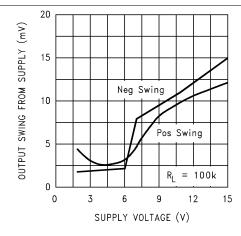


Figure 5-26. Output Voltage Swing vs Supply Voltage

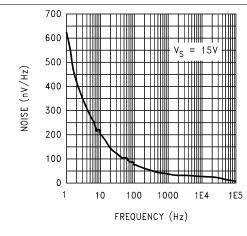


Figure 5-27. Input Voltage Noise vs Frequency

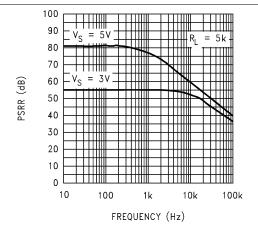
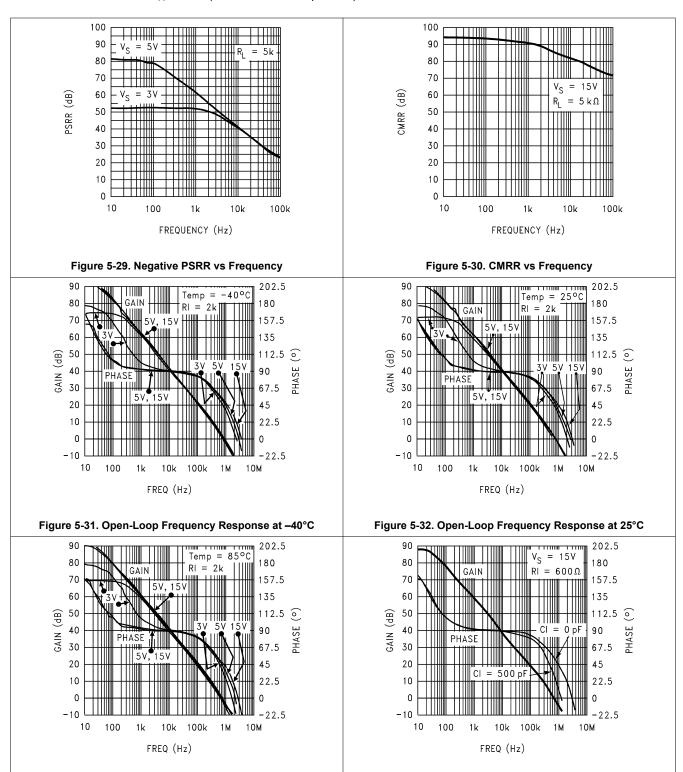


Figure 5-28. Positive PSRR vs Frequency



at V+ = 15V, V- = 0V, and T_A = 25°C (unless otherwise specified)



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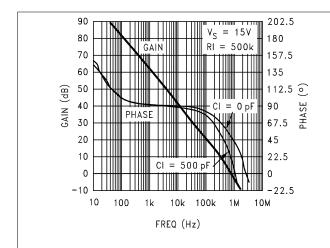
Figure 5-33. Open-Loop Frequency Response at 85°C

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Figure 5-34. Gain and Phase vs Capacitive Load



at V+ = 15V, V $_-$ = 0V, and T $_A$ = 25°C (unless otherwise specified)

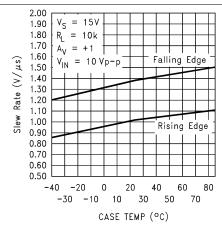


900 800 OUTPUT IMPEDANCE (\Omega) 700 600 = 3V **∏** 500 400 300 200 100 0 1k 10k 100k 1 M FREQUENCY (Hz)

1000

Figure 5-35. Gain and Phase vs Capacitive Load

Figure 5-36. Output Impedance vs Frequency



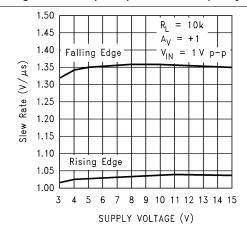
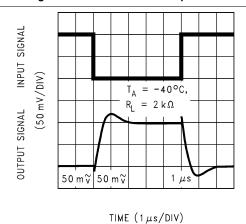
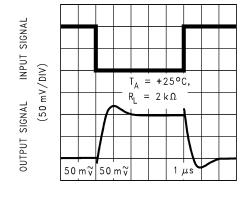


Figure 5-37. Slew Rate vs Temperature

Figure 5-38. Slew Rate vs Supply Voltage





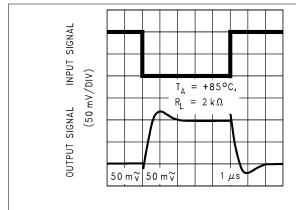
TIME $(1\mu s/DIV)$

Figure 5-39. Inverting Small-Signal Pulse Response

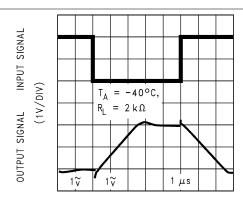
Figure 5-40. Inverting Small-Signal Pulse Response



at V+ = 15V, V $_-$ = 0V, and T $_A$ = 25°C (unless otherwise specified)



TIME $(1 \mu s/DIV)$

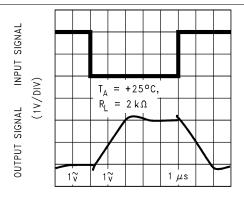


TIME $(1\mu s/DIV)$

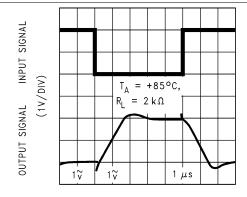
Figure 5-41. Inverting Small-Signal Pulse Response



Figure 5-42. Inverting Large-Signal Pulse Response



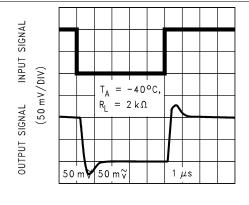
TIME $(1\mu s/DIV)$



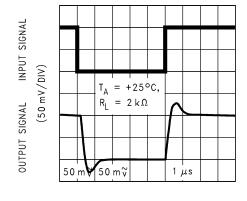
TIME $(1\mu s/DIV)$

Figure 5-43. Inverting Large-Signal Pulse Response

Figure 5-44. Inverting Large-Signal Pulse Response



TIME (1 μ s/DIV)

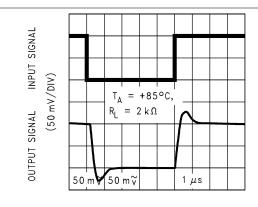


TIME $(1\mu s/DIV)$

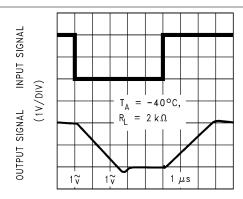
Figure 5-45. Noninverting Small-Signal Pulse Response

Figure 5-46. Noninverting Small-Signal Pulse Response

at V+ = 15V, V- = 0V, and T_A = 25°C (unless otherwise specified)

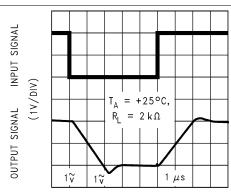


TIME $(1 \mu s/DIV)$



TIME $(1\mu s/DIV)$

Figure 5-47. Noninverting Small-Signal Pulse Response



TIME $(1 \mu s/DIV)$

INPUT SIGNAL (1V/DIV)OUTPUT SIGNAL = +85°C,

Figure 5-48. Noninverting Large-Signal Pulse Response

TIME $(1\mu s/DIV)$

 $2 k\Omega$

Figure 5-49. Noninverting Large-Signal Pulse Response

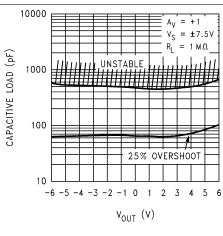


Figure 5-51. Stability vs Capacitive Load

Figure 5-50. Noninverting Large-Signal Pulse Response

1~

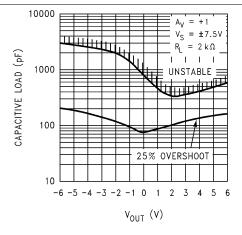
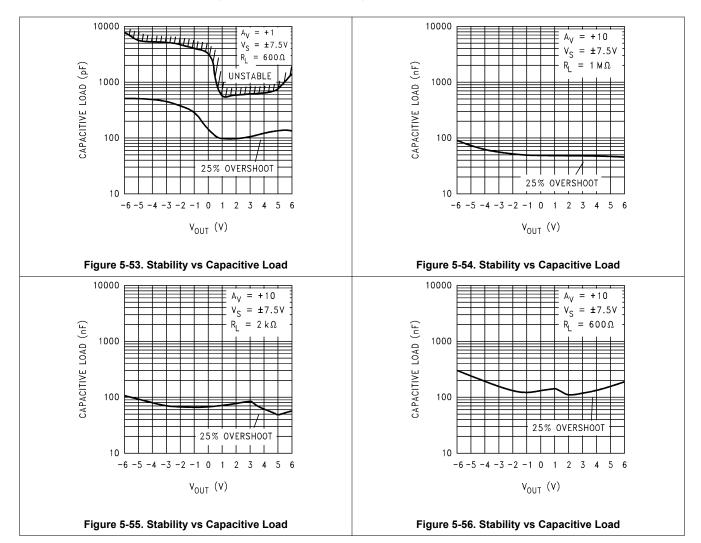


Figure 5-52. Stability vs Capacitive Load



at V+ = 15V, V- = 0V, and T_A = 25°C (unless otherwise specified)



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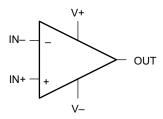
6 Detailed Description

6.1 Overview

The LMC7101 is a single-channel, low-power operational amplifier available in a space-saving SOT-23 package, offering rail-to-rail input and output operation across a wide range of power-supply configurations.

The LMC7101 is also available in an automotive-grade variant, see LMC7101Q-Q1.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Benefits of the LMC7101 Tiny Amplifier

6.3.1.1 Size

The small footprint of the SOT-23-5 packaged tiny amplifier, (0.12in × 0.118in, 3.05mm × 3mm) saves space on printed circuit boards, and enable the design of smaller electronic products. Many customers prefer smaller and lighter products because the designs can contribute to overall weight reduction in portable electronics.

6.3.1.2 Height

The 0.056 inches (1.43mm) height of the tiny LMC7101 amplifier makes the device an excellent choice for use in a wide range of circuit boards in which a thin profile is required.

6.3.1.3 Signal Integrity

Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the tiny amplifier can be placed closer to the signal source, thus reducing noise pickup and increasing signal integrity. The tiny amplifier can also be placed next to the signal destination, such as a buffer, for the reference of an analog-to-digital converter.

6.3.1.4 Simplified Board Layout

The tiny LMC7101 amplifier can simplify board layout in several ways. Avoid long PCB traces by correctly placing amplifiers instead of routing signals to a dual or quad device. By using multiple tiny amplifiers instead of duals or quads, complex signal routing and possibly crosstalk can be reduced.

6.3.1.5 Low THD

The high open-loop gain of the LMC7101 amplifier helps to achieve very low audio distortion—typically 0.01% at 10kHz with a 10k Ω load at 5V supplies. This makes the tiny amplifier an excellent choice for audio and low-frequency signal-processing applications.

6.3.1.6 Low Supply Current

The typical 0.5mA supply current of the LMC7101 can help improve thermal performance on high density circuit boards, and can allow the reduction of the overall board size in some applications.

6.3.1.7 Wide Voltage Range

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The LMC7101 is characterized at 15V, 5V and 3V. Performance data is provided at these popular voltages. This wide voltage range makes the LMC7101 a good choice for devices where the supply voltage can vary.



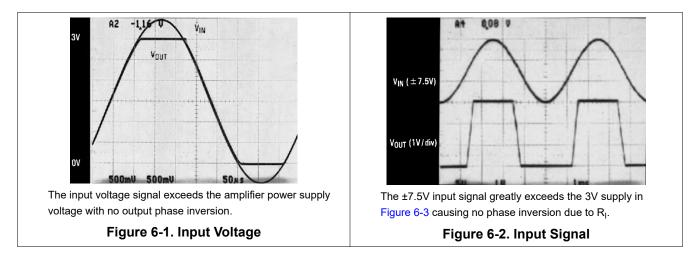
6.4 Device Functional Modes

6.4.1 Input Common Mode

6.4.1.1 Input Common-Mode Voltage Range

The LMC7101 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. Figure 6-1 shows an input voltage exceeding both supplies with no resulting phase inversion of the output.

The absolute maximum input voltage is 300mV beyond either rail at room temperature. Voltages greatly exceeding this maximum rating, as in Figure 6-2, can cause excessive current to flow in or out of the input pins, thus adversely affecting reliability.



Applications that exceed this rating must externally limit the maximum input current to ±5mA with an input resistor as shown in Figure 6-3.

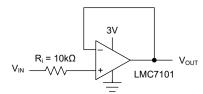


Figure 6-3. R_I Input Current Protection for Voltages Exceeding the Supply Voltage

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Rail-to-Rail Output

The approximate output resistance of the LMC7101 is 180Ω sourcing and 130Ω sinking at V_S = 3V and 110Ω sourcing and 80Ω sinking at V_S = 5V. Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

7.1.2 Capacitive Load Tolerance

The LMC7101 can typically directly drive a 100pF load with V_S = 15V at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of operational amplifiers. The combination of the output impedance and the capacitive load of the operational amplifier induces phase lag, which results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in Figure 7-1. This simple technique is useful for isolating the capacitive input of multiplexers and A/D converters.

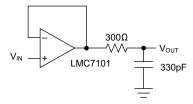


Figure 7-1. Resistive Isolation of a 330pF Capacitive Load

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7.1.3 Compensating for Input Capacitance When Using Large Value Feedback Resistors

When using very large value feedback resistors, (usually >500 k Ω) the large feed back resistance can react with the input capacitance due to transducers, photo diodes, and circuit board parasitics to reduce phase margins.

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in Figure 7-2), C_f is first estimated by Equation 1 and Equation 2, which typically provides significant overcompensation.

$$\frac{1}{2\pi R_1 C_{\text{IN}}} \ge \frac{1}{2\pi R_2 C_f} \tag{1}$$

$$2\pi R_1 C_{\text{IN}} \le 2\pi R_2 C_{\text{f}} \tag{2}$$

Printed circuit board stray capacitance can be larger or smaller than that of a breadboard, so the actual optimum value for C_F can be different. The values of C_F must be checked on the actual circuit.

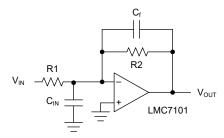


Figure 7-2. Canceling the Effect of Input Capacitance

7.2 Typical Application

Figure 7-3 shows a high input impedance noninverting circuit. This circuit gives a closed-loop gain equal to the ratio of the sum of R1 and R2 to R1 and a closed-loop 3dB bandwidth equal to the amplifier unity-gain frequency divided by the closed-loop gain. This design has the benefit of a very high input impedance, which is equal to the differential input impedance multiplied by loop gain (open loop gain / closed loop gain). In dc-coupled applications, input impedance is not as important as input current and the voltage drop across the source resistance. The amplifier output can go into saturation if the input is allowed to float, which can be important if the amplifier must be switched from source to source.

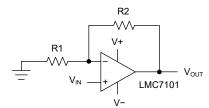


Figure 7-3. Example Application

7.2.1 Design Requirements

For this example application, the supply voltage is 5V, and 100 \times ±5% of noninverting gain is necessary. The signal input impedance is approximately 10k Ω .

7.2.2 Detailed Design Procedure

Use the equation for a noninverting amplifier configuration; G = 1 + R2 / R1, set R1 to $10k\Omega$, and R2 to $99 \times R1$, which is $990k\Omega$. Replacing the $990k\Omega$ resistor with a more readily available $1M\Omega$ resistor results in a gain of 101, which is within the desired gain tolerance. The gain-frequency characteristic of the amplifier and the feedback network must be such that oscillation does not occur. To meet this condition, the phase shift through amplifier and feedback network must never exceed 180° for any frequency where the gain of the amplifier and the feedback network is greater than unity. In practical applications, the phase shift must not approach 180° because this is the situation of conditional stability. The most critical case occurs when the attenuation of the feedback network is zero.

7.2.3 Application Curve

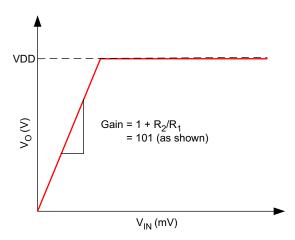


Figure 7-4. Output Response



7.3 Power Supply Recommendations

For proper operation, the power supplies must be decoupled. For supply decoupling, TI recommends placing 10nF to $1\mu F$ capacitors as close as possible to the operational-amplifier power supply pins. For single supply configurations, place a capacitor between the V+ and V- supply pins. For dual supply configurations, place one capacitor between V+ and ground, and place a second capacitor between V- and ground. Bypass capacitors must have a low ESR of less than 0.1Ω .

7.4 Layout

7.4.1 Layout Guidelines

Care must be taken to minimize the loop area formed by the bypass capacitor connection between supply pins and ground. A ground plane underneath the device is recommended; any bypass components to ground must have a nearby via to the ground plane. The optimum bypass capacitor placement is closest to the corresponding supply pin. Use of thicker traces from the bypass capacitors to the corresponding supply pins can lower the power-supply inductance and provide a more stable power supply.

The feedback components must be placed as close as possible to the device to minimize stray parasitics.

7.4.2 Layout Example

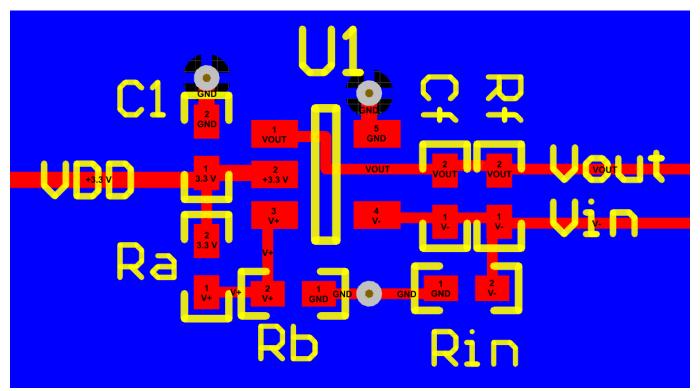


Figure 7-5. LMC7101 Example Layout

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8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, LMC66x CMOS Dual Operational Amplifiers data sheet
- Texas Instruments, RES11A Matched, Thin-Film Resistor Dividers With 1kΩ Inputs data sheet

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Trademarks

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8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

С	hanges from Revision SNOS719G (September 2015) to Revision * (January 2025)	Page
•	Moved LMC7101 commercial device from SNOS719G data sheet into new SBOSAL2 data sheet	1
•	Updated Features	1
•	Deleted machine model (MM) in ESD Ratings	3
•	Updated Thermal Information	
•	Updated parameter names and table format in all Electrical Characteristics	4
•	Added missing temperature range for input offset voltage drift in all Electrical Characteristics	4
•	Changed power-supply rejection ratio from 50dB to 45dB for LMC7101A	4
•	Changed power-supply rejection ratio from 50dB to 45dB for LMC7101A	4
•	Changed input common-mode voltage condition from CMRR ≥ 50dB to CMRR ≥ 47dB	4
•	Changed CMRR MIN from 50dB to 47dB for LMC7101B and from 55dB to 47dB for LMC7101A	4
•	Deleted notes 1 and 2 in all Electrical Characteristics	4
•	Updated note 3 to move information into slew rate test conditions	4
•	Changed input common-mode voltage condition from CMRR > 50dB to CMRR > 47dB	5
•	Changed CMRR MIN from 60dB to 47dB for LMC7101B and from 64dB to 47dB for LMC7101A	5
•	Added missing quiescent current per amplifier TYP value	



•	Changed CMRR TYP from 82dB to 75dB	6
•	Changed CMRR MIN from 60dB to 52dB for LMC7101B and from 65dB to 52dB for LMC7101A	6
•	Changed CMRR MIN for TJ = -40°C to +85°C from 55dB to 51dB for LMC7101B and from 60dB to 51dB	3 for
	LMC7101A	6
•	Changed CMRR TYP for TJ = -40C to +85C from 82dB to 74dB	6
•	Changed input offset voltage TYP from 0.11mV to 0.26mV	8
•	Changed CMRR MIN from 65dB to 62dB for LMC7101B and from 70dB to 62dB for LMC7101A	8
•	Changed CMRR MIN for $T_J = -40^{\circ}$ C to +85°C from 65dB to 60dB LMC7101A	<mark>8</mark>
•	Deleted note 3 and included information to open-loop voltage gain test conditions	<mark>8</mark>
•	Deleted Figures 6, 11, 14, 17, 20, 23, and 37	10
•	Added Figure 5-6	10
•	Added Figures 5-21 and 5-25	14

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com 7-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
LMC7101AIM5X/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	A00A
LMC7101AIM5X/NOPB.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A00A
LMC7101AIM5X/NOPB.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A00A
LMC7101BIM5X/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	A00B
LMC7101BIM5X/NOPB.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A00B
LMC7101BIM5X/NOPB.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A00B

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

www.ti.com 7-Nov-2025

PACKAGE MATERIALS INFORMATION

www.ti.com 5-Sep-2025

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC7101AIM5X/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101AIM5X/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101AIM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101BIM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101BIM5X/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101BIM5X/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC7101AIM5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMC7101AIM5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMC7101AIM5X/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMC7101BIM5X/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMC7101BIM5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMC7101BIM5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0



SMALL OUTLINE TRANSISTOR



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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