# LMC606x Precision CMOS, Micropower Operational Amplifiers

#### 1 Features

- Typical values unless otherwise noted
- Low offset voltage: 100µV
- Ultra-low supply current: 16µA/amplifier
- Supply range: 4.5V to 15V
- Ultra-low input bias current: 10fA
- Output swing within 10mV of supply rail,  $100k\Omega$
- Input common-mode includes V-
- High voltage gain: 140dB
- Improved latchup immunity

# 2 Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Portable analytic instruments
- Medical instrumentation
- Digital-to-analog converter (DAC)
- Charge amplifier for piezoelectric transducers

## 3 Description

The LMC6061, LMC6062, and LMC6064 (LMC606x) low-offset-voltage, precision, micropower operational amplifiers (op amps), capable of precision single-supply operation. Performance characteristics include ultra-low input bias current, high voltage gain, rail-to-rail output swing, and an input common-mode voltage range that includes ground. These features, plus the low power consumption of the op amps, make the LMC606x an excellent choice for batterypowered applications.

Other applications using the LMC606x include precision full-wave rectifiers, integrators, references, sample-and-hold circuits, and true instrumentation amplifiers.

This device is built with TI's advanced double-poly silicon-gate CMOS process.

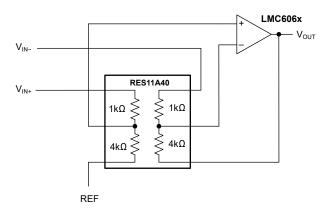
For designs that require higher speed, see the LMC608x precision operational amplifiers.

#### **PATENT PENDING**

#### **Device Information**

| PART NUMBER | CHANNEL COUNT | PACKAGE <sup>(1)</sup> |
|-------------|---------------|------------------------|
| LMC6061     | Single        | D (SOIC, 8)            |
| LMC6062     | Dual          | D (SOIC, 8)            |
|             | Duai          | P (PDIP, 8)            |
| LMC6064     | Quad          | D (SOIC, 8)            |

For more information, see Section 9.



**Difference Amplifier Application With RES11A** 



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# 4 Pin Configuration and Functions

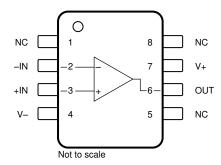


Figure 4-1. LMC6061: D Package, 8-Pin SOIC (Top View)

## Table 4-1. Pin Functions: LMC6061

| PIN  |         | TYPE   | DESCRIPTION                          |  |
|------|---------|--------|--------------------------------------|--|
| NAME | NO.     | IIPE   | DESCRIPTION                          |  |
| -IN  | 2       | Input  | Inverting input                      |  |
| +IN  | 3       | Input  | Noninverting input                   |  |
| NC   | 1, 8, 5 | _      | No connection (can be left floating) |  |
| OUT  | 6       | Output | Output                               |  |
| V-   | 4       | Power  | Negative (lowest) power supply       |  |
| V+   | 7       | Power  | Positive (highest) power supply      |  |

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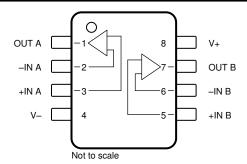


Figure 4-2. LMC6062: D Package, 8-Pin SOIC and P Package, 8-Pin PDIP (Top View)

Table 4-2. Pin Functions: LMC6062

|       | PIN |        |                              |  |
|-------|-----|--------|------------------------------|--|
|       |     | TYPE   | DESCRIPTION                  |  |
| NAME  | NO. |        |                              |  |
| −IN A | 2   | Input  | Inverting input channel A    |  |
| –IN B | 6   | Input  | Inverting input channel B    |  |
| +IN A | 3   | Input  | Noninverting input channel A |  |
| +IN B | 5   | Input  | Noninverting input channel B |  |
| OUT A | 1   | Output | Output channel A             |  |
| OUT B | 7   | Output | Output channel B             |  |
| V-    | 4   | Power  | Negative supply              |  |
| V+    | 8   | Power  | Positive supply              |  |



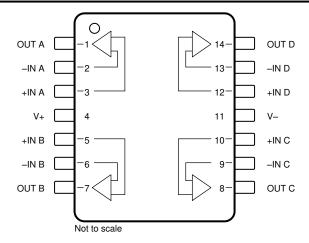


Figure 4-3. LMC6064: D Package, 14-Pin SOIC (Top View)

Table 4-3. Pin Functions: LMC6064

|       |     | 144.15 | C. I II I dilotionis. Linesco- |  |
|-------|-----|--------|--------------------------------|--|
|       | PIN | TYPE   | DESCRIPTION                    |  |
| NAME  | NO. | 1115   | DESCRIPTION                    |  |
| –IN A | 2   | Input  | Inverting input channel A      |  |
| –IN B | 6   | Input  | Inverting input channel B      |  |
| –IN C | 9   | Input  | Inverting input channel C      |  |
| –IN D | 13  | Input  | Inverting input channel D      |  |
| +IN A | 3   | Input  | Noninverting input channel A   |  |
| +IN B | 5   | Input  | Noninverting input channel B   |  |
| +IN C | 10  | Input  | Noninverting input channel C   |  |
| +IN D | 12  | Input  | Noninverting input channel D   |  |
| OUT A | 1   | Output | Output channel A               |  |
| OUT B | 7   | Output | Output channel B               |  |
| OUT C | 8   | Output | Output channel C               |  |
| OUT D | 14  | Output | Output channel D               |  |
| V–    | 11  | Power  | Negative supply                |  |
| V+    | 4   | Power  | Positive supply                |  |

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# **5 Specifications**

# 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

|                  |                                     |                     | MIN        | MAX                | UNIT |
|------------------|-------------------------------------|---------------------|------------|--------------------|------|
|                  | Differential input voltage          |                     |            | ±Supply voltage    | V    |
|                  | /oltage at input/output pin         |                     | (V-) - 0.3 | (V+) + 0.3         | V    |
| Vs               | Supply voltage, $V_S = (V+) - (V-)$ |                     |            | 16                 | V    |
|                  | Output short circuit current        | To V+               |            | See <sup>(3)</sup> |      |
| I <sub>SC</sub>  | Output short circuit current        | To V-               |            | See <sup>(4)</sup> |      |
|                  |                                     | At input pin        |            | ±10                |      |
|                  | Current                             | At output pin       |            | ±30                | mA   |
|                  |                                     | At power supply pin |            | 40                 |      |
|                  | Power dissipation                   |                     |            | See <sup>(5)</sup> |      |
|                  | Lead temperature (soldering, 10s)   |                     |            | 260                | °C   |
| TJ               | Junction temperature                |                     |            | 150                | °C   |
| T <sub>stg</sub> | Storage temperature                 |                     | -65        | 150                | °C   |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (3) Do not connect output to V+, when V+ is greater than 13V or reliability can be adversely affected.
- (4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30mA over long term can adversely affect reliability.
- (5) The maximum power dissipation is a function of  $T_{J(Max)}$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(Max)} T_A) / \theta_{JA}$

#### 5.2 ESD Ratings

|                    |                         |   | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup> | ±2000 | V    |

<sup>(1)</sup> JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

#### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                               |                                     |             | MIN   | NOM MAX            | UNIT |
|-------------------------------|-------------------------------------|-------------|-------|--------------------|------|
| V Supply voltage V = (VI) (V) | Single supply                       | 4.5         | 36    |                    |      |
| Vs                            | Supply voltage, $V_S = (V+) - (V-)$ | Dual supply | ±2.25 | ±18                | V    |
|                               | Specified temperature               |             | -40   | 125                | °C   |
|                               | Power dissipation                   |             |       | See <sup>(1)</sup> |      |

(1) To operate the device at elevated temperatures, derate the device based on thermal resistance  $\theta_{JA}$  with  $P_D = (T_J - T_A) / \theta_{JA}$ .



#### 5.4 Thermal Information: LMC6061

|                       |  | LMC6061  |      |
|-----------------------|--|----------|------|
|                       | THERMAL METRIC(1)                            | D (SOIC) | UNIT |
|                       |  | 8 PINS   |      |
| R <sub>θJA</sub>      | Junction-to-ambient thermal resistance       | 193.0    | °C/W |
| R <sub>θJC(top)</sub> | Junction-to-case(top) thermal resistance     | 57.9     | °C/W |
| R <sub>θJB</sub>      | Junction-to-board thermal resistance         | 62.3     | °C/W |
| $\Psi_{JT}$           | Junction-to-top characterization parameter   | 10.0     | °C/W |
| $\Psi_{JB}$           | Junction-to-board characterization parameter | 61.5     | °C/W |
| R <sub>θJC(bot)</sub> | Junction-to-case(bottom) thermal resistance  | N/A      | °C/W |

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

#### 5.5 Thermal Information: LMC6062

|                       |  | LMC      | 6062     |      |  |
|-----------------------|--|----------|----------|------|--|
|                       | THERMAL METRIC <sup>(1)</sup>                | D (SOIC) | P (PDIP) | UNIT |  |
|                       |  | 8 PINS   | 8 PINS   |      |  |
| R <sub>0JA</sub>      | Junction-to-ambient thermal resistance       | 193.0    | 115.0    | °C/W |  |
| R <sub>0JC(top)</sub> | Junction-to-case(top) thermal resistance     | 52.0     | 59.2     | °C/W |  |
| $R_{\theta JB}$       | Junction-to-board thermal resistance         | 56.9     | 43.2     | °C/W |  |
| ΨЈТ                   | Junction-to-top characterization parameter   | 6.8      | 25.1     | °C/W |  |
| ΨЈВ                   | Junction-to-board characterization parameter | 56.1     | 42.3     | °C/W |  |
| R <sub>0JC(bot)</sub> | Junction-to-case(bottom) thermal resistance  | N/A      | N/A      | °C/W |  |

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 5.6 Thermal Information: LMC6064

|                       |  | LMC6064  |      |
|-----------------------|--|----------|------|
|                       | THERMAL METRIC <sup>(1)</sup>                | D (SOIC) | UNIT |
|                       |  | 14 PINS  |      |
| $R_{\theta JA}$       | Junction-to-ambient thermal resistance       | 126.0    | °C/W |
| R <sub>0JC(top)</sub> | Junction-to-case(top) thermal resistance     | 34.6     | °C/W |
| $R_{\theta JB}$       | Junction-to-board thermal resistance         | 34.3     | °C/W |
| ΨЈТ                   | Junction-to-top characterization parameter   | 4.7      | °C/W |
| ΨЈВ                   | Junction-to-board characterization parameter | 33.7     | °C/W |
| R <sub>0JC(bot)</sub> | Junction-to-case(bottom) thermal resistance  | N/A      | °C/W |

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.



# **5.7 Electrical Characteristics**

at  $T_J = T_A = +25^{\circ}C$ ,  $V_T = 5V$ ,  $V_T = 0V$ ,  $V_{CM} = 1.5V$ ,  $V_{OUT} = 2.5V$ , and  $R_L > 1M\Omega$  connected to  $V_T / 2$  (unless otherwise noted)

|                      | PARAMETER                         | TEST COM                                       | NDITIONS  | MIN   | TYP        | MAX        | UNIT               |
|----------------------|-----------------------------------|--|---|-------|------------|------------|--------------------|
| OFFSET               | VOLTAGE                           |  |   |       |            |            |                    |
|                      |                                   | I MOGOGWAI                                     |   |       | ±100       | ±350       |                    |
| \/                   | Input offeet veltage              | LMC606xAI                                      | $T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ |       |            | ±900       | μV                 |
| Vos                  | Input offset voltage              | LMC606xI                                       |   |       | ±100       | ±800       |                    |
|                      |                                   | LIVICOUXI                                      | $T_A = -40$ °C to +85°C                             |       |            | ±1300      |                    |
| dV <sub>OS</sub> /dT | Input offset voltage drift        | $T_A = -40$ °C to +85°C                        |   |       | 1          |            | μV/°C              |
|                      |                                   |  | LMC606xAI   | 75    | 85         |            |                    |
|                      |                                   | Positive                                       | LMC606xAI<br>T <sub>A</sub> = -40°C to +85°C        | 72    |            |            |                    |
|                      |                                   | $5V \le V + \le 15V$ , $V_{OUT} = 2.5V$ ,      | LMC606xI  | 66    | 85         |            |                    |
| DODD                 | PSRR Power supply rejection ratio |  | LMC606xI<br>T <sub>A</sub> = -40°C to +85°C         | 63    |            |            | ٩D                 |
| PSRK                 | Power supply rejection ratio      |  | LMC606xAI   | 84    | 100        |            | dB                 |
|                      |                                   | Negative                                       | LMC606xAI<br>T <sub>A</sub> = -40°C to +85°C        | 81    |            |            |                    |
|                      |                                   | -10V ≤ V+ ≤ 0V                                 | LMC606xI  | 74    | 100        |            |                    |
|                      |                                   |  | LMC606xI<br>T <sub>A</sub> = -40°C to +85°C         | 71    |            |            |                    |
| INPUT B              | IAS CURRENT                       |  |   |       |            |            |                    |
|                      | land bing somet                   |  |   |       | ±10        |            | fA                 |
| I <sub>B</sub>       | Input bias current                | $T_A = -40$ °C to +85°C                        |   |       |            | ±4         | pА                 |
|                      | l                                 |  |   |       | ±5         |            | fA                 |
| los                  | Input offset current              | $T_A = -40$ °C to +85°C                        |   |       |            | ±4         | pА                 |
| NOISE                |                                   |  |   |       |            |            |                    |
| e <sub>n</sub>       | Input voltage noise density       | f = 1kHz                                       |   |       | 83         |            | nV/√ <del>Hz</del> |
| i <sub>n</sub>       | Input current noise density       | f = 1kHz                                       |   |       | 12.5       |            | fA/√ <del>Hz</del> |
| THD                  | Total Harmonic Distortion         | $f = 1kHz$ , $G = -5V/V$ , $R_L = 100kΩ$ , $V$ | $V_{OUT} = 2V_{pp}, V_S = \pm 5V$                   |       | 0.01       |            | %                  |
| INPUT V              | OLTAGE                            | 1  |   |       |            | '          |                    |
|                      |                                   | To positive rail                               |   |       | (V+) - 1.9 | (V+) - 2.3 |                    |
|                      |                                   | V+ = 15V and V+ = 5V, CMRR > 60dB              | $T_A = -40$ °C to +85°C                             |       |            | (V+) - 2.5 |                    |
| $V_{CM}$             | Common-mode voltage               | To negative rail                               |   | - 0.1 | - 0.4      |            | V                  |
|                      |                                   | V+ = 15V and V+ = 5V, CMRR > 60dB              | T <sub>A</sub> = -40°C to +85°C                     | 0     |            |            | Ì                  |
|                      |                                   |  | LMC606xAI   | 75    | 85         |            | - dB               |
| OMBB                 | Common-mode rejection             | ejection $V+ = 15V$ , $0V \le V_{CM} \le 12V$  | LMC606xAI, T <sub>A</sub> = -40°C to +85°C          | 72    |            |            |                    |
| CMRR                 | ratio                             |  | LMC606xI  | 66    | 85         |            |                    |
|                      |                                   |  | LMC606xI, T <sub>A</sub> = -40°C to<br>+85°C        | 63    |            |            |                    |
| INPUT IN             | IPEDANCE                          | •  | •   |       |            |            |                    |
| R <sub>IN</sub>      | Input resistance                  |  |   |       | >10        |            | ΤΩ                 |



# **5.7 Electrical Characteristics (continued)**

at  $T_J = T_A = +25^{\circ}\text{C}$ ,  $V_T = 5V$ ,  $V_T = 0V$ ,  $V_{CM} = 1.5V$ ,  $V_{OUT} = 2.5V$ , and  $R_L > 1M\Omega$  connected to  $V_T / 2$  (unless otherwise noted)

|                 | PARAMETER              | TEST COM   | TEST CONDITIONS                                       |     | TYP  | MAX  | UNIT   |
|-----------------|------------------------|--|---|-----|------|------|--------|
| OPEN-L          | OOP GAIN               |  |   |     |      | 1    |        |
|                 |                        |  | LMC606xAI   | 300 | 4000 |      |        |
|                 |                        | Sourcing, V+ = 15V, V <sub>CM</sub> = 7.5V,        | LMC606xAI, T <sub>A</sub> = -40°C to<br>+85°C         | 200 |      |      |        |
|                 |                        | $7.5V \le V_0 \le 11.5V, R_L = 100k\Omega$         | LMC606xI  | 300 | 4000 |      |        |
|                 |                        |  | LMC606xI, T <sub>A</sub> = -40°C to<br>+85°C          | 200 |      | V/m\ |        |
|                 |                        |  | LMC606xAI   | 180 | 3000 |      |        |
|                 |                        | Sinking, V+ = 15V, V <sub>CM</sub> = 7.5V,         | LMC606xAI, T <sub>A</sub> = -40°C to<br>+85°C         | 100 |      |      |        |
|                 |                        | $2.5V \le V_0 \le 7.5V$ , $R_L = 100k\Omega$       | LMC606xI  | 90  | 3000 |      |        |
|                 | Onen leen valtege gein |  | LMC606xI, T <sub>A</sub> = -40°C to<br>+85°C          | 60  |      |      | \//m\/ |
| A <sub>OL</sub> | Open-loop voltage gain |  | LMC606xAI   | 300 | 3000 | V/r  | V/mv   |
|                 |                        | Sourcing, V+ = 15V, V <sub>CM</sub> = 7.5V,        | LMC606xAI, T <sub>A</sub> = -40°C to<br>+85°C         | 150 |      |      |        |
|                 |                        | $7.5V \le V_0 \le 11.5V, R_L = 25k\Omega$          | LMC606xI  | 200 | 3000 |      |        |
|                 |                        |  | LMC606xI, T <sub>A</sub> = -40°C to<br>+85°C          | 80  |      |      |        |
|                 |                        |  | LMC606xAI   | 100 | 2000 |      |        |
|                 |                        | Sinking, $V_S = 15V$ , $V_{CM} = 7.5V$ ,           | LMC606xAI, T <sub>A</sub> = -40°C to<br>+85°C         | 50  |      |      |        |
|                 |                        | $2.5V \le V_0 \le 7.5V$ , $R_L = 25k\Omega$        | LMC606xI  | 70  | 2000 |      |        |
|                 |                        |  | LMC606xI, T <sub>A</sub> = -40°C to<br>+85°C          | 35  |      |      |        |
| FREQU           | ENCY RESPONSE          |  |   |     |      |      |        |
| GBW             | Gain bandwidth product |  |   |     | 100  |      | kHz    |
|                 |                        |  | LMC606xAI   | 20  | 35   |      |        |
| SR              | Slew rate              | V+ = 15V, 10V step, q = 1                          | LMC606xAI, -40°C to +85°C                             | 10  |      |      | V/ms   |
| υιν             | Olew Fale              | v · - 15 v, 10 v step, y - 1                       | LMC606xI  | 15  | 35   |      |        |
|                 |                        |  | LMC606xI, -40°C to +85°C                              | 7   |      |      |        |
|                 | Crosstalk              | Dual and quad channel, V+ = 15V, 12V <sub>pp</sub> | R <sub>L</sub> = 100kΩ, f = 100Hz, V <sub>OUT</sub> = |     | 155  |      | dB     |



# **5.7 Electrical Characteristics (continued)**

at  $T_J = T_A = +25$ °C,  $V_T = 5V$ ,  $V_T = 0V$ ,  $V_{CM} = 1.5V$ ,  $V_{OUT} = 2.5V$ , and  $R_L > 1M\Omega$  connected to  $V_T = 1.5V$  (unless otherwise noted)

|       | PARAMETER             | TEST  | CONDITIONS                                   | MIN    | TYP    | MAX   | UNIT                                  |  |
|-------|-----------------------|---|--|--------|--------|---|---------------------------------------|--|
| UTPUT |                       |   |  |        |        |   |                                       |  |
|       |                       |   | LMC606xAI                                    | 4.990  | 4.995  |   |                                       |  |
|       |                       | Positive rail                               | LMC606xAI, $T_A = -40$ °C to +85°C           | 4.980  |        |   |                                       |  |
|       |                       | V+ = 5V, $R_L = 100k\Omega$                 | LMC606xI                                     | 4.950  | 4.995  |   |                                       |  |
|       |                       |   | LMC606xI, T <sub>A</sub> = -40°C to +85°C    | 4.925  |        |   |                                       |  |
|       |                       | Negative rail                               | LMC606xAI                                    |        | 0.005  | 0.010   |                                       |  |
|       |                       |   | LMC606xAI, T <sub>A</sub> = -40°C to +85°C   |        |        | 0.020   |                                       |  |
|       |                       | $V+ = 5V$ , $R_L = 100k\Omega$              | LMC606xI                                     |        | 0.005  | 0.050   |                                       |  |
|       |                       |   | LMC606xI, T <sub>A</sub> = -40°C to +85°C    |        |        | 0.075   |                                       |  |
|       |                       | LMC606xAI                                   | 4.975  | 4.990  |        |   |                                       |  |
|       |                       | Positive rail V+ = 5V, $R_L$ = 25k $\Omega$ | LMC606xAI, $T_A = -40$ °C to +85°C           | 4.965  |        |   |                                       |  |
|       |                       |   | LMC606xI                                     | 4.950  | 4.990  |   |                                       |  |
|       |                       |   | LMC606xI, T <sub>A</sub> = -40°C to +85°C    | 4.850  |        |   |                                       |  |
|       |                       |   | LMC606xAI                                    |        | 0.010  | 0.020   |                                       |  |
|       |                       | Negative rail                               | LMC606xAI, $T_A = -40$ °C to +85°C           |        |        | 0.010<br>0.020<br>0.050<br>0.075  |                                       |  |
|       |                       | $V+ = 5V$ , $R_L = 25k\Omega$               | LMC606xI                                     |        | 0.010  | 0.050   |                                       |  |
| )     | Voltage output swing  |   | LMC606xI, $T_A = -40$ °C to +85°C            |        |        | 0.150   | ٧/                                    |  |
| )     | voltage output swilig |   |  |        |        |   | v                                     |  |
|       |                       | Positive rail                               |  | 14.965 |        |   |                                       |  |
|       |                       | $V+ = 15V, R_L = 100k\Omega$                | LMC606xI                                     | 14.950 | 14.990 |   |                                       |  |
|       |                       |   | LMC606xI, $T_A = -40$ °C to +85°C            | 14.925 |        |   | 20   20   20   20   20   20   20   20 |  |
|       |                       |   | LMC606xAI                                    |        | 0.010  | 0.020<br>0.050<br>0.075<br>0.020<br>0.035<br>0.050<br>0.150<br>0.075                            |                                       |  |
|       |                       | Negative rail                               | LMC606xAI, $T_A = -40$ °C to +85°C           |        |        | 0.035   |                                       |  |
|       |                       | $V + = 15V, R_L = 100k\Omega$               | LMC606xI                                     |        | 0.010  | 0.050   |                                       |  |
|       |                       |   | LMC606xI, $T_A = -40$ °C to +85°C            |        |        | 0.075   |                                       |  |
|       |                       |   | LMC606xAI                                    | 14.90  | 14.965 |   |                                       |  |
|       |                       | Positive rail                               | LMC606xAI, $T_A = -40$ °C to +85°C           | 14.850 |        | 0.020<br>0.050<br>0.075<br>0.020<br>0.035<br>0.050<br>0.150<br>0.050<br>0.075<br>0.050<br>0.150 |                                       |  |
|       |                       | $V+ = 15V, R_L = 25k\Omega$                 | LMC606xI                                     | 14.850 | 14.965 |   |                                       |  |
|       |                       |   | LMC606xI, T <sub>A</sub> = -40°C to +85°C    | 14.800 |        |   |                                       |  |
|       |                       |   | LMC606xAI                                    |        | 0.025  | 0.050   |                                       |  |
|       |                       | Negative rail                               | LMC606xAI, $T_A = -40$ °C to +85°C           |        |        | 0.150   | 1                                     |  |
|       |                       | $V + = 15V, R_L = 25k\Omega$                | LMC606xI                                     |        | 0.025  | 0.100   |                                       |  |
|       |                       |   | LMC606xI, T <sub>A</sub> = -40°C to<br>+85°C |        |        | 0.200   |                                       |  |



# **5.7 Electrical Characteristics (continued)**

at  $T_J = T_A = +25^{\circ}\text{C}$ ,  $V_T = 5V$ ,  $V_T = 0V$ ,  $V_{CM} = 1.5V$ ,  $V_{OUT} = 2.5V$ , and  $R_L > 1M\Omega$  connected to  $V_T + 2$  (unless otherwise noted)

|                 | PARAMETER             | TEST CO                           | ONDITIONS   | MIN | TYP  | MAX  | UNIT   |
|-----------------|-----------------------|-----------------------------------|---|-----|--|--|--|
|                 |                       |                                   | LMC606xAI   | 16  | 22   |  |  |
|                 |                       | Sourcing                          | LMC606xAI, T <sub>A</sub> = -40°C to +85°C          | 10  |  |  |  |
|                 |                       | V <sub>OUT</sub> = 0V             | LMC606xI  | 13  | 22   |  |  |
|                 |                       |                                   | LMC606xI, T <sub>A</sub> = -40°C to +85°C           | 8   |  |  |  |
|                 |                       |                                   | LMC606xAI   | 16  | 21   |  |  |
|                 |                       | Sinking                           | LMC606xAI, T <sub>A</sub> = -40°C to +85°C          | 8   |  | 21   |  |
|                 |                       | V <sub>OUT</sub> = 5V             | LMC606xI  | 16  | 21   |  |  |
|                 | Short circuit current |                                   | LMC606xI, T <sub>A</sub> = -40°C to +85°C           | 8   |  |  | mΛ   |
| I <sub>SC</sub> | Short-circuit current |                                   | LMC606xAI   | 15  | 5 21<br>3 5 25<br>0 5 25<br>0 26<br>3 0 26<br>3 20 24<br>32 20 32          |  | IIIA   |
| İ               |                       | Sourcing                          | LMC606xAI, T <sub>A</sub> = -40°C to<br>+85°C       | 10  |  | 21<br>25<br>25<br>26<br>26<br>20 24<br>32  |  |
|                 |                       | $V + = 15V, V_{OUT} = 0V$         | LMC606xI  | 15  | 25   |  |  |
|                 |                       |                                   | LMC606xI, T <sub>A</sub> = -40°C to +85°C           | 10  |  |  |  |
| l               |                       |                                   | LMC606xAI   | 20  | 26   | 32<br>32<br>40<br>19   |  |
|                 |                       | Sinking                           | LMC606xAI, T <sub>A</sub> = -40°C to<br>+85°C       | 8   |  |  |  |
|                 |                       | $V + = 15V, V_{OUT} = 13V^{(1)}$  | LMC606xI  | 20  | 26   |  |  |
|                 |                       |                                   | LMC606xI, T <sub>A</sub> = -40°C to +85°C           | 8   |  |  |  |
| POWE            | R SUPPLY              |                                   |   |     |  |  |  |
|                 |                       | LMC6061AI,                        |   |     | 20   | 24   |  |
|                 |                       | V <sub>OUT</sub> = 1.5V           | $T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ |     |  | 32   |  |
|                 |                       | LMC6061I,                         |   |     | 20   | 32   |  |
|                 |                       | V <sub>OUT</sub> = 1.5V           | $T_A = -40^{\circ}C \text{ to } +85^{\circ}C$       |     | 26  26  20  24  32  20  32  40  16  19  23  16  28  24  30  38  24  40  48 | 40   |  |
|                 |                       | LMC6062AI and LMC6064AI,          |   |     | 16   | 19   |  |
|                 |                       | V <sub>OUT</sub> = 1.5V           | $T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ |     |  | 23   |  |
|                 |                       | LMC6062I and LMC6064I,            |   |     | 16   | 24<br>32<br>32<br>40<br>19<br>23<br>23<br>28<br>30<br>38<br>40<br>48<br>23.5<br>27.5   |  |
| IQ              | Quiescent current per | V <sub>OUT</sub> = 1.5V           | $T_A = -40^{\circ}C \text{ to } +85^{\circ}C$       |     |  |  | пΔ   |
| ·Q              | amplifier             | LMC6061AI,                        |   |     | 24   | 30   | 32<br>32<br>40<br>19<br>23<br>23<br>28<br>30<br>38<br>40 |
|                 |                       | V <sub>OUT</sub> = 7.5V, V+ = 15V | $T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ |     |  | 32<br>32<br>40<br>19<br>23<br>23<br>28<br>30<br>38<br>40<br>48<br>23.5<br>27.5<br>28.5 |  |
|                 |                       | LMC6061I,                         |   |     | 24   |  |  |
|                 |                       | V <sub>OUT</sub> = 7.5V, V+ = 15V | $T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ |     |  | 48   |  |
|                 |                       | LMC6062AI and LMC6064AI,          |   |     | 20   | 23.5   |  |
|                 |                       | V <sub>OUT</sub> = 7.5V, V+ = 15V | $T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ |     |  | 27.5   |  |
|                 |                       | LMC6062I and LMC6064I,            |   |     | 20   | 28.5   |  |
|                 |                       | V <sub>OUT</sub> = 7.5V, V+ = 15V | $T_A = -40^{\circ}C \text{ to } +85^{\circ}C$       |     |  | 33   |  |

<sup>(1)</sup> Do not connect output to V+, when V+ is greater than 13V or reliability can be adversely affected.

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# 5.8 Typical Characteristics

at  $V_S = \pm 7.5V$  and  $T_A = 25$ °C (unless otherwise specified)

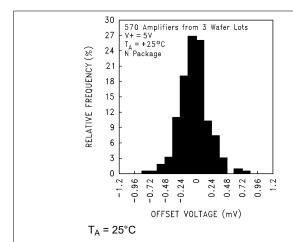


Figure 5-1. Distribution of Input Offset Voltage

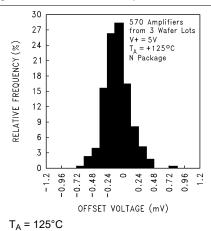


Figure 5-3. Distribution of Input Offset Voltage

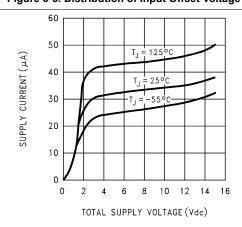
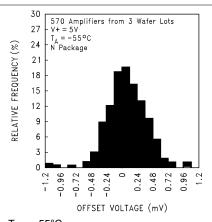


Figure 5-5. Supply Current vs Supply Voltage



 $T_A = -55$ °C

Figure 5-2. Distribution of Input Offset Voltage

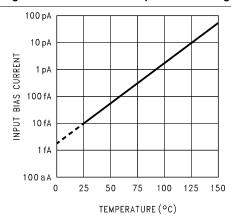


Figure 5-4. Input Bias Current vs Temperature

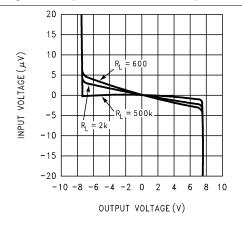


Figure 5-6. Input Voltage vs Output Voltage



# **5.8 Typical Characteristics (continued)**

at  $V_S = \pm 7.5V$  and  $T_A = 25^{\circ}C$  (unless otherwise specified)

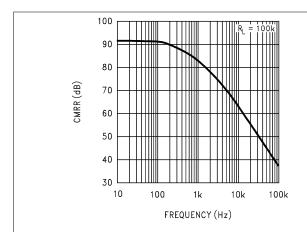


Figure 5-7. Common Mode Rejection Ratio vs Frequency

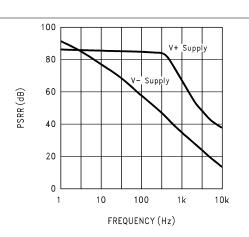


Figure 5-8. Power Supply Rejection Ratio vs Frequency

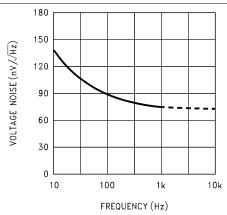


Figure 5-9. Input Voltage Noise vs Frequency

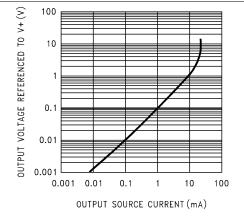


Figure 5-10. Output Characteristics Sourcing Current

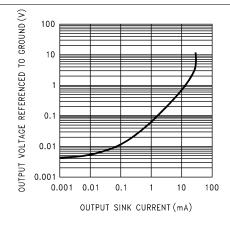
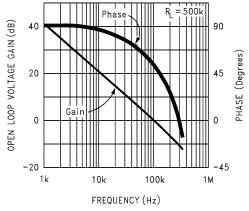


Figure 5-11. Output Characteristics Sinking Current



 $T_A = -55^{\circ}C \text{ to } +125^{\circ}C$ 

Figure 5-12. Gain and Phase Response vs Temperature

# **5.8 Typical Characteristics (continued)**

at  $V_S = \pm 7.5V$  and  $T_A = 25^{\circ}C$  (unless otherwise specified)

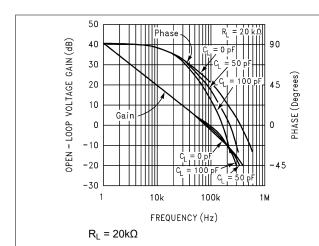


Figure 5-13. Gain and Phase Response vs Capacitive Load

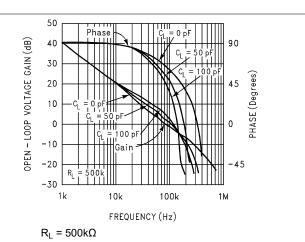


Figure 5-14. Gain and Phase Response vs Capacitive Load

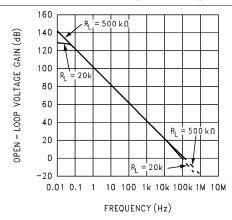
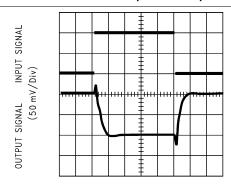


Figure 5-15. Open-Loop Frequency Response



TIME (10  $\mu$ s/Div)

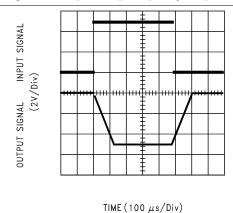


Figure 5-17. Inverting Large-Signal Pulse Response

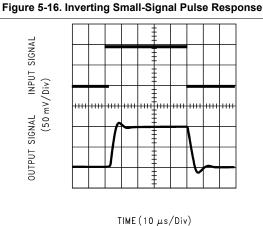
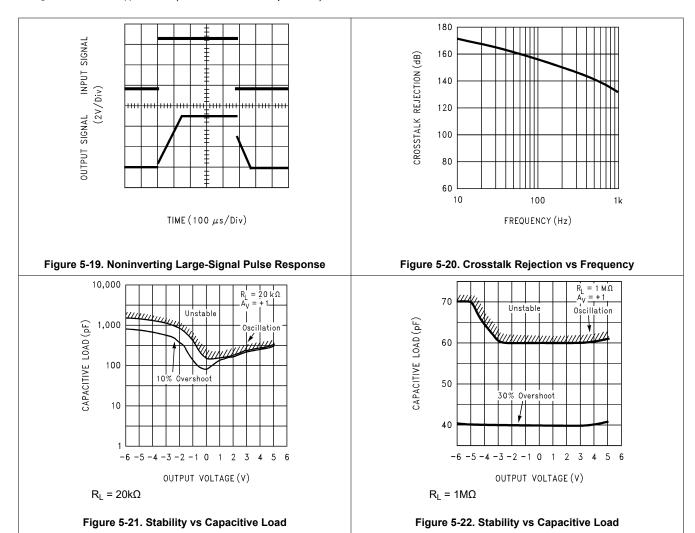


Figure 5-18. Noninverting Small-Signal Pulse Response



# **5.8 Typical Characteristics (continued)**

at  $V_S = \pm 7.5V$  and  $T_A = 25^{\circ}C$  (unless otherwise specified)





# **6 Application and Implementation**

#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

#### **6.1 Applications Information**

# 6.1.1 Amplifier Topology

The LMC606x incorporate a novel op amp design topology that enables rail-to-rail output swing even when driving a large load. Special compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op amps. These features make the LMC606x both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

#### 6.1.2 Compensating For Input Capacitance

Large values of feedback resistance are quite common for amplifiers with ultra-low input current, like the LMC606x. Although the LMC606x is highly stable over a wide range of operating conditions, take certain precautions to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC606x is suggested. Guarding input lines can not only reduce leakage, but also lower stray input capacitance. See also Section 6.3.1.1.

The effect of input capacitance can be compensated for by adding a capacitor. Place a capacitor,  $C_F$ , around the feedback resistor (as in Figure 6-1) such that:

$$\frac{1}{2\pi R1C_{\text{IN}}} \ge \frac{1}{2\pi R2C_{\text{F}}} \tag{1}$$

where

$$R1C_{IN} \le R2C_{F}$$

$$C_{F}$$

$$C_{F}$$

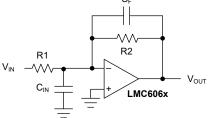


Figure 6-1. Canceling the Effect of Input Capacitance

The exact value of  $C_{IN}$  is often difficult to know, but  $C_F$  can be experimentally adjusted so that the desired pulse response is achieved. For a more detailed discussion on compensating for input capacitance, see the LMC660 and the LMC662.

#### 6.1.3 Capacitive Load Tolerance

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominate pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see *Section 5.8*).

Direct capacitive loading reduces the phase margin of many op amps. A pole in the feedback loop is created by the combination of the output impedance of the op amp and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. Figure 6-2 shows that with a few external components, op amps can easily indirectly drive capacitive loads.

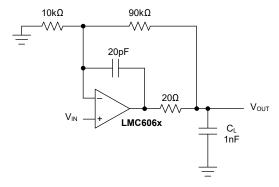


Figure 6-2. LMC606x Noninverting Gain of 10 Amplifier Compensated to Handle Capacitive Loads

In the circuit of Figure 6-2, R1 and C1 serve to counteract the loss of phase margin by feeding the high-frequency component of the output signal back to the inverting input of the amplifier, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pullup resistor to V+ (Figure 6-3). Typically, a pullup resistor conducting 10µA or more can significantly improve capacitive load responses. The value of the pullup resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. The open-loop gain of the amplifier can also be affected by the pullup resistor (see *Section 5.7*).

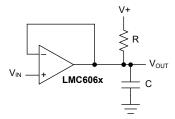


Figure 6-3. Compensating for Large Capacitive Loads With a Pullup Resistor

#### 6.1.4 Latchup

CMOS devices tend to be susceptible to latchup due to internal parasitic silicon controlled rectifier (SCR) effects. The input and output (I/O) pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC606x are designed to withstand 100mA surge current on the I/O pins. Use a resistive method to isolate any capacitance from supplying excess current to the I/O pins. In addition, like a SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins also inhibits latchup susceptibility.

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### 6.2 Typical Applications

#### 6.2.1 Instrumentation Amplifier

The extremely high input impedance, and low power consumption, of the LMC606x make them an excellent choice for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are portable pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon-based pressure transducers.

Figure 6-4 shows an instrumentation amplifier that features high differential and common mode input resistance (>  $10^{14}\Omega$ ), 0.01% gain accuracy at A<sub>V</sub> = 100, excellent CMRR with 1k $\Omega$  imbalance in bridge source resistance. Input current is less than 100fA and offset drift is less than 2.5 $\mu$ V/°C. R2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, use low-drift resistors.

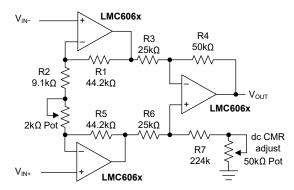


Figure 6-4. Instrumentation Amplifier

If R1 = R5, R3 = R6, and R4 = R7, then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R4}{R3} \left( \frac{R2 + 2R1}{R2} \right) \tag{3}$$

and  $A_V \cong 100$  for the circuit shown in Figure 6-4 (R2 = 9.1k $\Omega$ ). Note that  $V_{IN} = V_{IN+} - V_{IN-}$ .

#### 6.2.2 Low-Leakage Sample-and-Hold

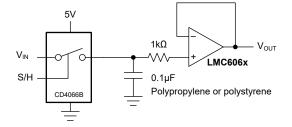


Figure 6-5. Low-Leakage Sample-and-Hold

#### 6.2.3 1Hz Square-Wave Oscillator

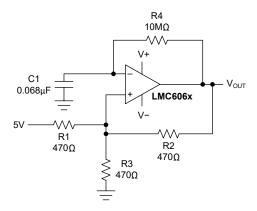


Figure 6-6. 1Hz Square-Wave Oscillator

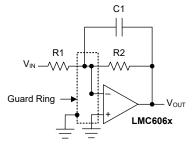
#### 6.3 Layout

#### 6.3.1 Layout Guidelines

#### 6.3.1.1 Printed Circuit Board Layout For High Impedance Work

Generally, any circuit that must operate with less than 1000pA of leakage current requires special layout of the printed circuit board (PCB). To take advantage of the ultra-low bias current of the LMC606x, typically less than 10fA, having an excellent layout is essential. Fortunately, the techniques used to obtain low leakages are quite simple. First, do not ignore the surface leakage of the PCB, even though the leakage can sometimes appear acceptably low. Under conditions of high humidity, dust, or contamination, the surface leakage can be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC606x inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, and so on, connected to the op amp inputs, as in Figure 6-11. To have a significant effect, place guard rings on both the top and bottom of the PCB. Then connect this foil to a voltage that is at the same voltage as the amplifier inputs, because no leakage current can flow between two points at the same potential. For example, a PCB trace-to-pad resistance of  $10^{12}\Omega$ , which is normally considered a very large resistance, can leak 5pA if the trace is a 5V bus adjacent to the pad of the input. This leak can cause a 100 times degradation from the LMC606x actual performance. However, if a guard ring is held within 5mV of the inputs, then even a resistance of  $10^{11}\Omega$  causes only 0.05pA of leakage current. See Figure 6-7 to Figure 6-9 for typical connections of guard rings for standard op amp configurations.



Guard R2 Ring Vout LMC606x

Figure 6-8. Typical Connections of Guard Rings:
Noninverting Amplifier

Figure 6-7. Typical Connections of Guard Rings: Inverting Amplifier

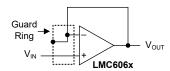
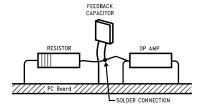


Figure 6-9. Typical Connections of Guard Rings: Follower

When laying out a PCB for the sake of just a few circuits is not practical, the following technique is even better than a guard ring. Do not insert the input pin of the amplifier into the PCB at all. Instead, bend the pin up in the air, and use only air as an insulator. Air is an excellent insulator. In this case, you forgo some of the advantages of PCB construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. Figure 6-10 shows an example of air wiring.



Note: Input pins are lifted out of the PCB and soldered directly to components. All other pins are connected to the PCB.

## Figure 6-10. Air Wiring

# 6.3.2 Layout Example

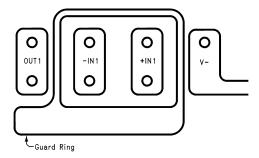


Figure 6-11. Example of Guard Ring in PCB Layout



# 7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

#### 7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 7.2 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 7.3 Trademarks

TI E2E<sup>™</sup> is a trademark of Texas Instruments.

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## 7.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 7.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

# 8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| C | hanges from Revision D (March 2013) to Revision E (March 2025)  | Page           |
|---|---|----------------|
| • | Added LMC6061 and LMC6064 and related content to this data sheet  | 1              |
| • | Deleted LMC6061 and LMC6064 PDIP content  | 1              |
| • | Added application circuit   | 1              |
| • | Added Pin Configuration and Functions   |                |
| • | Updated pin names in Pin Configuration and Functions  |                |
| • | Added ESD Ratings   | <mark>5</mark> |
| • | Deleted notes 1 and 2 from Recommended Operating Conditions   |                |
| • | Added Thermal Information   |                |
| • | Updated to combine ac and dc Electrical Characteristics   | <mark>7</mark> |
| • | Updated parameter names and symbols   | <mark>7</mark> |
| • | Deleted notes 1, 2, and 3 from dc Electrical Characteristics  |                |
| • | Changed input current noise from 0.2fA/√Hz to 12.5fA/Hz   | <mark>7</mark> |
| • | Moved note 4 conditions from dc Electrical Characteristics to open-loop voltage gain test conditions  | <mark>7</mark> |
| • | Changed open-loop gain for $R_L = 100k\Omega$ (sourcing) from $400V/mV$ to $300V/mV$ for LMC606xAI  | <mark>7</mark> |
| • | Changed open-loop gain for $R_L = 100 \text{k}\Omega$ (sourcing, $T_A = -40 ^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$ ) from 300V/mV to 200V/mV |                |
|   | for LMC606xAI   | <mark>7</mark> |
| • | Changed open-loop gain for RL = $25k\Omega$ (sourcing) from $400V/mV$ to $300V/mV$ for LMC606xAI  | <mark>7</mark> |
| • | Deleted notes 1, 2, and 3 from ac Electrical Characteristics  | <mark>7</mark> |
| • | Moved note 4 conditions from ac <i>Electrical Characteristics</i> to slew rate test conditions  | <mark>7</mark> |
|   |   |                |

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| <ul> <li>Moved note 5 conditions from ac <i>Electrical Characteristics</i> to crosstalk test cond</li> <li>Change supply current parameter name to quiescent current per amplifier</li> </ul> |      |
|---|------|
| Updated Amplifier Topology  |      |
|   |      |
| Changes from Revision C (March 2013) to Revision D (March 2013)   | Page |
| Changed layout of National Data Sheet to TI format  | 17   |

# 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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# **PACKAGING INFORMATION**

| Orderable part number | Status (1) | Material type | Package   Pins  | Package qty   Carrier | <b>RoHS</b> (3) | Lead finish/<br>Ball material | MSL rating/<br>Peak reflow | Op temp (°C) | Part marking (6) |
|-----------------------|------------|---------------|-----------------|-----------------------|-----------------|-------------------------------|----------------------------|--------------|------------------|
| LMC6061AIM/NOPB       | Obsolete   | Production    | SOIC (D)   8    | -                     | -               | Call TI                       | Call TI                    | -40 to 85    | LMC60<br>61AIM   |
| LMC6061AIMX/NOPB      | Active     | Production    | SOIC (D)   8    | 2500   LARGE T&R      | Yes             | SN                            | Level-1-260C-UNLIM         | -40 to 85    | LMC60<br>61AIM   |
| LMC6061AIMX/NOPB.A    | Active     | Production    | SOIC (D)   8    | 2500   LARGE T&R      | Yes             | SN                            | Level-1-260C-UNLIM         | -40 to 85    | LMC60<br>61AIM   |
| LMC6061AIMX/NOPB.B    | Active     | Production    | SOIC (D)   8    | 2500   LARGE T&R      | Yes             | SN                            | Level-1-260C-UNLIM         | -40 to 85    | LMC60<br>61AIM   |
| LMC6061IM/NOPB        | Obsolete   | Production    | SOIC (D)   8    | -                     | -               | Call TI                       | Call TI                    | -40 to 85    | LMC60<br>61IM    |
| LMC6061IMX/NOPB       | Active     | Production    | SOIC (D)   8    | 2500   LARGE T&R      | Yes             | SN                            | Level-1-260C-UNLIM         | -40 to 85    | LMC60<br>61IM    |
| LMC6061IMX/NOPB.A     | Active     | Production    | SOIC (D)   8    | 2500   LARGE T&R      | Yes             | SN                            | Level-1-260C-UNLIM         | -40 to 85    | LMC60<br>61IM    |
| LMC6061IMX/NOPB.B     | Active     | Production    | SOIC (D)   8    | 2500   LARGE T&R      | Yes             | SN                            | Level-1-260C-UNLIM         | -40 to 85    | LMC60<br>61IM    |
| LMC6062AIM/NOPB       | Obsolete   | Production    | SOIC (D)   8    | -                     | -               | Call TI                       | Call TI                    | -40 to 85    | LMC60<br>62AIM   |
| LMC6062AIMX/NOPB      | Active     | Production    | SOIC (D)   8    | 2500   LARGE T&R      | Yes             | SN                            | Level-1-260C-UNLIM         | -40 to 85    | LMC60<br>62AIM   |
| LMC6062AIMX/NOPB.A    | Active     | Production    | SOIC (D)   8    | 2500   LARGE T&R      | Yes             | SN                            | Level-1-260C-UNLIM         | -40 to 85    | LMC60<br>62AIM   |
| LMC6062AIMX/NOPB.B    | Active     | Production    | SOIC (D)   8    | 2500   LARGE T&R      | Yes             | SN                            | Level-1-260C-UNLIM         | -40 to 85    | LMC60<br>62AIM   |
| LMC6062I MDC          | Active     | Production    | DIESALE (Y)   0 | 288   OTHER           | Yes             | Call TI                       | Level-1-NA-UNLIM           | -40 to 85    |                  |
| LMC6062I-MDC.A        | Active     | Production    | DIESALE (Y)   0 | 288   OTHER           | Yes             | Call TI                       | Level-1-NA-UNLIM           | -40 to 85    |                  |
| LMC6062IM/NOPB        | Obsolete   | Production    | SOIC (D)   8    | -                     | -               | Call TI                       | Call TI                    | -40 to 85    | LMC60<br>62IM    |
| LMC6062IMX/NOPB       | Active     | Production    | SOIC (D)   8    | 2500   LARGE T&R      | Yes             | SN                            | Level-1-260C-UNLIM         | -40 to 85    | LMC60<br>62IM    |
| LMC6062IMX/NOPB.A     | Active     | Production    | SOIC (D)   8    | 2500   LARGE T&R      | Yes             | SN                            | Level-1-260C-UNLIM         | -40 to 85    | LMC60<br>62IM    |





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| Orderable part number | Status (1) | Material type | Dell material Deals willow |                  | Peak reflow | Op temp (°C) | Part marking (6)   |           |                |
|-----------------------|------------|---------------|----------------------------|------------------|-------------|--------------|--------------------|-----------|----------------|
| LMC6062IMX/NOPB.B     | Active     | Production    | SOIC (D)   8               | 2500   LARGE T&R | Yes         | SN           | Level-1-260C-UNLIM | -40 to 85 | LMC60<br>62IM  |
| LMC6062IN/NOPB        | Active     | Production    | PDIP (P)   8               | 40   TUBE        | Yes         | NIPDAU       | Level-1-NA-UNLIM   | -40 to 85 | LMC6062<br>IN  |
| LMC6062IN/NOPB.A      | Active     | Production    | PDIP (P)   8               | 40   TUBE        | Yes         | NIPDAU       | Level-1-NA-UNLIM   | -40 to 85 | LMC6062<br>IN  |
| LMC6062IN/NOPB.B      | Active     | Production    | PDIP (P)   8               | 40   TUBE        | Yes         | NIPDAU       | Level-1-NA-UNLIM   | -40 to 85 | LMC6062<br>IN  |
| LMC6064AIM/NOPB       | Obsolete   | Production    | SOIC (D)   14              | -                | -           | Call TI      | Call TI            | -40 to 85 | LMC6064<br>AIM |
| LMC6064AIMX/NOPB      | Active     | Production    | SOIC (D)   14              | 2500   LARGE T&R | Yes         | SN           | Level-1-260C-UNLIM | -40 to 85 | LMC6064<br>AIM |
| LMC6064AIMX/NOPB.A    | Active     | Production    | SOIC (D)   14              | 2500   LARGE T&R | Yes         | SN           | Level-1-260C-UNLIM | -40 to 85 | LMC6064<br>AIM |
| LMC6064AIMX/NOPB.B    | Active     | Production    | SOIC (D)   14              | 2500   LARGE T&R | -           | Call TI      | Call TI            | -40 to 85 |                |
| LMC6064IM/NOPB        | Obsolete   | Production    | SOIC (D)   14              | -                | -           | Call TI      | Call TI            | -40 to 85 | LMC6064IM      |
| LMC6064IMX/NOPB       | Active     | Production    | SOIC (D)   14              | 2500   LARGE T&R | Yes         | SN           | Level-1-260C-UNLIM | -40 to 85 | LMC6064IM      |
| LMC6064IMX/NOPB.A     | Active     | Production    | SOIC (D)   14              | 2500   LARGE T&R | Yes         | SN           | Level-1-260C-UNLIM | -40 to 85 | LMC6064IM      |
| LMC6064IMX/NOPB.B     | Active     | Production    | SOIC (D)   14              | 2500   LARGE T&R | -           | Call TI      | Call TI            | -40 to 85 |                |

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.



# **PACKAGE OPTION ADDENDUM**

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(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



# TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

| A0 | Dimension designed to accommodate the component width     |
|----|---|
| В0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

| Device           | Package<br>Type | Package<br>Drawing |    | SPQ  | Reel<br>Diameter<br>(mm) | Reel<br>Width<br>W1 (mm) | A0<br>(mm) | B0<br>(mm) | K0<br>(mm) | P1<br>(mm) | W<br>(mm) | Pin1<br>Quadrant |
|------------------|-----------------|--------------------|----|------|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| LMC6061AIMX/NOPB | SOIC            | D                  | 8  | 2500 | 330.0                    | 12.4                     | 6.5        | 5.4        | 2.0        | 8.0        | 12.0      | Q1               |
| LMC6061IMX/NOPB  | SOIC            | D                  | 8  | 2500 | 330.0                    | 12.4                     | 6.5        | 5.4        | 2.0        | 8.0        | 12.0      | Q1               |
| LMC6062AIMX/NOPB | SOIC            | D                  | 8  | 2500 | 330.0                    | 12.4                     | 6.5        | 5.4        | 2.0        | 8.0        | 12.0      | Q1               |
| LMC6062IMX/NOPB  | SOIC            | D                  | 8  | 2500 | 330.0                    | 12.4                     | 6.5        | 5.4        | 2.0        | 8.0        | 12.0      | Q1               |
| LMC6064AIMX/NOPB | SOIC            | D                  | 14 | 2500 | 330.0                    | 16.4                     | 6.5        | 9.35       | 2.3        | 8.0        | 16.0      | Q1               |
| LMC6064IMX/NOPB  | SOIC            | D                  | 14 | 2500 | 330.0                    | 16.4                     | 6.5        | 9.35       | 2.3        | 8.0        | 16.0      | Q1               |



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\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMC6061AIMX/NOPB | SOIC         | D               | 8    | 2500 | 367.0       | 367.0      | 35.0        |
| LMC6061IMX/NOPB  | SOIC         | D               | 8    | 2500 | 367.0       | 367.0      | 35.0        |
| LMC6062AIMX/NOPB | SOIC         | D               | 8    | 2500 | 367.0       | 367.0      | 35.0        |
| LMC6062IMX/NOPB  | SOIC         | D               | 8    | 2500 | 367.0       | 367.0      | 35.0        |
| LMC6064AIMX/NOPB | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 35.0        |
| LMC6064IMX/NOPB  | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 35.0        |

# **PACKAGE MATERIALS INFORMATION**

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## **TUBE**



\*All dimensions are nominal

| Device           | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| LMC6062IN/NOPB   | Р            | PDIP         | 8    | 40  | 502    | 14     | 11938  | 4.32   |
| LMC6062IN/NOPB.A | Р            | PDIP         | 8    | 40  | 502    | 14     | 11938  | 4.32   |
| LMC6062IN/NOPB.B | Р            | PDIP         | 8    | 40  | 502    | 14     | 11938  | 4.32   |





#### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







## NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



# P (R-PDIP-T8)

# PLASTIC DUAL-IN-LINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.



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Last updated 10/2025