LM7171QML Very High Speed, High Output Current, Voltage Feedback Amplifier

Check for Samples: LM7171QML, LM7171QML-SP

FEATURES

- **(Typical Unless Otherwise Noted)**
- **Easy-To-Use Voltage Feedback Topology**
- **Very High Slew Rate: 2400V/µs**
- **Wide Unity-Gain Bandwidth: 200 MHz**
- **−3 dB Frequency @ A_V = +2: 220 MHz**
- **Low Supply Current: 6.5 mA**
- **High Open Loop Gain: 85 dB**
- **High Output Current: 100 mA**
- **Specified for ±15V and ±5V Operation**
- **Available with Radiation Guarantee**
  - **Total Ionizing Dose 300 Krad(Si)**
  - **ELDRS Free 300 Krad(Si)**

APPLICATIONS

- **HDSL and ADSL Drivers**
- **Multimedia Broadcast Systems**
- **Professional Video Cameras**
- **Video Amplifiers**
- **Copiers/Scanners/Fax**
- **HDTV Amplifiers**
- **Pulse Amplifiers and Peak Detectors**
- **CATV/Fiber Optics Signal Processing**

DESCRIPTION

The LM7171 is a high speed voltage feedback amplifier that has the slewing characteristic of a current feedback amplifier; yet it can be used in all traditional voltage feedback amplifier configurations. The LM7171 is stable for gains as low as +2 or −1. It provides a very high slew rate at 4100V/µs and a wide unity-gain bandwidth of 200 MHz while consuming only 6.5 mA of supply current. It is ideal for video and high speed signal processing applications such as HDSL and pulse amplifiers. With 100 mA output current, the LM7171 can be used for video distribution, as a transformer driver or as a laser diode driver.

Operation on ±15V power supplies allows for large signal swings and provides greater dynamic range and signal-to-noise ratio. The LM7171 offers low SFDR and THD, ideal for ADC/DAC systems. In addition, the LM7171 is specified for ±5V operation for portable applications.

The LM7171 is built on Texas Instruments's advanced VIP™ III (Vertically integrated PNP) complementary bipolar process.

Connection Diagram

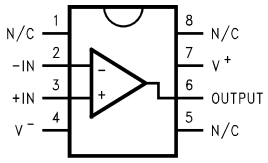

Figure 1. 8-Pin CDIP Top View

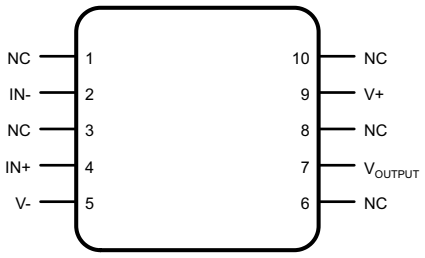

Figure 2. 10-Pin CFP Top View

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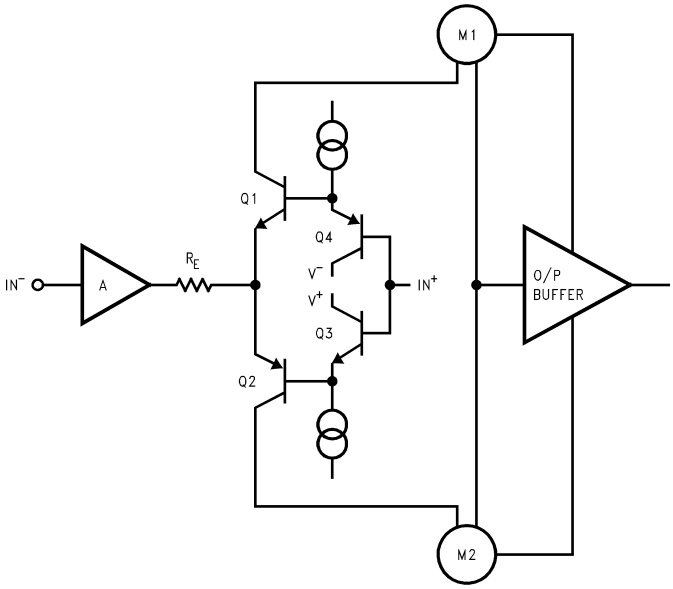
Simplified Schematic Diagram

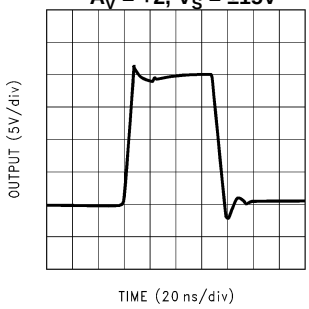


Note: M1 and M2 are current mirrors.

Typical Performance

Large Signal Pulse Response

A_V = +2, V_S = ±15V



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Supply Voltage (V^+–V^-)			36V
Differential Input Voltage(2)			±10V
Maximum Power Dissipation(3)			730mW
Output Short Circuit to Ground(4)			Continuous
Storage Temperature Range			−65°C ≤ T_A ≤ +150°C
Thermal Resistance(5)	θ_{JA}	8LD CDIP (Still Air)	106°C/W
		8LD CDIP (500LF/Min Air flow)	53°C/W
		10LD CFP (Still Air)	182°C/W
		10LD CFP (500LF/Min Air flow)	105°C/W
		10LD CFP "WG" (device 01, 02) (Still Air)	182°C/W
		10LD CFP "WG" (device 01, 02) (500LF/Min Air flow)	105°C/W
	θ_{JC}	8LD CDIP	3°C/W
		10LD CFP	5°C/W
		10LD CFP "WG" (device 01, 02)(6)	5°C/W
Package Weight (Typical)	8LD CDIP		965mg
	10LD CFP		235mg
	10LD CFP "WG" (device 01, 02)		230mg
Maximum Junction Temperature(3)			150°C
ESD Tolerance(7)			3000V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For specified specifications and test conditions, see the Electrical Characteristics. The specified specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) Differential input voltage is applied at V_S = ±15V.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.
(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(5) All numbers apply for packages soldered directly into a PC board.
(6) The package material for these devices allows much improved heat transfer over our standard ceramic packages. In order to take full advantage of this improved heat transfer, heat sinking must be provided between the package base (directly beneath the die), and either metal traces on, or thermal vias through, the printed circuit board. Without this additional heat sinking, device power dissipation must be calculated using θ_{JA}, rather than θ_{JC}, thermal resistance. It must not be assumed that the device leads will provide substantial heat transfer out the package, since the thermal resistance of the leadframe material is very poor, relative to the material of the package base. The stated θ_{JC} thermal resistance is for the package material only, and does not account for the additional thermal resistance between the package base and the printed circuit board. The user must determine the value of the additional thermal resistance and must combine this with the stated value for the package, to calculate the total allowed power dissipation for the device.
(7) Human body model, 1.5 kΩ in series with 100 pF.

Recommended Operating Conditions(1)

Supply Voltage	5.5V ≤ V_S ≤ 36V
Operating Temperature Range	−55°C ≤ T_A ≤ +125°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For specified specifications and test conditions, see the Electrical Characteristics. The specified specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Table 1. Quality Conformance Inspection Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp °C
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

LM7171 (±15) Electrical Characteristics DC Parameters[1][2]

The following conditions apply, unless otherwise specified.

DC: T_J = 25°C, V^+ = +15V, V^- = −15V, V_{CM} = 0V, and R_L > 1MΩ

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage			−1.0	1.0	mV	1
				−7.0	7.0	mV	2, 3
$+I_{IB}$	Input Bias Current				10	µA	1
					12	µA	2, 3
$-I_{IB}$	Input Bias Current				10	µA	1
					12	µA	2, 3
I_{IO}	Input Offset Current			−4.0	4.0	µA	1
				−6.0	6.0	µA	2, 3
CMRR	Common Mode Rejection Ratio	V_{CM} = ±10V		85		dB	1
				70		dB	2, 3
PSRR	Power Supply Rejection Ratio	V_S = ±15V to ±5V		85		dB	1
				80		dB	2, 3
A_V	Large Signal Voltage Gain	R_L = 1KΩ, V_O = ±5V	See[3]	80		dB	1
			See[3]	75		dB	2, 3
		R_L = 100Ω, V_O = ±5V	See[3]	75		dB	1
			See[3]	70		dB	2, 3
V_O	Output Swing	R_L = 1KΩ		13	-13	V	1
				12.7	-12.7	V	2, 3
		R_L = 100Ω		10.5	-9.5	V	1
				9.5	-9.0	V	2, 3
	Output Current (Open Loop)	Sourcing R_L = 100Ω	See[4]	105		mA	1
			See[4]	95		mA	2, 3
		Sinking R_L = 100Ω	See[4]		-95	mA	1
			See[4]		-90	mA	2, 3
I_S	Supply Current				8.5	mA	1
					9.5	mA	2, 3

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are specified only for the conditions as specified in MIL-STD-883, per Test Method 1019, Condition A.

(2) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. Low dose rate testing has been peformed on a wafer-by-wafer basis, per Test Method 1019, Condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS).

(3) Large signal voltage gain is the total output swing divided by the input signal required to produce that swing. For V_S = ±15V, V_{OUT} = ±5V. For V_S = ±5V, V_{OUT} = ±1V.

(4) The open loop output current is specified, by the measurement of the open loop output voltage swing, using 100Ω output load.

LM7171 (±15) Electrical Characteristics AC Parameters[1][2]

The following conditions apply, unless otherwise specified.

AC: T_J = 25°C, V^+ = +15V, V^- = −15V, V_{CM} = 0V, and R_L > 1MΩ

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
SR	Slew Rate	A_V = 2, V_I = ±2.5V 3nS Rise & Fall time	See[3][4]	2000		V/µS	4
GBW	Unity-Gain Bandwidth		See[5]	170		MHz	4

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are specified only for the conditions as specified in MIL-STD-883, per Test Method 1019, Condition A.

(2) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. Low dose rate testing has been peformed on a wafer-by-wafer basis, per Test Method 1019, Condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS).

(3) See AN00001 for SR test circuit.

(4) Slew Rate measured between ±4V.

(5) See AN00002 for GBW test circuit.

LM7171 (±15) Electrical Characteristics DC Drift Parameters[1][2]

The following conditions apply, unless otherwise specified.

DC: T_J = 25°C, V^+ = +15V, V^- = −15V, V_{CM} = 0V, and R_L > 1MΩ

Delta calculations performed on QMLV devices at group B , subgroup 5.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage			-250	250	µV	1
$+I_{Bias}$	Input Bias Current			-500	500	nA	1
$-I_{Bias}$	Input Bias Current			-500	500	nA	1

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are specified only for the conditions as specified in MIL-STD-883, per Test Method 1019, Condition A.

(2) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. Low dose rate testing has been peformed on a wafer-by-wafer basis, per Test Method 1019, Condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS).

LM7171 (±5) Electrical Characteristics DC Parameters[1][2]

The following conditions apply, unless otherwise specified.

DC: T_J = 25°C, V^+ = +5V, V^- = −5V, V_{CM} = 0V, and R_L > 1MΩ

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage			−1.5	1.5	mV	1
				−7.0	7.0	mV	2, 3
$+I_{IB}$	Input Bias Current				10	µA	1
					12	µA	2, 3
$-I_{IB}$	Input Bias Current				10	µA	1
					12	µA	2, 3
I_{IO}	Input Offset Current			−4.0	4.0	µA	1
				−6.0	6.0	µA	2, 3
CMRR	Common Mode Rejection Ratio	V_{CM} = ±2.5V		80		dB	1
				70		dB	2, 3
A_V	Large Signal Voltage Gain	R_L = 1KΩ, V_O = ±1V	See[3]	75		dB	1
			See[3]	70		dB	2, 3
		R_L = 100Ω, V_O = ±1V	See[3]	72		dB	1
			See[3]	67		dB	2, 3
V_O	Output Swing	R_L = 1KΩ		3.2	-3.2	V	1
				3.0	-3.0	V	2, 3
		R_L = 100Ω		2.9	-2.9	V	1
				2.8	-2.75	V	2, 3
	Output Current (Open Loop)	Sourcing R_L = 100Ω	See[4]	29		mA	1
			See[4]	28		mA	2, 3
		Sinking R_L = 100Ω	See[4]		-29	mA	1
			See[4]		-27.5	mA	2, 3
I_S	Supply Current				8.0	mA	1
					9.0	mA	2, 3

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are specified only for the conditions as specified in MIL-STD-883, per Test Method 1019, Condition A.

(2) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. Low dose rate testing has been peformed on a wafer-by-wafer basis, per Test Method 1019, Condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS).

(3) Large signal voltage gain is the total output swing divided by the input signal required to produce that swing. For V_S = ±15V, V_{OUT} = ±5V. For V_S = ±5V, V_{OUT} = ±1V.

(4) The open loop output current is specified, by the measurement of the open loop output voltage swing, using 100Ω output load.

LM7171 (±5) Electrical Characteristics DC Drift Parameters[1][2]

The following conditions apply, unless otherwise specified.

DC: T_J = 25°C, V^+ = +5V, V^- = −5V, V_{CM} = 0V, and R_L > 1MΩ

Delta calculations performed on QMLV devices at group B , subgroup 5.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage			-250	250	µV	1
$+I_{Bias}$	Input Bias Current			-500	500	nA	1
$-I_{Bias}$	Input Bias Current			-500	500	nA	1

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are specified only for the conditions as specified in MIL-STD-883, per Test Method 1019, Condition A.

(2) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. Low dose rate testing has been peformed on a wafer-by-wafer basis, per Test Method 1019, Condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS).

Typical Performance Characteristics

unless otherwise noted, T_A= 25°C

Supply Current vs Supply Voltage

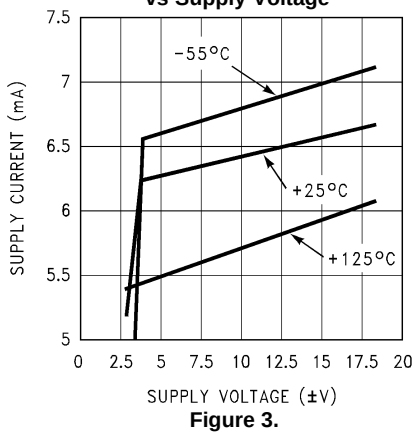


Figure 3.

Supply Current vs Temperature

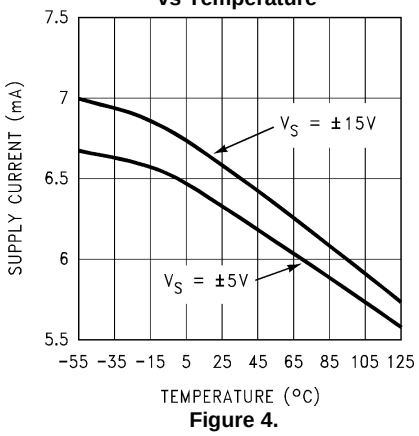


Figure 4.

Input Offset Voltage vs Temperature

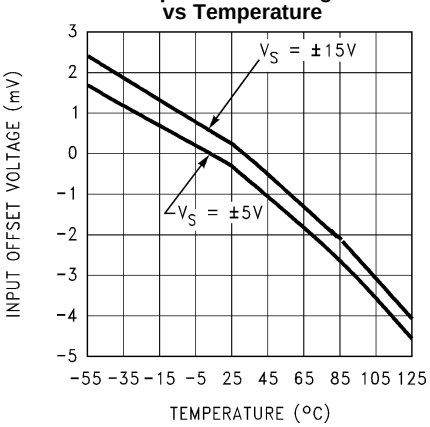


Figure 5.

Input Bias Current vs Temperature

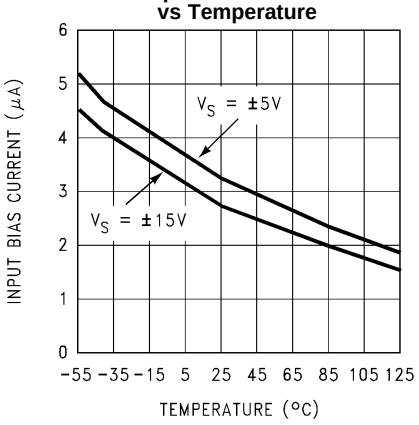


Figure 6.

Short Circuit Current vs Temperature (Sourcing)

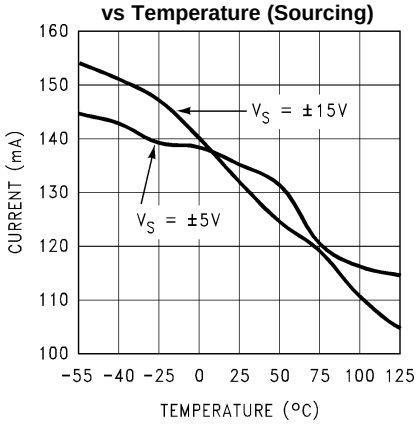


Figure 7.

Short Circuit Current vs Temperature (Sinking)

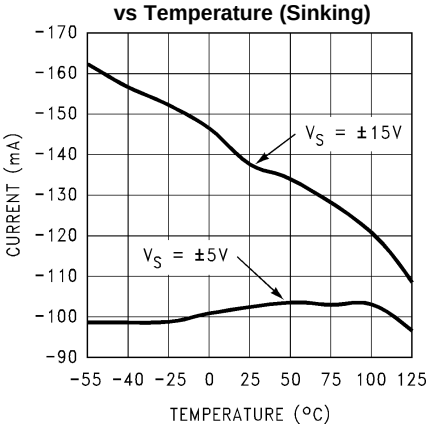


Figure 8.

Typical Performance Characteristics (continued)

unless otherwise noted, T_A= 25°C

Output Voltage vs Output Current

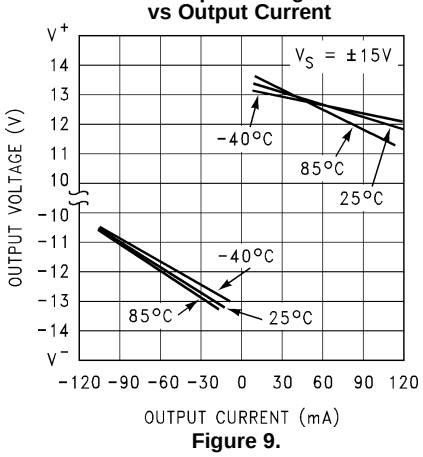


Figure 9.

Output Voltage vs Output Current

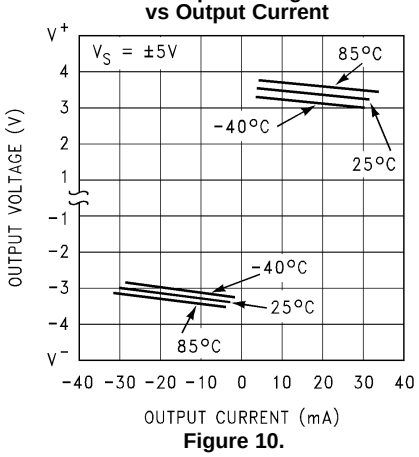


Figure 10.

CMRR vs Frequency

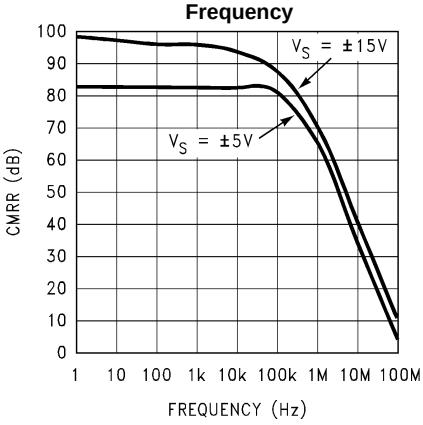


Figure 11.

PSRR vs Frequency

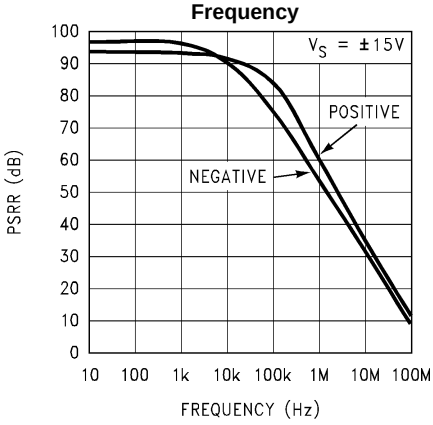


Figure 12.

PSRR vs Frequency

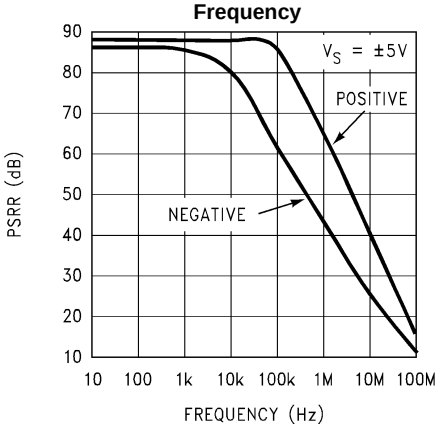


Figure 13.

Open Loop Frequency Response

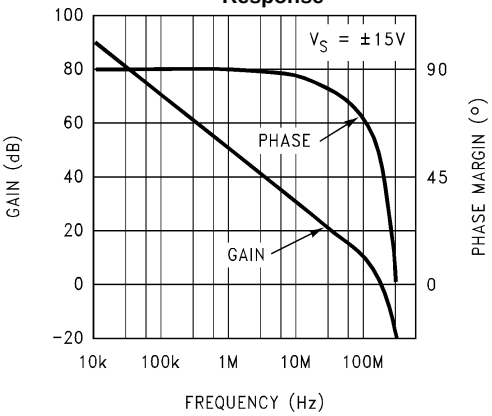


Figure 14.

Typical Performance Characteristics (continued)

unless otherwise noted, T_A= 25°C

Open Loop Frequency Response

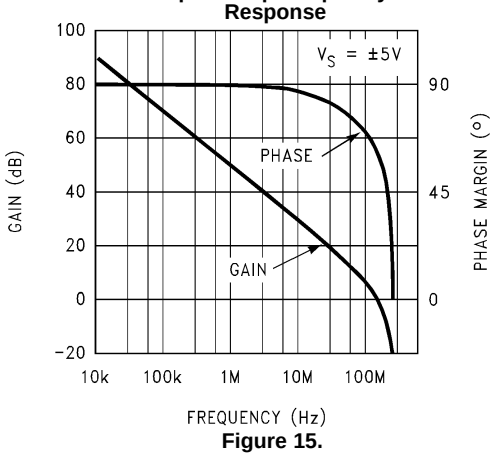


Figure 15.

Gain-Bandwidth Product vs Supply Voltage

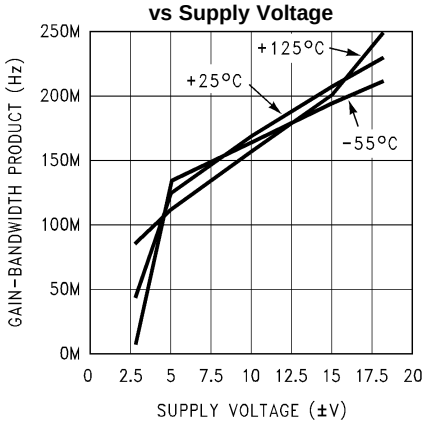


Figure 16.

Gain-Bandwidth Product vs Load Capacitance

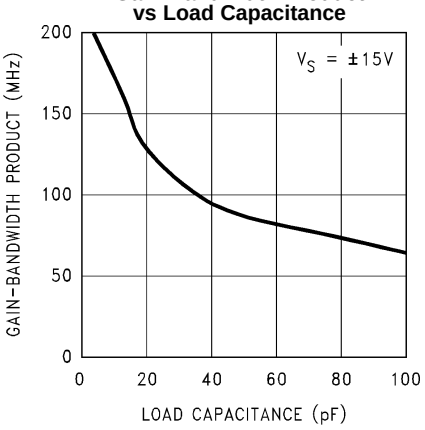


Figure 17.

Large Signal Voltage Gain vs Load

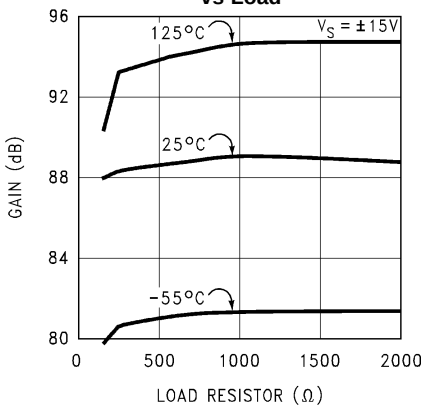


Figure 18.

Large Signal Voltage Gain vs Load

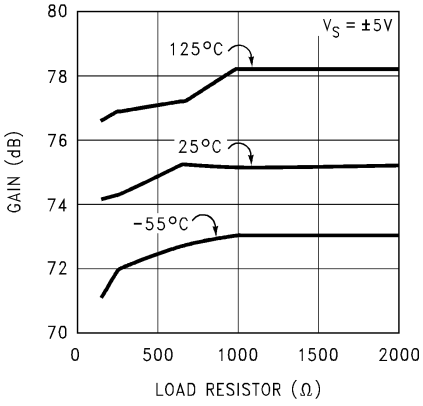


Figure 19.

Input Voltage Noise vs Frequency

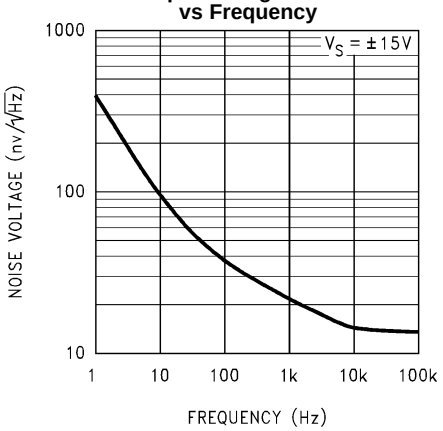


Figure 20.

Typical Performance Characteristics (continued)

unless otherwise noted, T_A= 25°C

Input Voltage Noise vs Frequency

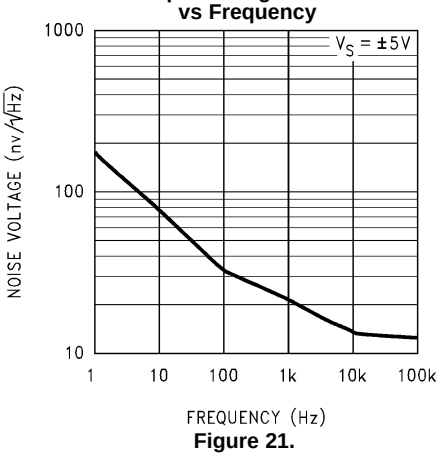


Figure 21.

Input Current Noise vs Frequency

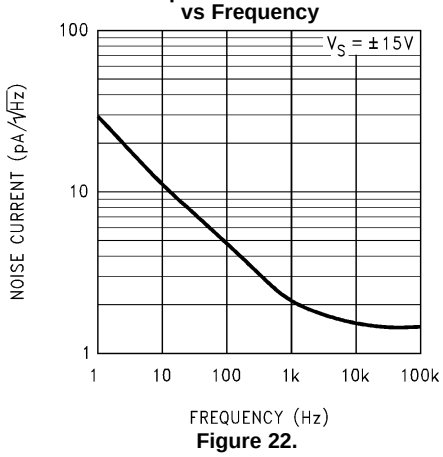


Figure 22.

Input Current Noise vs Frequency

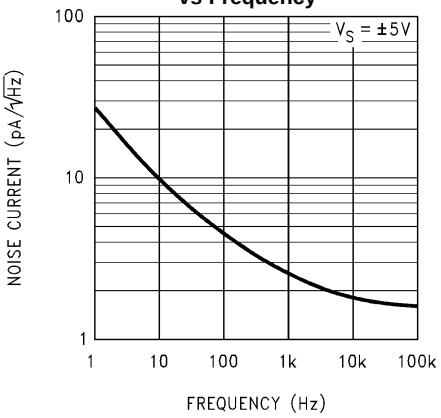


Figure 23.

Slew Rate vs Supply Voltage

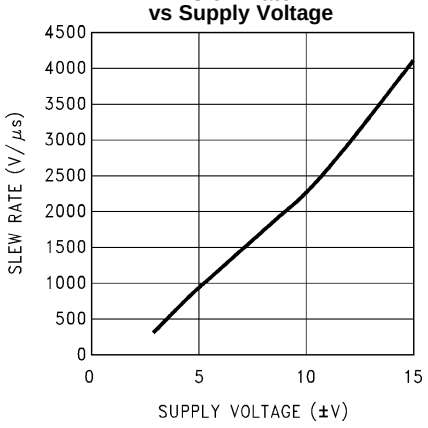


Figure 24.

Slew Rate vs Input Voltage

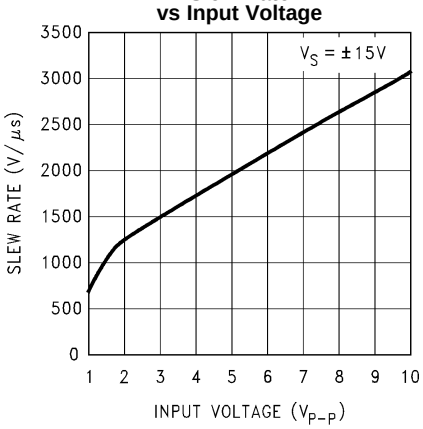


Figure 25.

Slew Rate vs Load Capacitance

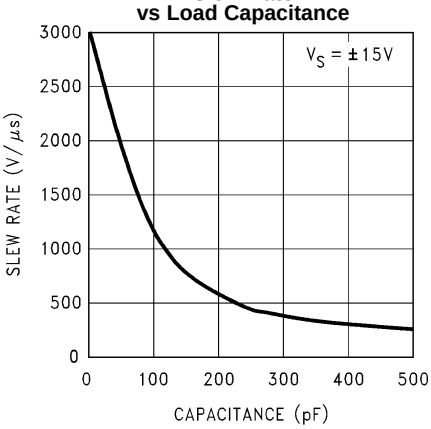


Figure 26.

Typical Performance Characteristics (continued)

unless otherwise noted, T_A= 25°C

Open Loop Output Impedance vs Frequency

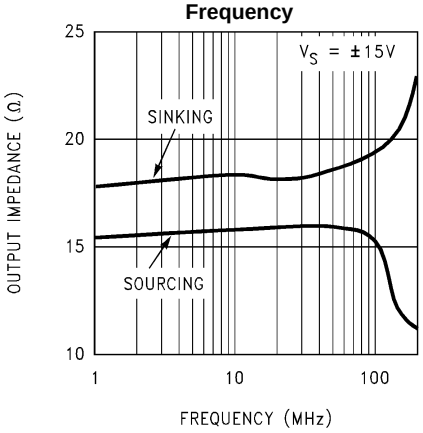


Figure 27.

Open Loop Output Impedance vs Frequency

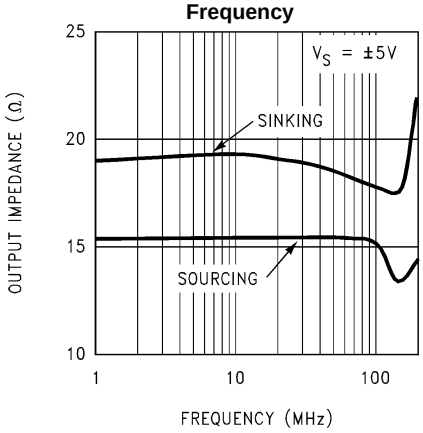


Figure 28.

Large Signal Pulse Response A_V = −1, V_S = ±15V

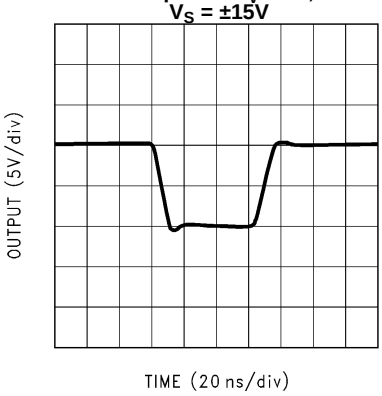


Figure 29.

Large Signal Pulse Response A_V = −1, V_S = ±5V

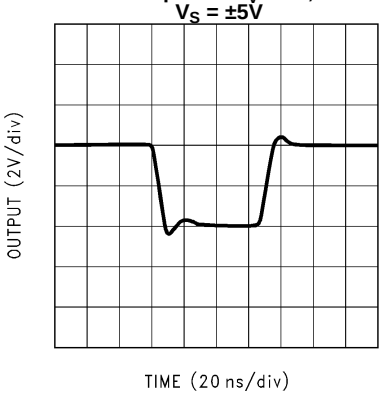


Figure 30.

Large Signal Pulse Response A_V = +2, V_S = ±15V

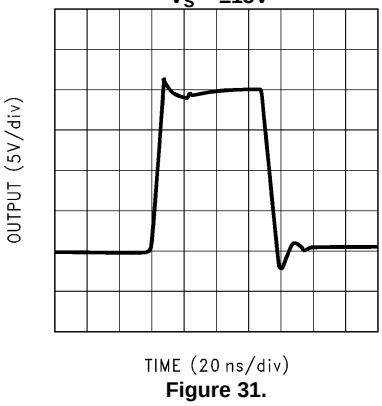


Figure 31.

Large Signal Pulse Response A_V = +2, V_S = ±5V

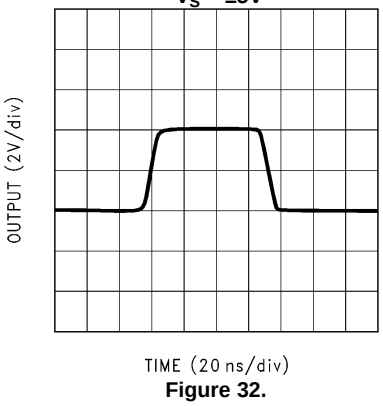


Figure 32.

Typical Performance Characteristics (continued)

unless otherwise noted, T_A= 25°C

Small Signal Pulse Response A_V = −1, V_S = ±15V

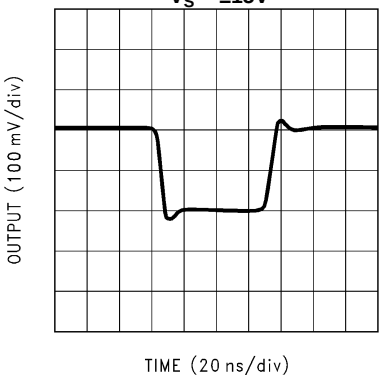


Figure 33.

Small Signal Pulse Response A_V = −1, V_S = ±5V

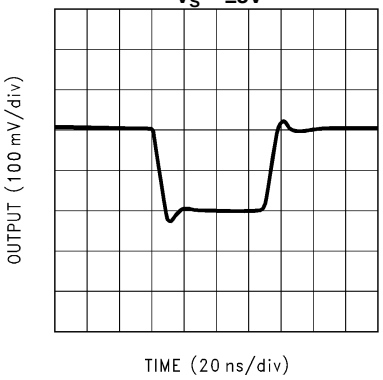


Figure 34.

Small Signal Pulse Response A_V = +2, V_S = ±15V

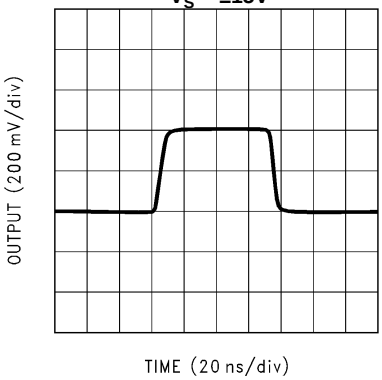


Figure 35.

Small Signal Pulse Response A_V = +2, V_S = ±5V

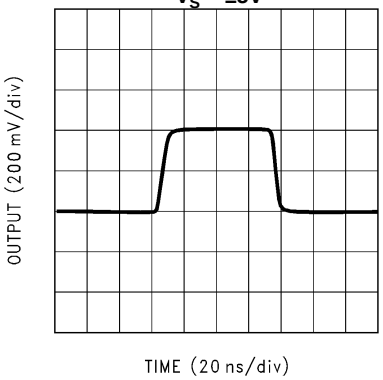


Figure 36.

Closed Loop Frequency Response vs Supply Voltage (A_V = +2)

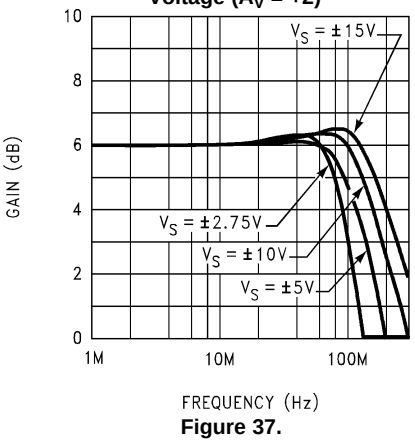


Figure 37.

Closed Loop Frequency Response vs Capacitive Load (A_V = +2)

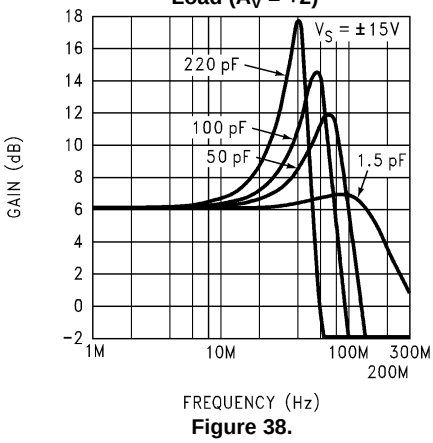


Figure 38.

Typical Performance Characteristics (continued)

unless otherwise noted, T_A= 25°C

Closed Loop Frequency Response vs Capacitive Load (A_V = +2)

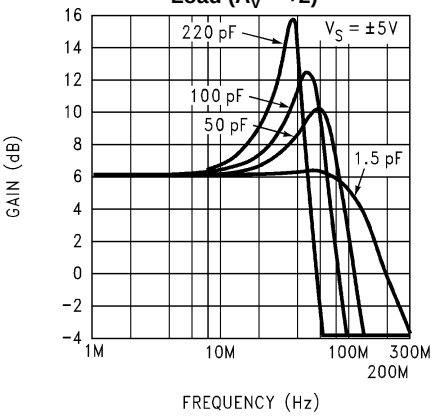


Figure 39.

Closed Loop Frequency Response vs Input Signal Level (A_V = +2)

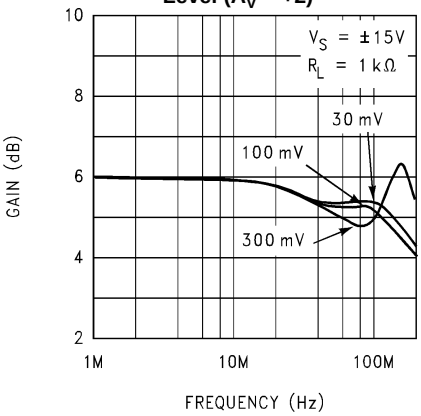


Figure 40.

Closed Loop Frequency Response vs Input Signal Level (A_V = +2)

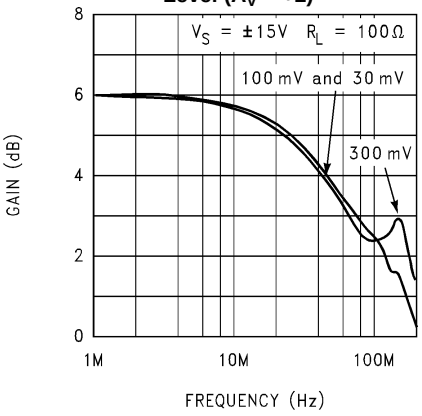


Figure 41.

Closed Loop Frequency Response vs Input Signal Level (A_V = +2)

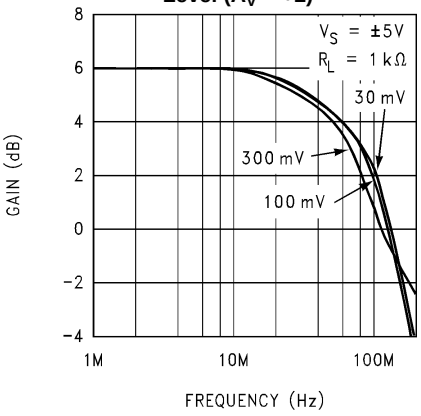


Figure 42.

Closed Loop Frequency Response vs Input Signal Level (A_V = +2)

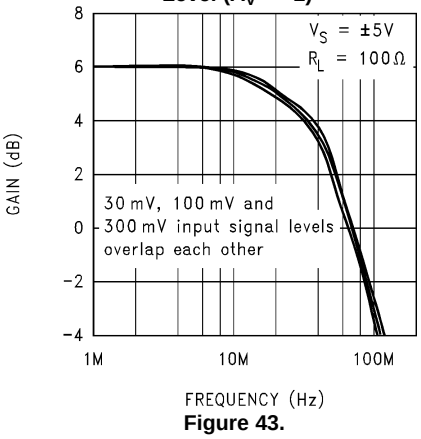


Figure 43.

Closed Loop Frequency Response vs Input Signal Level (A_V = +4)

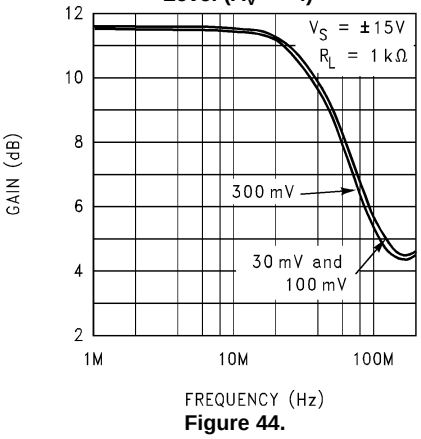


Figure 44.

Typical Performance Characteristics (continued)

unless otherwise noted, T_A= 25°C

Closed Loop Frequency Response vs Input Signal Level (A_V = +4)

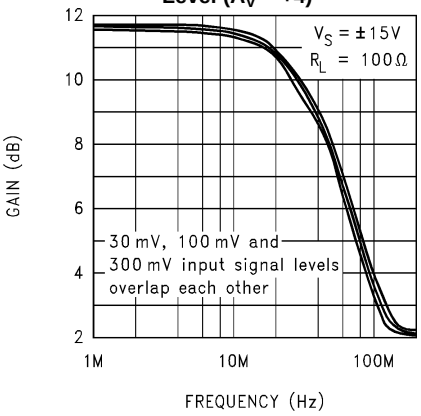


Figure 45.

Closed Loop Frequency Response vs Input Signal Level (A_V = +4)

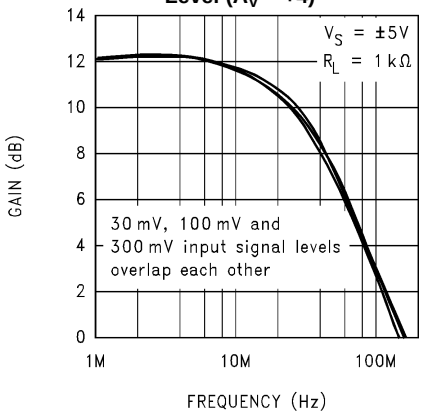


Figure 46.

Closed Loop Frequency Response vs Input Signal Level (A_V = +4)

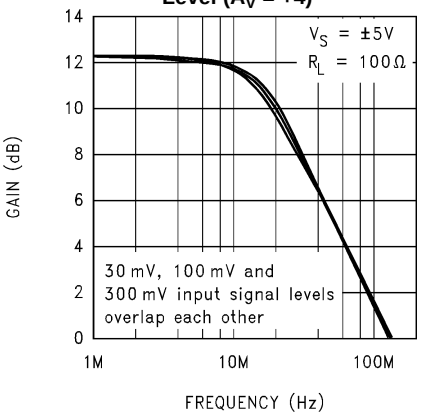


Figure 47.

Total Harmonic Distortion vs Frequency

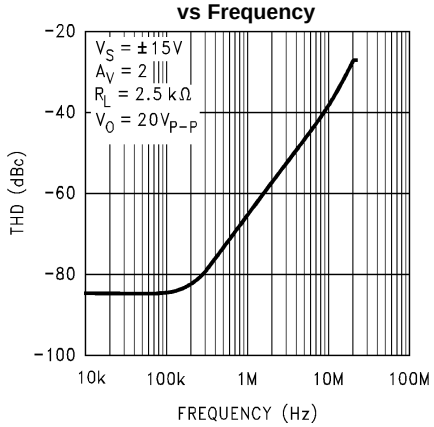


Figure 48.

Total Harmonic Distortion vs Frequency

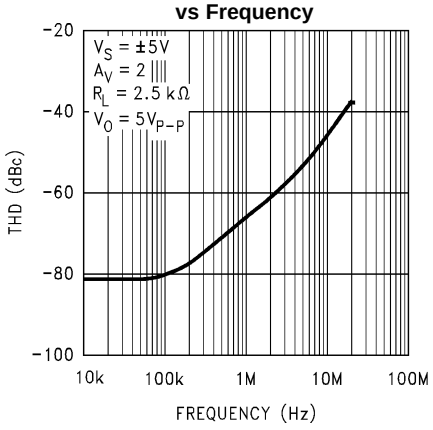


Figure 49.

Undistorted Output Swing vs Frequency

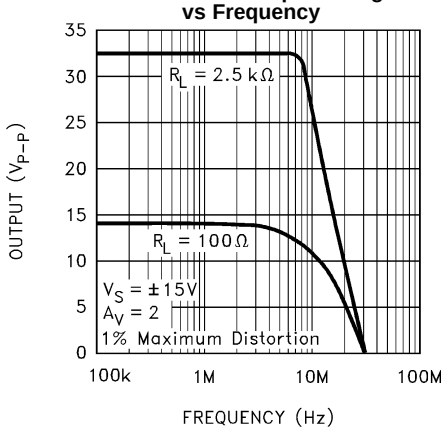


Figure 50.

Typical Performance Characteristics (continued)

unless otherwise noted, T_A= 25°C

Undistorted Output Swing vs Frequency

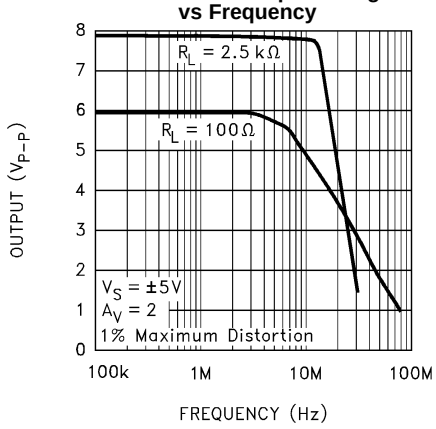


Figure 51.

Undistorted Output Swing vs Frequency

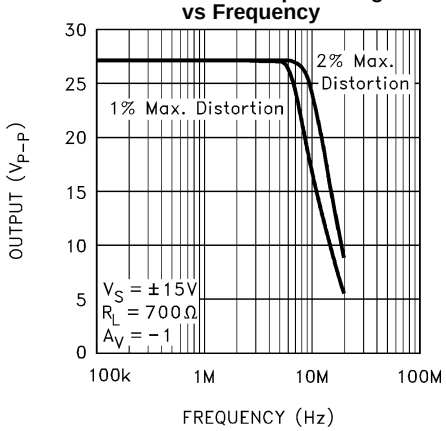


Figure 52.

Harmonic Distortion vs Frequency

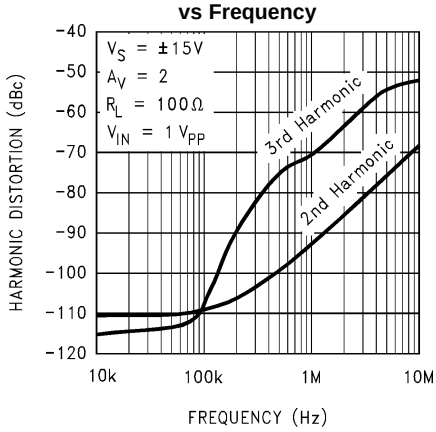


Figure 53.

Harmonic Distortion vs Frequency

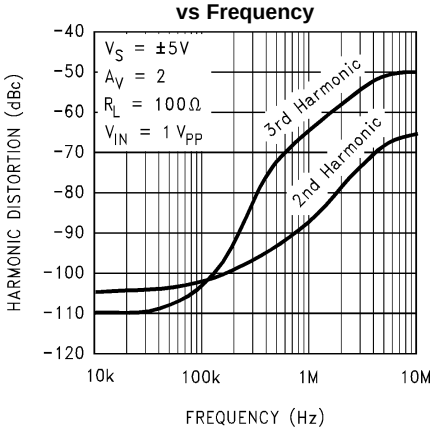
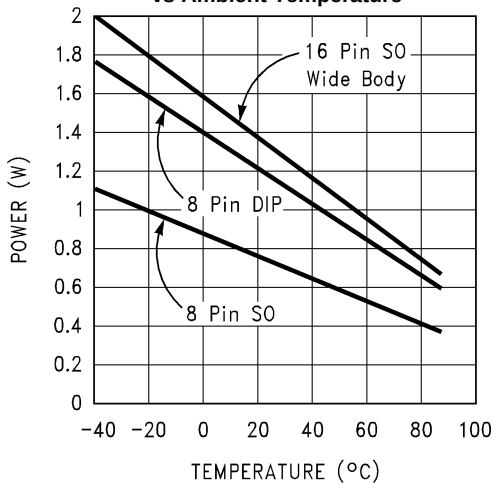


Figure 54.

Maximum Power Dissipation vs Ambient Temperature



The THD measurement at low frequency is limited by the test instrument.

Figure 55.

APPLICATION NOTES

LM7171 Performance Discussion

The LM7171 is a very high speed, voltage feedback amplifier. It consumes only 6.5 mA supply current while providing a unity-gain bandwidth of 200 MHz and a slew rate of 4100V/µs. It also has other great features such as low differential gain and phase and high output current.

The LM7171 is a true voltage feedback amplifier. Unlike current feedback amplifiers (CFAs) with a low inverting input impedance and a high non-inverting input impedance, both inputs of voltage feedback amplifiers (VFAs) have high impedance nodes. The low impedance inverting input in CFAs and a feedback capacitor create an additional pole that will lead to instability. As a result, CFAs cannot be used in traditional op amp circuits such as photodiode amplifiers, I-to-V converters and integrators where a feedback capacitor is required.

LM7171 Circuit Operation

The class AB input stage in the LM7171 is fully symmetrical and has a similar slewing characteristic to the current feedback amplifiers. In the LM7171 Simplified Schematic, Q1 through Q4 form the equivalent of the current feedback input buffer, R_E the equivalent of the feedback resistor, and stage A buffers the inverting input. The triple-buffered output stage isolates the gain stage from the load to provide low output impedance.

LM7171 Slew Rate Characteristic

The slew rate of the LM7171 is determined by the current available to charge and discharge an internal high impedance node capacitor. This current is the differential input voltage divided by the total degeneration resistor R_E. Therefore, the slew rate is proportional to the input voltage level, and the higher slew rates are achievable in the lower gain configurations. A curve of slew rate versus input voltage level is provided in the “Typical Performance Characteristics”.

When a very fast large signal pulse is applied to the input of an amplifier, some overshoot or undershoot occurs. By placing an external resistor such as 1 kΩ in series with the input of the LM7171, the bandwidth is reduced to help lower the overshoot.

Slew Rate Limitation

If the amplifier's input signal has too large of an amplitude at too high of a frequency, the amplifier is said to be slew rate limited; this can cause ringing in time domain and peaking in frequency domain at the output of the amplifier.

In the Typical Performance Characteristics section, there are several curves of A_V = +2 and A_V = +4 versus input signal levels. For the A_V = +4 curves, no peaking is present and the LM7171 responds identically to the different input signal levels of 30 mV, 100 mV and 300 mV.

For the A_V = +2 curves, slight peaking occurs. This peaking at high frequency (>100 MHz) is caused by a large input signal at high enough frequency that exceeds the amplifier's slew rate. The peaking in frequency response does not limit the pulse response in time domain, and the LM7171 is stable with noise gain of ≥+2.

Layout Consideration

PRINTED CIRCUIT BOARDS AND HIGH SPEED OP AMPS

There are many things to consider when designing PC boards for high speed op amps. Without proper caution, it is very easy to have excessive ringing, oscillation and other degraded AC performance in high speed circuits. As a rule, the signal traces should be short and wide to provide low inductance and low impedance paths. Any unused board space needs to be grounded to reduce stray signal pickup. Critical components should also be grounded at a common point to eliminate voltage drop. Sockets add capacitance to the board and can affect high frequency performance. It is better to solder the amplifier directly into the PC board without using any socket.

USING PROBES

Active (FET) probes are ideal for taking high frequency measurements because they have wide bandwidth, high input impedance and low input capacitance. However, the probe ground leads provide a long ground loop that will produce errors in measurement. Instead, the probes can be grounded directly by removing the ground leads and probe jackets and using scope probe jacks.

COMPONENT SELECTION AND FEEDBACK RESISTOR

It is important in high speed applications to keep all component leads short. For discrete components, choose carbon composition-type resistors and mica-type capacitors. Surface mount components are preferred over discrete components for minimum inductive effect.

Large values of feedback resistors can couple with parasitic capacitance and cause undesirable effects such as ringing or oscillation in high speed amplifiers. For the LM7171, a feedback resistor of 510Ω gives optimal performance.

Compensation for Input Capacitance

The combination of an amplifier's input capacitance with the gain setting resistors, adds a pole that can cause peaking or oscillation. To solve this problem, a feedback capacitor with a value

$$C_F > (R_G \times C_{IN})/R_F \quad (1)$$

can be used to cancel that pole. For the LM7171, a feedback capacitor of 2 pF is recommended. Figure 56 illustrates the compensation circuit.

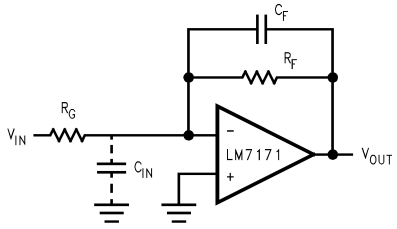


Figure 56. Compensating for Input Capacitance

Power Supply Bypassing

Bypassing the power supply is necessary to maintain low power supply impedance across frequency. Both positive and negative power supplies should be bypassed individually by placing 0.01 µF ceramic capacitors directly to power supply pins and 2.2 µF tantalum capacitors close to the power supply pins.

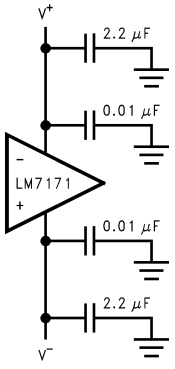


Figure 57. Power Supply Bypassing

Termination

In high frequency applications, reflections occur if signals are not properly terminated. Figure 58 shows a properly terminated signal while Figure 59 shows an improperly terminated signal.

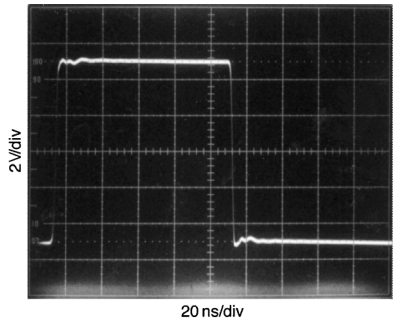


Figure 58. Properly Terminated Signal

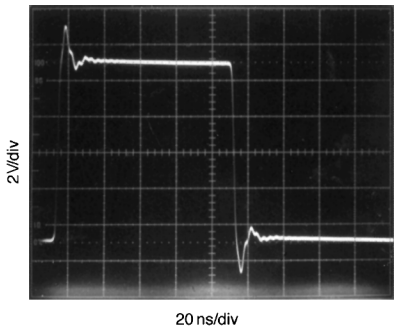


Figure 59. Improperly Terminated Signal

To minimize reflection, coaxial cable with matching characteristic impedance to the signal source should be used. The other end of the cable should be terminated with the same value terminator or resistor. For the commonly used cables, RG59 has 75Ω characteristic impedance, and RG58 has 50Ω characteristic impedance.

Driving Capacitive Loads

Amplifiers driving capacitive loads can oscillate or have ringing at the output. To eliminate oscillation or reduce ringing, an isolation resistor can be placed as shown below in Figure 60. The combination of the isolation resistor and the load capacitor forms a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of the isolation resistor; the bigger the isolation resistor, the more damped the pulse response becomes. For LM7171, a 50Ω isolation resistor is recommended for initial evaluation. Figure 61 shows the LM7171 driving a 150 pF load with the 50Ω isolation resistor.

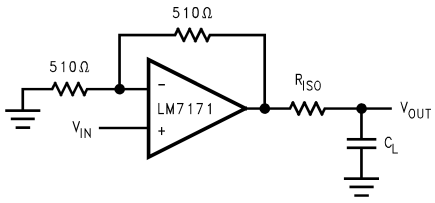


Figure 60. Isolation Resistor Used to Drive Capacitive Load

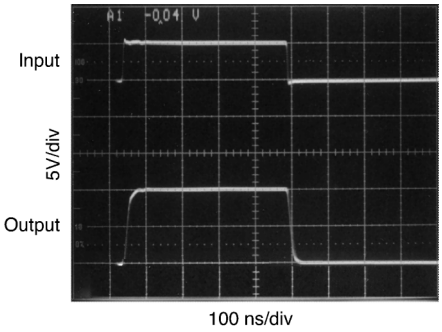


Figure 61. The LM7171 Driving a 150 pF Load with a 50Ω Isolation Resistor

Power Dissipation

The maximum power allowed to dissipate in a device is defined as:

$$P_D = (T_{J(max)} - T_A)/\theta_{JA} \quad (2)$$

Where

PD is the power dissipation in a device

$T_{J(max)}$ is the maximum junction temperature

T_A is the ambient temperature

θ_{JA} is the thermal resistance of a particular package

For example, for the LM7171 in a CFP package, the maximum power dissipation at 25°C ambient temperature is 680 mW.

Thermal resistance, θ_{JA}, depends on parameters such as die size, package size and package material. The smaller the die size and package, the higher θ_{JA} becomes. The 8-pin CDIP package has a lower thermal resistance (106°C/W) than that of the CFP (182°C/W). Therefore, for higher dissipation capability, use an 8-pin CDIP package.

The total power dissipated in a device can be calculated as:

$$P_D = P_Q + P_L \quad (3)$$

P_Q is the quiescent power dissipated in a device with no load connected at the output. P_L is the power dissipated in the device with a load connected at the output; it is not the power dissipated by the load.

Furthermore,

P_Q: = supply current × total supply voltage with no load

P_L: = output current × (voltage difference between supply voltage and output voltage of the same side of supply voltage)

For example, the total power dissipated by the LM7171 with V_S = ±15V and output voltage of 10V into 1 kΩ is

$P_D = P_Q + P_L$

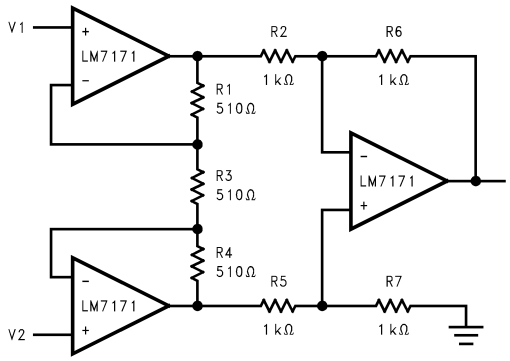
= (6.5 mA) × (30V) + (10 mA) × (15V − 10V)

= 195 mW + 50 mW

= 245 mW

Application Circuit

Figure 62. Fast Instrumentation Amplifier

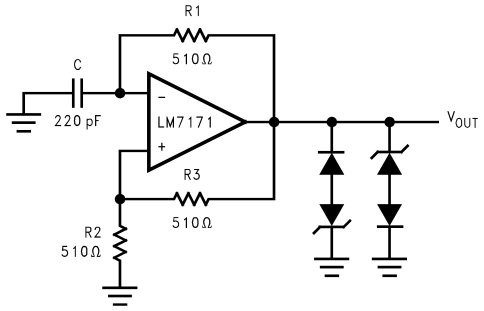


$$V_{IN} = V_2 - V_1$$

if R6 = R2, R7 = R5, and R1 = R4

$$\frac{V_{OUT}}{V_{IN}} = \frac{R6}{R2}\left(1 + 2\frac{R1}{R3}\right) = 3$$

Figure 63. Multivibrator



$$f = \frac{1}{2\left(R1\ C\ \ln\left(1 + 2\frac{R2}{R3}\right)\right)}$$

f = 4 MHz

Figure 64. Pulse Width Modulator

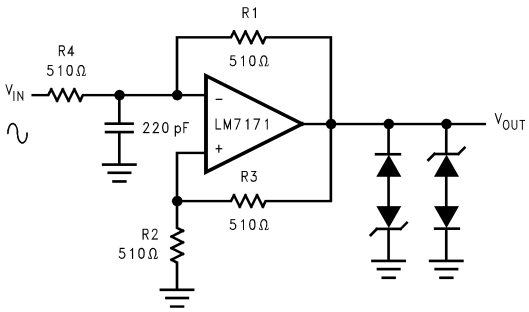
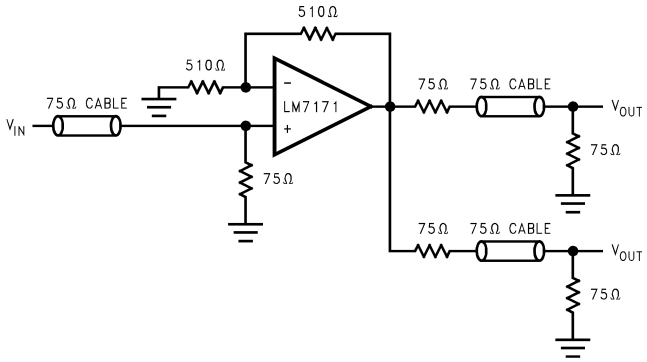


Figure 65. Video Line Driver



REVISION HISTORY

Released	Revision	Section	Changes
02/04/09	A	New Release, Corporate format	1 MDS data sheet converted into one Corp. data sheet format. Added ELDRS NSID's to Ordering Information Table. MNLM7171AM-X-RH Rev 0C0 will be archived.

Changes from Revision B (April 2013) to Revision C **Page**

- Changed layout of National Data Sheet to TI format 23

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9553601QPA	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM7171AMJQML 5962-95536 01QPA Q ACO 01QPA Q >T
5962-9553601QXA	Active	Production	CFP (NAC) | 10	54 | JEDEC TRAY (5+1)	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM7171AM WG Q 5962-95536 01QXA ACO 01QXA >T
5962F9553601VHA	Active	Production	CFP (NAD) | 10	19 | TUBE	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM7171AM WFQMLV Q 5962F95536 01VHA ACO 01VHA >T
5962F9553601VPA	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM7171AMJFQV 5962F95536 01VPA Q ACO 01VPA Q >T
5962F9553601VXA	Active	Production	CFP (NAC) | 10	54 | JEDEC TRAY (5+1)	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM7171AM WGFQMLV Q 5962F95536 01VXA ACO 01VXA >T
5962F9553602VHA	Active	Production	CFP (NAD) | 10	19 | TUBE	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM7171AM WFLQMLV Q 5962F95536 02VHA ACO 02VHA >T
LM7171AMJ-QML	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM7171AMJQML 5962-95536 01QPA Q ACO 01QPA Q >T
LM7171AMJ-QML.A	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM7171AMJQML 5962-95536 01QPA Q ACO 01QPA Q >T

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM7171AMJFQMLV	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM7171AMJFQV 5962F95536 01VPA Q ACO 01VPA Q >T
LM7171AMJFQMLV.A	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM7171AMJFQV 5962F95536 01VPA Q ACO 01VPA Q >T
LM7171AMWFLQMLV	Active	Production	CFP (NAD) | 10	19 | TUBE	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM7171AM WFLQMLV Q 5962F95536 02VHA ACO 02VHA >T
LM7171AMWFQMLV	Active	Production	CFP (NAD) | 10	19 | TUBE	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM7171AM WFQMLV Q 5962F95536 01VHA ACO 01VHA >T
LM7171AMWFQMLV.A	Active	Production	CFP (NAD) | 10	19 | TUBE	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM7171AM WFQMLV Q 5962F95536 01VHA ACO 01VHA >T
LM7171AMWG-QML	Active	Production	CFP (NAC) | 10	54 | JEDEC TRAY (5+1)	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM7171AM WG Q 5962-95536 01QXA ACO 01QXA >T
LM7171AMWG-QML.A	Active	Production	CFP (NAC) | 10	54 | JEDEC TRAY (5+1)	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM7171AM WG Q 5962-95536 01QXA ACO 01QXA >T
LM7171AMWGFQMLV	Active	Production	CFP (NAC) | 10	54 | JEDEC TRAY (5+1)	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM7171AM WGFQMLV Q 5962F95536 01VXA ACO 01VXA >T

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM7171AMWGFQMLV.A	Active	Production	CFP (NAC) | 10	54 | JEDEC TRAY (5+1)	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM7171AM WGFQMLV Q 5962F95536 01VXA ACO 01VXA >T
LM7171NAB/EM	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM7171NABEM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

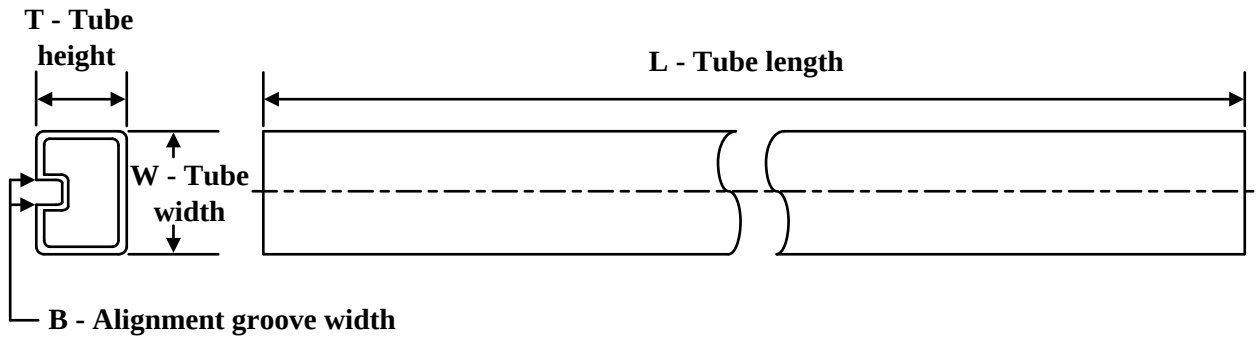
OTHER QUALIFIED VERSIONS OF LM7171QML, LM7171QML-SP :

- Military : LM7171QML
- Space : LM7171QML-SP

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

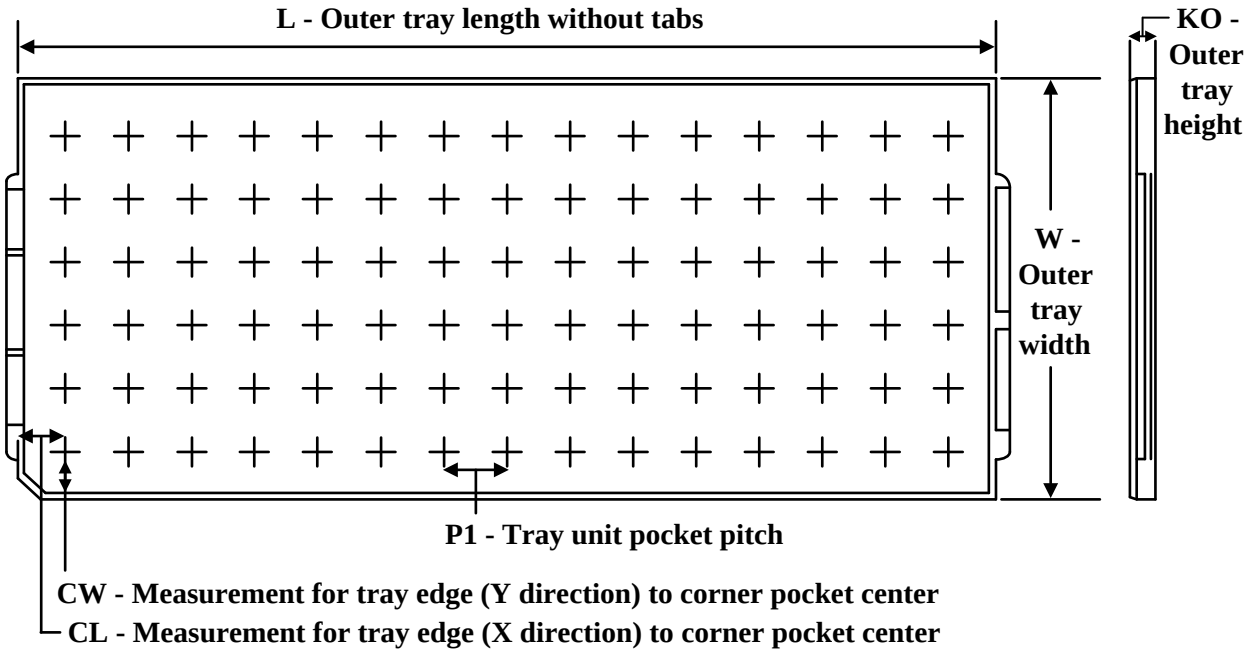
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9553601QPA	NAB	CDIP	8	40	506.98	15.24	13440	NA
5962F9553601VHA	NAD	CFP	10	19	502	23	9398	9.78
5962F9553601VPA	NAB	CDIP	8	40	506.98	15.24	13440	NA
LM7171AMJ-QML	NAB	CDIP	8	40	506.98	15.24	13440	NA
LM7171AMJ-QML.A	NAB	CDIP	8	40	506.98	15.24	13440	NA
LM7171AMJFQMLV	NAB	CDIP	8	40	506.98	15.24	13440	NA
LM7171AMJFQMLV.A	NAB	CDIP	8	40	506.98	15.24	13440	NA
LM7171AMWFQMLV	NAD	CFP	10	19	502	23	9398	9.78
LM7171AMWFQMLV.A	NAD	CFP	10	19	502	23	9398	9.78
LM7171NAB/EM	NAB	CDIP	8	40	506.98	15.24	13440	NA

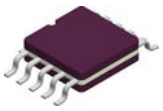
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
5962-9553601QXA	NAC	CFP	10	54	6 X 9	100	101.6	101.6	8001	2.78	16.08	16.08
5962F9553601VXA	NAC	CFP	10	54	6 X 9	100	101.6	101.6	8001	2.78	16.08	16.08
LM7171AMWG-QML	NAC	CFP	10	54	6 X 9	100	101.6	101.6	8001	2.78	16.08	16.08
LM7171AMWG-QML.A	NAC	CFP	10	54	6 X 9	100	101.6	101.6	8001	2.78	16.08	16.08
LM7171AMWGFQMLV	NAC	CFP	10	54	6 X 9	100	101.6	101.6	8001	2.78	16.08	16.08
LM7171AMWGFQMLV.A	NAC	CFP	10	54	6 X 9	100	101.6	101.6	8001	2.78	16.08	16.08

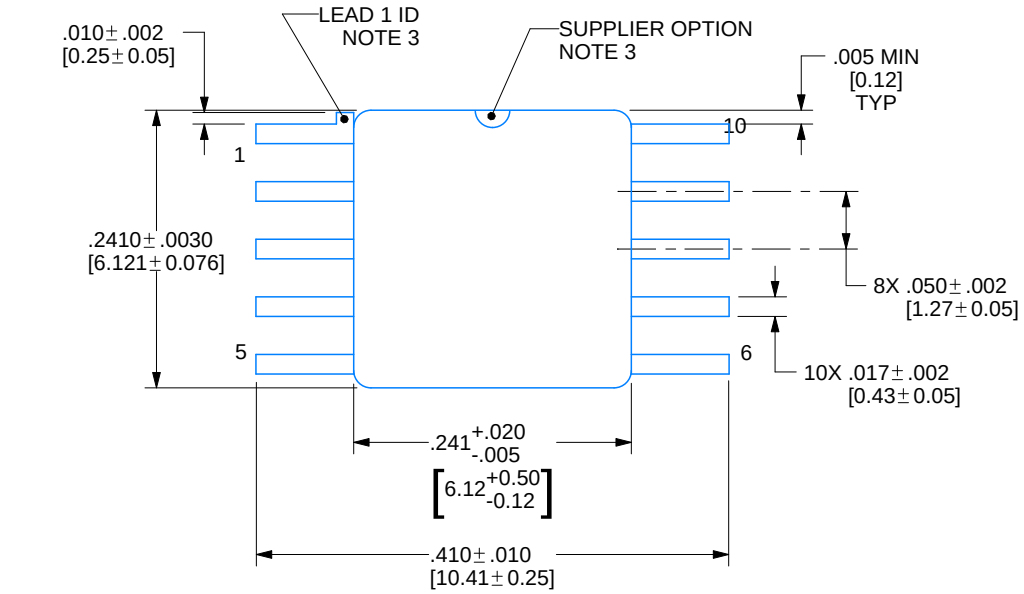


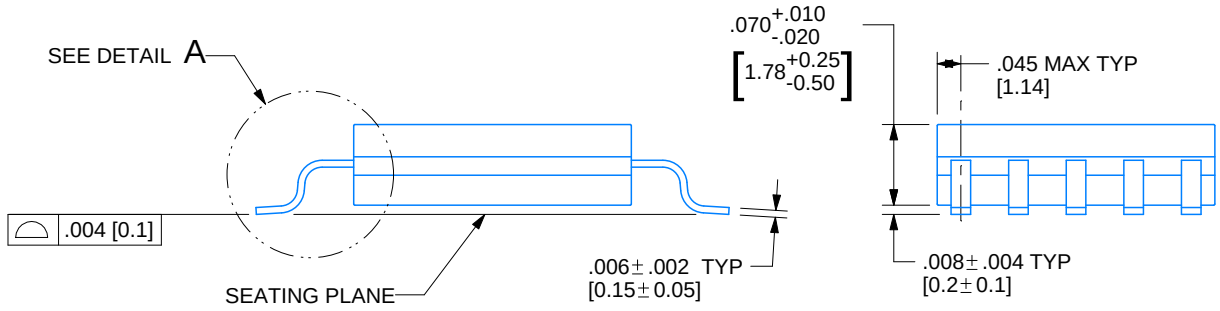
PACKAGE OUTLINE

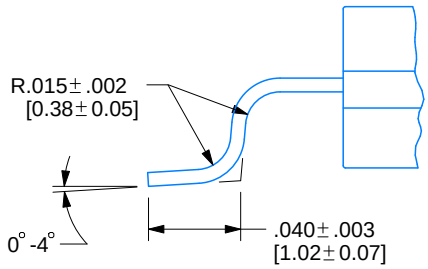
NAC0010A

CFP - 2.33mm max height

CERAMIC FLATPACK







DETAIL A
TYPICAL

4215196/D 08/2022

NOTES:

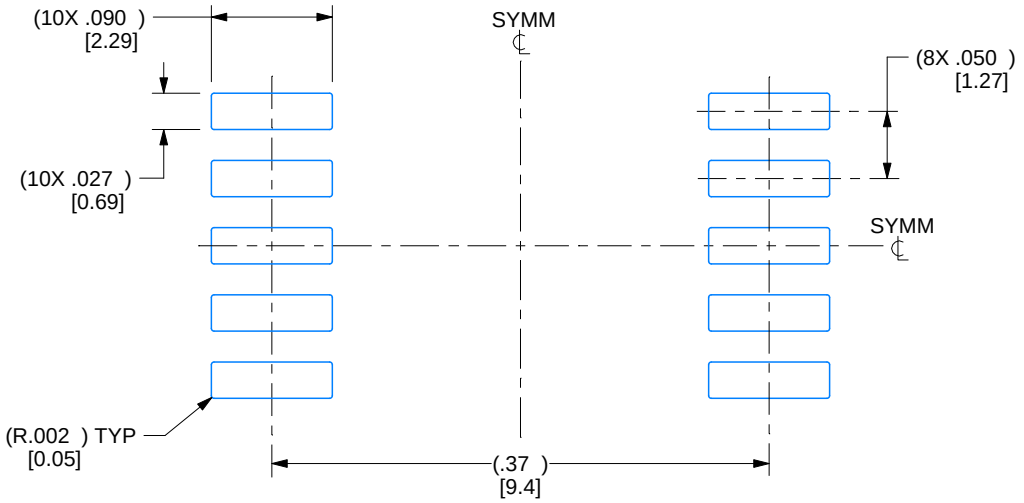
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. For solder thickness and composition, see the "Lead Finish Composition/Thickness" link in the packaging section of the Texas Instruments website
3. Lead 1 identification shall be:
   a) A notch or other mark within this area
   b) A tab on lead 1, either side
4. No JEDEC registration as of December 2021

EXAMPLE BOARD LAYOUT

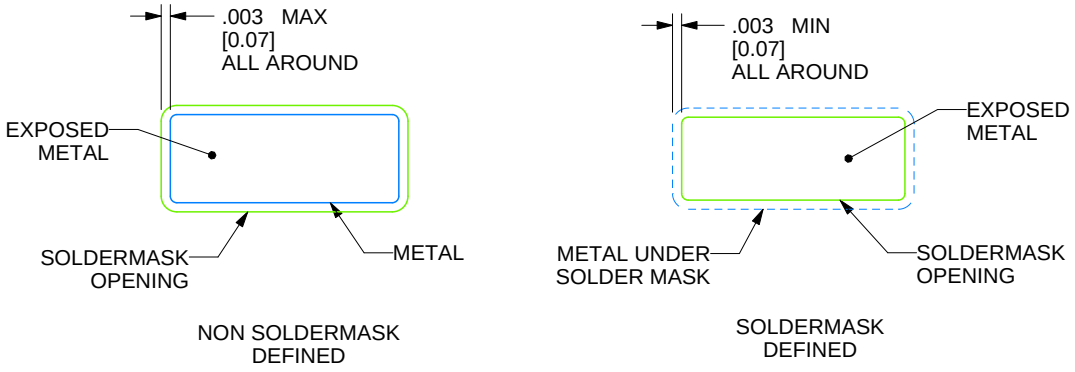
NAC0010A

CFP - 2.33mm max height

CERAMIC FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 7X



4215196/D 08/2022

REVISIONS

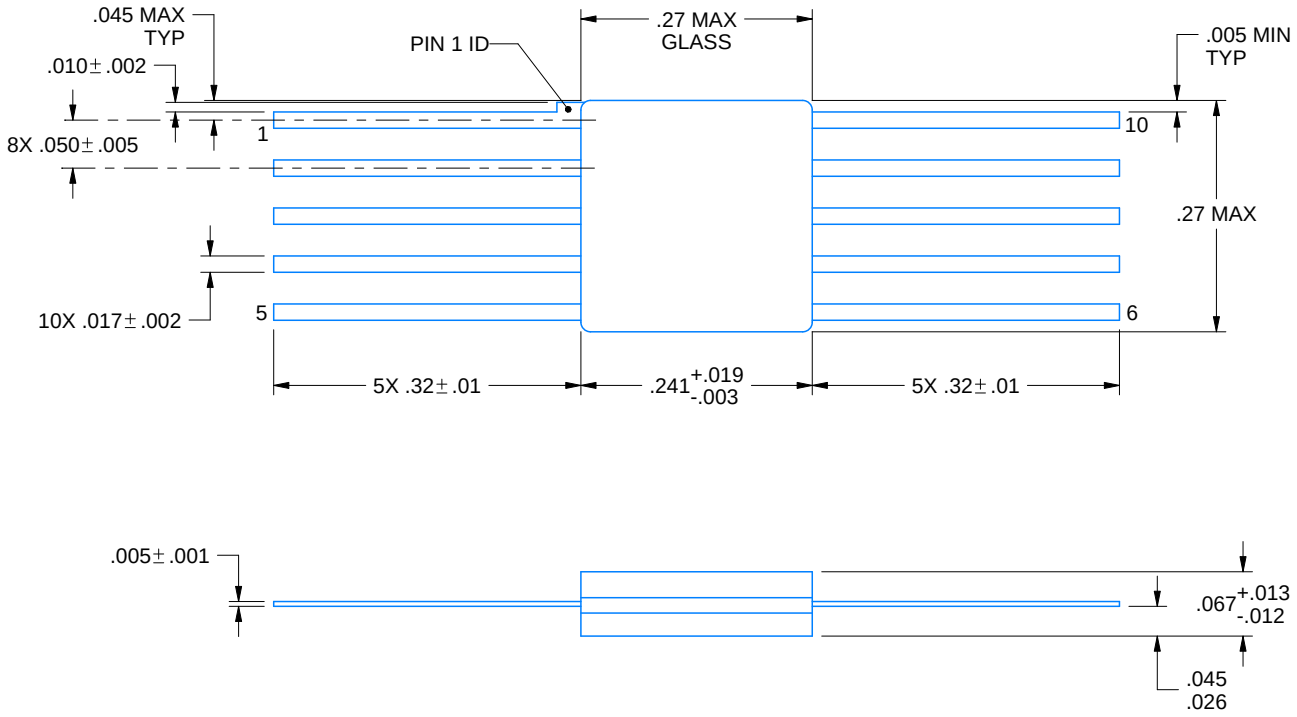
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	2197877	12/30/2021	DAVID CHIN / ANIS FAUZI
B	NO CHANGE TO DRAWING; REVISION FOR YODA RELEASE;	2198820	02/14/2022	K. SINCERBOX
C	CHANGE PIN 1 ID LOCATION ON PIN	2198845	02/18/2022	D. CHIN / K. SINCERBOX
D	.2410± .0030 WAS .2700 +.0012/-.0002;	2200915	08/08/2022	D. CHIN / K. SINCERBOX

NAD0010A

PACKAGE OUTLINE

CFP - 2.03 mm max height

CERAMIC FLATPACK

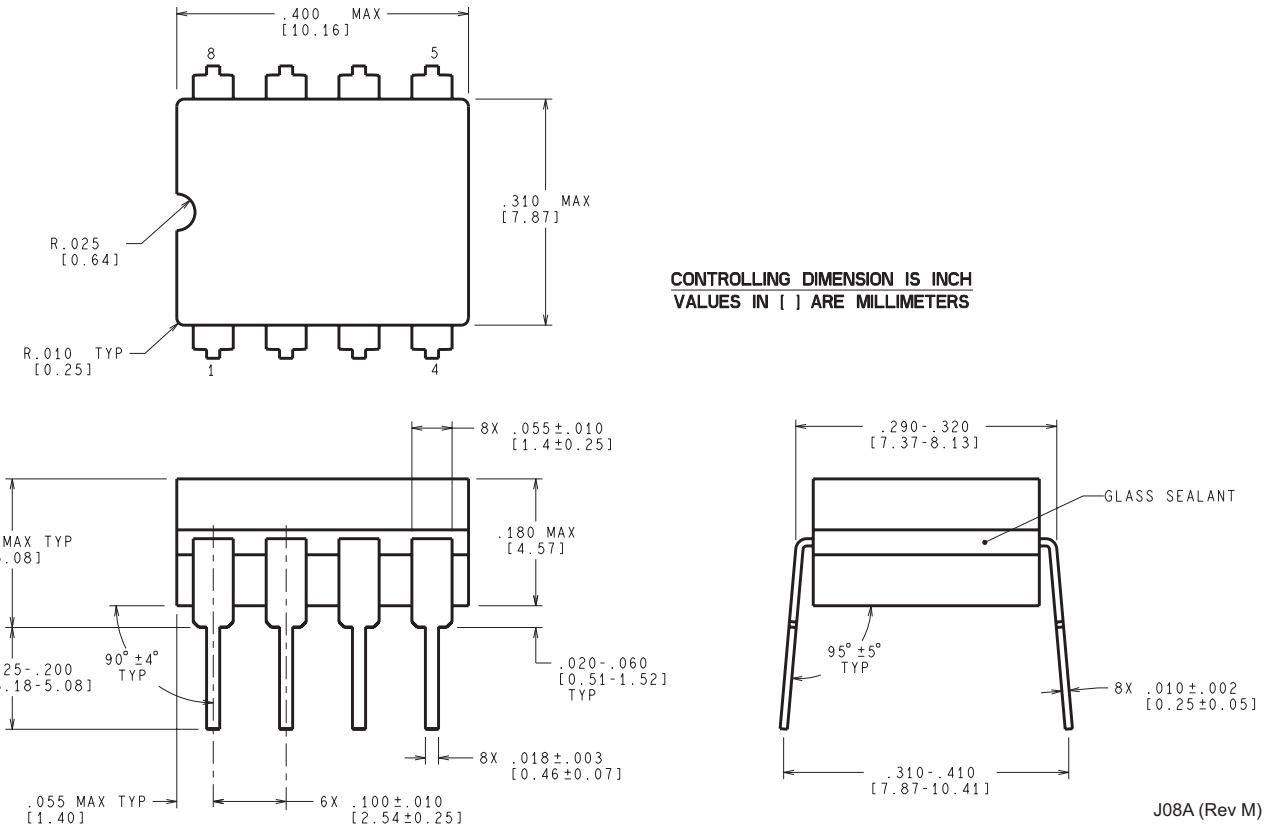


4215191/A 06/2021

NOTES:

1. All linear dimensions are in inches. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

NAB0008A


.400 MAX
[10.16]
8
5
.310 MAX
[7.87]
R.025
[0.64]
R.010 TYP
[0.25]
1
4
CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
8X .055±.010
[1.4±0.25]
.200 MAX TYP
[5.08]
.180 MAX
[4.57]
8X .125-.200
[3.18-5.08]
90° ±4°
TYP
.020-.060
[0.51-1.52]
TYP
8X .018±.003
[0.46±0.07]
.055 MAX TYP
[1.40]
6X .100±.010
[2.54±0.25]
.290-.320
[7.37-8.13]
GLASS SEALANT
95° ±5°
TYP
8X .010±.002
[0.25±0.05]
.310-.410
[7.87-10.41]
J08A (Rev M)

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