LM5171-Q1 Dual Channel Bidirectional Controller

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: –40°C to +125°C ambient operating range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- 85V HV-port and 80V LV-port max ratings
- 1% typical accuracy of bidirectional current regulation
- 1% typical accuracy of channel current monitoring
- I^2C interface for monitoring and diagnosis
- Built-in 3.5V 1% reference voltage
- Integrated 5V 10mA bias supply
- 5A peak half-bridge gate drivers
- Programmable or adaptive dead-time control
- Programmable oscillator frequency up to 1MHz with optional synchronization to external clock
- Independent channel enabling control inputs
- Integrated both current and voltage loop control
- Programmable cycle-by-cycle peak current limit
- Over-temperature shutdown
- HV and LV port overvoltage protection
- Dynamically selectable diode emulation and forced PWM operation modes
- Programmable soft-start timer
- Supports both multiphase and independent channel operations
- Supports urgent shutdown latch

2 Applications

- Automotive dual-battery systems
- Super-cap or battery backup power converter
- Stackable high-power buck or boost applications

3 Description

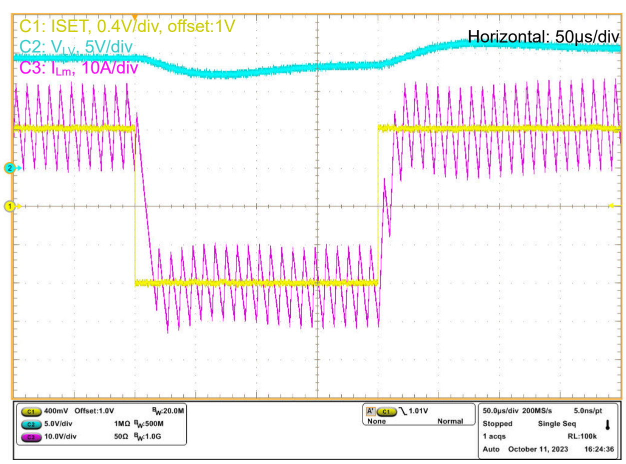
The LM5171-Q1 controller provides the high voltage and precision elements of a dual-channel bidirectional converter, examples include dual battery systems. The LM5171-Q1 supports multiphase parallel operation with balanced current sharing in each phase. The LM5171-Q1 also supports independent channel bi-directional operation making it versatile as standalone controller operating as multiphase buck/ boost or independent buck or boost.

The dual-channel differential current sense amplifiers and dedicated channel current monitors achieve a typical accuracy of 1%. The robust 5A half-bridge gate drivers are capable of driving parallel MOSFETs for more power per channel. Program the controller dynamically to operate in either diode emulation mode (DEM) or forced PWM (FPWM) mode. Versatile protection features include cycle-by-cycle current limiting, overvoltage protection, overtemperature protection and urgent shutdown latch.

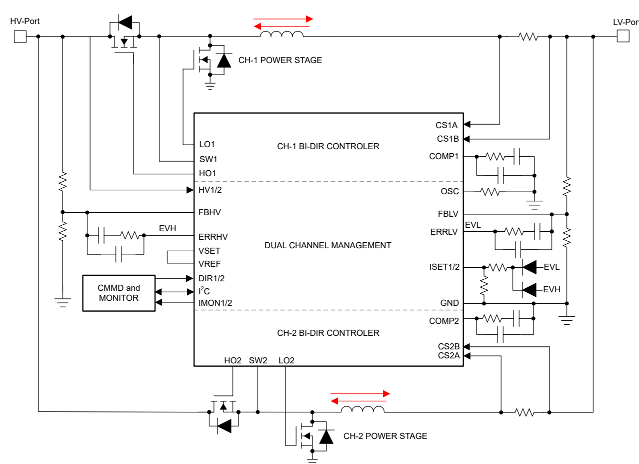
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE (NOM)
LM5171-Q1	TQFP (48)	7mm × 7mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Inductor Current Tracking with Direction Change



Simplified Application Circuit

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4 Pin Configuration and Functions

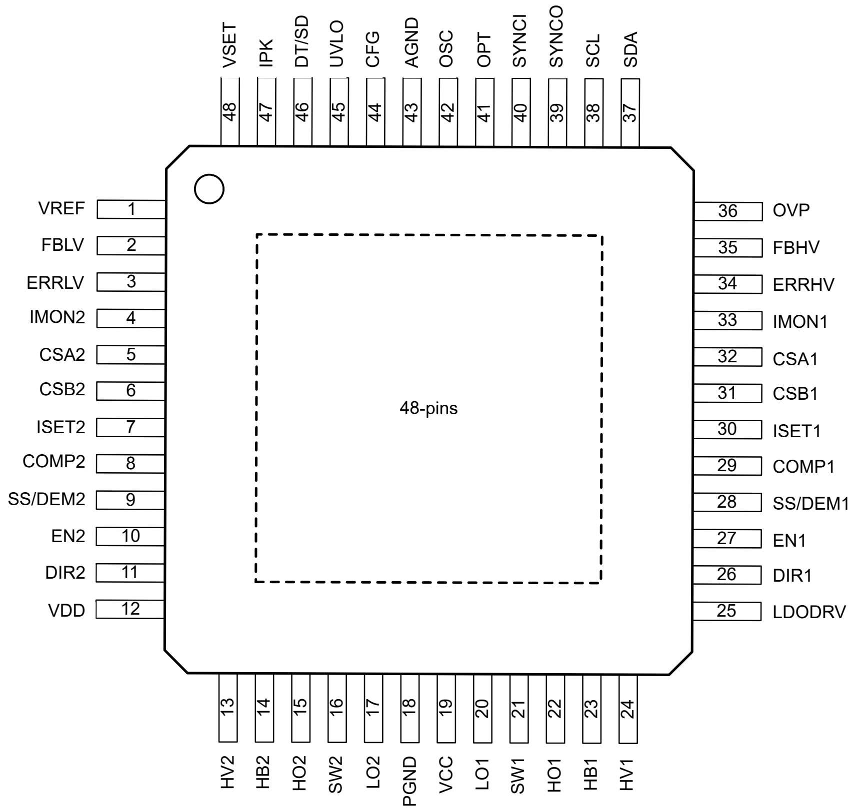


Figure 4-1. LM5171-Q1 PHP Package, 48-Pin TQFP (Top View)

Table 4-1. Pin Functions

PIN		I/O[(1)]	DESCRIPTION
NO.	NAME		
1	VREF	P	Output of the built-in 3.5V +/- 1% reference voltage. Connect a 0.1µF capacitor between the VREF pin and AGND.
2	FBLV	I	Inverting input of the error amplifier for buck mode. This error amplifier is active when DIR1 is high. Short FBLV and ERRLV when this amplifier is not used.
3	ERRLV	O	Output of the error amplifier for buck mode. This error amplifier is active when DIR1 is high. Short FBLV and ERRLV when this amplifier is not used.
4	IMON2	O	CH-2 current monitor pin. A current source flows out of this pin. The current source is proportional to the CH-2 inductor current or CH-2 boost mode output current based on CFG selection. Placing a terminating resistor and filter capacitor from IMON2 to AGND produces a DC voltage representing the CH-2 DC current level. An internal 50µA offset DC current source at the IMON2 pin raises the active signal above the ground noise, thus improving the monitor noise immunity.
5	CSA2	I	CH-2 differential current sense inputs. The CH-2 current sense resistor is placed between these two pins. The CSA2 pin connects to the power inductor and CSB2 pin connects to the LV-Port.
6	CSB2	I	
7	ISET2	I	CH-2 current programming pin. There is 1V offset on ISET2, that is, the CH-2 inductor current is proportional to (ISET2-1V). In DEM, the inductor current is 0 when ISET2 is less than1V. In FPWM, the inductor current reverses when ISET2 is less than 1V.
8	COMP2	O	Output of the CH-2 transconductance (gm) error amplifier and the inverting input of the CH-2 PWM comparator. Connect a loop compensation network to this pin.
9	SS/DEM2	I	ISET2 soft-start pin. The SS/DEM2-pin also sets CH-2 in either DEM or FPWM. An external capacitor sets the ramp rate of the SS/DEM2 pin voltage during soft start. SS/DEM2 overrides ISET2 voltage during soft-start. When an outer voltage loop is used, use 100pF soft-start capacitor. A 60.4kΩ resistor between SS/DEM2 and AGND sets CH-2 to DEM. CH-2 operates in FPWM without the resistor.

Table 4-1. Pin Functions (continued)

PIN NO.	PIN NAME	I/O(1)	DESCRIPTION
10	EN2	I	CH-2 enable pin. Pulling EN2 above 2V turns off the SS/DEM2 pulldown and allows CH-2 to begin a soft-start sequence. Pulling EN2 below 1 V discharges the SS/DEM2 capacitor and holds it low. The high side and low side gate drivers of both channels are held in the low state when SS/DEM2 is discharged.
11	DIR2	I	CH-2 direction command input. Pulling DIR2 pin above 2V sets the converter to buck mode. Pulling DIR2 below 1V sets the converter to the boost mode. If the DIR2 pin is left open, the device detects an invalid command and disables CH-2 with the MOSFET gate drivers in the low state.
12	VDD	P	Output of 5V internal LDO. Connect a 1μF capacitor between the VDD pin and AGND.
13	HV2	I	Connect to HV-Port for CH-2 controller.
14	HB2	I	CH-2 high-side gate driver bootstrap supply. Connect a 0.22μF capacitor between the pin and SW2. Connect a Zener diode between the pin and SW2 to protect the high side driver from overvoltage.
15	HO2	O	CH-2 high-side gate driver output. Connect to the gate of the high-side N-channel MOSFET through a short, low inductance path.
16	SW2	P	CH-2 switching node. Connect directly to the source of the high-side N-channel MOSFET.
17	LO2	O	CH-2 low-side gate driver output. Connect to the gate of the low-side N-channel MOSFET through a short, low inductance path.
18	PGND	G	Power ground connection pin for low-side gate drivers and VCC bias supply.
19	VCC	P	VCC bias supply pin. Connect a 2.2μF capacitor between the VCC pin and AGND.
20	LO1	O	CH-1 low-side gate driver output. Connect to the gate of the low-side N-channel MOSFET through a short, low inductance path.
21	SW1	P	CH-1 switch node. Connect directly to the source of the high-side N-channel MOSFET.
22	HO1	O	CH-1 high-side gate driver output. Connect to the gate of the high-side N-channel MOSFET through a short, low inductance path.
23	HB1	I	CH-1 high-side gate driver bootstrap supply input. Connect a 0.22μF capacitor between the pin and SW1. Connect a Zener diode between the pin and SW1 to protect the high side driver from overvoltage.
24	HV1	I	Connect to the HV-Port for CH-1 controller.
25	LDODRV	O	The LDO MOSFET driver. Connect to the LDO MOSFET gate to get a regulated 9V VCC. Leave this pin open when it is not used.
26	DIR1	I	CH-1 direction command input. Pulling DIR1 pin above 2V sets the converter to buck mode. Pulling DIR1 below 1V sets the converter to the boost mode. If the DIR1 pin is left open, the device detects an invalid command and disables CH-1 with the MOSFET gate drivers in the low state.
27	EN1	I	CH-1 enable pin. Pulling EN1 above 2V turns off the SS1 pulldown and allows CH-1 to begin a soft-start sequence. Pulling EN1 below 1 V discharges the SS1 capacitor and holds it low. The high side and low side gate drivers of both channels are held in the low state when SS1 is discharged.
28	SS/DEM1	I	ISET1 soft-start pin. The SS/DEM1-pin also sets CH-1 in either DEM or FPWM. An external capacitor sets the ramp rate of the SS/DEM1 pin voltage during soft start. SS/DEM1 overrides ISET1 voltage during soft-start. When an outer voltage loop is used, use 100pF soft-start capacitor. A 60.4kΩ resistor between SS/DEM1 and AGND sets CH-1 to DEM. CH-1 operates in FPWM without the resistor.
29	COMP1	O	Output of the CH-1 trans-conductance (gm) error amplifier and the inverting input of the CH-1 PWM comparator. Connect a loop compensation network to this pin.
30	ISET1	I	CH-1 current programming pin. There is 1V offset on ISET1, that is, the CH-1 inductor current is proportional to (ISET1-1V). In DEM, the inductor current is 0 when ISET1 is less than1V. In FPWM, the inductor current reverses when ISET1 is less than 1V.
31	CSB1	I	CH-1 differential current sense inputs. The CH-1 current sense resistor is placed between these two pins. The CSA1 pin connects to the power inductor and CSB1 pin connects to the LV-Port.
32	CSA1	I	
33	IMON1	O	CH-1 current monitor pin. A current source flows out of this pin. The current source is proportional to the CH-1 inductor current or CH-1 boost mode output current based on CFG selection. Placing a terminating resistor and filter capacitor from IMON1 to AGND produces a DC voltage representing the CH-1 DC current level. An internal 50μA offset DC current source at the IMON1 pin raises the active signal above the ground noise, thus improving the monitor noise immunity.
34	ERRHV	O	Output of the error amplifier for boost mode. This error amplifier is active when DIR1 is low.
35	FBHV	I	Inverting input of the error amplifier for boost mode. This error amplifier is active when DIR1 is low.

Table 4-1. Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
36	OVP	I	The inverting input of internal overvoltage comparator. When the OVP pin voltage rises above 1V, the SS/DEM1 and VSET capacitors are discharged and held low until the OVP pin drops to 0.9V.
37	SDA	I/O	Data of I^2C interface. Pull to VDD through a 10kΩ resistor if SDA is not used.
38	SCL	I	Clock of I^2C interface. Pull to VDD through a 10kΩ resistor if SCL is not used.
39	SYNCO	O	Clock synchronization output pin. Connect SYNCO to the downstream device SYNCI for 3-phase or 4-phase configuration. Leave this pin open when it is not used.
40	SYNCI	I	Input for an external clock that overrides the free-running internal oscillator. Connect the SYNCI pin to ground when not used. Ground the SYNCI pin or leave it open when it is not used.
41	OPT	I	Multiphase configuration pin. Tie OPT pin to VDD for 4-phase operation. Tie OPT pin to AGND for 3-phase operation.
42	OSC	I	The internal oscillator frequency is programmed by a resistor between OSC and AGND.
43	AGND	G	Analog ground reference. Connect AGND to PGND externally through a single point connection to improve the noise immunity.
44	CFG	I	The I^2C address and IMON function selection pin.
45	UVLO	I	The UVLO pin serves as the primary enable pin. When UVLO is pulled below 1.25 V, the device is in a low quiescent current shutdown mode. When UVLO is pulled above 1.25 V but below 2.5 V, the device enters the initialization mode. LDODRV is turned on to control the external MOSFET to produce the VCC. The VDD and VREF are also established. When UVLO is pulled above the 2.5 V, the device is ready to operate.
46	DT/SD	I	Dead-time programming and emergent latched shutdown pin. A resistor connected between DT/SD and AGND sets the dead time between the high-side and low-side driver outputs. Tie the DT pin to VDD to activate the internal adaptive dead time control. When DT/SD pin is pulled low, the device enters latched shutdown.
47	IPK	I	Peak current limit programming pin. IPK voltage sets the threshold for the cycle-by-cycle current limit comparator. Use a resistor divider from VREF to set IPK voltage.
48	VSET	I	Voltage error amplifier reference input pin. The VSET pin is pulled low when the device is shutdown, EN1 is low or DIR1 flips. Use a resistor divider from VREF to set VSET pin voltage. Connect a capacitor to VSET for voltage loop soft-start.
—	EP	—	Exposed pad of the package. Solder to the large ground plane to reduce thermal resistance.

(1) Note: G = Ground, I = Input, O = Output, P = Power

5 Specifications

5.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range(1)

		MIN	MAX	UNIT
Input	HV1, HV2 to AGND	–0.3	85	V
	HV1, HV2 to AGND (50ns Transient)		90	
	SW1, SW2 to PGND	-5	85	
	SW1, SW2 to PGND (20ns Transient)		90	
	SW1, SW2 to PGND (50ns Transient)	-16		
	HB1 to SW1, HB2 to SW2	–0.3	14	
	HO1 to SW1, HO2 to SW2	–0.3	HB+0.3	
	HO1 to SW1, HO2 to SW2 (20ns Transient)	–2		
	LO1, LO2 to PGND	-0.3	VCC+0.3	
	LO1, LO2 to PGND (20ns Transient)	-2		
	CSA1, CSB1,CSA2,CSB2 to PGND	-0.3	80	
	CSA1 to CSB1, CSA2 to CSB2	-0.3	0.3	
	CFG, DIR1, DIR2, EN1, EN2, FBHV, FBLV, IPK, ISET1, ISET2, OPT, OVP, SCL, SDA, SYNCI, UVLO, VDD, VSET to AGND	-0.3	5.5	
	COMP1, COMP2, DT/SD, ERRHV, ERRLV, IMON1, IMON2, OSC, SS/DEM1, SS/DEM2, SYNCO, VREF to AGND	-0.3	VDD+0.3	
	LDODRV TO VCC	-0.3	5	
	VCC to PGND	-0.3	14	
	PGND to AGND	–0.3	0.3	
Junction temperature, T_J (2)		–40	150	°C
Storage temperature, T_{stg}		–55	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) HBM ESD Classification		±2000	V
		Charged device model (CDM) per V ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	
			Corner pins (1,12,13,24,25,36,37,48)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.

5.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise specified)[(1)]

		MIN	NOM	MAX	UNIT
HV-Port (HV1, HV2)	Buck Mode	3		80	V
HV-Port (HV1, HV2)	Boost Mode	3		80	V
LV-Port	Buck Mode	0		75	V
LV-Port	Boost Mode	1		75	V
VCC	Applicable External Voltage to VCC Pin	9.5		12	V
T_J	Operating Junction Temperature[(2)]	–40		150	°C
F_{OSC}	Oscillator Frequency	50		1000	kHz
F_{EX_CLK}	Synchronization to External Clock Frequency (Minimal 50kHz)	0.8x F_{OSC}		1.2x F_{OSC}	kHz
F_{EX_CLK}	SYNCI Pulse	50		0.8/ F_{OSC}	ns
t_{DT}	Programmable Dead Time Range	15		200	ns

(1) *Operating Ratings* are conditions under the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics*.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

5.4 Thermal Information

THERMAL METRIC[(1)]		LM5171 PHP (TQFP) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	13.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 150°C. Unless otherwise stated, F_{OSC} = 100 kHz; V_{VCC} = 10 V; V_{HV1} = V_{HV2} = $V_{HV\text{-}Port}$ = 48V and $V_{LV\text{-}Port}$ = 12 V.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
HV Port (HV1, HV2)						
$I_{SHUTDOWN1}$	HV1 pin current in shutdown mode	V_{UVLO} = 0V			10	µA
$I_{SHUTDOWN2}$	HV2 pin current in shutdown mode	V_{UVLO} = 0V			10	µA
$I_{OPERATING}$	HV1 and HV2 pin current in operating	V_{UVLO} > 2.6V, V_{VCC} > 9V		1		mA
VCC Bias Supply (VCC)						
V_{VCC_reg}	VCC LDO regulation setting point	V_{HV1} > 10V	8.55	9	9.45	V
V_{CCUVLO}	VCC undervoltage detection	VCC falling	7.7	8	8.2	V
V_{CCHYS}	VCC UVLO hysteresis	VCC rising	8.2	8.5	8.7	V
I_{VCC_SD}	VCC sink current in shutdown mode	V_{UVLO} = 0V, V_{VCC}=10V			25	µA
I_{VCC_SB}	VCC sink current in standby: no switching	V_{UVLO} > 2.6V, V_{VCC} > 9V, EN1=EN2=0V			10	mA
VDD Analog Bias Supply (VDD)						

5.5 Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 150°C. Unless otherwise stated, F_{OSC} = 100 kHz; V_{VCC} = 10 V; V_{HV1} = V_{HV2} = $V_{HV\text{-}Port}$ = 48V and $V_{LV\text{-}Port}$ = 12 V.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VDD}	VDD voltage	V_{UVLO} > 2.6V, V_{VCC} > 9V	4.75	5	5.25	V
V_{DDUV}	VDD undervoltage detection	VDD falling	4.25	4.5	4.75	V
V_{DDHYS}	VDD UVLO hysteresis	VDD rising above V_{DDUV}	0.1	0.2	0.3	V
I_{VDD}	VDD source current limit	V_{VDD} = 4.6V	10			mA
VOLTAGE REFERENCE (VREF)						
V_{REF}	Voltage reference	V_{UVLO} > 2.6V, V_{VCC} > 9V, V_{VDD} > V_{DDUV}	3.465	3.500	3.535	V
I_{VREF}	VREF source current limit	V_{VREF} = 3.5V	2			mA
Primary ON/OFF Control (UVLO)						
V_{UVLO_TH}	UVLO release threshold	UVLO voltage rising	2.4	2.5	2.6	V
I_{HYS}	UVLO hysteresis current	UVLO source current when V_{UVLO} > 2.6V	21	25	29	µA
V_{RES}	UVLO shutdown and IC reset voltage threshold	UVLO voltage falling	1	1.25	1.5	V
	UVLO shutdown release	UVLO voltage rising above V_{RES}	0.15	0.25	0.35	V
t_{UVLO}	UVLO 2.5V threshold glitch filter	UVLO voltage both rising and falling		2.5		µs
t_{VRES}	UVLO 1.25V V_{RES} threshold glitch filter			5	10	µs
	UVLO internal pull-down current		25	100	250	nA
Enable Inputs EN1 and EN2						
V_{IL}	Enable input low state	The driver outputs disabled			1.0	V
V_{IH}	Enable input high state	The driver outputs enabled	2.0			V
	Internal pulldown impedance	EN1, EN2 logic inputs internal pulldown resistor	0.7	1	1.3	MegΩ
	EN glitch filter time (the rising and falling edges)			2.5		µs
DIRECTION COMMANDS (DIR1, DIR2)						
V_{DIR1}, V_{DIR2}	Command for current flowing from LV-Port to HV-Port (boost mode 12 V to 48 V), for CH-1 and CH-2, respectively	Actively pulled low by external circuit			1	V
V_{DIR1}, V_{DIR2}	Command for current flowing from HV-Port to LV-Port (buck mode 48 V to 12 V), for CH-1 and CH-2, respectively	Actively pulled high by external circuit	2			V
V_{DIR1}, V_{DIR2}	Standby (invalid DIR command)	DIR pin (DIR1 or DIR2) neither active High nor active Low		1.5		V
	DIR glitch filter (the rising and falling edges)	Both Rising and Falling Edges		10		µs
ISET INPUTS (ISET1, ISET2)						
	ISET DC Offset Voltage		0.87	1.0	1.13	V
G_{ISET}	Gain of the regulated inductor DC current sense voltage to ISET voltage	$\|V_{CSA} – V_{CSB}\|$ = 50mV	24.3	25	25.7	mV/V
	ISET internal pull-down current sink			75	200	nA
Output Current Monitor (IMON1, IMON2)						
	Gain of IMON1 and IMON2 current source versus channel current sense voltage	|CSA-CSB| = 50mV, CONFIG = 'IMON_IL monitor", V_{DIR} > 2V	1.96	2	2.04	µA/mV

5.5 Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 150°C. Unless otherwise stated, F_{OSC} = 100 kHz; V_{VCC} = 10 V; V_{HV1} = V_{HV2} = $V_{HV\text{-}Port}$ = 48V and $V_{LV\text{-}Port}$ = 12 V.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Gain of IMON1 and IMON2 current source versus channel current sense voltage	|CSA-CSB| = 50mV, CONFIG = 'IMON_IL monitor", V_{DIR} < 1V	1.96	2	2.04	uA/mV
	Gain of IMON1 and IMON2 current source versus channel current sense voltage	|CSA-CSB| = 50mV, CONFIG = 'IMON_BSTOUT monitor", V_{DIR} < 1V, Duty cycle = 0.75	0.475	0.5	0.525	uA/mV
	Gain of IMON1 and IMON2 current source versus channel current sense voltage	|CSA-CSB| = 10mV, CONFIG = "IMON_IL monitor", V_{DIR} > 2V	1.96	2	2.04	uA/mV
	Gain of IMON1 and IMON2 current source versus channel current sense voltage	|CSA-CSB| = 10mV, CONFIG = 'IMON_IL monitor", V_{DIR} < 1V	1.96	2	2.04	uA/mV
	Gain of IMON1 and IMON2 current source versus channel current sense voltage	|CSA-CSB| = 10mV, CONFIG = 'IMON_BSTOUT monitor", V_{DIR} < 1V, Duty cycle = 0.75	0.475	0.5	0.525	uA/mV
	IMON1 and IMON2 DC offset current	|CSA-CSB| = 0mV	42	50	56	µA
CURRENT SENSE AMPLIFIER (BOTH CHANNELS)						
G_{CS_BK1}	Gain of amplifier output to current sense voltage in buck mode	$\|V_{CSA} – V_{CSB}\|$ = 50mV, V_{DIR} > 2V	39	40	41	V/V
G_{CS_BST1}	Gain of amplifier output to current sense voltage in boost mode	$\|V_{CSA} – V_{CSB}\|$ = 50mV, V_{DIR} < 1V	39	40	41	V/V
G_{CS_BK2}	Gain of amplifier output to current sense voltage in buck mode	$\|V_{CSA} – V_{CSB}\|$ = 10mV, V_{DIR} > 2V	38.4	40	41.7	V/V
G_{CS_BST2}	Gain of amplifier output to current sense voltage in boost mode	$\|V_{CSA} – V_{CSB}\|$ = 10mV, V_{DIR} < 1V	38.4	40	41.7	V/V
TRANSCONDUCTION AMPLIFIER (COMP1, COMP2)						
Gm	Transconductance		75	100	125	µA/V
I_{COMP}	Output source current limit	V_{ISET} = 4V, $\|V_{CSA} – V_{CSB}\|$ = 0mV	190	250	280	µA
I_{COMP}	Output sink current limit	V_{ISET} = 0V, $V_{CSA} – V_{CSB}$ = 50mV in the buck mode, or $V_{CSA} – V_{CSB}$ = -50mV in the boost mode	–280	–250	–190	µA
VOLTAGE LOOP ERROR AMPLIFIERS (VSET, LVFB, LVERR, HVFB, HVERR)						
A_{OL}	Open loop gain	V_{VCC} > 9 V, V_{VDD} > V_{DDUV}		80		dB
F_{BW}	Unity gain bandwidth			2.1		MHz
V_{OS}	Input offset voltage			0	5	mV
V_{ERR_MIN}	Minimum amplifier output voltage	Sourcing 2mA	4			V
V_{ERR_MAX}	Maximum amplifier output voltage	Sinking 2mA			0.5	V
PWM Comparator						
	COMP to output delay			50		ns
	COMP to PWM comparator offset			1		V
T_{OFF_MIN}	Minimum off time			100	150	ns
PEAK CURRENT LIMIT (IPK)						
G_{IPK_BK1}	Gain from current sense voltage to cycle-by-cycle limit threshold voltage given at IPK pin, in buck mode	V_{IPK} = 3V, V_{DIR} >2V	45	50	55	mV/V
G_{IPK_BK2}	Gain from current sense voltage to cycle-by-cycle limit threshold voltage given at IPK pin, in buck mode	V_{IPK} = 1V, V_{DIR} >2V	45	50	55	mV/V

5.5 Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 150°C. Unless otherwise stated, F_{OSC} = 100 kHz; V_{VCC} = 10 V; V_{HV1} = V_{HV2} = $V_{HV\text{-}Port}$ = 48V and $V_{LV\text{-}Port}$ = 12 V.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
G_{IPK_BST1}	Gain from current sense voltage to cycle-by-cycle limit threshold voltage given at IPK pin, in boost mode	V_{IPK} = 3V, V_{DIR} <1V	45	50	55	mV/V
G_{IPK_BST2}	Gain from current sense voltage to cycle-by-cycle limit threshold voltage given at IPK pin, in boost mode	V_{IPK} = 1V, V_{DIR} <1V	45	50	55	mV/V
OVERVOLTAGE PROTECTION (OVP)						
	OVP threshold		0.99	1	1.01	V
OVP_{HYS}	OVP Hysteresis			100		mV
t_{OVP}	OVP Glitch Filter			5		us
OSCILLATOR (OSC)						
F_{OSC}	Oscillator frequency 1	R_{OSC} = 41.5kΩ, no external clock signal at SYNCI pin	90	100	110	kHz
	Oscillator frequency 2	R_{OSC} = 4.15kΩ, no external clock signal at SYNCI pin	900	1000	1100	kHz
V_{OSC}	OSC pin DC voltage	OSC DC Level		1		V
SYNCHRONIZATION CLOCK INPUT (SYNCI)						
V_{SYNIH}	SYNCI input threshold for high state		2			V
V_{SYNIL}	SYNCI input threshold for low state				1	V
	Delay to establish synchronization	0.8 x F_{OSC} < F_{SYNCI} < 1.2 x Fosc		200	300	us
	Internal pull-down impedance	V_{SYNCI} = 2.5V	700	1000	1300	kΩ
SYNCHRONIZATION CLOCK OUTPUT (SYNCO)						
V_{SYNOH}	SYNCO high state		2.5			V
V_{SYNOL}	SYNCO low state				0.4	V
	Sourcing current when SYNCO in high state	V_{SYNCO} = 2.5V		1		mA
	Sinking current when SYNCO in low state	V_{SYNCO} = 0.5V		1		mA
	SYNCO pulse width		60	90	120	ns
	SYNCO pulse delay for multiphase daisy chain connection	V_{OPT} > 2V, R_{SYNCO} > 61.9kΩ		90		Degree
		V_{OPT} < 1V, R_{SYNCO} > 61.9kΩ		120		Degree
BOOTSTRAP (HB1, HB2)						
$V_{HB\text{-}UV}$	Bootstrap undervoltage threshold	(V_{HB} – V_{SW}) voltage rising	6	6.5	7	V
$V_{HB\text{-}UV\text{-}HYS}$	Bootstrap undervoltage hysteresis			0.5		V
I_{HB_LK}	Bootstrap quiescent current	V_{HB} – V_{SW} = 10V, V_{HO} – V_{SW} = 0V			100	µA
HIGH SIDE GATE DRIVERS (HO1, HO2)						
V_{OLH}	HO low-state output voltage	I_{HO} = 100mA		0.1		V
V_{OHH}	HO high-state output voltage	I_{HO} = -100mA, V_{OHH} = V_{HB} - V_{HO}		0.15		V
	HO rise time (10% to 90% pulse magnitude)	C_{LD} = 1000pF		5		ns
	HO fall time (90% to 10% pulse magnitude	C_{LD} = 1000pF		4		ns
I_{OHH}	HO peak source current	V_{HB} – V_{SW} = 10V		4		A
I_{OLH}	HO peak sink current	V_{HB} – V_{SW} = 10V		5		A
LOW SIDE GATE DRIVERS (LO1, LO2)						
V_{OLL}	LO low-state output voltage	I_{LO} = 100mA		0.1		V

5.5 Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 150°C. Unless otherwise stated, F_{OSC} = 100 kHz; V_{VCC} = 10 V; V_{HV1} = V_{HV2} = $V_{HV\text{-}Port}$ = 48V and $V_{LV\text{-}Port}$ = 12 V.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OHL}	LO high-state output voltage	I_{LO} = -100mA, V_{OHL} = V_{VCC} - V_{LO}		0.15		V
	LO rise time (10% to 90% pulse magnitude)	C_{LD} = 1000pF		5		ns
	LO fall time (90% to 10% pulse magnitude)	C_{LD} = 1000pF		4		ns
I_{OHL}	LO peak source current	V_{VCC} = 10V		4		A
I_{OLL}	LO peak sink current	V_{VCC} = 10V		5		A
INTERLEAVE PHASE DELAY FROM CH-2 To CH-1 (OPT)						
V_{OPTL}	OPT Input Low State	OPT="0"			1.0	V
V_{OPTH}	OPT Input High State	OPT="1"	2.0			V
	$HO2_{rising}$ -$HO1_{rising}$ in the buck mode, or $LO2_{rising}$ -$LO1_{rising}$ in the boost mode	OPT = "0" for 3 Phases in Daisy Chain Interleaving Operation		240		Degree
	$HO2_{rising}$ -$HO1_{rising}$ in the buck mode, or $LO2_{rising}$ -$LO1_{rising}$ in the boost mode	OPT= "1" for 1, 2, or 4 phases in Daisy Chain Interleaving Operation		180		Degree
	Internal Pull down impedance			1		MegΩ
DEAD TIME and LATCHED SHUTDOWN (DT/SD)						
t_{DT}	LO falling edge to HO rising edge delay	R_{DT} = 19.1kΩ	35	50	60	ns
	HO falling edge to LO rising edge delay	R_{DT} = 19.1kΩ	35	50	65	ns
V_{DT}	DC voltage level for dead time programming			1.2		V
	DC voltage level for adaptive dead time programming		3.1			V
V_{ADPT}	HO-SW or LO-GND voltage threshold to enable cross output for adaptive dead time scheme	V_{VCC} > 9V, (V_{HB} – V_{SW}) > 8V, HO or LO voltage falling		1.5		V
t_{ADPT}	LO falling edge to HO rising edge delay	V_{DT} = V_{VDD}	28	40	75	ns
	HO falling edge to LO rising edge delay	V_{DT} = V_{VDD}	30	40	75	ns
t_{SD}	Latched shutdown glitch filter		1.875	2.5	3.125	µs
R_{SD}	Shutdown latch pulldown resistance	Resistor in series with an external pull-down NFET			2	kΩ
SOFT START and FORCED PWM and DIODE EMULATION PRGRAMMING (SS/DEM1, SS/DEM2)						
I_{SS}	SS charging current source during startup	V_{SS} ≤ 3.3V, V_{EN} > 2V, V_{UVLO} > 2.5V, DIR < 1 or DIR > 2	63	70	77	µA
I_{SS}	SS charging current source after startup	V_{SS} ≥ 3.9V, V_{EN} > 2V, V_{UVLO} > 2.5V, DIR < 1 or DIR > 2	45	50	55	µA
	SS to gm input offset		0.8	1	1.3	V
R_{SS}	SS discharge device Rds(ON)	V_{SS} = 2V	5	20	30	Ω
V_{SS_LOW}	SS discharge completion threshold	Once it is discharged by internal logic	0.15	0.3	0.35	V
CONFIGURATIONS (CFG)						
R_{CFG1}	I2C Address: b0100000. IMON = IMON_IL			0		kΩ
R_{CFG2}	I2C Address: b0100001. IMON = IMON_IL		0.316		0.324	kΩ

5.5 Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 150°C. Unless otherwise stated, F_{OSC} = 100 kHz; V_{VCC} = 10 V; V_{HV1} = V_{HV2} = $V_{HV\text{-}Port}$ = 48V and $V_{LV\text{-}Port}$ = 12 V.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{CFG3}	I2C Address: b0100010. IMON = IMON_IL		0.649		0.665	kΩ
R_{CFG4}	I2C Address: b0100011. IMON = IMON_IL		1.1		1.13	kΩ
R_{CFG5}	I2C Address: b0100100. IMON = IMON_IL		1.65		1.69	kΩ
R_{CFG6}	I2C Address: b0100101. IMON = IMON_IL		2.43		2.49	kΩ
R_{CFG7}	I2C Address: b0100110. IMON = IMON_IL		3.32		3.4	kΩ
R_{CFG8}	I2C Address: b0100111. IMON = IMON_IL		4.53		4.64	kΩ
R_{CFG9}	I2C Address: b0100111. IMON = IMON_BSTOUT		6.65		6.81	kΩ
R_{CFG10}	I2C Address: b0100110. IMON = IMON_BSTOUT		10.2		10.5	kΩ
R_{CFG11}	I2C Address: b0100101. IMON = IMON_BSTOUT		13.7		14.0	kΩ
R_{CFG12}	I2C Address: b0100100. IMON = IMON_BSTOUT		18.7		19.1	kΩ
R_{CFG13}	I2C Address: b0100011. IMON = IMON_BSTOUT		26.1		26.7	kΩ
R_{CFG14}	I2C Address: b0100010. IMON = IMON_BSTOUT		37.4		38.3	kΩ
R_{CFG15}	I2C Address: b0100001. IMON = IMON_BSTOUT		60.4		61.9	kΩ
R_{CFG16}	I2C Address: b0100000. IMON = IMON_BSTOUT		95.3		97.6	kΩ
I2C INTERFACE (SLC, SDA)						
V_{SDAL}	SDA input low state				1.0	V
V_{SDAH}	SDA input high state		2.0			V
V_{SCLL}	SCL input low state				1.0	V
V_{SCLH}	SCL input high state		2.0			V
Thermal Shutdown						
T_{J_SD}	Thermal shutdown		155	175		℃
	Thermal shutdown hysteresis			15		℃

5.6 Timing Requirements

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
I²C INTERFACE						
f_{SCL}	SCL clock frequency	Standard mode	0		100	kHz
		Fast mode	0		400	kHz
		Fast mode plus (1)	0		1000	kHz
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7			µs
		Fast mode	1.3			µs
		Fast mode plus (1)	0.5			µs

5.6 Timing Requirements (continued)

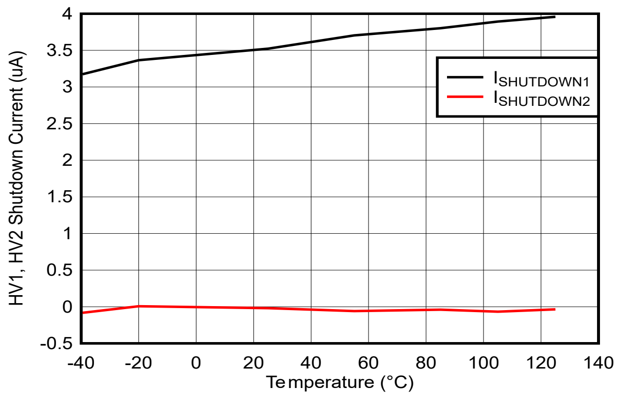
Over operating junction temperature range and recommended supply voltage range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus (1)	0.26			
t_{BUF}	Bus free time between a STOP and a START condition	Standard mode	4.7			µs
		Fast mode	1.3			
		Fast mode plus (1)	0.5			
$t_{SU:STA}$	Set-up time for a repeated START condition	Standard mode	4.7			µs
		Fast mode	0.6			
		Fast mode plus (1)	0.26			
$t_{HD:STA}$	Hold time (repeated) START condition	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus (1)	0.26			
$t_{HD:DAT}$	Data hold time	Standard mode	0			µs
		Fast mode	0			
		Fast mode plus (1)	0			
t_r	Rise time of both SDA and SCL signals	Standard mode			1000	ns
		Fast mode	20		300	
		Fast mode plus (1)			20	
t_f	Fall time of both SDA and SCL signals	Standard mode			300	ns
		Fast mode	$20\times V_{DD}/5.5$		300	
		Fast mode plus (1)	$20\times V_{DD}/5.5$		120	
$t_{su:STO}$	Set-up time for STOP condition	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus (1)	0.26			
$t_{VD;DAT}$	Data valid time	Standard mode			3.45	µs
		Fast mode			0.9	
		Fast mode plus (1)			0.45	
$t_{VD;ACK}$	Data valid acknowledge time	Standard mode			3.45	µs
		Fast mode			0.9	
		Fast mode plus (1)			0.45	
C_b	Capacitive load for each bus line	Standard mode			400	pF
		Fast mode			400	

(1) Fast mode plus is supported but not fully compliant with I^2C standard

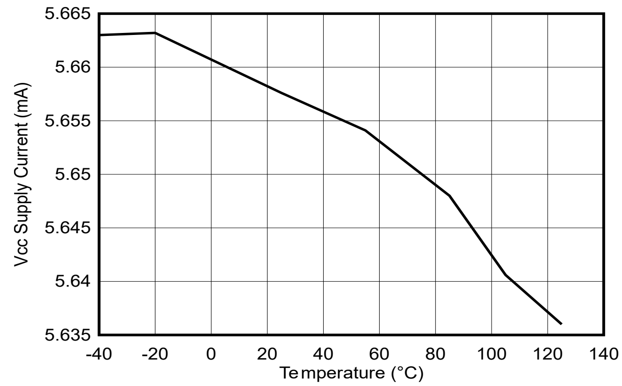
5.7 Typical Characteristics

V_{VIN} = 48V, V_{VCC} = 10V, V_{UVLO} = 3.3V, T_J = 25°C, unless otherwise stated.



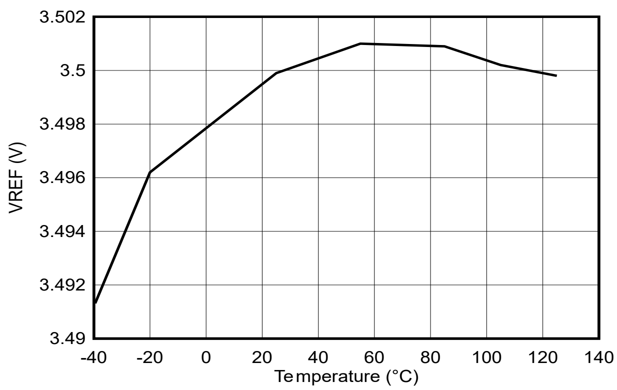
V_{UVLO} = 0

Figure 5-1. Shutdown Current vs Temperature



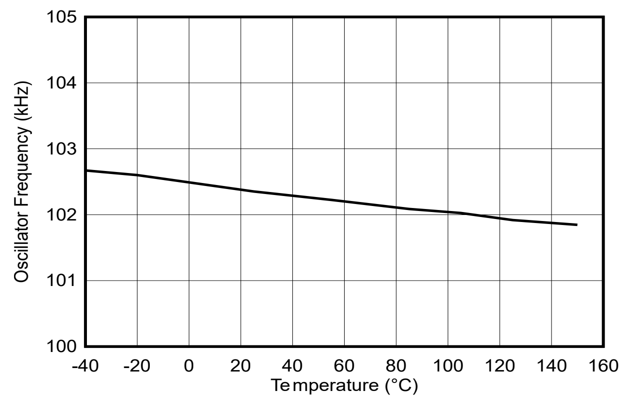
V_{UVLO} = 3V V_{EN1} = 0V,V_{EN2} = 0V

Figure 5-2. VCC Current vs Temperature



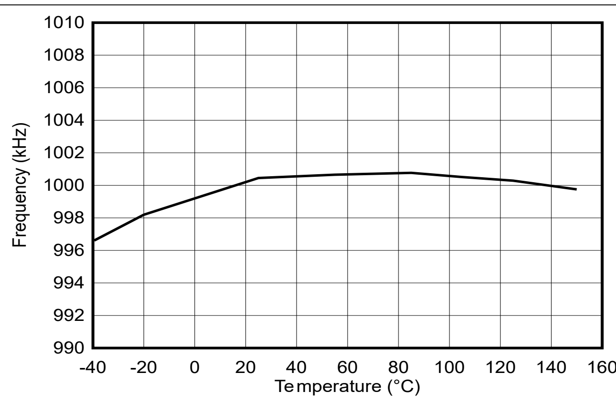
V_{UVLO} = 3V V_{EN1} = 0V,V_{EN2} = 0V

Figure 5-3. VREF Accuracy vs Temperature



R_{OSC} = 40.2kΩ

Figure 5-4. Oscillator Frequency vs Temperature



R_{OSC} = 4.15kΩ

Figure 5-5. Oscillator Frequency vs Temperature

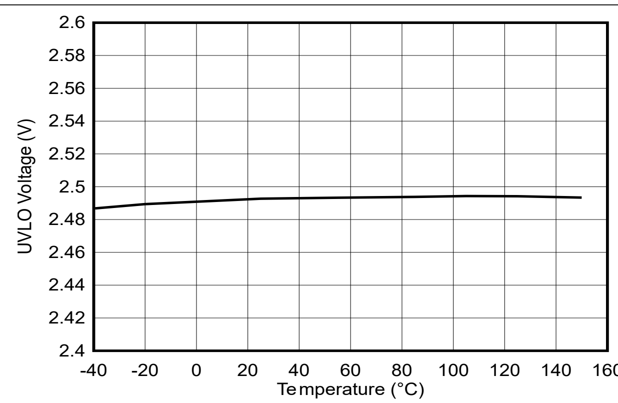


Figure 5-6. UVLO threshold (V_{UVLO_TH}) vs Temperature

5.7 Typical Characteristics (continued)

V_{VIN} = 48V, V_{VCC} = 10V, V_{UVLO} = 3.3V, T_J = 25°C, unless otherwise stated.

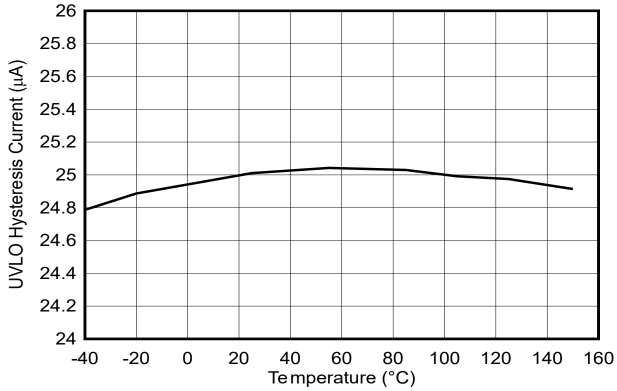


Figure 5-7. UVLO Hysteresis Current (I_{HYS}) vs Temperature

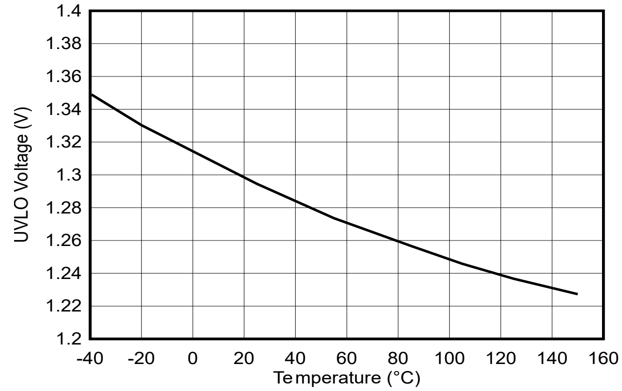


Figure 5-8. UVLO Shutdown Voltage (V_{RES}) vs Temperature

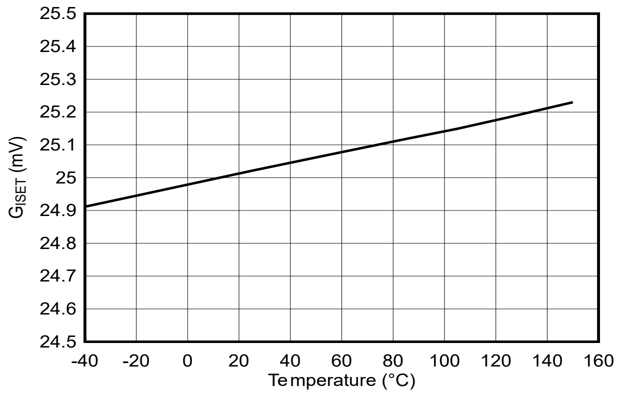


Figure 5-9. Sense Voltage Gain (G_{ISET}) vs Temperature

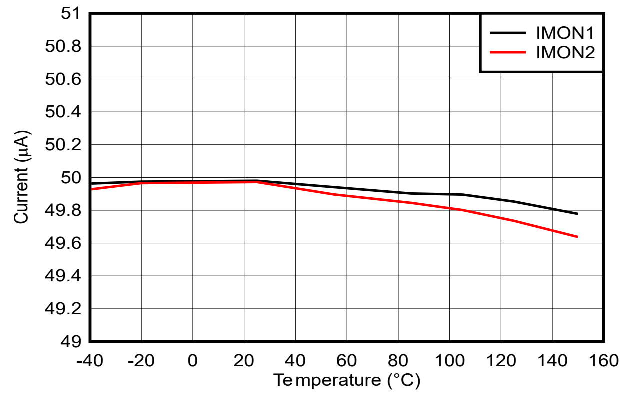


Figure 5-10. IMON Offset Current vs Temperature

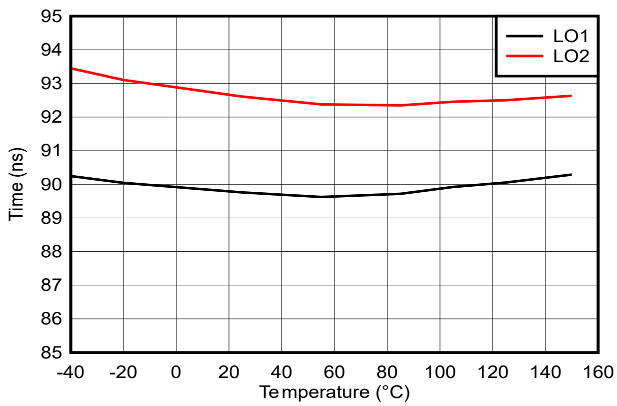
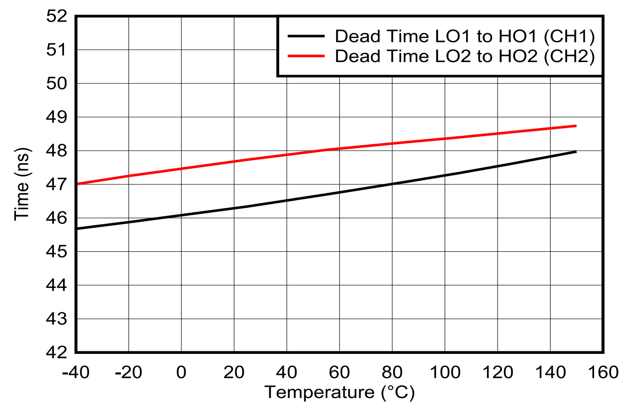


Figure 5-11. Minimum Off Time (T_{OFF_MIN}) vs Temperature

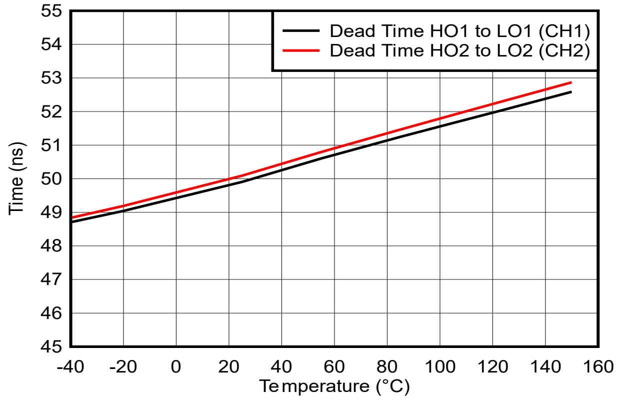


R_{DT} = 19.1kΩ LO falling to HO rising.

Figure 5-12. Dead Time (t_{DT}) vs Temperature

5.7 Typical Characteristics (continued)

V_{VIN} = 48V, V_{VCC} = 10V, V_{UVLO} = 3.3V, T_J = 25°C, unless otherwise stated.



R_{DT} = 19.1kΩ HO rising to LO falling.

Figure 5-13. Dead Time (t_{DT}) vs Temperature

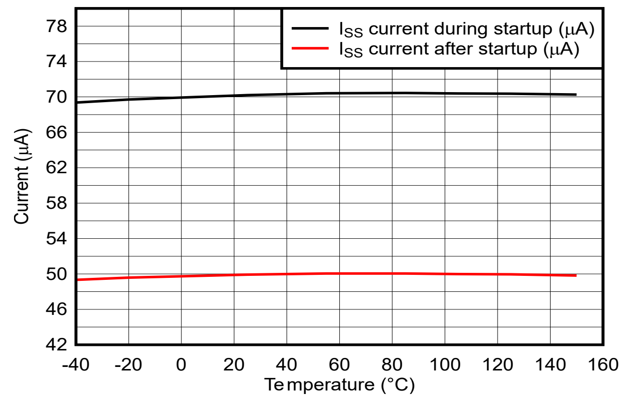


Figure 5-14. Soft-Start Current (I_{SS}) vs Temperature

6 Detailed Description

6.1 Overview

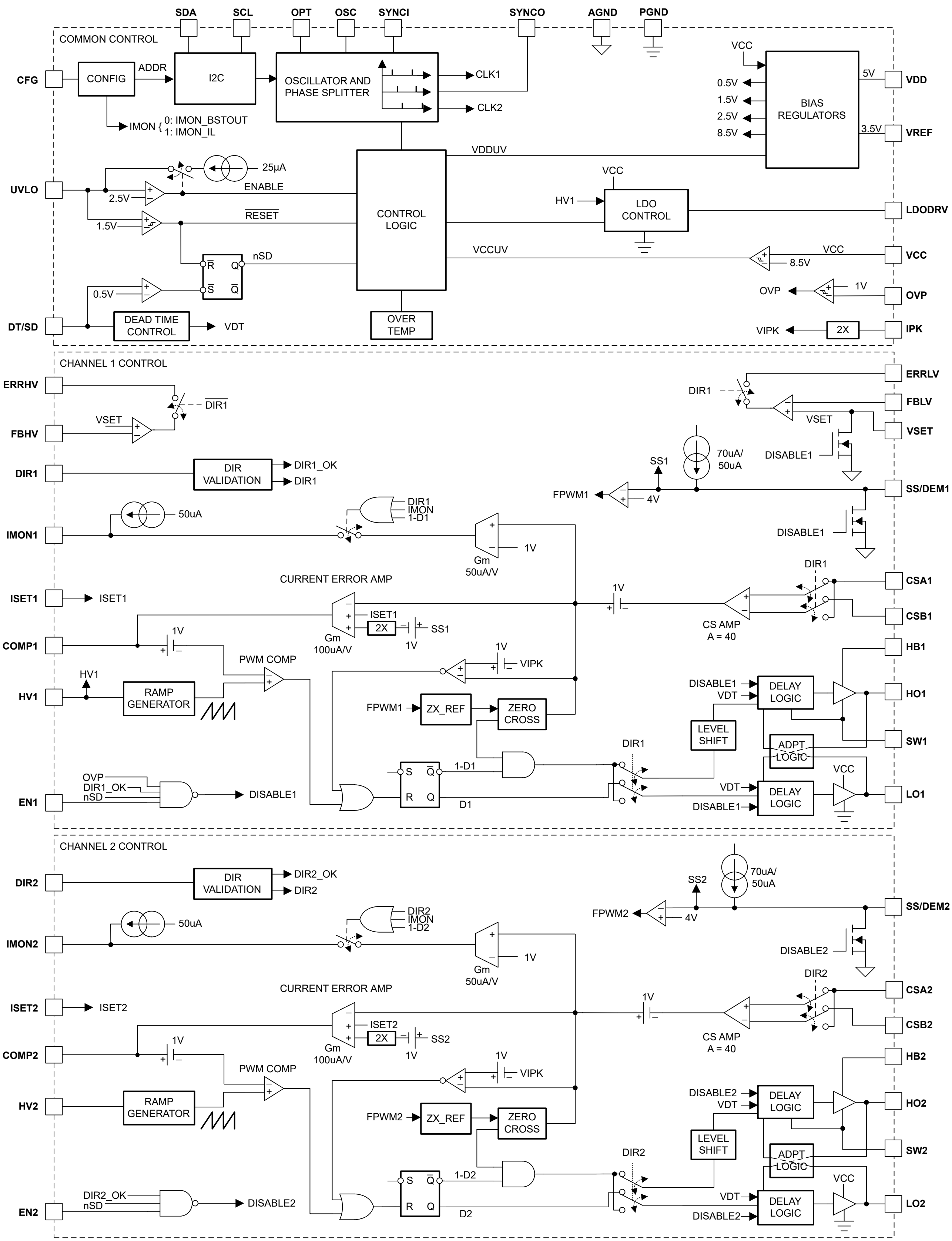
The LM5171-Q1 device is a high performance, dual-channel bidirectional PWM controller intended to manage power transfer between the High Voltage Port (HV-Port) and the Low Voltage Port (LV-Port) . The LM5171-Q1 integrates the essential analog functions that enable the design of high-power converters with a minimal number of external components. Depending on the operating mode, the device regulates both the output port voltages, or currents, in either direction by the DIRx signal.

The dual-channel differential current sense amplifiers and dedicated channel current monitors achieve a typical accuracy of 1%. The robust 5A half-bridge gate drivers are capable of driving parallel MOSFET switches for higher power per channel. The device offers dynamically selectable Diode Emulation Mode (DEM) and Forced PWM (FPWM). With DEM, the buck or boost synchronous rectifiers enables discontinuous mode operation for improved efficiency under light load conditions, and it also prevents negative current. With FPWM, the synchronous rectifier allows negative current and hence helps achieving a fast dynamic response under large circuit transients. Versatile protection features include the cycle-by-cycle peak current limit, overvoltage protection of both HV and LV Ports, detection and protection of MOSFET switch failures, and overtemperature protection.

The LM5171-Q1 uses an innovative average current mode control technology which simplifies the inner current loop compensation by maintaining a constant loop gain regardless of the power flow direction and the operating voltages and load level. The device also integrates two error amplifiers and a 1% accurate voltage reference to facilitate the bi-directional output voltage regulation. The free-running oscillator is adjustable up to 1000kHz and can be synchronized to an external clock within ±20% of the free running oscillator frequency. The stackable multiphase parallel operation is achieved by connecting two LM5171-Q1 controllers in parallel for 3 or 4 phase operation, or by synchronizing multiple LM5171-Q1 controllers with external multiphase clocks for a higher number of phases. In addition, an independent bi-directional converter can be realized by the two channels of the LM5171-Q1. The UVLO pin provides the commander ON/OFF control that disables the LM5171-Q1 in a low quiescent current shutdown state when the pin is held low.

The LM5171-Q1 also features an I^2C port, through which the status of operation and alarms of the device are monitored.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Bias Supplies and Voltage Reference (VCC, VDD, and VREF)

The LM5171-Q1 integrates a LDO driver to drive an external N-channel MOSFET to generate a 9V bias supply at the VCC pin. The VCC pin also accepts an external supply of 9.5V to 12V and the device turns off the LDO driver to save the power dissipation in the external LDO MOSFET. Figure 6-1 shows typical connections of the bias supply.

When an external supply is used, it is recommended to add a block diode to prevent from discharging the VCC during transient in the external supply. If an external supply voltage is greater than 12V, a 10V LDO or switching regulator is used to produce 10V for VCC. The VCC voltage is directly fed to the low-side MOSFET drivers. Place a 1µF to 2.2µF ceramic capacitance between the VCC and PGND pins to bypass the driver switching currents. For the LDO MOSFET, it is recommended to have the C_{iss} around 300pF or below.

The internal VCC undervoltage (UV) detection circuit monitors the VCC voltage. When the VCC voltage falls below 8V on the falling edge, the LM5171-Q1 is held in the shutdown state. For normal operation, a VCC voltage greater than 8.5V on the rising edge is needed.

Once the VCC voltage rises above the VCC_UV, the VDD and VREF regulators turn on. The VDD regulator provides 5V output with a loading capability of 10mA. Place a 1µF ceramic capacitor between VDD and AGND. The VREF is a 1% tolerance 3.5V voltage reference with a loading capability of 2mA. Place 0.1 µF ceramic capacitor between VREF and AGND.

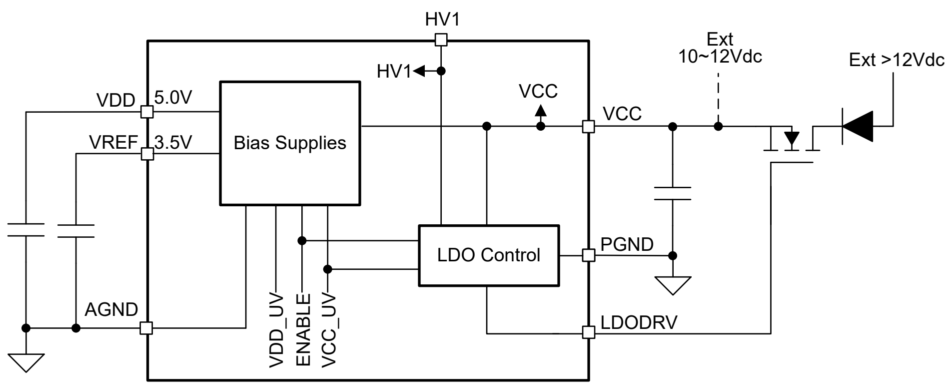


Figure 6-1. Bias Supplies Connections

6.3.2 Undervoltage Lockout (UVLO)

The UVLO pin serves as the primary enable or disable pin. There are two UVLO voltage thresholds. When the pin voltage is externally pulled below 1.25V, the LM5171-Q1 is in shutdown mode, in which all gate drivers are in the OFF state, all internal logic resets, and the IC draws less than 10µA through each of the HV and VCC pins.

When the UVLO pin voltage is pulled higher than 1.5V but lower than 2.5V, the LM5171-Q1 is in the initialization mode in which LDODRV pin turns on to control the external MOSFET to establish the VCC voltage at 9.0V, and the VDD at 5.0V and VREF at 3.5V. The DT/SD pin is pulled up to 1.2V, but the rest of the LM5171-Q1 remains off.

When the UVLO pin is pulled higher than 2.5V, which is the UVLO release threshold and the controller enable threshold, the LM5171-Q1 oscillator is activated, and the SYNCO pin gives out the phase shifted clock at the oscillator frequency, and the LM5171-Q1 is ready to operate. The SS/DEM1 and SS/DEM2 as well as LO1, LO2, HO1, and HO2 drivers remain off until the EN1, EN2, and DIR inputs command them to operate.

The UVLO pin can be directly controlled by an external control unit like an MCU.

Nevertheless, the UVLO pin can also fulfill the undervoltage lockout function of a particular power rail. The rail is either the HV-Port, the LV-Port or VCC. Use a resistor divider to set the UVLO threshold, as shown in . The divider is calculated as Equation 1:

$$\frac{R_{UVLO2}}{R_{UVLO1} + R_{UVLO2}} \times V_{UVLO} = 2.5\ \text{V} \tag{1}$$

The UVLO hysteresis is accomplished with an internal 25µA current source. When UVLO > 2.5V, the current source is activated to instantly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 2.5V threshold the current source is turned off, causing the voltage at the UVLO pin to fall. The UVLO hysteresis is determined by Equation 2:

$$V_{HYS} = R_{UVLO1} \times 25\ \mu\text{A} \tag{2}$$

Place an optional ceramic capacitor C_{UVLO} in parallel with R_{UVLO2} to improve the noise immunity. C_{UVLO} is usually between 1nF to 10nF. A large C_{UVLO} prolongs the delay to respond to a real UVLO event.

If Equation 2 does not provide adequate hysteresis voltage, add R_{UVLO3} as shown in UVLO With Additional Hysteresis Programming. The hysteresis voltage is thus given by Equation 3:

$$V_{HYS} = \left[R_{UVLO1} + R_{UVLO3} \times \left(1 + \frac{R_{UVLO1}}{R_{UVLO2}}\right)\right] \times 25\ \mu\text{A} \tag{3}$$

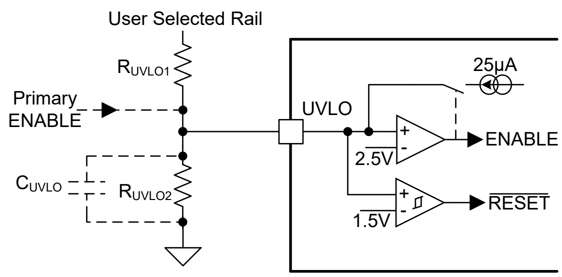


Figure 6-2. UVLO Programming

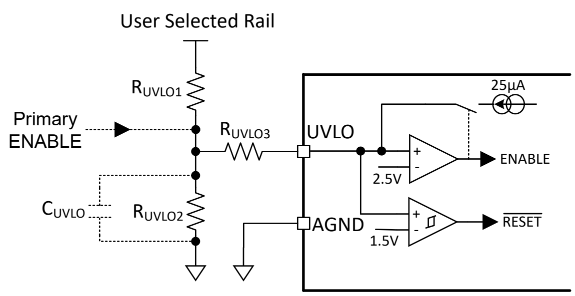


Figure 6-3. UVLO With Additional Hysteresis Programming

6.3.3 Device Configurations (CFG)

A resistor between CFG and AGND selects the I2C address and IMON function as listed in Table 6-1.

IMONx will monitor the boost output current when IMON_BSTOUT is selected in boost mode. When IMON_IL is selected or the device is operating in buck mode, IMONx monitors the inductor current. Refer to Channel Current Monitor (IMON1, IMON2) for more details.

Table 6-1. CFG Programming for IMONs and I2C Address

CFG Resistor Selection (kΩ) (1% Resistor)		I2C Address	IMON Function
Min	Max		
0	0.1	0x20	IMON_IL
0.316	0.324	0x21	IMON_IL
0.649	0.665	0x22	IMON_IL

Table 6-1. CFG Programming for IMONs and I2C Address (continued)

CFG Resistor Selection (kΩ) (1% Resistor)		I2C Address	IMON Function
Min	Max		
1.10	1.13	0x23	IMON_IL
1.65	1.69	0x24	IMON_IL
2.43	2.49	0x25	IMON_IL
3.32	3.40	0x26	IMON_IL
4.53	4.64	0x27	IMON_IL
6.65	6.81	0x27	IMON_BSTOUT
10.2	10.5	0x26	IMON_BSTOUT
13.7	14.0	0x25	IMON_BSTOUT
18.7	19.1	0x24	IMON_BSTOUT
26.1	26.7	0x23	IMON_BSTOUT
37.4	38.3	0x22	IMON_BSTOUT
60.4	61.9	0x21	IMON_BSTOUT
95.3	97.6	0x20	IMON_BSTOUT

6.3.4 High Voltage Inputs (HV1, HV2)

Figure 6-4 shows the external and internal configuration for the HV1 and HV2 pins. Both pins are rated at $85V_{DC}$. For independent channel operation connect the HV1 and HV2 pins to the HV-port voltage rails for each channel, respectively, which are not necessarily the same HV-port. When operating in parallel dual phase configuration to support high power the two HV pins can be tied together and connect to the same HV-port. As shown in Figure 6-4 to bypass high frequency noises apply a small RC filter like 10Ω and 0.1µF at these two pins.

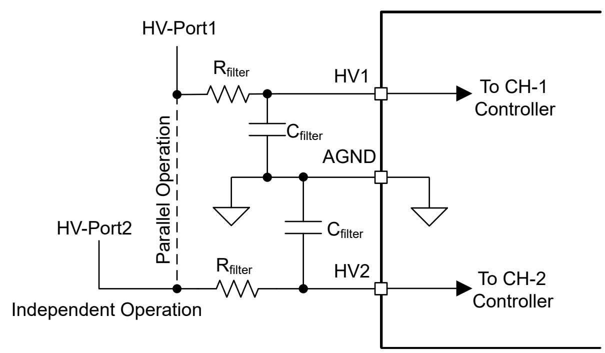


Figure 6-4. HV1 and HV2 Pins Configuration

6.3.5 Current Sense Amplifier

Each channel of the LM5171-Q1 has a bidirectional high accuracy high-speed current sense amplifier. The current sense polarity is determined by the DIR1 and DIR2. The amplifier gain is 40, such that a smaller current sense resistor is supported to reduce power dissipation. The amplified current sense signal is used to perform the following functions:

- Applied to the inverting input of the trans-conductance amplifier for the current loop regulation.
- Used to reconstruct the channel current monitor signal at the IMON1 and IMON2 pins.
- Monitored by the cycle-by-cycle peak current limit comparator for the instantaneous overcurrent protection.
- Sensed by the current zero cross detector to operate the synchronous rectifiers in the diode emulation mode.

Select the current sense resistor R_{CS} for 50mV current sense voltage at rated current. Connect the CSA1, CSB1, CSA2 and CSB2 pins via Kelvin connection for accurate sensing.

It is very important that the current sense resistors are low-inductive. Otherwise the sensed current signals are distorted even if the parasitic inductance is only a few nH. Such inductance has only minimal influence on the current regulation during continuous conduction mode, but it affects current zero cross detection, and hence the performance of diode emulation mode under light load. As a consequence, the synchronous rectifier gate pulse is truncated much earlier than the inductor current zero crossing, causing the body diode of the synchronous rectifier to conduct unnecessarily for a longer time. See the *Diode Emulation* for details.

If the selected current sense resistor has parasitic inductance, see the *Section 8.1* for methods to compensate for this condition and achieve optimal performance.

6.3.6 Control Commands

6.3.6.1 Channel Enable Commands (EN1, EN2)

These pins are two state function pins. EN1 and EN2 are independent command signals. EN1 controls CH-1, and EN2 controls CH-2.

1. When the EN1 pin voltage is pulled above 2V (logic state of 1), the HO1 and LO1 outputs of the same channel are enabled through soft start programmed by SS/DEM1.
2. When the EN1 pin voltage is pulled below 1V (logic state of 0), CH-1 controller is disabled and both HO1 and LO1 outputs are turned off, and SS/DEM1 is discharged.
3. Similar behaviors for EN2, HO2 and LO2, and SS/DEM2 of CH-2.
4. When the EN1 and EN2 pins are left open, an internal 1000kΩ pulldown resistor sets them to the low state.
5. The built-in 2.5µs glitch filters prevent errant operation due to the noise on the EN1 and EN2 signals.

6.3.6.2 Direction Command (DIR1 and DIR2)

These pins are tri-state function pins. DIR1 controls CH-1, and DIR2 controls CH-2.

1. When the DIR1 pin is actively pulled above 2V (logic state of 1), CH-1 operates in buck mode, and current flows from the HV-Port to the LV-Port.
2. When the DIR1 pin is actively pulled below 1V (logic state of 0), CH-1 operates in boost mode, and current flows from the LV-Port to the HV-Port.
3. When DIR1 is left open, the DIR1 is around 1.5V that is considered an invalid command and CH-1 remains in standby mode regardless of the EN1 states. This tri-state function prevents faulty operation when losing the DIR signal connection to the MCU.
4. When DIR1 changes the logic state between 1 and 0 dynamically during operation, the transition causes the SS/DEM1 pin to discharge first to below 0.3V, then the SS/DEM1 pin pulldown is released and CH-1 goes through a new soft-start process to produce the current in the new direction. The soft-start eliminates the surge current during the direction change.
5. Similar behaviors for DIR2, CH-2, EN2, and SS/DEM2.
6. The built-in 10µs glitch filter prevents errant operation by noise on the DIR1 and DIR2 signals.

6.3.6.3 Channel Current Setting Commands (ISET1 and ISET2)

Each channel has an independent current setting pin ISETx. Apply a voltage to ISETx pin to set the channel current. Balanced current sharing is achieved when same voltage is applied to each ISETx pins.

As shown in Figure 6-5, the ISETx pin signal feeds directly to one of the two non-inverting inputs of the gm amplifier. The other non-inverting pin is controlled by the soft-start. The current sense signal has 1V offset before it feeds to the inverting input of the gm amplifier.

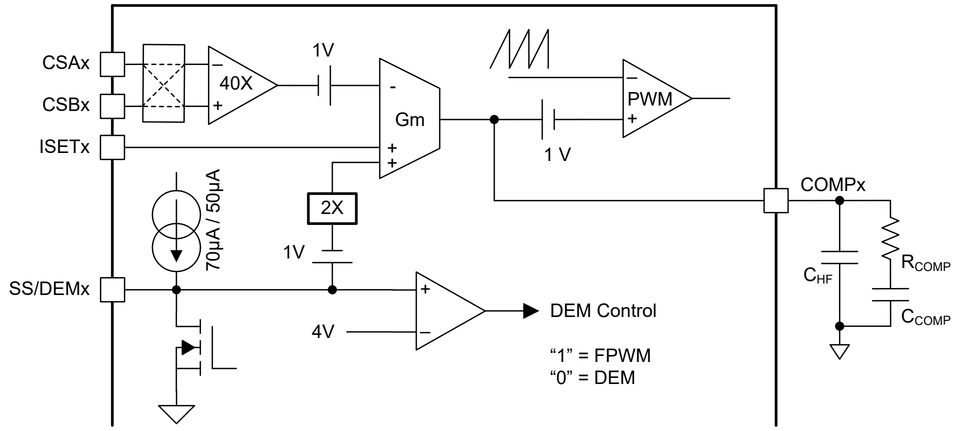


Figure 6-5. Inner Loop GM Amplifier, Soft-Start, and PWM Comparator

In close loop operation, the voltage across the current sense resistor R_{CS} is determined by,

$$V_{CS} = \frac{V_{ISET} - 1V}{40} \tag{4}$$

The equation is illustrated in Figure 6-6. In FPWM mode, the current sense voltage goes negative if V_{ISET} is less than 1V. In DEM mode the sense voltage stays at 0V if V_{ISET} is less than 1V.

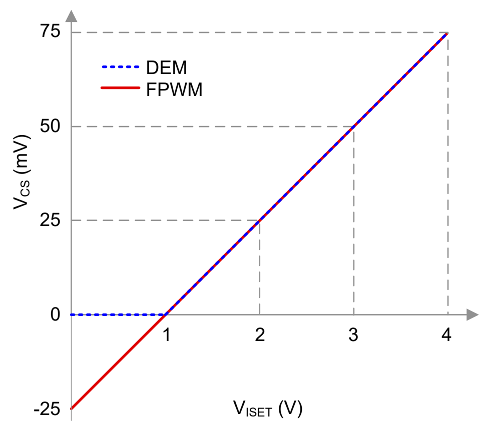


Figure 6-6. ISET voltage and current sense voltage

If a PWM signal is provided to control the channel current but no DAC is available, it is recommend to use a two-stage RC filter to convert it to the analog voltage at the ISET, as shown in Figure 6-7. The corner frequency of the filter is set to at least 1 decade below the PWM frequency in order to attenuate the ripple voltage to less than 1% at the ISET pin, namely, the RC selection satisfies , and the PWM to analog voltage conversion is given by Equation 6.

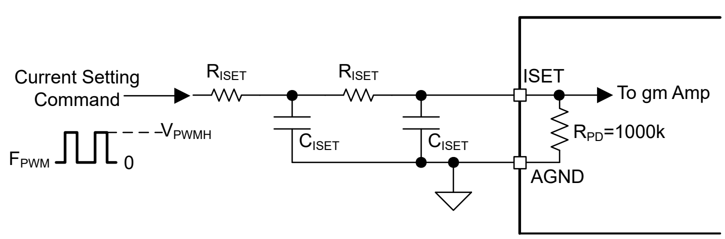


Figure 6-7. PWM Channel Current Programming

$$\frac{1}{2\pi \times R_{ISET} \times C_{ISET}} < \frac{F_{PWM}}{10} \tag{5}$$

$$V_{ISET} = \frac{R_{PD}}{R_{PD} + 2 \times R_{ISET}} \times V_{PWMH} \times D_{PWM} \tag{6}$$

Where

- F_{PWM} is the PWM signal frequency.
- R_{PD} is the internal pulldown resistor, which is 1000kΩ typical.
- V_{PWMH} is the PWM signal magnitude.
- D_{PWM} is the PWM signal duty cycle.

Note that the internal pulldown resistor R_{PD} has some error. If R_{ISET} << R_{PD}, the effects of the tolerance on V_{ISET} accuracy are greatly reduced.

6.3.7 Channel Current Monitor (IMON1, IMON2)

The LM5171-Q1 monitors the real time inductor current in each channel by converting the current sense voltage to small current sources at IMON1 and IMON2 pins.

As shown in Table 6-2, IMONx is set to monitor the inductor current or boost output current.

- When DIR = boost **and** IMON Function = IMON_BSTOUT, IMONx monitors the boost output current.
- When DIR = buck **or** IMON Function = IMON_IL, IMONx monitors the inductor current.

Table 6-2. IMON function and DIR

		IMON Function	
		IMON_IL	**IMON_BSTOUT**
DIR	**Buck**	Monitoring Inductor Current	Monitoring Inductor Current
	Boost	Monitoring Inductor Current	Monitoring Boost Output Current

6.3.7.1 Individual Channel Current Monitor

When the IMONx is "Monitoring Inductor Current" as shown in Table 6-2, the IMONx pin source current is determined by,

$$I_{IMON} = R_{CS} \times I_{Lm} \times 2\frac{\mu A}{mV} + 50\mu A \tag{7}$$

Where

- R_{CS} is the current sense resistor of the channel.
- I_{Lm} is the inductor current of the channel.
- 50µA is the DC offset current superimposed on to the IMON signals.

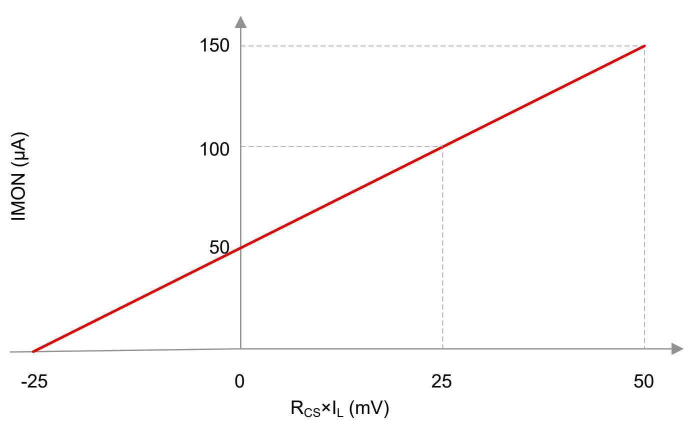


Figure 6-8. IMON Current Source vs Current Sense Voltage

When the IMONx is configured to monitor boost output current (Refer to Table 6-2), the IMONx pin source current is determined by,

$$I_{IMON\_BSTOUT} = R_{CS} \times I_{BSTOUT} \times 2\frac{\mu A}{mV} + 50\mu A \quad (8)$$

Where

- I_{MON_BSTOUT} is the boost mode output current of the channel.

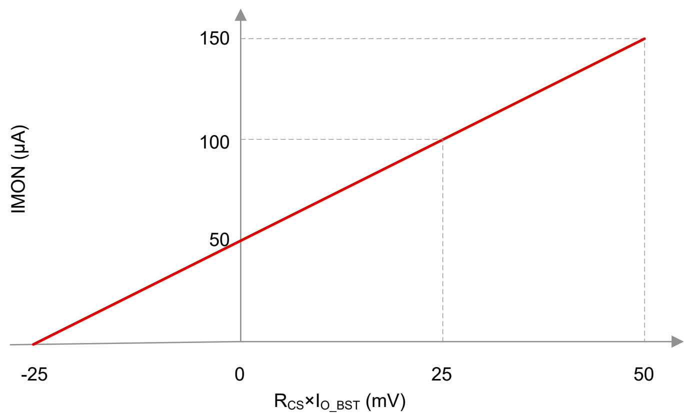


Figure 6-9. IMON Current Source vs Boost Output Current

The 50µA DC offset current is introduced to raise the no-load signal above the possible ground noise floor. Because the monitor signal is in the form of current, an accurate reading is obtained across a termination resistor even if the resistor is located far from the LM5171-Q1 but close to the MCU, thus rejecting potential ground differences between the LM5171-Q1 and the MCU. Figure 6-10 shows a typical channel current monitor through a 20kΩ termination resistor and a 10nF to 100nF ceramic capacitor in parallel. The RC network converts the current monitor signal into a DC voltage proportional to the channel DC current. Note that the maximum active operating voltage of the IMONx pin is 3V.

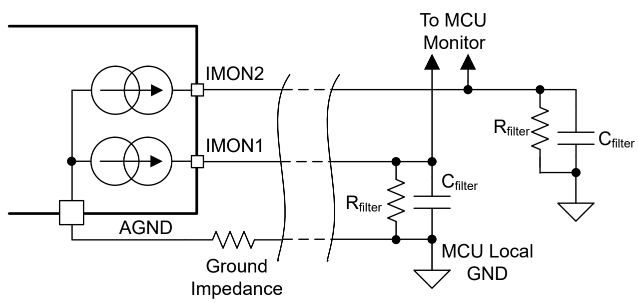


Figure 6-10. Channel Current Monitor

6.3.7.2 Multiphase Total Current Monitoring

For multiphase parallel operation, all LM5171-Q1 IMON pins can be combined to serve as a total current monitor. Combining the IMON signals also helps to save monitor lines. Figure 6-11 shows an example of total current monitor of a three-phase system in which the unused fourth phase monitor (U2-IMON2) is grounded.

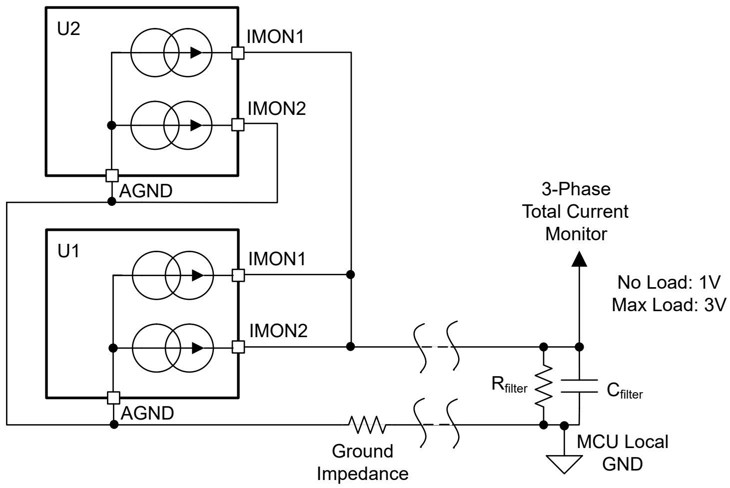


Figure 6-11. An Example of the 3-Phase Total Inductor Current Monitor

6.3.8 Cycle-by-Cycle Peak Current Limit (IPK)

IPK pin voltage programs the cycle-by-cycle current limit threshold. The threshold applies to both CH-1 and CH-2. The current sense signal of both phases are monitored in real time. Once the current sense voltage reaches the programmed threshold, the controller terminates the main switch duty cycle, thereby preventing the peak current from exceeding the threshold, and this function is fulfilled in each switching cycle. Device register faults when 9 peak current limit switching cycles occurred in operation and resumes itself when 4 non peak current limit cycles occur.

To set the inductor peak current limit threshold to I_{PK}, the IPK pin voltage is calculated as,

$$V_{IPK} = \frac{I_{PK} \times R_{CS}}{50\mathrm{mV/V}} \tag{9}$$

Select I_{PK} greater than the inductor peak current at full load, and lower than the inductor saturation current.

Program V_{IPK} with a resistor divider from VREF as shown in Figure 6-12. V_{IPK} is calculated as,

$$\mathrm{V_{IPK}} = \frac{\mathrm{R_{IPKB}}}{\mathrm{R_{IPKT}} + \mathrm{R_{IPKB}}} \times 3.5\mathrm{V} \tag{10}$$

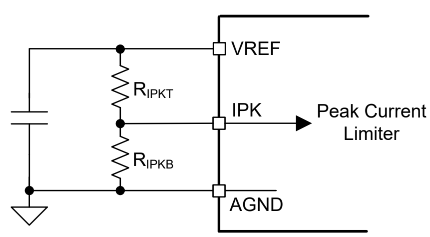


Figure 6-12. Cycle-by-Cycle Peak Current Limit Programming

It is recommended to select R_{IPKT} and R_{IPKB} such that the resistors do not draw more than 0.1mA from VREF pin, in order to keep the overall VREF current consumption low.

Note that IPK pin voltage needs to remain below 3V. When IPK pin voltage is greater than 3.3V, owing to an open R_{IPKB} or a short R_{IPKT} or some other reasons, an internal monitor circuit shuts down the switching off both controllers of the LM5171-Q1 by pulling SS1 and SS2 low internally, preventing the LM5171-Q1 from operating with erroneous peak current limit threshold.

6.3.9 Inner Current Loop Error Amplifier

As shown in Figure 6-5, each channel has an independent gm amplifier for the inner current loop. The inner current loop is basically a first order system. A Type-II compensation network is adequate to stabilize the inner current loop. The compensation applies to both the buck and boost operating modes. Refer to *Section 8.1* for more details.

6.3.10 Outer Voltage Loop Error Amplifier

As shown in Figure 8-6, two op amps are integrated by LM5171-Q1, which are designed for use as outer voltage loop error amplifiers. DIR1 determines which op amp is active. If CH-2 has an independent output, two external op amps are needed. Once the inner current loop is closed, the outer voltage loop is also a first order system and a Type-II compensation network is used to stabilize the output voltage loop. Refer to the *Section 8.1* section for details of the compensation.

6.3.11 Soft Start, Diode Emulation, and Forced PWM Control (SS/DEM1 and SS/DEM2)

The SS/DEMx are multifunction pins, which serve as ISETx soft-start, and also program each channel to operate in the Diode Emulation Mode (DEM) or Forced PWM Mode (FPWM).

Each channel has a real time zero current detector to monitor instantaneous V_{CS}. When V_{CS} is detected to cross zero, the LM5171-Q1 turns off the gate driver of the synchronous rectifier (Sync FET) to prevent negative current. In this way, the negative current is prevented and the light load efficiency is improved. Figure 6-13 shows typical waveforms in the DEM.

In FPWM mode, the sync FET has a complementary gate drive signal with the control FET, the zero crossing is ignored.

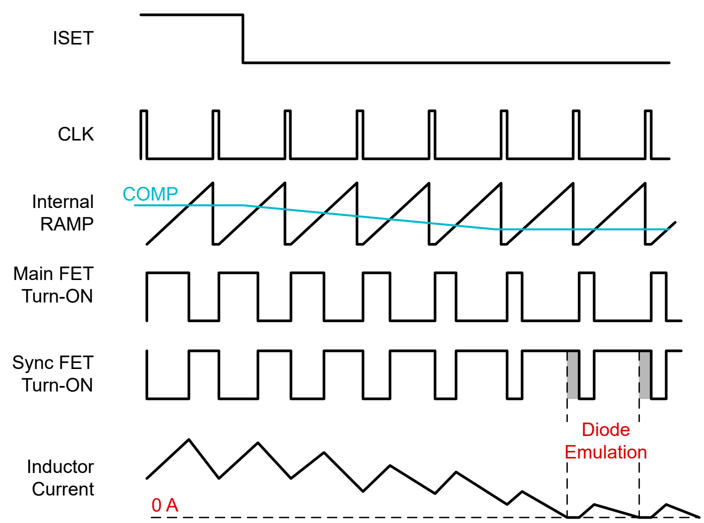


Figure 6-13. Diode Emulation Mode Operation

To obtain the designed diode emulation performance, the current sense signal are monitored with low noise and low delay. Any signal distortion caused by parasitic inductance in the current sense resistor or sensing traces leads to erroneous zero crossing detection and cause non-optimal diode emulation operation, and the Sync FET turnes off at high current. Refer to Current Sense (R_{CS}) for optimal diode emulation operation.

6.3.11.1 ISET Soft-Start Control by the SS/DEM Pins

Place a ceramic capacitor C_{SS1} between the SS/DEM1 pin and AGND to program ISET1 soft-start time. When EN1 goes low, C_{SS1} is discharged by the internal pulldown FET, the pulldown FET remains on until the SS/DEM1 voltage falls below 0.3V, which is the threshold voltage indicating the completion of SS/DEM1 discharge. When EN1 goes high, the SS pulldown FET is released, and C_{SS1} is charged up slowly by 70μA current source, as shown in Figure 6-5. The slow ramping SS/DEM1 voltage overrides the ISET1 voltage during soft-start.

The SS/DEM1 sets the non-inverting input of the gm amplifier to,

$$V_{ISET\_clamp} = 2 \times (V_{SS} - 1V) \tag{11}$$

From the equation, when the SS/DEM1 voltage is less than 1.5V, the non-inverting input of the gm amplifier is less than 1V, CH-1 does not switch.

Similar behaviors apply to SS/DEM2.

As shown in Figure 6-14, SS/DEM1 is pulled low when EN1 is low, DIR1 flips (DIR_OK1=0), shutdown, or OVP is triggered. OVP does not pull SS/DEM2 low.

SS/DEMx pin can be pulled low by external circuit to stop switching. The converter restarts switching once SS/DEMx pin is not pulled down. Pull DT/SD pin low for a latched shutdown.

In multiphase parallel operation, the SS/DEMx pins can be tied together.

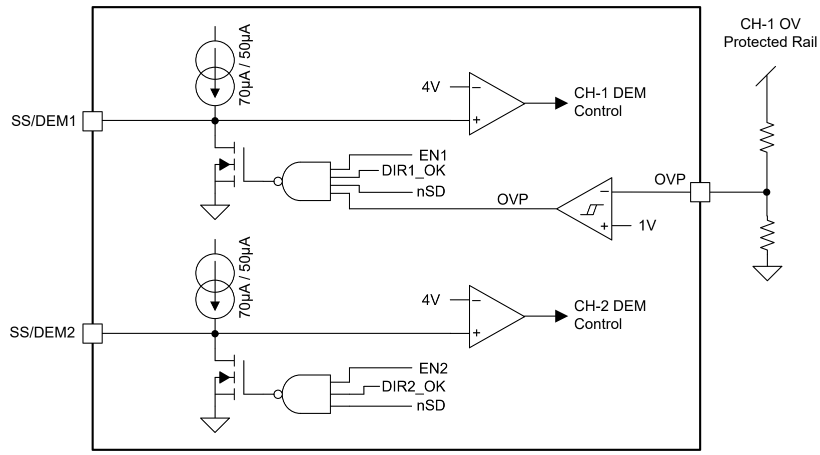


Figure 6-14. Soft-Start Control by the SS/DEMx Pins

6.3.11.2 DEM Programming

As shown in Figure 6-15, the SS/DEMx pin is monitored by an internal comparator in real time. When SS/DEMx pin voltage is less than 4V, the corresponding channel operates in DEM. When SS/DEMx pin voltage is higher than 4V, the corresponding channel operates in FPWM.

When SS/DEMx pin is less than 3.6V, the internal current source is 70µA. When SS/DEMx pin voltage reaches 3.6V, the current source deceases to 50µA. Placing a resistor between 54.9kΩ and 68.1kΩ from SS/DEMx to AGND sets SS/DEMx pin to 3.6V, and the channel operates in DEM.

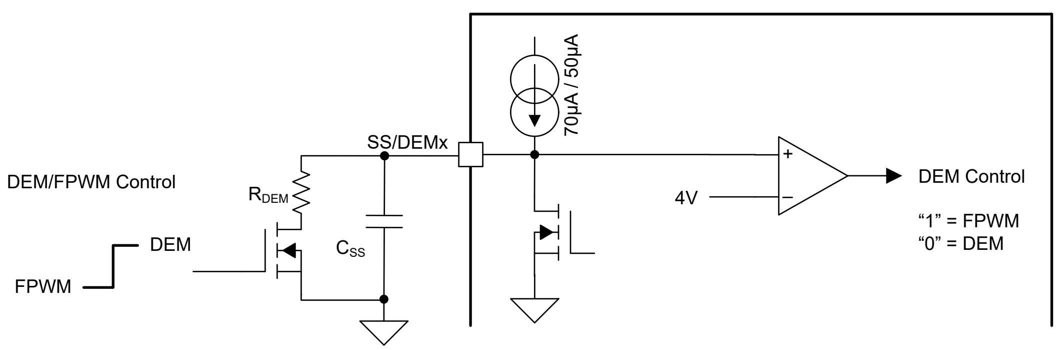


Figure 6-15. Dynamic FPWM and DEM Change

6.3.11.3 FPWM Programming and Dynamic FPWM and DEM Change

To dynamically change the operating mode between FPWM and DEM, switch on and off the R_{DEM} resistor by controlling the series FET, as shown in Figure 6-15. When the FET is turned on, it sets the channel in DEM. When the FET is turned off, it sets the channel in FPWM.

In 128 switching cycles the mode gradually changes from one mode to the other.

6.3.12 Gate Drive Outputs, Dead Time Programming and Adaptive Dead Time (HO1, HO2, LO1, LO2, DT/SD)

Each channel of the LM5171-Q1 has a robust 5A (peak) half bridge driver to drive external N-channel power MOSFETs. As shown in Figure 6-16, the low-side drive is directly powered by VCC, and the high-side driver by the bootstrap capacitor C_{BT}. During the on-time of the low-side driver, the SW pin is pulled down to PGND and C_{BT} is charged by VCC through the boot diode D_{BT}. TI recommends selecting a 0.1µF or larger ceramic capacitor for C_{BT}, and an ultra-fast diode of 1A and 100V ratings for D_{BT}. TI also strongly recommends users to add a 2Ω to 5Ω resistor (R_{BT}) in series with D_{BT} to limit the surge charging current and improve the noise immunity of the high-side driver.

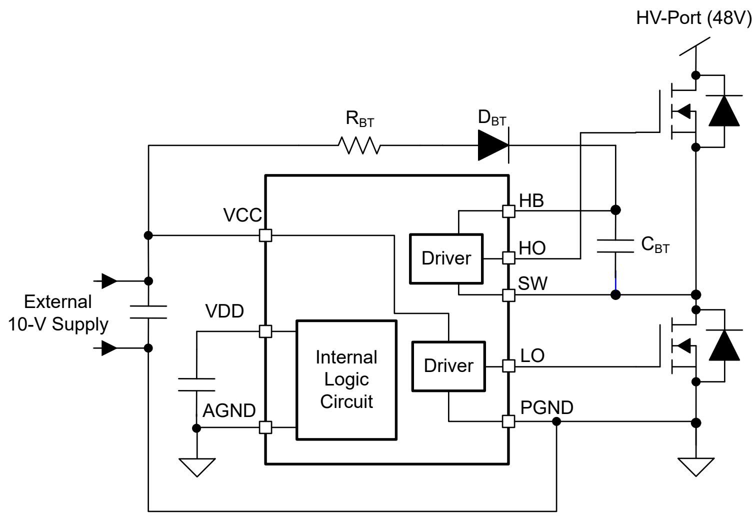


Figure 6-16. Bootstrap Circuit for High-Side Bias Supply (Only One Channel is Shown)

In case during start-up in buck mode, C_{BT} is not charged initially; the LM5171-Q1 then holds off the high-side driver outputs (HO1 and HO2) and sends LO pulses of 100ns width in consecutive cycles to pre-charge C_{BT}. When the boot voltage is greater than the 6.5V boot UV threshold, the high-side drivers output PWM signals at the HO1 and HO2 pins for normal switching action. If the boot voltage becomes lower than the boot UV threshold voltage on the falling edge, the corresponding HO output pulls low until the boot voltage recovers to assume normal HO switching pulses. During normal buck mode operation, when the CBT voltage falls below the 6.5V boot UV threshold, the same precharge function starts by interrupting the normal switching until the boot voltage restores above the UV threshold. The pre-charge function helps prevent the power MOSFETs from running into linear mode by inadequate gate voltage. Note that the gate threshold voltage of the MOSFETs potentially rises to 6V due to degradation over aging.

During start-up and normal operation in boost mode, C_{BT} is naturally charged by the normal turn on of the low side MOSFET, therefore there is no such 100-ns pre-charge pulse at the LO pins.

To prevent shoot-through between the high-side and low-side power MOSFETs on the same half bridge leg, two types of dead time schemes are selected with the DT pin: the programmable dead time or built-in adaptive dead time.

To program the dead time, place a resistor R_{DT} across the DT/SD and AGND pins as shown in Figure 6-17.

The dead time t_{DT} as depicted in Figure 6-18 is determined by Equation 12:

$$t_{DT} = R_{DT} \times 2.625 \frac{ns}{k\Omega} \quad (12)$$

Note that the equation is valid for programming t_{DT} between 15ns and 200ns. When the power MOSFET is connected to the gate drive, its gate input capacitance C_{ISS} becomes a load of the gate drive output, and the HO and LO slew rate are reduced, leading to a reduced effective t_{DT} between the high- and low-side MOSFETs. Evaluate the effective t_{DT} to make sure it is adequate to prevent shoot-through between the high- and low-side MOSFETs.

When the DT programmability is not used, simply connect the DT/SD pin to VDD as shown in Figure 6-19, to activate the built-in adaptive dead time. The adaptive dead time is implemented by real time monitoring of the output of a driver (either HO or LO) by the other driver (LO or HO) of the same half bridge switch leg, as shown in Figure 6-19 and Figure 6-20. Only when the output voltage of a driver falls below 1.5V does the other driver starts turn on. The effectiveness of adaptive dead time is greatly reduced if a series gate resistor is used, or if the PCB traces of the gate drive have excessive impedance due to poor layout design.

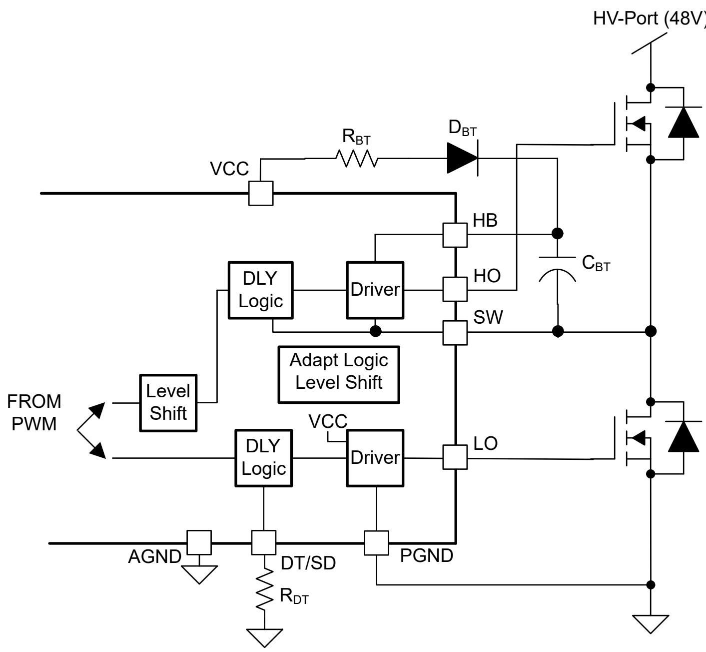


Figure 6-17. Dead Time Programming With DT Pin (Only One Channel is Shown)

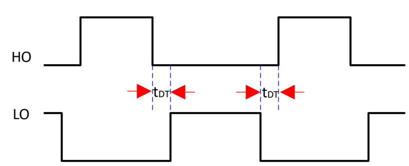


Figure 6-18. Gate Drive Dead Time (Only One Channel is Shown)

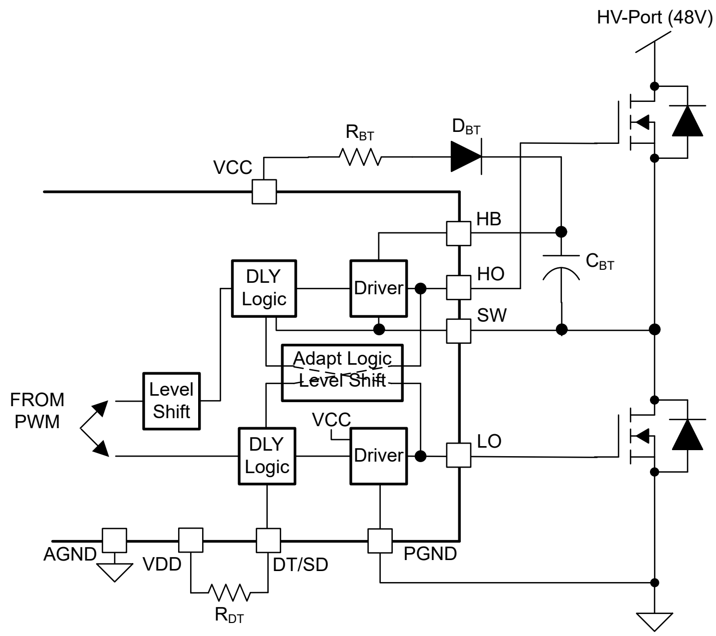


Figure 6-19. Dead Time without external Programming (Only One Channel is Shown)

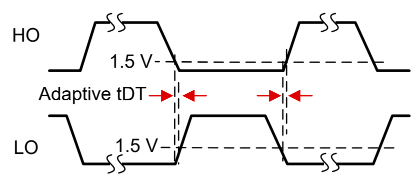


Figure 6-20. Adaptive Dead Time (Only One Channel is Shown)

6.3.13 Emergency Latched Shutdown (DT/SD)

The DT/SD pin also serves as an emergency latched shutdown pin. During the operation the DT/SD pin is monitored by an internal circuit. The pin is normally regulated at 1.2V with a sourcing current limit of 300µA. Once the pin is externally pulled down below 0.5V for more than 2.5µs, the LM5171-Q1 shuts down and the state is latched until the UVLO is pulled below 1.25V to unlatch. Figure 6-21 shows an example of implementing the emergency latched shutdown function

When the LM5171-Q1 sets for adaptive dead time scheme, DT/SD pin needs to be pulled up to VDD. In order to implement the emergency latched shutdown control in this case, a 20kΩ limiting resistor is placed across the VDD and DT/SD pin, as shown in Figure 6-22.

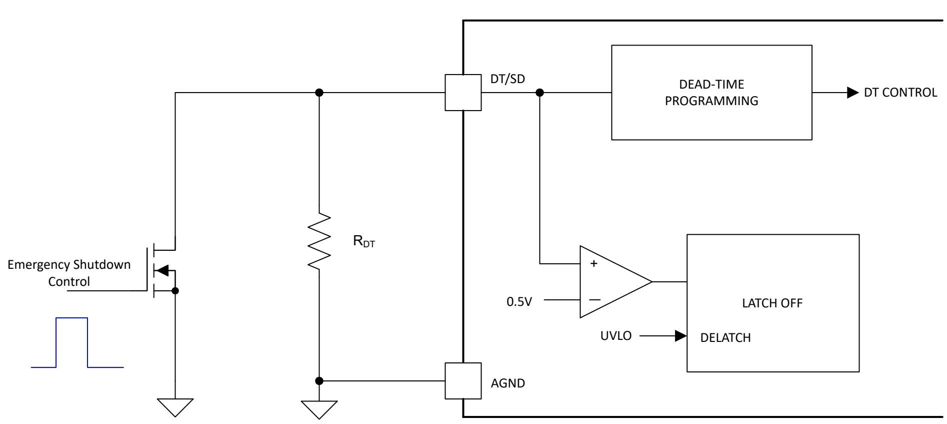


Figure 6-21. Emergency Latched Shutdown

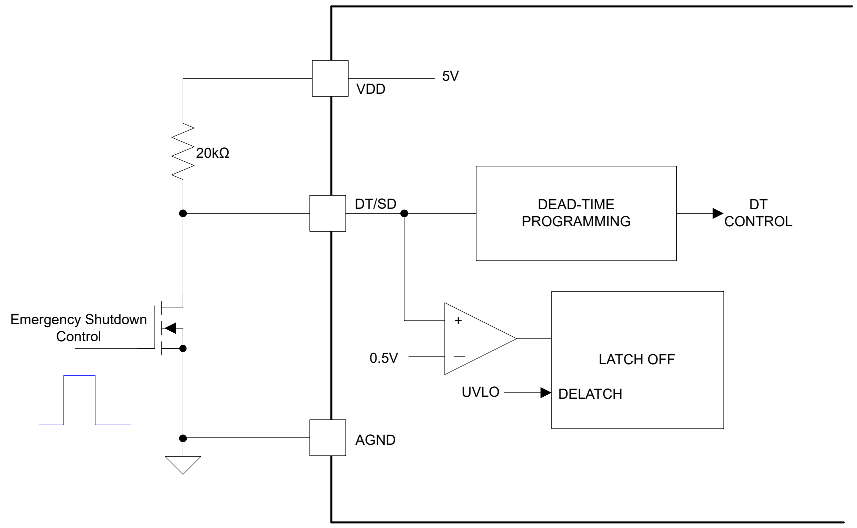


Figure 6-22. Emergency Latched Shutdown with Adaptive Deadtime Scheme

6.3.14 PWM Comparator

Each channel of the LM5171-Q1 has a pulse width modulator (PWM) employing a high-speed comparator. The modulator compares the internal ramp signal and the COMP pin signal to produce the PWM duty cycle. Note that the COMP signal passes through a 1V DC offset before it is applied to the PWM comparator, as shown in Figure 6-5. Owing to this DC offset, the duty cycle reduces to zero when the COMP pin or SS pin is pulled lower than 1V. The maximum duty cycle is limited by the 100ns typical minimum off-time, with the worst case max limit of 150ns. Note that the programmed dead time reduces the maximum duty cycle because it is additional to the minimum off-time. Therefore, the maximum duty cycle, for both buck and boost mode operation, is determined by,

$$D_{MAX} = 1 - (150\text{ns} + t_{DT}) \times F_{sw} \tag{13}$$

Where

- t_{DT} is the dead time given by Equation 12 or the adaptive dead time, whichever applicable.

This maximum duty cycle limits the minimum voltage step-down ratio in buck mode operation, and the maximum step-up ratio in boost mode operation.

6.3.15 Oscillator (OSC)

The LM5171-Q1 oscillator frequency is set by the external resistor R_{OSC} connected between the OSC pin and AGND, as shown in Figure 6-23. Keep the OSC pin connected whether or not an external clock is present. To set a desired oscillator frequency F_{OSC}, R_{OSC} is approximately determined by Equation 14:

$$R_{OSC} = \frac{41.5\text{k}\Omega \times 100\text{ kHz}}{F_{OSC}} \tag{14}$$

Place R_{OSC} as close as possible to the OSC and AGND pins. Take the tolerance of the external resistor and the frequency tolerance indicated in *Electrical Characteristics* into account when determining the worst-case operating frequency.

The LM5171-Q1 also includes a Phase-Locked Loop (PLL) circuit to manage multiphase interleaving phase angle as well as the synchronization to the external clock applied at the SYNCI pin. When no external clock is present, the converter operates at the oscillator frequency given by Equation 14. If an external clock signal of a frequency within ±20% of F_{SW} is applied (see *Section 6.3.16*), the converter switches at the frequency of the external clock F_{EX_CLK}, namely Equation 15:

$$F_{SW} = \begin{cases} F_{OSC} & \text{(in Standalone)} \\ F_{EX\_CLK} & \text{(in Synchronization)} \end{cases} \tag{15}$$

Two internal clock signals CLK1 and CLK2 are produced to control the interleaving operation of CH-1 and CH-2, respectively. The third clock signal is output at the SYNCO pin. All these three clock signals run at the same frequency of F_{SW}. The phase angles among these three clock signals are controlled by the state of the OPT pin. See *Section 6.3.18* for details.

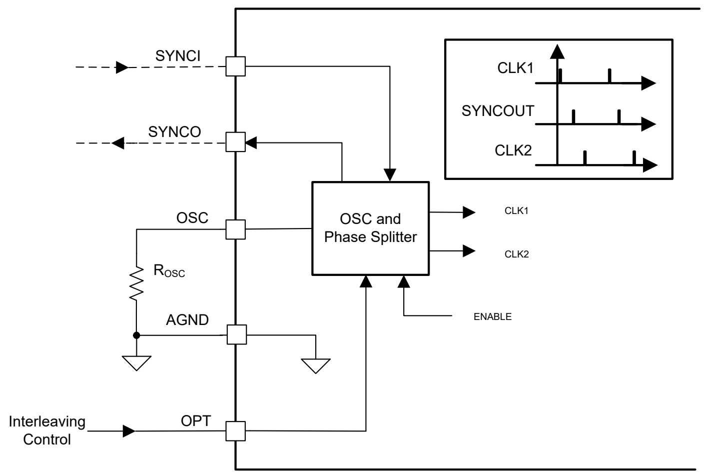


Figure 6-23. Oscillator and Interleaving Clock Programming

6.3.16 Synchronization to an External Clock (SYNCI, SYNCO)

The LM5171-Q1 synchronizes to an external clock if F_{EX_CLK} is within ±20% of F_{OSC}. The SYNCIN clock pulse width needs to be in the range of 100ns to 0.8/F_{OSC}, with a high voltage level > 2V and low voltage level < 1V.

F_{EX_CLK} allows dynamic adjustment. However the LM5171-Q1 PLL takes approximately 150µs to settle down to the newly asserted frequency. During the PLL transient, the instantaneous F_{SW} drops temporarily by up to 25%. To avoid overstress during the transient, TI recommends the user to reduce the load current to less than 50% by lowering the ISET voltage, or to simply turn off the dual-channels by setting EN1 = EN2 = 0 when making an the external clock change.

6.3.17 Overvoltage Protection (OVP)

As shown in Figure 6-24, the LM5171-Q1 includes OVP function, which can be used to monitor either the HV-port, or the LV-port, or a user defined voltage rail, through a resistor divider at the OVP pin.

A resistor divider at the OVP pin sets the OVP threshold. When the OVP pin voltage exceeds the 1V threshold on the rising edge, both HO1 and LO1 are turned off. At the same time C_{SS1} is discharged, and the C_{SS1} remains discharged as long as the OVP event lasts. When the OVP voltage falls below 0.9V threshold on the falling edge, the OVP alarm is removed, the SS/DEM1 pulldown is released, and CH-1 resumes operation through a soft-start. See ISET Soft-Start Control by the SS/DEM Pins for details.

Note that OVP only affects CH-1, but not CH-2. Connect SS/DEM1 and SS/DEM2 to enable OVP for both channels. Refer to Figure 6-24 for additional OVP. An open drain comparator discharges SS/DEM1 and SS/DEM2 once the protected railed voltage exceeds the OVP threshold.

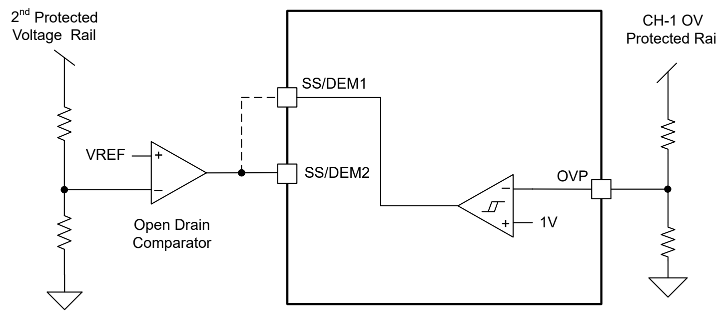


Figure 6-24. OVP for Second Protected Voltage Rail

6.3.18 Multiphase Configurations (SYNCO, OPT)

There are various options to make multiphase configurations.

6.3.18.1 Multiphase in Star Configuration

Each LM5171-Q1 synchronizes to an external clock. Each clock signals has an appropriate phase delay for proper multiphase interleaving operation. The interleave angle between the two phases of each LM5171-Q1 are programmed to 180° or 240° by the OPT pin. The SYNCIN and SYNCOUT are phase shifted by 90° with each other. For higher stage phases (more than 8) a HOST MCU is used to generate SYNCIN pulses for set of each 8 phase block. Table 6-3 summarizes the settings of the external clocks and the OPT pin state for multiphase configurations.

Table 6-3. Multiphase Configurations With Individual External Clock

NUMBER OF PHASES	PHASE SHIFT BETWEEN EXTERNAL CLOCKS FOR MULTIPHASE INTERLEAVING	OPT LOGIC STATE(1)	CH-2 PHASE LAGGING VS CH-1	NUMBER OF LM5171 CONTROLLERS NEEDED	NUMBER OF EXTERNAL CLOCKS NEEDED
2	180°	1	180°	1	1 or 0
3	120°	0	240°	2	2
4	90°	1	180°	2	2
6	60° or 120°	1	180°	3	3
8	45°	1	180°	4	2

(1) OPT State = 0 when the pin connects to AGND, and 1 when the pin voltage is VDD.

6.3.18.2 Daisy-Chain Configurations for 2, 3, or 4 Phases parallel operations

Daisy-chaining is used to achieve 1, 2, 3, or 4 phases without using an external clock. Table 6-4 summarizes the OPT settings for the daisy-chain multiphase configurations. Figure 6-25 shows an example of daisy-chain connection for three and four phases interchangeable operation.

Table 6-4. Multiphase Configurations With Built-In Daisy-Chain Controller - Responder Configuration

NUMBER OF PHASES	OPT LOGIC STATE(1)	CH-2 PHASE LAGGING VS CH-1	SYNCOUT PHASE LAGGING VS CH-1	NUMBER OF LM5171 CONTROLLERS NEEDED	NUMBER OF EXTERNAL CLOCKS NEEDED
2	1	180°	90°	1	0 or 1
3	0	240°	120°	2	0 or 1
4	1	180°	90°	2	0 or 1

(1) OPT State = 0 when the pin connects to AGND, and 1 when the pin voltage is VDD.

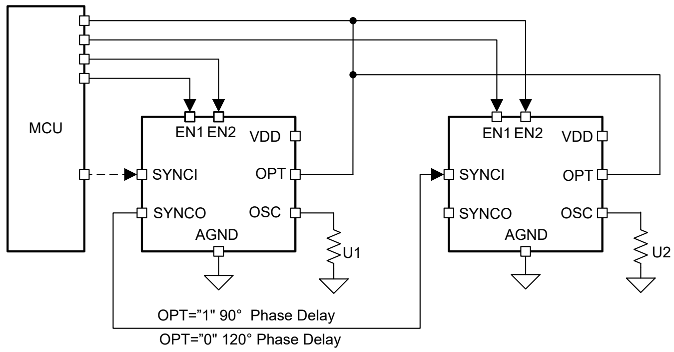


Figure 6-25. Three or Four Phases Interchangeable Configuration

6.3.18.3 Daisy-Chain configuration for 6 or 8 phases parallel operation

To configure 6 phases, it requires daisy chain as shown in Figure 6-26 and for 8 phases, it requires daisy chain as shown in Figure 6-27.

Note that two phase-shifted external clock signals are required for proper interleaving operation

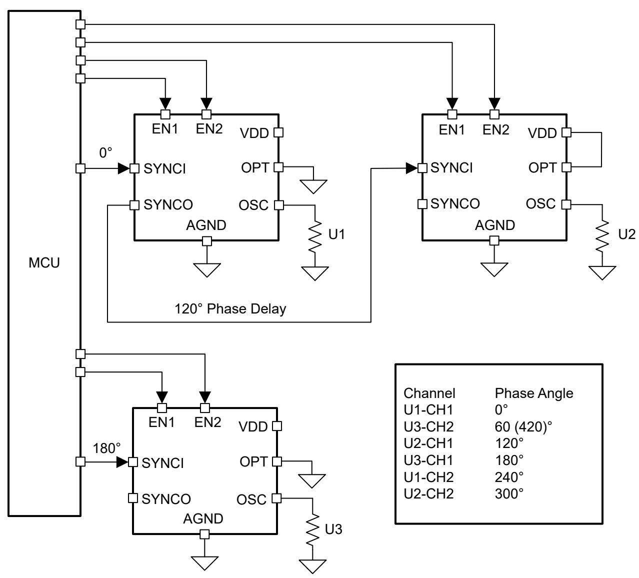


Figure 6-26. Six Phases 60° Interleaving Configuration using External Clock Shift

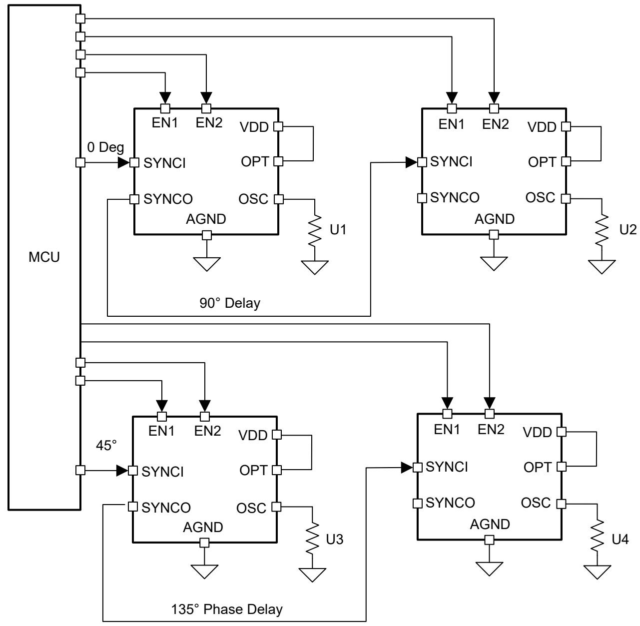


Figure 6-27. Eight Phases 45° Interleaving Configuration using External Clock Shift

When external clock signals are not available, the 6-phase is configured in 120° interleaving as shown in Figure 6-28.

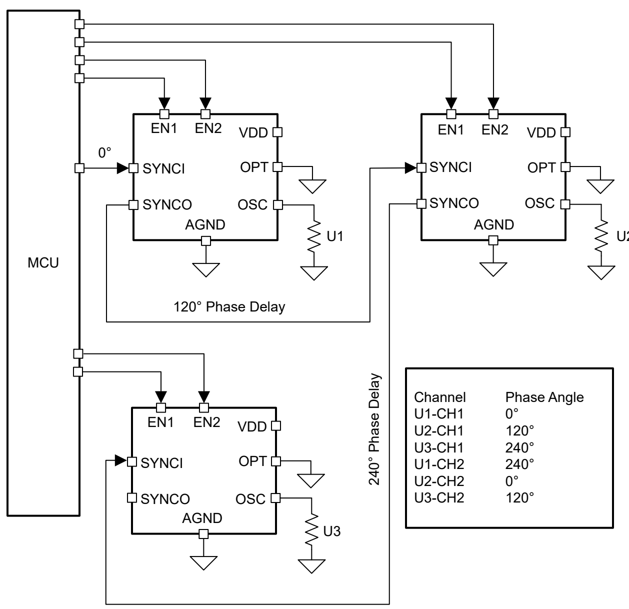


Figure 6-28. Six Phases 120° Interleaving Configuration using Internal Clock Shift

6.3.19 Thermal Shutdown

An internal thermal shutdown is provided to protect the device in case that the junction temperature exceeds 175°C typical. During thermal shutdown, the device is forced into a low power state with the MOSFET drivers disabled, and SS/DEM1 and SS/DEM2 pin internally pulled down and held low. After the junction temperature is reduced (typical hysteresis is 15°C), the device steps out of the thermal shutdown mode, and it restarts through soft-start by releasing the SS/DEM1 and SS/DEM2 pulldown.

6.4 Device Functional Modes

6.4.1 Initialization Mode

When the UVLO pin is > 1.5V but < 2.5V, and DT/SD > 0.5V, the LM5171-Q1 establishes proper internal logic states, and the LDODRV is turned on to control the external MOSFET to produce the VCC, and LM5171-Q1 prepares for circuit operation. Once VCC voltage is >8.5V, VDD and VREF are also established at approximately 5.0V and 3.5V, respectively.

6.4.2 Standby Mode

When the UVLO pin is > 2.5V, and VCC > 8.5V, VDD> 4.5V, and DT/SD > 0.5V, the LM5171-Q1 is ready to operate. The oscillator is activated and the SYNCO is firing phase-shifted clock signals, but the four gate drive outputs remain off until the EN1 or EN2 initiate the power delivery mode.

6.4.3 Power Delivery Mode

When the UVLO pin > 2.5V, VCC > 8.5V, VDD > 4.5V, DT/SD > 0.5V, EN1 or EN2 > 2V, DIR1 and/or DIR2 is valid (> 2V or < 1V), the SS capacitor is charged. Once the SS voltage rises above 1.5V, the LM5171-Q1 starts switching.

6.4.4 Shutdown Mode

When the UVLO pin is < 1.25V, the LM5171-Q1 is in the shutdown mode with all gate drivers in the low state, and all internal logic reset. When UVLO < 1.25V, the device draws < 10μA through each of the HV1, HV2 and VCC pins.

6.4.5 Latched Shutdown mode

Pulling DT/SD pin low sets LM5171-Q1 in latched shutdown mode. In latched shutdown mode, all gate drivers remain in low state, and both SS/DEM1 and SS/DEM2 pins are held low. Reset the latch by pulling the UVLO to below 1.25V for at least 10μs.

7 Registers

7.1 I²C Serial Interface

In LM5171-Q1, I²C communication is available when the UVLO pin is > 1.5V and the configuration is complete. VDD pin voltage falling below 4.5V VDDUV disables the communication, but as long as it stays above 2.5V (the lower threshold), it does not require reconfiguring to enter the I²C communication when VDD goes out of VDDUV.

7.2 I²C Bus Operation

The I ² C bus is a communications link between a Controller and a series of Peripheral devices. The link is established using a two-wired bus consisting of a serial clock signal (SCL) and a serial data signal (SDA). The serial clock is sourced from the Controller in all cases where the serial data line is bi-directional for data communication between the Controller and the Peripheral terminals. Each device has an open-drain output to transmit data on the serial data line (SDA). An external pull-up resistor is placed on the serial data line to pull the drain output high during data transmission. The device hosts a Peripheral I ² C interface that supports standard-mode, fast-mode and fast-mode plus operation with data rates up to 100kbit/s, 400 kbit/s and 1000 kbit/s respectively and auto-increment addressing compatible to I ² C standard 3.0.

Data transmission is initiated with a start bit from the controller as shown in the figure below. The start condition is recognized when the SDA line transitions from high to low during the high portion of the SCL signal. Upon reception of a start bit, the device receives serial data on the SDA input and check for valid address and control information. If the peripheral address bits are set for the device, then the device issues an acknowledge pulse and prepares to receive the register address and data. Data transmission is completed by either the reception of a stop condition or the reception of the data word sent to the device. A stop condition is recognized as a low to high transition of the SDA input during the high portion of the SCL signal. All other transitions of the SDA line need to occur during the low portion of the SCL signal. An acknowledge is issued after the reception of valid address, sub-address and data words. The I ² C interfaces auto-sequence through register addresses, so that multiple data words are sent for a given I ² C transmission.

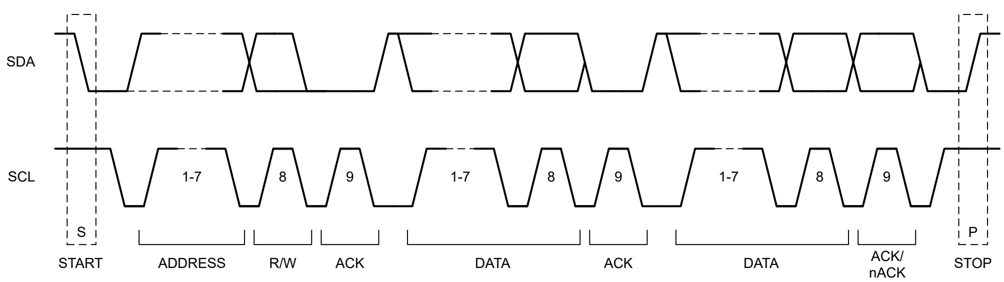


Figure 7-1. I ² C START / STOP / ACKNOWLEDGE Protocol

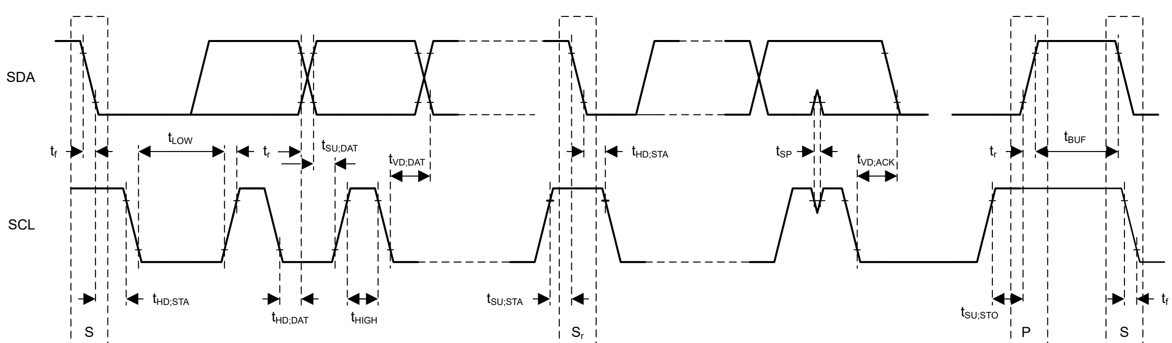


Figure 7-2. I ² C Data Transmission Timing

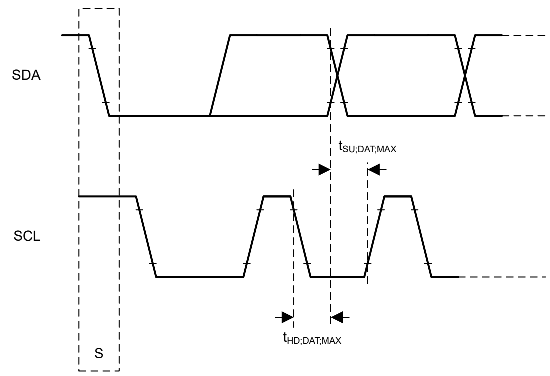


Figure 7-3. I ^{2} C Data Transmission Timing for maximum rise/fall times.

7.3 Clock Stretching

Clock stretching is not supported. If the device is addressed while busy and not able to process the received data, it does not acknowledge the transaction.

7.4 Data Transfer Formats

The device supports four different read/write operations:

- Single read from a defined register address.
- Single write to a defined register address.
- Sequential read starting from a defined register address
- Sequential write starting from a defined register address

7.5 Single READ From a Defined Register Address

Figure 7-4 shows the format of a single read from a defined register address. First, the Controller issues a start condition followed by a seven-bit I ^{2} C address. Next, the Controller writes a zero to signify that a write operation is conducted. Upon receiving an acknowledge from the Peripheral the Controller sends the eight-bit register address across the bus. Following a second acknowledge the device sets the internal I ^{2} C register number to the defined value. Then the Controller issues a repeat start condition and the seven-bit I ^{2} C address followed by a one to signify that a read operation has conducted. Upon receiving a third acknowledge, the Controller releases the bus to the device. The device then returns the eight-bit data value from the register on the bus. The Controller does not acknowledge (nACK) and issues a stop condition. This action concludes the register read.

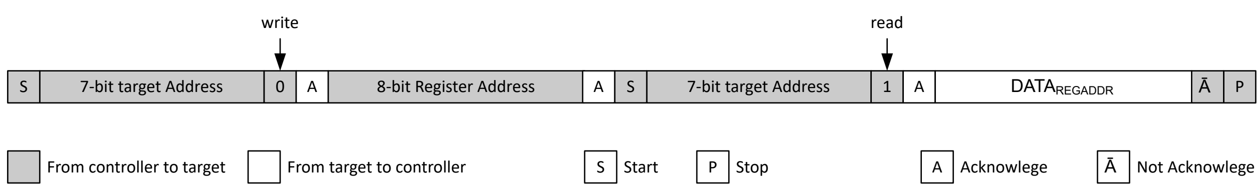


Figure 7-4. Single READ From a Defined Register Address

7.6 Sequential READ Starting From a Defined Register Address

A sequential read operation is an extension of the single read protocol and shown in Figure 7-5. The Controller acknowledges the reception of a data byte, the device auto increments the register address and returns the data from the next register. The data transfer is stopped by the Controller not acknowledging the last data byte and sending a stop condition.

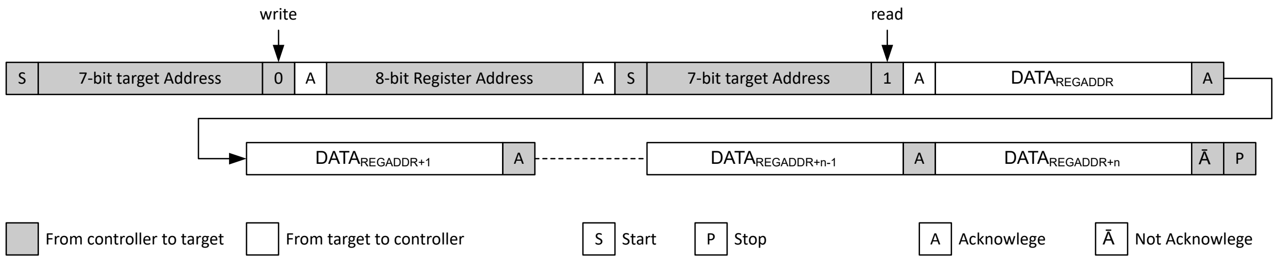


Figure 7-5. Sequential READ Starting From A Defined Register Address

7.7 Single WRITE to a Defined Register Address

Figure 7-6 shows the format of a single write to a defined register address. First, the Controller issues a start condition followed by a seven-bit I ^{2} C address. Next, the Controller writes a zero to signify that it wishes to conduct a write operation. Upon receiving an acknowledge from the Peripheral, the Controller sends the eight-bit register address across the bus. Following a second acknowledge the device sets the I ^{2} C register address to the defined value and the Controller writes the eight-bit data value. Upon receiving a third acknowledge the device auto increments the I ^{2} C register address by one and the Controller issues a stop condition. This action concludes the register write.

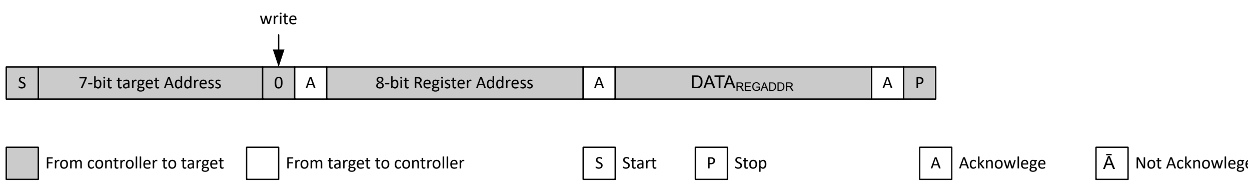


Figure 7-6. Single WRITE to Defined Register Address

7.8 Sequential WRITE Starting From A Defined Register Address

A sequential write operation is an extension of the single write protocol and shown in Figure 7-7 . If the Controller does not send a stop condition after the device has issued an ACK, the device auto increments the register address by one and the Controller writes to the next register.

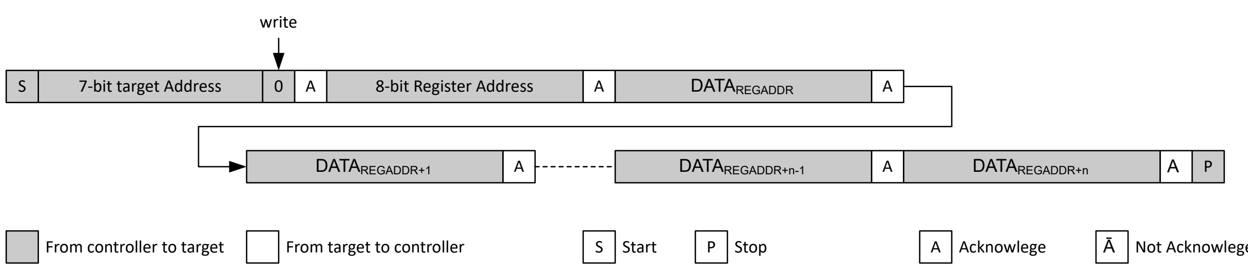


Figure 7-7. Sequential WRITE Starting At A Defined Register Address

7.9 REGFIELD Registers

Table 7-1 lists the memory-mapped registers for the REGFIELD registers. All register offset addresses not listed in Table 7-1 should be considered as reserved locations and the register contents should not be modified.

Table 7-1. REGFIELD Registers

Address	Acronym	Register Name	Section
3h	CLEAR_FAULTS	CLEAR_FAULTS	Section 7.9.1
78h	FAULT_STATUS	FAULT_STATUS	Section 7.9.2
D0h	DEVICE_STATUS_1	DEVICE_STATUS_1	Section 7.9.3
D1h	DEVICE_STATUS_2	DEVICE_STATUS_2	Section 7.9.4

Complex bit access types are encoded to fit into small table cells. Table 7-2 shows the codes that are used for access types in this section.

Table 7-2. REGFIELD Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.9.1 CLEAR_FAULTS Register (Address = 3h) [Reset = 00h]

CLEAR_FAULTS is shown in Table 7-3.

Return to the Summary Table.

Clear all latched status flags in 0x78 register

Table 7-3. CLEAR_FAULTS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLEAR_FAULTS	R/W	0h	Accessing the address is enough to clear fault

7.9.2 FAULT_STATUS Register (Address = 78h) [Reset = 00h]

FAULT_STATUS is shown in Table 7-4.

Return to the Summary Table.

Fault status

Table 7-4. FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IPK_FAULT	R	0h	IPK float detection 0h = no fault 1h = fault
6	VREF_FAULT	R	0h	VREF to VDD short detection 0h = no fault 1h = fault
5	BOOTUV1	R	0h	Boot UV (HB-SW undervoltage) Channel 1 0h = no fault 1h = fault
4	BOOTUV2	R	0h	Boot UV (HB-SW undervoltage) Channel 2 0h = no fault 1h = fault
3	ILIM1	R	0h	Current limit Channel 1 0h = no fault 1h = fault
2	ILIM2	R	0h	Current limit Channel 2 0h = no fault 1h = fault
1	OVP	R	0h	Overvoltage fault 0h = no fault 1h = fault
0	TSD	R	0h	Thermal shutdown fault 0h = no fault 1h = fault

7.9.3 DEVICE_STATUS_1 Register (Address = D0h) [Reset = 00h]

DEVICE_STATUS_1 is shown in Table 7-5.

Return to the Summary Table.

Informational bits about the part status

Table 7-5. DEVICE_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN1	R	0h	Channel 1 enable status 0h = Channel 1 disabled 1h = Channel 1 enabled
6	EN2	R	0h	Channel 2 enable status 0h = Channel 2 disabled 1h = Channel 2 enabled
5	DEM1	R	0h	Channel 1 DEM status 0h = Channel 1 FPWM 1h = Channel 1 DEM
4	DEM2	R	0h	Channel 2 DEM status 0h = Channel 2 FPWM 1h = Channel 2 DEM
3	DIR1	R	0h	DIR 1 status 0h = DIR1 low 1h = DIR1 high
2	DIR2	R	0h	DIR 2 status 0h = DIR2 low 1h = DIR2 high
1	DIR_INVALID1	R	0h	Invalid DIR1 command 0h = Valid DIR1 command 1h = Invalid DIR1 command
0	DIR_INVALID2	R	0h	Invalid DIR2 command 0h = Valid DIR2 command 1h = Invalid DIR2 command

7.9.4 DEVICE_STATUS_2 Register (Address = D1h) [Reset = 00h]

DEVICE_STATUS_2 is shown in Table 7-6.

Return to the Summary Table.

Informational bits about the part status

Table 7-6. DEVICE_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OSC_FAULT	R	0h	OSC short detection 0h = No OSC fault 1h = OSC fault
6	UVLO	R	0h	UVLO status 0h = Not in UVLO 1h = In UVLO (UVLO<2.5V)
5	OPT	R	0h	OPT pin status 0h = OPT low 1h = OPT high
4	SS1_DONE	R	0h	SS channel 1 completion status 0h = SS1 not done 1h = SS1 done
3	SS2_DONE	R	0h	SS channel 2 completion status 0h = SS2 not done 1h = SS2 done
2	SD	R	0h	SD/DT pin status 0h = Part not in SD 1h = Part in SD
1	ADAPT_DT	R	0h	Adaptive deadtime status 0h = No adaptive deadtime 1h = Adaptive deadtime
0	VCC_UV	R	0h	VCC UV status 0h = VCC not in UV 1h = VCC in UV

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

LM5171-Q1 is suitable for the bidirectional DC-DC converters for dual battery systems, and battery backup systems. LM5171-Q1 is easy to stack, phase interleaving and balanced current sharing is achieved among phases.

LM5171-Q1 uses average current mode control which is a two-loop system. LM5171-Q1 integrates two operational amplifiers to achieve HV voltage regulation and LV voltage regulation. Please note only one operational amplifier is enabled according to DIR1. External operational amplifiers is necessary for CH-2 in case of independent operation. The interface signals between the inner current loop and outer voltage loop are basically the DIR and ISET signals, of which the DIR signal controls the current direction, and the ISET signal carries the error information of the outer voltage loop.

8.1.1 Small Signal Model

The following describes the small signal model of inner current loop and outer voltage loop of LM5171-Q1. Some simplifications are made for better insight. And the compensation for the loops are also introduced.

LM5171-Q1 Design Calculator is also provided for the loop compensation.

8.1.1.1 Current Loop Small Signal Model

Figure 8-1 shows the current loop block diagram of each phase in buck mode. V_{HV} is the input while V_{LV} is the output.

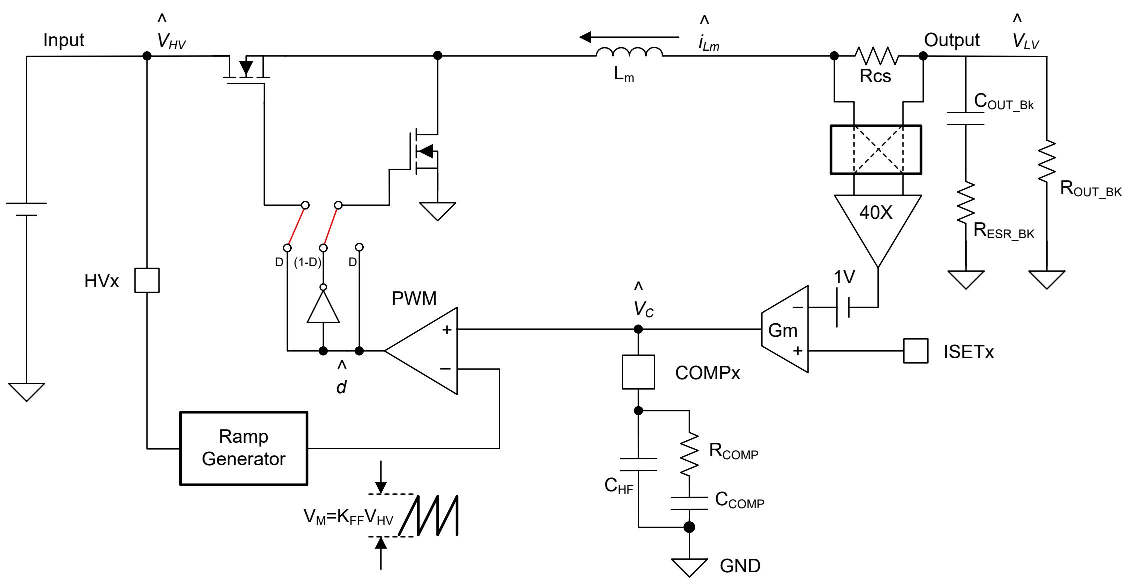


Figure 8-1. Buck Loop Block Diagram

The inner current loop is designed first. The average current-mode control loop of buck mode is modeled in Figure 8-2.

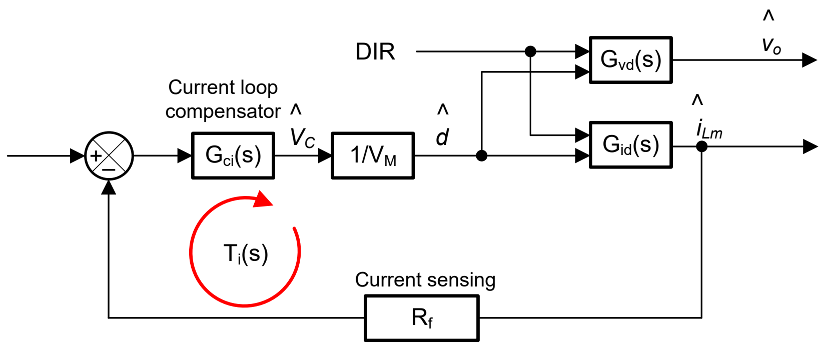


Figure 8-2. Current Loop Block Diagram

The buck mode duty cycle (d) to channel inductor current (i_{Lm}) transfer function is determined by the following:

$$G_{id\_BK}(s) = \frac{\hat{i}_{Lm}}{\hat{d}} = \frac{V_{HV}}{R_{OUT\_BK}} \times \frac{1 + \frac{s}{\omega_{Z\_il\_BK}}}{1 + \frac{s}{\omega_{0\_BK} \times Q_{BK}} + \frac{s^2}{\omega_{0\_BK}^2}} \tag{16}$$

where

$$R_{OUT\_BK} = \frac{V_{LV}}{n_p \times I_{Lmax}} \tag{17}$$

$$\omega_{Z\_il\_BK} = \frac{1}{R_{OUT\_BK} \times C_{OUT\_BK}} \tag{18}$$

$$\omega_{0\_BK} = \frac{1}{\sqrt{L_m \times C_{OUT\_BK}}} \tag{19}$$

$$Q_{BK} = \frac{1}{\omega_{0\_BK}} \times \frac{1}{\frac{L_m}{R_{OUT\_BK}} + \left(R_{ESR\_BK} + R_{CS} + R_S\right) \times C_{OUT\_BK}} \tag{20}$$

- L_m is the power inductor,
- R_{CS} is the current sense resistor,
- R_S is the equivalent total resistance along the current path excluding R_{CS},
- C_{OUT_BK} is the total output capacitance in buck mode.
- R_{ESR_BK} is the total output capacitor equivalent series resistance (ESR).

Figure 8-3 shows the current loop block diagram in boost mode. V_{LV} is the input while V_{HV} is the output.

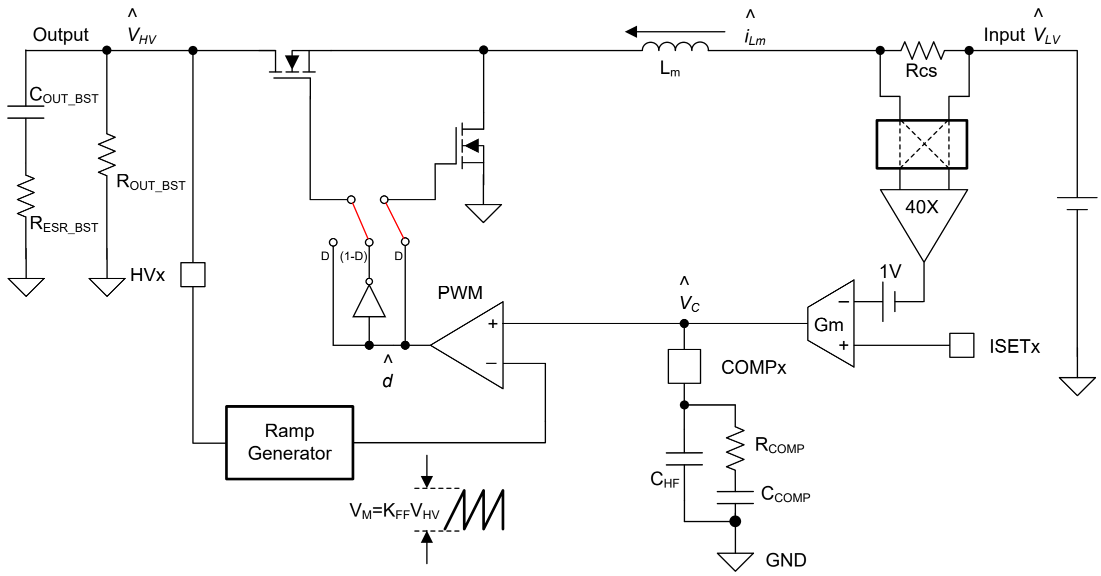


Figure 8-3. Boost Loop Block Diagram

The average current-mode control loop of boost mode is the same as buck as shown in Figure 8-2. But the transfer function of the boost power stage $G_{id}(s)$ and $G_{vd}(s)$ is different from that of buck power stage.

The boost mode duty cycle (d) to channel inductor current (i_{Lm}) transfer function is determined by the following:

$$G_{id\_BST}(s) = \frac{\hat{i}_{Lm}}{\hat{d}} = \frac{2 \times V_{LV}}{D'^3 \times R_{OUT\_BST}} \times \frac{1 + \frac{s}{\omega_{Z\_il\_BST}}}{1 + \frac{s}{\omega_{0\_BST} \times Q_{BST}} + \frac{s^2}{\omega_{0\_BST}^2}} \tag{21}$$

where

$$D' = \frac{V_{LV}}{V_{HV}} \tag{22}$$

$$R_{OUT\_BST} = \frac{{V_{HV}}^2}{V_{LV} \times I_{Lmax}} \tag{23}$$

$$\omega_{Z\_il\_BST} = \frac{2}{R_{OUT\_BST} \times C_{OUT\_BST}} \tag{24}$$

$$\omega_{0\_BST} = \frac{D'}{\sqrt{L_m \times C_{OUT\_BST}}} \tag{25}$$

$$Q_{BST} = \frac{D'}{\omega_{0\_BST}} \times \frac{1}{\frac{L_m}{D' \times R_{OUT\_BST}} + \frac{(R_{CS} + R_S) \times C_{OUT\_BST}}{D'} + R_{ESR\_BST} \times C_{OUT\_BST}} \tag{26}$$

- C_{OUT_BST} is the total output capacitance for each phase in boost mode.
- R_{ESR_BST} is the total output capacitor equivalent series resistance (ESR) for each phase in boost mode.

When we select the current loop cross over frequency at 1/6 of switching frequency, $G_{id\_BK}(s)$ is simplified. For the numerator, $s \times R_{OUT\_BK} \times C_{OUT\_BK}$ dominates. And for the denominator, $s^2/{\omega_{0\_BK}}^2$ dominates. Equation 16 is simplified as:

$$G_{id\_BK}(s) = \frac{V_{HV}}{R_{OUT\_BK}} \times \frac{1 + \frac{s}{\omega_{Z\_il\_BK}}}{\frac{s^2}{\omega_{0\_BK}{}^2}} = \frac{V_{HV}}{s \times L_m} \tag{27}$$

Similarly, Equation 21 is simplified as:

$$G_{id\_BST}(s) = \frac{2 \times V_{LV}}{D'^3 \times R_{OUT\_BST}} \times \frac{\frac{s}{\omega_{Z\_il\_BST}}}{\frac{s^2}{\omega_{0\_BST}{}^2}} = \frac{V_{HV}}{s \times L_m} \tag{28}$$

From Equation 27 and Equation 28, the same duty cycle (d) to channel inductor current (i_{Lm}) transfer function is shared by both buck and boost mode:

$$G_{id}(s) = \frac{V_{HV}}{s \times L_m} \tag{29}$$

So compensator for buck current loop and boost current loop is also shared.

8.1.1.2 Current Loop Compensation

Equation 29 indicates that the power plant is basically a first-order system. A Type-II compensator as shown in Figure 8-1 is adequate to stabilize the loop for both buck and boost mode operations.

Assuming the output impedance of the gm amplifier is R_{GM}, the current loop compensation gain is determined by :

$$G_{ci}(s) = G_m \times \left[R_{GM} \| Z_{comp}(s)\right] \tag{30}$$

where

- A_{CS} is the current sense amplifier gain, that is 40;
- G_m is the trans-conductance of the gm error amplifier, which is 100µA/V;
- $Z_{COMP}(s)$ is the equivalent impedance of the compensation network seen at the COMP pin (see Figure 8-1)

$$Z_{COMP}(s) = \frac{1}{C_{HF} + C_{COMP}} \times \frac{1 + s \times R_{COMP} \times C_{COMP}}{s \times \left(1 + s \times R_{COMP} \times \frac{C_{HF} \times C_{COMP}}{C_{HF} + C_{COMP}}\right)} \tag{31}$$

Considering C_{HF} << C_{COMP}, Equation 31 is simplified to :

$$Z_{COMP}(s) = \frac{1}{C_{COMP}} \times \frac{1 + s \times R_{COMP} \times C_{COMP}}{s \times (1 + s \times R_{COMP} \times C_{HF})} \tag{32}$$

Because R_{GM} is > 5MegΩ, and the frequency range for loop compensation is usually above a few kHz, the effects of R_{GM} on the loop gain in the interested frequency range becomes negligible. Therefore, substituting Equation 32 into Equation 30, and neglecting R_{GM},

$$G_{ci}(s) = \frac{G_m}{C_{COMP}} \times \frac{1 + s \times R_{COMP} \times C_{COMP}}{s \times (1 + s \times R_{COMP} \times C_{HF})} \tag{33}$$

From Figure 8-2, the open-loop gain of the inner current loop is:

$$T_i(s) = G_{ci}(s) \times \frac{1}{V_M} \times G_{id}(s) \times R_f \tag{34}$$

where

$$V_M = V_{HV} \times K_{FF} \tag{35}$$

$$R_f = R_{CS} \times A_{CS} \tag{36}$$

- K_{FF} is the ramp generator coefficient. For LM5171-Q1, K_{FF}=0.03125.

Substituting Equation 33 and Equation 29 into Equation 34, $T_i(s)$ is found as:

$$T_i(s) = \frac{1}{s \times K_{FF} \times L_m} \times \frac{R_f \times G_m}{C_{COMP}} \times \frac{1 + s \times R_{COMP} \times C_{COMP}}{s \times (1 + s \times R_{COMP} \times C_{HF})} \tag{37}$$

The poles and zeros of the total loop transfer function are determined by:

$$f_{p1} = 0 \tag{38}$$

$$f_{p2} = \frac{1}{2\pi \times R_{COMP} \times C_{HF}} \tag{39}$$

$$f_z = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}} \tag{40}$$

To tailor the total inner current loop gain to crossover at f_{CI}, select the components of the compensation network according to the following guidelines, then fine tune the network for optimal loop performance.

1. The zero f_z is placed at around 1/5 of target crossover frequency f_{CI},
2. The pole f_{p2} is placed at approximately 1/2 of switching frequency f_{SW},
3. The total open-loop gain is set to unity at f_{CI}, namely,

$$|T_i(2i \times \pi \times f_{CI})| = 1 \tag{41}$$

Therefore, the compensation components are derived from the above equations, as shown in Equation 42.

$$\begin{cases} R_{COMP} = \dfrac{K_{FF}}{A_{CS} \times R_{CS} \times G_m} \times |2i \times \pi \times f_{CI} \times L_m| \\ C_{COMP} = \dfrac{1}{\left|2i \times \pi \times \frac{f_{CI}}{5} \times R_{COMP}\right|} \\ C_{HF} = \dfrac{1}{\left|2i \times \pi \times \frac{f_{SW}}{2} \times R_{COMP}\right|} \end{cases} \tag{42}$$

8.1.1.3 Voltage Loop Small Signal Model

When the current loop compensator is designed, the outer voltage loop is then analyzed.

A system with n_p phases is shown in Figure 8-4.

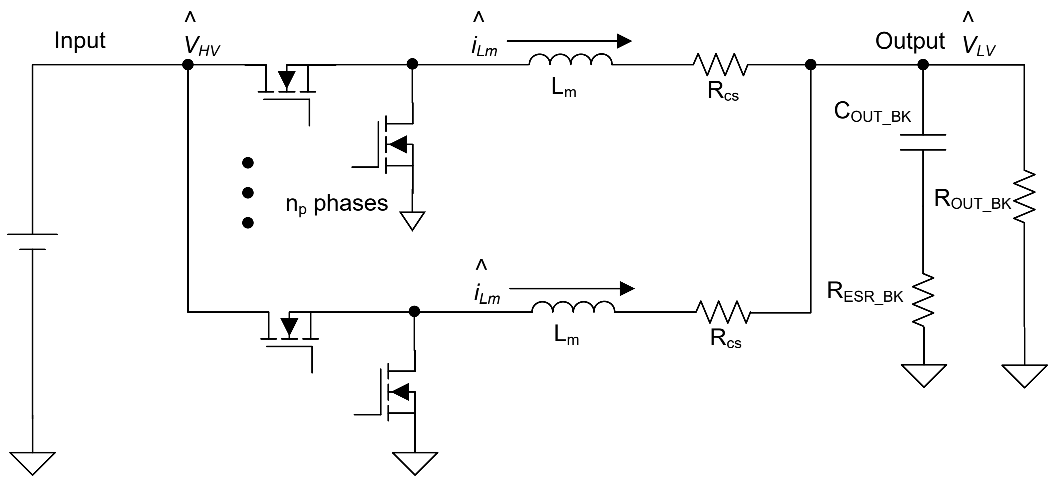


Figure 8-4. n_p phases system

The equivalent inductance and resistance are determined by

$$L_{mnp} = \frac{L_m}{n_p} \tag{43}$$

$$R_{Snp} = \frac{R_S}{n_p} \tag{44}$$

$$R_{CSnp} = \frac{R_{CS}}{n_p} \tag{45}$$

$$R_{fnp} = \frac{R_f}{n_p} \tag{46}$$

The buck mode duty cycle (d) to n_p phases inductor current transfer function is determined by the following:

$$G_{idnp\_BK}(s) = \frac{n_p \times \hat{i}_{Lm}}{\hat{d}} = \frac{V_{HV}}{R_{OUT\_BK}} \times \frac{1 + \frac{s}{\omega_{Z\_il\_BK}}}{1 + \frac{s}{\omega_{0np\_BK} \times Q_{npBK}} + \frac{s^2}{\omega_{0np\_BK}^2}} \tag{47}$$

where

$$R_{OUT\_BK} = \frac{V_{LV}}{n_p \times I_{Lmax}} \tag{48}$$

$$\omega_{Z\_il\_BK} = \frac{1}{R_{OUT\_BK} \times C_{OUT\_BK}} \tag{49}$$

$$\omega_{0np\_BK} = \frac{1}{\sqrt{L_{mnp} \times C_{OUT\_BK}}} \tag{50}$$

$$Q_{npBK} = \frac{1}{\omega_{0np\_BK}} \times \frac{1}{\frac{L_{mnp}}{R_{OUT\_BK}} + \left(R_{ESR\_BK} + R_{CSnp} + R_{Snp}\right) \times C_{OUT\_BK}} \tag{51}$$

For n_p phase, the equivalent open loop gain $T_{inp}(s)$ is obtained as

$$T_{inp}(s) = G_{ci}(s) \times \frac{1}{V_M} \times G_{id}(s) \times R_{fnp} \tag{52}$$

where

Figure 8-5 shows the outer voltage control loop and inner current loop.

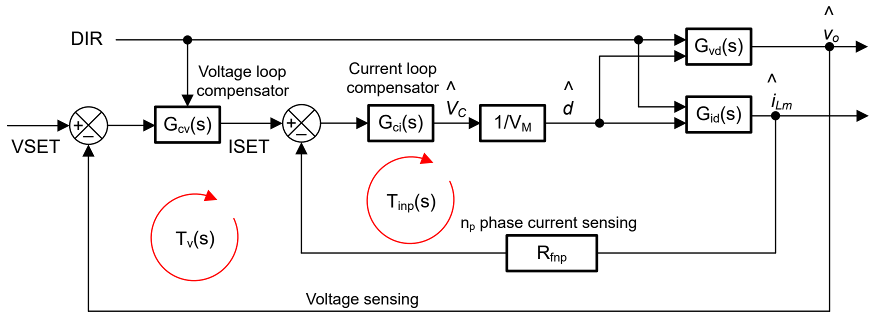


Figure 8-5. Voltage Loop and Current Loop Block Diagram

The ISET to output voltage (v_O) close loop transfer function is obtained as:

$$G_{vs}(s) = \frac{\hat{v}_{LV}}{\hat{v}_{ISET}} = \frac{G_{ci}(s) \times \frac{1}{V_M} \times G_{vd}(s)}{1 + T_{inp}(s)} \tag{53}$$

When selecting the crossover frequency of the buck voltage loop lower than the current loop crossover frequency, $G_{vs}(s)$ is simplified. For the denominator, $T_{inp}(s)$ dominates, Equation 53 is written as:

$$G_{vs}(s) = \frac{\hat{v}_{LV}}{\hat{v}_{ISET}} = \frac{G_{ci}(s) \times \frac{1}{V_M} \times G_{vd}(s)}{T_{inp}(s)} = \frac{G_{vd}(s)}{G_{id}(s) \times R_{fnp}} \tag{54}$$

The buck power plant duty cycle (d) to output voltage (v_{LV}) transfer function is determined by :

$$G_{vd\_BK}(s) = \frac{\hat{v}_{LV}}{\hat{d}} = V_{HV} \times \frac{1 + \frac{s}{\omega_{Z\_vl\_BK}}}{1 + \frac{s}{\omega_{0np\_BK} \times Q_{npBK}} + \frac{s^2}{\omega_{0np\_BK}^2}} \tag{55}$$

where

$$\omega_{Z\_vl\_BK} = \frac{1}{R_{ESR\_BK} \times C_{OUT\_BK}} \tag{56}$$

Substituting Equation 55 into Equation 54, a simplified ISET to output voltage (V_{LV}) transfer function is determined by the following:

$$G_{vs\_BK}(s) = \frac{\hat{v}_{LV}}{\hat{v}_{ISET}} = K_{dc\_BK} \times \frac{1 + \frac{s}{\omega_{Z\_vl\_BK}}}{1 + \frac{s}{\omega_{Z\_il\_BK}}} \tag{57}$$

where

$$K_{dc\_BK} = \frac{R_{OUT\_BK}}{R_{fnp}} \tag{58}$$

Similarly, the boost power plant duty cycle (d) to output voltage (v_{HV}) transfer function is determined by :

$$G_{vd\_BST}(s) = \frac{\hat{v}_{HV}}{\hat{d}} = \frac{V_{LV}}{D'^2} \times \frac{\left(1 + \frac{s}{\omega_{Z\_vl\_BST}}\right)\left(1 - \frac{s}{\omega_{RHPZ}}\right)}{1 + \frac{s}{\omega_{0np\_BST} \times Q_{npBST}} + \frac{s^2}{\omega_{0np\_BST}^2}} \tag{59}$$

where

$$\omega_{Z\_vl\_BST} = \frac{1}{R_{ESR\_BST} \times C_{OUT\_BST}} \tag{60}$$

$$\omega_{RHPZ} = \frac{R_{OUT\_BST} \times D'^2}{L_{mnp}} \tag{61}$$

Substituting Equation 59 into Equation 54, a simplified ISET to output voltage (V_{HV}) transfer function is determined by the following:

$$G_{vs\_BST}(s) = \frac{\hat{v}_{HV}}{\hat{i}_{set}} = K_{dc\_BST} \times \frac{\left(1 + \frac{s}{\omega_{Z\_vl\_BST}}\right)\left(1 - \frac{s}{\omega_{RHPZ}}\right)}{1 + \frac{s}{\omega_{Z\_il\_BST}}} \tag{62}$$

where

$$K_{dc\_BST} = \frac{R_{OUT\_BST} \times D'}{2 \times R_{fnp}} \tag{63}$$

8.1.1.4 Voltage Loop Compensation

The typical bi-directional application with HV voltage regulation and LV voltage regulation is shown in Figure 8-6. Connect the error voltage of the outer voltage loop error amplifiers (ERRHV and ERRLV) to ISETx as the reference for the inner current loop.

The outer voltage loop crossover frequency f_{CV} needs to be one decade below that of the inner current loop crossover frequency f_{CI}. And boost outer voltage loop crossover frequency also needs to be below 1/5 of the Right-Half-Plane Zero (RHPZ).

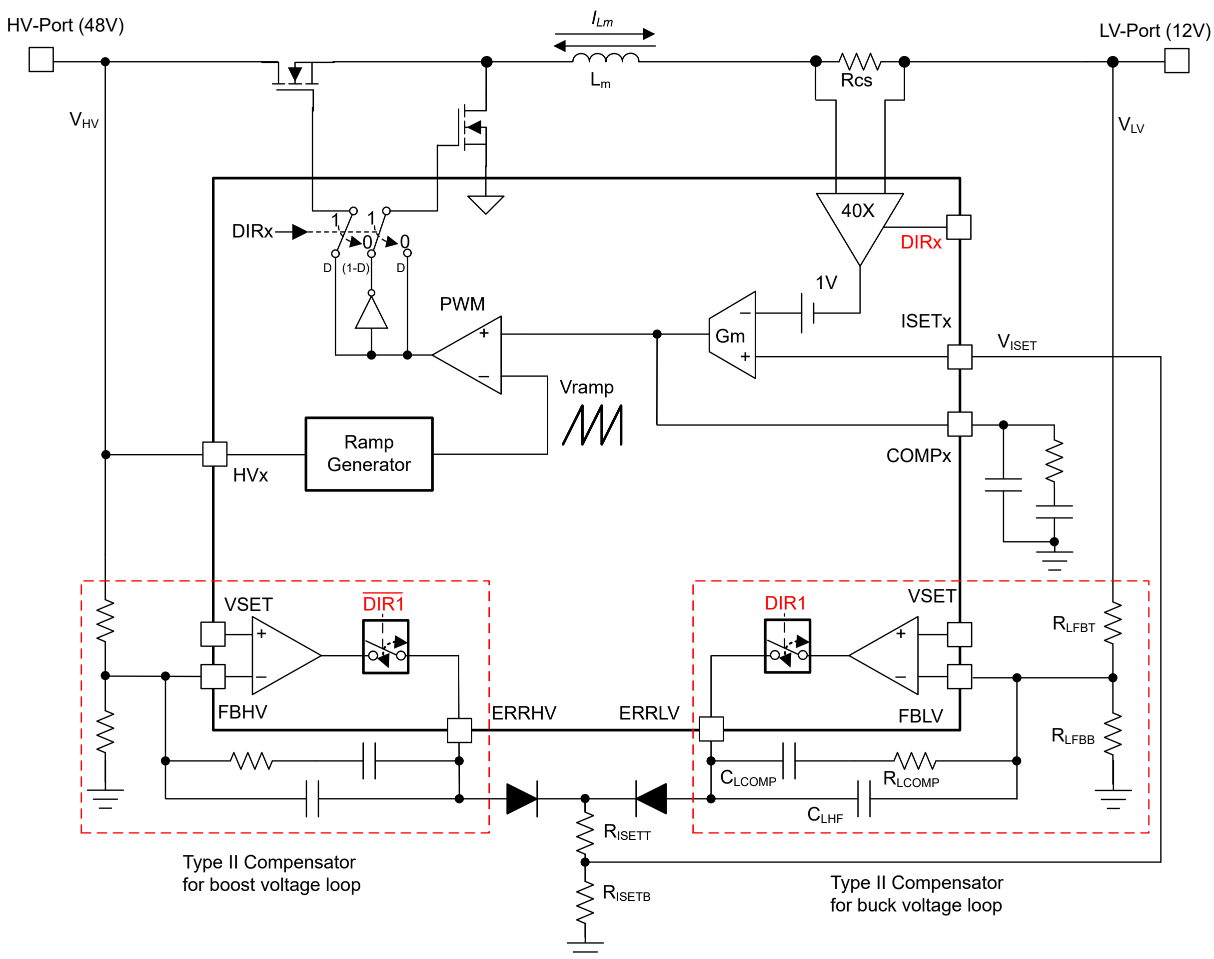


Figure 8-6. Outer Voltage Loop Control

Type-II compensator as shown in Figure 8-6 is recommended to stabilize the voltage loop for both buck and boost mode operations.

Buck mode compensation is analyzed as an example. The transfer function of the compensator of buck mode is found as:

$$G_{cv}(s) = \frac{\hat{v}_{ISET}}{\hat{v}_{LV}} \approx \frac{A_{VM} \times \omega_{ZEA}}{s} \times \frac{1 + \frac{s}{\omega_{ZEA}}}{1 + \frac{s}{\omega_{HF}}} \times K_{ISET} \tag{64}$$

where

$$A_{VM} \approx \frac{R_{LCOMP}}{R_{LFBT}} \tag{65}$$

$$\omega_{ZEA} = \frac{1}{R_{LCOMP} \times C_{LCOMP}} \tag{66}$$

$$\omega_{HF} \approx \frac{1}{R_{LCOMP} \times C_{LHF}} \tag{67}$$

$$K_{ISET} = \frac{R_{ISETB}}{R_{ISETT} + R_{ISETB}} \tag{68}$$

The total open-loop gain of the outer voltage loop of buck mode $T_{v\_BK}(s)$ is the product of $G_{vs\_BK}(s)$ and $G_{cv}(s)$:

$$T_{v\_BK}(s) = G_{vs\_BK}(s) \times G_{cv}(s) \tag{69}$$

Or:

$$T_{v\_BK}(s) = K_{dc\_BK} \times \frac{1 + \frac{s}{\omega_{Z\_vl}}}{1 + \frac{s}{\omega_{Z\_il}}} \times \frac{A_{VM} \times \omega_{ZEA}}{s} \times \frac{1 + \frac{s}{\omega_{ZEA}}}{1 + \frac{s}{\omega_{HF}}} \times K_{ISET} \tag{70}$$

To tailor the total outer voltage loop gain to crossover at f_{CV}, select the components of the compensation network according to the following guidelines, then fine tune the network for optimal loop performance.

1. Choose a value for R_{LFBT} based on the bias current and power dissipation,
2. The zero ω_{ZEA} is placed around 1/5 of target crossover frequency f_{CV},
3. The pole ω_{HF} is placed at approximately 10 times of f_{CV},
4. The total open-loop gain is set to unity at f_{CV}, namely,

$$\left|T_{v\_BK}(2i \times \pi \times f_{CV})\right| = 1 \tag{71}$$

Therefore, the compensation components are derived from the above equations as:

$$\begin{cases} R_{LCOMP} = \dfrac{R_{LFBT}}{K_{dc\_BK} \times \left| \dfrac{1 + \frac{2i \times \pi \times f_{CV}}{\omega_{Z\_vl}}}{1 + \frac{2i \times \pi \times f_{CV}}{\omega_{Z\_il}}} \right| \times K_{ISET}} \\ C_{LCOMP} = \dfrac{1}{\left|2i \times \pi \times \frac{f_{CV}}{5} \times R_{COMP}\right|} \\ C_{LHF} = \dfrac{1}{\left|2i \times \pi \times 10 \times f_{CV} \times R_{COMP}\right|} \end{cases} \tag{72}$$

The compensator of boost voltage loop is designed similarly. Please note that boost voltage loop crossover frequency also needs to be below 1/5 of the RHPZ.

8.2 PWM to ISET Pins

For digital application using PWM signals, an external two-stage RC filter is recommended to convert the PWM signal to a DC voltage feeding the ISET pin as shown in Figure 8-7. A two stage RC filter requires much smaller capacitance, and has a shorter delay time compared to a single stage filter. Please note, conversion errors occur if the PWM signal voltage levels are not well regulated.

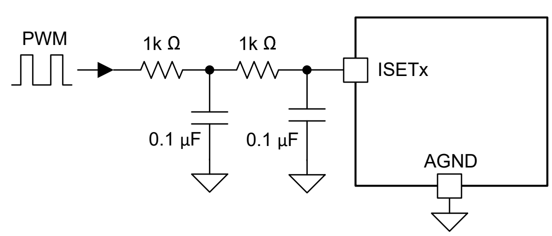


Figure 8-7. Two-Stage RC Filter to Convert the PWM into an Analog Voltage at the ISETx Pin

8.3 ISET Clamp

Clamp the ISETx voltage to limit the average current. .

ISET clamp with TLV431 is shown in Figure 8-8. The resistor divider set the ISET clamp voltage.

ISET clamp with op amp is shown in Figure 8-9. ISET voltage is clamped to ISET_max.

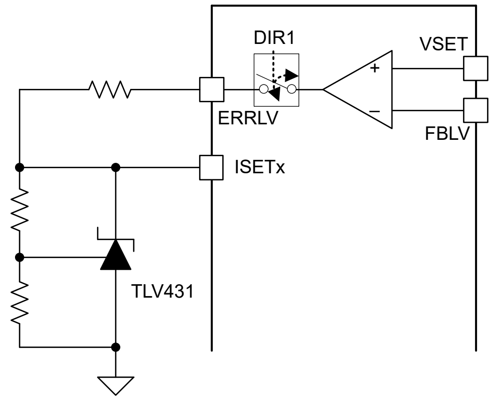


Figure 8-8. ISET Clamp with TLV431

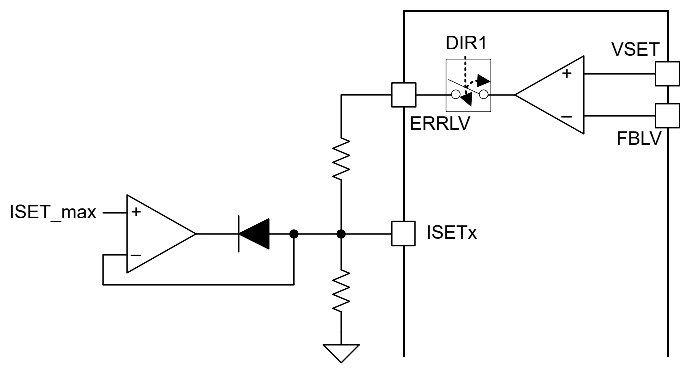


Figure 8-9. ISET Clamp with Op Amp

8.4 Dynamic Dead Time Adjustment

In addition to a fixed dead time programming by R_{DT}, the dead time is dynamically adjusted either by applying an analog voltage or a PWM signal as shown in Figure 8-10. Varying the analog voltage or the duty ratio of the PWM signal adjusts the DT programming. For analog adjustment, a single stage RC filter is recommended to filter out any possible noise. For PWM adjustment, a two-stage RC filter is recommended to minimize the ripple voltage resulted on the DT pin.

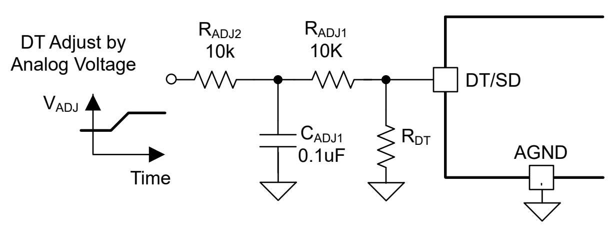


Figure 8-10. Dynamic Dead Time Adjustment a

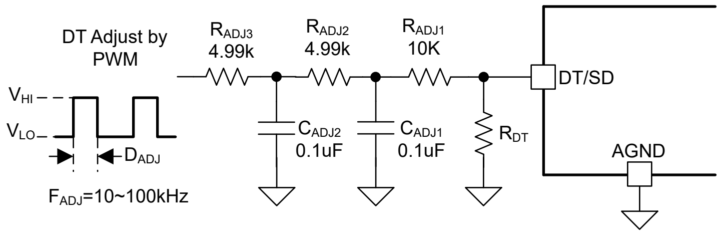


Figure 8-11. Dynamic Dead Time Adjustment b

When an analog voltage is applied, the resulted dead time is determined by Equation 73:

$$t_{DT}(V_{ADJ}) = \left(\frac{1}{R_{DT}} + \frac{1}{R_{ADJ1} + R_{AJD2}} - \frac{0.8 \times V_{ADJ}}{R_{ADJ1} + R_{AJD2}}\right)^{-1} \times 2.625\frac{ns}{k\Omega} \quad (73)$$

where

- V_{ADJ} is the analog voltage used to adjust the dead time

When a PWM signal is applied, the resulted dead time is determined by Equation 74:

$$t_{DT}(D_{ADJ}) = \left(\frac{1}{R_{DT}} + \frac{1}{R_{ADJ1} + R_{AJD2} + R_{AJD3}} - \frac{0.8 \times \left[(V_{HI} - V_{LO}) \times D_{ADJ} + V_{LO}\right]}{R_{ADJ1} + R_{AJD2} + R_{AJD3}}\right)^{-1} \times 2.625\frac{ns}{k\Omega} \quad (74)$$

where

- V_{HI} and V_{LO} are the high and low voltage levels of the PWM signal, respectively,
- D_{ADJ} is the duty factor of the PWM signal.

Note that in dynamic dead time programming, the equivalent impedance at the DT /SD pin seen by the IC needs to be greater than 5 kΩ to prevent unintended shutdown latch. See Section 6.3.13 for details.

8.5 Proper Termination of Unused Pins

In applications where the error amplifier, LDODRV or I2C is not used, follow Figure 8-12 for proper termination of unused pins.

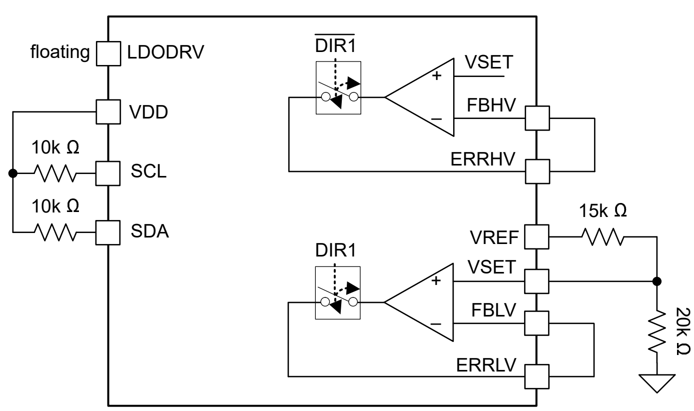


Figure 8-12. Proper Termination of Unused Pins

8.6 Typical Application

8.6.1 60A, Dual-Phase, 48V to 12V Bidirectional Converter

A typical application example is a 60A, dual-phase bidirectional converter as shown in Figure 8-13. The HV-Port voltage range is 32V to 70V and the LV-Port 0V to 23V. Each phase is able to deliver $30A_{DC}$ current through the inductor.

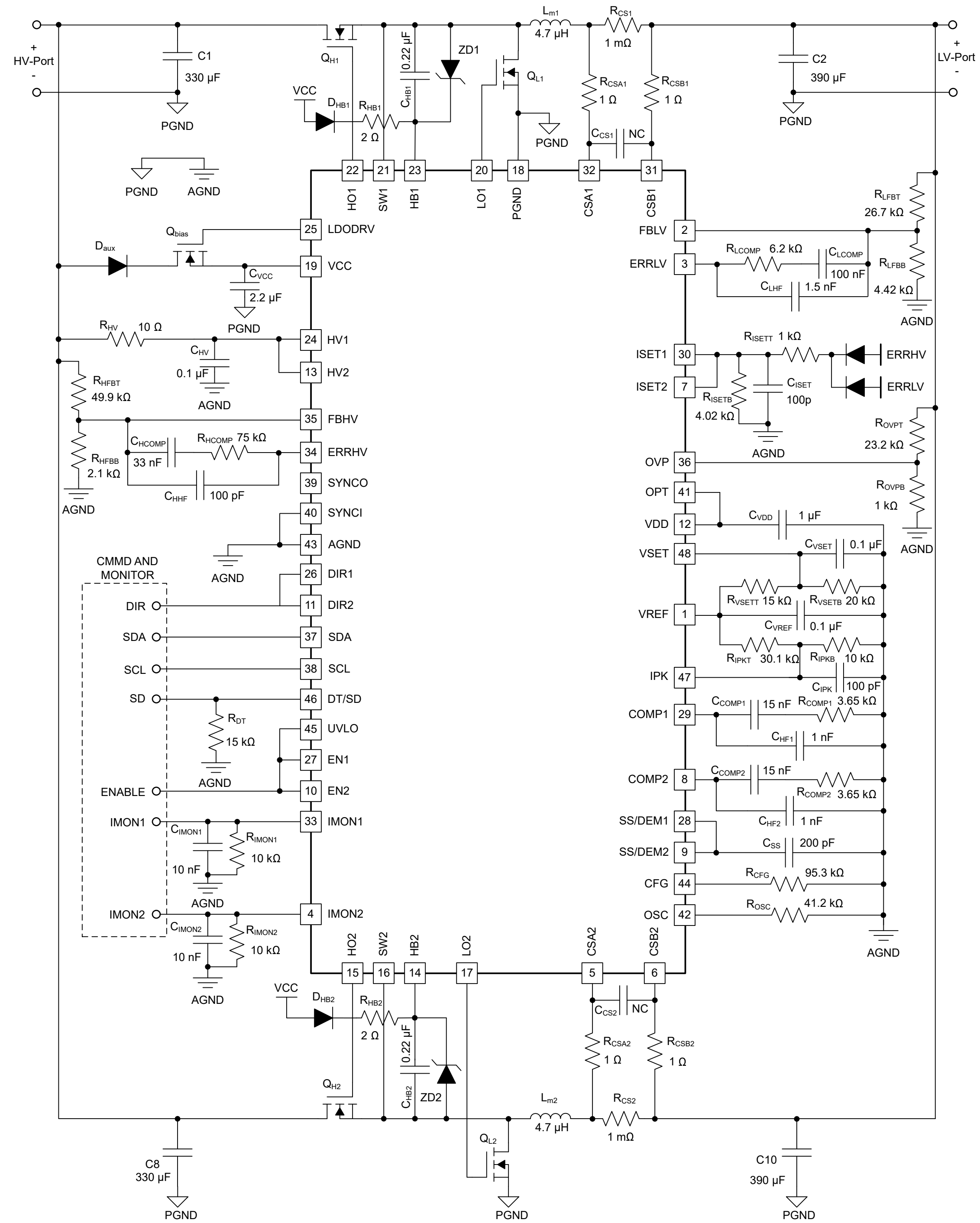


Figure 8-13. Schematic of the Example Dual-Phase Bidirectional Converter

8.6.1.1 Design Requirements

Table 8-1 lists the design parameters for this example.

Table 8-1. Design Parameters

PARAMETER	EXAMPLE VALUE	NOTE
V_{LV_min}	6V	LV-Port minimum operating voltage
V_{LV_reg}	14V	LV-Port nominal voltage
V_{LV_max}	23V	LV-Port maximum operating voltage
V_{HV_min}	32V	HV-Port minimum operating voltage
V_{HV_reg}	50V	HV-Port nominal operating voltage
V_{HV_max}	70V	HV-Port maximum operating voltage
F_{SW}	100kHz	Switching frequency
I_{Lmax}	30A	Maximum average inductor current for each channel
I_{total}	60A	Total bidirectional DC at the LV-Port

8.6.1.2 Detailed Design Procedure

8.6.1.2.1 Determining the Duty Cycle

Obviously, the duty cycles are determined by Equation 75 through Equation 78:

$$D_{BK\_min} = \frac{V_{LV\_reg}}{V_{HV\ max}} = \frac{14\ V}{70\ V} = 0.2 \tag{75}$$

$$D_{BK\_max} = \frac{V_{LV\_reg}}{V_{HV\ min}} = \frac{14\ V}{32\ V} = 0.438 \tag{76}$$

$$D_{BST\_min} = \frac{V_{HV\_reg} - V_{LV\_max}}{V_{HV\_reg}} = \frac{50\ V - 23\ V}{50\ V} = 0.54 \tag{77}$$

$$D_{BST\_max} = \frac{V_{HV\_reg} - V_{LV\_min}}{V_{HV\_reg}} = \frac{50\ V - 6\ V}{50\ V} = 0.88 \tag{78}$$

8.6.1.2.2 Oscillator Programming (OSC)

To operate the converter at the desired switching frequency F_{SW}, select the R_{OSC} by satisfying Equation 14:

$$R_{osc} = \frac{41.5k\Omega \times 100kHz}{F_{osc}} = 41.5k\Omega \tag{79}$$

Choose standard resistor R_{OSC} = 41.2kΩ.

8.6.1.2.3 Power Inductor, RMS and Peak Currents

The inductor current has a triangle waveform, as shown in Effects of Parasitic Inductance on the Current Sense Signal and Zero Crossing Detection. TI recommends selecting an inductor such that its peak-to-peak ripple current is less than 80% of the channel inductor full load DC current. Therefore, the inductor needs to satisfy Equation 80:

$$L_m \geq \frac{V_{LV\_reg} \times \left(1 - D_{BK\_min}\right)}{80\% \times I_{max} \times F_{sw}} = \frac{14\ V \times (1 - 0.2)}{0.8 \times 30\ A \times 100\ kHz} = 4.67\ \mu H \tag{80}$$

Select L_m = 4.7µH.

Then, the actual inductor peak to peak inductor current is determined by Equation 81:

$$I_{pk-pk} = \frac{V_{LV\_reg} \times (1 - D_{BK\_min})}{L_m \times F_{sw}} = \frac{14\ V \times (1 - 0.2)}{4.7\ \mu H \times 100\ kHz} = 23.83\ A \tag{81}$$

The peak inductor current is determined by Equation 82:

$$I_{peak} = I_{max} + \frac{I_{pk-pk}}{2} = 30\ A + \frac{23.83}{2} = 41.9\ A \tag{82}$$

Select an inductor that has a saturation current I_{sat} at least 20% greater than I_{peak} to allow full power with adequate margin. In this example, TI recommends selecting an inductor of I_{sat} > 49A.

The power inductor full load Root Mean Square (RMS) current I_{LM_RMS} determines its conduction losses. The RMS current is given by Equation 83:

$$I_{Lm\_RMS} = \sqrt{I_{max}^2 + \frac{1}{12} \times I_{pk-pk}^2} = 30.8\ \text{A} \quad (83)$$

8.6.1.2.4 Current Sense (R_{CS})

To achieve the highest regulation accuracy over wider load range, the user needs to target to create 50mV of V_{CS} at full current. Therefore, R_{CS} is selected as Equation 84:

$$R_{CS} \le \frac{50\ \text{mV}}{I_{max}} = \frac{50\ \text{mV}}{30\ \text{A}} = 1.667\ \text{m}\Omega \quad (84)$$

Owing to availability, a standard non-inductive 1mΩ current sense resistor is selected,

$$R_{CS} = 1.0\ \text{m}\Omega \quad (85)$$

Wide terminal chip resistors are recommended for minimized parasitic inductance. For low ohmic value resistors, 4-terminal current sense resistors are suggested for best accuracy.

Reserve room for some ceramic capacitors for possible noise filtering as shown in Figure 8-14. C_{CS1} and C_{CS2} filter out differential-mode noise, 100pF ceramic capacitors at each current sense pin filter out common-mode noise.

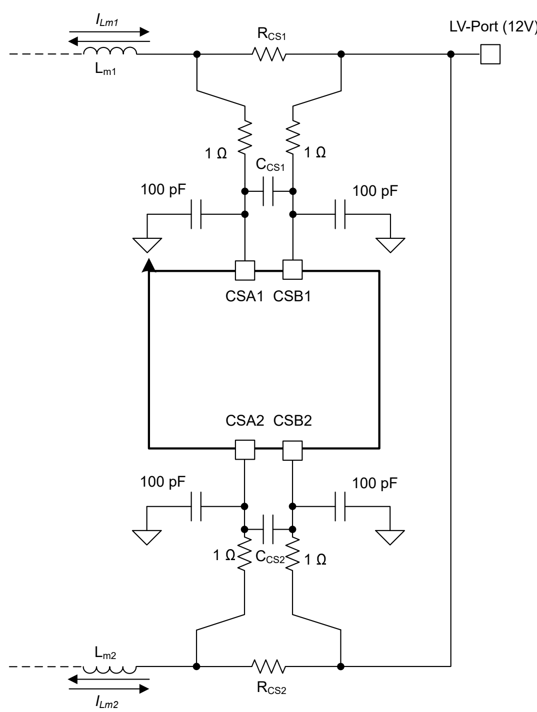


Figure 8-14. Current Sense With RC filter

8.6.1.2.5 Current Setting Commands (ISETx)

TI recommends setting a hard limit for the ISETx signal such that the converter is not over driven by an errant current setting signal. Assume the converter is allowed up to 10% overloading current. Refer to Channel Current Setting Commands (ISET1 and ISET2), the analog current setting signal ISETx needs to be limited by the following voltage level:

$$V_{ISET\_max} = \frac{110\% \times \text{Imax} \times R_{CS}}{G_{ISET}} + 1\text{V} = \frac{110\% \times 30\text{A} \times 1\text{m}\Omega}{0.025} + 1\text{V} = 2.32\text{V} \quad (86)$$

As shown in Figure 8-6, R_{ISETT} and R_{ISETB} are used to limit the maximum voltage on ISETx.

TLV431 or op amp are used to clamp the ISETx voltage in a precise way as shown in ISET Clamp.

8.6.1.2.6 Peak Current Limit (IPK)

One purpose of the peak current limit is to protect the power inductor from saturation. Program V_{IPK} such that the peak current limit threshold is 5% greater than I_{peak}. According to Equation 9 , one gets:

$$V_{IPK} = \frac{105\% \times I_{peak} \times R_{CS}}{G_{IPK}} = \frac{105\% \times 41.9A \times 1m\Omega}{0.05} = 0.880V \tag{87}$$

Select R_{IPKB} = 10kΩ and R_{IPKT} = 30.1kΩ which results in V_{IPK} = 0.873V, corresponding to a nominal peak inductor current limit of 43.6A per channel.

8.6.1.2.7 Power MOSFETS

The power MOSFETs need to be chosen with a V_{DS} rating capable of withstanding the maximum HV-port voltage plus transient spikes (ringing). 100V rated MOSFETs is selected in this application.

When the voltage rating is determined, select the MOSFETs by making tradeoffs between the MOSFET $R_{ds(ON)}$ and total gate charge Qg to balance the conduction and switching losses. For high power applications, parallel MOSFETs to share total power and reduce the dissipation on any individual MOSFET, hence relieving the thermal stress. The conduction losses in each MOSFET is determined by Equation 88.

$$P_{Q\_cond} = \frac{1.8 \times R_{ds(ON)}}{N} \times I_{Q\_RMS}^2 \tag{88}$$

where

- N is the number of MOSFETs in parallel
- 1.8 is the approximate temperature coefficient of the $R_{ds(ON)}$ at 125 °C
- and the total RMS switch current I_{Q_RMS} is approximately determined by Equation 89

$$I_{Q\_RMS} \approx \sqrt{D_{max}} \times I_{max} = \sqrt{D_{max}} \times I_{max} \tag{89}$$

where

- D_{max} is the maximum duty cycle, either in the buck mode or boost mode.

The switching transient rise and fall times are approximately determined by:

$$\Delta t_{rise} \approx \frac{N \times Q_g}{4\ A} \tag{90}$$

$$\Delta t_{fall} \approx \frac{N \times Q_g}{5\ A} \tag{91}$$

And the switching losses of each of the paralleled MOSFETs are approximately determined by:

$$P_{Q\_sw} = \frac{1}{2} \times C_{oss} \times V_{HV}^2 \times F_{sw} + \frac{1}{2} \times \frac{I_{peak}}{N} \times V_{HV} \times (\Delta t_{rise} + \Delta t_{fall}) \times F_{sw} \tag{92}$$

where

- C_{oss} is the output capacitance of the MOSFET.

The power MOSFET usually requires a gate-to-source resistor of 10kΩ to 100kΩ to mitigate the effects of a failed gate drive. When using parallel MOSFETs, a good practice is to use 1 to 2Ω gate resistor for each MOSFET, as shown in Figure 8-15.

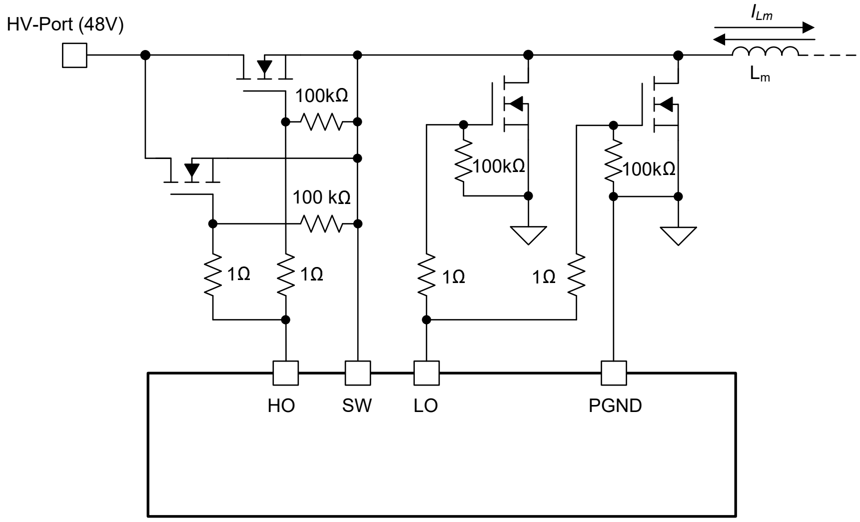


Figure 8-15. Paralleled MOSFET Configuration

If the dead time is not optimal, the body diode of the power synchronous rectifier MOSFET causes losses in reverse recovery. Assuming the reverse recovery charge of the power MOSFET is Q_{rr}, the reverse recovery losses are thus determined by Equation 93:

$$P_{Q\_rr} = Q_{rr} \times V_{HV\_max} \times F_{sw} \tag{93}$$

To reduce the reverse recovery losses, an optional Schottky diode is placed in parallel with the power MOSFETs. The diode needs to have the same voltage rating as the MOSFET, and it needs to be placed directly across the MOSFETs drain and source. The peak repetitive forward current rating needs to be greater than I_{peak}, and the continuous forward current rating needs to be greater than the following Equation 94:

$$I_{SD\_avg} = I_{peak} \times t_{DT} \times F_{sw} \tag{94}$$

8.6.1.2.8 Bias Supply

The total load current of the bias supply is mainly determined by the total MOSFET gate charge Qg. Assume the system employs multiple LM5171-Q1s to implement M number of phases, and each phase uses N number of MOSFETs in parallel as one switch. There are 2× N MOSFETs per phase to drive. Then the total current to drive these MOSFETs through VCC bias supply is determined by Equation 95.

$$I_{VCC} = 2 \times M \times N \times Q_g \times F_{sw} + M \times 5\text{ mA} \tag{95}$$

where

- 5mA is the worst case maximum current used by the control logic circuit of each phase.

In an example of a four-phase system employing two parallel MOSFETs for one switch, where M = 4, N = 2, Q_g = 100nC, and F_{sw} = 100KHz, the bias supply needs to be able to support at least the following total load current:

$$I_{VCC} \geq 2 \times 4 \times 2 \times 100\text{ nC} \times 100\text{ kHz} + 4 \times 5\text{ mA} = 180\text{ mA} \tag{96}$$

In an example of an eight-phase system employing the same parallel MOSFETs for one switch, the bias supply needs to be able to support the following total load current:

$$I_{VCC\_8ph} = 2 \times 8 \times 2 \times 100\ nC \times 100\ kHz + 8 \times 5\ mA = 360\ mA \quad (97)$$

As described in Bias Supplies and Voltage Reference (VCC, VDD, and VREF), the LM5171-Q1 integrates a LDO driver to drive an external N-channel enhancement MOSFET to generate 9V bias supply at the VCC pin. PMT560ENEAX is selected in this application.

However, when the gate driver loss of the external MOSFETs is high, external 10 to 12V VCC bias supply is preferred. If not available in the system, generate a bias supply from the LV-port using a buck-boost or SEPIC converter, or from the HV-port using a buck converter. Refer to the Texas Instruments LM25118 and LM5118 to implement a buck-boost converter, or LM5158 to implement a SEPIC converter, or the LM5160 and LM5161 to implement a buck converter.

A bypass capacitor needs to be placed close to the VCC and PGND pins. In this application, 2.2µF, 16V ceramic capacitor is selected.

8.6.1.2.9 Boot Strap Capacitor

Select a ceramic capacitor C_{HB1} = C_{HB2} = 0.1µF to 0.22µF. Placed the boot strap capacitor close to the HB and SW pins. The fast switching diode of the forward current rated at 1A and reverse voltage not lower than V_{HV_max} needs to be selected as the boot strap diode, through which the boot capacitor C_{HB1} or C_{HB2} is charged by VCC. A 2Ω to 5Ω current limiting resistor needs to be placed in series with each boot diode. A 12V Zener diode from SW to HB protects the high side driver from overvoltage condition.

8.6.1.2.10 Overvoltage Protection (OVP)

As described in Overvoltage Protection (OVP), LM5171-Q1 has a built in comparator with 1V internal reference and 100mV hysteresis to fulfill overvoltage protection.

In this application, We select LV-prot OVP voltage V_{OVP} = 24V. Here we select R_{OVPB} = 1kΩ thus the current through R_{OVPB} is 1mA. R_{OVPT} is found according to:

$$R_{OVPT} = \frac{V_{OVP} - V_{OVPTH}}{V_{OVPTH}} \times R_{OVPB} = \frac{24V - 1V}{1V} \times 1k\Omega = 23k\Omega \quad (98)$$

Choose standard resistor R_{OVPT} = 23.2kΩ.

8.6.1.2.11 Dead Time (DT/SD)

Pull DT pin to VDD via a 20kΩ resistor to enable built-in adaptive dead time,.

To program the dead time, follow Equation 12 to select the resistor R_{DT}. To dynamically adjust the dead time with an external analog voltage signal, follow Figure 8-10. To dynamically adjust the dead time with an external PWM signal, follow Figure 8-11.

In this application, the nominal dead time is selected to be 50ns. According to Equation 12, the programming resistor is:

$$R_{DT} = \frac{t_{DT}}{2.625} \frac{k\Omega}{ns} = 19.05k\Omega \quad (99)$$

Select standard value R_{DT} = 20kΩ.

8.6.1.2.12 Channel Current Monitor (IMONx)

For best current monitor accuracy, choose IMONx resistor that the maximum operating voltage on the IMONx pin is less than 3V.

Considering two phase current monitoring with maximum 50A for each channel, and make sure IMONx voltage no more than 3V, R_{IMONx} is found as:

$$R_{IMONx} = 10k\Omega \quad (100)$$

Choose C_{IMONx} considering delay and voltage ripple. Here we select:

$$C_{IMONx} = 10nF \tag{101}$$

Then the delay of the monitor is determined by the following time constant:

$$\tau_{IMONx} = R_{IMONx} \times C_{IMONx} = 10k\Omega \times 10ns = 100\mu s \tag{102}$$

At full load, the DC component of the monitor voltage is:

$$V_{IMONx} = 2 \times \left(\frac{I_{max} \times R_{CS}}{500\Omega} + 50\mu A\right) \times R_{IMONx} = 2 \times \left(\frac{30A \times 1m\Omega}{500\Omega} + 50\mu A\right) \times 10k\Omega = 2.2V \tag{103}$$

Considering the inductor ripple current, the IOUT peak to peak ripple current is:

$$\Delta IMONx = \frac{I_{pk-pk} \times R_{CS}}{500\Omega} = \frac{23.8A \times 1m\Omega}{500\Omega} = 47.6\mu A \tag{104}$$

The RC filter corner frequency is thus given by:

$$f_{IMONx} = \frac{1}{2\pi \times R_{IMONx} \times C_{IMONx}} = \frac{1}{6.28 \times 10k\Omega \times 10nF} = 1.59kHz \tag{105}$$

The resulting peak-to-peak monitor ripple voltage is approximately determined by:

$$\Delta V_{IMONx} = \Delta IMONx \times \left(R_{IMONx} \| \frac{1}{2i \times \pi \times F_{SW} \times C_{IMONx}}\right) = 47.6\mu A \times \left(10k\Omega \| \frac{1}{2i \times \pi \times 100kHz \times 10nF}\right) = 7.5mV \tag{106}$$

The peak-to-peak monitor ripple voltage is approximately 0.34% of the full load DC monitor voltage. Increasing C_{IMONx} attenuates the ripple voltage at the cost of higher monitor delay.

8.6.1.2.13 Undervoltage Lockout (UVLO)

The example circuit uses UVLO pin as the Controller enable pin of LM5171-Q1. However, UVLO pin also fulfills the function of undervoltage lockout, either the 48V rail UVLO, or 12V rail UVLO, or VCC UVLO.

Assume the user implements the 48V rail UVLO, and the low-side resistor R_{UVLO2} = 10kΩ, the 48V UVLO release threshold V_{UVLO} = 24V, and UVLO hysteresis is V_{HYS} = 2.4V. Referring to Equation 1, R_{UVLO1} is given by:

$$R_{UVLO1} = \frac{V_{UVLO} - 2.5\ V}{2.5\ V} \times R_{UVLO2} = \frac{24\ V - 2.5\ V}{2.5\ V} \times 10\ k\Omega = 86\ k\Omega \tag{107}$$

Select the closest standard resistor of R_{UVLO1} = 86.6kΩ.

Referring Equation 3, R_{UVLO3} is found as:

$$R_{UVLO3} = \frac{\frac{V_{HYS}}{25\ \mu A} - R_{UVLO1}}{1 + \frac{R_{UVLO1}}{R_{UVLO2}}} = \frac{\frac{2.4\ V}{25\ \mu A} - 86.6\ k\Omega}{1 + \frac{86.6\ k\Omega}{10\ k\Omega}} = 0.973\ k\Omega \tag{108}$$

Select the closest standard resistor, R_{UVLO1} = 976Ω.

If the user chooses to add the capacitor C_{UVLO} = 1nF, it leads to a delay time constant of 10µs to filter possible noise at the at the UVLO pin.

8.6.1.2.14 HVx Pin Configuration

Connect the HVx pin to the HV voltage rail. Add a small RC filter to improve the HVx noise immunity, as shown in Figure 8-16. Usually the filter resistor is 10Ω, and the bypass capacitor is 0.1µF.

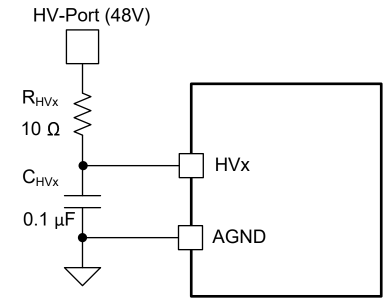


Figure 8-16. HVx Pin Configuration

8.6.1.2.15 Loop Compensation

Select current loop cross over frequency f_{CI} to 1/6 of the switching frequency. According to Equation 42, the compensation network for the inner current loop is determined by:

$$\begin{cases} R_{COMP} = \frac{K_{FF}}{A_{CS} \times R_{CS} \times G_m} \times |2i \times \pi \times f_{CI} \times L_m| = \frac{0.03125}{40 \times 1m\Omega \times 100\mu A/V} \times |2i \times \pi \times 15kHz \times 4.7\mu H| = 3.5k\Omega \\ C_{COMP} = \frac{1}{\left|2i \times \pi \times \frac{f_{CI}}{5} \times R_{COMP}\right|} = \frac{1}{\left|2i \times \pi \times \frac{15kHz}{5} \times 3.5k\Omega\right|} = 15nF \\ C_{HF} = \frac{1}{\left|2i \times \pi \times \frac{f_{SW}}{2} \times R_{COMP}\right|} = 0.9nF \end{cases} \quad (109)$$

Selecting the closest standard values for the compensation network, namely,

$R_{COMP1} = R_{COMP2} = 3.65k\Omega$

$C_{COMP1} = C_{COMP2} = 15nF$

$C_{HF1} = C_{HF2} = 1nF$

Figure 8-17 shows the bode plots of the power plant $\frac{1}{V_M} \times G_{id}(s) \times A_{CS} \times R_{CS}$, the current loop compensation gain $G_{ci}(s)$, and the resulting total open loop gain $T_i(s)$.

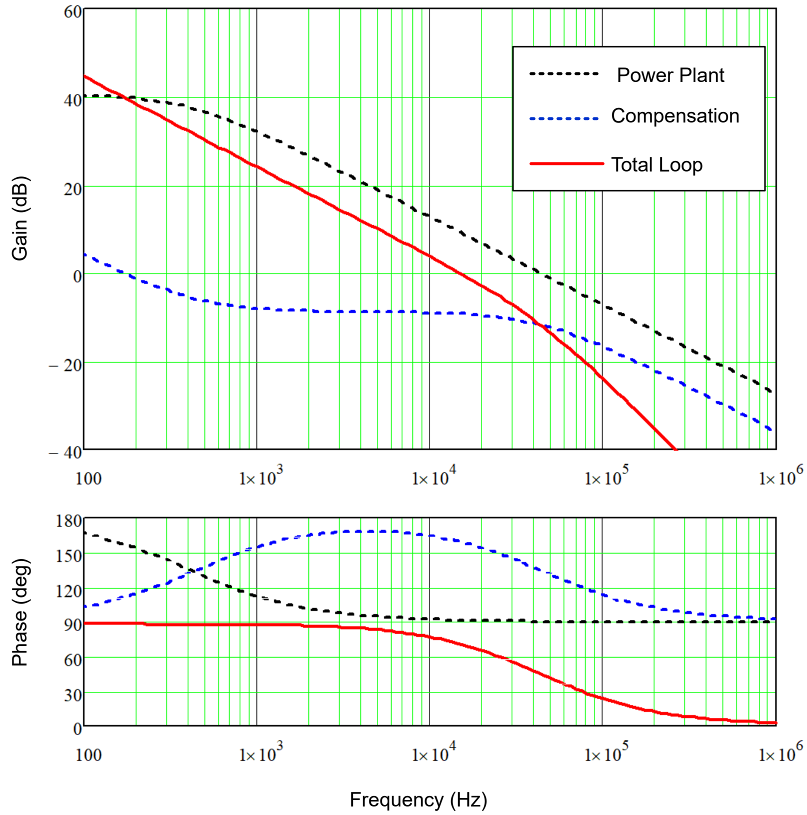


Figure 8-17. Bode Plots of the Current Loop

For buck mode, select the voltage loop crossover frequency at 1/10 of the current loop crossover frequency. According to Equation 110, the compensation network for the voltage current loop is determined by:

$$\begin{cases} R_{LCOMP} = \dfrac{R_{LFBT}}{K_{dc\_BK} \times \left| \dfrac{1 + \dfrac{2i \times \pi \times f_{CV}}{\omega_{Z\_vl}}}{1 + \dfrac{2i \times \pi \times f_{CV}}{\omega_{Z\_il}}} \right| \times K_{ISET}} = \dfrac{26.7k\Omega}{\dfrac{0.4\Omega}{40 \times 1m\Omega} \times \left| \dfrac{1 + \dfrac{2i \times \pi \times 1.5kHz}{250kHz}}{1 + \dfrac{2i \times \pi \times 1.5kHz}{6.25kHz}} \right| \times 0.8} = 6.1k\Omega \\ C_{LCOMP} = \dfrac{1}{\left| 2i \times \pi \times \dfrac{f_{CV}}{5} \times R_{COMP} \right|} = \dfrac{1}{\left| 2i \times \pi \times \dfrac{1.5kHz}{5} \times 6.1k\Omega \right|} = 86nF \\ C_{LHF} = \dfrac{1}{\left| 2i \times \pi \times 10 \times f_{CV} \times R_{COMP} \right|} = 1.7nF \end{cases} \quad (110)$$

Selecting the closest standard values for the compensation network, namely,

R_{LCOMP} = 6.2kΩ

C_{COMP1} = 100nF

C_{HF1} = 1.5nF

Figure 8-18 shows the bode plots of the power plant $G_{vs\_BK}(s)$, the voltage loop compensation gain $G_{cv}(s)$, and the resulting total open loop gain $T_{vs\_BK}(s)$.

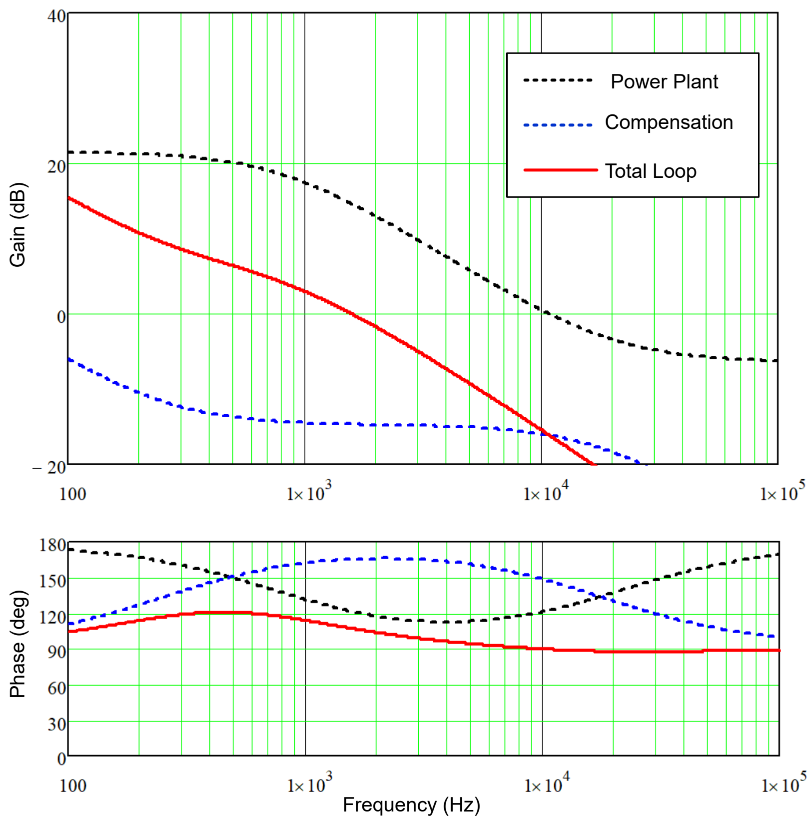


Figure 8-18. Bode Plots of the Voltage Loop

8.6.1.2.16 Soft Start (SS/DEMx)

Soft start is used to ramp the current slowly. For applications with outer loop, the current soft start is not desired, C_{SS} needs to be minimized. Select 100pF for C_{SS}.

For applications where current soft start is required, place a ceramic capacitor C_{SS} to programmed the soft start time. The soft start completes when the SS pin voltage reaches approximately 3V. If full load current soft start time ΔT_{SS} = 1ms is chosen, the capacitor C_{SS} is calculated as :

$$C_{SS} = \frac{I_{SS} \times \Delta T_{SS}}{3V} = \frac{70\mu A \times 1ms}{3V} = 23nF \tag{111}$$

When SS/DEM1 and SS/DEM2 are connected together, double the capacitance to maintain the same soft start time.

8.6.1.3 Application Curves

8.6.1.3.1 Efficiency and Thermal Performance

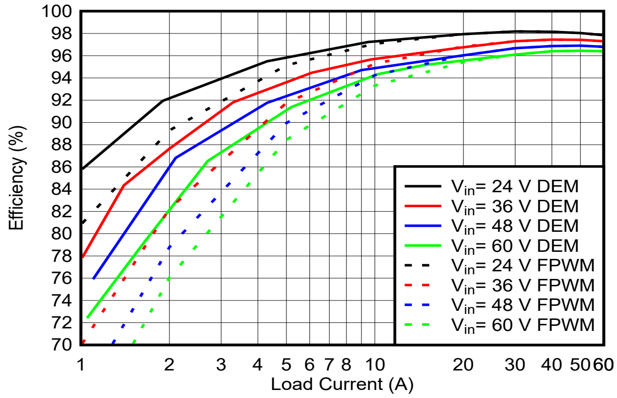


Figure 8-19. Buck Mode Efficiency vs Input Voltage and Load Current: V_{OUT} = 14.5V

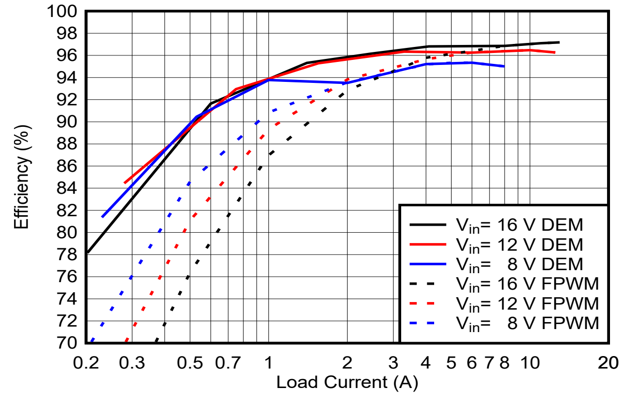


Figure 8-20. Boost Mode Efficiency vs Input Voltage and Load Current: V_{OUT} = 50.5V

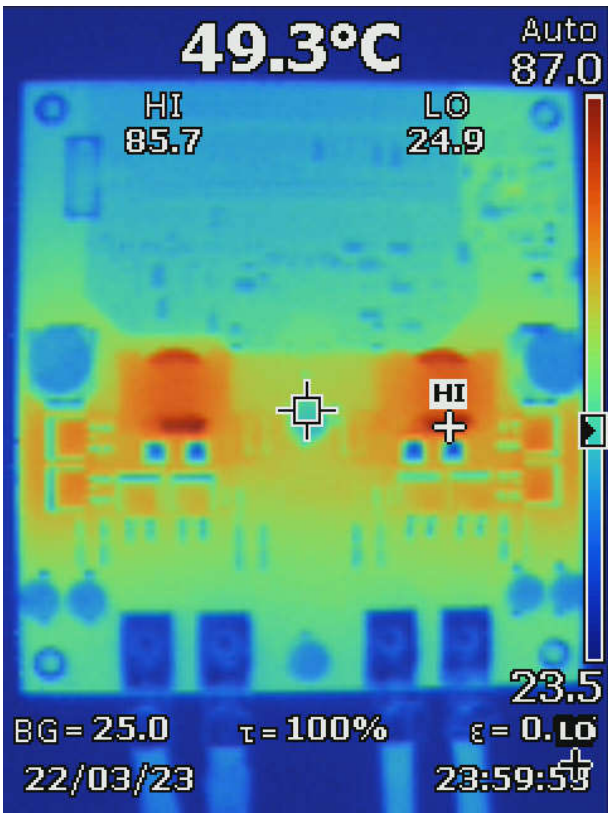


Figure 8-21. Thermal Image: Buck Mode, V_{in}=48V, V_{OUT} = 14.5V, I_{OUT}=60A, Natural Convection

8.6.1.3.2 Step Load Response

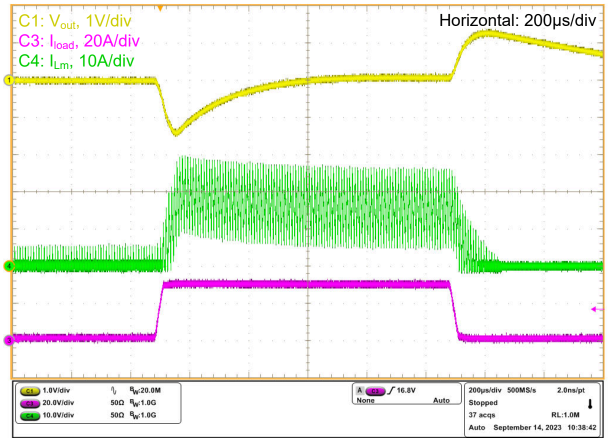


Figure 8-22. Step Load Response: Buck Mode; DEM; 1A to 30A Load Step; 1A/μs

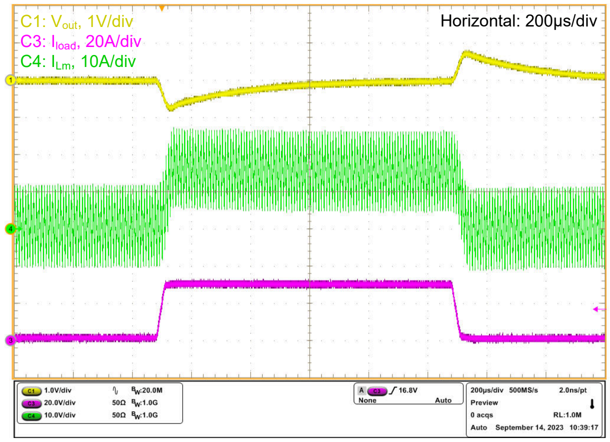


Figure 8-23. Step Load Response: Buck Mode; FPWM; 1A to 30A Load Step; 1A/μs

8.6.1.3.3 Dual-Channel Interleaving Operation

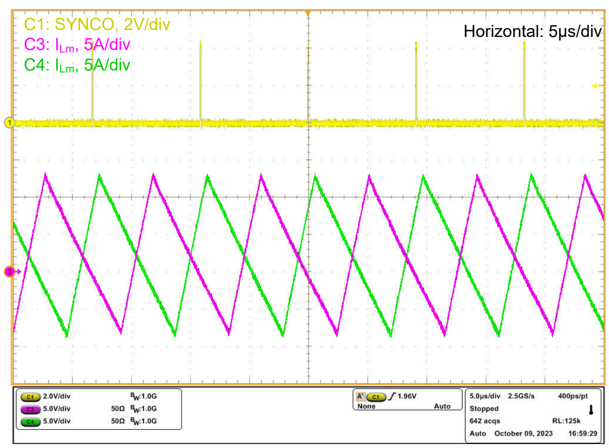


Figure 8-24. Dual-Channel Interleaving Operation: Buck Mode, I_{load}= 4A

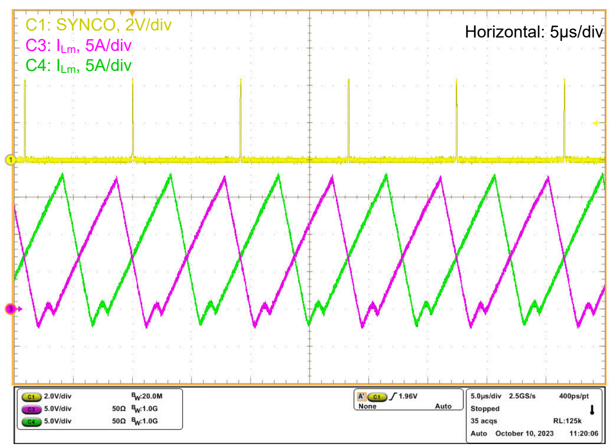


Figure 8-25. Dual-Channel Interleaving Operation: Boost Mode, I_{load}= 4A

8.6.1.3.4 Typical Start Up and Shutdown

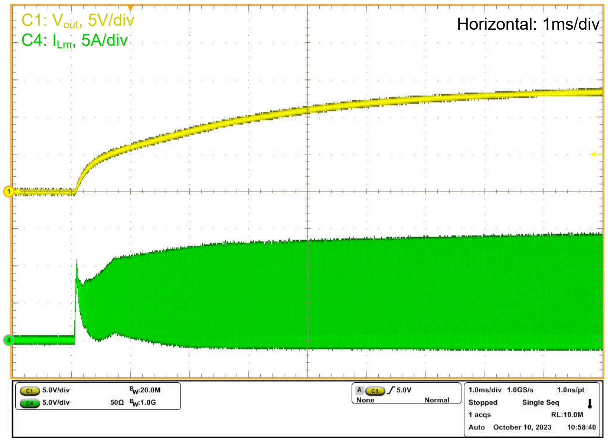


Figure 8-26. Start Up: Buck Mode, I_{load}= 10A

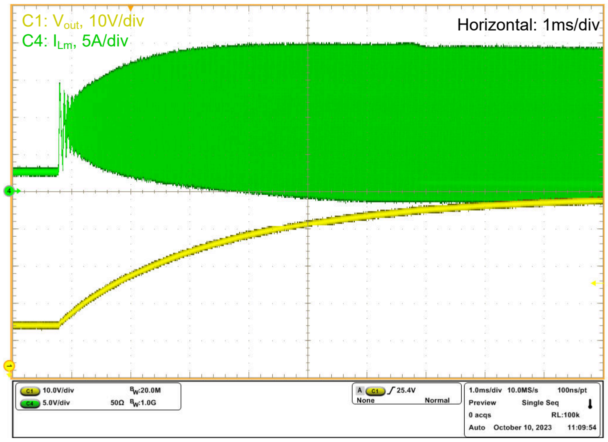


Figure 8-27. Start Up: Boost Mode, I_{load}= 4A

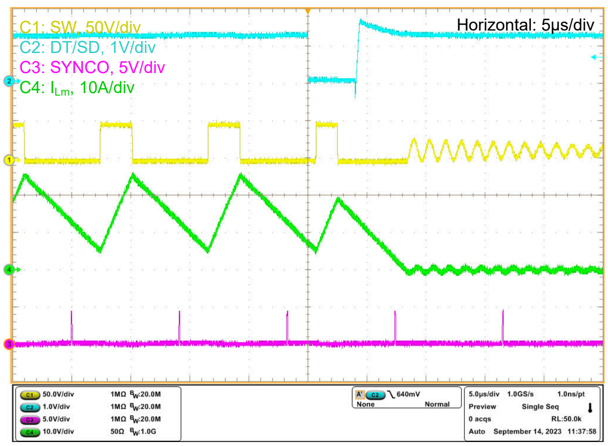


Figure 8-28. Shutdown: Latched Shutdown by DT/SD

8.6.1.3.5 DEM and FPWM

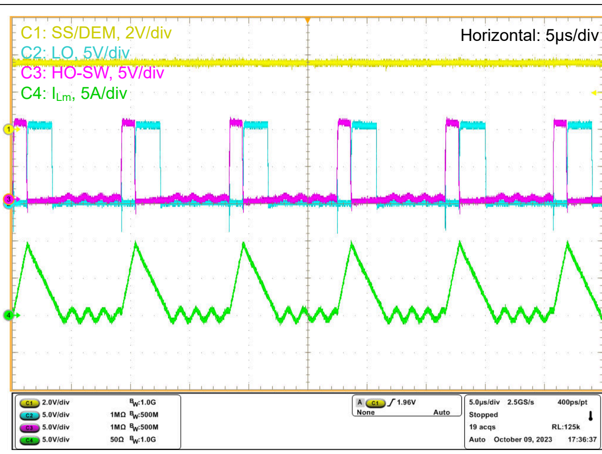


Figure 8-29. DEM: Buck Mode, I_{load}= 4A

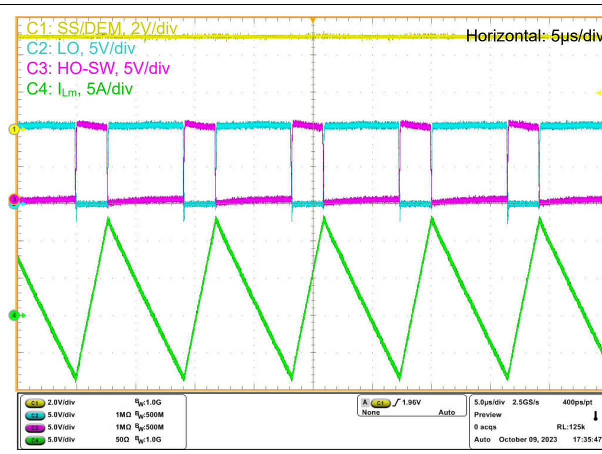


Figure 8-30. FPWM: Buck Mode, I_{load}= 4A

8.6.1.3.6 Mode Transition Between DEM and FPWM

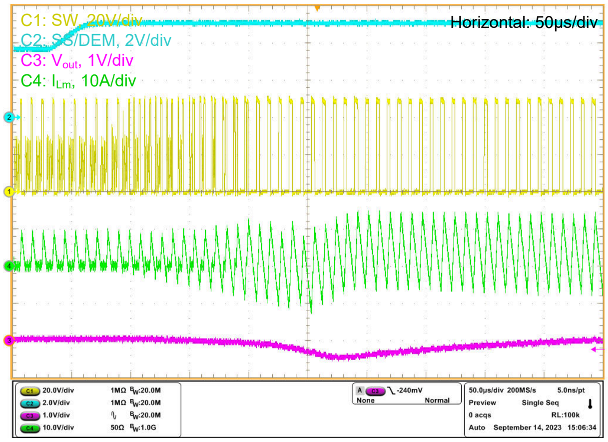


Figure 8-31. Mode Transition from DEM to FPWM: Buck Mode, I_{load} = 4A

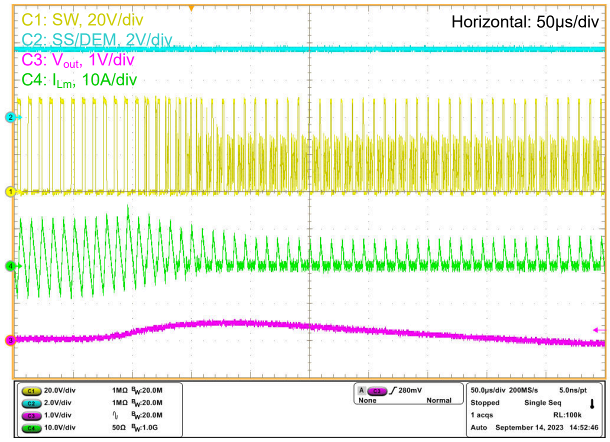


Figure 8-32. Mode Transition from FPWM to DEM: Buck Mode, I_{load} = 4A

8.6.1.3.7 ISET Tracking and Pre-charge

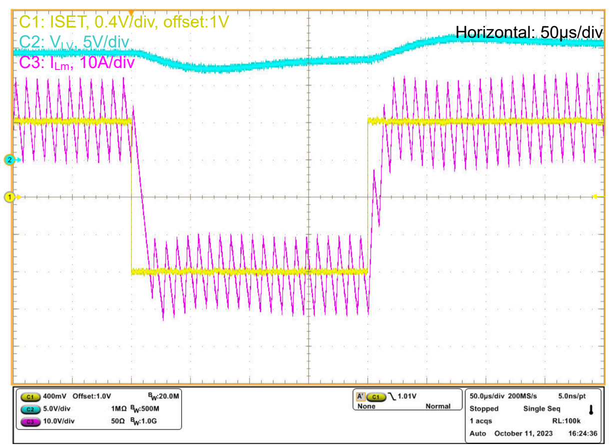


Figure 8-33. ISET Tracking: Inductor Current Tracking with Direction Change

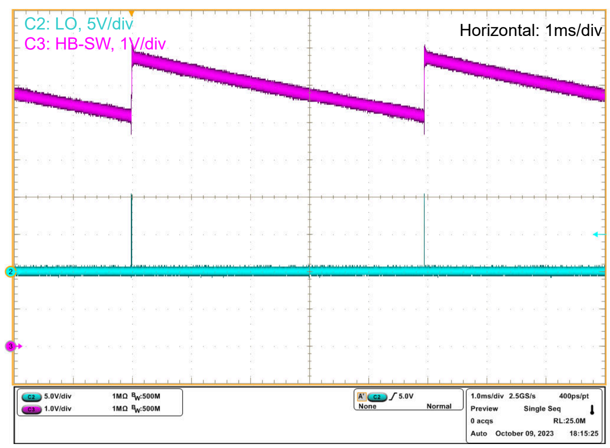


Figure 8-34. Pre-charge: Buck Mode, I_{load}= 0A

8.6.1.3.8 Protections

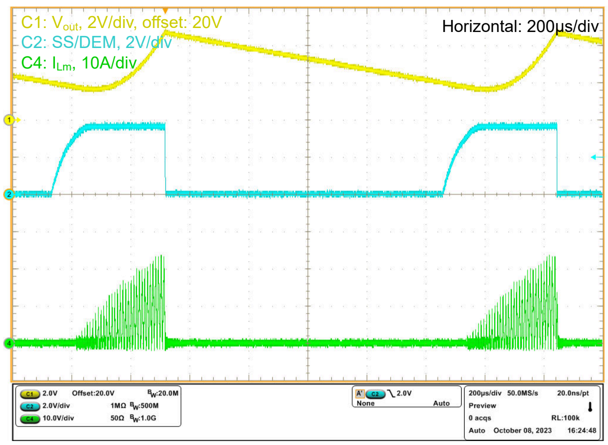


Figure 8-35. OVP: Buck Mode

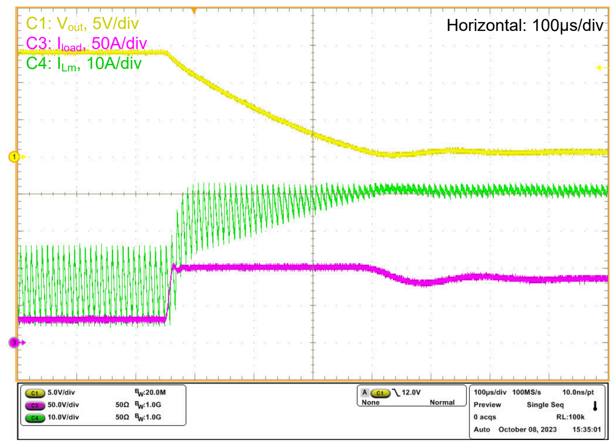


Figure 8-36. Output Short Circuit: Buck Mode

8.7 Power Supply Recommendations

The LM5171-Q1-based converter is designed to operate with two differential voltage rails like the 48V and 12V dual battery system, or a storage system having a battery on one end and the Super-Cap on the other end. When operating with bench power supplies, each supply needs to be capable of sourcing and sinking the maximum operating current. Parallel an Electronic load (E-Load) with the bench power supply (PS) to emulate the batteries, as shown in Figure 8-37.

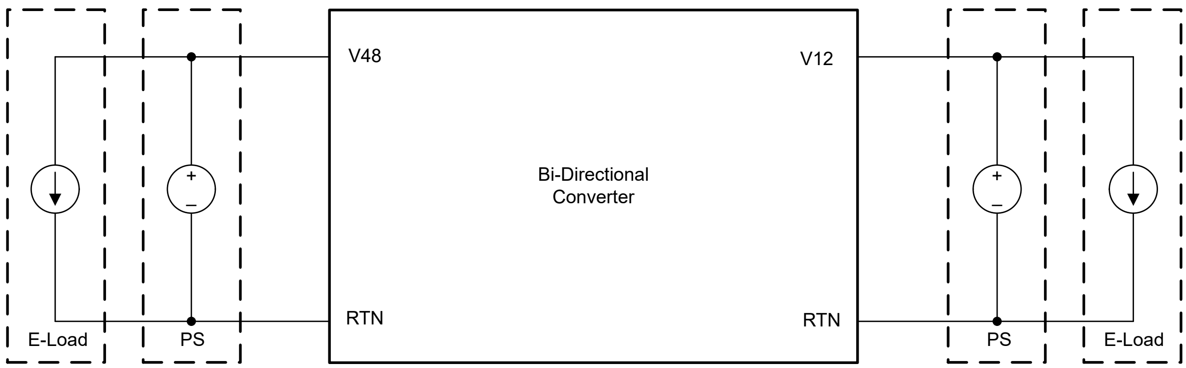


Figure 8-37. Emulated Dual Battery System With Bench Power Supplies and E-Loads

8.8 Layout

8.8.1 Layout Guidelines

Careful PCB layout is critical to achieve low EMI and stable power supply operation as well as optimal efficiency. Make the high frequency current loops as small as possible, and follow these guidelines of good layout practices:

1. For high power board design, use at least a 4-layer PCB of 2oz or thicker copper planes. Make the first inner layer a ground plane that is adjacent to the top layer on which the power components are installed, and use the second inner layer for the critical control signals including the current sense, gate drive, commands, and so forth. The ground plane between the signal and top layers helps shield switching noises on the top layer away from affecting the control signals.
2. Optimize the component placements and orientations before routing any traces. Place the power components such that the power flow from port to port is direct, straight and short. Avoid making the power flow path zigzag on the board.
3. Identify the high frequency AC current loops. In the bidirectional converter, the AC current loop of each channel is along the path of the HV-port rail capacitors, high-side MOSFET, low-side MOSFET, and back to the return of the HV-port rail capacitor. Place these components such that the current flow path is short, direct and the special area enclosed by the loop is minimized.
4. Place the power circuit symmetrically between CH-1 and CH-2. Split the HV-port rail capacitors and LV-port rail capacitors evenly between CH-1 and CH-2.
5. If more than one LM5171-Q1 is used on the same PCB for multi phases, place the circuits of each LM5171-Q1 in the similar pattern.
6. Use adequate copper for the power circuit, so as to minimize the conduction losses on high-current PCB tracks. Adequate copper also helps dissipating the heat generated by the power components, especially the power inductors, power MOSFETs, and current sense resistors. However, pay attention to the polygon of the switch node, which connects the high-side MOSFET source, low-side MOSFET drain, power inductor, and the controller SW pin. The switch node polygon sees high dv/dt during switching operation. To minimize the EMI emission by the switch node polygon, make its size sufficient but not excessive to conduct the switched current.
7. Use appropriate number of via holes to conduct current to, and heat through, the inner layers.
8. Always separate the power ground from the analog ground, and make a single point connection of the power ground, analog ground, and the EP pad, at the location of the PGND pin.
9. Minimize current-sensing errors by routing each pair of CSA and CSB traces using a kelvin-sensing directly across the current sense resistors. The pair of traces need to be routed closely side by side for good noise immunity.
10. Route sensitive analog signals of the CS, FBLV, FBHV, IPK, VSET, IMON, COMP and OVP pins away from the high-speed switching nodes (HB, HO, LO, and SW).
11. Route the paired gate drive traces, namely the pairs of HO1 and SW1, HO2 and SW2, LO1 and return, and LO2 and return, closely side by side. Route CH-1 gate drive traces in symmetry with that of CH-2.
12. Place the device setting, programming and controlling components as close as possible to the corresponding pins, including the following component: R_{OSC}, R_{CFG}, R_{DT}, , C_{COMP1}, R_{COMP2}, C_{COMP1}, C_{COPM2}, C_{HF1}, C_{HF2}, R_{HVC}, R_{LVC}, C_{HVC}, C_{LVC}, C_{HVHF} and C_{LVHF}.
13. Place the bypass capacitors as close as possible to the corresponding pins, including C_{HV}, C_{VCC}, C_{VDD}, C_{VREF}, C_{VSET}, C_{HB1}, C_{HB2}, C_{OVP}, C_{IPK}, C_{ISET}, C_{CS1}, C_{CS2} as well as the 100-pF current sense common-mode bypassing capacitors.
14. Flood each layer with copper to take up the empty areas for optimal thermal performance.
15. Apply heat sink to components as necessary according to the system requirements.

8.8.2 Layout Examples

The following figures are some examples illustrating these layout guidelines. For the detailed PCB layout artwork of the LM5171-Q1 Evaluation Module (LM5171EVM-BIDIR), please refer to the *LM5171 EVM User's Guide*.

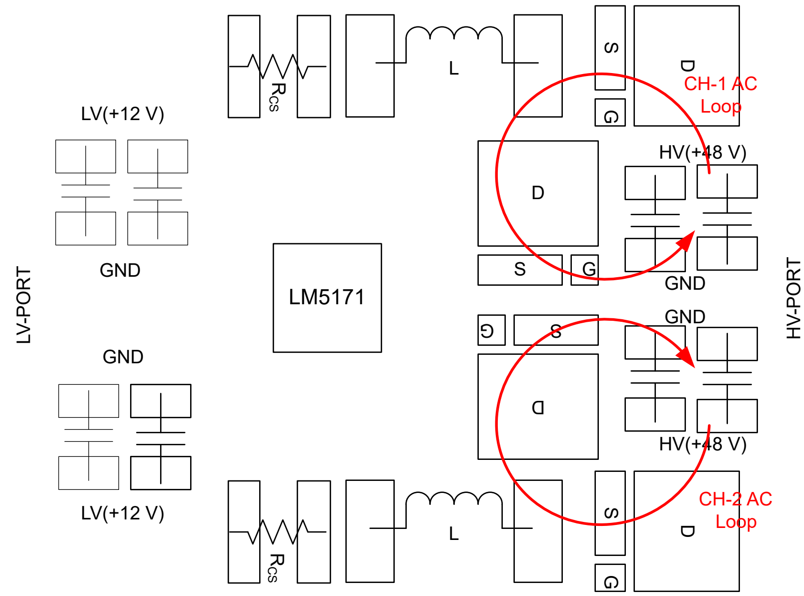


Figure 8-38. A Layout Example of Dual-Channel Power Circuit Placement

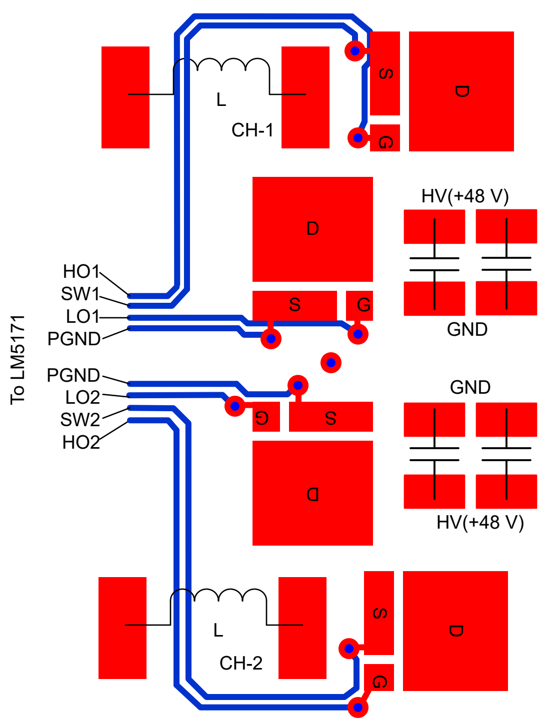
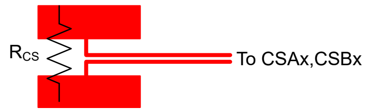
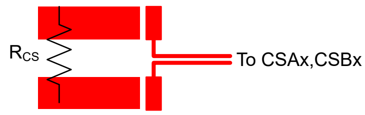


Figure 8-39. A Layout Example of MOSFET Gate Drive Routing



(a) Kelvin Connect of Resistor without Sense Pins



(b) Kelvin Connect of Resistor with Sense Pins

Figure 8-40. A Layout Example of Current Sense Routing

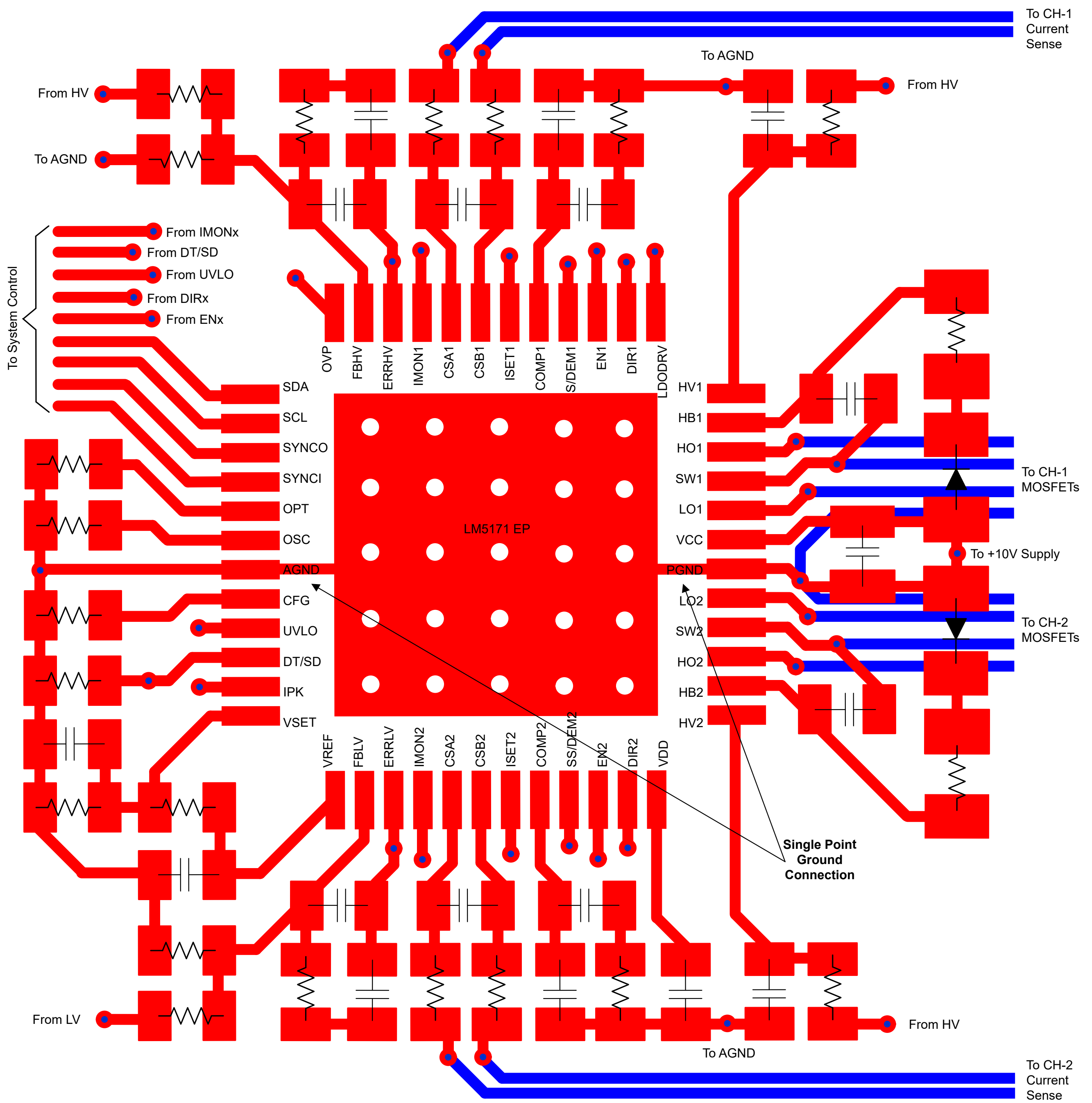


Figure 8-41. A Layout Example of LM5171-Q1 Critical Signal Routing

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

For development support, see the following:

- LM5170
- LM25118
- LM5118
- LM5158
- LM5160
- LM5161

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2025) to Revision B (September 2025)	Page
• Changed document status from Advance Information to Production Data	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5171QPHPRQ1	Active	Production	HTQFP (PHP) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 150	LM5171Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM5171-Q1 :

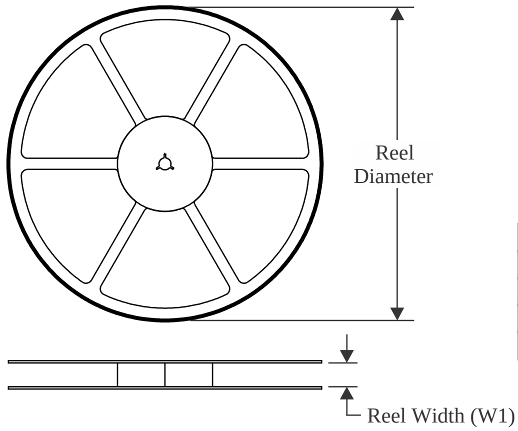
- Catalog : LM5171

NOTE: Qualified Version Definitions:

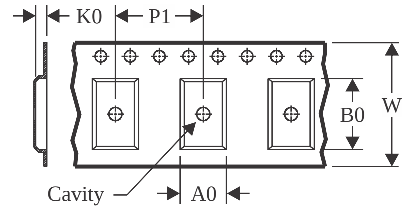
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

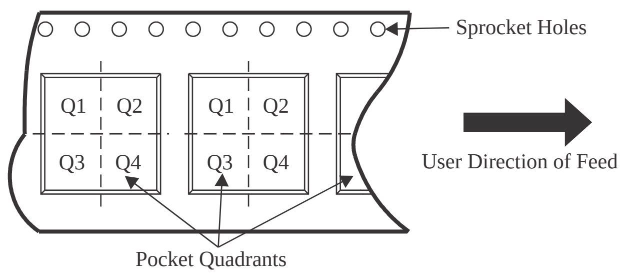


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

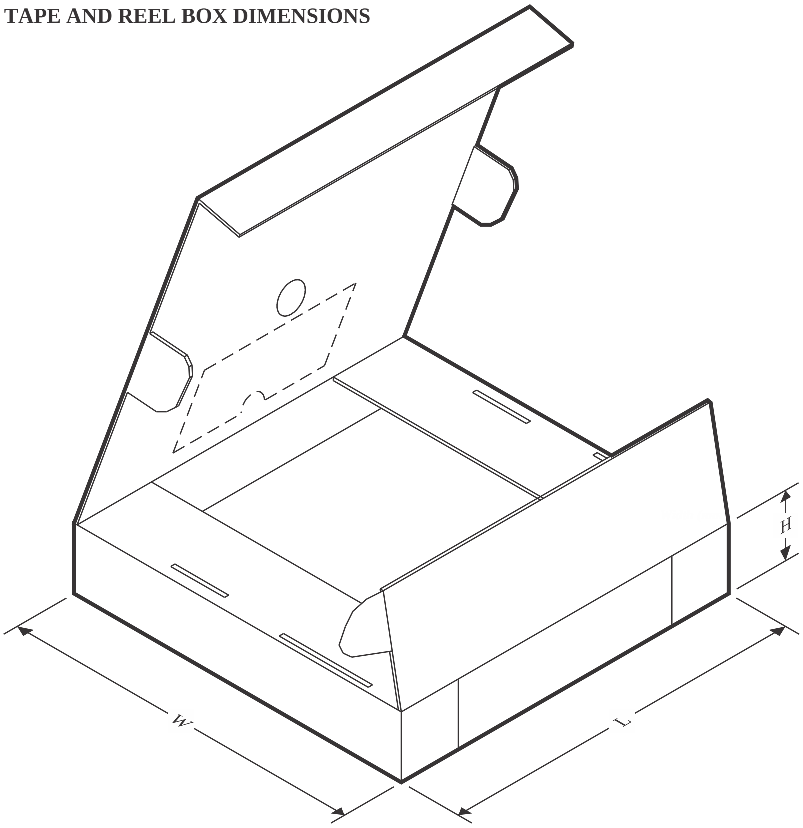
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5171QPHPRQ1	HTQFP	PHP	48	2500	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5171QPHPRQ1	HTQFP	PHP	48	2500	336.6	336.6	31.8

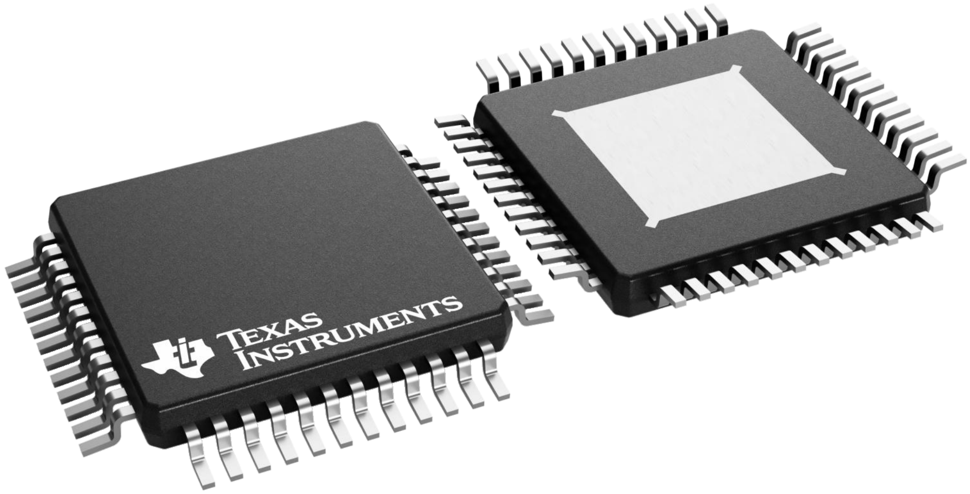
PHP 48

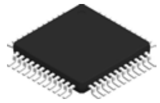
TQFP - 1.2 mm max height

7 x 7, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

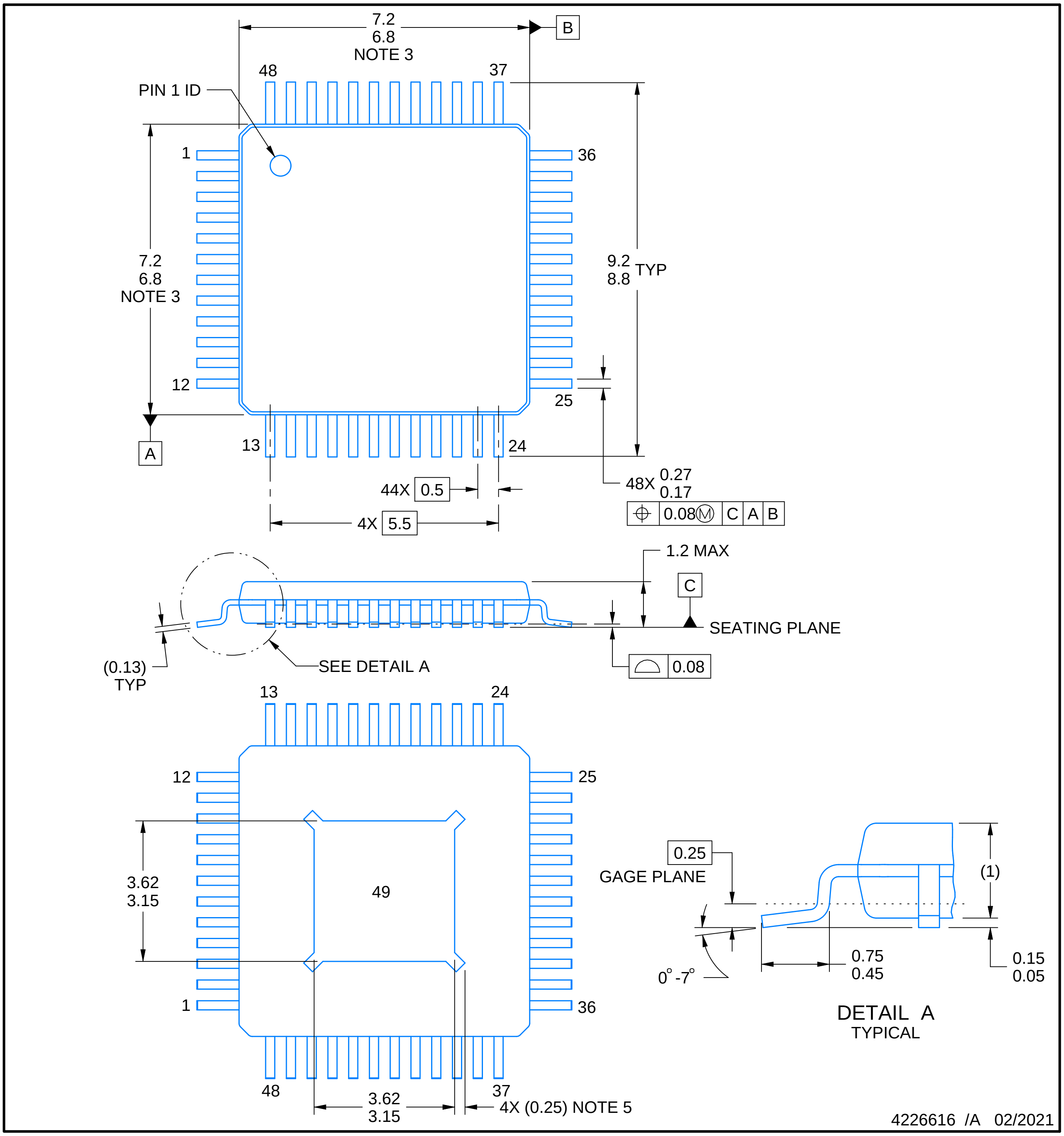




PACKAGE OUTLINE

PHP0048E

PowerPAD™ HTQFP - 1.2 mm max height



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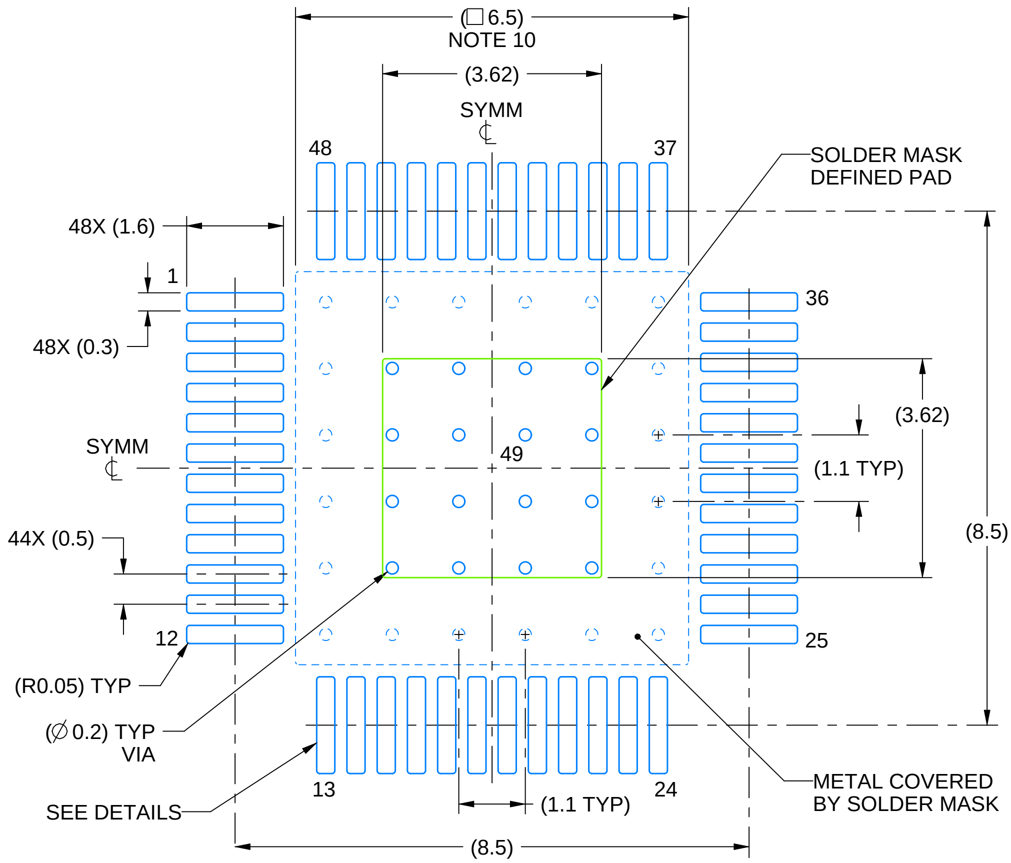
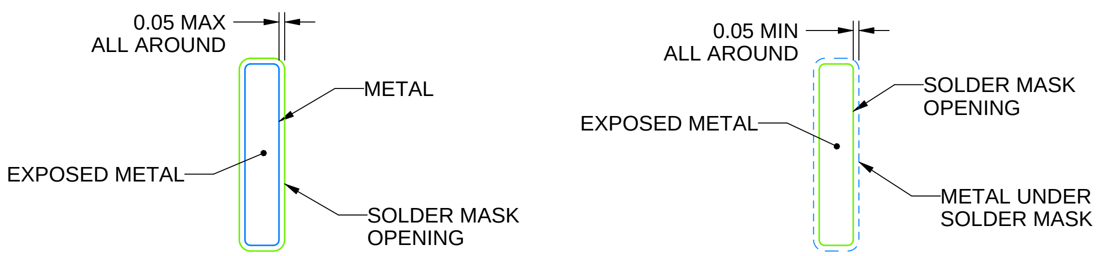
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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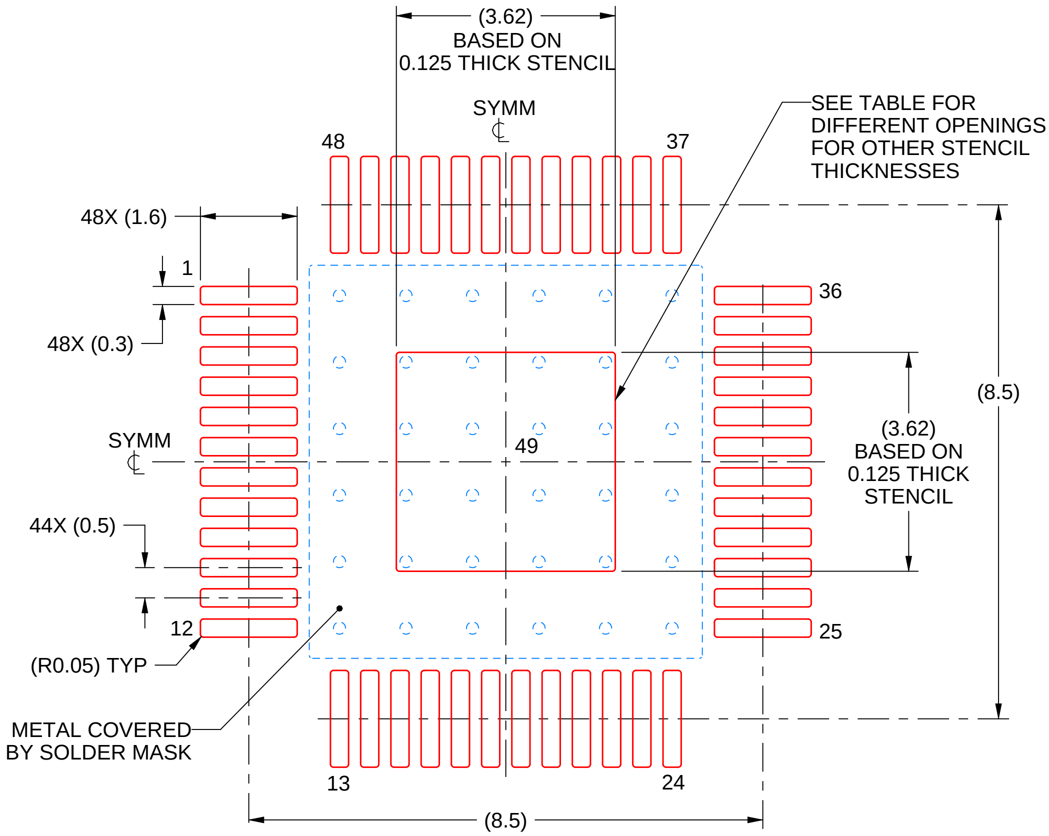
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.05 X 4.05
0.125	3.62 x 3.62 (SHOWN)
0.150	3.30 x 3.30
0.175	3.06 x 3.06

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.