

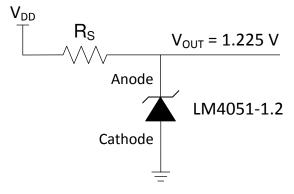
LM4051-N Precision Micropower Shunt Voltage Reference

1 Features

- No output capacitor required
- Tolerates capacitive loads
- Reverse breakdown voltage options of 1.225V and adjustable
- Key specifications:
 - Output voltage tolerance (A Grade, 25 °C) ± 0.1% (maximum)
 - Output noise (10Hz to 10kHz) 20µVrms
 - Operating current range: 60µA to 12mA
 - Industrial temp. range: −40 °C to +85 °C
 - Extended temp. range: -40 °C to +125 °C
 - Temperature coefficient: 50ppm/ ℃ (maximum)

2 Applications

- **Battery-Powered Equipment**
- **Data-Acquisition Systems**
- Instrumentation and Test Equipment
- **Process Control**
- **Energy Management/Metering**
- **Automotive Electronics**
- **Precision Audio**
- **Base Stations**
- **Battery Chargers**
- **Medical Equipment**
- Communication



1.2 V_{REF} Simplified Schematic

3 Description

Designed for space critical applications, the LM4051-N precision voltage reference is available in the sub-miniature (3mm x 1.30mm) SOT-23 surface mount package. The LM4051-N's advanced design eliminates the need for an external stabilizing capacitor while maintaining stability with capacitive load, thus making the LM4051-N easy to use. Further reducing design effort is the availability of a fixed (1.225V) and adjustable reverse breakdown voltage. The minimum operating current is 60µA for the LM4051-1.2 and the LM4051-ADJ. Both versions have a maximum operating current of 12mA.

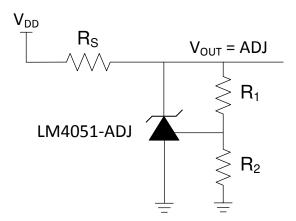
The LM4051-N comes in three grades (A, B, and C). The best grade devices (A) have an initial accuracy of 0.1%, while the B-grade have 0.2% and the C-grade 0.5%, all with a tempco of 50 ppm/ °C designed for -40°C to 125°C.

The LM4051-N utilizes fuse and zener-zap trim of reference voltage during wafer sort to ensure that the prime parts have an accuracy of better than ± 0.1% (A grade) at 25°C.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
LM4051-N	SOT-23 (3)	3.00mm x 1.30mm

- For all available packages, see the orderable addendum at the end of the data sheet.
- The package size (length × width) is a nominal value and includes pins, where applicable.



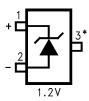
Adjustable Reference Simplified Schematic



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4 Pin Configuration and Functions



^{*} This pin must be left floating or connected to pin 2.(1)

Figure 4-1. DBZ Package 1.2V, 3-Pin SOT-23 Top View

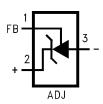


Figure 4-2. DBZ Package Adjustable, 3-Pin SOT-23 Top View

Pin Functions

	PIN		I/O	DESCRIPTION	
NAME	1.2V	ADJ	1/0	DESCRIPTION	
Anode	2	3	0	Common pin, normally connected to ground	
Cathode	1	2	I/O	Shunt Current/Voltage input	
NC	3	-	-	Must float or connect to anode ⁽¹⁾	
FB	-	1	I	Threshold relative to cathode	

⁽¹⁾ In applications with high electromagnetic interference (for example, when placed near transformers or other electromagnetic sources) or significant high-frequency switching noise, TI recommends connecting this pin to the anode

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Reverse current		20	mA	
Forward current			10	mA
Maximum output voltage (LM4051-ADJ)			15	V
Power dissipation (T _A = 25°C) ⁽²⁾ M3 package			280	mW
Load tomporature M2 packages	Vapor phase (60 seconds)		215	°C
Lead temperature M3 packages	Infrared (15 seconds)		220	
Storage temperature, T _{stg}			150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
- (2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is P_{Dmax}= (T_{Jmax} ¬T_A)/ θ_{JA} or the number given in the Section 5.1, whichever is lower. For the LM4051-N, T_{Jmax} = 125°C, and the typical thermal resistance (θ_{JA}), when board mounted, is 280°C/W for the SOT-23 package.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	L' I	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ (2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽³⁾	±500	\ \ \ \

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) The human-body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. All pins are rated at 2kV for human-body model, but the feedback pin which is rated at 1kV.
- (3) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250V CDM is possible with the necessary precautions.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM MAX	UNIT	
Temperature $(T_{min} \le T_A \le T_{max})$	Industrial temperature	-40 85		°C	
Temperature (T _{min} > T _A > T _{max})	Extended temperature	-40	125	C	
Reverse current	LM4051-1.2	0.06	12	mA	
ixeverse current	LM4051-ADJ	0.06	12		
Output voltage	LM4051-ADJ	1.24	10	V	



5.4 Thermal Information

	THERMAL METRIC(1)	LM4051-ADJ, LM4051-1.2 V	UNIT
	I TERMAL METRIC	DBZ	UNIT
		3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	214.7	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	76.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.3	°C/W
ΨЈТ	Junction-to-top characterization parameter	2.0	°C/W
ΨЈВ	Junction-to-board characterization parameter	40.9	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 LM4051-1.2 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	T	EST CONDITIONS	MIN TYP	MAX	UNIT	
	Reverse Breakdown Voltage	I _R = 100μA		1.225		V	
			LM4051AIM3 ⁽¹⁾		±1.2		
		I _R = 100μA	LM4051BIM3 LM4051BEM3 ⁽¹⁾		±2.4		
V_			LM4051CIM3 ⁽¹⁾		±6		
V_R	Reverse Breakdown		LM4051AIM3 ⁽¹⁾		±5.2 ⁽²⁾	mV	
	Voltage Tolerance ⁽²⁾	Industrial Temp. Range T _A = T _J = T _{MIN} to T _{MAX}	LM4051BIM3 ⁽¹⁾		±6.4 ⁽²⁾	1111	
		I'A - I'J - I'MIN to I'MAX	LM4051CIM3 ⁽¹⁾		±10.1 ⁽²⁾		
		Extended Temp. Range $T_A = T_J = T_{MIN}$ to T_{MAX}	LM4051BEM3 ⁽¹⁾		±8.6 ⁽²⁾		
		T _J = 25°C		39			
I _{RMIN}	Minimum Operating Current	Industrial Temp. Range $T_A = T_J = T_{MIN}$ to T_{MAX}			65	μA	
	Outlone	Extended Temp. Range $T_A = T_J = T_{MIN}$ to T_{MAX}			70		
	Average Reverse Breakdown Voltage Temperature Coefficient ⁽²⁾	I _R =10mA		±20			
		I _R =1mA		±15			
$\Delta V_R/\Delta T$		emperature I_ = 100µA	T _J = 25°C	±15		ppm/℃	
			$T_A = T_J = T_{MIN}$ to T_{MAX}		±50 ⁽²⁾		
	Payarsa Braakdown	Reverse Breakdown		T _J = 25°C	0.3		
			I _{RMIN} ≤ I _R ≤ 1mA	Industrial Temp. Range $T_A = T_J = T_{MIN}$ to T_{MAX}		1.1 ⁽²⁾	
$\Delta V_R / \Delta I_R$	Voltage Change with Operating Current		Extended Temp. Range $T_A = T_J = T_{MIN}$ to T_{MAX}		1.5 ⁽²⁾	mV	
	Change		T _J = 25°C	1.8			
		1mA ≤ I _R ≤ 12mA	Industrial Temp. Range $T_A = T_J = T_{MIN}$ to T_{MAX}		6 ⁽²⁾		
			Extended Temp. Range $T_A = T_J = T_{MIN}$ to T_{MAX}		8(2)		
Z _R	Reverse Dynamic Impedance	I _R = 1mA, f = 120Hz		0.5		Ω	
e _N	Wide band Noise	I _R = 100μA 10Hz ≤ f ≤ 10kHz		20		μVrms	

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5.5 LM4051-1.2 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔV_{R}	Reverse Breakdown Voltage Long Term Stability ⁽³⁾	t = 1000 hrs, T = 25 °C ± 0.1 °C, I _R = 100μA	-	120		ppm
V _{HYST}	Thermal Hysteresis ⁽⁴⁾	$\Delta T = -40 \text{°C}$ to 125 °C		0.36		mV/V

- (1) Limits are 100% production tested at 25 °C. Limits over temperature are made sure through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's AOQL.
- (2) This over temperature limit for Reverse Breakdown Voltage Tolerance is defined as the room temperature Reverse Breakdown Voltage Tolerance ±[(ΔVR/ΔT)(maxΔT)(VR)]. Where, ΔVR/ΔT is the VR temperature coefficient, maxΔT is the maximum difference in temperature from the reference point of 25°C to TMAX or TMIN, and VR is the reverse breakdown voltage. The total over temperature tolerance for the different grades in the industrial temperature range where maxΔT=65C is shown below:
 - A-grade: ±0.425% = ±0.1% ±50 ppm/°C x 65°C
 - B-grade: $\pm 0.525\% = \pm 0.2\% \pm 50 \text{ ppm/°C x } 65\%$
 - C-grade: $\pm 0.825\% = \pm 0.5\% \pm 50 \text{ ppm/°C x } 65^{\circ}\text{C}$

Therefore, as an example, the A-grade LM4051-1.2 has an over-temperature Reverse Breakdown Voltage tolerance of \pm 1.2V x 0.425% = \pm 5.2mV.

- (3) Long-term stability is V_R at 25°C measured during 1000 hrs.
- (4) Thermal hysteresis is defined as the difference in voltage measured at +25 ℃ after cycling to temperature –40 ℃ and the 25 ℃ measurement after cycling to temperature +125 ℃.

5.6 LM4051-ADJ Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TI	EST CONDITIONS	MIN TYP	MAX	UNIT	
	Reference Voltage	I _R = 100μA, V _{OUT} = 5V		1.212		V	
			LM4051AIM3 ⁽¹⁾		±1.2		
V_{REF}		$I_R = 100 \mu A, V_{OUT} = 5V$	LM4051BIM3 ⁽¹⁾		±2.4		
	Reference Voltage		LM4051CIM3 ⁽¹⁾		±6		
	Tolerance ^{(2) (4)}		LM4051AIM3 ⁽¹⁾		±5.2	mV	
		Industrial Temp. Range $T_A = T_{.1} = T_{MIN}$ to T_{MAX}	LM4051BIM3 ⁽¹⁾		±6.4		
		I'A - IJ - IMIN to IMAX	LM4051CIM3 ⁽¹⁾		±10.1		
		LM4051AIM3 ⁽¹⁾		36			
		LM4051BIM3 ⁽¹⁾		36			
	Minimum Operating Current	LM4051CIM3 ⁽¹⁾		36			
I _{RMIN}		Industrial Temp. Range $T_A = T_J = T_{MIN}$ to T_{MAX}	LM4051AIM3 ⁽¹⁾		60	μΑ	
			LM4051BIM3 ⁽¹⁾		60		
			LM4051CIM3 (1)		65		
				T _J = 25°C	0.3		
ΔV_{REF}	Reference Voltage	$I_{RMIN} \le I_R \le 1mA$ $V_{OUT} \ge 1.6V^{(3)}$	Industrial Temp. Range $T_A = T_J = T_{MIN}$ to T_{MAX}		1.1(2)	mV	
ΔI_R	Change with Operating Current Change	4 4. 4. 4. 4. 4. 4. 4. 4. 4. 4. 4. 4.	T _J = 25°C	0.6			
	Carrent Change	$1\text{mA} \le I_R \le 12\text{mA}$ $V_{\text{OUT}} \ge 1.6V^{(3)}$	Industrial Temp. Range T _A = T _J = T _{MIN} to T _{MAX}		6 ⁽²⁾		
	Reference Voltage		T _J = 25°C	-1.69			
$\Delta V_{REF}/$ ΔV_{O}	Change with Output Voltage Change	nge with Output I _R = 0.1mA	Industrial Temp. Range $T_A = T_J = T_{MIN}$ to T_{MAX}		-2.8 ⁽²⁾	mV	
I _{FB}	Feedback Current			70	130	nA	

5.6 LM4051-ADJ Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TE	ST CONDIT	TIONS	MIN	TYP	MAX	UNIT
				T _J = 25°C		20		
			I _R = 10mA	Industrial Temp. Range $T_A = T_J = T_{MIN}$ to T_{MAX}			±50 ⁽²⁾	
AV/ /	Average Reference	\/ - 2.5\/		T _J = 25°C		15		
ΔV _{REF} / ΔT	Voltage Temperature Coefficient (Note 8)	$V_{OUT} = 2.5V$ $\Delta T = -40 \degree C$ to +125 $\degree C$	I _R = 1mA	Industrial Temp. Range $T_A = T_J = T_{MIN}$ to T_{MAX}			±50 ⁽²⁾	ppm/°C
			I _R =100μA	T _J = 25°C		15		
				Industrial Temp. Range $T_A = T_J = T_{MIN}$ to T_{MAX}			±50 ⁽²⁾	
7	Dynamic Output	I _R = 1mA, f = 120Hz, I _{AC}	V _{OUT} = V _{RE}	EF		0.3		Ω
Z _{OUT}	Impedance	= 0.1 I _R	V _{OUT} = 10\	/		2		1 12
e _N	Wide band Noise	$I_{R} = 100\mu A, V_{OUT} = V_{REF}, 10Hz \le f \le 10kHz$				20		μVrms
ΔV_{REF}	Reference Voltage Long Term Stability ⁽⁵⁾	t = 1000 hrs, I_R = 100 μ A, T = 25 °C ± 0.1 °C				120		ppm
V_{HYST}	Thermal Hysteresis ⁽⁶⁾	ΔT = −40 °C to +125 °C				0.3		mV/V

- (1) Limits are 100% production tested at 25°C. Limits over temperature are made sure through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's AOQL.
- (2) This over temperature limit for Reverse Breakdown Voltage Tolerance is defined as the room temperature Reverse Breakdown Voltage Tolerance ± [(ΔV_R/ΔT)(maxΔT)(V_R)]. Where, ΔV_R/ΔT is the V_R temperature coefficient, maxΔT is the maximum difference in temperature from the reference point of 25°C to T_{MAX} or T_{MIN}, and V_R is the reverse breakdown voltage. The total over temperature tolerance for the different grades in the industrial temperature range where maxΔT = 65°C is shown below:
 - A-grade: $\pm 0.425\% = \pm 0.1\% \pm 50$ ppm/°C × 65°C
 - B-grade: ± 0.525% = ± 0.2% ± 50ppm/°C × 65°C
 - C-grade: $\pm 0.825\% = \pm 0.5\% \pm 50$ ppm/°C × 65°C

Therefore, as an example, the A-grade LM4051-1.2 has an over temperature Reverse Breakdown Voltage tolerance of \pm 1.2 V × 0.425% = \pm 5.2mV.

- (3) When V_{OUT} ≤ 1.6V, the LM4051-ADJ in the SOT-23 package must operate at reduced I_R. This is caused by the series resistance of the die attach between the die (–) output and the package (–) output pin. See the Output Saturation curve in the Section 5.7 section.
- (4) Reference voltage and temperature coefficient change with output voltage. See Section 5.7 curves.
- (5) Long-term stability is V_R at 25°C measured during 1000 hrs.
- (6) Thermal hysteresis is defined as the difference in voltage measured at +25 °C after cycling to temperature –40 °C and the 25 °C measurement after cycling to temperature +125 °C.

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5.7 Typical Characteristics

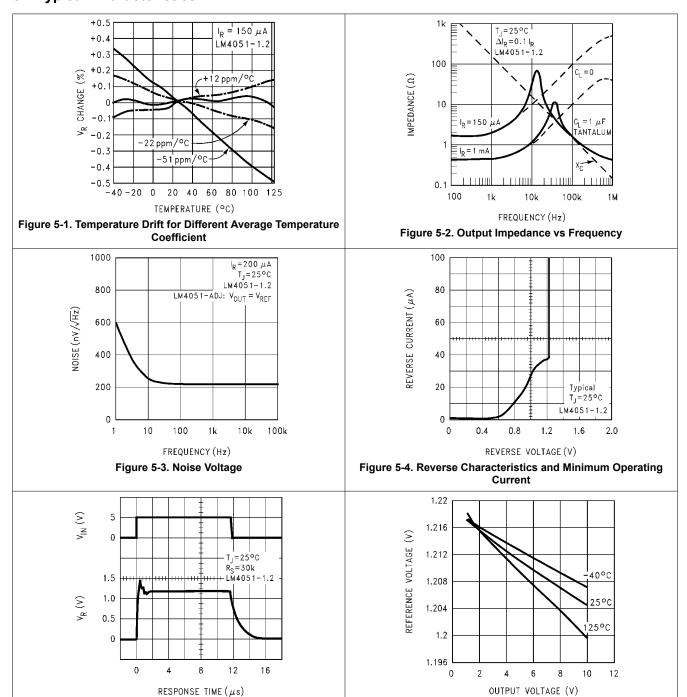
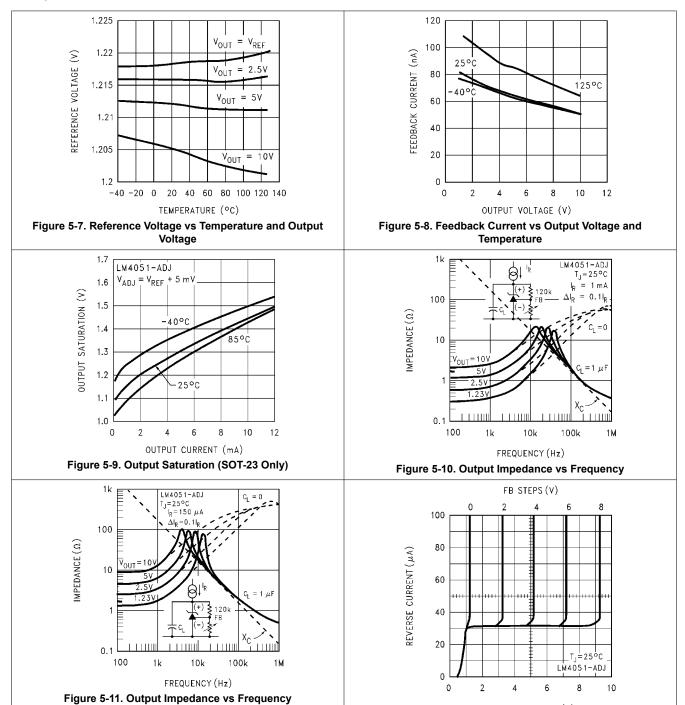


Figure 5-5. Start-Up Characteristics

Figure 5-6. Reference Voltage vs Output Voltage and Temperature



5.7 Typical Characteristics (continued)

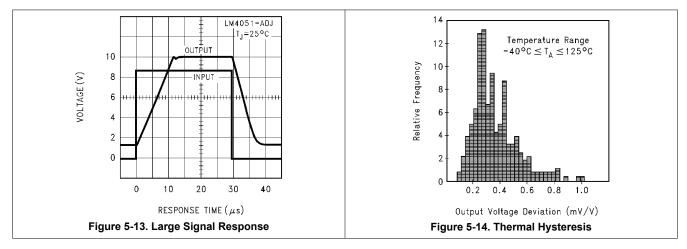


OUTPUT VOLTAGE (V)

Figure 5-12. Reverse Characteristics



5.7 Typical Characteristics (continued)





6 Parameter Measurement Information

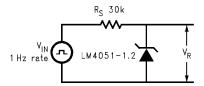


Figure 6-1. Test Circuit for Start-Up Characteristics

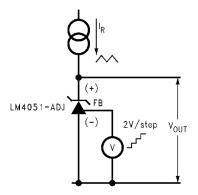


Figure 6-2. Test Circuit for Reverse Characteristics

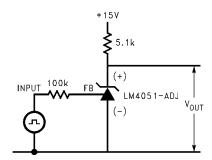


Figure 6-3. Test Circuit for Large Signal Response

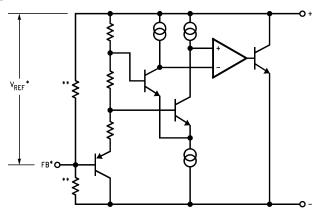


7 Detailed Description

7.1 Overview

The LM4051-N is a precision voltage reference available in SOT-23 surface mount package. The LM4051-N is available in a 1.225V fixed-option as well as an adjustable voltage option. The LM4051-N comes in three different tolerance grades (A, B, and C). The best grade devices (A) have an initial accuracy of 0.1%, while the B-grade have 0.2% and the C-grade 0.5%, all with a temperature coefficient of 50ppm/°C maintained from -40°C to 125°C.

7.2 Functional Block Diagram



*LM4051-ADJ only **LM4051-1.2 only

7.3 Feature Description

The LM4051-N device is effectively a precision Zener diode. The part requires a small quiescent current for regulation, and regulates the output voltage by shunting more or less current to ground, depending on input voltage and load. The only external component requirement is a resistor between the cathode and the input voltage to set the input current. An external capacitor can be used on the input or output, but is not required.

For the adjustable version, feedback is applied from the Cathode and Reference pins, the LM4051-N behaves as a Zener diode, regulating to a constant voltage dependent on current being supplied into the cathode. This is due to the internal amplifier and reference entering the proper operating regions. The same amount of current needed in the above feedback situation must be applied to this device in open loop, servo or error amplifying implementations to be in the proper linear region giving the LM4051-N enough gain.

7.4 Device Functional Modes

7.4.1 LM4051-N-1.2 V

The LM4051-N-1.2V device is a fixed output voltage part, where the feedback is internal. Therefore, the part can only operate is a closed loop mode and the output voltage cannot be adjusted. The output voltage remains in regulation as long as IR is between IRMIN. Proper selection of the external resistor for input voltage range and load current range makes sure these conditions are met.

7.4.2 LM4051-N - ADJ

The majority of applications involving LM4051-N uses closed loop operation to regulate a fixed voltage or current. The feedback enables this device to behave as an error amplifier, computing a portion of the output voltage and adjusting to maintain the desired regulation. This is done by relating the output voltage back to the reference pin in a manner to be equal to the internal reference voltage, which can be accomplished via resistive or direct feedback.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LM4051-N is a precision micro-power curvature-corrected band gap shunt voltage reference. For space critical applications, the LM4051-N is available in the sub-miniature SOT-23 surface-mount package. The LM4051-N has been designed for stable operation without the need of an external capacitor connected between the "+" pin and the "-" pin. If, however, a bypass capacitor is used, the LM4051-N remains stable. Design effort is further reduced with the choice of either a fixed 1.2V or an adjustable reverse breakdown voltage. The minimum operating current is 60µA for the LM4051-1.2 and the LM4051-ADJ. Both versions have a maximum operating current of 12mA.

LM4051-N's using the SOT-23 package have pin 3 connected as the (–) output through the package's die attach interface. Therefore, the LM4051-1.2's pin 3 must be left floating or connected to pin 2 and the LM4051-ADJ's pin 3 is the (–) output.

The typical thermal hysteresis specification is defined as the change in +25 $^{\circ}$ C voltage measured after thermal cycling. The device is thermal cycled to temperature -40 $^{\circ}$ C and then measured at 25 $^{\circ}$ C. Next the device is thermal cycled to temperature +125 $^{\circ}$ C and again measured at 25 $^{\circ}$ C. The resulting V_{OUT} delta shift between the 25 $^{\circ}$ C measurements is thermal hysteresis. Thermal hysteresis is common in precision references and is induced by thermal-mechanical package stress. Changes in environmental storage temperature, operating temperature and board mounting temperature are all factors that can contribute to thermal hysteresis.

In a conventional shunt regulator application (Figure 8-1), an external series resistor (R_S) is connected between the supply voltage and the LM4051-N. R_S determines the current that flows through the load (I_L) and the LM4051-N (I_Q). Since load current and supply voltage can vary, R_S needs to be small enough to supply at least the minimum acceptable I_Q to the LM4051-N even when the supply voltage is at the minimum and the load current is at the maximum value. When the supply voltage is at the maximum and I_L is at the minimum, R_S needs to be large enough so that the current flowing through the LM4051-N is less than 12mA.

 R_S is selected based on the supply voltage, (V_S) , the desired load and operating current, $(I_L$ and $I_Q)$, and the LM4051-N's reverse breakdown voltage, V_R .

$$R_{\rm S} = \frac{V_{\rm S} - V_{\rm R}}{I_{\rm L} + I_{\rm Q}} \tag{1}$$

The LM4051-ADJ's output voltage can be adjusted to any value in the range of 1.24V through 10V. The output voltage is a function of the internal reference voltage (V_{REF}) and the ratio of the external feedback resistors as shown in Figure 8-3. The output voltage is found using Equation 2:

$$V_{O} = V_{REF} \Big[(R2 / R1) + 1 \Big]$$
(2)

where

V_O is the output voltage



$$R_{S} = \frac{V_{S} - V_{R}}{I_{L} + I_{Q} + I_{F}}$$
(3)

The actual value of the internal V_{REF} is a function of V_O . The *corrected* V_{REF} is determined by Equation 4:

$$V_{REF} = V_{O} \left(\Delta V_{REF} / \Delta V_{O} \right) + V_{Y}$$
(4)

where

V_Y = 1.22V

 $\Delta V_{REF}/\Delta V_{O}$ is found in the *Section 5.6* and is typically -1.55mV/V. You can get a more accurate indication of the output voltage by replacing the value of V_{REF} in Equation 2 with the value found using Equation 4.

8.2 Typical Applications

8.2.1 Shunt Regulator

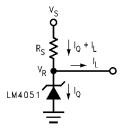


Figure 8-1. Shunt Regulator

8.2.1.1 Design Requirements

 $V_{IN} > V_{OUT}$

Select R_S such that:

 $I_{RMIN} < I_{R} < I_{RMAX}$ where $I_{RMAX} = 12$ mA

See Section 5.5 for minimum operating current for each voltage option and grade.

8.2.1.2 Detailed Design Procedure

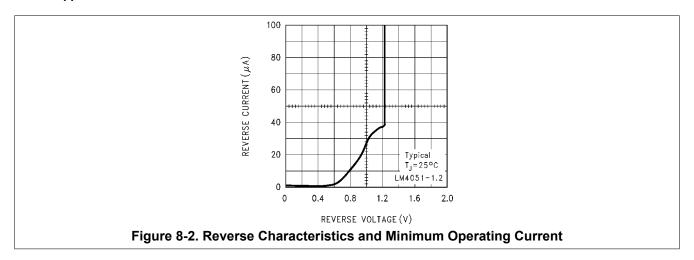
The resistor R_S must be selected such that current, I_R , remains in the operational region of the part for the entire V_{IN} range and load current range. The two extremes to consider are V_{IN} at the maximum, and the load at the minimum, where R_S must be large enough to main $I_R < I_{RMAX}$. For most designs, $0.1 \text{mA} \le I_R \le 1 \text{mA}$ is a good starting point.

Use cross and cross to set R_S between $R_{S\ MIN}$ and $R_{S\ MAX}$.

$$R_{S_MIN} = \frac{V_{IN_MAX} - V_{OUT}}{I_{LOAD_MIN} + I_{R_MAX}}$$
(5)

$$R_{S_MAX} = \frac{V_{IN_MIN} - V_{OUT}}{I_{LOAD_MAX} + I_{R_MIN}}$$
(6)

8.2.1.3 Application Curves



8.2.2 Adjustable Shunt Regulator

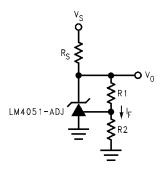


Figure 8-3. Adjustable Shunt Regulator

8.2.2.1 Design Requirements

 $V_{IN} > V_{OUT}$

Select R_S such that:

 $I_{RMIN} < I_{R} < I_{RMAX}$ where $I_{RMAX} = 12mA$

See Section 5.6 for minimum operating current for each voltage option and grade.

8.2.2.2 Detailed Design Procedure

To program the cathode voltage to a regulated voltage a resistive bridge must be shunted between the cathode and anode pins with the mid point tied to the reference pin. This can be seen in Figure 8-3, with R1 & R2 being the resistive bridge. The cathode/output voltage in the shunt regulator configuration can be approximated by the equation shown in Equation 7. The cathode voltage can be more accurately determined by taking in to account the cathode current shown in equation Equation 8.

$$V_{O} = V_{REF}[(R2/R1) + 1]$$

$$V_{O} = (1 + R_2/R_1)x(V_{REF} - I_{REF}xR_1)$$
(8)



For this equation to be valid, LM4051-ADJ must be fully biased so there is enough open loop gain to mitigate any gain error. This can be done be meeting the I_{RMIN} denoted in Section 5.6. When the output voltage, VZ, is set below 2.5V on adjustable versions of LM4051-N, the device can experience increased reference voltage change with output voltage change ($\Delta VREF/\Delta VO$) when compared to output voltages set equal to or above 2.5V

8.3 System Examples

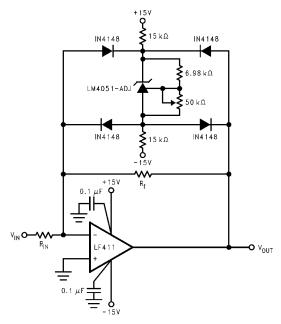


Figure 8-4. Bounded Amplifier Reduces Saturation-induced Delays and Can Prevent Succeeding Stage Damage. Nominal Clamping Voltage is $\pm V_O$ (LM4051-N's Reverse Breakdown Voltage) +2 Diode V_F .

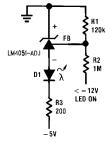


Figure 8-5. Voltage Level Detector

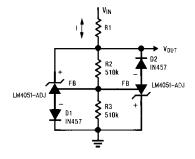


Figure 8-6. Voltage Level Detector

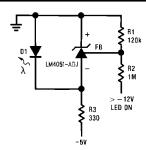


Figure 8-7. Fast Positive Clamp 2.4V + V_{D1}

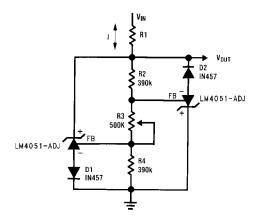


Figure 8-8. Bidirectional Clamp ± 2.4V

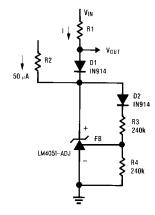


Figure 8-9. Bidirectional Adjustable Clamp ± 18V to ± 2.4V

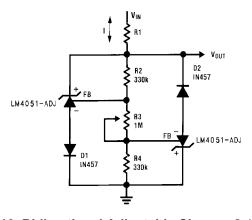


Figure 8-10. Bidirectional Adjustable Clamp ± 2.4V to ± 6V



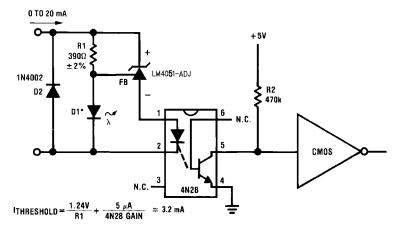
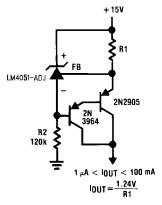


Figure 8-11. Simple Floating Current Detector



*D1 can be any LED, $V_F = 1.5V$ to 2.2V at 3mA. D1 may act as an indicator. D1 will be on if $I_{THRESHOLD}$ falls below the threshold current, except with I = O.

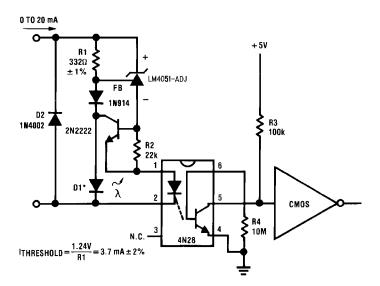


Figure 8-12. Current Source

Figure 8-13. Precision Floating Current Detector

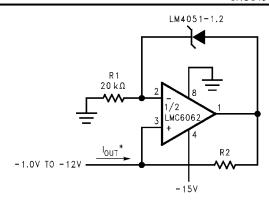


Figure 8-14. Precision 1µA to 1mA Current Source

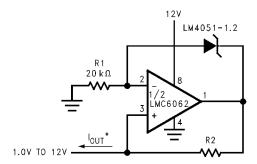


Figure 8-15. Precision 1µA to 1mA Current Source

8.4 Power Supply Recommendations

While a bypass capacitor is not required on the input voltage line, TI recommends reducing noise on the input which can affect the output. A 0.1µF ceramic capacitor or larger is recommended.

To not exceed the maximum cathode current, be sure that the supply current is limited. For applications shunting high currents, pay attention to the cathode and anode trace lengths, adjusting the width of the traces to have proper current density.

8.5 Layout

8.5.1 Layout Guidelines

Place bypass capacitors as close to the device as possible. Current-carrying traces need to have widths appropriate for the amount of current. Place R_S as close as possible to the cathode. Although not as critical, keep feedback resistor close to the device whenever possible.

Product Folder Links: LM4051-N

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8.5.2 Layout Example

R_S physically close to device cathode

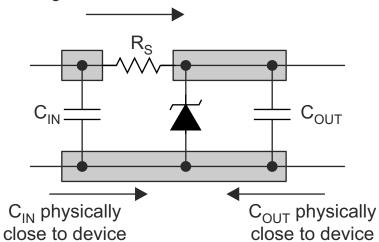


Figure 8-16. Layout Diagram

Rs physically close to device cathode

RS

Cin

R1

Cout

Cout

Cout

Cout physically close to device

Figure 8-17. Feedback Resistors Layout Diagram

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

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9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

C	nanges from Revision D (September 2018) to Revision E (June 2024)	Page
•	Updated Applications links	
	Added information about device behavior in high EMI environments	
•	Added information about device behavior in high EMI environments	3
•	Removed machine model (MM) ESD specification and added CDM ESD specification	4
•	Corrected Equation 7 and Equation 8, added information about device behavior with output voltage le	
•	Added part number clarification for part numbers including "X"	

Changes from Revision C (March 2005) to Revision D (September 2018)

Observes from Devision D (Contember 2040) to Devision E (Ives 2004)

Page

Added Device Information table, Device Comparison table, ESD Ratings table, Feature Description section,
Device Functional Modes, Application and Implementation section, Power Supply Recommendations section,
Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable
Information section.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of

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this document. For browser-based versions of this data sheet, refer to the left-hand navigation. Part numbers containing an "X" contain the same electrical properties as those which do not contain an "X".

Table 11-1. SOT-23 Package Marking Information

PART MARKING		FIELD DEFINITION								
RHA RIA			Third Field:							
RHB RIB	First Field: R = Reference	Second Field: H = 1.225V Voltage Option I = Adjustable	A-C = Initial Reserved Breakdown Voltage or Reference Voltage Tolerance							
RHC RIC			A = ±0.1%, B = ±0.2%, C = ±0.5%							

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
LM4051AIM3-1.2/NO.A	Active	Production	SOT-23 (DBZ) 3	3000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RHA
LM4051AIM3-1.2/NOPB	Active	Production	SOT-23 (DBZ) 3	3000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	RHA
LM4051AIM3-ADJ/NO.A	Active	Production	SOT-23 (DBZ) 3	3000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RIA
LM4051AIM3-ADJ/NOPB	Active	Production	SOT-23 (DBZ) 3	3000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	RIA
LM4051AIM3X-1.2/NO.A	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RHA
LM4051AIM3X-1.2/NOPB	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	RHA
LM4051AIM3X-ADJ/NO.A	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RIA
LM4051AIM3X-ADJ/NOPB	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	RIA
LM4051BEM3-1.2/NO.A	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RHB
LM4051BEM3-1.2/NOPB	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RHB
LM4051BIM3-1.2/NO.A	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RHB
LM4051BIM3-1.2/NOPB	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	RHB
LM4051BIM3-ADJ/NO.A	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RIB
LM4051BIM3-ADJ/NO.B	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RIB
LM4051BIM3-ADJ/NOPB	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	RIB
LM4051BIM3X-1.2/NO.A	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RHB
LM4051BIM3X-1.2/NOPB	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	RHB
LM4051BIM3X-ADJ/NO.A	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RIB
LM4051BIM3X-ADJ/NOPB	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	RIB
LM4051CIM3-1.2/NO.A	Active	Production	SOT-23 (DBZ) 3	3000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RHC
LM4051CIM3-1.2/NOPB	Active	Production	SOT-23 (DBZ) 3	3000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	RHC
LM4051CIM3-ADJ/NO.A	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RIC
LM4051CIM3-ADJ/NOPB	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	RIC
LM4051CIM3X-1.2/NO.A	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RHC
LM4051CIM3X-1.2/NOPB	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	RHC
LM4051CIM3X-ADJ/NO.A	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	RIC
LM4051CIM3X-ADJ/NOPB	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	RIC

⁽¹⁾ Status: For more details on status, see our product life cycle.



PACKAGE OPTION ADDENDUM

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- (2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION





Γ	A0	Dimension designed to accommodate the component width
	В0	Dimension designed to accommodate the component length
	K0	Dimension designed to accommodate the component thickness
	W	Overall width of the carrier tape
	P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4051AIM3-1.2/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM4051AIM3-1.2/NOPB	SOT-23	DBZ	3	3000	180.0	8.4	3.2	2.85	1.3	4.0	8.0	Q3
LM4051AIM3-ADJ/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM4051AIM3X-1.2/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM4051AIM3X-1.2/NOPB	SOT-23	DBZ	3	3000	180.0	8.4	3.2	2.85	1.3	4.0	8.0	Q3
LM4051AIM3X- ADJ/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM4051BEM3-1.2/NOPB	SOT-23	DBZ	3	3000	180.0	8.4	3.2	2.85	1.3	4.0	8.0	Q3
LM4051BEM3-1.2/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM4051BIM3-1.2/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM4051BIM3-1.2/NOPB	SOT-23	DBZ	3	3000	180.0	8.4	3.2	2.85	1.3	4.0	8.0	Q3
LM4051BIM3-ADJ/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM4051BIM3X-1.2/NOPB	SOT-23	DBZ	3	3000	180.0	8.4	3.2	2.85	1.3	4.0	8.0	Q3
LM4051BIM3X-1.2/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM4051BIM3X- ADJ/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM4051CIM3-1.2/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3



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Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4051CIM3-1.2/NOPB	SOT-23	DBZ	3	3000	180.0	8.4	3.2	2.85	1.3	4.0	8.0	Q3
LM4051CIM3-ADJ/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM4051CIM3X-1.2/NOPB	SOT-23	DBZ	3	3000	180.0	8.4	3.2	2.85	1.3	4.0	8.0	Q3
LM4051CIM3X-1.2/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3
LM4051CIM3X- ADJ/NOPB	SOT-23	DBZ	3	3000	178.0	8.4	3.3	2.9	1.22	4.0	8.0	Q3



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4051AIM3-1.2/NOPB	SOT-23	DBZ	3	3000	208.0	191.0	35.0
LM4051AIM3-1.2/NOPB	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LM4051AIM3-ADJ/NOPB	SOT-23	DBZ	3	3000	208.0	191.0	35.0
LM4051AIM3X-1.2/NOPB	SOT-23	DBZ	3	3000	208.0	191.0	35.0
LM4051AIM3X-1.2/NOPB	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LM4051AIM3X-ADJ/NOPB	SOT-23	DBZ	3	3000	208.0	191.0	35.0
LM4051BEM3-1.2/NOPB	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LM4051BEM3-1.2/NOPB	SOT-23	DBZ	3	3000	208.0	191.0	35.0
LM4051BIM3-1.2/NOPB	SOT-23	DBZ	3	3000	208.0	191.0	35.0
LM4051BIM3-1.2/NOPB	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LM4051BIM3-ADJ/NOPB	SOT-23	DBZ	3	3000	208.0	191.0	35.0
LM4051BIM3X-1.2/NOPB	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LM4051BIM3X-1.2/NOPB	SOT-23	DBZ	3	3000	208.0	191.0	35.0
LM4051BIM3X-ADJ/NOPB	SOT-23	DBZ	3	3000	208.0	191.0	35.0
LM4051CIM3-1.2/NOPB	SOT-23	DBZ	3	3000	208.0	191.0	35.0
LM4051CIM3-1.2/NOPB	SOT-23	DBZ	3	3000	210.0	185.0	35.0
LM4051CIM3-ADJ/NOPB	SOT-23	DBZ	3	3000	208.0	191.0	35.0
LM4051CIM3X-1.2/NOPB	SOT-23	DBZ	3	3000	210.0	185.0	35.0



PACKAGE MATERIALS INFORMATION

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4051CIM3X-1.2/NOPB	SOT-23	DBZ	3	3000	208.0	191.0	35.0
LM4051CIM3X-ADJ/NOPB	SOT-23	DBZ	3	3000	208.0	191.0	35.0



SMALL OUTLINE TRANSISTOR



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 This drawing is subject to change without notice.
 Reference JEDEC registration TO-236, except minimum foot length.

- 4. Support pin may differ or may not be present.
- 5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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