SNOSBJ6G – OCTOBER 1999 – REVISED OCTOBER 2018

LMx93-N, LM2903-N Low-Power, Low-Offset Voltage, Dual Comparators

1 Features

- Wide Supply
  - Voltage Range: 2.0 V to 36 V
  - Single or Dual Supplies: ±1.0 V to ±18 V
- Very Low Supply Current Drain (0.4 mA) — Independent of Supply Voltage
- Low Input Biasing Current: 25 nA
- Low Input Offset Current: ±5 nA
- Maximum Offset voltage: ±3 mV
- Input Common-Mode Voltage Range Includes Ground
- Differential Input Voltage Range Equal to the Power Supply Voltage
- Low Output Saturation Voltage: 250 mV at 4 mA
- Output Voltage Compatible with TTL, DTL, ECL, MOS and CMOS logic systems
- Available in the 8-Bump (12 mil) DSBGA Package
- See AN-1112 (SNVA009) for DSBGA Considerations
- Advantages
  - High Precision Comparators
  - Reduced V_{OS} Drift Over Temperature
  - Eliminates Need for Dual Supplies
  - Allows Sensing Near Ground
  - Compatible with All Forms of Logic
  - Power Drain Suitable for Battery Operation

2 Applications

- Battery Powered Applications
- Industrial Applications

3 Description

The LM193-N series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM193-N series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM19-N series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

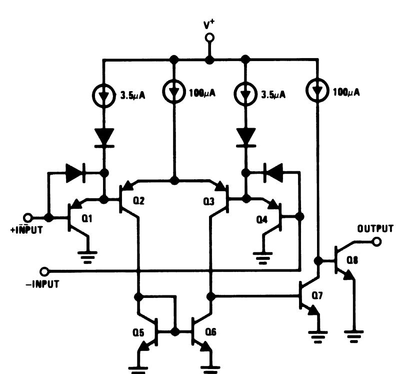
The LM393 and LM2903 parts are available in TI's innovative thin DSBGA package with 8 (12 mil) large bumps.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM193-N	TO-99 (8)	9.08 mm x 9.08 mm
LM293-N		
LM393-N	SOIC (8)	4.90 mm x 3.91 mm
	DSBGA (8)	1.54 mm x 1.54 mm
LM2903-N	SOIC (8)	4.90 mm x 3.91 mm
	DSBGA (8)	1.54 mm x 1.54 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

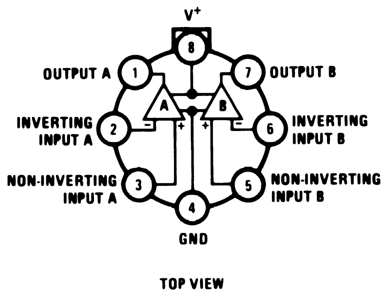
Changes from Revision F (December 2014) to Revision G	Page
• Added DSBGA packages inadvertantly omitted from Device Info table during format conversion	1

Changes from Revision E (March 2013) to Revision F	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

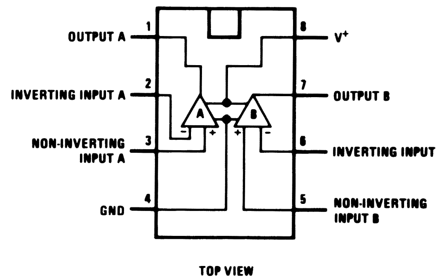
Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	1

5 Pin Configuration and Functions

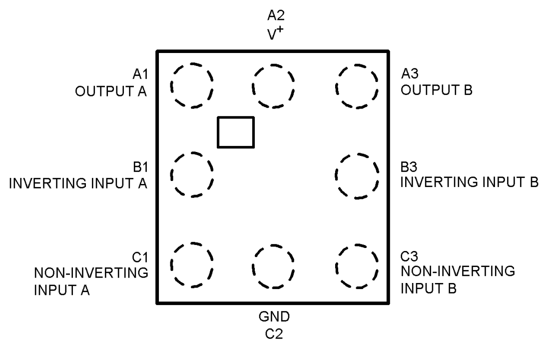
LMC Package
8-Pin TO-99
Top View



P and D Package
8-Pin CDIP, PDIP, SOIC
Top View



YZR Package
8-Pin DSBGA
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	PDIP/SOIC/TO-99	DSBGA		
OUTA	1	A1	O	Output, Channel A
-INA	2	B1	I	Inverting Input, Channel A
+INA	3	C1	I	Noninverting Input, Channel A
GND	4	C2	P	Ground
+INB	5	C3	I	Noninverting Input, Channel B
-INB	6	B3	I	Inverting Input, Channel B
OUTB	7	A3	O	Output, Channel B
V+	8	A2	P	Positive power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

			MIN	MAX	UNIT
Differential Input Voltage (4)				36	V
Input Voltage			−0.3	36	V
Input Current (V_{IN}<−0.3 V) (5)				50	mA
Power Dissipation (6)	PDIP			780	mW
	TO-99			660	mW
	SOIC			510	mW
	DSBGA			568	mW
Output Short-Circuit to Ground (7)				Continuous	
Lead Temperature (Soldering, 10 seconds)				260	°C
Soldering Information	PDIP Package Soldering (10 seconds)			260	°C
	SOIC Package	Vapor Phase (60 seconds)		215	°C
		Infrared (15 seconds)		220	°C
Storage temperature, T_{stg}			-65	150	°C

(1) *Absolute Maximum Ratings* indicate limits beyond which damage may occur. *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.
(2) Refer to RETS193AX for LM193AH military specifications and to RETS193X for LM193H military specifications.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(4) Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3V (or 0.3V below the magnitude of the negative power supply, if used).
(5) This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V.
(6) For operating at high temperatures, the LM393 and LM2903 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 170°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM193/LM193A/LM293 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the “ON-OFF” characteristic of the outputs keeps the chip dissipation very small (P_D≤100 mW), provided the output transistors are allowed to saturate.
(7) Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1300	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply Voltage (V+) - Single Supply	2.0		36	V
Supply Voltage (V+) - Dual Supply	±1.0		±18	V
Operating Input Voltage on (VIN pin)	0		(V+) -1.5V	V
Operating junction temperature, T_J : LM193/LM193A	-55		125	°C
Operating junction temperature, T_J : LM2903	-40		85	°C
Operating junction temperature, T_J : LM293	-25		85	°C
Operating junction temperature, T_J : LM393	0		70	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMx93 TO-99 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	170	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: LM193A V^+= 5 V, T_A = 25°C

Unless otherwise stated.

PARAMETER	TEST CONDITIONS		LM193A MIN	TYP	MAX	UNIT
Input Offset Voltage	See (1).			1.0	2.0	mV
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(−)$ with Output In Linear Range, V_{CM} = 0 V (2)			25	100	nA
Input Offset Current	$I_{IN}(+)−I_{IN}(−)$ V_{CM} = 0 V			3.0	25	nA
Input Common Mode Voltage Range	V+ = 30 V (3)		0		$V^+−1.5$	V
Supply Current	R_L=∞	V^+=5 V		0.4	1	mA
		V^+=36 V		1	2.5	mA
Voltage Gain	R_L≥15 kΩ, V^+=15 V V_O = 1 V to 11 V		50	200		V/mV
Large Signal Response Time	V_{IN}=TTL Logic Swing, V_{REF}=1.4 V V_{RL}=5V, R_L=5.1 kΩ			300		ns
Response Time	V_{RL}=5V, R_L=5.1 kΩ (4)			1.3		μs
Output Sink Current	$V_{IN}(−)$=1V, $V_{IN}(+)$=0, V_O≈1.5 V		6.0	16		mA
Saturation Voltage	$V_{IN}(−)$=1V, $V_{IN}(+)$=0, I_{SINK}≤4 mA			250	400	mV
Output Leakage Current	$V_{IN}(−)$=0, $V_{IN}(+)$=1V, V_O=5 V			0.1		nA

(1) At output switch point, V_O≃1.4V, R_S= 0 Ω with V^+ from 5V to 30V; and over the full input common-mode range (0V to $V^+−1.5$V), at 25°C.
(2) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
(3) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+−1.5$ V at 25°C, but either or both inputs can go to 36 V without damage, independent of the magnitude of V^+.
(4) The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see *LMx93 and LM193A Typical Characteristics* .

6.6 Electrical Characteristics: LM193A (V+ = 5 V)(1)

PARAMETER	TEST CONDITIONS	LM193A MIN	TYP	MAX	UNIT
Input Offset Voltage	See (2)			4.0	mV
Input Offset Current	$I_{IN(+)}−I_{IN(−)}$, V_{CM}=0 V			100	nA
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(−)$ with Output in Linear Range, V_{CM}=0 V (3)			300	nA
Input Common Mode Voltage Range	V^+=30 V (4)	0		$V^+−2.0$	V
Saturation Voltage	$V_{IN}(−)$=1V, $V_{IN}(+)$=0, I_{SINK}≤4 mA			700	mV
Output Leakage Current	$V_{IN}(−)$=0, $V_{IN(+)}$=1V, V_O=30 V			1.0	μA
Differential Input Voltage	Keep All V_{IN}'s≥0 V (or $V^−$, if Used), (5)			36	V

(1) These specifications are limited to −55°C≤T_A≤+125°C, for the LM193/LM193A. With the LM293 all temperature specifications are limited to −25°C≤T_A≤+85°C and the LM393 temperature specifications are limited to 0°C≤T_A≤+70°C. The LM2903 is limited to −40°C≤T_A≤+85°C.
(2) At output switch point, V_O≃1.4V, R_S= 0 Ω with V^+ from 5V to 30V; and over the full input common-mode range (0V to $V^+−1.5$V), at 25°C.
(3) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
(4) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+−1.5$ V at 25°C, but either or both inputs can go to 36 V without damage, independent of the magnitude of V^+.
(5) Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3V (or 0.3V below the magnitude of the negative power supply, if used).

6.7 Electrical Characteristics: LMx93 and LM2903 V^+= 5 V, T_A = 25°C

Unless otherwise stated.

PARAMETER	TEST CONDITIONS		LM193-N			LM293-N, LM393-N			LM2903-N			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	See [1]			1.0	5.0		1.0	5.0		2.0	7.0	mV
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output In Linear Range, V_{CM} = 0 V [2]			25	100		25	250		25	250	nA
Input Offset Current	$I_{IN}(+)-I_{IN}(-)$ V_{CM} = 0 V			3.0	25		5.0	50		5.0	50	nA
Input Common Mode Voltage Range	V+ = 30 V [3]		0		V+−1.5	0		V+−1.5	0		V+−1.5	V
Supply Current	R_L=∞	V^+=5 V		0.4	1		0.4	1		0.4	1.0	mA
		V^+=36 V		1	2.5		1	2.5		1	2.5	mA
Voltage Gain	R_L≥15 kΩ, V^+=15 V V_O = 1 V to 11 V		50	200		50	200		25	100		V/mV
Large Signal Response Time	V_{IN}=TTL Logic Swing, V_{REF}=1.4 V V_{RL}=5 V, R_L=5.1 kΩ			300			300			300		ns
Response Time	V_{RL}=5 V, R_L=5.1 kΩ [4]			1.3			1.3			1.5		μs
Output Sink Current	$V_{IN}(-)$=1 V, $V_{IN}(+)$=0, V_O≤1.5 V		6.0	16		6.0	16		6.0	16		mA
Saturation Voltage	$V_{IN}(-)$=1 V, $V_{IN}(+)$=0, I_{SINK}≤4 mA			250	400		250	400		250	400	mV
Output Leakage Current	$V_{IN}(-)$=0, $V_{IN}(+)$=1V, V_O=5 V			0.1			0.1			0.1		nA

(1) At output switch point, V_O≃1.4V, R_S= 0 Ω with V^+ from 5V to 30V; and over the full input common-mode range (0V to V^+−1.5V), at 25°C.
(2) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
(3) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+−1.5 V at 25°C, but either or both inputs can go to 36 V without damage, independent of the magnitude of V^+.
(4) The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see *LMx93 and LM193A Typical Characteristics* .

6.8 Electrical Characteristics: LMx93 and LM2903 (V+ = 5 V)(1)

PARAMETER	TEST CONDITIONS	LM193-N			LM293-N, LM393-N			LM290-N			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	See (2)			9			9		9	15	mV
Input Offset Current	$I_{IN(+)}-I_{IN(-)}$, V_{CM}=0 V			100			150		50	200	nA
Input Bias Current	I_{IN}(+) or I_{IN}(−) with Output in Linear Range, V_{CM}=0 V (3)			300			400		200	500	nA
Input Common Mode Voltage Range	V^+=30V (4)	0		V^+−2.0	0		V^+−2.0	0		V^+−2.0	V
Saturation Voltage	V_{IN}(−)=1V, V_{IN}(+)=0, I_{SINK}≤4 mA			700			700		400	700	mV
Output Leakage Current	V_{IN}(−)=0, $V_{IN(+)}$=1V, V_O=30 V			1.0			1.0			1.0	µA
Differential Input Voltage	Keep All V_{IN}'s≥0 V (or V^-, if Used), (5)			36			36			36	V

(1) These specifications are limited to −55°C≤T_A≤+125°C, for the LM193/LM193A. With the LM293 all temperature specifications are limited to −25°C≤T_A≤+85°C and the LM393 temperature specifications are limited to 0°C≤T_A≤+70°C. The LM2903 is limited to −40°C≤T_A≤+85°C.
(2) At output switch point, V_O≃1.4V, R_S= 0 Ω with V^+ from 5V to 30V; and over the full input common-mode range (0V to V^+−1.5V), at 25°C.
(3) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
(4) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+−1.5 V at 25°C, but either or both inputs can go to 36 V without damage, independent of the magnitude of V^+.
(5) Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3V (or 0.3V below the magnitude of the negative power supply, if used).

6.9 Typical Characteristics: LMx93 and LM193A

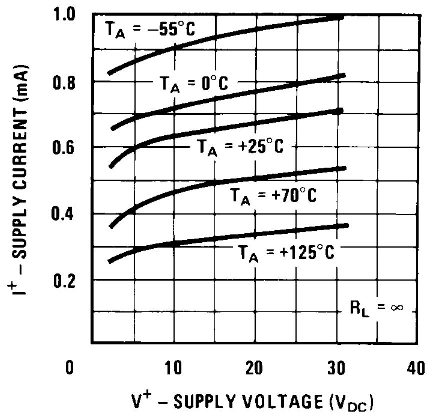


Figure 1. Supply Current

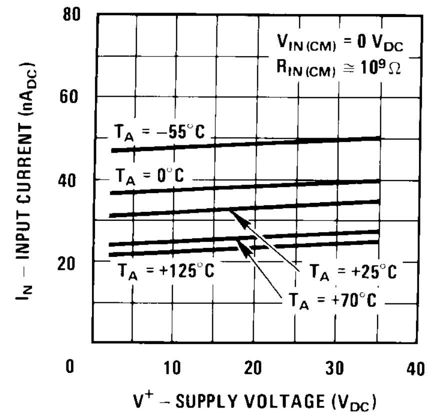


Figure 2. Input Current

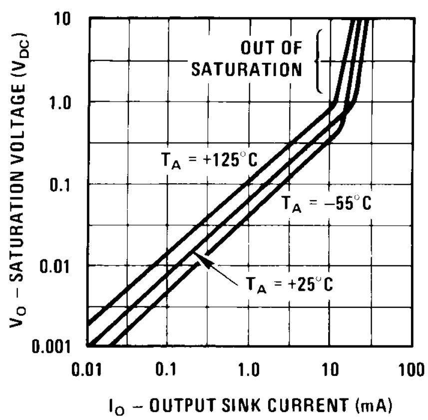


Figure 3. Output Saturation Voltage

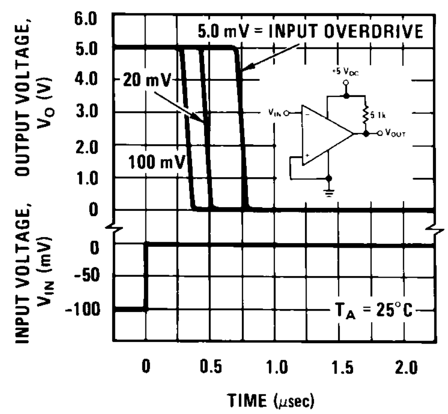


Figure 4. Response Time for Various Input Overdrives—Negative Transition

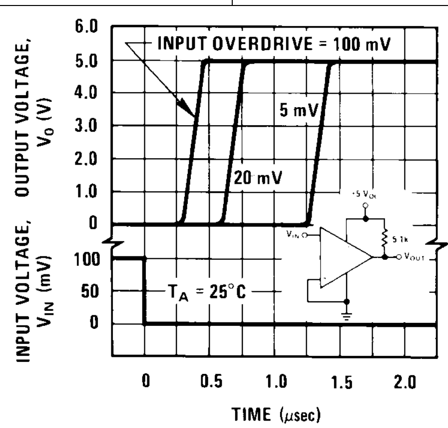


Figure 5. Response Time for Various Input Overdrives—Positive Transition

6.10 Typical Characteristics: LM2903

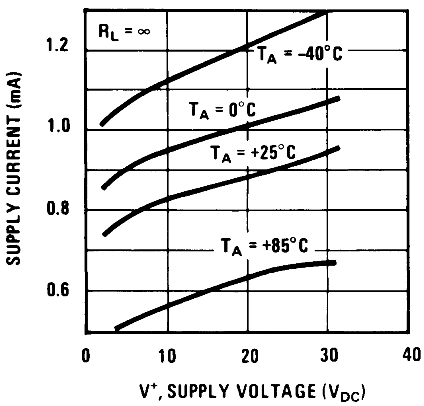


Figure 6. Supply Current

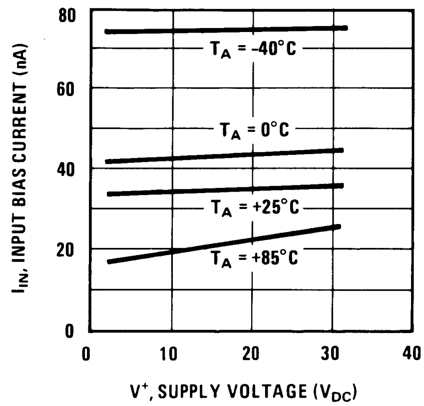


Figure 7. Input Current

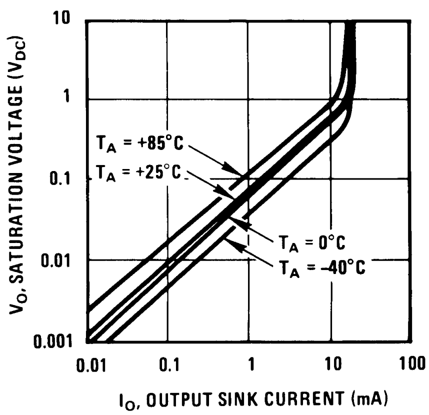


Figure 8. Output Saturation Voltage

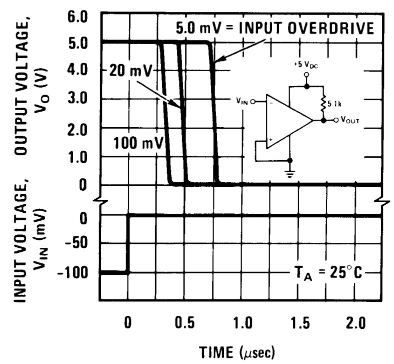


Figure 9. Response Time for Various Input Overdrives—Negative Transition

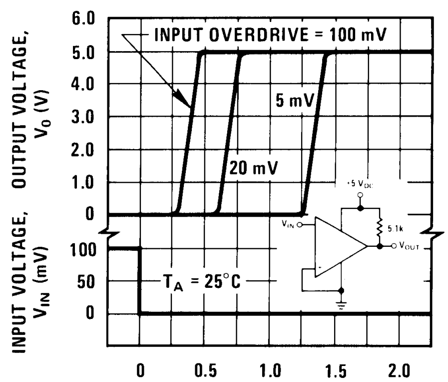


Figure 10. Response Time for Various Input Overdrives—Positive Transition

7 Detailed Description

7.1 Overview

The LM139 provides two independently functioning, high-precision, low V_{OS} drift, low input bias current comparators in a single package. The low power consumption of 0.4 mA at 5 V and the 2.0 V supply operation makes the LM139 suitable for battery powered applications.

7.2 Functional Block Diagram

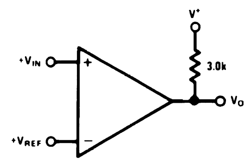


Figure 11. Basic Comparator

7.3 Feature Description

The input bias current of 25 nA enables the LM193 to use even very high impedance nodes as inputs. The differential voltage input range equals the supply voltage range.

The LM193 can be operated with a single supply, where V+ can be from 2.0 V to 36 V, or in a dual supply voltage configuration, where GND pin is used as a V– supply. The supply current draws only 0.4 mA for both comparators.

The output of each comparator in the LM193 is the open collector of a grounded-emitter NPN output transistor which can typically draw up to 16 mA.

7.4 Device Functional Modes

A basic comparator circuit is used for converting analog signals to a digital output. The output is HIGH when the voltage on the non-inverting (+IN) input is greater than the inverting (-IN) input. The output is LOW when the voltage on the non-inverting (+IN) input is less than the inverting (-IN) input. The inverting input (-IN) is also commonly referred to as the "reference" or "VREF" input. All pins of any unused comparators should be tied to the negative supply.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM193 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator change states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to < 10 kΩ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All input pins of any unused comparators should be tied to the negative supply.

The bias network of the LM193 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2.0 V_{DC} to 30 V_{DC}.

The differential input voltage may be larger than V^+ without damaging the device*Typical Applications* . Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in *Typical Applications* .

The output of the LM193 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pullup resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM193 package. The output can also be used as a simple SPST switch to ground (when a pullup resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60 Ω r_{SAT} of the output transistor. The low offset voltage of the output transistor (1.0 mV) allows the output to clamp essentially to ground level for small load currents.

8.2 Typical Applications

8.2.1 Basic Comparator

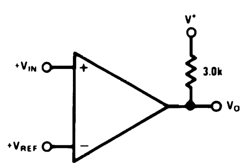


Figure 12. Basic Comparator

8.2.1.1 Design Requirements

The basic usage of a comparator is to indicate when a specific analog signal has exceeded some predefined threshold. In this application, the negative input (IN–) is tied to a reference voltage, and the positive input (IN+) is connected to the input signal. The output is pulled up with a resistor to the logic supply voltage, V+ with a pullup resistor.

For an example application, the supply voltage is 5V. The input signal varies between 1 V and 3 V, and we want to know when the input exceeds 2.5 V±1%. The supply current draw should not exceed 1 mA.

Typical Applications (continued)

8.2.1.2 Detailed Design Procedure

First, we determine the biasing for the 2.5-V reference. With the 5-V supply voltage, we would use a voltage divider consisting of one resistor from the supply to IN- and an second resistor from IN–. The 25 nA of input current bias should be < 1% of the bias current for Vref. With a 100-kΩ resistor from IN– to V+ and an additional 100-KΩ resistor from IN– to ground, there would be 25 µA of current through the two resistors. The 3-kΩ pullup shown will need 5 V/3 kΩ → 1.67 mA, which exceeds our current budget.

With the 400-µA supply current and 25 µA of VREF bias current, there is 575 µA remaining for output pullup resistor; with 5-V supply, we need a pullup larger than 8.7 kΩ. A 10-kΩ pullup is a value that is commonly available and can be used here.

8.2.1.3 Application Curve

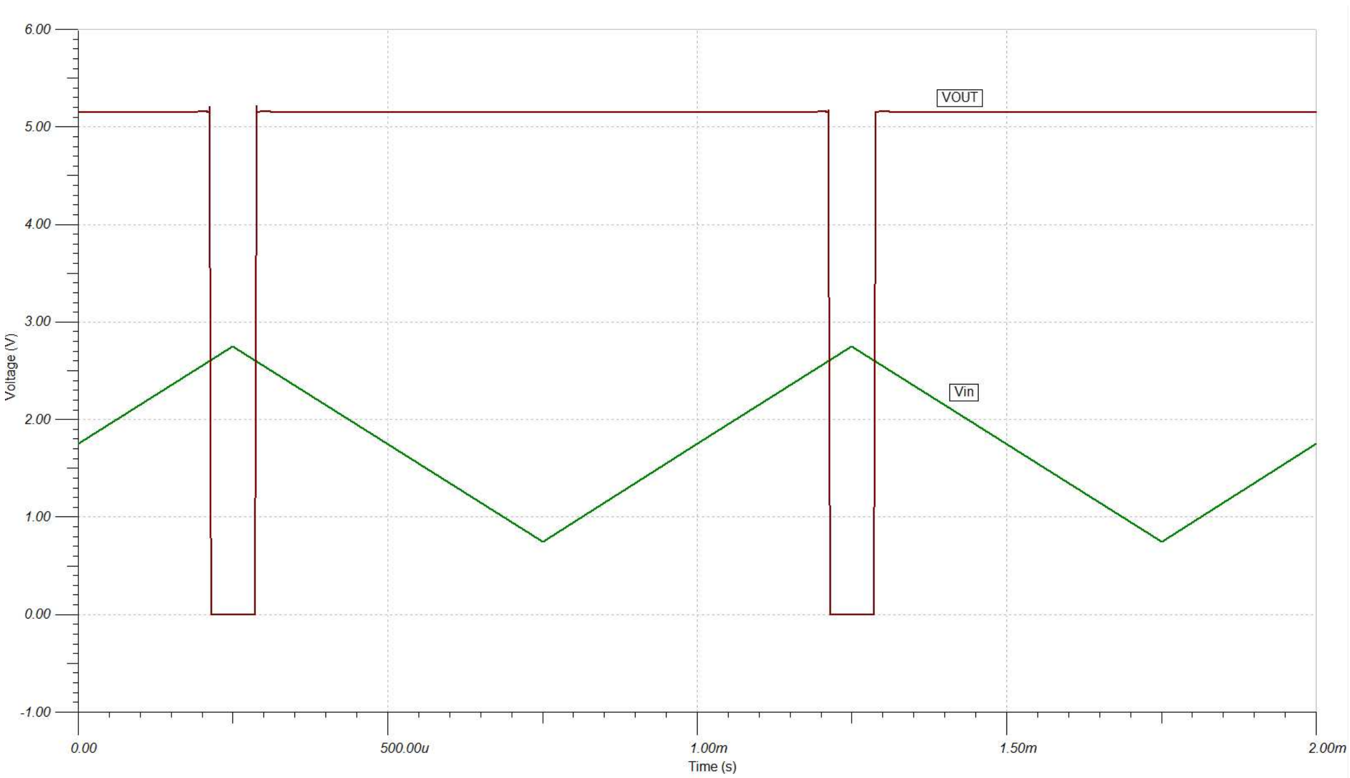
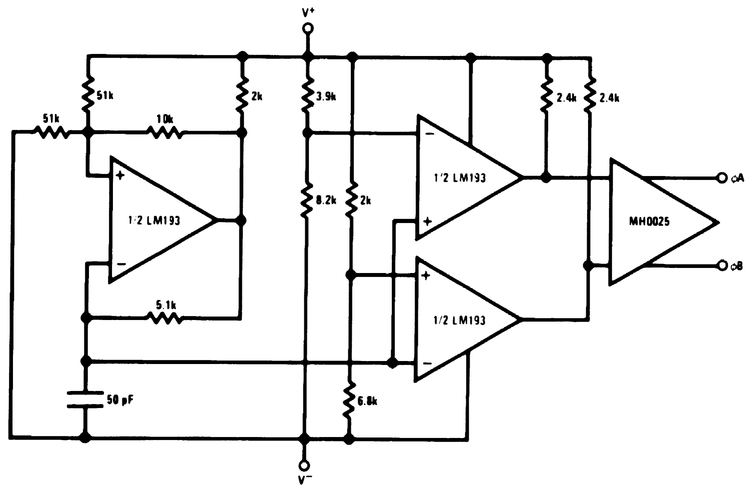


Figure 13. Basic Comparator Response

Typical Applications (continued)

8.2.2 System Examples

8.2.2.1 Split-Supply Application



(V+=-15 V_{DC} and V-=-15 V_{DC})

Figure 14. MOS Clock Driver

8.2.2.2 V+ = 5.0 V_{DC} Application Circuits

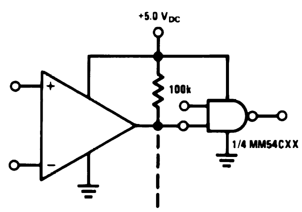


Figure 15. Driving CMOS

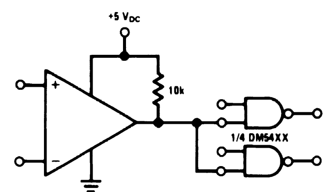


Figure 16. Driving TTL

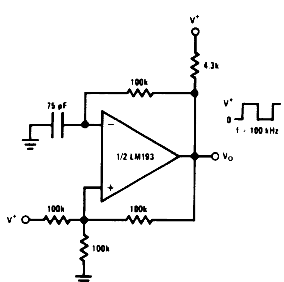
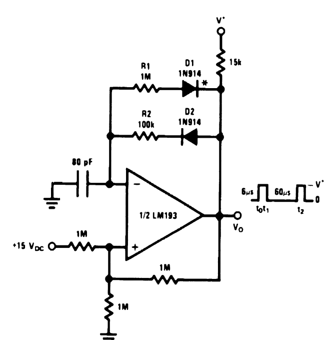


Figure 17. Squarewave Oscillator



* For large ratios of R1/R2,
D1 can be omitted.

Figure 18. Pulse Generator

Typical Applications (continued)

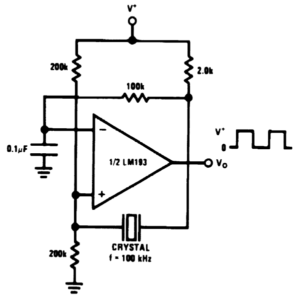
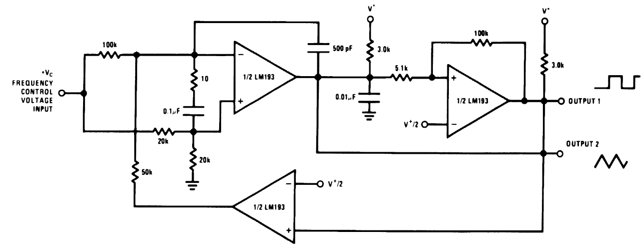


Figure 19. Crystal Controlled Oscillator



$V^* = +30\ V_{DC}$

$+250\ mV_{DC} \le V_C \le +50\ V_{DC}$

$700Hz \le f_o \le 100kHz$

Figure 20. Two-Decade High Frequency VCO

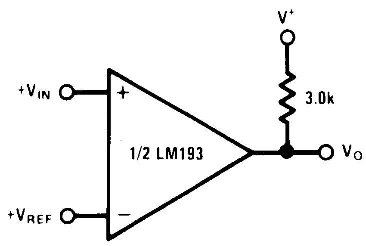


Figure 21. Basic Comparator

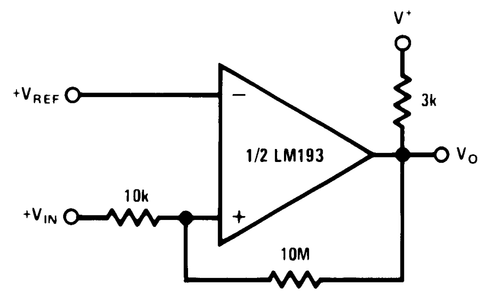


Figure 22. Non-Inverting Comparator With Hysteresis

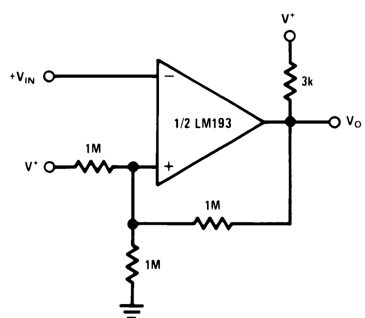


Figure 23. Inverting Comparator With Hysteresis

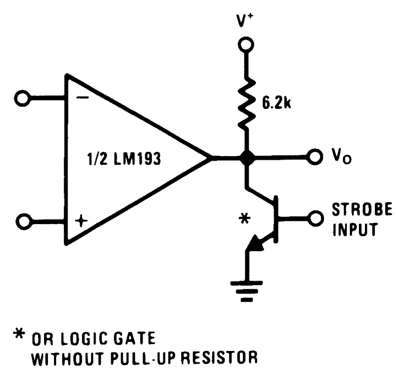


Figure 24. Output Strobing

Typical Applications (continued)

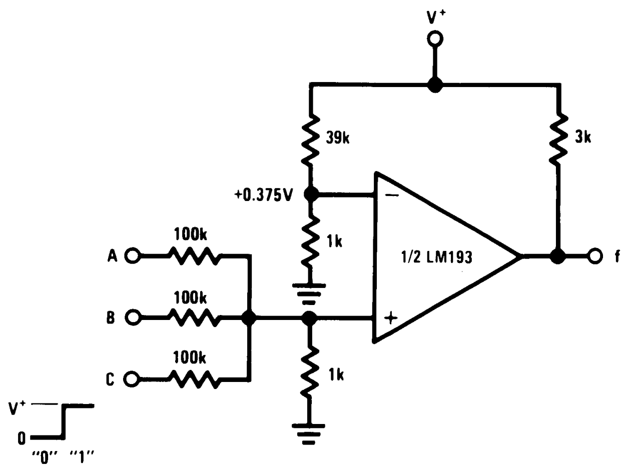


Figure 25. And Gate

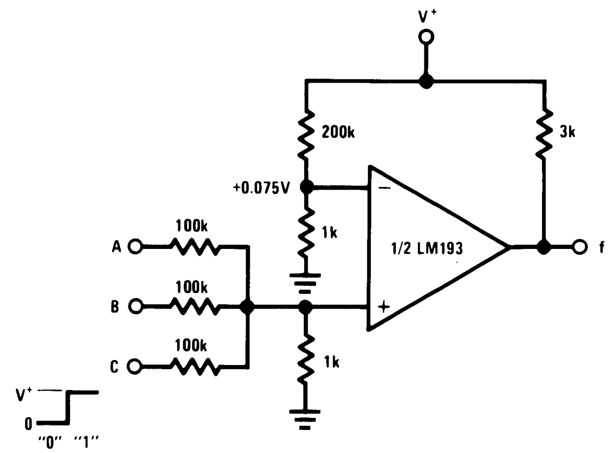


Figure 26. Or Gate

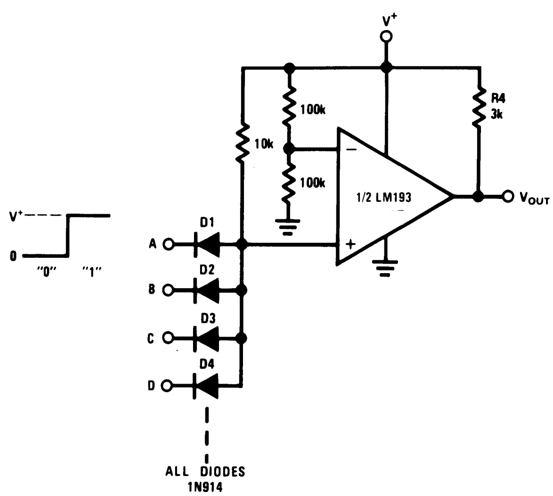


Figure 27. Large Fan-In and Gate

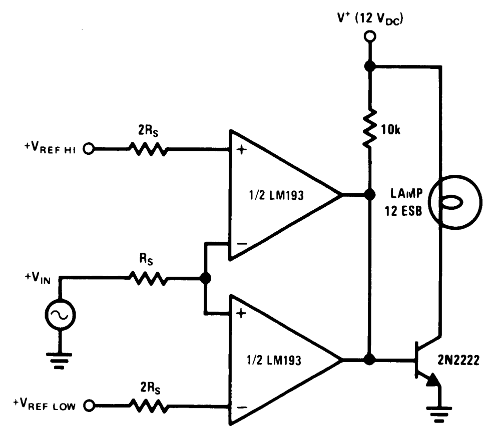


Figure 28. Limit Comparator

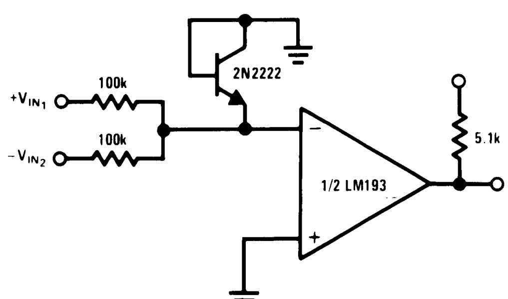


Figure 29. Comparing Input Voltages of Opposite Polarity

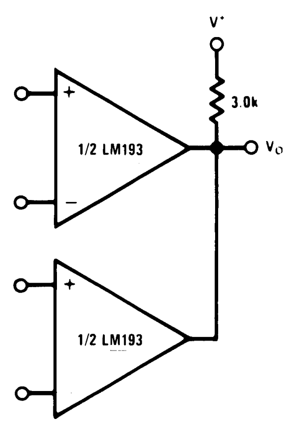


Figure 30. Oring the Outputs

Typical Applications (continued)

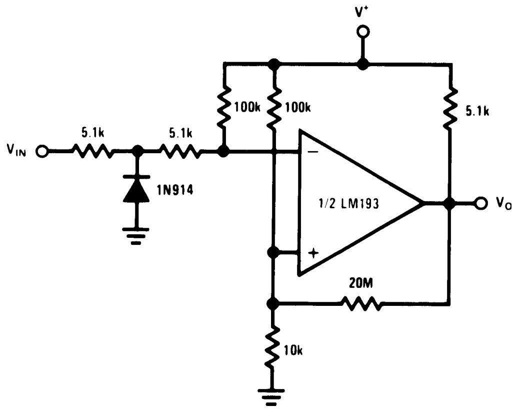


Figure 31. Zero Crossing Detector (Single Power Supply)

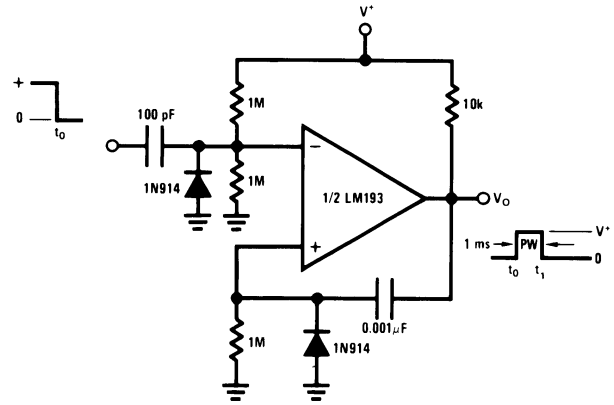


Figure 32. One-Shot Multivibrator

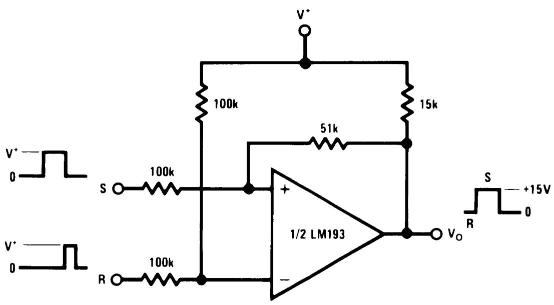


Figure 33. Bi-Stable Multivibrator

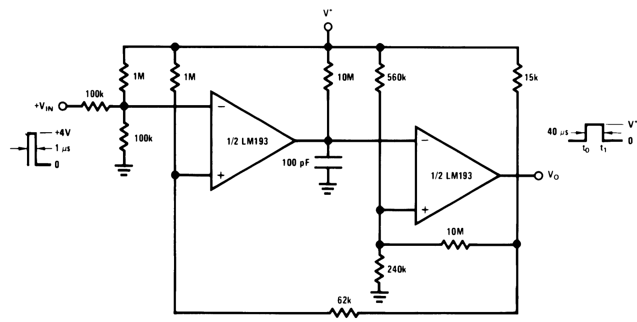


Figure 34. One-Shot Multivibrator With Input Lock Out

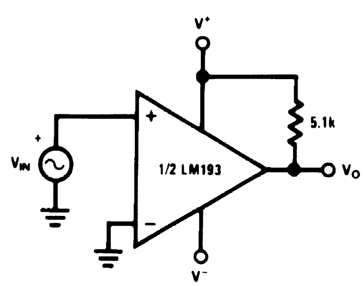


Figure 35. Zero Crossing Detector

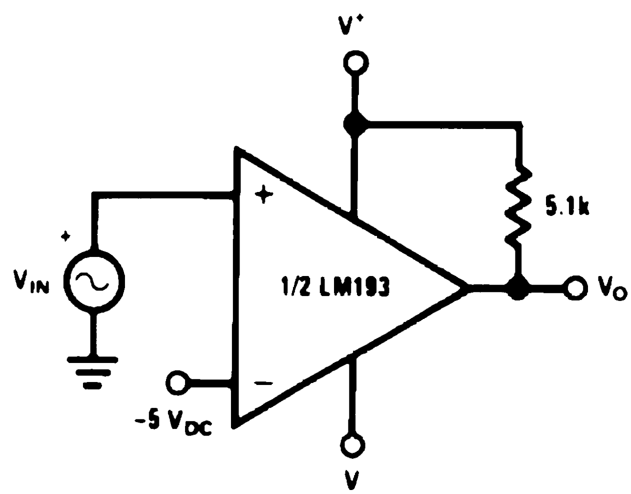


Figure 36. Comparator With a Negative Reference

Typical Applications (continued)

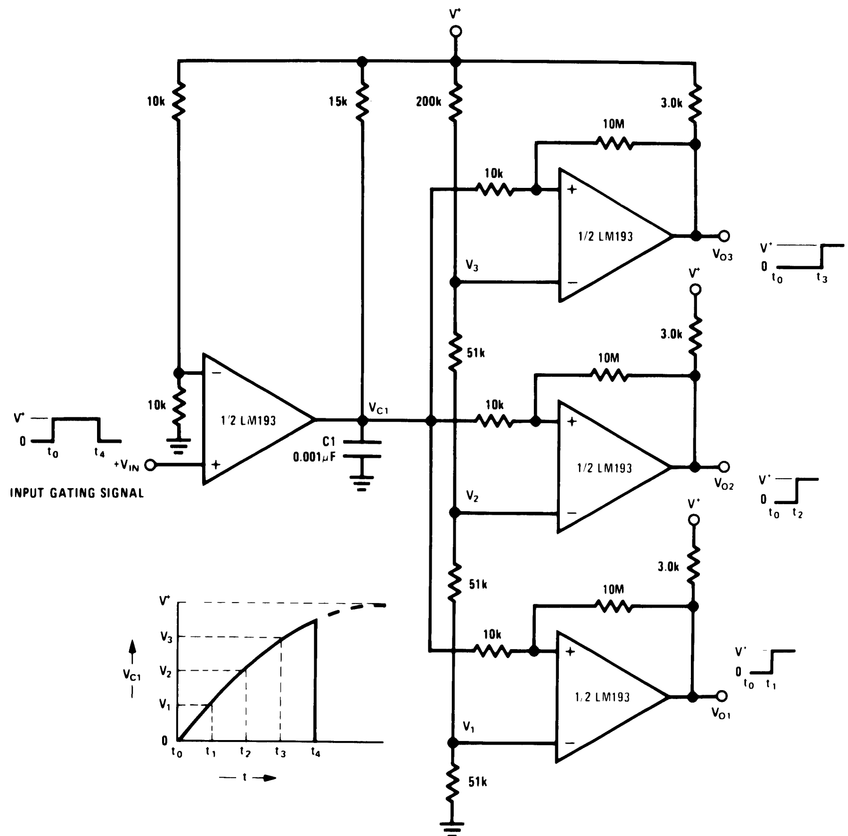


Figure 37. Time Delay Generator

9 Power Supply Recommendations

Even in low frequency applications, the LM139-N can have internal transients which are extremely quick. For this reason, bypassing the power supply with 1.0 μF to ground will provide improved performance; the supply bypass capacitor should be placed as close as possible to the supply pin and have a solid connection to ground. The bypass capacitor should have a low ESR and also a SRF greater than 50MHz.

10 Layout

10.1 Layout Guidelines

Try to minimize parasitic impedances on the inputs to avoid oscillation. Any positive feedback used as hysteresis should place the feedback components as close as possible to the input pins. Care should be taken to ensure that the output pins do not couple to the inputs. This can occur through capacitive coupling if the traces are too close and lead to oscillations on the output. The optimum placement for the bypass capacitor is closest to the V+ and ground pins. Take care to minimize the loop area formed by the bypass capacitor connection between V+ and ground. The ground pin should be connected to the PCB ground plane at the pin of the device. The feedback components should be placed as close to the device as possible minimizing strays.

10.2 Layout Example

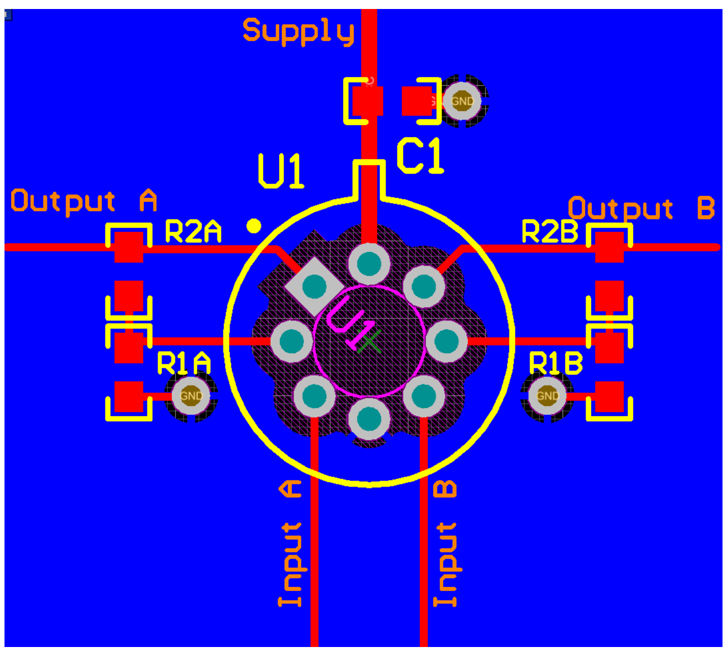


Figure 38. Layout Example

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM193-N	Click here	Click here	Click here	Click here	Click here
LM2903-N	Click here	Click here	Click here	Click here	Click here
LM293-N	Click here	Click here	Click here	Click here	Click here
LM393-N	Click here	Click here	Click here	Click here	Click here

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM193AH	Active	Production	TO-99 (LMC) | 8	500 | OTHER	No	Call TI	Level-1-NA-UNLIM	-55 to 125	(LM193AH, LM193AH)
LM193AH/NOPB	Active	Production	TO-99 (LMC) | 8	500 | OTHER	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	(LM193AH, LM193AH)
LM193H	Active	Production	TO-99 (LMC) | 8	500 | OTHER	No	Call TI	Level-1-NA-UNLIM	-55 to 125	(LM193H, LM193H)
LM193H/NOPB	Active	Production	TO-99 (LMC) | 8	500 | OTHER	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	(LM193H, LM193H)
LM2903ITL/NOPB	Active	Production	DSBGA (YZR) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C 03
LM2903ITL/NOPB.B	Active	Production	DSBGA (YZR) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C 03
LM2903ITLX/NOPB	Active	Production	DSBGA (YZR) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C 03
LM2903ITLX/NOPB.B	Active	Production	DSBGA (YZR) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C 03
LM2903M	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	LM 2903M
LM2903M/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM 2903M
LM2903M/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM 2903M
LM2903MX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM 2903M
LM2903MX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM 2903M
LM2903N/NOPB	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LM 2903N
LM2903N/NOPB.B	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LM 2903N
LM293H	Active	Production	TO-99 (LMC) | 8	500 | TRAY NON-STD	No	Call TI	Level-1-NA-UNLIM	-25 to 85	(LM293H, LM293H)
LM293H/NOPB	Active	Production	TO-99 (LMC) | 8	500 | OTHER	Yes	Call TI	Level-1-NA-UNLIM	-25 to 85	(LM293H, LM293H)
LM393M	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	LM 393M

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM393M/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM 393M
LM393M/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM 393M
LM393MX	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	LM 393M
LM393MX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM 393M
LM393MX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 70	LM 393M
LM393N/NOPB	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	0 to 70	LM 393N
LM393N/NOPB.B	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	0 to 70	LM 393N
LM393TL/NOPB	Active	Production	DSBGA (YZR) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 70	C 02
LM393TL/NOPB.B	Active	Production	DSBGA (YZR) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 70	C 02
LM393TLX/NOPB	Active	Production	DSBGA (YZR) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 70	C 02
LM393TLX/NOPB.B	Active	Production	DSBGA (YZR) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 70	C 02

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM2903-N, LM293-N :

- Automotive : LM2903-Q1

- Enhanced Product : LM293-EP

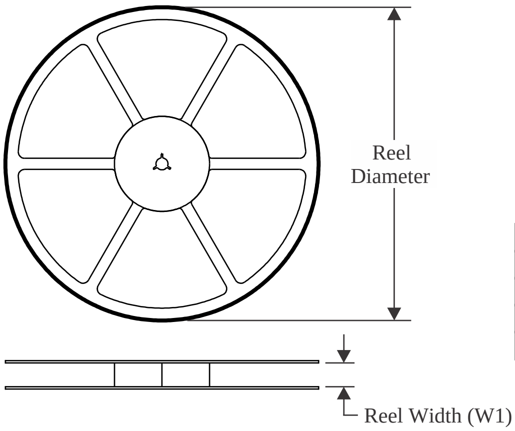
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

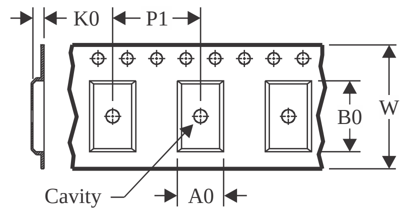
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

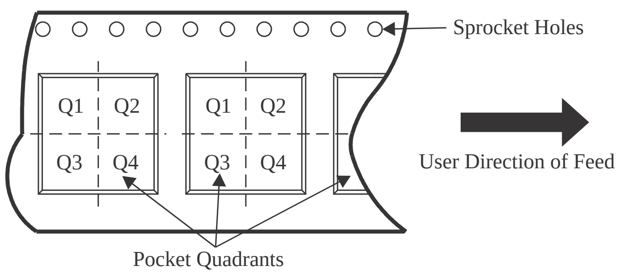


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

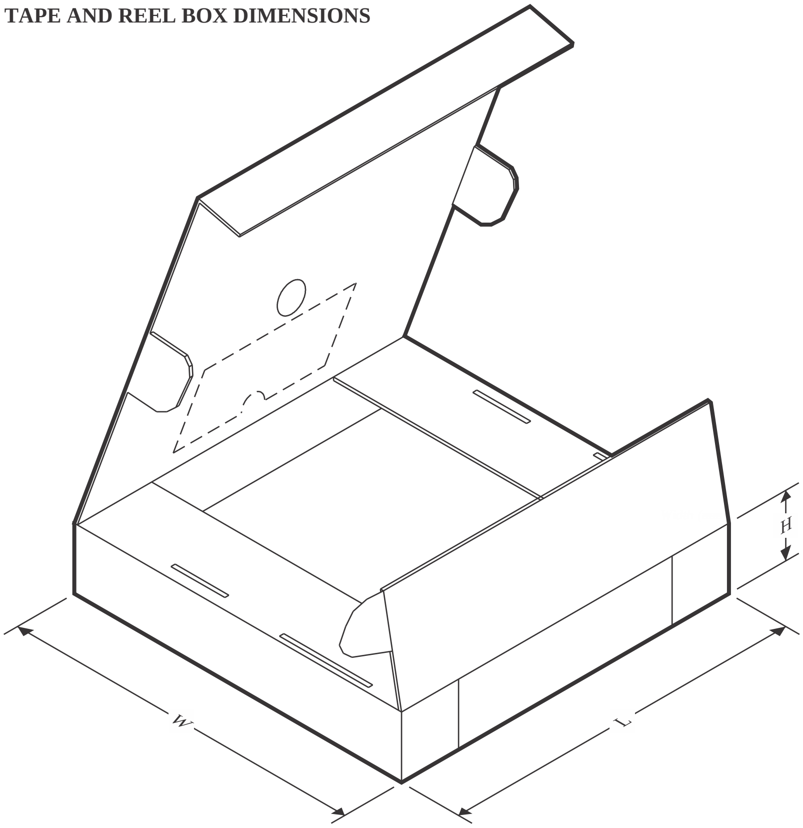
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2903ITL/NOPB	DSBGA	YZR	8	250	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1
LM2903ITLX/NOPB	DSBGA	YZR	8	3000	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1
LM2903MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM393MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM393TL/NOPB	DSBGA	YZR	8	250	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1
LM393TLX/NOPB	DSBGA	YZR	8	3000	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1

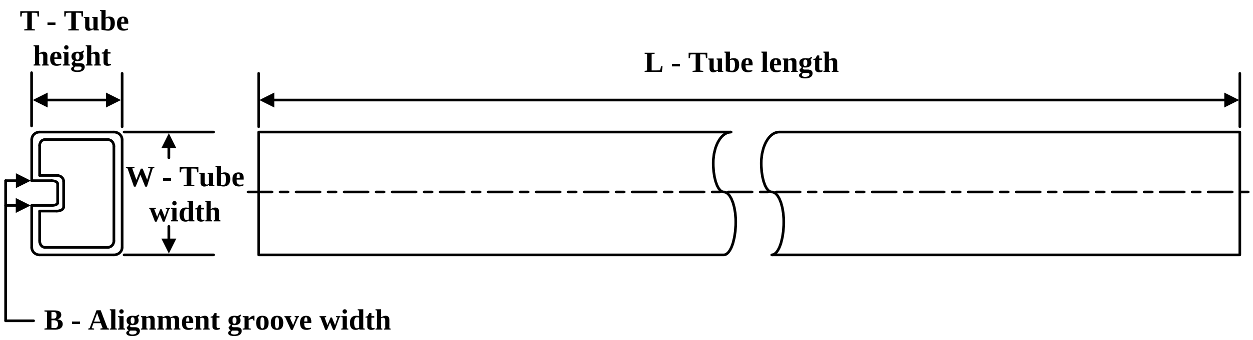
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2903ITL/NOPB	DSBGA	YZR	8	250	208.0	191.0	35.0
LM2903ITLX/NOPB	DSBGA	YZR	8	3000	208.0	191.0	35.0
LM2903MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM393MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM393TL/NOPB	DSBGA	YZR	8	250	208.0	191.0	35.0
LM393TLX/NOPB	DSBGA	YZR	8	3000	208.0	191.0	35.0

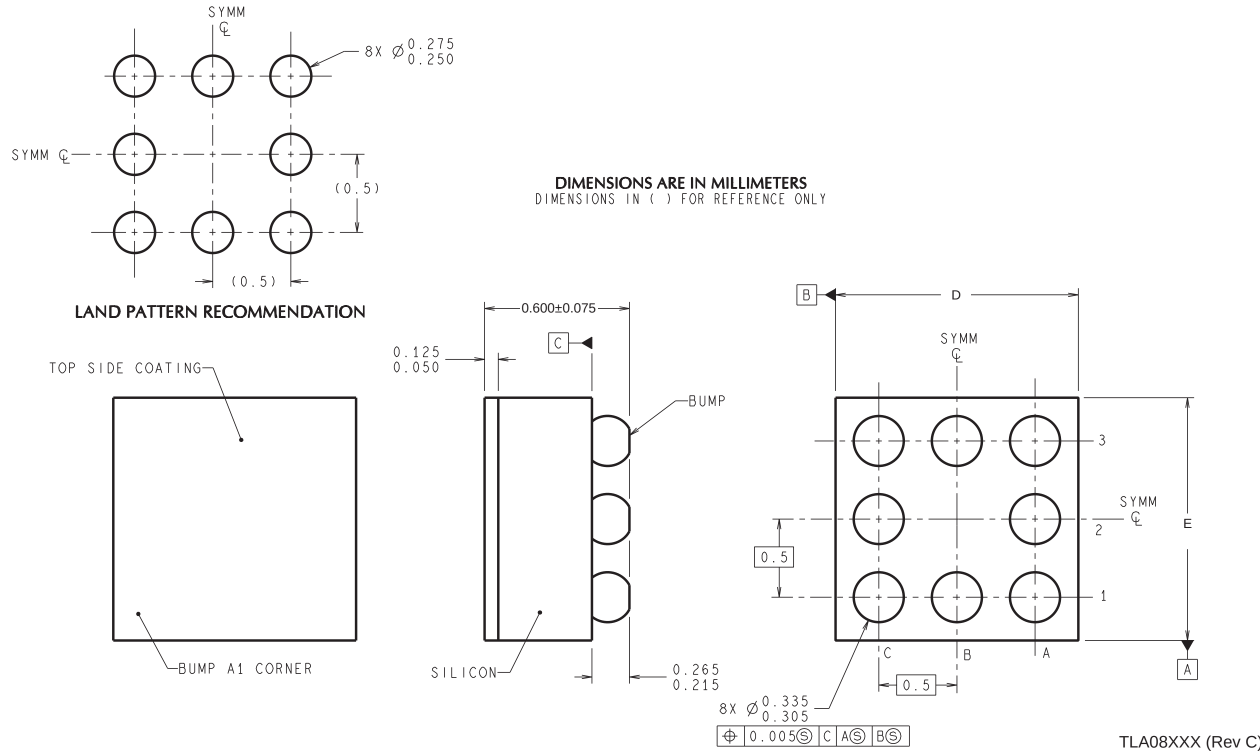
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM2903M/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM2903M/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LM2903N/NOPB	P	PDIP	8	40	502	14	11938	4.32
LM2903N/NOPB.B	P	PDIP	8	40	502	14	11938	4.32
LM393M/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM393M/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LM393N/NOPB	P	PDIP	8	40	502	14	11938	4.32
LM393N/NOPB.B	P	PDIP	8	40	502	14	11938	4.32

YZR0008

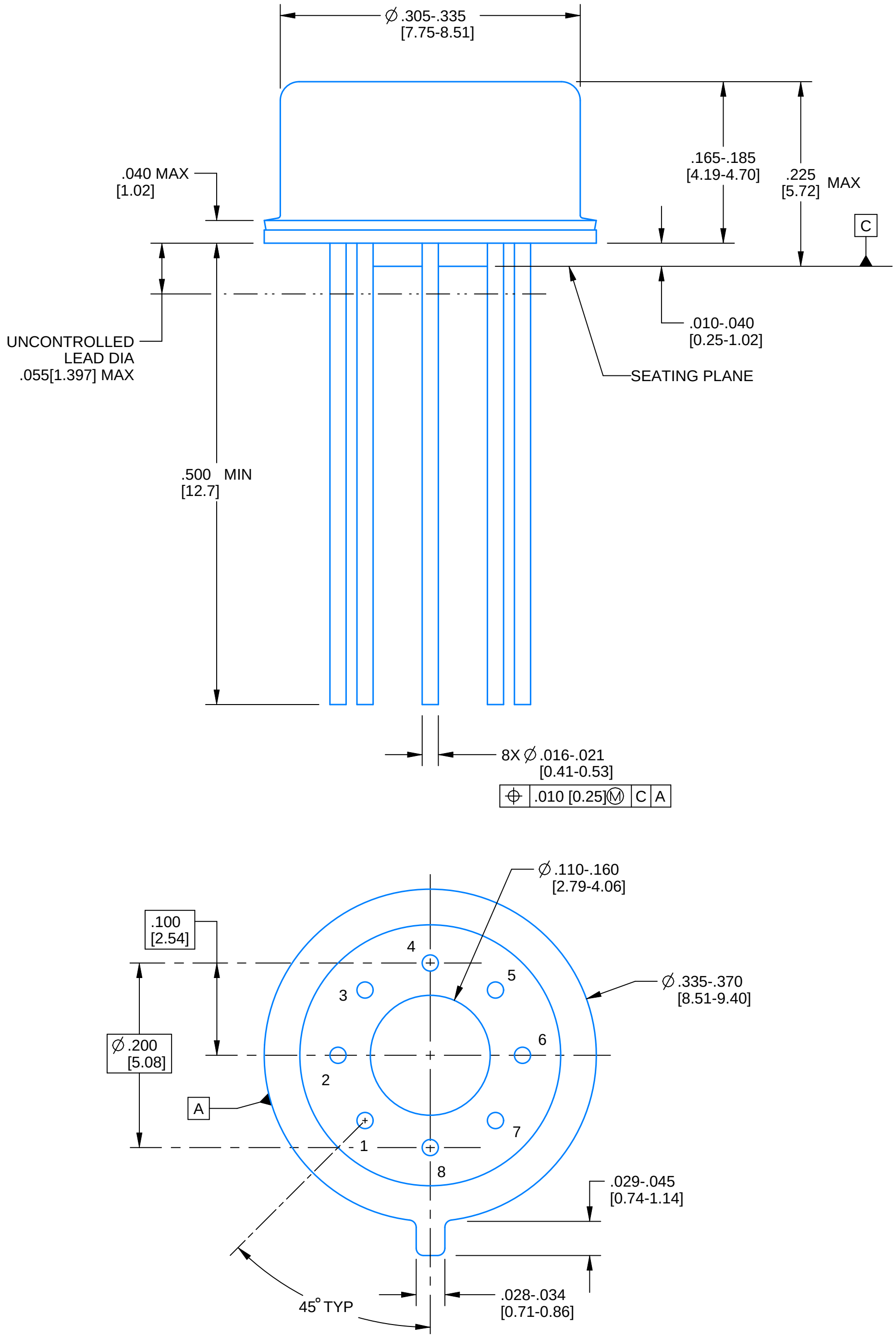


D: Max = 1.54 mm, Min = 1.479 mm

E: Max = 1.54 mm, Min = 1.479 mm

4215045/A 12/12

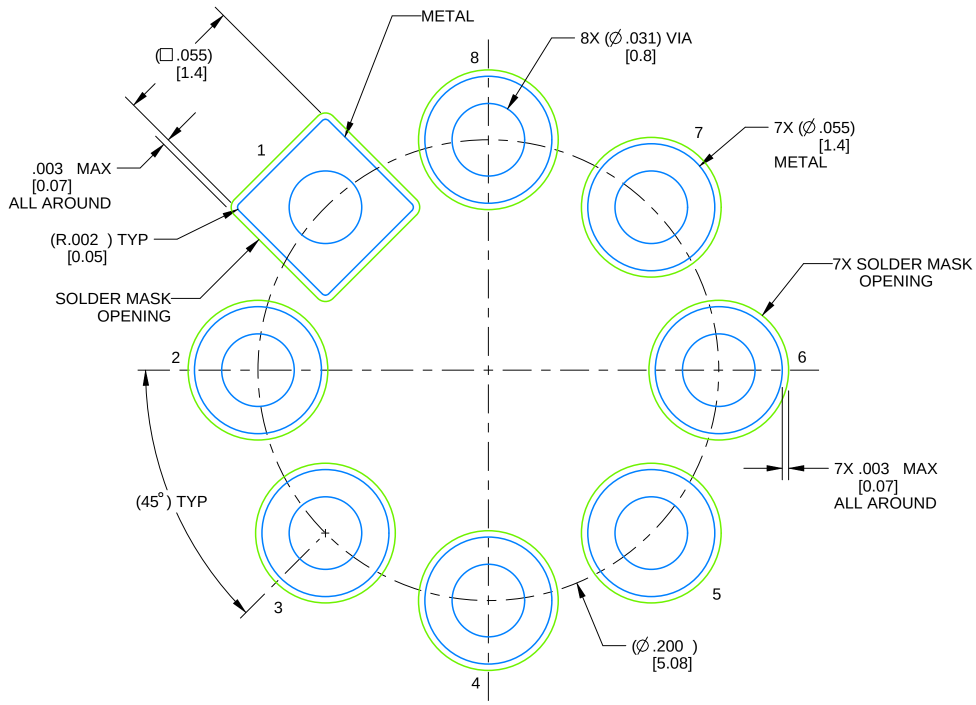
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.



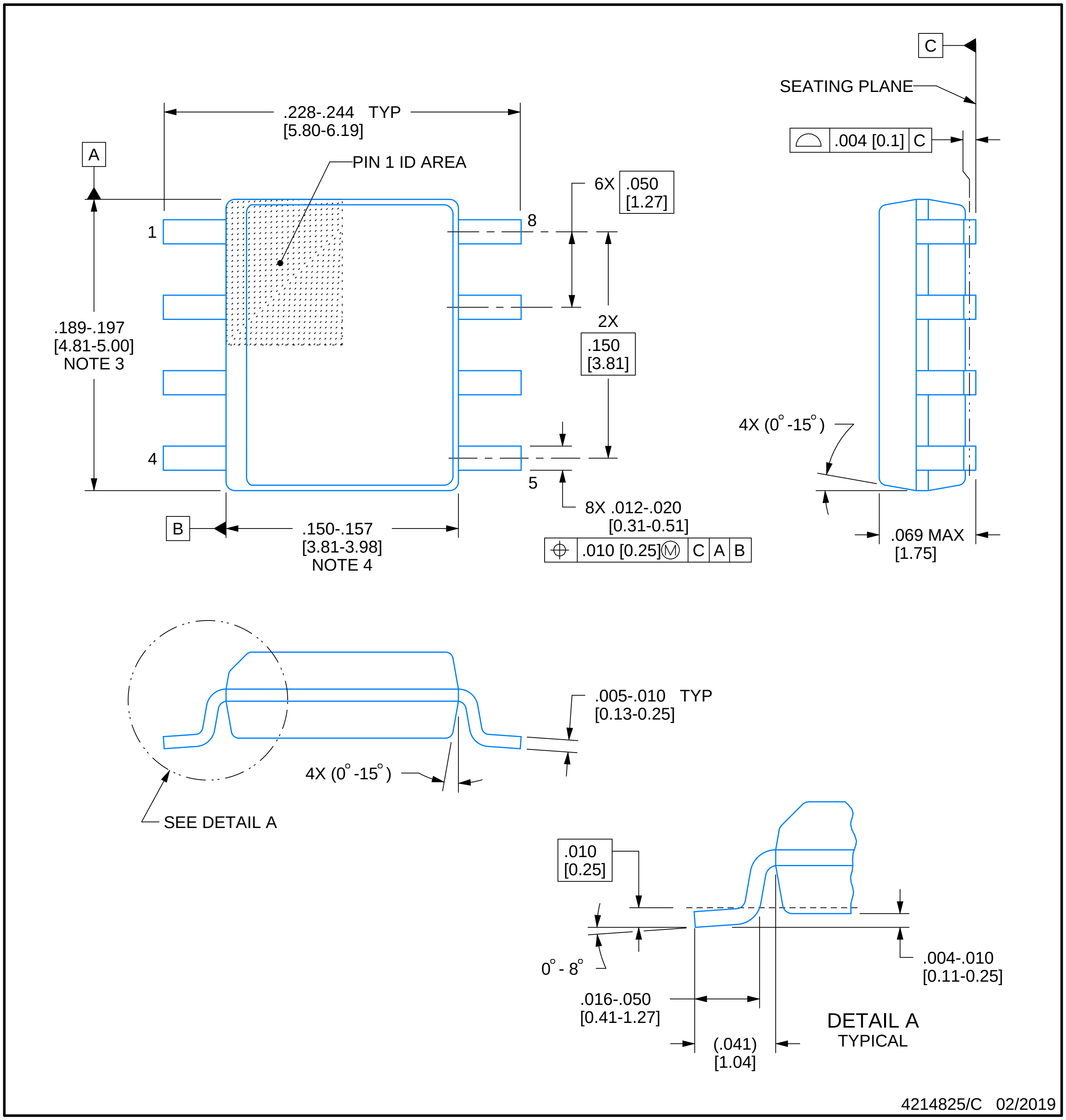
4220610/B 09/2024

NOTES:

1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pin numbers shown for reference only. Numbers may not be marked on package.
4. Reference JEDEC registration MO-002/TO-99.



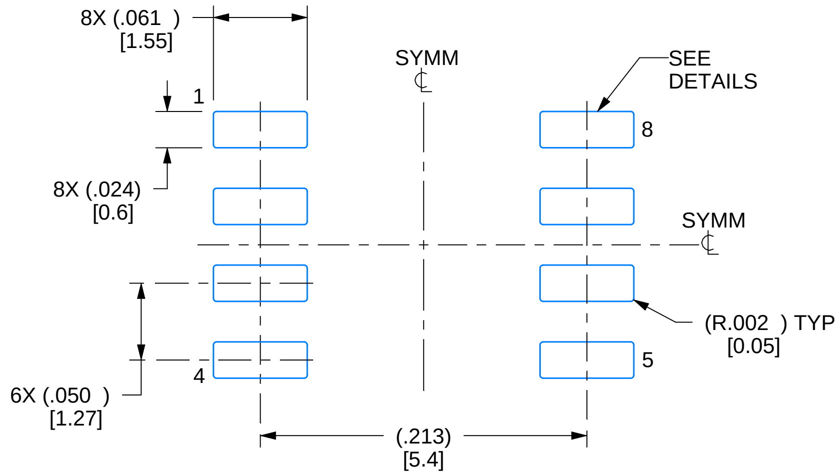
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X



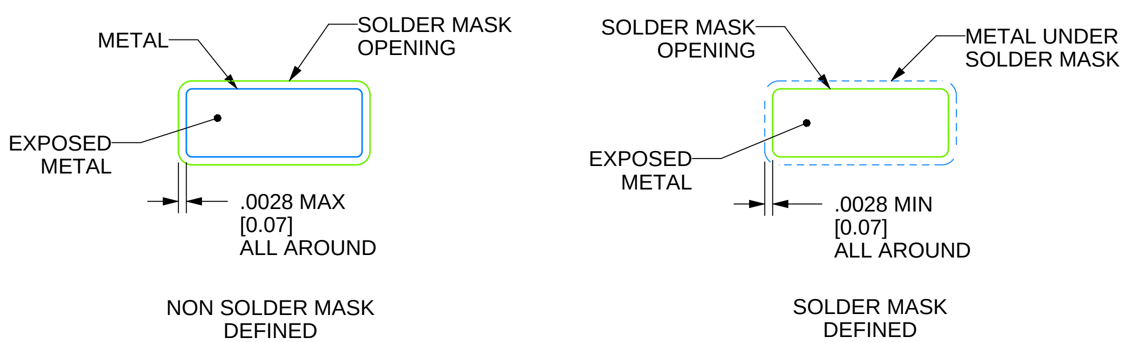
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

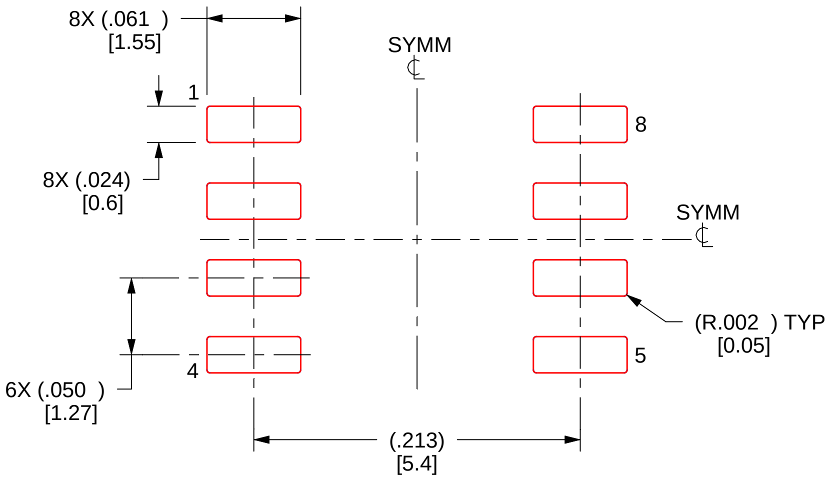


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



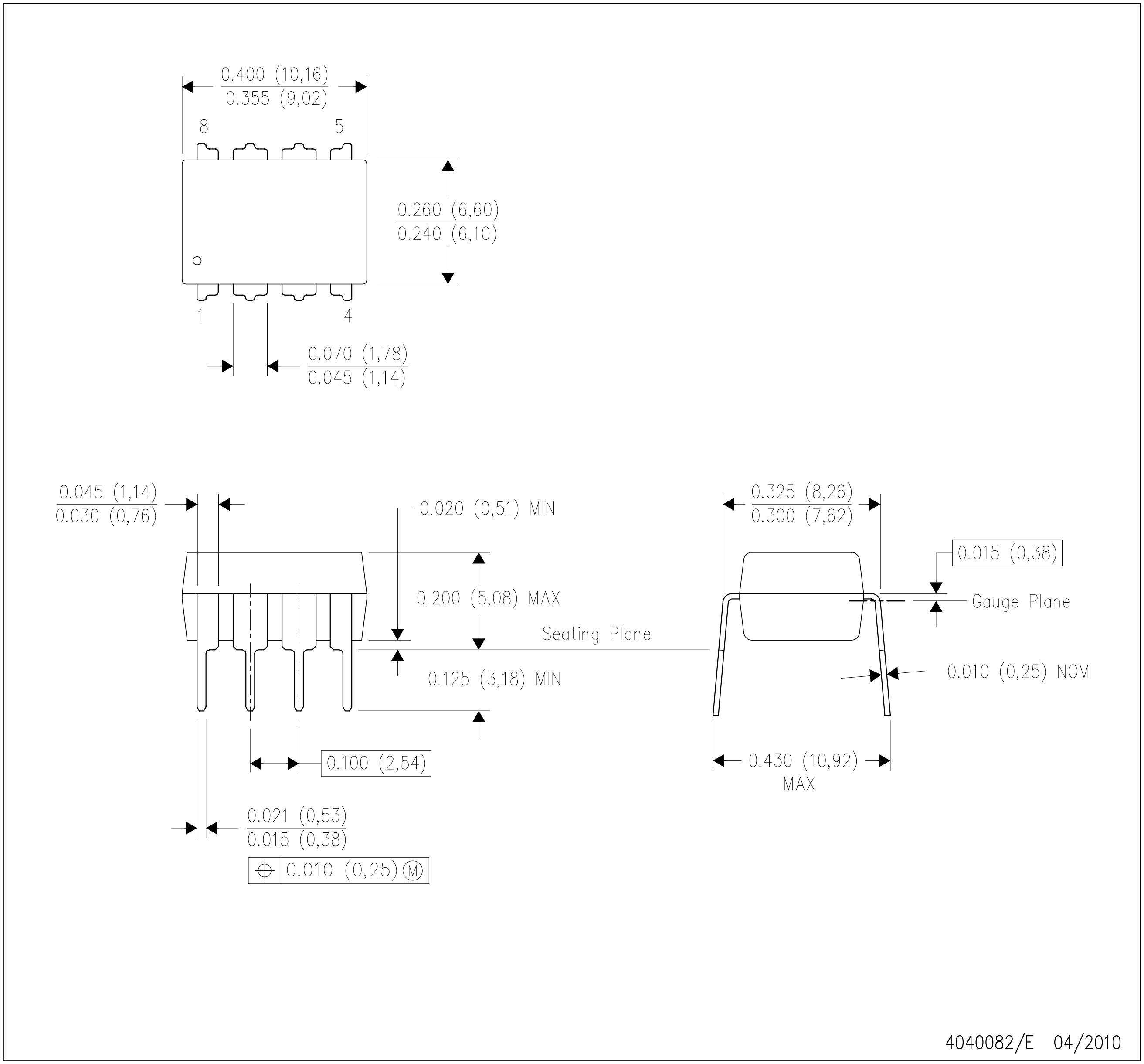
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.