LM118, LM218, LM318 FAST GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

The LM118 and LM218 are obsolete and are no longer supplied.

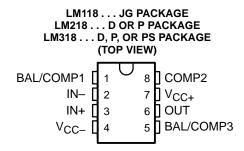
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- Small Signal Bandwidth . . . 15 MHz Typ
- Slew Rate . . . 50 V/μs Min
- Bias Current . . . 250 nA Max (LM118, LM218)
- Supply Voltage Range . . . ±5 V to ±20 V
- Internal Frequency Compensation
- Input and Output Overload Protection
- Same Pin Assignments as General-Purpose Operational Amplifiers

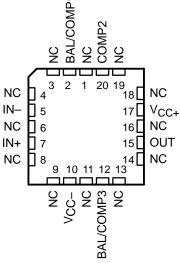
description/ordering information

The LM118, LM218, and LM318 are precision, fast operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor-of-ten increase in speed over general-purpose devices without sacrificing dc performance.

These operational amplifiers have internal unity-gain frequency compensation. considerably simplifies their application because no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feed-forward compensation boosts the slew rate to over 150 V/µs and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the settling time for 0.1% error band to under 1 μs.



LM118 ... FK PACKAGE (TOP VIEW)



NC - No internal connection

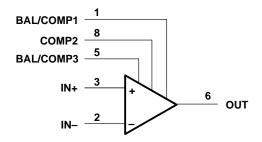
The high speed and fast settling time of these operational amplifiers make them useful in A/D converters, oscillators, active filters, sample-and-hold circuits, and general-purpose amplifiers.

ORDERING INFORMATION

TA	V _{IO} max AT 25°C	PACK	AGET	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	0°C to 70°C 10 mV	PDIP (P)	Tube of 50	LM318P	LM318P
000 45 7000		0010 (D)	Tube of 75	LM318D	1.0404.0
0°C to 70°C		SOIC (D)	Reel of 2500	LM318DR	LM318
		SOP (PS)	Reel of 2000	LM318PSR	LM18

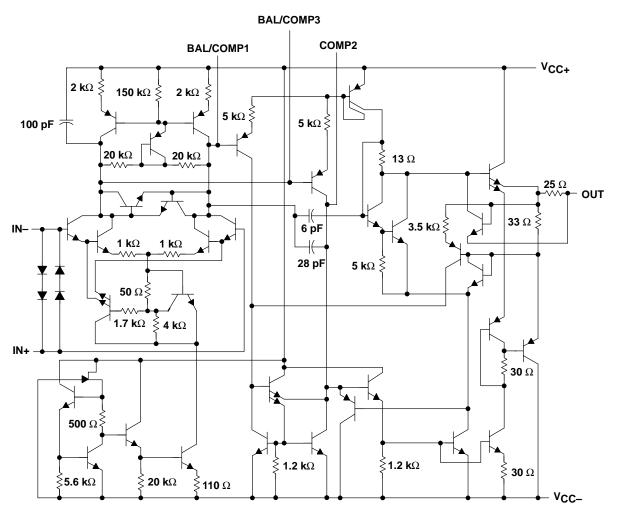
[†] Package drawings, standard packing quantities, thermal data, symboliztion, and PCB design guidelines are available at www.ti.com/sc/package.

symbol



Pin numbers shown are for the D, JG, P, and PS packages.

schematic



Component values shown are nominal.



LM118, LM218, LM318 FAST GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

The LM118 and LM218 are obsolete and are no longer supplied.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage: V _{CC+} (see Note 1)	20 V
V _{CC} – (see Note 1)	–20 V
Input voltage, V _I (either input, see Notes 1 and 2)	±15 V
Differential input current, V _{ID} (see Note 3)	±10 V
Duration of output short circuit (see Note 4)	Unlimited
Operating virtual junction temperature, T _J	
Package thermal impedance, θ _{JA} (see Notes 5 and 6): D package	
P package	
PS package	95°C/W
Package thermal impedance, θ _{JC} (see Notes 7 and 8): FK package	5.61°C/W
JG package	14.5°C/W
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: JG package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: D, P, PS, or PW package	260°C
Storage temperature range, T _{stq}	. −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}
 - 2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
 - 3. The inputs are shunted with two opposite-facing base-emitter diodes for overvoltage protection. Therefore, excessive current flows if a different input voltage in excess of approximately 1 V is applied between the inputs unless some limiting resistance is used.
 - 4. The output can be shorted to ground or either power supply. For the LM118 and LM218 only, the unlimited duration of the short circuit applies at (or below) 85°C case temperature or 75°C free-air temperature.
 - 5. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperautre is P_D = (T_J(max) T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
 - 6. The package thermal impedance is calculated in accordance with JESD 51-7.
 - 7. Maximum power dissipation is a function of $T_J(max)$, θ_{JC} , and T_C . The maximum allowable power dissipation at any allowable ambient temperautre is $P_D = (T_J(max) T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 - 8. The package thermal impedance is calculated in accordance with MIL-STD-883.



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electrical characteristics at specified free-air temperature (see Note 5)

PARAMETER		TEST	- +	LM1	18, LM2	18			LINUT	
		CONDITIONS†	T _A ‡	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
V	land offertualte as	V 0	25°C		2	4		4	10	>/
VIO	Input offset voltage	VO = 0	Full range			6			15	mV
	hand affect account	V 0	25°C		6	50		30	200	- ^
IIO	Input offset current	VO = 0	Full range			100			300	nA
	Land his a summer	V 0	25°C		120	250		150	500	- ^
IВ	Input bias current	V _O = 0	Full range			500			750	nA
VICR	Common-mode input voltage range	$V_{CC\pm} = \pm 15 \text{ V}$	Full range	±11.5			±11.5			V
V _{OM}	Maximum peak output voltage swing	$V_{CC\pm} = \pm 15 \text{ V},$ $R_L = 2 \text{ k}\Omega$	Full range	±12	±13		±12	±13		V
	Large-signal differential	$V_{CC\pm} = \pm 15 \text{ V},$	25°C	50	200		25	200		
AVD	voltage amplification	$V_O = \pm 10 \text{ V},$ $R_L \ge 2 \text{ k}\Omega$	Full range	25			20			V/mV
B ₁	Unity-gain bandwidth	$V_{CC\pm} = \pm 15 \text{ V}$	25°C		15			15		MHz
rį	Input resistance		25°C	1*	3		0.5	3		$M\Omega$
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICR} min	Full range	80	100		70	100		dB
ksvr	Supply-voltage rejection ratio (ΔV _{CC} /ΔV _{IO})		Full range	70	80		65	80		dB
ICC	Supply current	$V_O = 0$, No load	25°C		5	8		5	10	mA

^{*} On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS				TYP	MAX	UNIT
SR	Slew rate at unity gain	$\Delta V_{I} = 10 V$,	C _L = 100 pF,	See Figure 1	50*	70		V/μs

^{*} On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

PARAMETER MEASUREMENT INFORMATION

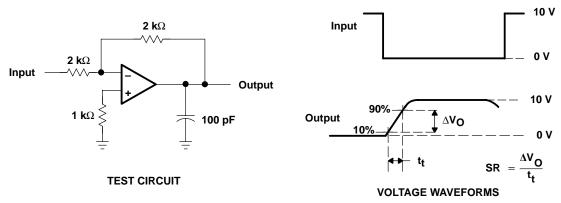


Figure 1. Slew Rate



[†] All characteristics are measured under open-loop conditions with common-mode input voltage, unless otherwise specified.

[‡] Full range for LM118 is -55°C to 125°C, full range for LM218 is -25°C to 85°C, and full range for LM318 is 0°C to 70°C.

NOTE 9: Unless otherwise noted, $V_{CC} = \pm 5 \text{ V}$ to $\pm 20 \text{ V}$. All typical values are at $V_{CC\pm} = \pm 15 \text{ V}$ and $T_A = 25^{\circ}\text{C}$.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
LM318D	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM318
LM318D.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM318
LM318DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM318
LM318DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM318
LM318P	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LM318P
LM318P.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	LM318P
LM318PE4	Active	Production	PDIP (P) 8	50 TUBE	-	Call TI	Call TI	0 to 70	
LM318PSR	Active	Production	SO (PS) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	L318
LM318PSR.A	Active	Production	SO (PS) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	L318

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM318DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM318PSR	so	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM318DR	SOIC	D	8	2500	353.0	353.0	32.0
LM318PSR	SO	PS	8	2000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM318D	D	SOIC	8	75	507	8	3940	4.32
LM318D.A	D	SOIC	8	75	507	8	3940	4.32
LM318P	Р	PDIP	8	50	506	13.97	11230	4.32
LM318P.A	Р	PDIP	8	50	506	13.97	11230	4.32



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.



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