LM251772-Q1 36V V_{IN}4 Switch Buck-Boost Controller With I2C for

1 Features

- Input range from 3.5V to 36V
- Dynamical V_o programming using I^2C from:
  - 3.3V up to in 20mV monotonous steps
  - 1V up to 23V in 10mV monotonous steps
- Peak current regulation control
- Small voltage transition ripple overall operating modes
- Dynamic output voltage tracking (digital PWM tracking input, analog tracking input)
  - Via I^2C interface programming
- Shut down quiescent current 3µA
- Operating quiescent current 60µA
- Drive (DRV) pin for dual role port power path
  - Push-Pull output for fast pMOS FET control
  - Configurable as charge pump driver stage for nMOS FET
- Operation mode selection for high efficiency in light load and high load conditions:
  - Power save mode (Single Pulse/µSleep)
  - Automatic conduction mode
- Integrated high voltage supply LDO
- Auxiliary high voltage LDO for microcontroller supply
- Integrated full-bridge gate drive
  - 2A peak current capability
  - Bootstrap over and under-voltage protection
  - Integrated boot-strap diode
- Fixed frequency independent from operating mode (boost, buck-boost, buck)
  - Forced PWM mode selectable
  - Switching frequency from 100kHz to 2200kHz
  - External clock synchronization and clock output
- Spread spectrum operation selectable
- Average input or output current sensor
  - Programmable from 0.5A to 7A in 50mA steps
- I^2C programmable with diagnostics
- Automotive temperature range (Tj = -40°C to 150°C)
- 40-Pin WSON package with wettable flanks
- Functional Safety-Capable
  - Documentation available to aid functional safety
- Create a custom design using the LM251772-Q1 with the WEBENCH® Power Designer

2 Applications

- Automotive infotainment, digital cockpit
- USB-PD EPR (extended power range)

3 Description

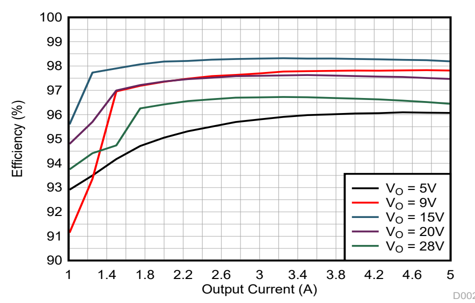
The LM251772-Q1 is a four switch Buck-Boost controller. The device provides a regulated output voltage if the input voltage is higher, equal or lower than the adjusted output voltage. In power save mode the device supports very high efficiency over the complete operation range of the output. The output voltage and average current is dynamically programmable using the integrated I^2C interface. The configuration range for output voltage and average current meets the USB-PD standard requirements. The integrated DRV pin is used to control an optional disconnect FET if the system is targeted to support dual role port (DRP) requirements.

LM251772-Q1 runs at a fixed switching frequency, which is set using the RT/SYNC pin. The switching frequency remains the same during buck, boost and buck-boost operation. The device maintains small mode transition ripple over all operating modes.

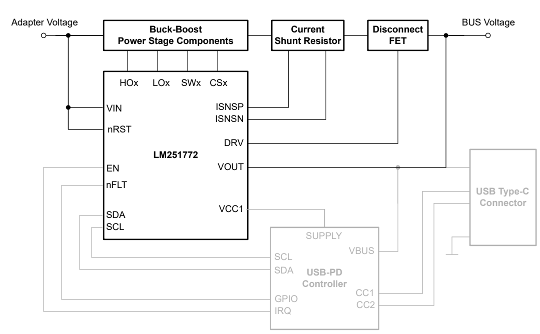
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LM251772-Q1RHAR	RHA (VQFN, 40)	6mm × 6mm

(1) For more information, see Section 13.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Efficiency vs. Output Current, V_I = 12V, PSM



Typical Application Schematic

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4 Device Comparison

Table 4-1. Device Comparison

FUNCTION	LM251772Q1	LM51772Q1	LM251772	LM51770Q1	LM34938Q1
Maximum Recommended Input Voltage	36V	55V	36V	78V	36V
Absolute Maximum Input Voltage	48V	59V	48V	85V	48V
Maximum Recommended Switching Frequency	2.2MHz	2.2MHz	600kHz	2MHz	2.2MHz
Default Output Voltage Value	5.1V	12V	5.1V	n/a	5V
Default Output Current Limit Value	900mA	5A	900mA	n/a	Analog Setting only
Output Start-up State Without Programming	Disabled	Enabled	Disabled	Enabled	Disabled
I^2C interface	yes	yes	yes	no	yes
PSM - Automatic Conduction Mode	yes	yes	yes	yes	yes
PSM - Programmable Conduction Mode	no	yes	no	no	no
Output Discharge	yes	yes	yes	no	yes
Input voltage regulation	yes	yes	yes	with external circuit	yes
Analog Current Limit Setting	no	yes	no	no	yes
T_j Temperature Range	-40°C to 150°C	-40°C to 150°C	0°C to 70C	-40°C to 150°C	-40°C to 150°C

5 Pin Configuration and Functions

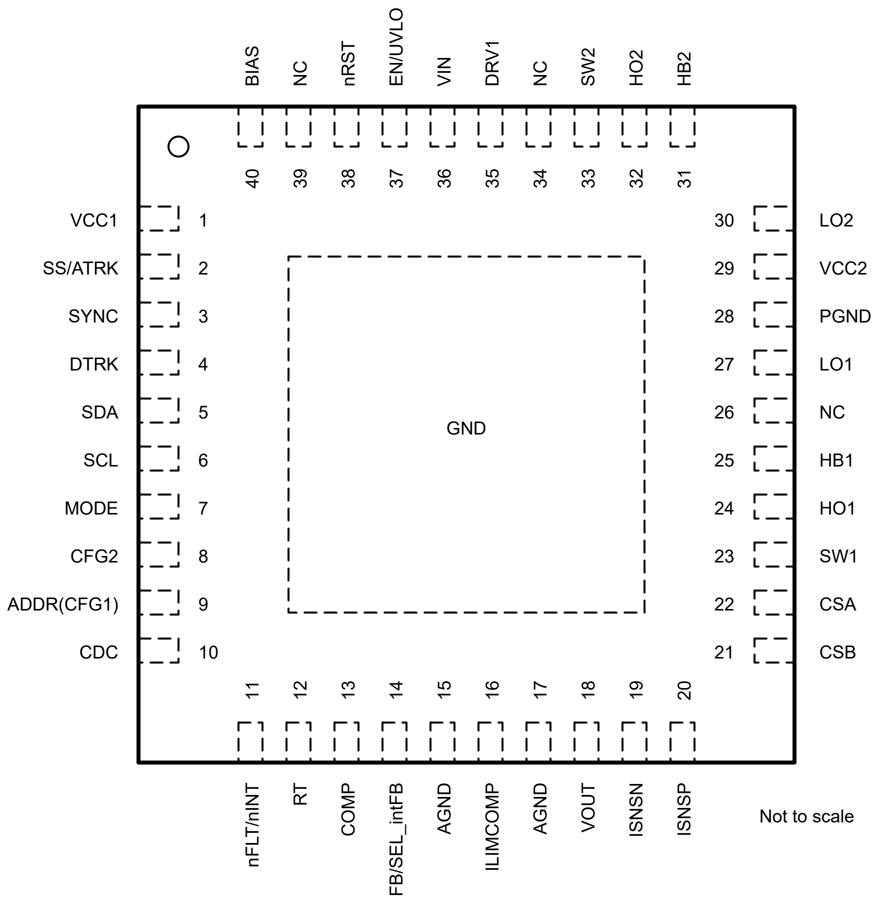

Figure 5-1. LM251772-Q1 RHA Package, 40-Pin QFN (Top View)

Table 5-1. Pin Functions LM251772Q1

PIN		Type[1]	DESCRIPTION
NAME	NO.		
VCC1	1	O	Auxiliary 5V regulator output. Place a capacitor close to the pin for good decoupling. If the output is disabled by the according logic selection tie the pin to GND with a resistor or pulled to VCC2. Do not leave the pin floating.
SS/ATRK	2	I/O	Soft-start programming pin. A capacitor between the SS pin and AGND pin programs soft-start time. Analog output voltage tracking pin. The pin programs the VOUT regulation target by connecting the pin to variable voltage reference (for example, through a digital to analog converter) if needed. The internal circuit selects the lowest voltage between the pin voltage and the internal voltage reference.
SYNC	3	I	Synchronization clock input/output. The internal oscillator synchronizes to an external clock during operation if a valid clock input signal is present. *Do not leave this pin floating*. If this function is not used, connect the pin to VCC2 or GND. The SYNC pin also features a clock synchronization output signal which is configured through the device logic. The clock phase has a option to be selected to 0° and 180° to directly operate two devices in a parallel (dual phase) operation.
DTRK	4	I	Digital PWM input pin for the dynamic output voltage tracking. *Do not leave this pin floating.* If this function is not used, connect the pin to VCC or GND.
SDA	5	I/O	I^2C interface serial data line. Connect an external a pull-up resistor
SCL	6	I	I^2C interface serial clock line. Connect an external a pull-up resistor
MODE	7	I	Digital input to select device operation mode. If the pin is pulled low, power save mode (PSM) is enabled. If the pin is pulled high, the forced PWM or CCM operation is enabled. It is possible to change the operation mode dynamically during operation. *Do not leave this pin floating*.
CFG2	8	I/O	Device configuration pin. Connect a resistor between the CFG2 pin and GND to select the device operation according the Section 8.3.21
ADDR(CFG1)	9	I	Address selection. Pull to GND for I^2C target address LSB = 0. Pull to VCC2 for I^2C target address LSB = 1
CDC	10		Cable drop compensation or current monitor output pin. Connect a resistor between the CDC pin and AGND to select the gain for the cable drop compensation. Per default this pin provides a current monitoring signal of the sensed voltage between the ISNSP and ISNSN pins In case the current monitor is disabled connect CDC to ground
nFLT/nINT	11	O	Open-drain output pin for fault indication or power good. This pin has a further function if the pin is configured as an interrupt pin. In case of a STATUS register change the pin toggles low for 256µs.
RT	12	I/O	Switching frequency programming pin. An external resistor is connected to the RT pin and AGND to set the switching frequency
COMP	13	O	Output of the error amplifier. An external RC network needs to be connected between COMP and AGND to stabilize/compensate the regulator voltage loop.
FB/SEL_intFB	14	I	Feedback pin for output voltage regulation. Connect a resistor divider network from the output of the converter to the FB pin. Connect the FB pin to VCC2 to operate at a fixed output voltage default setting of the device. To select the internal feedback connect the pin to VCC2 before the device start-up
AGND	15		Connect to AGND
ILIMCOMP	16		Compensation pin for average current limit loop. Connect an capacitor or a type 2R-C network if the current limit is set by the internal DAC. If the internal DAC is disabled the pin sets the current limit threshold for the average current limit. Connect a resistor to AGND. A parallel filter of capacitor is recommended depending on the application requirements Connect the ILIMCOMP pin to VCC2 to disable the block and reduce the quiescent current
AGND	17	G	Analog Ground
VOUT	18	I	Output voltage sense input. Connect to the power stage output rail.

Table 5-1. Pin Functions LM251772Q1 (continued)

PIN		Type[(1)]	DESCRIPTION
NAME	NO.		
ISNSN	19	I	Negative sense input of the output or input average current sense amplifier. An optional current sense resistor connected between ISNSN and ISNSP is required if the internal average current sensor is used. It is possible to place the sense resistor n the input side or on the output side of the power stage. In case the optional current sensor is disabled connect ISNSN and ISNSP together to AGND
ISNSP	20	I	Positive sense input of the output or input current sense amplifier. An optional current sense resistor connected between ISNSN and ISNSP is required if the internal average current sensor is used. It is possible to place the sense resistor n the input side or on the output side of the power stage. In case the optional current sensor is disabled connect ISNSP to ground
CSB	21	I	Inductor peak current sense negative input. Connect CSB to the negative side of the external current sense resistor using a Kelvin connection.
CSA	22	I	Inductor peak current sense positive input. Connect CSA to the positive side of the external current sense resistor using a Kelvin connection.
SW1	23	P	Inductor switch node for the buck half-bridge
HO1	24	O	High-side gate driver output for the buck half-bridge
HB1	25	P	Bootstrap supply pin for buck half-bridge. An external capacitor is required between the HB1 pin and the SW1 pin, to provide bias to the high-side MOSFET gate driver. Place the external capacitor close to the pin without any resistance between the pin and capacitor for good decoupling
NC	26	O	Not Connected
LO1	27	O	Low-side gate driver output for the buck half-bridge
PGND	28	G	Power Ground
VCC2	29	O	Internal linear bias regulator output. Connect a ceramic decoupling capacitor from VCC to PGND. This rail supplies the internal logic and the gate driver. Place the external capacitor close to the pin without any resistance between the pin and capacitor for good decoupling.
LO2	30	O	Low-side gate driver output for the boost half-bridge
HB2	31	P	Bootstrap supply pin for boost half-bridge. An external capacitor is required between the HB2 pin and the SW2 pin, to provide bias to the high-side MOSFET gate driver Place the external capacitor close to the pin without any resistance between the pin and capacitor for good decoupling
HO2	32	O	High-side gate driver output for the boost half-bridge
SW2	33	P	Inductor switch node for the boost half-bridge
NC	34	O	Not Connected
DRV1	35		External FET drive pin. This pin features a high-voltage push pull stage, a open drain output or a charge pump driver stage according to the selected configuration. In case the optional DRV pin is unused, leave DRV open.
VIN	36	I	The input supply and sense input of the device. Connect VIN to the supply voltage of the power stage.
EN/UVLO	37	I	Enable pin. Digital input pin to enable the converter switching. The input features a precise analog comparator and a hysteresis to monitor the input voltage. Connect a resistor divider from the input voltage to maintain the under voltage lookout(UVLO) feature.
nRST	38	I	Digital input pin to enable the device internal logic, interface operation and the VCC1 regulator if selected.
NC	39	O	Not Connected
BIAS	40		Optional input to the VCC2 bias regulator. Powering VCC2 from an external supply instead of VIN this helps to reduce power loss at high V_{IN} for the internal LDO.

Table 5-1. Pin Functions LM251772Q1 (continued)

PIN		Type[1]	DESCRIPTION
NAME	NO.		
GND	PAD	G	Thermal pad

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise specified)[1]

		MIN	MAX	UNIT
Input	BIAS to AGND	–0.3	48	V
Input	VIN, ISNSP, ISNSN to AGND	–0.3	48	V
Input	EN/UVLO, nRST	–0.3	48	V
		–0.3	$V_{(VIN)}$+5 [4]	
Input	SS/ATRK, DTRK, RT, SYNC, MODE, SDA, SCL, ADDR, CFG2, to AGND [3]	–0.3	5.8	V
Input	FB	–0.3	5.8	V
Input	ISNSP to ISNSN	-0.3	0.3	V
Input	CSA, CSB to SW1	–0.3	0.3	V
Input	SW1 to AGND(DC)	–0.5	48	V
Input	SW2 to AGND(DC)	–0.5	59	V
Input	SW1 to AGND (≤ 100ns duration)	–2	48	V
Input	SW2 to AGND (≤ 100ns duration)	–2	59	V
Input	SW1 to AGND(≤ 10ns duration)	–3	48	V
Input	SW2 to AGND(≤ 10ns duration)	–3	59	V
Input	SW1 to AGND(≤ 5ns duration)	–4	48	V
Input	SW2 to AGND(≤ 5ns duration)	–4	59	V
Input	PGND to AGND	–0.3	0.3	V
Output	VCC1, VCC2 to AGND	–0.3	5.5	V
Output	VOUT, DRV1 to AGND	–0.3	59	V
Output	nFLT to AGND	–0.3	5.8	V
Output	COMP, ILIMCOMP, CDC to AGND[2]	–0.3	5.8	V
Output	LO1, LO2, to PGND	–0.3	$V_{(VCC2)}$+0.3	V
Output	HB1 to SW1, HB2 to SW2	–0.3	5.5 [5]	V
Output		–0.3	6	V
Output	HO1 to SW1	–0.3	$V_{(HB1)}$+0.3	V
Output	HO2 to SW2	–0.3	$V_{(HB2)}$+0.3	V
Output	HO1, HO2, HB1, HB2 to AGND	–0.3	65	V
Storage temperature, T_{STG}		–55	150	°C
Operating junction temperature, T_J [3]		–40	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) This pin has an internal max. voltage clamp which supports typ. 1.6mA of current
(3) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.
(4) Both of the stated conditions need to be observed
(5) Operating lifetime is de-rated for voltage bigger than the specified maximum

6.2 Handling Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range (unless otherwise specified)[1]

		MIN	NOM	MAX	UNIT
$V_{(VIN)}$	Input Voltage Sense	3.5	20	36	V
$V_{(BIAS)}$	Bias Input Voltage Supply	0		36	V
	Input/Bias start-up voltage	3.5			V
$V_{(VOUT)}$	Output Voltage Sense	1	53.5	55 [3]	V
$V_{(DRV1)}$	High voltage drive pin output	0		55	V
	ISNSP;ISNSN	2.8		55	V
R(SNS)	current limit sense resistor		10		mΩ
	current limit sense resistor tolerance	–1		1	%
$C_{(VCC1)}$	VCC1 regulator output capacitance	2			µF
$C_{(VCC2)}$	VCC2 regulator output capacitance	6			µF
V_{FB}	FB Input	0		$V_{(VCC2)}$	V
V_{IL}	Logic pin low-level (MODE, DTRK, SYNC, SDA, SCL)			0.4	V
V_{IH}	Logic pin high-level (MODE, DTRK, SYNC, SDA, SCL)	1.3			V
F_{SW}	Typical Switching Frequency	100		2200	kHz
F_{SYNC}	Synchronization switching Frequency range	100		2200	kHz
T_J	Operating Junction Temperature[2]	–40		150	°C

(1) Operating Ratings are conditions under the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.
(2) High junction temperatures degrade operating lifetimes.
(3) Nominal value determined by minimum OVP threshold.

6.4 Thermal Information

THERMAL METRIC[1]		LM251772-Q1 QFN 40 PINS	UNIT
R_{qJA}	Junction-to-ambient thermal resistance	33.9	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	26.6	°C/W
R_{qJB}	Junction-to-board thermal resistance	15.4	°C/W
Y_{JT}	Junction-to-top characterization parameter	0.4	°C/W
Y_{JB}	Junction-to-board characterization parameter	15.4	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	4.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Electrical Characteristics

Typical values correspond to T_J=25°C. Minimum and maximum limits apply over T_J=-40°C to 150°C. Unless otherwise stated, $V_{(BIAS)}$ =12 V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
	Shutdown current into VIN	$V_{(VIN)}$ = 48V, $V_{(BIAS)}$ = 0V $V_{(EN)}$ = 0V	T_J = 25°C		1.1	1.5	µA
			T_J = –40°C to 125°C		1.1	2	µA
	Shutdown current into BIAS	$V_{(VIN)}$ = 0V, $V_{(EN)}$ = 0V	T_J = 25°C		1.3	1.7	µA
			T_J = –40°C to 125°C		1.3	2.2	µA
	Stand-by current into VIN	$V_{(VIN)}$ = 12V, $V_{(BIAS)}$ = 0V; $V_{(nRST)}$ = High	T_J = 25°C		55	75	µA
			T_J = –40°C to 125°C		55	100	µA
	Quiescent current into BIAS	$V_{(EN)}$ = 3.3 V, $V_{(FB)}$ > 1V, uSleep enabled, ILIMCOMP = $V_{(VCC2)}$, EN_VCC1 = 0b0	T_J = 25°C		65	75	µA
			T_J = –40°C to 125°C		65	100	µA
VCC1 REGULATOR							
	VCC1 regulation	V_I = 12.0V ,$I_{(VCC1)}$ = 1mA		4.95	5	5.05	V
	VCC1 drop-out voltage	$I_{(VCC1)}$ = 34mA	V_I = 5V		0.6	1.4	V
			V_I = 4.5V		0.6	1.5	V
	VCC1 sourcing current limit	VCC1=GND	V_I = 12V	34		70	mA
VCC2 REGULATOR							
	VCC2 regulation	V_{BIAS} =12.0V ,$I_{(VCC2)}$ = 20mA		4.85	5	5.1	V
	VCC2 drop-out voltage	$I_{(VCC2)}$ = 45mA	V_I = 4V		130	300	mV
			V_I = 3.5V		190	400	mV
	VCC2 sourcing current limit	$V_{(VCC2)}$ ≥ 3V	V_I = 6V, V_{BIAS} = 12V	200	260	450	mA
$V_{T+(VCC2)}$	Positive going threshold	$V_{(VCC2)}$ rising		3.3	3.35	3.4	V
$V_{T-(VCC2)}$	Negative going threshold	$V_{(VCC2)}$ falling		3	3.05	3.1	V
$V_{T+(Force,BIAS)}$	Positive going threshold for Forced $V_{(BIAS)}$	FORCE_BIASPIN = 0b1		4.5	4.6	4.7	V
$V_{hyst(Force,BIAS)}$	LDO switch-over hysteresis for Forced V(BIAS)			230	275		mV
$V_{T+(VCC2,SUP)}$	Positive going threshold for LDO switch-over	FORCE_BIASPIN = 0b0		6.7	6.8	6.9	V
$V_{hyst(VCC2,SUP)}$	LDO switch-over hysteresis			350	400		mV
	VCC2 UVLO rising detection delay time	$V_{(VCC2)}$ rising			100		µs
nRST							
$V_{T+(nRST)}$	Enable positive-going threshold	nRST rising				1.4	V
$V_{T-(nRST)}$	Enable negative-going threshold	nRST falling		0.35			V
Vhyst(nRST)	Enable threshold hysteresis				300		mV
EN/UVLO							
	VDET positive-going threshold	$V_{(VIN)}$ rising, VDET_RISE = 0x3		3.3	3.4	3.5	V
	VDET negative-going threshold	$V_{(VIN)}$ falling, VDET_FALL = 0x0		2.6	2.7	2.799	V
$V_{T+(UVLO)}$	UVLO positive-going threshold	$V_{(EN/UVLO)}$ rising		1.23	1.25	1.27	V
$V_{T-(UVLO)}$	UVLO negative-going threshold	$V_{(EN/UVLO)}$ falling		1.18	1.2	1.22	V
$V_{hyst(UVLO)}$	UVLO threshold hysteresis			38	50	62	mV
I_{UVLO}	UVLO hysteresis sinking current	$V_{(EN/UVLO)}$ < 1.26V		4	5	6	µA
$t_{d(UVLO)}$	UVLO detection delay time	$V_{(EN/UVLO)}$ falling;		25.5	30	38.5	µs

6.5 Electrical Characteristics (continued)

Typical values correspond to T_J=25°C. Minimum and maximum limits apply over T_J=-40°C to 150°C. Unless otherwise stated, $V_{(BIAS)}$ =12 V

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{T+(POR)}$	POR positive-going threshold	POR positive-going threshold	VIN rising or BIAS rising			1.75		V
$V_{T-(POR)}$	POR negative-going threshold	POR negative-going threshold	VIN falling or BIAS falling			1.7		V
SYNC								
$V_{T+(SYNC)}$	Sync input positive going threshold						1.19	V
$V_{T-(SYNC)}$	Sync input negative going threshold				0.41			V
	Sync activity detection frequency				99			kHz
$t_{d(Det,Sync)}$	Sync activity detection frequency threshold		referred to $f_{(SYNC)}$				3	cycles
	Sync PLL lock time		referred to $f_{(SYNC)}$	until $f_{(SYNC)}$ - 5% < $f_{(sw)}$ < $f_{(SYNC)}$ + 5%		10		cycles
	SYNC high level output voltage drop		EN_SYNC_OUT = 0b1	Referenced to $V_{(VCC2)}$			0.4	V
	SYNC low level output voltage		$I_{(SYNC)}$ = 2mA, $V_{(VCC2)}$ ≥ 3.5V,				0.3	V
	SYNC output drive strength		EN_SYNC_OUT = 0b1 $V_{(VCC2)}$ = 5V	sink	–42	–31	–22	mA
				source	22	34	42	mA
SOFT-START								
$I_{(SS)}$	Soft-start current				9	10	11	uA
	SS pull-down switch $R_{DS(on)}$		$V_{(SS)}$ = 1V			21	40	Ω
$t_{d(DISCH;SS)}$	SS Pin discharge time		Time from internal SS discharge until the soft-start current is allowed to charge the capacitor on the pin again		500			µs
$t_{d(EN\_SS)}$	SS Pin ramp start delay time		Internal delay until soft-start current starts		2.5		4	µs
$V_{(SS,clamp)}$	Clamp Voltage for SS pin					4.1		V
VOUT TRACKING								
$V_{T+(DTRK)}$	DTRK positive-going threshold		$V_{(DTRK)}$ rising				1.19	V
$V_{T-(DTRK)}$	DTRK negative-going threshold		$V_{(DTRK)}$ falling		0.41			V
	DTRK activity detection frequency	DTRK activity detection frequency			148			kHz
$t_{d(DTRK)}$	DTRK detection delay time						3	cycles
fc(LPF)	Corner frequency of internal low pass					40		kHz
	$V_{(REF)}$ voltage offset error	$V_{(REF)}$voltage offset error	$f_{(DTRK)}$ = 500kHz, duty = 50%, $V_{(REF)}$ = 1V				±10	mV
PULSE WIDTH MODULATION								
	Switching frequency		R_{RT} = 14.20kΩ,		2000	2200	2400	kHz
	Switching frequency		R_{RT} = 15.63kΩ,		1845	2000	2255	kHz

6.5 Electrical Characteristics (continued)

Typical values correspond to T_J=25°C. Minimum and maximum limits apply over T_J=-40°C to 150°C. Unless otherwise stated, $V_{(BIAS)}$ =12 V

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Switching frequency		R_{RT} = 316kΩ,		90	100	110	kHz
	Minimum controllable on-time		fPWM, R_{RT} = 14 kΩ, positive inductor current	Boost Mode		64		ns
				Buck Mode		107		ns
	Minimum controllable off-time			Boost Mode		96		ns
				Buck Mode		97		ns
	RT regulation voltage					0.75		V
MODE SELECTION								
$V_{T+(MODE)}$	Mode input positive going threshold						1.19	V
$V_{T-(MODE)}$	Mode input negative going threshold				0.41			V
CURRENT SENSE								
$V_{th+(CSB-CSA)}$	Positive peak current limit threshold				45	50	55	mV
Vth-(CSB-CSA)	Negative peak current limit threshold		T_J=-40°C to 125°C		–56	–50	–44	mV
AVERAGE CURRENT LIMIT								
$gm_{(ISET)}$	Current sense amplifier transconductance		I2C interface disabled or SEL_ISET_PIN = 0b1; $V_{(ISNSP)}$ > 3.3V; EN_NEG_CL_LIMIT = 0	25 mV ≤ $\Delta V_{(ISNS)}$ ≤ 50 mV	0.9	1	1.1	mS
	Offset voltage		V_{ISNS} > 4.8V	T_J= 25°C	-1.5	0	1.5	mV
			V_{ISNS} > 4.8V	T_J=-40°C to 125°C	-2.5	0	2.5	mV
	Current sense amplifier output current		I2C interface disabled or SEL_ISET_PIN = 0b1; $V_{(ISNSP)}$ > 3.3V; EN_NEG_CL_LIMIT = 0	5 mV	2	5	8	µA
				25 mV	21.5	25	28.5	µA
				50 mV	45	50	55	µA
$gm_{(ILIMCOMP)}$	Current sense amplifier transconductance		I2C interface enabled and SEL_ISET_PIN = 0b0 V_{ISNS} > 4.8V; N_NEG_CL_LIMIT = 0	$\Delta V_{(ISNS)}$ = 30mV and 50mV	450	500	550	µS
	Current limit		$R_{(ISNS)}$ = 10mΩ±1%; ILIM_THRESHOLD = 0x64		4.75	5	5.25	A
$\Delta V_{(ISNSx)}$	Current limit threshold voltage		ILIM_THRESHOLD = 0x14	EN_NEG_CL_LIMIT = 0$_J$=-10°C to 70°C; ISNSP/N ≥ 5V;	8.6	10	11.4	mV
	Current limit threshold voltage		ILIM_THRESHOLD = 0x3C		28.8	30	31.2	mV
	Current limit threshold voltage		ILIM_THRESHOLD = 0x64		48	50	52	mV
$\Delta V_{(ISNSx)}$	Current limit threshold voltage	Current limit threshold voltage	ILIM_THRESHOLD = 0xFF	EN_NEG_CL_LIMIT = 0$_J$=-10°C to 70°C; ISNSP/N ≥ 5V;	67.2	70	72.8	mV
	Typical current limit threshold voltage programming range				5		70	mV
	Current limit threshold voltage step size		from 5mV to 68.5 mV			0.5		mV
	Minimum voltage to disable ILIM		Referred to VCC2		75			%
ERROR AMPLIFIER								
V_{REF}	FB reference Voltage				0.99	1	1.01	V
	FB pin leakage current		$V_{(FB)}$ = 1V			2	60	nA

6.5 Electrical Characteristics (continued)

Typical values correspond to T_J=25°C. Minimum and maximum limits apply over T_J=-40°C to 150°C. Unless otherwise stated, $V_{(BIAS)}$ =12 V

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Output voltage accuracy		$V_{(FB)}$= VCC2; SEL_DIV20=0b1	Vo,nom = 5V	4.75	5	5.25	V
				Vo,nom = 20V	19.6	20	20.4	V
				Vo,nom = 48V	47.04	48	48.96	V
	Transconductance				510	600	690	µS
	COMP sourcing current					95		µA
	COMP sinking current					120		µA
	COMP clamp voltage		$V_{(FB)}$ = 990mV		1.2	1.25	1.3	V
	COMP clamp voltage		$V_{(FB)}$ = 1.01V		0.225	0.25	0.275	V
$V_{T+(SEL,iFB)}$	Minimum voltage to select internal FB operation		$V_{(FB)}$ rising		2.6			V
$t_{d(uSleep)}$	delay time to wake-up from uSleep					7		µs
OVP								
VT+(OVP)	Over-voltage rising threshold		FB rising reference to V_{REF}		107	110	113	%
VT-(OVP)	Over-voltage falling threshold		FB falling reference to V_{REF}		101	105	109	%
VT+(OVP2)	Over-voltage rising threshold		$V_{(VOUT)}$ rising	V_OVP2 = 0b111111	53.5	55	56.5	V
VT+(IVP)	Input Over-voltage rising threshold		$V_{(VIN)}$ rising	IVP_VOLTAGE = 0b00101010	9.9	10	10.1	V
	Over-voltage de-glitch time				9	10	12.5	µs
nFLT								
	nFLT pull-down switch R_{DSON}		1mA sinking			85	140	Ω
$V_{T+(PG)}$	Under-voltage positive going threshold		FB rising (reference to V_{REF})		92	95	97	%
VT-(PG)	Under-voltage negative going threshold		FB falling (reference to V_{REF})		87	90	93	%
	nFLT off-state leakage		$V_{(nFLT)}$=12V				100	nA
$t_{d(nFLT-PIN)}$	Deglitch filter					20	37	µs
MOSFET DRIVER								
t_r	Rise time	LO1, LO2	C_G = 3.3nF			10		ns
t_r	Fall time		C_G = 3.3nF			8		ns
t_f	Rise time	HO1, HO2	C_G = 3.3nF			15		ns
t_f	Fall time		C_G = 3.3nF			15		ns
t_t	Transition (Dead) time		C_G = 3.3nF	$R_{(RT)}$ = 316 kΩ (0.1 MHz), SEL_MIN_DEADTIME_GDRV = 0b01, SEL_SCALE_DT = 0b1, EN_CONST_TDEAD = 0b0		42		ns
t_t	Transition (Dead) time		C_G = 3.3nF	$R_{(RT)}$ = 14.2 kΩ (2.2 MHz), SEL_MIN_DEADTIME_GDRV = 0b01, SEL_SCALE_DT = 0b1, EN_CONST_TDEAD = 0b0		19.5		ns

6.5 Electrical Characteristics (continued)

Typical values correspond to T_J=25°C. Minimum and maximum limits apply over T_J=-40°C to 150°C. Unless otherwise stated, $V_{(BIAS)}$ =12 V

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Gate driver high side on-resistance	LO1, LO2	$I_{(test)}$ = 500mA			1.8		Ω
	Gate driver high side on-resistance	HO1, HO2				1.5		Ω
	Gate driver low side on-resistance	LO1, LO2				0.9		Ω
	Gate driver low side on-resistance	HO1, HO2				0.8		Ω
$V_{TH-(BOOT\_UV)}$	Negative going boot-strap UVLO threshold		V(HBx) - V(SWx) falling		2.5	2.7	3.1	V
$V_{TH-(BOOT\_UV)}$	Boot-strap UVLO hysteresis					300		mV
$V_{TH+(BST\_OV)}$	Positive going boot-strap over-voltage threshold		V(HBx) - V(SWx) rising, I_HBx=10mA		5.1	5.5	5.9	V
$V_{TH(GATEOUT)}$	Gate driver output switching detection	LO1,LO2	referenced to VCC			37		%
$V_{TH(GATEOUT)}$	Gate driver output switching detection	HO2, HO2	referenced to V(HBx) - V(SWx)			37		%
THERMAL SHUTDOWN								
T_{T+J}	Thermal shutdown threshold	Thermal shutdown threshold	T_J rising			164		°C
	Thermal shutdown hysteresis	Thermal shutdown hysteresis				15		°C
THERMAL WARNING								
	Thermal warning threshold		T_J rising	THW_THRESHOLD=0b00		140		°C
	Thermal warning typ. programming range				95		140	°C
	Thermal warning accuracy					±10		°C
R2D INTERFACE								
	Internal reference resistor				31.77	33	34.23	kΩ

6.5 Electrical Characteristics (continued)

Typical values correspond to T_J=25°C. Minimum and maximum limits apply over T_J=-40°C to 150°C. Unless otherwise stated, $V_{(BIAS)}$ =12 V

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
R_{CFG}	External selection resistor resistance	R2D setting #0				0	0.1	kΩ
		R2D setting #1			0.49567	0.511	0.52633	kΩ
		R2D setting #2			1.1155	1.15	1.1845	kΩ
		R2D setting #3			1.8139	1.87	1.9261	kΩ
		R2D setting #4			2.6578	2.74	2.8222	kΩ
		R2D setting #5			3.7151	3.83	3.9449	kΩ
		R2D setting #6			4.9567	5.11	5.2633	kΩ
		R2D setting #7			6.2953	6.49	6.6847	kΩ
		R2D setting #8			8.0025	8.25	8.4975	kΩ
		R2D setting #9			10.185	10.5	10.815	kΩ
		R2D setting #10			12.901	13.3	13.699	kΩ
		R2D setting #11			15.714	16.2	16.686	kΩ
		R2D setting #12			19.885	20.5	21.115	kΩ
		R2D setting #13			24.153	24.9	25.647	kΩ
		R2D setting #14			29.197	30.1	31.003	kΩ
		R2D setting #15			35.405	36.5	37.595	kΩ
Protection/Monitoring								
	SCP Hiccup mode on time				0.85	1	1.15	ms
	SCP Hiccup mode off time				20.4	24	27.6	ms
CABLE DROP COMPENSATION								
	VOUT increase for cable drop compensation with external feedback		$R_{(FB,top)}$ = 100kΩ; CDC_GAIN=0b01	$V_{(CDC)}$ = 0.2V	0.08	0.1	0.12	V
				$V_{(CDC)}$ = 1V	0.45	0.5	0.55	V
	VOUT increase for cable drop compensation with internal feedback		CDC_GAIN=0b01	$V_{(CDC)}$ = 0.2V	0.075	0.1	0.125	V
				$V_{(CDC)}$ = 1V	0.45	0.5	0.55	V
$gm_{(CDC)}$	CDC current sense amplifier transconductance		$\Delta V_{(IMON)}$ = 50mV and 30mV	$V_{(ISNSP)}$ > 3.3V; EN_NEG_CL_LIMIT = 0	450	500	550	µS
	CDC current sense amplifier bandwidth					1		MHz
	Output current CDC		$\Delta V_{(IMON)}$ = 50mV; EN_NEG_CL_LIMIT = 0		23.3	25.0	26.8	µA
			$\Delta V_{(IMON)}$ = 25mV; EN_NEG_CL_LIMIT = 0		10.6	12.5	14.4	µA
			$\Delta V_{(IMON)}$ = 5mV; EN_NEG_CL_LIMIT = 0		0.8	2.5	4.2	µA

6.5 Electrical Characteristics (continued)

Typical values correspond to T_J=25°C. Minimum and maximum limits apply over T_J=-40°C to 150°C. Unless otherwise stated, $V_{(BIAS)}$ =12 V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVE PIN							
	Pull down resistance	SEL_DRV_SUP = 0b00, 0b01, 0b10				1400	Ω
	Pull up resistance	SEL_DRV_SUP = 0b01 or SEL_DRV_SUP = 0b10,				1500	Ω
	Maximum output current	SEL_DRV_SUP = 0b00, 0b01, 0b10	sink	3	9	16	mA
	Maximum output current	SEL_DRV_SUP = 0b01 or SEL_DRV_SUP = 0b10,	source	5	9	14	mA
	Pull down resistance	SEL_DRV_SUP = 0b11				900	Ω
	Pull up resistance	SEL_DRV_SUP = 0b11				1200	Ω
	Maximum output current	SEL_DRV_SUP = 0b11	sink	5	9	14	mA
	Maximum output current	SEL_DRV_SUP = 0b11	source	5	8	13	mA
	Charge pump switching frequency	SEL_DRV_SUP = 0b11			100		kHz
OUTPUT DISCHARGE							
	Output discharge current	VO_DISCH = 0b00		17.5	25	32.5	mA
	Output discharge current	VO_DISCH = 0b01		35	50	65	mA
	Output discharge current	VO_DISCH = 0b10		52.5	75	97.5	mA
$V_{TH-(DISCH)}$	Discharge done threshold			0.4	0.5	0.6	V
SPREAD SPECTRUM							
	Switching frequency modulation range upper limit				7.8		%
	Switching frequency modulation range lower limit				–7.8		%

6.6 Timing Requirements

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
OVERALL DEVICE FEATURES						
	Minimum time low EN toggle	time measured from EN toggle from H to L and from L to H	22			μs
I²C INTERFACE						
f_{SCL}	SCL clock frequency	Standard mode	0		100	kHz
		Fast mode	0		400	
		Fast mode plus [(1)]	0		1000	
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7			μs
		Fast mode	1.3			
		Fast mode plus [(1)]	0.5			
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4.0			μs
		Fast mode	0.6			
		Fast mode plus [(1)]	0.26			
t_{BUF}	Bus free time between a STOP and a START condition	Standard mode	4.7			μs
		Fast mode	1.3			
		Fast mode plus [(1)]	0.5			

6.6 Timing Requirements (continued)

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$t_{SU:STA}$	Set-up time for a repeated START condition	Standard mode	4.7			µs
		Fast mode	0.6			
		Fast mode plus (1)	0.26			
$t_{HD:STA}$	Hold time (repeated) START condition	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus (1)	0.26			
$t_{HD:DAT}$	Data hold time	Standard mode	0			µs
		Fast mode	0			
		Fast mode plus (1)	0			
t_r	Rise time of both SDA and SCL signals	Standard mode			1000	ns
		Fast mode	20		300	
		Fast mode plus (1)			20	
t_f	Fall time of both SDA and SCL signals	Standard mode			300	ns
		Fast mode	$20×V_{DD}/5.5$		300	
		Fast mode plus (1)	$20×V_{DD}/5.5$		120	
$t_{su:STO}$	Set-up time for STOP condition	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus (1)	0.26			
$t_{VD;DAT}$	Data valid time	Standard mode			3.45	µs
		Fast mode			0.9	
		Fast mode plus (1)			0.45	
$t_{VD;ACK}$	Data valid acknowledge time	Standard mode			3.45	µs
		Fast mode			0.9	
		Fast mode plus (1)			0.45	
C_b	Capacitive load for each bus line	Standard mode			400	pF
		Fast mode			400	

(1) Fast mode plus is supported but not fully compliant with I^2C standard

6.7 Typical Characteristics

The following conditions apply (unless otherwise noted): T_J = 25°C; $V_{(VCC2)}$ = 5V

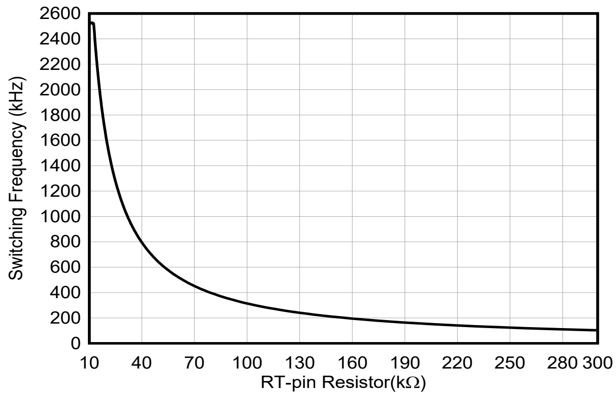

Figure 6-1. Switching Frequency Versus RT Resistance

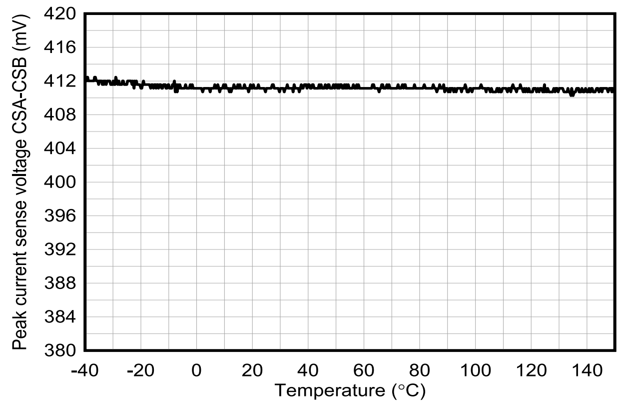

Figure 6-2. Switching Frequency versus Temperature $R_{(RT)}$ = 75KΩ

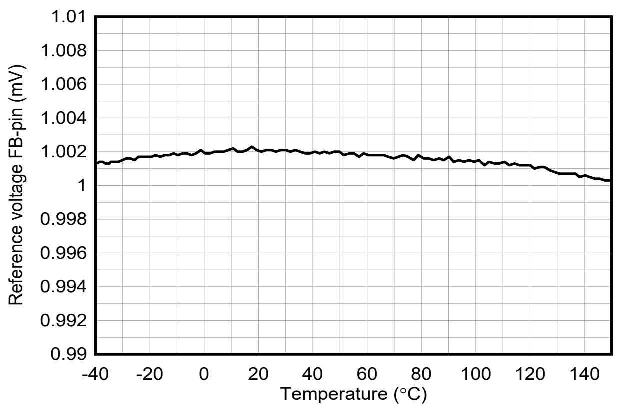

Figure 6-3. FB Pin Reference Voltage versus Temperature

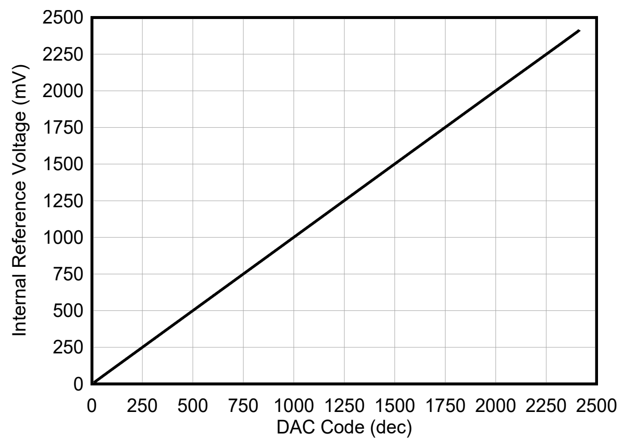

Figure 6-4. FB Pin Reference Voltage versus VO Register DAC-Code

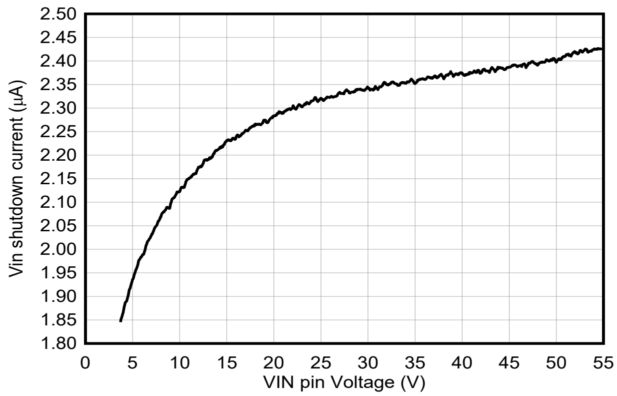

Figure 6-5. Shutdown Current into VIN versus Pin Voltage $V_{EN/UVLO}$ = 0V ,$V_{(VIN)}$ = 12V, $V_{(BIAS)}$ = 0V

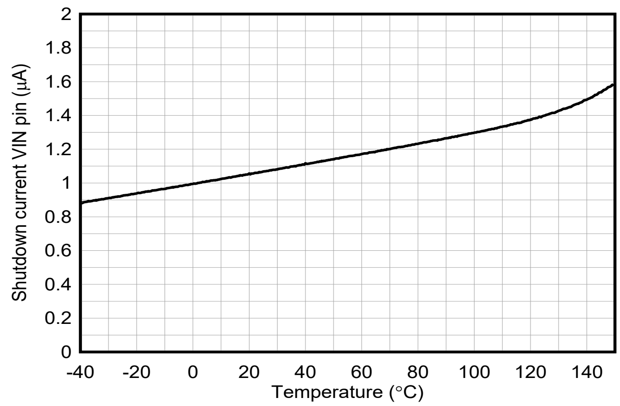

Figure 6-6. Shutdown Current into VIN versus Temperature $V_{EN/UVLO}$ = 0V ,$V_{(VIN)}$ = 12V,$V_{(BIAS)}$ = 0V

6.7 Typical Characteristics (continued)

The following conditions apply (unless otherwise noted): T_J = 25°C; $V_{(VCC2)}$ = 5V

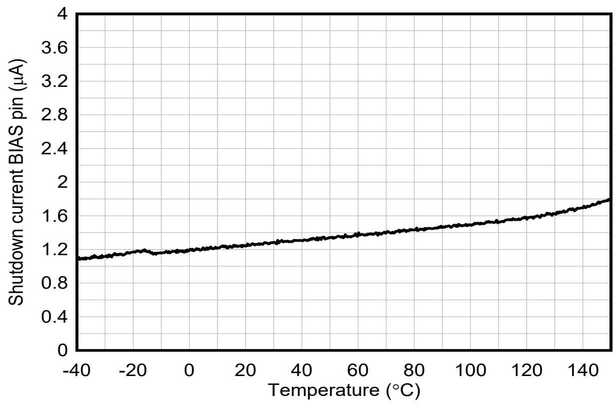

Figure 6-7. Shutdown Current into BIAS versus Temperature
$V_{EN/UVLO}$ = 0V ,$V_{(VIN)}$ = 3.5V,$V_{(BIAS)}$ = 12V

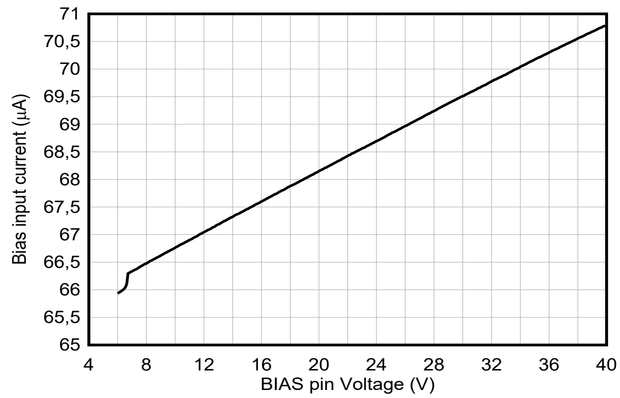

Figure 6-8. Quiescent Current into BIAS versus BIAS pin voltage
$V_{(VIN)}$ = 3.5V

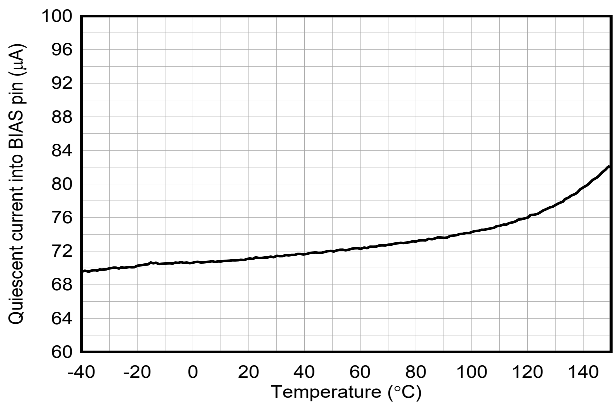

Figure 6-9. Quiescent Current into BIAS versus BIAS
$V_{(BIAS)}$ = 12V , $V_{(VIN)}$ = 3.5V

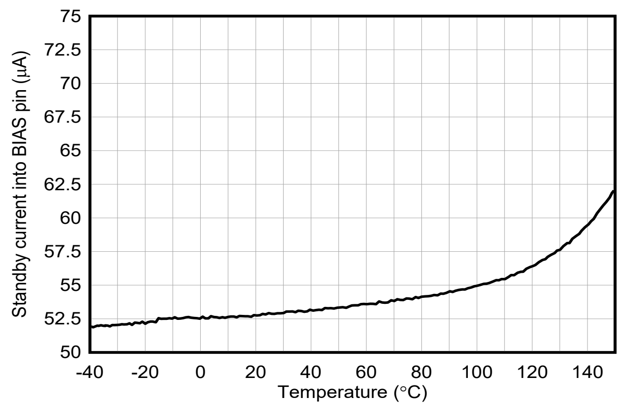

Figure 6-10. Standby Current into BIAS versus Temperature
$V_{(VIN)}$ = 3.5V $V_{(VIN)}$ = 12V

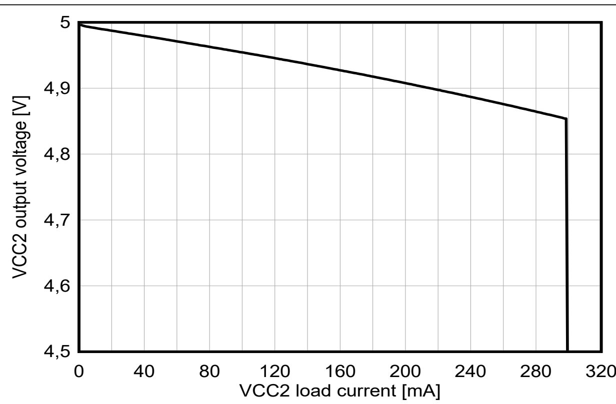

Figure 6-11. VCC2 LDO Output voltage versus VCC2 Load Current
$V_{(VIN)}$ = 12V, $V_{(BIAS)}$ = 0V

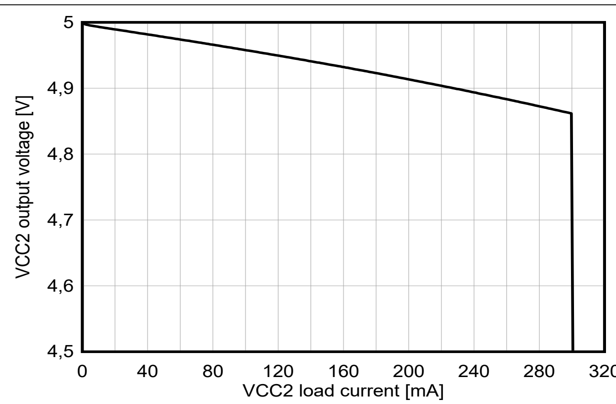

Figure 6-12. VCC2 LDO Output voltage versus VCC2 Load Current
$V_{(VIN)}$ = 3.5V, $V_{(BIAS)}$ = 12V

6.7 Typical Characteristics (continued)

The following conditions apply (unless otherwise noted): T_J = 25°C; $V_{(VCC2)}$ = 5V

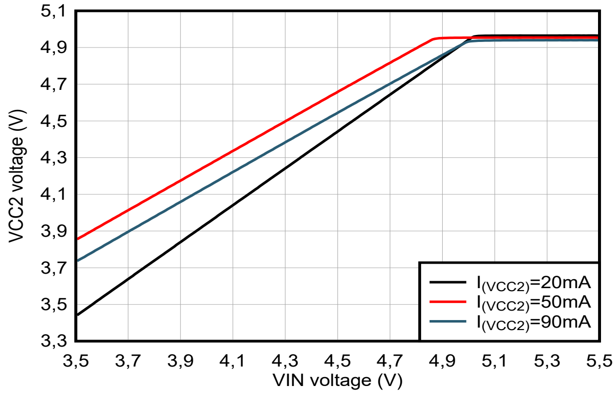

Figure 6-13. VCC2 LDO Output voltage versus VIN Voltage $V_{(BIAS)}$ = 0V

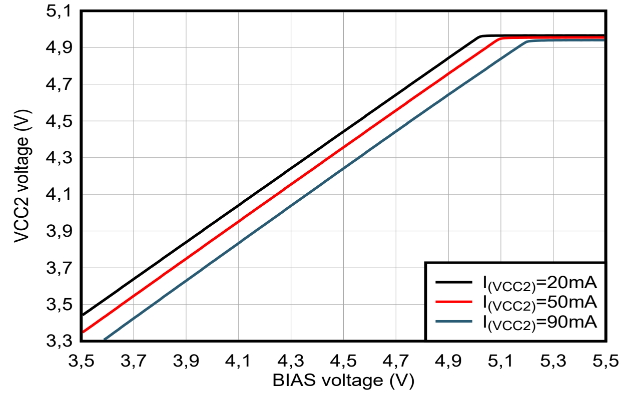

Figure 6-14. VCC2 LDO Output voltage versus BIAS Voltage $V_{(VIN)}$ = 2.5V

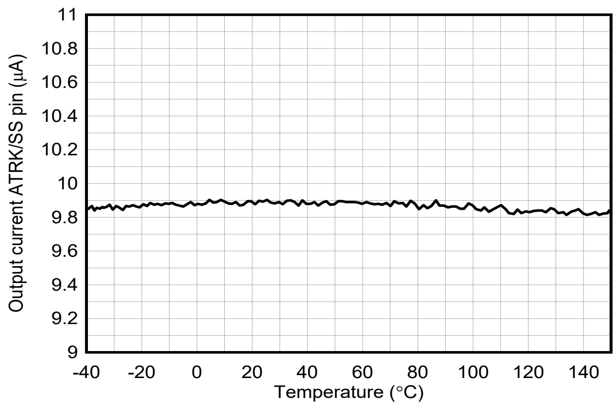

Figure 6-15. Soft-Start current versus Temperature

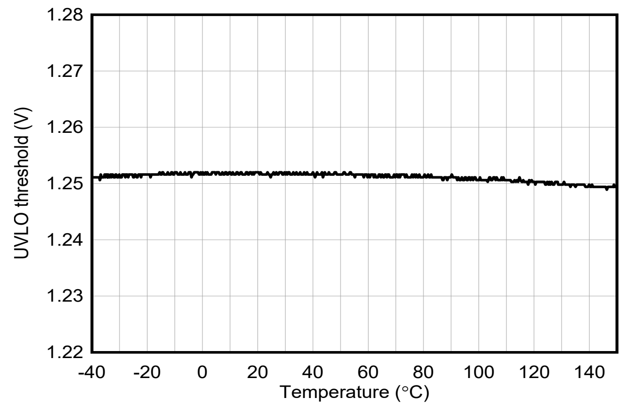

Figure 6-16. EN/UVLO Threshold versus Temperature

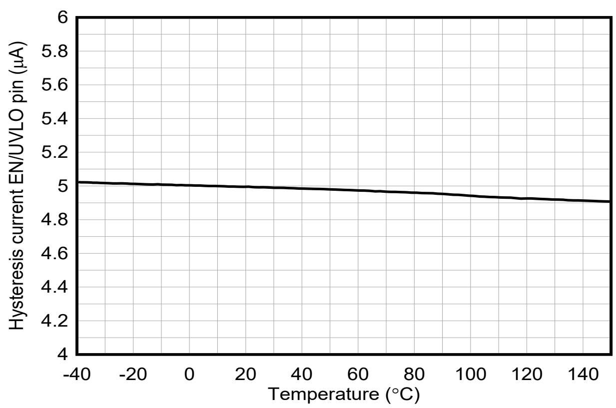

Figure 6-17. Hysteresis Current on EN/UVLO versus Temperature

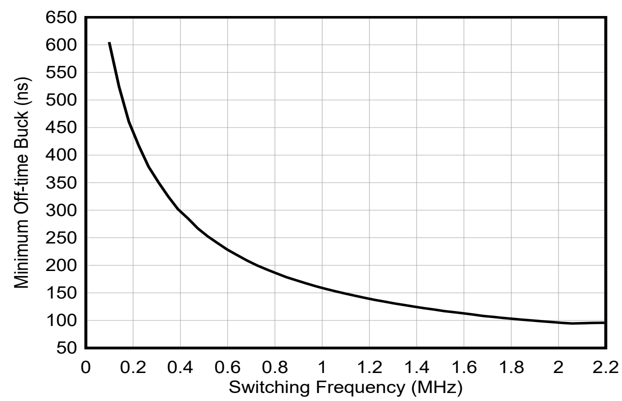

Figure 6-18. Buck Minimum Off-time versus Switching Frequency

6.7 Typical Characteristics (continued)

The following conditions apply (unless otherwise noted): T_J = 25°C; $V_{(VCC2)}$ = 5V

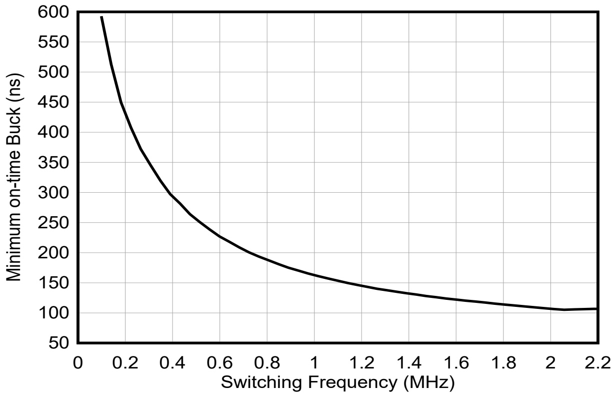

Figure 6-19. Buck Minimum On-time versus Switching Frequency

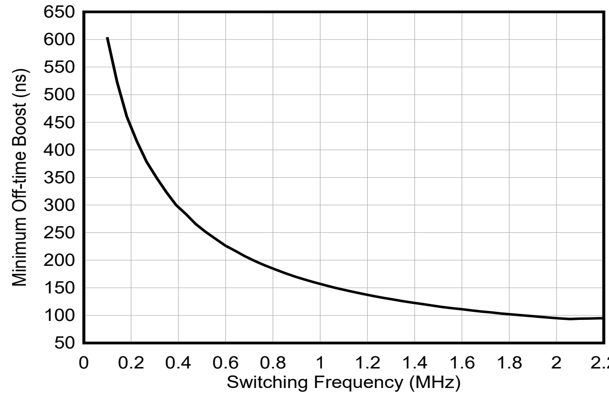

Figure 6-20. Boost Minimum Off-time versus Switching Frequency

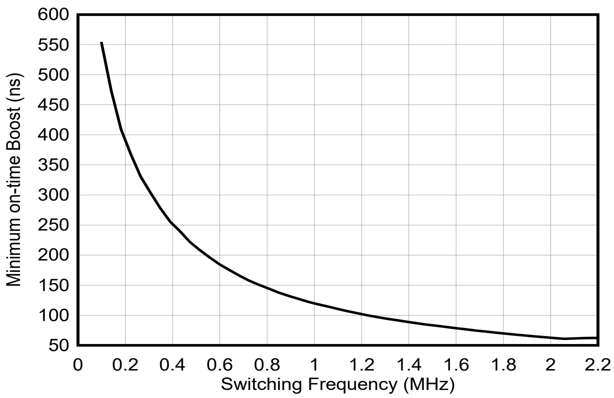

Figure 6-21. Boost Minimum On-time versus Switching Frequency

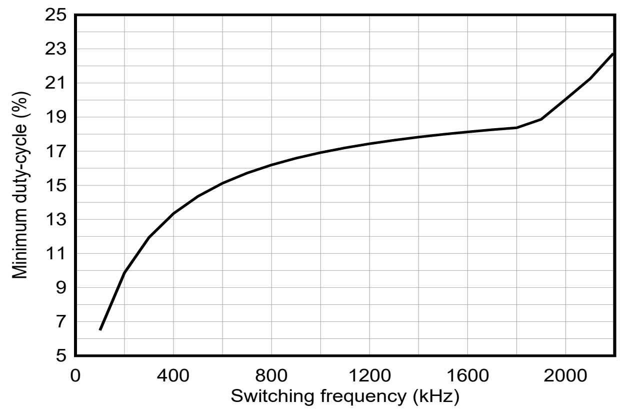

Figure 6-22. Buck Minimum Duty -cycle for PSM Operation versus Switching Frequency (SYNC_OUT = Enabled)

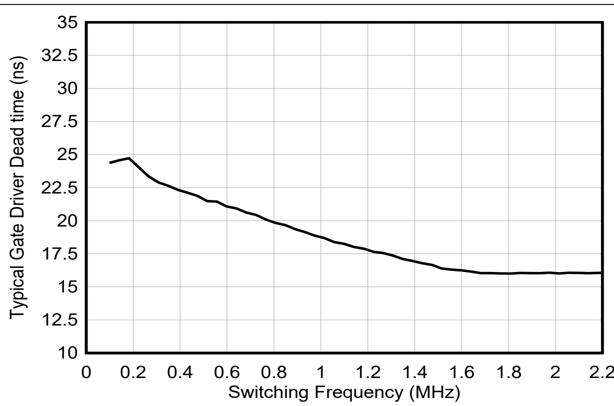

Figure 6-23. Gate Driver Transition (Dead) Time versus Switching Frequency
SEL_MIN_DEADTIME_GDRV = 0b01,SEL_SCALE_DT = 0b0, EN_CONST_TDEAD = 0b0

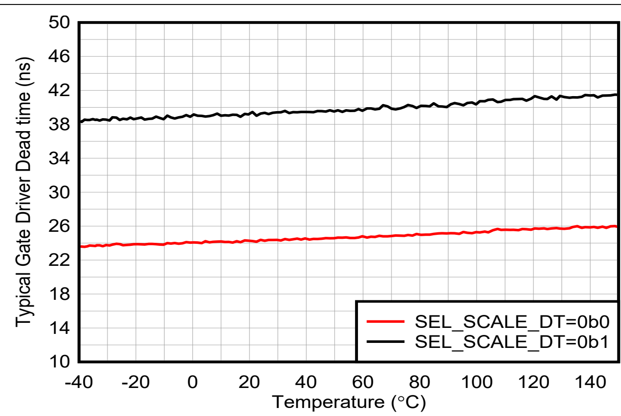

Figure 6-24. Gate Driver Transition (Dead) Time versus Switching Frequency
$f_{(sw)}$ = 100kHz ,SEL_MIN_DEADTIME_GDRV = 0b01, EN_CONST_TDEAD = 0b0, Turn Low-Side off, Turn High-Side on

6.7 Typical Characteristics (continued)

The following conditions apply (unless otherwise noted): T_J = 25°C; $V_{(VCC2)}$ = 5V

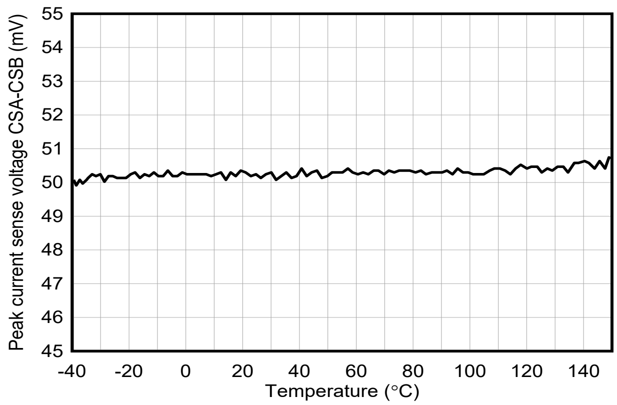

Figure 6-25. Peak Current Limit Threshold Voltage Versus Temperature

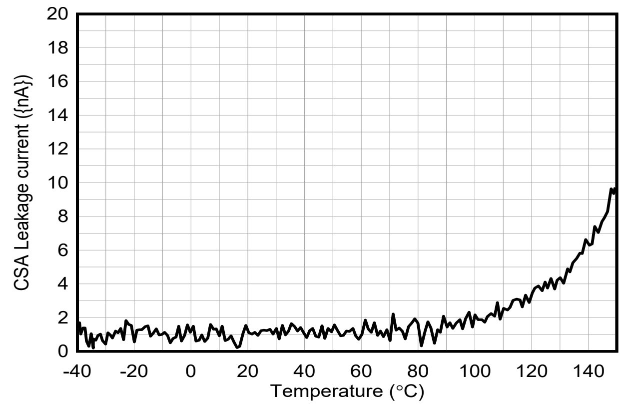

Figure 6-26. CSA Input Current versus Temperature

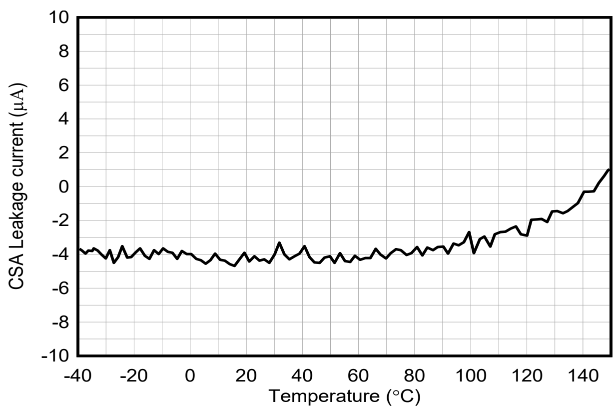

Figure 6-27. CSB Input Current versus Temperature

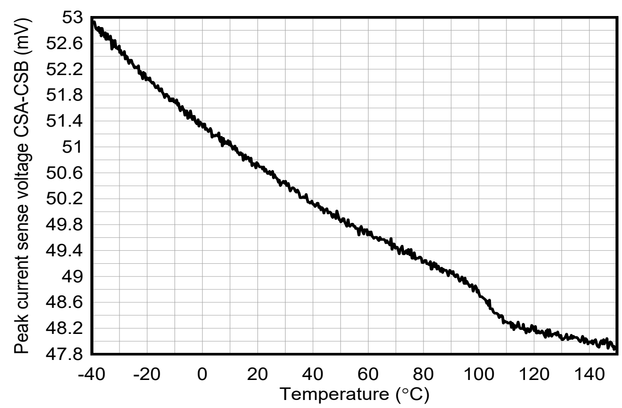

Figure 6-28. Average Current Limit Threshold Voltage Versus Temperature ILIM_THRESHOLD = 0x64

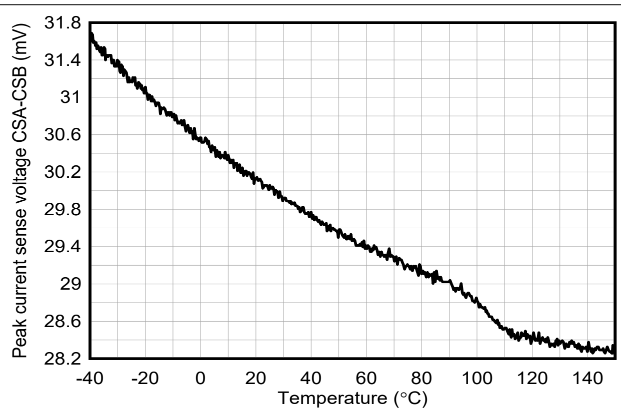

Figure 6-29. Average Current Limit Threshold Voltage Versus Temperature ILIM_THRESHOLD = 0x3C

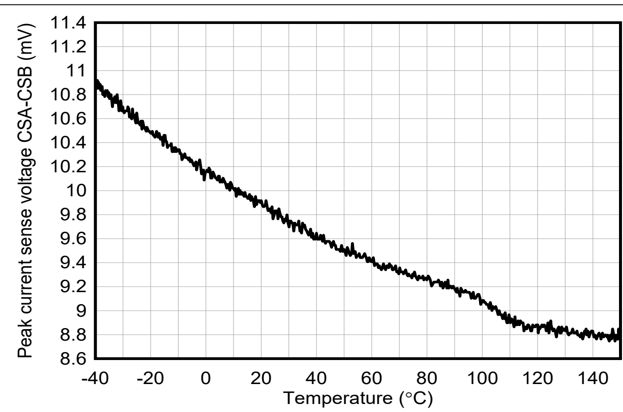

Figure 6-30. Average Current Limit Threshold Voltage Versus Temperature ILIM_THRESHOLD = 0x14

7 Parameter Measurement Information

Gate Driver Rise Time and Fall Time

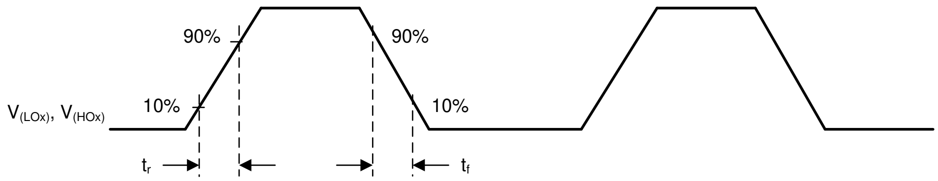

Figure 7-1. Timing Diagram Gate Driver t_r , t_f

Gate Driver Dead (Transition) - Time

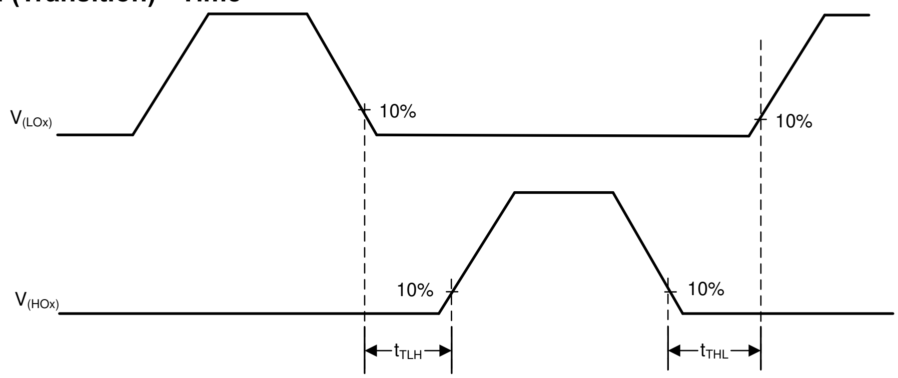

Figure 7-2. Timing Diagram Gate Driver t_t

8 Detailed Description

8.1 Overview

The LM251772-Q1 is a four switch Buck-Boost controller. The device provides a regulated output voltage if the input voltage is higher, equal or lower as the adjusted output voltage. In power-save mode the device supports a high efficiency over the full range of the output load.

The LM251772-Q1 runs at a fixed switching frequency (in fPWM), which is set via the RT and SYNC pin. The switching frequency remains constant during buck, boost and buck-boost operation. The device maintains small mode transition ripple over all operating modes.

programming the output voltage and device configurations dynamically using the integrated I2C interface is possible. The integrated and optional high side current sensor features an accurate and output current limitation. The average current limit of the LM251772-Q1 is also configurable through the I2C interface.

8.2 Functional Block Diagram

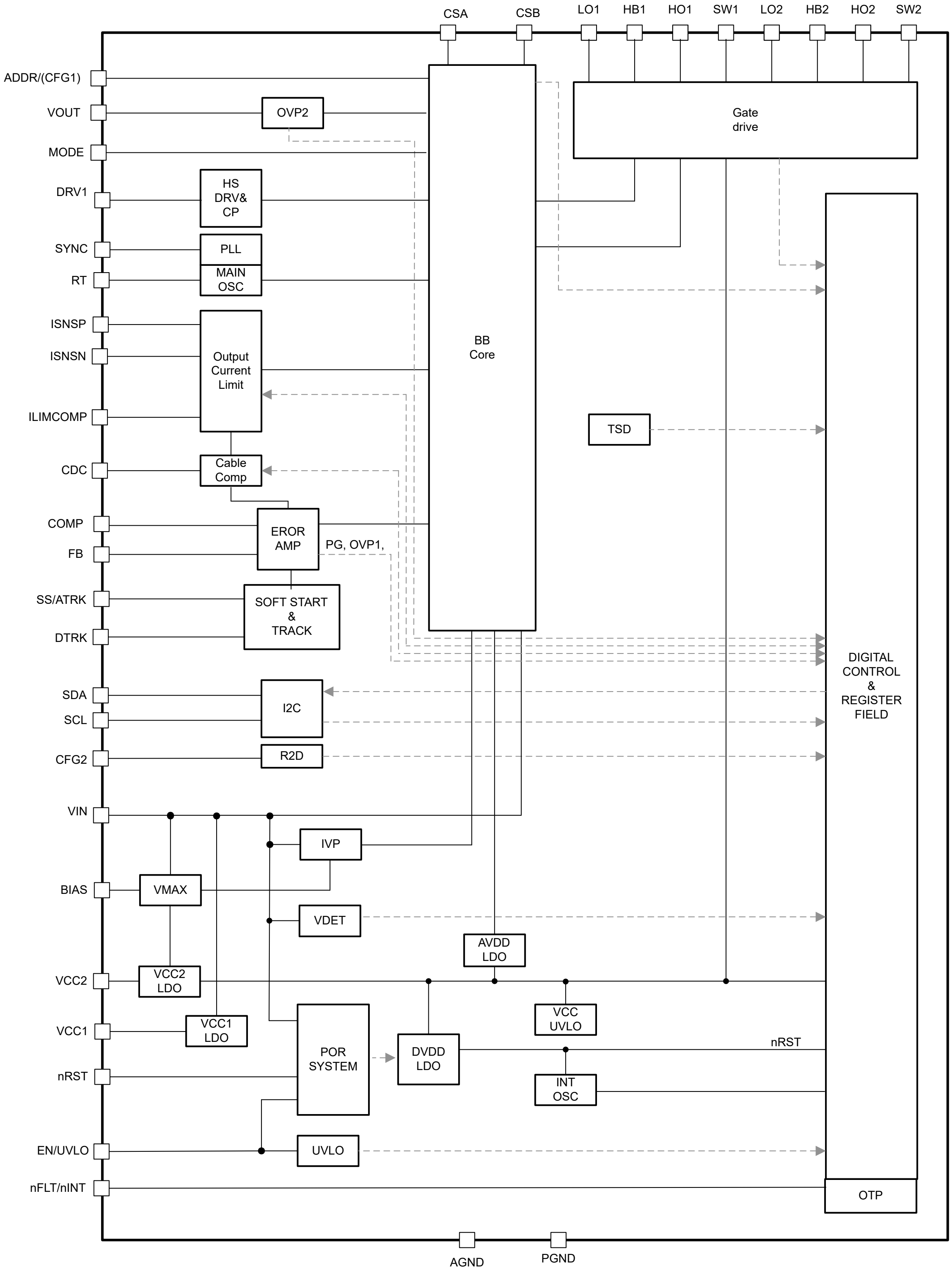

Figure 8-1. LM251772-Q1 Functional Block Diagram

8.3 Feature Description

8.3.1 Buck-Boost Control Scheme

The LM251772-Q1 buck-boost control algorithm enables a seamless transition between the different operating modes, fixed frequency operation, and power stage protection features. The internal state machine controls the current flow using three active switching states:

State I: Transistors Q1 and Q3 are conducting. Q2 and Q4 are not conducting (boost mode magnetization state).

State II: Transistors Q1 and Q4 are conducting. Q2 and Q3 are not conducting (boost demagnetization or buck magnetization state).

State III: Transistors Q2 and Q4 are conducting. Q1 and Q3 are not conducting (buck demagnetization state).

Switch	State I	State II	State III
Q1	ON	ON	OFF
Q2	OFF	OFF	ON
Q3	ON	OFF	OFF
Q4	OFF	ON	ON

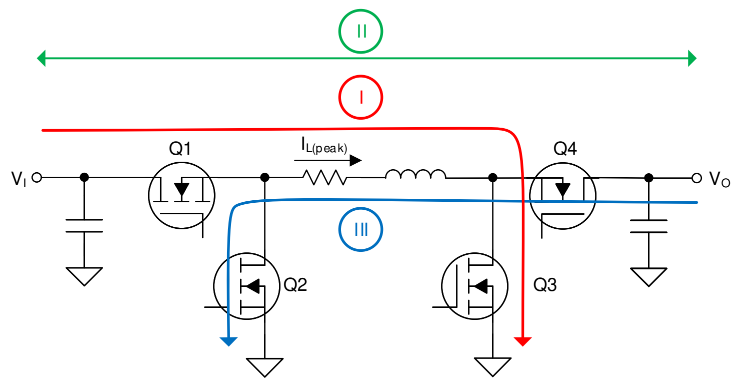

Figure 8-2. Buck-Boost Active Switching States

8.3.1.1 Buck Mode

In buck mode operation, the converter starts a buck magnetization cycle (state II) with the internal clock signal. When the inductor reaches the peak current, the converter proceeds to the buck demagnetization (state III). With the next clock signal, the converter changes back to a buck magnetization cycle and starts a new switching cycle with sampling the peak current. As long as the duty cycle does not reach the minimum off-time, the current control remains in buck operating mode.

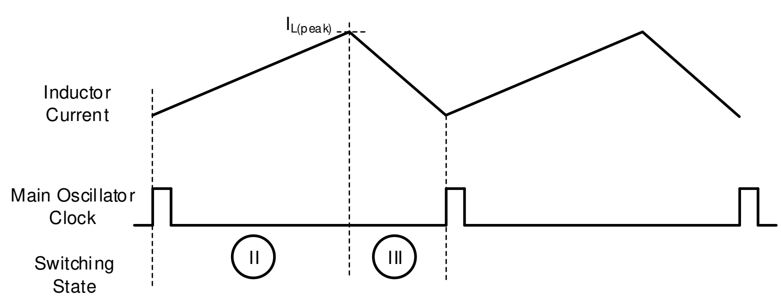

Figure 8-3. Inductor Current in Continuous Current Buck Operation

8.3.1.2 Boost Mode

In boost mode operation, the converter starts a boost magnetization cycle (switching state I) with the internal clock signal. After the converter samples the inductor current, the device transitions to switching state II, which is the boost demagnetization state. The maximum duty cycle in boost mode is limited by the minimum boost on-time and the selected switching frequency.

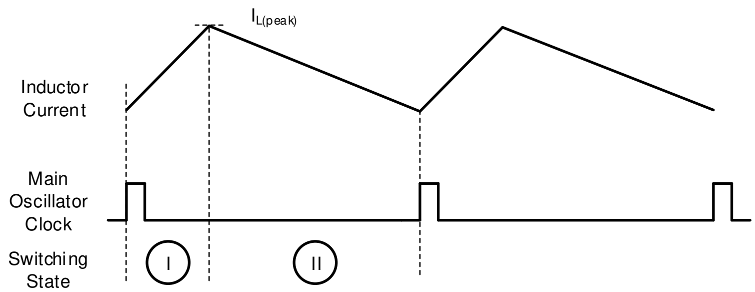

Figure 8-4. Inductor Current in Continuous Current Boost Operation

8.3.1.3 Buck-Boost Mode

As soon as the on time in boost mode operation is lower than the minimum on-time or the off-time in buck mode is lower than the minimum off-time, the control transits into the buck-boost operation. In the continuous current buck-boost mode, the control adds a boost magnetization (state I) switching cycle before the peak current is reached. Therefore, buck-boost operation mode always consists of all three switching cycles state I, state II, and state III. The peak current detection in this mode happens at the end of switching state I.

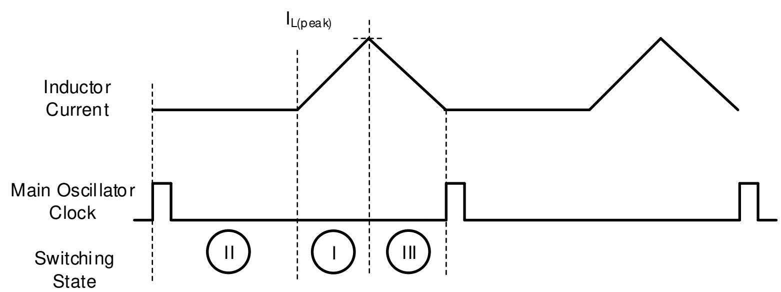

Figure 8-5. Inductor Current in Continuous Buck-Boost Operation

8.3.2 Power Save Mode

With the MODE pin low, power save mode (PSM) is active. In this operating mode, the switching activity is reduced and efficiency is maximized. If the mode pin is high, power save mode is disabled. The converter then operates in continuous conduction mode (CCM) or forced PWM mode (fPWM).

In PFM boost, buck or in buck-boost mode, the converter is operating down to the minimum defined peak current. If this minimum current (PSM entry threshold) is reached the PWM changes the operation to single pulse. The single pulse operation consists all three states (I, II.III). The duty cycles in single pulse operation are timer based and adopt to the different VIN and VOUT sense voltages. To get a small output voltage ripple the converter modulation scheme uses one or multiple single pulses for the switching activity below the PSM entry threshold.

If the inductor current (load current) further decreases, the frequency of the single pulses are reduced to approximately one quarter of the selected switching frequency. With a further decrease of the inductor (load current) the output voltage increases, as the energy consumed by the load is less than what the converter generates during switching. If the V_O increase the voltage regulation loop detects the increase and turns the device into a pause or if enabled a TI proprietary sleep mode (µSleep).

In µSleep mode, both low sides are turned on to provide the high-side gate supply for HB1 and HB2 are charged. Other internal circuits are partially turned off to reduce the current consumption of the converter to a minimum possible. In case the output voltage reaches the nominal output voltage set point, the switching activity starts again after a short wake-up time.

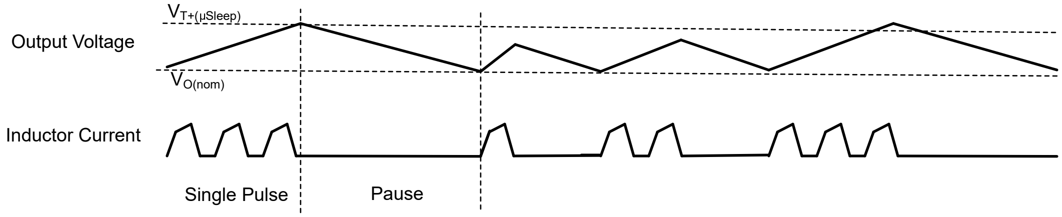

Figure 8-6. Timing Diagram for the Power Save Mode (μSleep Disabled)

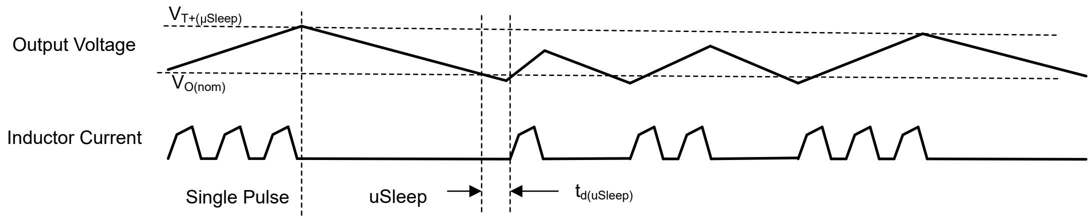

Figure 8-7. Timing Diagram for the Power Save Mode (μSleep Enabled)

The PSM - ACM (automated conduction mode) is a high output current power save mode for the 4 switch buck-boost operation. In the buck-boost operation area with loads higher than the PSM entry threshold, switching pulses are skipped and the control enters ACM. Here the device regulation maintains in State II and conducts the input to the output of the power stage. When necessary, the control initiates switching activities with a minimum time of state I or state III to maintain the inductor current as required by the voltage regulation loop. Hence the output voltage is still fully regulated and the device maintains all protection features like the OCP.

The LM251772-Q1 features an adaptive power save mode threshold (see Figure 8-8). The internal algorithm derives $I_{VT(PSM)}$ from:

- The applied input voltage sense on VIN pin
- The output voltage derived from the VOUT pin
- The programmed slope compensation factor (m_{sc}) using the SEL_SLOPE_COMP register in MFR_SPECIFIC_D7 Register Field Descriptions
- The selected SEL_INDUCT_DERATE setting in MFR_SPECIFIC_D0 Register Field Descriptions.

  Select the inductor de-rating based on the inductor manufacturer data sheet at the maximum current the power stage (R_{CS}) of the LM251772-Q1 is designed for.

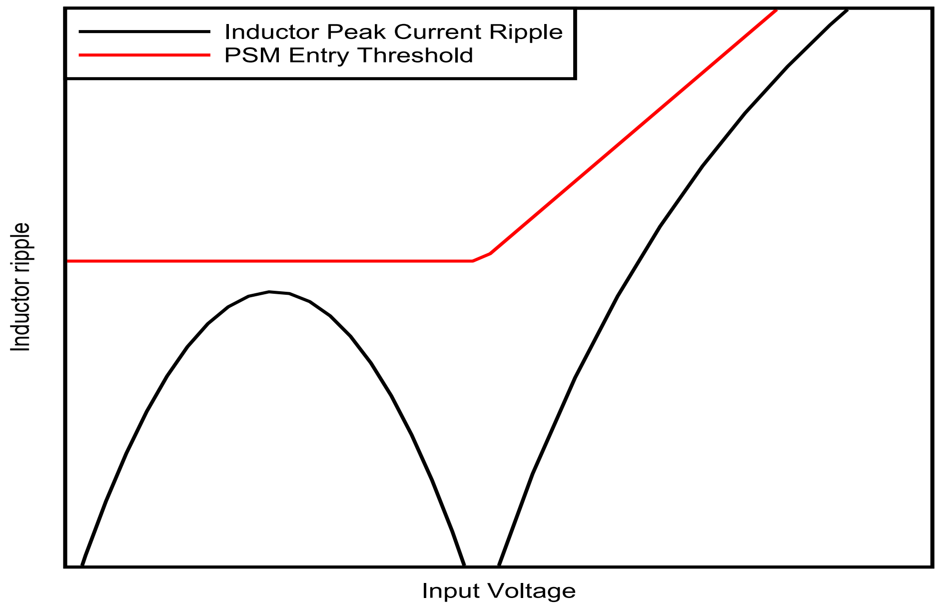

Figure 8-8. Generic Graph of PSM Entry Threshold And Ripple Current Versus Input Voltage

8.3.3 Reference System

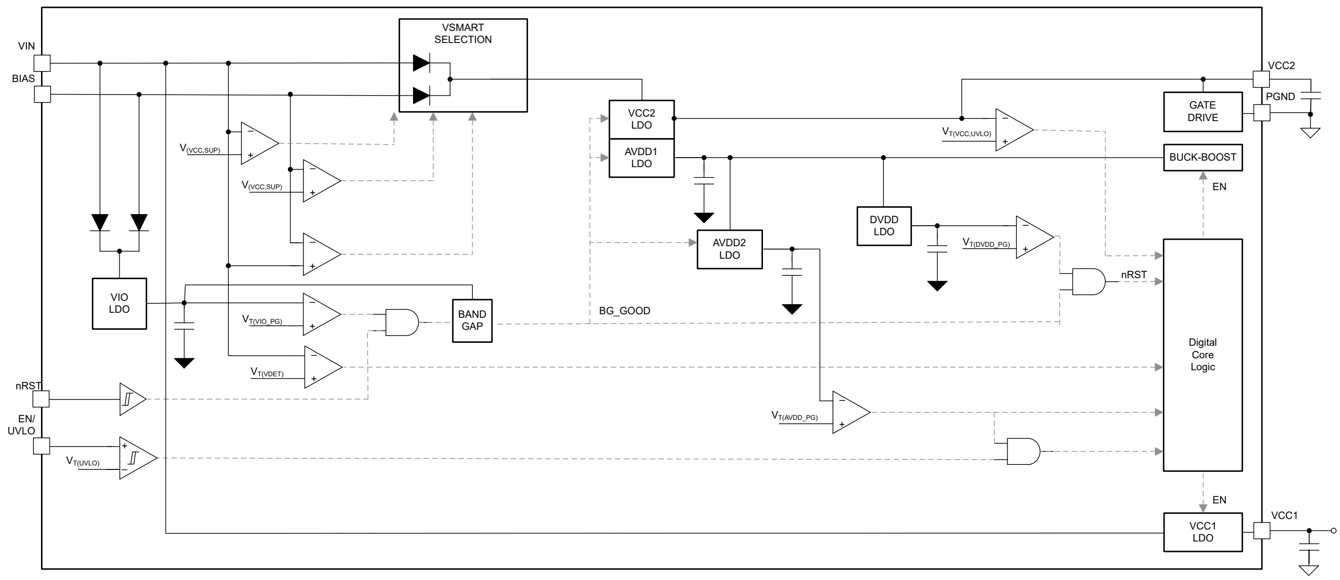

Figure 8-9. Functional Block Diagram Reference System

8.3.3.1 VIO LDO and nRST-PIN

The VIO LDO supplies the IO pin buffers and comparators. Once the voltage on the VIN-pin or BIAS-pin is above the positive going POR threshold VT+(POR) and the nRST-PIN is higher than VT+(nRST) the internal bias is active and the device is in standby mode.

When the nRST - pin is below the standby threshold $V_{T-(nRST)}$, the device is held in a low power shutdown mode to maintain a minimum input quiescent current of the device supply rails.

8.3.4 Supply Voltage Selection – VSMART Switch and Selection Logic

There are two pins to supply the LM251772-Q1 internal voltage regulators. Due to the internal supply voltage selection circuit, the device reduces the internal power dissipation by providing a seamless operation at low input or output voltages as well as in transient operating conditions like an output short. The VSMART switch selects the pin with the lower voltage from the VIN or BIAS pin once the voltage on both is above the switch-over threshold ($V_{T(VCC,\ SUP)}$). If one pin voltage is lower than the threshold, the other supply pin is selected. And if both pins are lower than the switch-over threshold, the higher voltage of VIN or BIAS is selected as supply. The following are common configurations for the supply pins:

- The VIN pin is connected to the supply voltage. The BIAS pin is connected to VOUT. During start-up, as long as the output voltage is not higher than the supply switch-over threshold, VIN supplies the internal regulators. Once V_O is high enough, the supply current comes from the BIAS pin.
- The VIN is connected to the input supply voltage and the BIAS pin is connected to an auxiliary supply (for example, an existing 12V DC/DC converter). This configuration is commonly used at high voltage applications on the input and output voltages where the power dissipation over the integrated linear regulators need to be further minimized for thermal reasons.
- If the BIAS pin is not used, put BIAS to ground, the device always used the VIN LDO, and the quiescent is minimized.

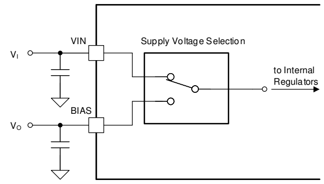

Figure 8-10. VSMART Supply Scenario 1

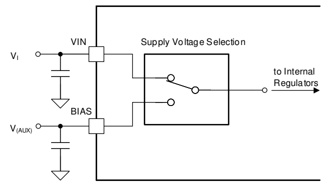

Figure 8-11. VSMART Supply Scenario 2

To achieve a minimum of power losses over the LDO the VSMART logic decides which voltage is the closest one to the target supply $V_{T(VCC,SUP)}$. When the FORCE_BIAS bit is set to 0b1, the device does not directly select the highest voltage between the two supply pins BIAS and VIN. The Table 8-1 gives an overview for the selection conditions:

Table 8-1. VSMART Selection Truth Table

$V_{(BIAS)}$	$V_{(VIN)}$	VSMART supply
X	> $V_{T+(VCC2,SUP)}$ && < $V_{(BIAS)}$	VIN-PIN
> $V_{T+(VCC2,SUP)}$ && < $V_{(VIN)}$	X	BIAS-PIN
< $V_{T-(VCC2,SUP)}$	X	VIN-PIN
X	< $V_{T-(VCC2,SUP)}$	BIAS-PIN
> $V_{T+(VCC2,SUP)}$ && > $V_{(VIN)}$	> $V_{T+(VCC2,SUP)}$	VIN-PIN
> $V_{T+(VCC2,SUP)}$	> $V_{T+(VCC2,SUP)}$ && > $V_{(BIAS)}$	BIAS-PIN

If the FORCE_BIAS bit is set, the bit lowers and prioritizes the switchover threshold for the BIAS pin. Intention is to support an external supply of nominal 5V for the VCC2 but still be able to start-up with the VIN supply if the sequencing if the external supply does not meet the start-up timing. The selection of the VCC2 supply follows this behavior:

- If the BIAS voltages is below the $V_{T+(Force,BIAS)}$, then the VIN gets selected.
- If the BIAS voltage is above $V_{T+(Force,BIAS)}$, then the BIAS gets selected regardless of VIN being above the $V_{T+(VCC2,SUP)}$

8.3.5 Enable and Undervoltage Lockout

The LM251772-Q1 has a dual function enable and undervoltage lockout (UVLO) pin. Figure 8-12 shows the UVLO block diagram.

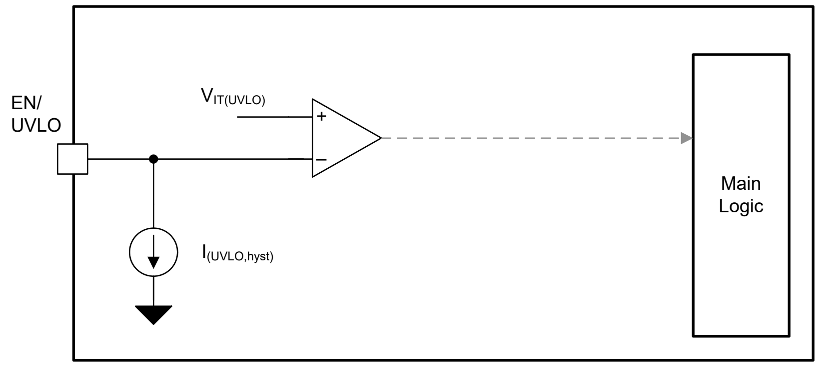

Figure 8-12. Functional Block Diagram UVLO

8.3.5.1 UVLO

With this function the device detects an low input voltage condition for the power stage to avoid a brown out condition. The detection threshold as well as the required hysteresis is adjustable with the external voltage divider on the EN/UVLO - pin.

The UVLO features an internal delay time ($t_{d(UVLO)}$) for the shutdown to avoid any undesired converter shutdown due to input noise on the UVLO detection pin. If the voltage on the EN/UVLO - pin is below the $V_{T-(UVLO)}$ threshold for the delay time $t_{d(UVLO)}$, the device logic immediately stops the converter operation

If the EN/UVLO-pin voltage is below the $V_{T+(EN)}$ threshold the internal current source for the UVLO hysteresis is active. If the EN/UVLO-pin voltage is above the $V_{T+(UVLO)}$ threshold the internal current source for the UVLO hysteresis is off.

8.3.6 Internal VCC Regulators

8.3.6.1 VCC1 Regulator

The LM251772-Q1 features a VCC1 regulator which provides an LDO output for auxiliary use in the system. VCC1 gets directly supplied by VIN pin. In most applications the output is used to supply the I2C controller device which sends data to the LM251772-Q1. See the application below.

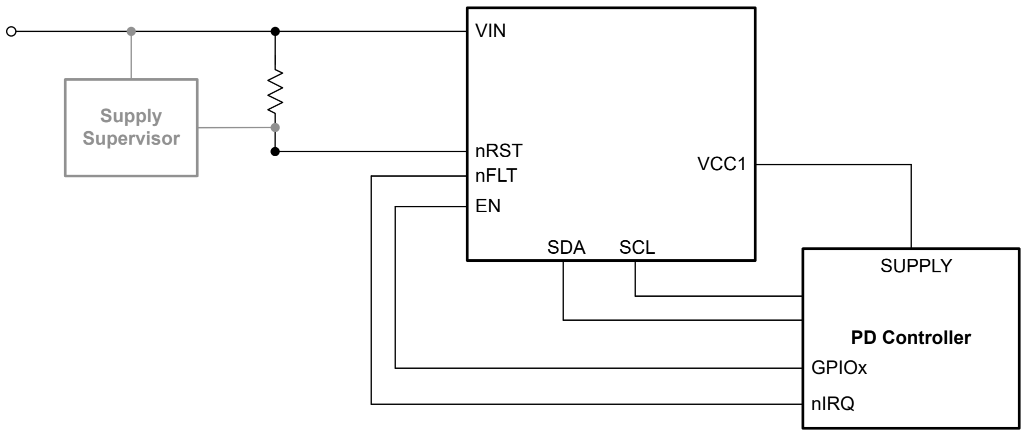

Figure 8-13. Simplified Schematic

The VCC1 starts up when the device enters the standby mode to allow the power sequence of the system to be met. See a typical power up sequence below.

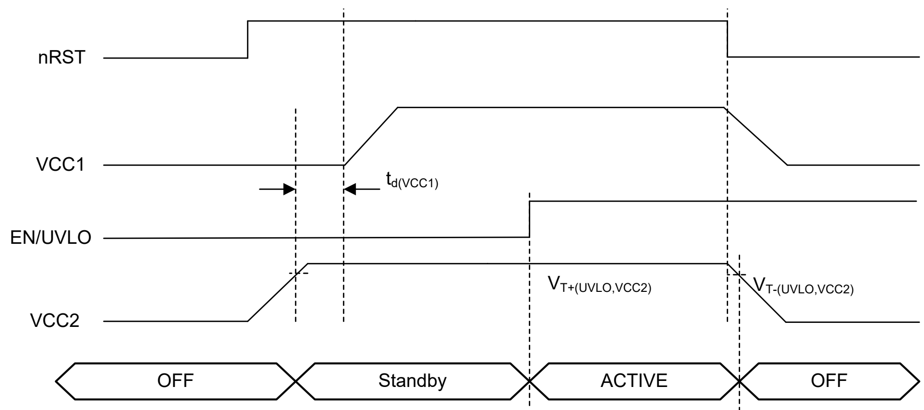

Figure 8-14. Timing Diagram VCC Regulator

The VCC1 regulator provides high DC accuracy at light load condition to support a use as a reference voltage for external circuits for example a comparator or operational amplifier.

The VCC1 is enabled/disabled via R2D or the I^2C interface . Therefore the start-up of VCC1 is gated by the R2D readout.

8.3.6.2 VCC2 Regulator

The VCC2 regulator is the supply for the integrated gate driver. The LDO starts in low-current, pre-bias mode, once the voltage on the nRST-Pin is higher than the rising threshold. If the EN/UVLO pin is higher than the rising threshold the VCC2 is fully active and provides the target performance specified by the electrical characteristics parameters.

Do not connect an external load to the VCC2-PIN

8.3.7 Error Amplifier and Control

8.3.7.1 Output Voltage Regulation

The device features an internal error amplifier (EA) to regulate the output voltage. The output voltage gets sensed on the FB-pin. The reference for the EA is supplied via the soft-start and V_O tracking pins. The COMP-pin is the output of the gm-stage and gets connected to the external compensation network.

Due to the selected implementation of the error amplifier, the voltage on the LM251772-Q1 COMP pin, is in steady-state, accurately reflecting the nominal peak-current value of the inductor.

The Figure 8-15 shows the control V/I-characteristics of the error amplifier in fPWM mode. Use the below image as guidance for applicative designs that require an external control of the inner peak current loop regulation.

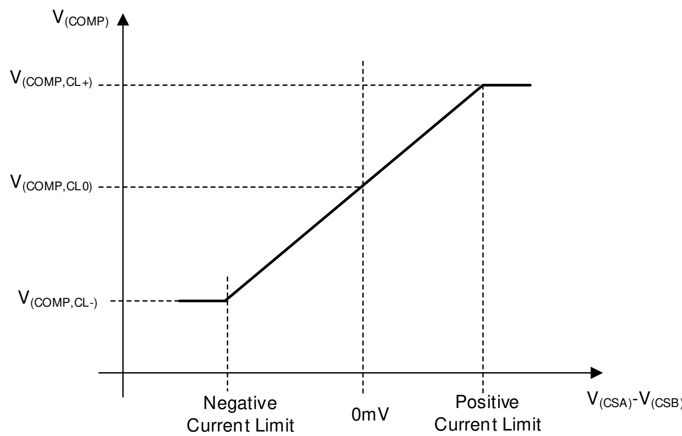

Figure 8-15. Control Function for the Peak Current Sense Voltage Versus V_{COMP}

8.3.7.2 Output Voltage Feedback

For applications with external feedback divider use a resistive divider network from the output capacitance to the FB-pin. Use the following equation to calculate the resistor values.

$$R_{FB,top} = \left(V_{(VOUT)} - V_{(REF)}\right) \times R_{FB,bot} \quad (1)$$

To maintain fixed voltage and interface programmable voltage the device contains an internal voltage divider. In this case the FB is not used for sensing the output voltage for the loop regulation. Instead the VOUT-pin is used to sense the output voltage on the power stage.

The selection between internal and external feedback divider is done through the FB pin. If the voltage on the FB-pin is higher than $V_{T+(SEL,iFB)}$, before the soft-start is initiated, the device operates with the internal feedback. The selection of internal and external FB cannot be done dynamically and the pin information gets latched until the next EN or $V_{(POR)}$ power cycle. A simple method of selecting the internal feedback divider is to connect the divider to VCC2.

The ratio of the internal feedback divider can be changed with the SEL_DIV20 bit (see MFR_SPECIFIC_D8 Register Field Descriptions).

Rewriting VOUT_A after changing SEL_DIV20 bit is recommended.

Below an overview of the possible Vo setting according the VOUT_A and SEL_DIV20

Table 8-2. SEL_DIV 20 = 0b0

Parameter	Value
Output voltage min.	1.0V
Output voltage max.	24V
Output voltage programming step size typ.	10mV

Use the following equation to calculate the nominal output voltage:

$$V_{(O,NOM)} = [[VOUT\_TARGET1\_MSB[3:0]][VOUT\_TARGET1\_LSB[7:0]]] \cdot 10\ mV \tag{2}$$

Table 8-3. SEL_DIV 20 = 0b1

Parameter	Value
Output voltage min.	3.3V
Output voltage max	48V
Output voltage programming step size typ.	20mV

The read-out register value of the 'VOUT_A' control register is clamped for the lower and for the upper limit of the register range.

- The reg. readout value is clamped to the lowest clamp voltage (for example 3.3V if SEL_FB_DIV20 = 0b1) if a register value below the value of clamp voltage (for example 3.3V) has been written in before.
- The reg. readout value is clamped to the highest clamp voltage (for example 48V if SEL_FB_DIV20 = 0b1) if a register value above the highest value of clamp voltage (for example 48V) has been written in before.

Use the following equation to calculate the nominal output voltage:

$$V_{(O,NOM)} = [[VOUT\_TARGET1\_MSB[3:0]][VOUT\_TARGET1\_LSB[7:0]]] \cdot 20\ mV \tag{3}$$

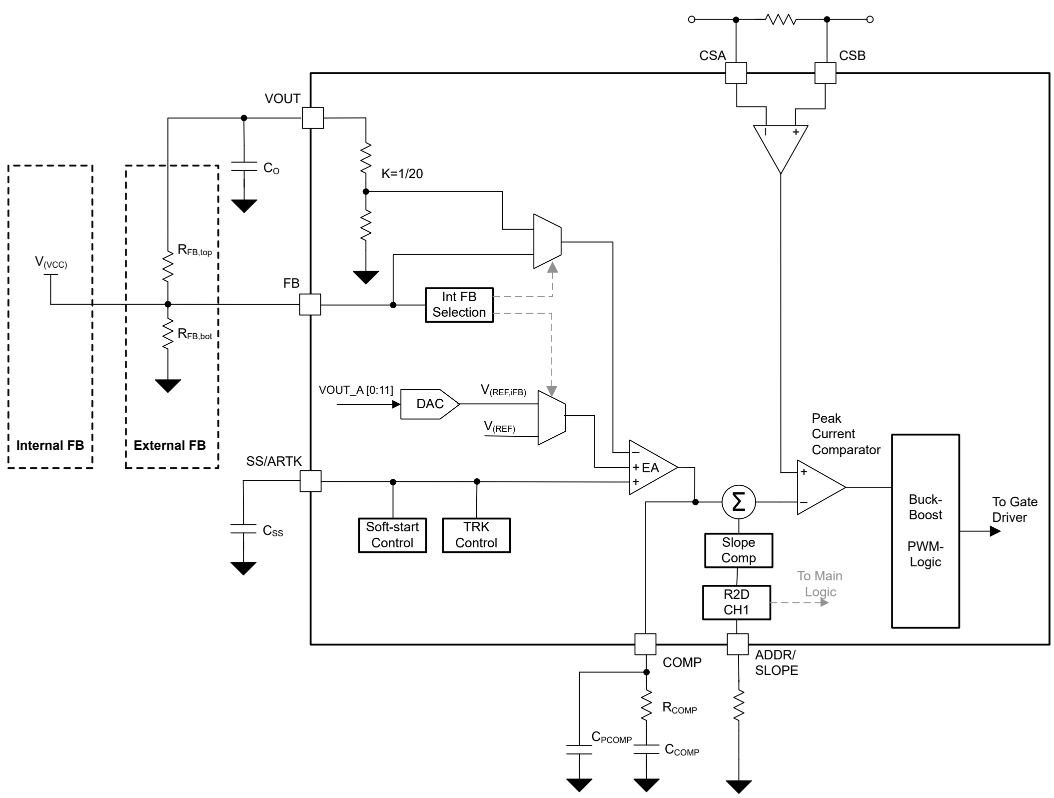

Figure 8-16. EA Functions Block Diagram

8.3.7.3 Voltage Regulation Loop

The LM251772-Q1 features an internal error amplifier (EA) to regulate the output voltage. The output voltage gets sensed on the FB pin through external resistors, which determine the target or nominal output voltage. The reference for the EA builds the soft-start and analog output voltage tracking pin (SS/ATRK). The COMP pin is the output of the internal gm-stage and gets connected to the external compensation network. The voltage over the compensation network is the nominal value for the inner peak current control loop of the device.

Use the following equations to calculate the external components:

External Feedback:

$$R_{(COMP)} = \frac{2\pi \times f_{(BW)}}{gm_{(ea)}} \times \frac{R_{(FB,bot)} + R_{(FB,top)}}{R_{(FB,bot)}} \times \frac{10 \times R_{(CS)} \times C_O}{1 - D_{max}} \quad (4)$$

Internal Feedback:

$$R_{(COMP)} = \frac{2\pi \times f_{(BW)}}{gm_{(ea)}} \times 20 \times \frac{10 \times R_{(SNS1)} \times C_O}{1 - D_{max}} \quad (5)$$

Common for Internal and External Feedback:

$$C_{(COMP)} = \frac{1}{2\pi \times f_{(CZ)} \times R_{(COMP)}} \quad (6)$$

$$C_{(PCOMP)} = \frac{1}{2\pi \times 10 \times f_{(BW)} \times R_{(COMP)}} \quad (7)$$

For most applications, TI recommends the following guidelines for bandwidth selection of the compensation.

The hard limit of the bandwidth ($f_{(BW)}$) is the right half plane zero of the boost operation:

$$f_{RHPZ} = \frac{1}{2\pi} \times \frac{V_{(VOUT)} \times \left(1 - D_{max}\right)^2}{I_{o,max} \times L} \quad (8)$$

The maximum recommended bandwidth must be within the following boundaries:

$$f_{(BW)} < \frac{1}{3} \times f_{RHPZ} \quad (9)$$

$$f_{(BW)} < \frac{1}{10} \times \left(1 - D_{max}\right) \times f_{(SW)} \quad (10)$$

The compensation zero (f_{CZ}) must be placed in relation to the dominating pole of the boost.

$$f_{CZ} = 1.5 \times f_{pole,boost} \quad (11)$$

$$f_{pole,boost} = \frac{1}{2\pi} \times \frac{2 \times I_{o,max}}{V_{(VOUT)} \times C_O} \quad (12)$$

8.3.7.4 Dynamic Voltage Scaling

The device features a dynamic voltage scaling (DVS), in case the output voltage register gets programmed during the converter is in operation. The DVS feature avoids excessive current and voltage spike as the control loop bandwidth is set by external components. If the output voltage target gets programmed in the converter off state converter soft-start ramps V_O to the newly programmed target voltage.

Once the VOUT_A field of the register is changed the reference voltage slowly changes over to the new target value. The rising and falling slew rate do not exceed the defined $\Delta V_{o(DVS)}$ within the time $t_{d(DVS)}$. The slope time is programmable via NVM setting.

If the converter operates in PSM, negative inductor current blocked by the converter. The device features a passive and a active DVS configuration, selectable using NVM setting. If passive DVS is selected the Vo slope of the system does not follow the defined DVS slew rates as the output capacitor is only discharged passively using the output load. If active DVS is selected the internal output discharge is active during the negative ramp of the DVS. The maximum discharge current is used for the active DVS setting, independently of the register selection of the discharge strength. The output capacitor voltage can follow the reference as long as the capacitor is selected to match the maximum discharge current for the selected DVS ramp speed.

8.3.8 Output Voltage Discharge

The LM251772-Q1 features a internal output discharge circuit.

The discharge strength is configured with the register DISCHARGE_STREGTH (see MFR_SPECIFIC_D2 Register Field Descriptions) to achieve different slew rates of the output voltage while discharging. The sequence is configured with the registers DISCHARGE_CONFIG0 and DISCHARGE_CONFIG1 in MFR_SPECIFIC_D2 Register Field Descriptions.

The register FORCE_DISCH in USB_PD_CONTROL_0 Register Field Descriptions forces the discharge circuit to be enabled or disabled and overwrites the sequence settings.

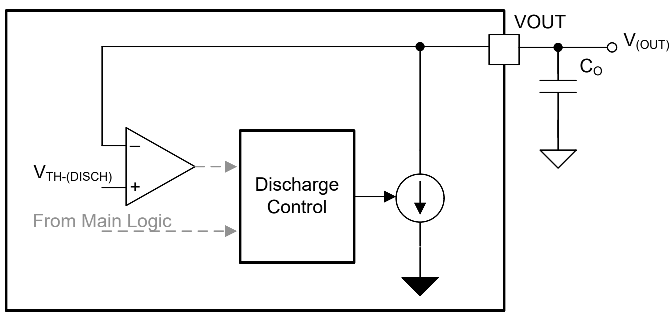

Figure 8-17. Functional Block Diagram Output Discharge

8.3.9 Peak Current Sensor

The integrated peak current sensor enables a low inductive sensing. The sensor is located in series with the main inductor and also monitors the peak inductor current under all operation modes (boost, buck-boost and buck) as well as for both current directions, that is, the bi-directional operation.

As the integrated sensor supports high bandwidth signals a differential mode filter adopted to the selected operating point is recommended for best performance. For most applications we recommend a resistor value for $R_{(DIFF1/2)}$ of 10Ω. Use the equation below to determine the filter capacitor:

$$C_{(DIFF)} = \frac{t_{on,min}}{2\pi \cdot \left(R_{(DIFF1)} + R_{(DIFF2)}\right) \cdot 10} \quad (13)$$

Set the differential filter to a 10th of the minimum on-time of Buck or Boost mode.

Current sense resistors consist a parasitic inductance based on geometry and the selected component vendors design. If the desired application requires high currents, reduce the impact of the external component parasitic by placing multiple sense resistors in parallel.

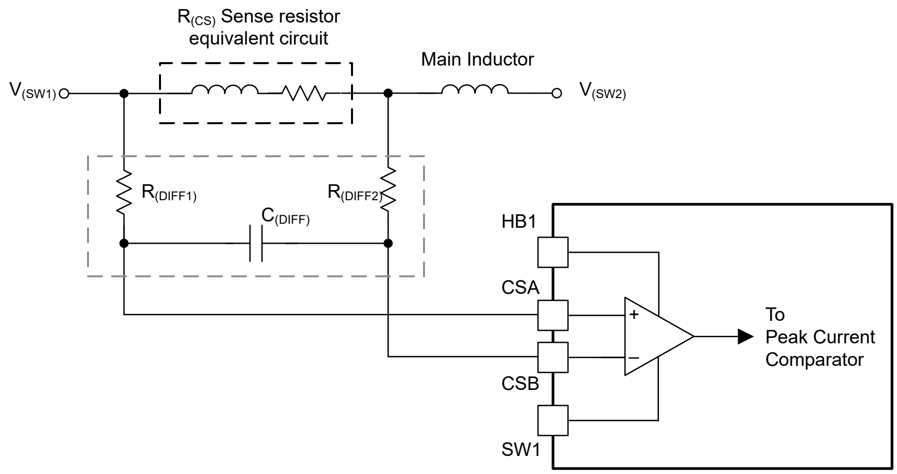

Figure 8-18. Simplified Schematic of the Peak Current Sensor

8.3.10 Short Circuit - Hiccup Protection

The LM251772-Q1 features a short circuit protection or over current protection. This protection uses cycle-by-cycle peak current sensor connected to the CSA and CSB-pin. There are two modes for this protection. In hiccup mode, the controller stops the converter operation after detecting cycle-by-cycle peak current longer as the hiccup mode on-time. The converter logic initiates a discharge of the soft-start capacitor and the output stays off until the hiccup mode off-time elapses. Afterward the logic exits the hiccup mode and re-start the output with a normal soft-start sequence where the soft-start capacitor is charged with the internal current source. If the short or overload condition persist the hiccup timer starts again after the soft-ramp finishes. If hiccup mode protection is not enabled, the device operates in cycle-by-cycle current limiting as long as the overload condition persists. The peak inductor current limit in steady state is calculated as shown in Equation 14

$$I_{L(PEAK,\ ILIMIT)} = \frac{50\mathrm{mV}}{R_{CS}} \tag{14}$$

8.3.11 Current Monitor/Limiter

8.3.11.1 Overview

The device features two high voltage current sensors. The first one maintains the peak current sensing between the CSA and CSB pins. The second current sensor inputs are connected to the ISNSP and ISNSN pins. This optional current sensing provides the capability to monitor (CDC-pin) and limit (ILIMCOMP-pin) either the input or the output current of the DC/DC converter.

If the optional current sense amplifier is not used, connect the ILIMCOMP pin to VCC2 to all current limiting/ monitoring functions off. The configuration gets latched at start-up of the converter. Do not do this dynamically during the operation of the device. If the current monitoring/limit block is not used for the target application and therefore disabled, do this before the device gets enabled through EN, EN_CONV or a power cycle.

Directly connect the ILIMCOMP to VCC2 or with a pullup resistor < 50kΩ.

Use the I2C register to select the following desired operation modes:

1. If the current sense amplifier operates in monitor configuration with IMON_LIMITER_EN is set to 0b0 by I2C interface. Both CDC and ILIMCOMP pins provide a current proportional to the differential sense voltage.
2. The current monitor block limiter operation is activated via MON_LIMITER_EN bit.
3. The negative current limit direction is selected by the EN_NEG_CL_LIMIT bit.
4. The internal DAC is the reference for the current limit threshold. The value for the DAC is set by the ILIM_THRESHOLD register.

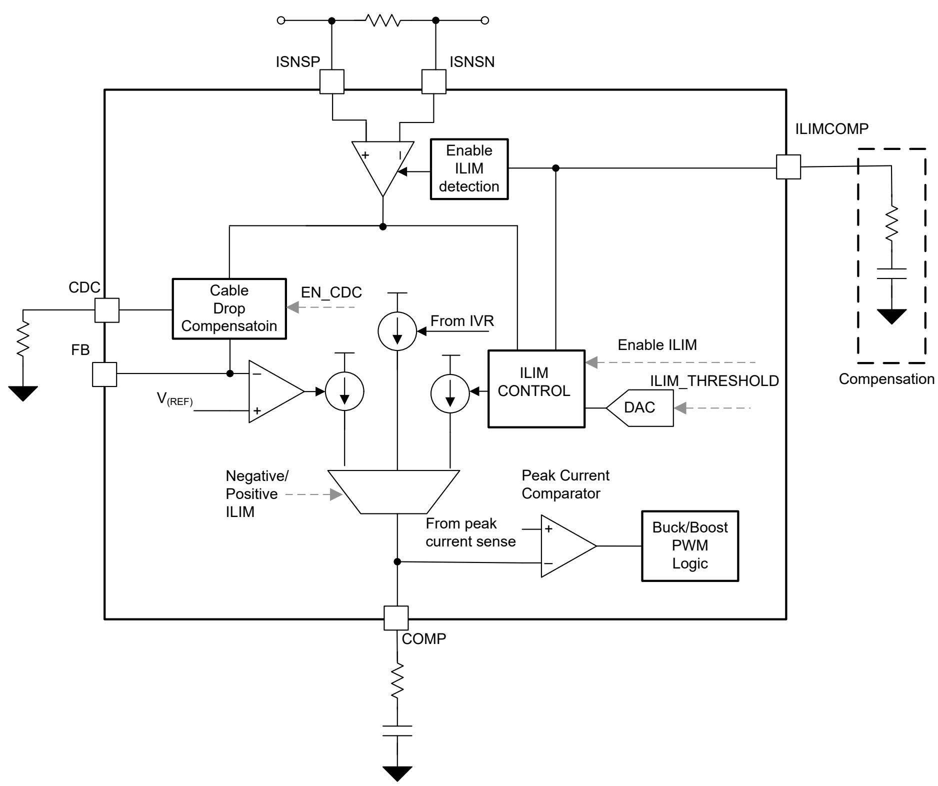

Figure 8-19. Current Monitor Functional Block Diagram

8.3.11.2 Output Current Limitation

The threshold for the current limit is programmed by the internal DAC. The bandwidth of the current limit control loop is optimized for different loads with a resistor and capacitor network on the ILIMCOMP pin. For resistive loads a simple integrator compensation is selected according the following equations:

$$C_{O2} = \frac{5}{2 \cdot \pi \cdot f_{bw} \cdot R_{(LOAD)}} \tag{15}$$

Where C_{O2} is the capacitance after the average current sense resistor $R_{(SNS)}$

f_{bw} is the bandwidth of the voltage loop compensation (see Voltage Regulation Loop)

$$C_{O1} = C_O - C_{O2} \tag{16}$$

Where C_O is the total output capacitance determined by the voltage loop calculation and the applications voltage ripple requirement.

Where C_{O1} is the capacitance before the average current sense resistor $R_{(SNS)}$

$$f_p = \frac{1}{2 \cdot \pi \cdot R_{(SNS)} \cdot C_{O2}} \tag{17}$$

$$f_{bwilim} = f_p \cdot 10^{-0.25} \tag{18}$$

$$C_{(ILIMCOMP)} = \frac{gm_{(ILIMCOMP)}}{2\pi \cdot f_{bwilim}} \tag{19}$$

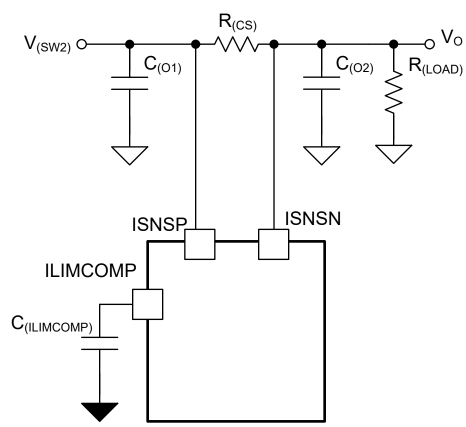

Figure 8-20. Simplified Schematic current limit components with resistive load

For an electronic load (CC-mode CR-mode) a type II compensation network is necessary in most cases. To adopt to the internal regulation loop and bandwidth of the used electronic load. Please refer to the Quick Start Calculator Tool for more detailed optimization.

The read-out register value of the "ILIM_THRESHOLD" control register is clamped for the lower and for the upper limit of the register range.

- The reg. readout value is clamped to the lowest clamp current (for example 500mA) if a register value below the value of clamp current been written in before.
- The reg. readout value is clamped to the highest clamp current if a register value above the highest value of clamp current has been written in before.

8.3.11.3 Output Current Monitor

The current through the sense resistor is monitored though the CDC pin simultaneously and has no impact to a configured current limit via the ILIMCOMP pin. If the limiter is disabled (IMON_LIMITER_EN = 0b0) both pins provide a proportional current to the differential voltage of ISNSP/N with. To calculate the sense voltage use the equation below.

$$V_{(CDC)} = \left(V_{(ISNSP)} - V_{(ISNSN)}\right) \times gm_{(CDC)} \times R_{(CDC)} \tag{20}$$

$$V_{(\mathrm{ILIMCOMP})} = \left(V_{(ISNSP)} - V_{(ISNSN)}\right) \times gm_{(\mathrm{ILIMCOMP})} \times R_{(\mathrm{ILIMCOMP})} \tag{21}$$

8.3.12 Oscillator Frequency Selection

The LM251772-Q1 has a low tolerance internal trimmed oscillator.

Do not operate in these with the RT pin "open" or short "short" as the frequencies are not accurate. With the RT pin left open, the oscillator frequency is at the minimum possible boundary. With the RT pin grounded, the switching frequency is at the maximum possible boundary.

The oscillator frequency is programmed up or down by connecting a resistor from the RT pin to ground. To calculate the RT resistor for a specific oscillator frequency, use Equation 22.

$$R_{(RT)} = \frac{1}{32 \cdot 10^{-12} \cdot f_{sw}} \tag{22}$$

The RT pin is regulated to 0.75V by an internal voltage source when the device is in active mode. Therefore, switching frequency to be dynamically changed during operation by changing the current flowing through the resistor is possible. Figure 8-21 and Figure 8-22 show two examples for changing the frequency by the switching the resistor value or applying an external voltage source through a resistor. Connecting any additional capacitance directly to the RT pin is not recommended.

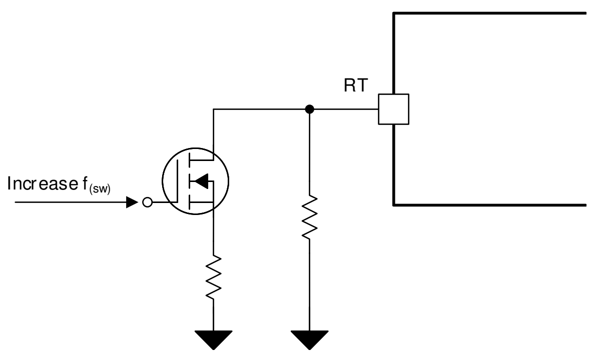

Figure 8-21. Frequency Hopping Example

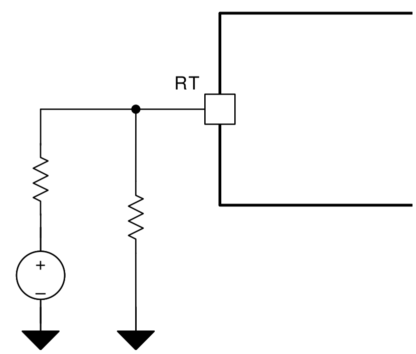

Figure 8-22. Dynamic Frequency Changing Example

8.3.13 Frequency Synchronization

The device features an internal phase looked loop (PLL), which is designed to transition the switching frequency seamlessly between the frequency set by the RT pin and the external frequency synchronization signal. If no external frequency is provided, the RT pin sets the center frequency of the synchronization range. The external synchronization signal changes the switching frequency by ±50%. To create low quiescent current, the input buffer of the SYNC pin is disabled if no valid sync frequency, that is a frequency signal outside the recommended synchronization range is applied.

The $f_{(SW)}$ synchronization stops if the device enters power save mode or µSleep operation, if enabled. Once the converter enters the PWM operation again, the device re-syncs to a pin signal. The synchronization timings are given in Figure 8-24

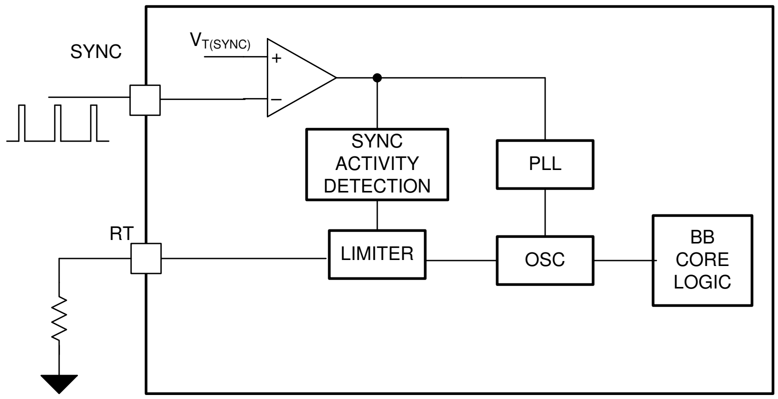

Figure 8-23. Main Oscillator Functional Block Diagram

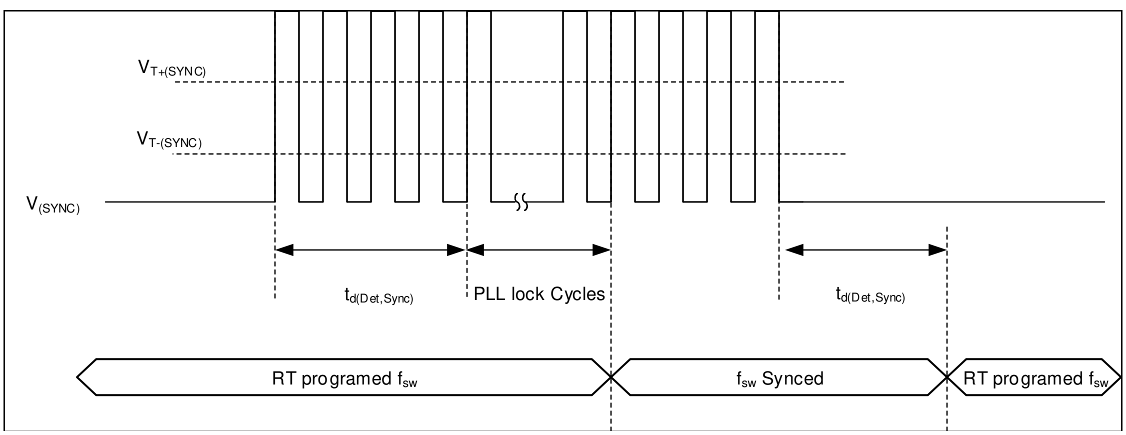

Figure 8-24. Timing Diagram SYNC Function

The SYNC pin function is programmed through I^2C or configured via R2D interface:

- As input triggering on the rising edge
- As input triggering on the falling edge (180deg phase shift)
- As an output of the main oscillator clock

8.3.14 Output Voltage Tracking

There are two kinds of output voltage tracking features integrated in the device.

- Analog voltage tracking function through the SS/ATRK pin
- Digital voltage tracking function through the DTRK pin

8.3.14.1 Analog Voltage Tracking

For the analog output voltage tracking, a voltage applied to the SS/ATRK pin overwrites the reference voltage for the output regulation loop. Although possible, do not apply this voltage before the soft start is finished because the soft-start ramp time and, therefore, the input current during the start-up is changed.

As the internal error amplifier is designed to use the lowest reference input voltage, the applied voltage on the SS/ATRK pin is only effective for voltages lower than the V_{ref} of the feedback pin. Hence, the maximum voltage for the output is determined by the resistor network on the FB pin.

If the analog voltage tracking is used to start-up the converter voltage a change at the mode pin from high to low or low to high signals the internal logic that the soft-start is completed.

8.3.14.2 Digital Voltage Tracking

The DTRK input of the LM251772-Q1 directly modulates the internal reference voltage. This function activates if the voltage on the DTRK pin is higher than the rising threshold of $V_{T(DTRK)}$ and a PWM signal in the recommended frequency is applied to the pin.

The voltage tracking implementation does not allow that target output voltage during digital tracking exceeds the nominal reference voltage selected with the FB resistor divider. The applied PWM signal reduces the internal reference voltage in relation with the duty cycle on the DTRK pin. A small duty cycle means less output voltage and a high duty cycle of the PWM input represents a high output voltage. For example, a duty cycle of 30% causes a output voltage of 30% of the selected voltage by the FB divider resistors.

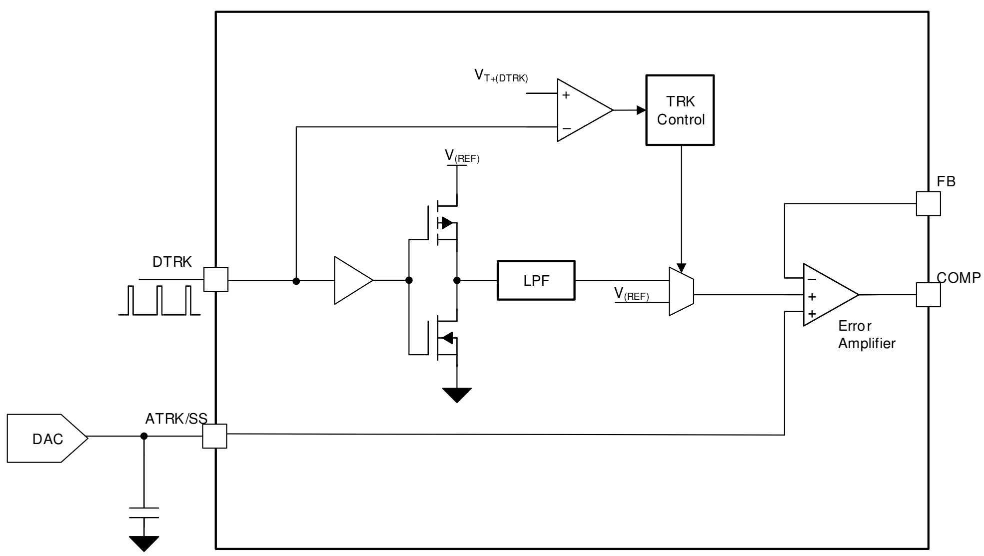

Figure 8-25. Output Voltage Tracking Functional Block Diagram

8.3.15 Slope Compensation

The LM251772-Q1 provides slope compensation for stable operation and the best transient performance over a wide operating range.

First a correction factor needs to be calculated from Equation 23

$$m_{SC} = \frac{R_{CS}}{f_{SW} \times L_{eff}} \times 625 \quad (23)$$

- Where the R_{CS} is the selected peak current sense resistor
- L_{eff} is the effective (de-rated), inductance of the inductor at the selected peak current
- $f_{SW}$is the selected switching frequency
- m_{SC}slope compensation correction factor

If the used inductor has no inductance de-rating disabling the inductor de-rating with the SEL_INDUC_DERATE in MFR_SPECIFIC_D7 Register Field is possible.

If the used inductor has no inductance de-rating (meaning: m_{sc} × 1.2 or m_{sc} × 1.3). By doing so there is a compromise on the slope compensation and the PSM entry threshold.

Select the slope compensation based on the calculated correction factor through I^2C.

8.3.16 Configurable Soft Start

The soft-start feature allows the regulator to gradually reach the steady-state operating point, thus reducing start-up stresses and surges.

The LM251772-Q1 features an adjustable soft start that determines the charging time of the output. The soft-start feature limits inrush current as a result of high output capacitance to avoid an over-current condition.

At the beginning of the soft-start sequence, the SS voltage is 0V. If the SS pin voltage is below the feedback reference voltage, V_{REF}, the soft-start pin controls the regulated FB voltage and the internal soft-start current source gradually increases the voltage on an external soft-start capacitor connected to the SS pin, resulting in a gradual rise of the output voltage and FB pin. Once the voltage on the SS exceeds the internal reference voltage, the soft-start interval is complete and the error amplifier is referenced to $V_{(REF)}$.

The soft-start time ($t_{(ss)}$) is given by:

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{Ref}} \quad (24)$$

The soft-start capacitor is internally discharged when the converter is disabled because of the following:

- EN/UVLO falling below the operating threshold
- VCC2 falling below the VCC2 under-voltage threshold
- The device is in hiccup mode current limiting.
- The device is in thermal shutdown.
- The bootstrap voltage is below the bootstrap under-voltage threshold

8.3.17 Drive Pin

The device features a high voltage drive pin (DRV1) to support an input or output disconnect FET. There is the option to use the pin a driver for a charge pump output. For example as a reverse polarity protection using a external n-channel FET. The supply for this pin is selected by R2D and I2C configurations.

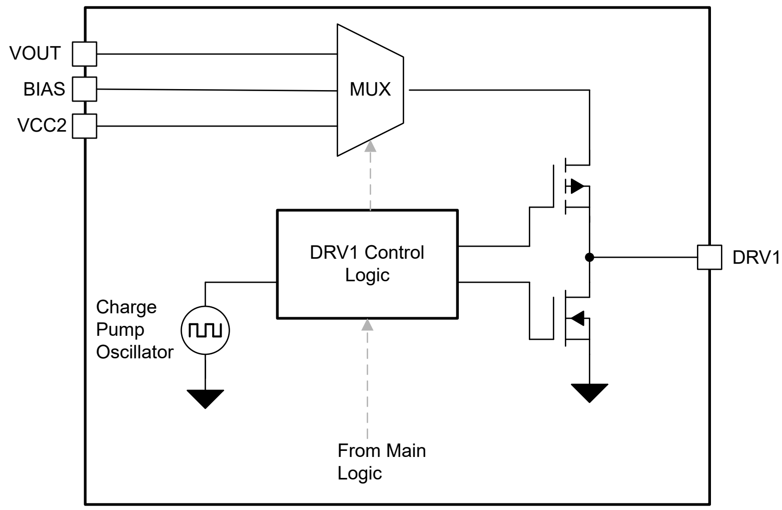

Figure 8-26. Functional Block Diagram - DRV pin

The following configurations are possible with to support with the DRV1 pin:

1. Open drain output.
2. High Voltage Push-pull supplied by VOUT
3. High Voltage Push-pull supplied by VBIAS
4. CP drive pin supplied by the VCC2

The sequencing of the DRV pin is depending on the setting an given by the register MFR_SPECIFIC_D8 Register Field Descriptions.

8.3.18 Dual Random Spread Spectrum – DRSS

The device provides a digital spread spectrum, which reduces the EMI of the power supply over a wide frequency range. This function is selected by the Register MFR_SPECIFIC_D0 Register Field Descriptions. When the spread spectrum is enabled, the internal modulator dithers the internal clock. When an external synchronization clock is applied to the SYNC pin, the internal spread spectrum is disabled. DRSS combines a low frequency triangular modulation profile with a high frequency random modulation profile. The low frequency triangular modulation improves performance in lower radio frequency bands (for example, AM band), while the high frequency random modulation improves performance in higher radio frequency bands (for example, FM band). In addition, the frequency of the triangular modulation is further modulated randomly to reduce the likelihood of any audible tones. To minimize output voltage ripple caused by spread spectrum, duty cycle is modified on a cycle-by-cycle basis to maintain a nearly constant duty cycle when dithering is enabled.

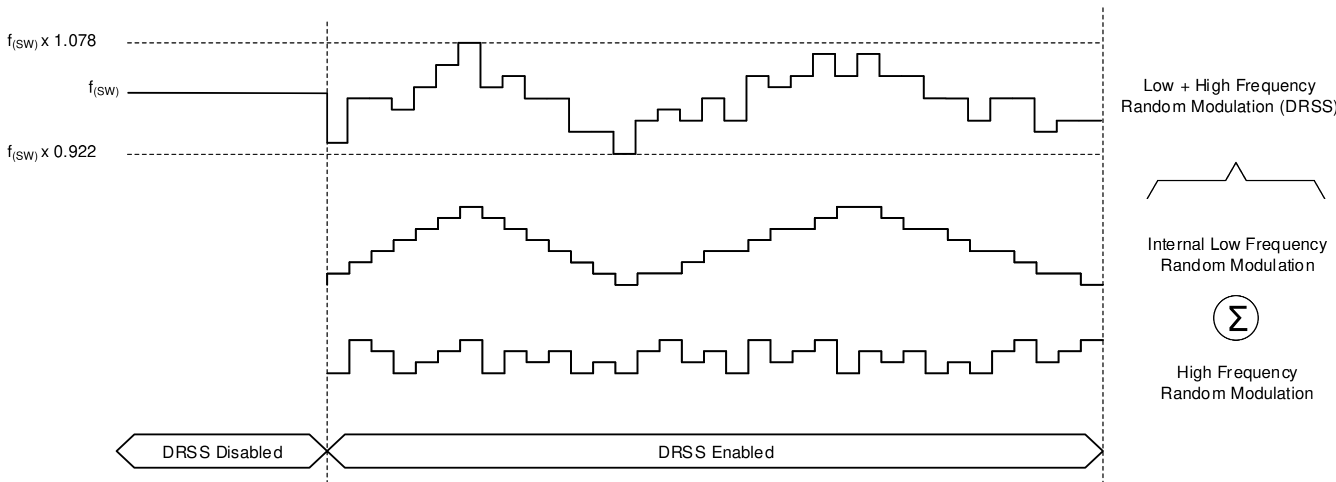

Figure 8-27. Dual Random Spread Spectrum

8.3.19 Gate Driver

The LM251772-Q1 features four internal logic-level nMOS gate drivers. The drivers maintain the high frequency switching of both half bridges needed for a buck-boost operation. If the device is in boost or buck mode, the other half bridge high-side switch needs to be permanent on. The internal gate drivers support this by sharing the current from the other half bridge, which is switching. Therefore the device achieves a minimum quiescent current, as no internal char pump is needed. Due to the high drive current capability, the LM251772-Q1 supports a wide range of external power FETs as well as a parallel operation of them.

The LO and HO outputs are protected with a shoot-through protection, which prevents both outputs to be turned on at the same time. If the PWM modulation logic of the buck-boost turns the LOx pin off, the HOx pin is not turned on until the following are true:

1. A minimum internal transition time ($t_{t(dead)}$) is reached.
2. The voltage on the LOx pin drops below the detection threshold $V_{TH(GATEOUT)}$.

This behavior is similar when HOx turns off and LOx turns on.

The high-side supply voltage for the gate driver are monitored by an additional bootstrap UVLO comparator. This comparator monitors the differential voltage between SWx and HBx. If the voltage drops below the threshold the buck-boost converter operation turns off. The device restarts automatically once the positive going threshold is reached with the soft-start scheme.

Additionally, the LM251772-Q1 monitors the upper voltage between SWx and HBx. If this voltage exceeds the threshold voltage of the clamping circuit, the LM251772-Q1 activates a internal current source to pull the voltage down.

The dead-time values are selected by SEL_SCALE_DT, SEL_MIN_DEADTIME_GDRV in the register MFR_SPECIFIC_D6 Register Field Descriptions.

Additionally there is a optional frequency dependency of the transition (dead) -time between high and low side. This feature enables the device to optimize the performance for usual differences of the silicon MOSFET Q_g in high power applications with low switching frequencies and lower power application with higher switching frequencies. When this option is enabled, the dead-time is shorter when the switching frequency is set higher. The frequency dependency is enabled or disabled with the register EN_CONST_TDEAD in register MFR_SPECIFIC_D6 Register Field Descriptions.

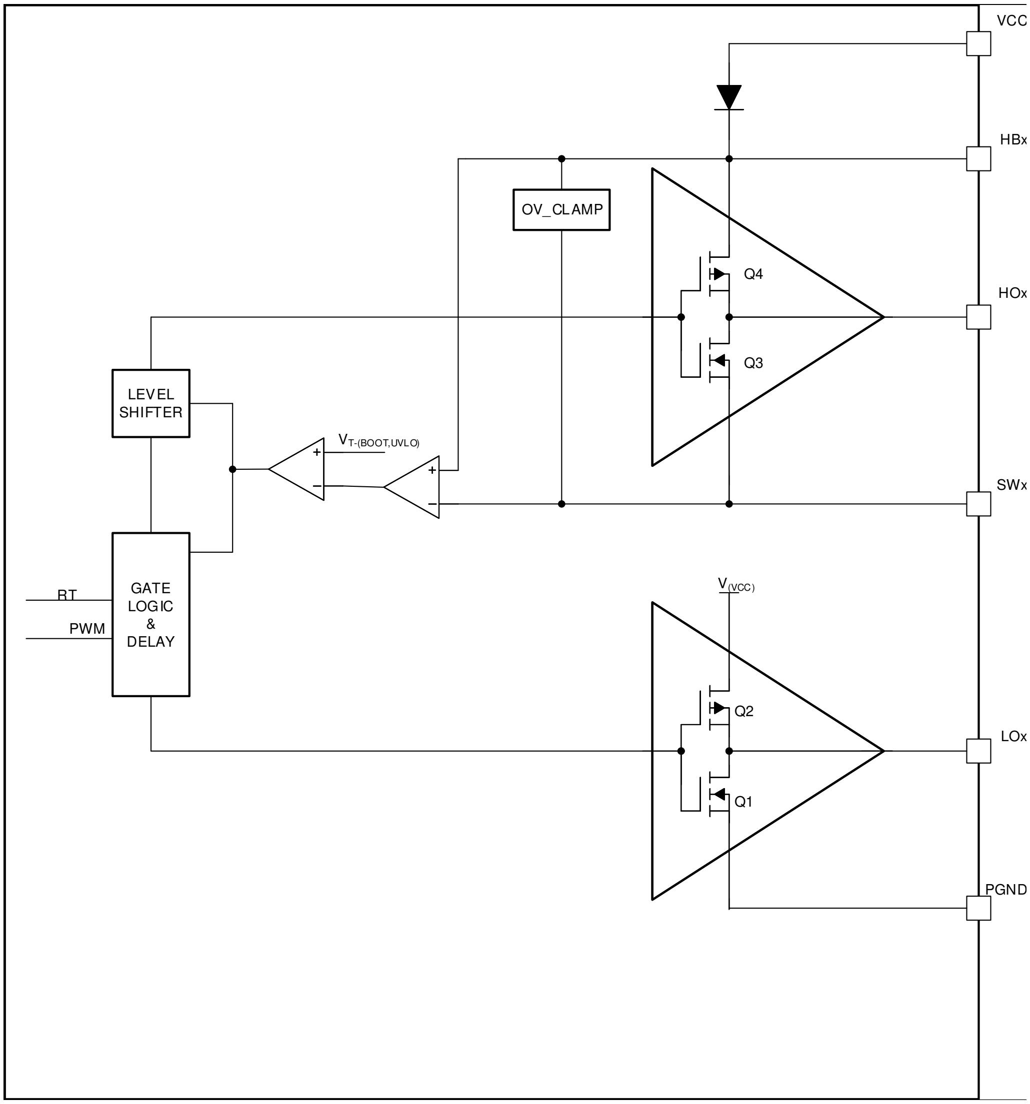

Figure 8-28. Functional Block Diagram Gate Driver

8.3.20 Cable Drop Compensation (CDC)

The cable drop compensation feature helps to keep the output voltage at the nominal value over a wide range of load current without the need for additional remote sensing. The cable drop compensation measures the current and offsets the output voltage proportionally to the measured current.

If enabled, the gm-stage of the current monitor sensor (ISNSP/N) sends a proportional current to the CDC pin. The voltage on the CDC pin is applied as a offset to the nominal output voltage. Select the resistor value on the CDC-pin to not to exceed 1V.See the Equation below:

$$V_{(CDC)} = \left(V_{(ISNSP)} - V_{(ISNSN)}\right) \times gm_{(CDC)} \times R_{(CDC)} \tag{25}$$

To achieve an accurate operation for the desired range cable drop compensation the gain of the CDC offset is programmable via the CDC_GAIN register bits.

The CDC function operates equally with the external Feedback divider. Use a 100kΩ feedback divider top resistance. If a different resistance is used, the gain of the CDC is multiplied by Rtop/100kΩ.

The figure below shows the control curve of the CDC feature.

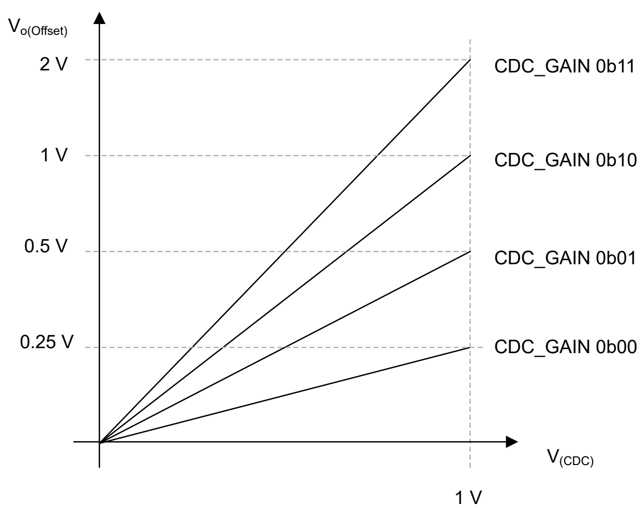

Figure 8-29. Vo Offset vs CDC voltage

8.3.21 CFG-pin and R2D Interface

The resistor value on the CFG pins is read and latched during the power-up sequence of the device. The device ignores the changes to the CFG selection until the voltage on the nRST pin is toggled or VCC2 voltage drops below the $V_{VCC2T\text{-}(UVLO)}$ threshold. The following table shows the possible device configurations versus the different resistor values on the CFG pins.

Table 8-4. ADDR Pin (R2D-CH1) Configuration Overview

#	$R_{(CFG)}$ / kΩ	I2C/ADDR	Slope Compensation ($m_{(SC)}$)
1	GND	Address 0x6A	Default register setting of
2	VCC2	Address 0x6B	Default register setting of

Table 8-5. CFG2 Pin (R2D-CH2) Configuration Overview

<table>
<tr><th>#</th><th>R_(CFG) / kΩ</th><th>EN_SYNC_OUT</th><th>SYNC_IN_FALLING</th><th>FORCE_BIAS</th><th>UNUSED</th></tr>
<tr><td>1</td><td>0</td><td>DISABLED</td><td rowspan="2">DISABLED</td><td rowspan="4">DISABLED</td><td rowspan="16">RESERVED</td></tr>
<tr><td>2</td><td>0.511</td><td>ENABLED</td></tr>
<tr><td>3</td><td>1.15</td><td>DISABLED</td><td rowspan="2">ENABLED</td></tr>
<tr><td>4</td><td>1.9</td><td>ENABLED</td></tr>
<tr><td>5</td><td>2.7</td><td>DISABLED</td><td rowspan="2">DISABLED</td><td rowspan="4">ENABLED</td></tr>
<tr><td>6</td><td>3.8</td><td>ENABLED</td></tr>
<tr><td>7</td><td>5.1</td><td>DISABLED</td><td rowspan="2">ENABLED</td></tr>
<tr><td>8</td><td>6.5</td><td>ENABLED</td></tr>
<tr><td>9</td><td>8.3</td><td>DISABLED</td><td rowspan="2">DISABLED</td><td rowspan="4">DISABLED</td></tr>
<tr><td>10</td><td>10.5</td><td>ENABLED</td></tr>
<tr><td>11</td><td>13.3</td><td>DISABLED</td><td rowspan="2">ENABLED</td></tr>
<tr><td>12</td><td>16.2</td><td>ENABLED</td></tr>
<tr><td>13</td><td>20.5</td><td>DISABLED</td><td rowspan="2">DISABLED</td><td rowspan="4">ENABLED</td></tr>
<tr><td>14</td><td>24.9</td><td>ENABLED</td></tr>
<tr><td>15</td><td>30.1</td><td>DISABLED</td><td rowspan="2">ENABLED</td></tr>
<tr><td>16</td><td>36.5</td><td>ENABLED</td></tr>
</table>

8.3.22 Advanced Monitoring Features

8.3.22.1 Overview

The device features a status register in which represents the current operation status of the device logic. Use the I^{2}C interface to get the current status flags.

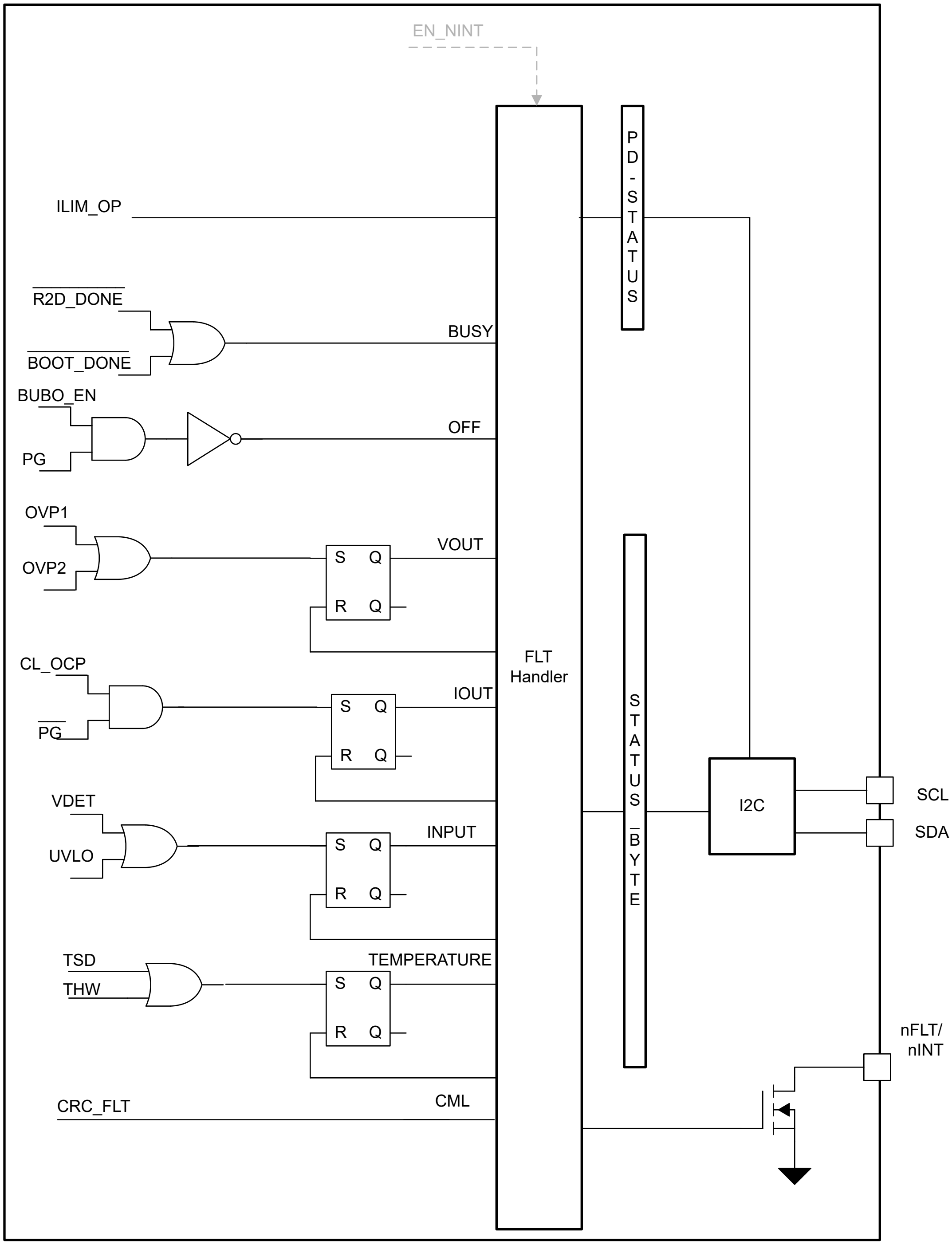

Figure 8-30. Functional Block Diagram Fault Handler

8.3.22.2 BUSY

If the device register field is busy or in use by another instance this bit is high. Writing via the I^2C interface is not recommended during busy flag high. This bit is only observed after the device start-up

8.3.22.3 OFF

Is high if the device is not providing a high enough output voltage ($V_{(VOUT)} < V_{T+(PG)}$). This bit is also high if the converter is turned off by system input. This bit is only observed after the device start-up

8.3.22.4 VOUT

Output voltage over voltage threshold (OVP1, OVP2) is exceeded. This error gets latched until the register is cleared or a power cycle happens

8.3.22.5 IOUT

Over current protection, this is going high when the inductor peak current limit is reached. This error gets latched until the register is cleared or a power cycle happens

8.3.22.6 INPUT

The input voltage detection (VDET) or the UVLO resistor senses voltage is blow the falling threshold. This error gets latched until the register is cleared or a power cycle happens

8.3.22.7 TEMPERATURE

The device has entered TSD state or the programmable thermal warning threshold is reached. This error gets latched until the register is cleared or a power cycle happens

8.3.22.8 CML

The device detects an internal logic fault, that is, the NVM memory check-sum has detected data retention event.

8.3.22.9 OTHER

unused

8.3.22.10 ILIM_OP

This signal is enabled together with the average current limit. If the current limiter is disabled the signal is low. If the programmed (via I^2C) current limit threshold is reached the signal goes high. The PD-STATUS byte is instantaneously changing with the ILIM_OP signal. The input signal gets de-glitch in the analog domain.

8.3.22.11 nFLT/nINT Pin Output

If the bit EN_NINT (see MFR_SPECIFIC_D0 Register Field Descriptions) is set to 0b0 the nFLT/nINT pin indicates all faults that are reported to the STATUS byte.

After a restart of the converter operation or in case the failure mode disappears the nFLT pin goes back to HighZ. The input signals to the STATUS-BYTE and therefore the nFLT/nINT pin are de-glitched. Because of this the maximum reaction time of the FLT pin is given by $t_{d(nFLT\text{-}PIN)}$

Do not change the EN_NINT dynamically during operation, but during the CONV_OFF state.

In case the EN_NINT = 0b1 the nFLT/nINT pin acts as interrupt pin. A change of the instantaneous signal to the STATUS_BYTE as well as the inputs to the USB_PD_STATUS_0 toggles the pin.

8.3.22.12 Status Byte

Use the following methods to clear a fault:

1. Perform an I^2C write to the CLEAR_FAULTS byte.
2. Perform an I^2C read to the CLEAR_FAULTS byte.
3. Perform an I^2C write to the STATUS_BYTE where a fault is indicated with a '1' and clear this bit by setting the bit to '1'.With this implementation a previously stored STATUS_BYTE clears the faults for diagnosis.

8.3.23 Protection Features

8.3.23.1 Thermal Shutdown (TSD)

To avoid the case of a thermal damage of the device the temperature of the die is monitored. The device stops operation once the sensed temperature rises over the thermal shutdown threshold. After the temperature drops below the thermal shutdown hysteresis the TSD signal goes back to normal and the converter returns to normal operation according to the main FSM definition.

8.3.23.2 Over Current Protection

The device features a hiccup mode short circuit protection to avoid excessive power dissipation in the die or at the fault of the application in the System. The CL_OP triggers if the peak current sensing voltage between CSA-pin and CSB-pin is exceeded.

If enabled the protection stops the converter operating and re-start the converter in case a short is event is detected.

The bit HICCUP_EN in the NVM register enables the OCP.

8.3.23.3 Output Over Voltage Protection 1 (OVP1)

This overvoltage protection monitors the voltage of the FB-pin and the internal feedback.

As this threshold is referenced to the programmed $V_{(REF)}$ the OVP1 is still working if one of the tracking features (for example, DTRK or ATRK) has changed the V_o target value.

The converter maintains operation even the OVP1 threshold triggers.

The OVP1 is disabled during µSleep to avoid additional leakage current. The OVP1 signal gets masked that no fault is indicated from this signal during the µSleep operation.

This protection is disabled during the soft-start procedure and if the internal feedback is used instead of the external FB.

8.3.23.4 Output Over Voltage Protection 2 (OVP2)

This feature targets to avoid damage to the device in case the external feedback pin or compensation pin is not working properly (for example in case of a component or pin short)

The over voltage protection is realized by the converter core and reference system. The absolute output voltage is monitored and when the OVP2 function is triggered the converter logic takes an appropriate measure (for example the emergency skip mode) to avoid a further increase of the output voltage.

If the output voltage threshold $V_{T+(OVP2)}$ is reach on the VOUT-pin the buck-boost core logic disables the converter power stage and enters a high impedance state at the switch nodes. If the output voltage falls back under this threshold the converter operation is resumed

To accommodate a wide operating range, the OVP2 threshold is programmable by the V_OVP2 register field.

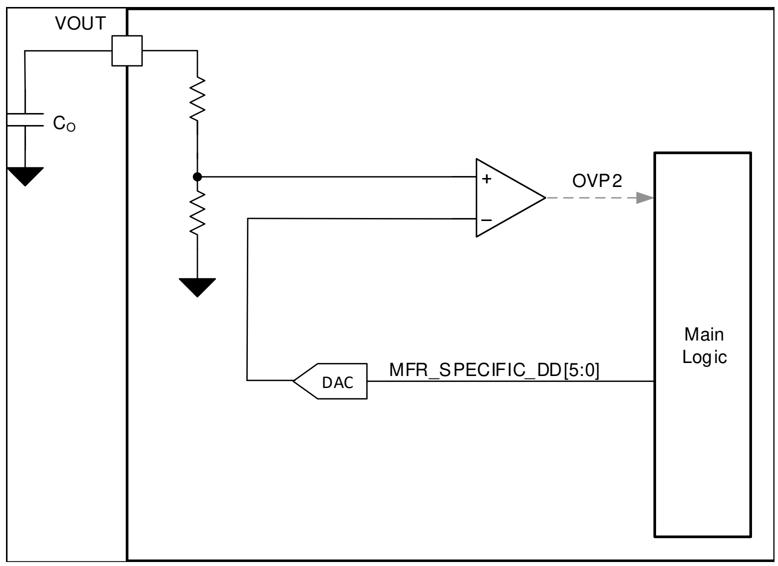

Figure 8-31. Functional Block Diagram OVP2

8.3.23.5 Input Voltage Protection (IVP)

The input over voltage protection is realized by the converter core modulation scheme. The IVP targets to avoid damage to the device in case the current flows from the output to the input and the input source is not capable to sink current. If the converter forced PWM mode is active the inductor current is able to go negative until to the negative peak current limit. Once the input voltage threshold $V_{T+(IVP)}$ is reach on the VIN-pin the protection disables the forced PWM mode and only allows current to flow from VIN to VOUT. After the input voltage drops under the input voltage protection threshold, the logic allows to activate the fPWM mode again.

The threshold for the $V_{T+(IVP)}$ is programmable via the V_IVP register field. The IVP is enabled or disabled through the EN_IVP bit.

8.3.23.6 Input Voltage Regulation (IVR)

The input over voltage regulation (IVR) regulates the input voltage. The inductor current is limited with the positive and negative peak current limit or the optional average current limit. The target voltage is programmed by IVP_VOLTAGE Register Field Descriptions. The IVR function is enabled once both EN_IVP and EN_IVR set to 0b1. The fPWM need to be enabled to allow the reverse current to charge the input. If the MODE pin is pulled low the IVR operation is paused until the fPWM is enabled again.

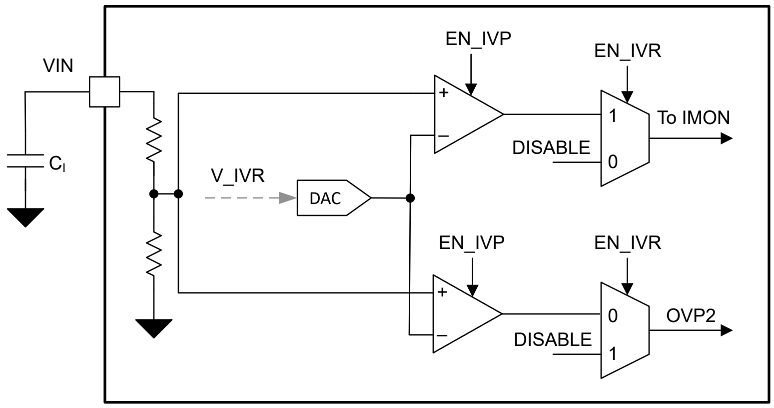

Figure 8-32. Functional Block Diagram IVP/IVR

8.3.23.7 Power Good

The device features a power good (PG) detection. The internal PG signal is used for the monitoring function.

The power good information is available once the soft-start ramp is finished.

8.3.23.8 Boot-Strap Under Voltage Protection

The high side supply voltage for the gate driver is monitored by an internal bootstrap UVLO comparator. This comparator monitors the differential voltage between SWx and HBx. This protection supports the two modes in the following manner.

1. If the measured voltage drops below $V_{TH\text{-}(BST\_UV)}$ in fPWM mode the converter stops operation after a fixed amount of switching cycles.
2. In PSM - ACM buck-boost operation, the BOOT_UV triggers switching the converter to re-fresh the boot strap voltage. If the initiated switching does not bring up the BOOT_UV after the fixed amount of re-fresh cycles the BOOT_UV protection deactivates the converter operation.

8.3.23.9 Boot-strap Over Voltage Clamp

To protect the ext. FET gate and the internal gate drive circuit the gate driver features an over voltage clamp. If the voltage goes above $V_{TH(BST\_OV)}$ the over-voltage clamp circuit sinks a current from HBx to SWx as long as the voltage is above the threshold.

8.3.23.10 CRC - CHECK

To enable data integrity of the NVM the device features a CRC- algorithm to generate a check-sum for the data stored in the device NVM.

The check-sum gets generated and stored to the separate NVM register automatically with the production programming process.

After the NVM boot phase the CRC algorithm compares the check-sum of the loaded registers with the check-sum stored in the NVM register generated during the production tests. If the two values are not equal the device is not allowed to exit the CONV_OFF state.

8.4 Device Functional Modes

8.4.1 Overview

The device contains a digital logic core that controls the functional behavior.

8.4.2 Logic State Description

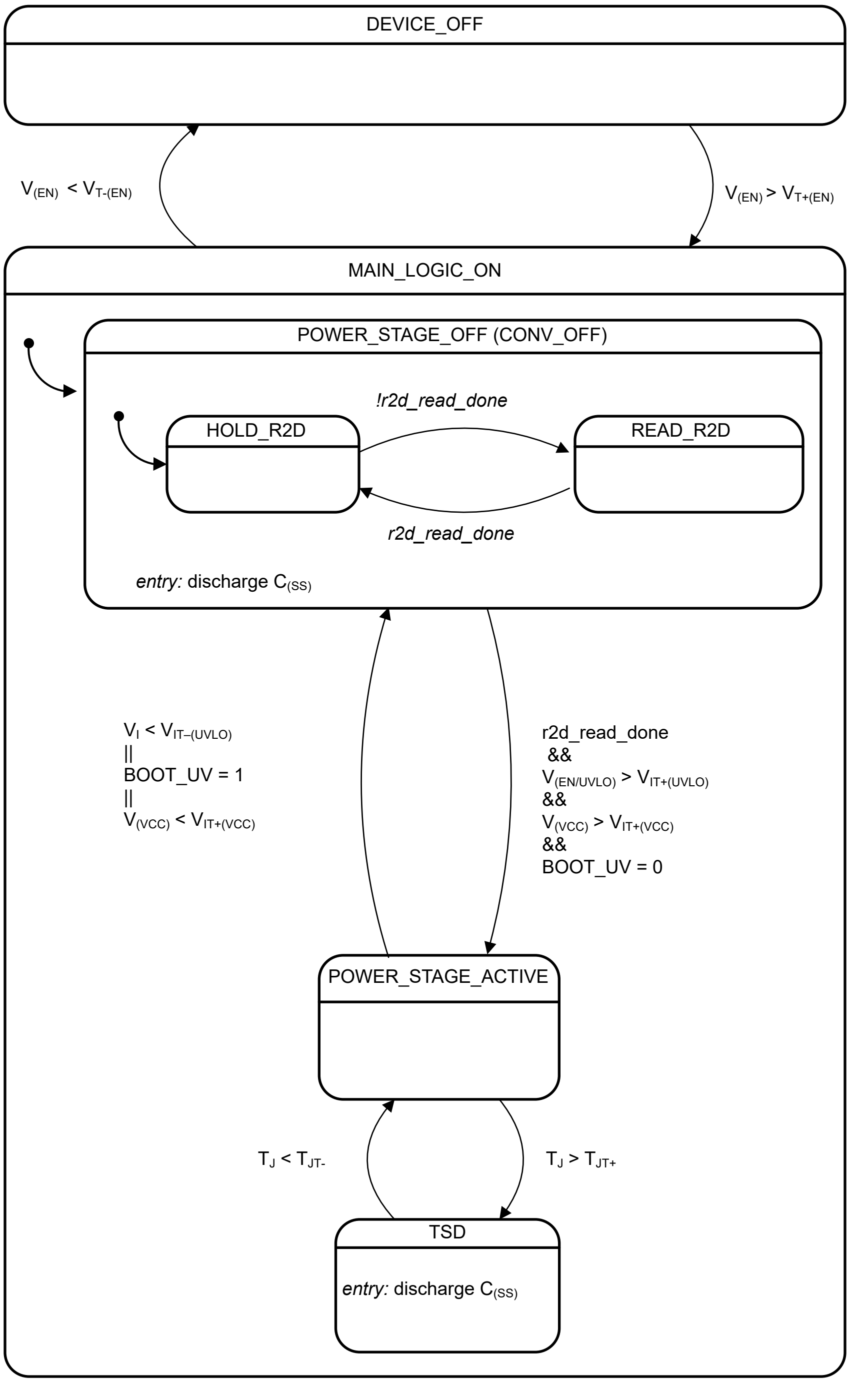

Figure 8-33. State Diagram

8.5 Programming

8.5.1 I²C Bus Operation

The I ² C bus is a communications link between a controller and a series of target devices. The link is established using a two-wired bus consisting of a serial clock signal (SCL) and a serial data signal (SDA). The serial clock is sourced from the controller in all cases where the serial data line is bi-directional for data communication between the controller and the target terminals. Each device has an open-drain output to transmit data on the serial data line (SDA). Place an external pullup resistor on the serial data line to pull the drain output high during data transmission. The device hosts a target I ² C that supports standard-mode, fast-mode and fast-mode plus operation with data rates up to 100kbit/s, 400kbit/s and 1000kbit/s respectively and auto-increment addressing compatible to I ² C standard 3.0.

The 7 bit target address of this device is 0x6A if the ADDR/SLOPE pin is pulled to GND and 0x6B if the pin is connected to VCC2

Data transmission is initiated with a start bit from the controller as shown in the figure below . The start condition is recognized when the SDA line transitions from high to low during the high portion of the SCL signal. Upon reception of a start bit, the device receives serial data on the SDA input and check for valid address and control information. If the target address bits are set for the device, then the device issues an acknowledge pulse and prepares the receive of register address and data. Data transmission is completed by either the reception of a stop condition or the reception of the data word sent to the device. A stop condition is recognized as a low to high transition of the SDA input during the high portion of the SCL signal. All other transitions of the SDA line targeted to occur during the low portion of the SCL signal for a valid communication. An acknowledge is issued after the reception of valid address, sub-address and data words. The I ² C interfaces auto-sequence through register addresses, to enable sending multiple data words for a given I ² C transmission.

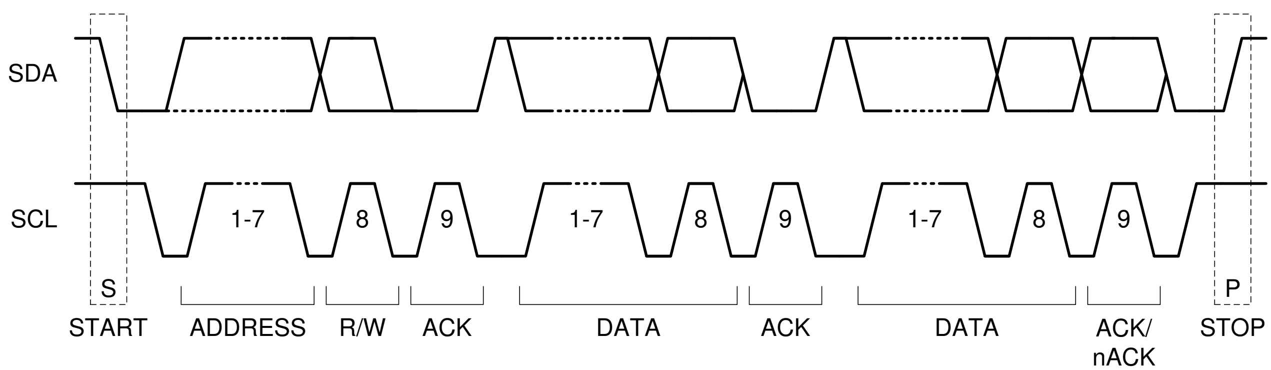

Figure 8-34. I ² C START / STOP / ACKNOWLEDGE Protocol

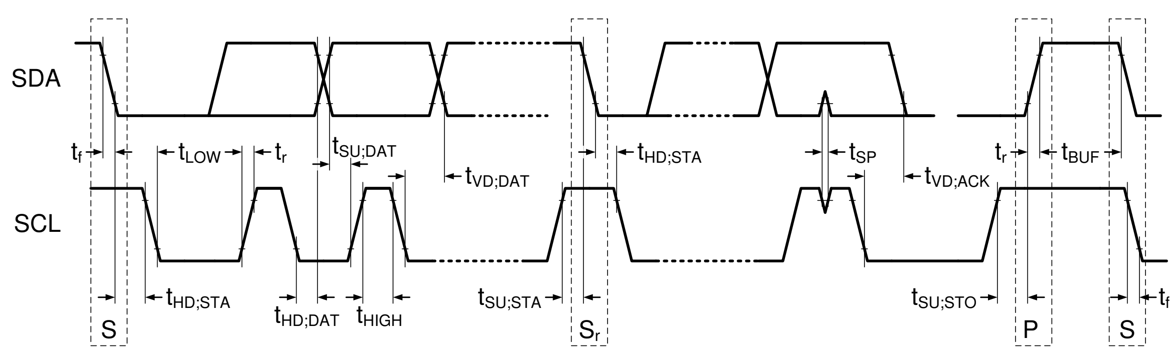

Figure 8-35. I ² C Data Transmission Timing

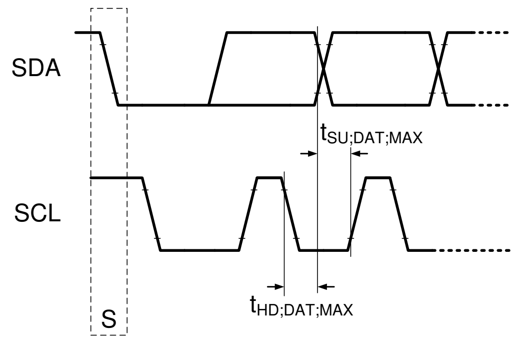

Figure 8-36. I 2 C Data Transmission Timing for maximum rise/fall times.

8.5.2 Clock Stretching

Clock stretching is not supported. If the device is addressed while busy and not able to process the received data, the transaction is not acknowledged. The previous described scenario is possible, if the controller initiates an I^2C transaction while the device is in BOOT state.

8.5.3 Data Transfer Formats

The device supports four different read/write operations:

- Single read from a defined register address.
- Single write to a defined register address.
- Sequential read starting from a defined register address
- Sequential write starting from a defined register address

8.5.4 Single READ From a Defined Register Address

Single READ From a Defined Register Address shows the format of a single read from a defined register address. First, the controller issues a start condition followed by a seven-bit I^2C address. Next, the controller writes a zero to signify that the controller is conducting a write operation. Upon receiving an acknowledge from the target the controller sends the eight-bit register address across the bus. Following a second acknowledge the device sets the internal I^2C register number to the defined value. Then the controller issues a repeat start condition and the seven-bit I^2C address followed by a one to signify that the controller is conducting a read operation. Upon receiving a third acknowledge, the controller releases the bus to the device. The device then returns the eight-bit data value from the register on the bus. The controller does not acknowledge (nACK) and issues a stop condition. This action concludes the register read.

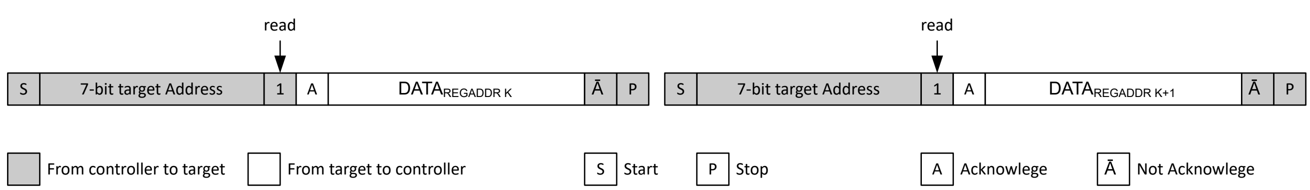

Figure 8-37. Single READ From a Defined Register Address

8.5.5 Sequential READ Starting from a Defined Register Address

A sequential read operation is an extension of the single read protocol and shown in Sequential READ starting from a defined register address. The controller acknowledges the reception of a data byte, the device auto increments the register address and returns the data from the next register. The data transfer is stopped by the controller not acknowledging the last data byte and sending a stop condition.

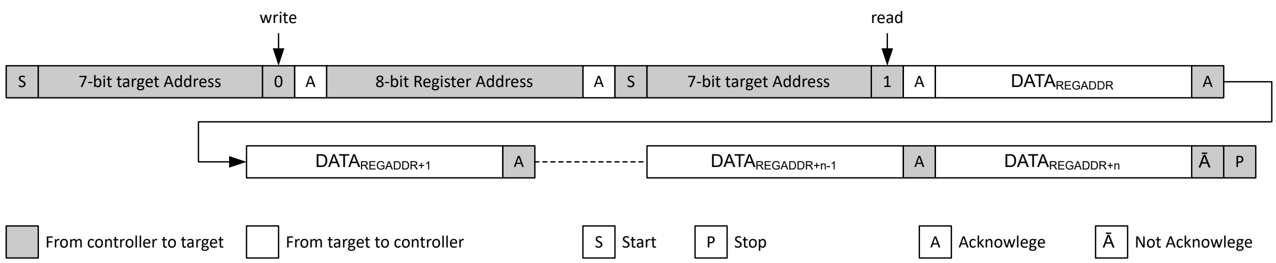

Figure 8-38. Sequential READ starting from a defined register address

8.5.6 Single WRITE to a Defined Register Address

Single WRITE to Defined Register Address shows the format of a single write to a defined register address. First, the controller issues a start condition followed by a seven-bit I ^{2} C address. Next, the controller writes a zero to signify that the controller is trying to conduct a write operation. Upon receiving an acknowledge from the target, the controller sends the eight-bit register address across the bus. Following a second acknowledge the device sets the I ^{2} C register address to the defined value and the controller writes the eight-bit data value. Upon receiving a third acknowledge the device auto increments the I ^{2} C register address by one and the controller issues a stop condition. This action concludes the register write.

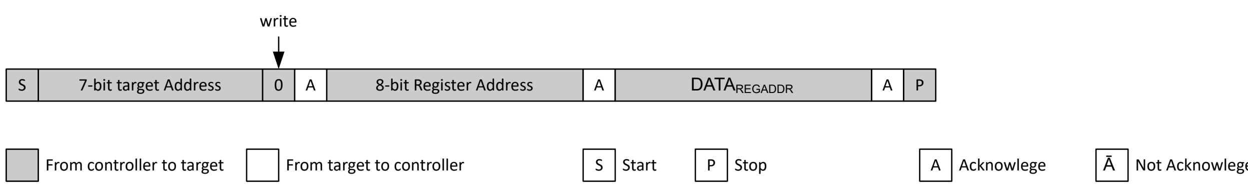

Figure 8-39. Single WRITE to Defined Register Address

8.5.7 Sequential WRITE Starting at a Defined Register Address

A sequential write operation is an extension of the single write protocol and shown in Sequential WRITE Starting at a Defined Register Address . If the controller does not send a stop condition after the device has issued an ACK, the device auto increments the register address by one and the controller is able to write to the next register.

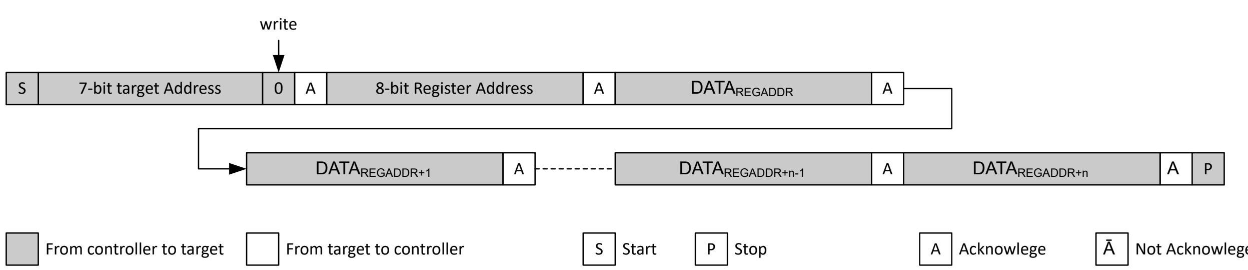

Figure 8-40. Sequential WRITE Starting at a Defined Register Address

9 LM251772 Registers

Table 9-1 lists the memory-mapped registers for the LM251772 registers. All register offset addresses not listed in Table 9-1 must be considered as reserved locations and the register contents must not be modified.

Table 9-1. LM251772 Registers

Offset	Acronym	Register Name	Section
3h	CLEAR_FAULTS	CLEAR_FAULTS	Section 9.1
Ah	ILIM_THRESHOLD	ILIM_THRESHOLD	Section 9.2
Ch	VOUT_TARGET1_LSB	VOUT_TARGET1_LSB	Section 9.3
Dh	VOUT_TARGET1_MSB	VOUT_TARGET1_MSB	Section 9.4
21h	USB_PD_STATUS_0	USB_PD_STATUS_0	Section 9.5
78h	STATUS_BYTE	STATUS_BYTE	Section 9.6
81h	USB_PD_CONTROL_0	USB_PD_CONTROL_0	Section 9.7
D0h	MFR_SPECIFIC_D0	MFR_SPECIFIC_D0	Section 9.8
D1h	MFR_SPECIFIC_D1	MFR_SPECIFIC_D1	Section 9.9
D2h	MFR_SPECIFIC_D2	MFR_SPECIFIC_D2	Section 9.10
D5h	MFR_SPECIFIC_D5	MFR_SPECIFIC_D5	Section 9.11
D6h	MFR_SPECIFIC_D6	MFR_SPECIFIC_D6	Section 9.12
D7h	MFR_SPECIFIC_D7	MFR_SPECIFIC_D7	Section 9.13
D8h	MFR_SPECIFIC_D8	MFR_SPECIFIC_D8	Section 9.14
DAh	IVP_VOLTAGE	IVP_VOLTAGE	Section 9.15

Complex bit access types are encoded to fit into small table cells. Table 9-2 shows the codes that are used for access types in this section.

Table 9-2. LM251772 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

9.1 CLEAR_FAULTS Register (Offset = 3h) [Reset = 00h]

CLEAR_FAULTS is shown in Table 9-3.

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clear all latched status flags

Table 9-3. CLEAR_FAULTS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLEAR_FAULTS	R	0h	Accessing the address is enough to clear fault

9.2 ILIM_THRESHOLD Register (Offset = Ah) [Reset = 12h]

ILIM_THRESHOLD is shown in Table 9-4.

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Table 9-4. ILIM_THRESHOLD Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ILIM_THRESHOLD	R/W	12h	ISNS current limit threshold voltage. Value in bracket considers a 10mOhms sens resistor 0h = 5mV (0.5A) 1h = 5mV (0.5A) 2h = 5mV (0.5A) 3h = 5mV (0.5A) 4h = 5mV (0.5A) 5h = 5mV (0.5A) 6h = 5mV (0.5A) 7h = 5mV (0.5A) 8h = 5mV (0.5A) 9h = 5mV (0.5A) Ah = 5mV (0.5A) Bh = 5.5mV (0.55A) Ch = 6mV (0.6A) Dh = 6.5mV (0.65A) Eh = 7mV (0.7A) Fh = 7.5mV (0.75A) 10h = 8mV (0.8A) 11h = 8.5mV (0.85A) 12h = **9mV (0.9A)** 13h = 9.5mV (0.95A) 14h = 10mV (1A) 15h = 10.5mV (1.05A) 16h = 11mV (1.1A) 17h = 11.5mV (1.15A) 18h = 12mV (1.2A) 19h = 12.5mV (1.25A) 1Ah = 13mV (1.3A) 1Bh = 13.5mV (1.35A) 1Ch = 14mV (1.4A) 1Dh = 14.5mV (1.45A) 1Eh = 15mV (1.5A) 1Fh = 15.5mV (1.55A) 20h = 16mV (1.6A) 21h = 16.5mV (1.65A) 22h = 17mV (1.7A) 23h = 17.5mV (1.75A) 24h = 18mV (1.8A) 25h = 18.5mV (1.85A) 26h = 19mV (1.9A) 27h = 19.5mV (1.95A) 28h = 20mV (2A) 29h = 20.5mV (2.05A) 2Ah = 21mV (2.1A) 2Bh = 21.5mV (2.15A) 2Ch = 22mV (2.2A) 2Dh = 22.5mV (2.25A) 2Eh = 23mV (2.3A) 2Fh = 23.5mV (2.35A) 30h = 24mV (2.4A) 31h = 24.5mV (2.45A) 32h = 25mV (2.5A) 33h = 25.5mV (2.55A) 34h = 26mV (2.6A) 35h = 26.5mV (2.65A) 36h = 27mV (2.7A) 37h = 27.5mV (2.75A) 38h = 28mV (2.8A) 39h = 28.5mV (2.85A) 3Ah = 29mV (2.9A) 3Bh = 29.5mV (2.95A) 3Ch = 30mV (3A) 3Dh = 30.5mV (3.05A) 3Eh = 31mV (3.1A)

Table 9-4. ILIM_THRESHOLD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				3Fh = 31.5mV (3.15A) 40h = 32mV (3.2A) 41h = 32.5mV (3.25A) 42h = 33mV (3.3A) 43h = 33.5mV (3.35A) 44h = 34mV (3.4A) 45h = 34.5mV (3.45A) 46h = 35mV (3.5A) 47h = 35.5mV (3.55A) 48h = 36mV (3.6A) 49h = 36.5mV (3.65A) 4Ah = 37mV (3.7A) 4Bh = 37.5mV (3.75A) 4Ch = 38mV (3.8A) 4Dh = 38.5mV (3.85A) 4Eh = 39mV (3.9A) 4Fh = 39.5mV (3.95A) 50h = 40mV (4A) 51h = 40.5mV (4.05A) 52h = 41mV (4.1A) 53h = 41.5mV (4.15A) 54h = 42mV (4.2A) 55h = 42.5mV (4.25A) 56h = 43mV (4.3A) 57h = 43.5mV (4.35A) 58h = 44mV (4.4A) 59h = 44.5mV (4.45A) 5Ah = 45mV (4.5A) 5Bh = 45.5mV (4.55A) 5Ch = 46mV (4.6A) 5Dh = 46.5mV (4.65A) 5Eh = 47mV (4.7A) 5Fh = 47.5mV (4.75A) 60h = 48mV (4.8A) 61h = 48.5mV (4.85A) 62h = 49mV (4.9A) 63h = 49.5mV (4.95A) 64h = 50mV (5A) 65h = 50.5mV (5.05A) 66h = 51mV (5.1A) 67h = 51.5mV (5.15A) 68h = 52mV (5.2A) 69h = 52.5mV (5.25A) 6Ah = 53mV (5.3A) 6Bh = 53.5mV (5.35A) 6Ch = 54mV (5.4A) 6Dh = 54.5mV (5.45A) 6Eh = 55mV (5.5A) 6Fh = 55.5mV (5.55A) 70h = 56mV (5.6A) 71h = 56.5mV (5.65A) 72h = 57mV (5.7A) 73h = 57.5mV (5.75A) 74h = 58mV (5.8A) 75h = 58.5mV (5.85A) 76h = 59mV (5.9A) 77h = 59.5mV (5.95A) 78h = 60mV (6A) 79h = 60.5mV (6.05A) 7Ah = 61mV (6.1A) 7Bh = 61.5mV (6.15A) 7Ch = 62mV (6.2A) 7Dh = 62.5mV (6.25A) 7Eh = 63mV (6.3A) 7Fh = 63.5mV (6.35A)

Table 9-4. ILIM_THRESHOLD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				80h = 64mV (6.4A) 81h = 64.5mV (6.45A) 82h = 65mV (6.5A) 83h = 65.5mV (6.55A) 84h = 66mV (6.6A) 85h = 66.5mV (6.65A) 86h = 67mV (6.7A) 87h = 67.5mV (6.75A) 88h = 68mV (6.8A) 89h = 68.5mV (6.85A) 8Ah = 69mV (6.9A) 8Bh = 69.5mV (6.95A) 8Ch = 70mV (7A) 8Dh = 70mV (7A) 8Eh = 70mV (7A) 8Fh = 70mV (7A) 90h = 70mV (7A) 91h = 70mV (7A) 92h = 70mV (7A) 93h = 70mV (7A) 94h = 70mV (7A) 95h = 70mV (7A) 96h = 70mV (7A) 97h = 70mV (7A) 98h = 70mV (7A) 99h = 70mV (7A) 9Ah = 70mV (7A) 9Bh = 70mV (7A) 9Ch = 70mV (7A) 9Dh = 70mV (7A) 9Eh = 70mV (7A) 9Fh = 70mV (7A) A0h = 70mV (7A) A1h = 70mV (7A) A2h = 70mV (7A) A3h = 70mV (7A) A4h = 70mV (7A) A5h = 70mV (7A) A6h = 70mV (7A) A7h = 70mV (7A) A8h = 70mV (7A) A9h = 70mV (7A) AAh = 70mV (7A) ABh = 70mV (7A) ACh = 70mV (7A) ADh = 70mV (7A) AEh = 70mV (7A) AFh = 70mV (7A) B0h = 70mV (7A) B1h = 70mV (7A) B2h = 70mV (7A) B3h = 70mV (7A) B4h = 70mV (7A) B5h = 70mV (7A) B6h = 70mV (7A) B7h = 70mV (7A) B8h = 70mV (7A) B9h = 70mV (7A) BAh = 70mV (7A) BBh = 70mV (7A) BCh = 70mV (7A) BDh = 70mV (7A) BEh = 70mV (7A) BFh = 70mV (7A) C0h = 70mV (7A)

Table 9-4. ILIM_THRESHOLD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				C1h = 70mV (7A) C2h = 70mV (7A) C3h = 70mV (7A) C4h = 70mV (7A) C5h = 70mV (7A) C6h = 70mV (7A) C7h = 70mV (7A) C8h = 70mV (7A) C9h = 70mV (7A) CAh = 70mV (7A) CBh = 70mV (7A) CCh = 70mV (7A) CDh = 70mV (7A) CEh = 70mV (7A) CFh = 70mV (7A) D0h = 70mV (7A) D1h = 70mV (7A) D2h = 70mV (7A) D3h = 70mV (7A) D4h = 70mV (7A) D5h = 70mV (7A) D6h = 70mV (7A) D7h = 70mV (7A) D8h = 70mV (7A) D9h = 70mV (7A) DAh = 70mV (7A) DBh = 70mV (7A) DCh = 70mV (7A) DDh = 70mV (7A) DEh = 70mV (7A) DFh = 70mV (7A) E0h = 70mV (7A) E1h = 70mV (7A) E2h = 70mV (7A) E3h = 70mV (7A) E4h = 70mV (7A) E5h = 70mV (7A) E6h = 70mV (7A) E7h = 70mV (7A) E8h = 70mV (7A) E9h = 70mV (7A) EAh = 70mV (7A) EBh = 70mV (7A) ECh = 70mV (7A) EDh = 70mV (7A) EEh = 70mV (7A) EFh = 70mV (7A) F0h = 70mV (7A) F1h = 70mV (7A) F2h = 70mV (7A) F3h = 70mV (7A) F4h = 70mV (7A) F5h = 70mV (7A) F6h = 70mV (7A) F7h = 70mV (7A) F8h = 70mV (7A) F9h = 70mV (7A) FAh = 70mV (7A) FBh = 70mV (7A) FCh = 70mV (7A) FDh = 70mV (7A) FEh = 70mV (7A) FFh = 70mV (7A)

9.3 VOUT_TARGET1_LSB Register (Offset = Ch) [Reset = FFh]

VOUT_TARGET1_LSB is shown in Table 9-5.

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Table 9-5. VOUT_TARGET1_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VOUT_A	R/W	FFh	Output target Voltage Logical Register Vout Setting Lower Limit: 3.3V or 1V depending on SEL__FB_DIV20 Upper Limit: 48V or 24V depending on SEL__FB_DIV20 Step size: 20mV or 10mV depending on SEL__FB_DIV20 Value Calculation for 20mV Equation 3 Value Calculation for 10mV Equation 2

9.4 VOUT_TARGET1_MSB Register (Offset = Dh) [Reset = 00h]

VOUT_TARGET1_MSB is shown in Table 9-6.

Return to the Summary Table.

Table 9-6. VOUT_TARGET1_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	NIL	R	0h	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.
3-0	VOUT_A	R/W	0h	Output target Voltage Logical Register Vout Setting Lower Limit: 3.3V or 1V depending on SEL__FB_DIV20 Upper Limit: 48V or 24V depending on SEL__FB_DIV20 Step size: 20mV or 10mV depending on SEL__FB_DIV20 Value Calculation for 20mV Equation 3 Value Calculation for 10mV Equation 2

9.5 USB_PD_STATUS_0 Register (Offset = 21h) [Reset = 00h]

USB_PD_STATUS_0 is shown in Table 9-7.

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USB-PD STATUS REGISTER

Table 9-7. USB_PD_STATUS_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	NIL	R	0h	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.
6	CC_OPERATION	R	0h	Instantaneous status for constant current (CC) ILIM operation
5-0	NIL	R	0h	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.

9.6 STATUS_BYTE Register (Offset = 78h) [Reset = 00h]

STATUS_BYTE is shown in Table 9-8.

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FAULT STATUS LOW BYTE

Table 9-8. STATUS_BYTE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUSY	R	0h	unit is busy 0h = **unit not busy** 1h = unit busy
6	OFF	R	0h	device not providing VOUT and/or unit is off 0h = **unit on** 1h = unit off
5	VOUT	R	0h	VOUT_OV fault 0h = **no fault** 1h = fault
4	IOUT	R	0h	IOUT_OC fault 0h = **no fault** 1h = fault
3	INPUT	R	0h	VIN_UV fault 0h = **no fault** 1h = fault
2	TEMPERATURE	R	0h	Temperature fault or warning 0h = **no fault** 1h = fault
1	CML	R	0h	Comm, Logic, Memory event 0h = **no fault** 1h = fault
0	OTHER	R	0h	other fault or warning 0h = **no fault** 1h = fault

9.7 USB_PD_CONTROL_0 Register (Offset = 81h) [Reset = 00h]

USB_PD_CONTROL_0 is shown in Table 9-9.

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USB-PD CONTROL REGISTER

Table 9-9. USB_PD_CONTROL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	NIL	R	0h	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.
1	FORCE_DISCH	R/W	0h	Activates Vo discharge 0h = **DISABLE** 1h = ENABLE
0	CONV_EN2	R/W	0h	Enables the power stage 0h = **DISABLE** 1h = ENABLE

9.8 MFR_SPECIFIC_D0 Register (Offset = D0h) [Reset = 32h]

MFR_SPECIFIC_D0 is shown in Table 9-10.

Return to the Summary Table.

CONFIG_0 Device Configuration Register 0

Table 9-10. MFR_SPECIFIC_D0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	NIL	R	0h	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.
6	EN_NEG_CL_LIMIT	R/W	0h	Enables ILIM for negative current limit, If disabled ILIM clamps pos I_L 0h = **DISABLE** 1h = ENABLE
5	EN_VCC1	R/W	1h	Enables the VCC1 auxiliary LDO 0h = DISABLE 1h = **ENABLE**
4	IMON_LIMITER_EN	R/W	1h	Enables the Imon in limiter configuration 0h = DISABLE 1h = **ENABLE**
3	HICCUP_EN	R/W	0h	Enables Hiccup short circuit 0h = **DISABLE** 1h = ENABLE
2	DRSS_EN	R/W	0h	Enables Dual Spread Spectrum 0h = **DISABLE** 1h = ENABLE
1	USLEEP_EN	R/W	1h	Enables micro sleep mode 0h = DISABLE 1h = **ENABLE**
0	CONV_EN	R/W	0h	Enables the power stage 0h = **DISABLE** 1h = ENABLE

9.9 MFR_SPECIFIC_D1 Register (Offset = D1h) [Reset = 19h]

MFR_SPECIFIC_D1 is shown in Table 9-11.

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CONFIG_1 Device Configuration Register 1

Table 9-11. MFR_SPECIFIC_D1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_THER_WARN	R/W	0h	Enables Thermal Warning 0h = **DISABLE** 1h = ENABLE
6-5	THW_THRESHOLD	R/W	0h	Selects the Thermal Warning Threshold 0h = **140degC** 1h = 125degC 2h = 110degC 3h = 95degC
4	EN_NINT	R/W	1h	Configures the nFLT pin handler to act as interrupt pin or nFLT pin 0h = DISABLE 1h = **ENABLE**
3	EN_DTRK_STARTOVER	R/W	1h	Enables a direct start-up if DTRK is enabled without waiting for the DTRK PWM signal 0h = DISABLE 1h = **ENABLE**
2	FORCE_BIASPIN	R/W	0h	Enables the priority to supply VCC2 from BIAS by lowering the threshold. 0h = **DISABLE** 1h = ENABLE
1	EN_BB_2P_FPWM	R/W	0h	Enables 2phase BB switching in fPWM mode 0h = **DISABLE** 1h = ENABLE
0	EN_BB_2P_PSM	R/W	1h	Enables 2phase BB switching in PSM mode 0h = DISABLE 1h = **ENABLE**

9.10 MFR_SPECIFIC_D2 Register (Offset = D2h) [Reset = 7Ah]

MFR_SPECIFIC_D2 is shown in Table 9-12.

Return to the Summary Table.

Table 9-12. MFR_SPECIFIC_D2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	NIL	R	0h	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.
6	EN_ACTIVE_DVS	R/W	1h	Enables the active down ramp for DVS using the discharge 0h = DISABLE 1h = **ENABLE**
5-4	DVS_SLEW_RAMP	R/W	3h	Sets the positive and negative Vo slew rate for DVS 0h = 40mV/µs 1h = 20mV/µs 2h = 1mV/µs 3h = **0.5mV/µs**
3-2	DISCHARGE_STRENGTH	R/W	2h	Sets the discharge current for the Vo discharge 0h = SLOW (25mA) 1h = MEDIUM (50mA) 2h = **FAST (75mA)** 3h = FAST (75mA)
1	DISCHARGE_CONFIG0	R/W	1h	Selects the discharge together with CONV_EN 0h = DISABLE 1h = **ENABLE**
0	DISCHARGE_CONFIG1	R/W	0h	Selects the discharge until the VTH DISCH 0h = **DISABLE** 1h = ENABLE

9.11 MFR_SPECIFIC_D5 Register (Offset = D5h) [Reset = 3Fh]

MFR_SPECIFIC_D5 is shown in Table 9-13.

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Table 9-13. MFR_SPECIFIC_D5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	NIL	R	0h	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.

Table 9-13. MFR_SPECIFIC_D5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	V_OVP2	R/W	3Fh	OVP2 threshold voltage 0h = 4.00V 1h = 4.500V 2h = 5.000V 3h = 5.500V 4h = 6.000V 5h = 6.500V 6h = 7.000V 7h = 7.500V 8h = 8.000V 9h = 8.500V Ah = 9.000V Bh = 9.500V Ch = 10.000V Dh = 10.500V Eh = 11.000V Fh = 11.500V 10h = 12.000V 11h = 12.500V 12h = 13.000V 13h = 13.500V 14h = 14.000V 15h = 14.500V 16h = 15.000V 17h = 15.500V 18h = 16.000V 19h = 17.000V 1Ah = 18.000V 1Bh = 19.000V 1Ch = 20.000V 1Dh = 21.000V 1Eh = 22.000V 1Fh = 23.000V 20h = 24.000V 21h = 25.000V 22h = 26.000V 23h = 27.000V 24h = 28.000V 25h = 29.000V 26h = 30.000V 27h = 31.000V 28h = 32.000V 29h = 33.000V 2Ah = 34.000V 2Bh = 35.000V 2Ch = 36.000V 2Dh = 37.000V 2Eh = 38.000V 2Fh = 39.000V 30h = 40.000V 31h = 41.000V 32h = 42.000V 33h = 43.000V 34h = 44.000V 35h = 45.000V 36h = 46.000V 37h = 47.000V 38h = 48.000V 39h = 49.000V 3Ah = 50.000V 3Bh = 51.000V 3Ch = 52.000V 3Dh = 53.000V 3Eh = 54.000V

Table 9-13. MFR_SPECIFIC_D5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				3Fh = **55.000V**

9.12 MFR_SPECIFIC_D6 Register (Offset = D6h) [Reset = 15h]

MFR_SPECIFIC_D6 is shown in Table 9-14.

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PS_Config0 Power stage Configuration

Table 9-14. MFR_SPECIFIC_D6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CONFIG_SYNC_PIN	R/W	0h	Selects the SYNC function to maintain parallel operation 0h = **Input sync on rising edge** 1h = Input sync on falling edge 2h = Sync output from internal rising edge 3h = Sync output from internal falling edge (180deg phase)
5	EN_CONST_TDEAD	R/W	0h	Forces a constant deadtime for the setting of SEL_MIN_DEADTIME_GDRV. Disables frequency dependency of min Tdead 0h = **DISABLE** 1h = ENABLE
4	SEL_SCALE_DT	R/W	1h	Scales the gate driver dead time freq dependence and 2MHz setpoint 0h = DISABLE 1h = **ENABLE**
3-2	SEL_MIN_DEADTIME_GDRV	R/W	1h	Defines the minimum dead time at fsw = 2Mhz for the gate driver 0h = 10ns (No delay) 1h = **20ns** 2h = 40ns 3h = 60ns
1-0	BB_MIN_TIME_OFFSET	R/W	1h	Scales the BB min Ton or Toff time for the gate refresh 0h = 0.75x 1h = **1x** 2h = 1.25x 3h = 1.5x

9.13 MFR_SPECIFIC_D7 Register (Offset = D7h) [Reset = 28h]

MFR_SPECIFIC_D7 is shown in Table 9-15.

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Table 9-15. MFR_SPECIFIC_D7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	NIL	R	0h	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.
5-4	SEL_INDUC_DERATE	R/W	2h	Select the inductor de-rating for PSM mode to slope 0h = DISABLE 1h = 20% 2h = **30%** 3h = 40%
3-0	SEL_SLOPE_COMP	R/W	8h	Select slope comp current, as ratio of RT current 0h = 0.125 1h = 0.25 2h = 0.375 3h = 0.5 4h = 0.625 5h = 0.75 6h = 0.875 7h = 1 8h = **1.5** 9h = 2 Ah = 2.5 Bh = 3 Ch = 3.5 Dh = 4 Eh = 4.5 Fh = 5

9.14 MFR_SPECIFIC_D8 Register (Offset = D8h) [Reset = 84h]

MFR_SPECIFIC_D8 is shown in Table 9-16.

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Table 9-16. MFR_SPECIFIC_D8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SEL_FB_DIV20	R/W	1h	Select internal FB divider ratio of 20 0h = DIV10 1h = **DIV20**
6	EN_CDC	R/W	0h	Enables the cable drop compensation 0h = **DISABLE** 1h = ENABLE
5-4	CDC_GAIN	R/W	0h	Selects the Gain for the CDC voltage (1V) with respect to Vout 0h = **0.250V** 1h = 0.500V 2h = 1.000V 3h = 2.000V
3-2	SEL_DRV1_SEQ	R/W	1h	Select the sequencing for the DRV 1 operation 0h = Pull-Low/ CP running if converter operation is off 1h = **Pull-Low/ CP running if converter operation is on** 2h = FORCE ACTIVE 3h = FORCE OFF
1-0	SEL_DRV1_SUP	R/W	0h	Select the driver configuration for DRV1 pin 0h = **Open Drain (active = pull low)** 1h = Vout 2h = VBIAS 3h = VCC2 (Charge Pump driver)

9.15 IVP_VOLTAGE Register (Offset = DAh) [Reset = FFh]

IVP_VOLTAGE is shown in Table 9-17.

Return to the Summary Table.

Table 9-17. IVP_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	V_IVP	R/W	FFh	Input Overvoltage Protection and Regulation Threshold 0h = 4.75V 1h = 4.875V 2h = 5.000V 3h = 5.125V 4h = 5.250V 5h = 5.375V 6h = 5.500V 7h = 5.625V 8h = 5.750V 9h = 5.875V Ah = 6.000V Bh = 6.125V Ch = 6.250V Dh = 6.375V Eh = 6.500V Fh = 6.625V 10h = 6.750V 11h = 6.875V 12h = 7.000V 13h = 7.125V 14h = 7.250V 15h = 7.375V 16h = 7.500V 17h = 7.625V 18h = 7.750V 19h = 7.875V 1Ah = 8.000V 1Bh = 8.125V 1Ch = 8.250V 1Dh = 8.375V 1Eh = 8.500V 1Fh = 8.625V 20h = 8.750V 21h = 8.875V 22h = 9.000V 23h = 9.125V 24h = 9.250V 25h = 9.375V 26h = 9.500V 27h = 9.625V 28h = 9.750V 29h = 9.875V 2Ah = 10.000V 2Bh = 10.125V 2Ch = 10.250V 2Dh = 10.375V 2Eh = 10.500V 2Fh = 10.625V 30h = 10.750V 31h = 10.875V 32h = 11.000V 33h = 11.125V 34h = 11.250V 35h = 11.375V 36h = 11.500V 37h = 11.625V 38h = 11.750V 39h = 11.875V 3Ah = 12.000V 3Bh = 12.125V 3Ch = 12.250V 3Dh = 12.375V 3Eh = 12.500V 3Fh = 12.625V

Table 9-17. IVP_VOLTAGE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				40h = 12.750V 41h = 12.875V 42h = 13.000V 43h = 13.125V 44h = 13.250V 45h = 13.375V 46h = 13.500V 47h = 13.625V 48h = 13.750V 49h = 13.875V 4Ah = 14.000V 4Bh = 14.125V 4Ch = 14.250V 4Dh = 14.375V 4Eh = 14.500V 4Fh = 14.625V 50h = 14.750V 51h = 14.875V 52h = 15.000V 53h = 15.125V 54h = 15.250V 55h = 15.375V 56h = 15.500V 57h = 15.625V 58h = 15.750V 59h = 15.875V 5Ah = 16.000V 5Bh = 16.125V 5Ch = 16.250V 5Dh = 16.375V 5Eh = 16.500V 5Fh = 16.625V 60h = 16.750V 61h = 16.875V 62h = 17.000V 63h = 17.125V 64h = 17.250V 65h = 17.375V 66h = 17.500V 67h = 17.625V 68h = 17.750V 69h = 17.875V 6Ah = 18.000V 6Bh = 18.125V 6Ch = 18.250V 6Dh = 18.375V 6Eh = 18.500V 6Fh = 18.625V 70h = 18.750V 71h = 18.875V 72h = 19.000V 73h = 19.125V 74h = 19.250V 75h = 19.375V 76h = 19.500V 77h = 19.625V 78h = 19.750V 79h = 19.875V 7Ah = 20.000V 7Bh = 20.125V 7Ch = 20.250V 7Dh = 20.375V 7Eh = 20.500V 7Fh = 20.625V 80h = 20.750V

Table 9-17. IVP_VOLTAGE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				81h = 20.875V 82h = 21.000V 83h = 21.125V 84h = 21.250V 85h = 21.375V 86h = 21.500V 87h = 21.625V 88h = 21.750V 89h = 21.875V 8Ah = 22.000V 8Bh = 22.125V 8Ch = 22.250V 8Dh = 22.375V 8Eh = 22.500V 8Fh = 22.625V 90h = 22.750V 91h = 22.875V 92h = 23.000V 93h = 23.125V 94h = 23.250V 95h = 23.500V 96h = 23.750V 97h = 24.000V 98h = 24.250V 99h = 24.500V 9Ah = 24.750V 9Bh = 25.000V 9Ch = 25.250V 9Dh = 25.500V 9Eh = 25.750V 9Fh = 26.000V A0h = 26.250V A1h = 26.500V A2h = 26.750V A3h = 27.000V A4h = 27.250V A5h = 27.500V A6h = 27.750V A7h = 28.000V A8h = 28.250V A9h = 28.500V AAh = 28.750V ABh = 29.000V ACh = 29.250V ADh = 29.500V AEh = 29.750V AFh = 30.000V B0h = 30.250V B1h = 30.500V B2h = 30.750V B3h = 31.000V B4h = 31.250V B5h = 31.500V B6h = 31.750V B7h = 32.000V B8h = 32.250V B9h = 32.500V BAh = 32.750V BBh = 33.000V BCh = 33.250V BDh = 33.500V BEh = 33.750V BFh = 34.000V C0h = 34.250V C1h = 34.500V

Table 9-17. IVP_VOLTAGE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				C2h = 34.750V C3h = 35.000V C4h = 35.250V C5h = 35.500V C6h = 35.750V C7h = 36.000V C8h = 36.250V C9h = 36.500V CAh = 36.750V CBh = 37.000V CCh = 37.250V CDh = 37.500V CEh = 37.750V CFh = 38.000V D0h = 38.250V D1h = 38.500V D2h = 38.750V D3h = 39.000V D4h = 39.250V D5h = 39.500V D6h = 39.750V D7h = 40.000V D8h = 40.250V D9h = 40.500V DAh = 40.750V DBh = 41.000V DCh = 41.250V DDh = 41.500V DEh = 41.750V DFh = 42.000V E0h = 42.250V E1h = 42.500V E2h = 42.750V E3h = 43.000V E4h = 43.250V E5h = 43.500V E6h = 43.750V E7h = 44.000V E8h = 44.250V E9h = 44.500V EAh = 44.750V EBh = 45.000V ECh = 45.250V EDh = 45.500V EEh = 45.750V EFh = 46.000V F0h = 46.250V F1h = 46.500V F2h = 46.750V F3h = 47.000V F4h = 47.250V F5h = 47.500V F6h = 47.750V F7h = 48.000V F8h = 48.250V F9h = 48.500V FAh = 48.750V FBh = 49.000V FCh = 49.250V FDh = 49.500V FEh = 49.750V FFh = **50.000V**

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The LM251772-Q1 is a wide input voltage, synchronous, non-inverting buck-boost controller, designed for applications that need a regulated output voltage from an input supply range higher or lower than the output voltage. To expedite and streamline the process of designing the external circuits and select the components, a comprehensive quickstart calculator is available for download to assist the designer with component selection for a given application.

10.2 Typical Application

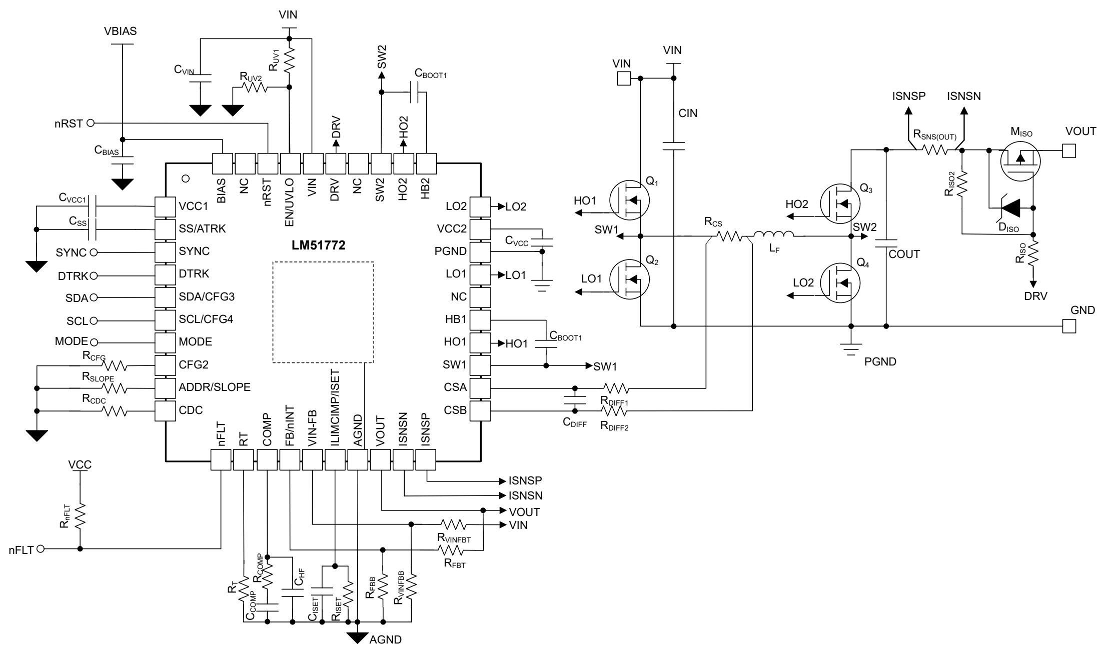


Figure 10-1. Simplified Schematic of a Typical Application

10.2.1 Design Requirements

Table 10-1 shows the intended input, output, and performance parameters for a typical design example.

Table 10-1. Design Parameters

Parameter	Value
V_I minimum	9V
V_I typical = V_I start-up	19.5V
V_I maximum	48V
V_O nominal	20V
P_O maximum	100W

10.2.2 Detailed Design Procedure

10.2.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the LM251772-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize the design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible applications from Texas Instruments.
3. WEBENCH Power Designer provides a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, WEBENCH Power Designer also provides:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of the board,
   - Export the customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share the design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

10.2.2.2 Frequency

The switching frequency of LM251772-Q1 is set by an R_T resistor connected from the RT/SYNC pin to AGND. The R_T resistor required to set the desired frequency is calculated using Equation 26. A 1% standard resistor of 51.0kΩ is selected for f_{SW} = 600kHz.

$$R_{(RT)} = \frac{1}{32 \times 12^{-12} \times f_{SW}} = 52.08k\Omega \tag{26}$$

10.2.2.3 Feedback Divider

The feedback voltage divider is found with Equation 27:

$$R_{FB,top} = \frac{\left(V_{(VOUT)} - V_{(REF)}\right)}{V_{(REF)}} \times R_{FB,bot} \tag{27}$$

For the 20V output, an upper resistor of 82.0kΩ and a lower resistor of 4.3kΩ have been selected.

FB Pin Resistor Divider Examples with $R_{FB,top}$ = 71.5kΩ shows an overview of a possible selection for the feedback divider resistors over common output voltages.

Table 10-2. FB Pin Resistor Divider Examples with $R_{FB,top}$ = 71.5kΩ

V_O – Target	$R_{FB,bot}$ – Calculation	$R_{FB,bot}$ – E48 Series	V_O Nominal	Error from FB Resistor
5V	17.9kΩ	17.8kΩ	5.02V	0.3%
9V	8.94kΩ	9.09kΩ	8.87V	-1.5%
12V	6.50kΩ	6.59kΩ	12.02V	0.1%
16V	4.77kΩ	4.87kΩ	15.68V	-2.0%
24V	3.11kΩ	3.16kΩ	23.63V	–1.6%
28V	2.65kΩ	2.61kΩ	28.39V	1.4%
36V	2.04kΩ	2.05kΩ	35.88V	–0.3%
42V	1.74kΩ	1.78kΩ	41.17V	-2.0%
48V	1.50kΩ	1.54kΩ	47.43V	–1.2%

10.2.2.4 Inductor and Current Sense Resistor Selection

The inductor selection is based on consideration of both buck and boost modes of operation and the range of the supported slope compensation. As inductor and current sense resistor influencing each other both needs to be selected depending on each other. A good starting point is to set the current sense resistor to have an average current level of 60% of the overcurrent detection level. This considers an inductor ripple ΔI_L of 20% and a margin of 20% to the overcurrent detection level. The highest inductor current appears at the lowest input voltage.

$$I_{L\ Peak,\ \mathrm{max,est.}} = \frac{V_{OUT}}{V_{IN,min}} \times I_{OUT} \times 1.4 = 15.6\mathrm{A} \tag{28}$$

The sense resistor is calculated with:

$$R_{CS} = \frac{\mathrm{V_{th+(CSB-CSA),nom}}}{I_{L\ Peak,\ \mathrm{max,est.}}} = 3.2\mathrm{m\Omega} \tag{29}$$

The inductor is selected with have a mid-level slope compensation and calculated with:

$$L = \frac{R_{CS} \times 625}{f_{SW}} = 3.35\mathrm{\mu H} \tag{30}$$

Additionally, the inductor selection can be based on the peak-to-peak current ripple ΔI_L for buck and boost mode, depending if better efficiency for buck or boost operation is important. The target inductance for buck mode with approximately 60% of the maximum inductor current at the maximum input voltage is:

$$\mathrm{L_{BUCK}} = \frac{\left(\mathrm{V_{IN(MAX)}} - \mathrm{V_{OUT}}\right) \times \mathrm{V_{OUT}}}{0.6 \times \mathrm{I_{OUT(MAX)}} \times \mathrm{F_{SW}} \times \mathrm{V_{IN(MAX)}}} = 6.48\mathrm{\mu H} \tag{31}$$

The target inductance for boost mode with approximately 30% of the maximum inductor current at the maximum input voltage is:

$$\mathrm{L_{BOOST}} = \frac{\mathrm{V_{IN(MIN)}^2} \times \left(\mathrm{V_{OUT}} - \mathrm{V_{IN(MIN)}}\right)}{0.3 \times \mathrm{I_{OUT(MAX)}} \times \mathrm{F_{SW}} \times \mathrm{V_{OUT}^2}} = 2.48\mathrm{\mu H} \tag{32}$$

For this application, an inductor with 3.3µH is selected.

The peak inductor current occurs at in this configuration occurs at minimum input voltage and with an efficiency of 95% is given by:

$$I_{L\ Peak\ Boost} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN,min}} + \frac{V_{IN,min} \times \left(V_{OUT} - V_{IN,min}\right)}{2 \times L \times f_{SW} \times V_{OUT}} = 12.9\mathrm{A} \tag{33}$$

For the current sense resistor a margin of 20% is considered to have enough headroom for the dynamic responses, for example load step regulation. To verify that the maximum output current be delivered, the minimum level of the peak current limit threshold is used:

$$R_{CS} = \frac{\mathrm{V_{th+(CSB-CSA),min}}}{I_{L\ Peak\ Boost}} = 3.5\mathrm{m\Omega} \tag{34}$$

The standard value of RCS = 2.5mΩ with 2 times 5mΩ is selected. With the two resistors in parallel, parasitic inductance is also reduced. The maximum power dissipation in RCS happens at VIN(MAX):

$$\mathrm{P}_{\mathrm{R}_{CS(Max)}} = \left(\frac{\mathrm{V_{th+(CSB-CSA),max}}}{R_{CS}}\right)^2 \times R_{CS} \times \left(1 - \frac{\mathrm{V_{OUT}}}{\mathrm{V_{IN(Max)}}}\right) = 0.704\mathrm{W} \tag{35}$$

10.2.2.5 Output Capacitor

In boost mode, the output capacitor conducts high ripple current. The output capacitor RMS ripple current is given by:

$$I_{COUT(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} - 1} \quad (36)$$

where the minimum V_{IN} corresponds to the maximum capacitor current.

In this example, the maximum output ripple RMS current is $I_{COUT(RMS)}$ = 5.5A. A 3mΩ output capacitor ESR causes an output ripple voltage of 33.3mV as given by:

$$\Delta V_{RIPPLE(ESR)} = \frac{I_{OUT} \times V_{OUT}}{V_{IN(MIN)}} \times ESR \quad (37)$$

A 80µF output capacitor causes a capacitive ripple voltage of 115mV as given by:

$$\Delta V_{RIPPLE(COUT)} = \frac{I_{OUT} \times \left(1 - \frac{V_{IN(MIN)}}{V_{OUT}}\right)}{C_{OUT} \times f_{SW}} \quad (38)$$

Typically, a combination of ceramic and bulk capacitors is needed to provide low ESR and high ripple current capacity. Section 10.2 shows a good starting point for C_{OUT} for typical applications.

10.2.2.6 Input Capacitor

In buck mode, the input capacitor supplies high ripple current. The RMS current in the input capacitor is given by:

$$I_{CIN(RMS)} = I_{OUT} \times \sqrt{D \times (1 - D)} \quad (39)$$

The maximum RMS current occurs at D = 0.5, which gives $I_{CIN(RMS)}$ = I_{OUT} / 2 = 2.5A. A combination of ceramic and bulk capacitors provides a short path for high di/dt current and to reduces the output voltage ripple. Figure 10-1 is a good starting point for C_{IN} for typical applications.

10.2.2.7 Slope Compensation

For stable current loop operation and to avoid subharmonic oscillations, the slope resistor is selected based on Equation 40.

For the calculation of the m_{SC} value for the Slope Compensation use the effective inductance at the maximum inductor current (set by the current limit). With a R_{CS} of 2.5mΩ the current limit is set to 20A (typically). For the used inductor the inductance does decrease to L_{eff} =2.5µH at this peak current.

$$m_{SC} = \frac{R_{CS}}{f_{sw} \times L_{eff}} \times 625 = 1.04 \quad (40)$$

The next higher value has to be selected which is 1.5 and then be set via R_{CFG1} or the I2C interface.

This slope compensation results in “dead-beat” operation, in which the current loop disturbances die out in one switching cycle. Theoretically, a current mode loop is stable with half the “dead-beat” slope (considered already in the calculated slope resistor value in Equation 40). A larger m_{sc} value results in larger slope signal, which is better for noise immunity in the transition region (V_{IN} is approximately equal to V_{OUT}). A larger slope signal, however, restricts the achievable input voltage range for a given output voltage, switching frequency, and inductor. For this design, a slope compensation factor of 1.5 (see Configuration Pin CFG2) is selected for better transition region behavior while still providing the required V_{IN} range.

The inductor derating is around 24% and the settling for 30% derating can be used (see Configuration Pin CFG3) or set using I2C.

10.2.2.8 UVLO Divider

The UVLO resistor divider need to be designed for turn-on below 8.7V. Selecting $R_{UVLO,top}$ = 75kΩ gives a UVLO hysteresis of 0.375V based on Equation 41. The lower UVLO resistor is selected using:

$$V_{(VIN,IT+,UVLO)} = V_{IT+(UVLO)} \times \left(1 + \frac{R_{UVLO,top}}{R_{UVLO,bot}}\right) + R_{UVLO,top} \times I_{(UVLO,hyst)} \tag{41}$$

A standard value of 12.4kΩ is selected for $R_{UVLO,bot}$.

When programming the UVLO threshold for lower input voltage operation, select MOSFETs with gate (Miller) plateau voltage lower than the minimum V_{IN}.

10.2.2.9 Soft-Start Capacitor

The soft-start time is programmed using the soft-start capacitor. The relationship between C_{SS} and the soft-start time is given by:

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{Ref}} = 18\ \text{nF} \tag{42}$$

C_{SS} = 18nF gives a soft-start time of 1.8ms.

10.2.2.10 MOSFETs QH1 and QL1

The input side MOSFETs QH1 (Q1) and QL1 (Q2) need to withstand the maximum input voltage of 48V. In addition, MOSFETS need to withstand the transient spikes at SW1 during switching. Therefore, QH1 and QL1 need to be rated for 58V or higher. The gate plateau voltages of the MOSFETs need to be smaller than the minimum input voltage of the converter, otherwise, the MOSFETs do not fully enhance during start-up or overload conditions.

The power loss in QH1 in boost mode is approximated by:

$$P_{COND(QH1)} = \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}}\right)^2 \times R_{DS,On(QH1)} \tag{43}$$

The power loss in QH1 in buck mode consists of both conduction and switching loss components given by Equation 44 and Equation 45, respectively:

$$P_{COND(QH1)} = \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}}\right)^2 \times R_{DS,On(QH1)} \tag{44}$$

$$P_{SW(QH1)} = \frac{1}{2} \times V_{IN} \times I_{OUT} \times (t_r + t_f) \times f_{SW} \tag{45}$$

The rise (t_r) and the fall (t_f) times are based on the MOSFET data sheet information or measured in the lab. Typically, a MOSFET with smaller R_{DSON} (smaller conduction loss) has longer rise and fall times (larger switching loss).

The power loss in QL1 in the buck mode of operation is shown in Equation 46:

$$P_{COND(QL1)} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times {I_{OUT}}^2 \times R_{DS,On(QL1)} \tag{46}$$

10.2.2.11 MOSFETs QH2 and QL2

The output side MOSFETs QH2 (Q4) and QL2 (Q3) see the output voltage of 48V and additional transient spikes at SW2 during switching. Therefore, QH2 and QL2 need to be rated for 58V or more. The gate plateau voltages of the MOSFETs need to be smaller than the minimum input voltage of the converter, otherwise, the MOSFETs do not always fully enhance during start-up or overload conditions.

The power loss in QH2 in buck mode of operation is approximated by:

$$P_{COND(QH2)} = I_{OUT}^2 \times R_{DS,On(QH2)} \tag{47}$$

The power loss in QL2 in the boost mode of operation consists of both conduction and switching loss components given by:

$$P_{COND(QL2)} = \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}}\right)^2 \times R_{DS,On(QL2)} \tag{48}$$

and, respectively:

$$P_{SW(QL2)} = \frac{1}{2} \times V_{OUT} \times \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}}\right) \times (t_r + t_f) \times f_{SW} \tag{49}$$

The rise (t_r) and the fall (t_f) times is obtained by the MOSFET data sheet information or measured in the lab. Typically, a MOSFET with smaller R_{DSON} (lower conduction loss) has longer rise and fall times (larger switching loss).

The power loss in QH2 in the boost mode of operation is shown below:

$$P_{COND(QH2)} = \frac{V_{IN}}{V_{OUT}} \times \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}}\right)^2 \times R_{DS,On(QH2)} \tag{50}$$

10.2.2.12 Loop Compensation

This section presents the control loop compensation design procedure for the LM251772-Q1 buck-boost controller. The LM251772-Q1 operates mainly in buck or boost modes, separated by a transition region, and therefore, the control loop design is done for both buck and boost operating modes. Then, a final selection of compensation is made based on the mode that is more restrictive from a loop stability point of view. Typically, for a converter designed to go deep into both buck and boost operating regions, the boost compensation design is more restrictive due to the presence of a right half plane zero (RHPZ) in boost mode.

The boost power stage output pole location is given by:

$$f_{p1(boost)} = \frac{1}{2\pi}\left(\frac{2}{R_{OUT} \times C_{OUT}}\right) = 995\text{Hz} \tag{51}$$

where

- R_{OUT} = 5.0Ω corresponds to the maximum load of 5.0A.

The boost power stage ESR zero location is given by:

$$f_{z1} = \frac{1}{2\pi}\left(\frac{1}{R_{ESR} \times C_{OUT}}\right) = 73.7\text{kHz} \tag{52}$$

The boost power stage RHP zero location is given by:

$$f_{RHP} = \frac{1}{2\pi}\left(\frac{R_{OUT} \times (1 - D_{MAX})^2}{L_1}\right) = 39.1\text{kHz} \tag{53}$$

where

- D_{MAX} is the maximum duty cycle at the minimum V_{IN}.

The buck power stage output pole location is given by:

$$f_{p1(buck)} = \frac{1}{2\pi}\left(\frac{1}{R_{OUT} \times C_{OUT}}\right) = 497\text{Hz} \tag{54}$$

The buck power stage ESR zero location is the same as the boost power stage ESR zero.

Equation 53 shows that RHP zero is the main factor limiting the achievable bandwidth. For a robust design, the crossover frequency needs to be less than 1/3 of the RHP zero frequency. Given the position of the RHP zero, a reasonable target bandwidth in boost operation is around 8kHz:

$$f_{bw} = 8\text{kHZ} \tag{55}$$

For some power stages, the boost RHP zero is not as restrictive, which happens when the boost maximum duty cycle (D_{MAX}) is small, or when a really small inductor is used. In those cases, compare the limits posed by the RHP zero (f_{RHP} / 3) with 1/20 of the switching frequency and use the smaller of the two values as the achievable bandwidth.

The compensation zero is placed at 1.5 times the boost output pole frequency. Keep in mind that this locates the zero at three times the buck output pole frequency, which results in approximately 30 degrees of phase loss before crossover of the buck loop and 15 degrees of phase loss at intermediate frequencies for the boost loop:

$$f_{ZC} = 1.5\text{kHz} \tag{56}$$

The compensation gain resistor, R_{c1}, is calculated with:

$$R_{C1} = \frac{2\pi \times f_{bw}}{gm_{EA}} \times \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \times \frac{A_{CS} \times R_{CS} \times C_{OUT}}{1 - D_{MAX}} \times \frac{1}{\sqrt{1 + \left(\frac{f_{bw}}{f_{RHP}}\right)^2}} = 7.4\text{k}\Omega \tag{57}$$

where

- D_{MAX} is the maximum duty cycle at the minimum V_{IN} in boost mode.
- A_{CS} is the current sense amplifier gain: 10.

The compensation capacitor, C_{c1}, is then calculated from:

$$C_{C1} = \frac{1}{2\pi \times f_{ZC} \times R_{c1}} = 14.5\text{nF} \tag{58}$$

The standard values of compensation components are selected to be R_{c1} = 7.32kΩ and C_{c1} = 15nF.

A high frequency pole (f_{pc2}) is placed using a capacitor (C_{c2}) in parallel with R_{c1} and C_{c1}. Set the frequency of this pole at seven to ten times of f_{bw} to provide attenuation of switching ripple and noise on COMP while avoiding excessive phase loss at the crossover frequency. For a target f_{pc2} = 98kHz, C_{c2} is calculated using Equation 59:

$$C_{C2} = \frac{1}{2\pi \times f_{pc2} \times R_{c1}} = 263\text{pF} \tag{59}$$

Select a standard value of 270pF for C_{c2}. These values provide a good starting point for the compensation design. Each design needs to be tuned in the lab to achieve the desired balance between stability margin across the operating range and transient response time.

10.2.2.13 External Component Selection

Table 10-3. Components Example for Typical Application

Reference	Description	Part Number	Comment
R_{COMP}	7.15kΩ		
C_{COMP1}	12nF, 50V Ceramic Capacitor		
C_{COMP2}	220pF, 50V Ceramic Capacitor		
C_{SS}	20nF, 50V Ceramic Capacitor or 20nF, 80V Ceramic Capacitor		
$R_{FB,top}$	82. 0kΩ		
$R_{FB,bot}$	4.3kΩ		
R_{nFLT}	10kΩ		
$C_{ILIMCOMP}$	82kΩ		
C_{IN1}	2 × 10µF, 100V Ceramic Capacitor	C3225X7R2A106K250AC	
C_{IN2}	3× 27µF, 63V Aluminum Capacitor	A768KE276M1JLAE054	
M_1	N-Channel 60V MOSFET, $R_{DS(on)}$ = 4.2mΩ	ISZ034N06LM5ATMA1	
M_2	N-Channel 60V MOSFET, $R_{DS(on)}$ = 4.2mΩ	ISZ034N06LM5ATMA1	
M_3	N-Channel 60V MOSFET, $R_{DS(on)}$ = 4.2mΩ	ISZ034N06LM5ATMA1	
M_4	N-Channel 60V MOSFET, $R_{DS(on)}$ = 4.2mΩ	ISZ034N06LM5ATMA1	
R_{CS}	2.5mΩ	2xKRL2012E-M-R005F-T5	
L_1	3.3µH, DCR = 5.7mΩ	XGL1060-332MEC	
C_{OUT1}	6 × 10µF, 100V Ceramic Capacitor	C3225X7R2A106K250AC	
C_{OUT2}	2 × 100µF, 63V Aluminum Capacitor	A768KE276M1JLAE054	
R_{ISNS}	10mΩ	KRL2012E-C-R010F-T05	
C_{BST1}	0.1µF, 50V Ceramic Capacitor	GCM155R71H104KE02D	
C_{BST2}	0.1µF, 50V Ceramic Capacitor	GCM155R71H104KE02D	
C_{VCC}	22µF, 10V Ceramic Capacitor	GRT188R61A226ME13D	
$R_{UVLO,top}$	75kΩ		
$R_{UVLO,bot}$	12.4kΩ		
R_{CFG2}	8.3kΩ		
R_{RT}	51kΩ		

10.2.3 Application Curves

$R_{(COMP)}$ = 20kΩ, $C_{(COMP)}$ = 2.1nF, $C_{(HF)}$ = 50pF unless otherwise noted

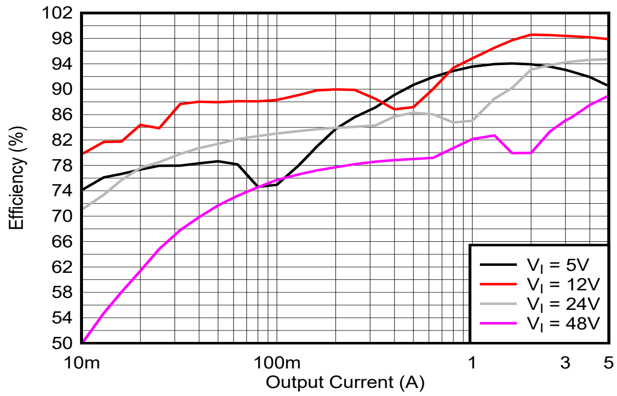


Figure 10-2. Efficiency Versus I_O (MODE = 0V, V_o = 12V)

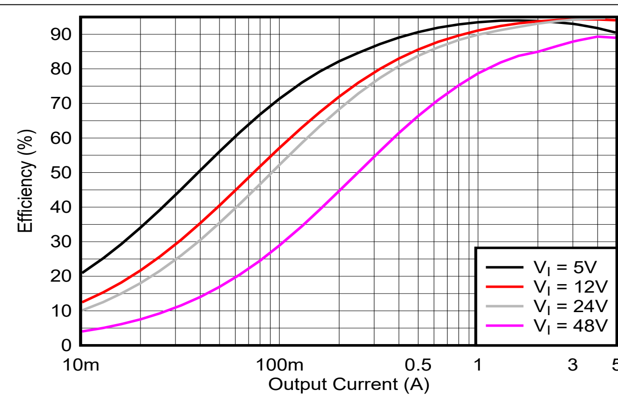


Figure 10-3. Efficiency Versus I_O (MODE = VCC2, V_o = 12V)

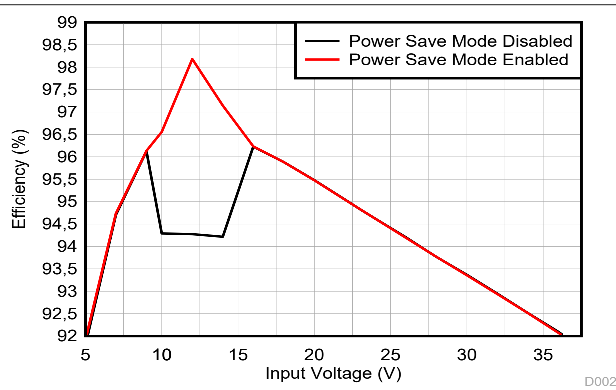


Figure 10-4. Efficiency Versus V_I (V_o = 12V, I_O = 5A)

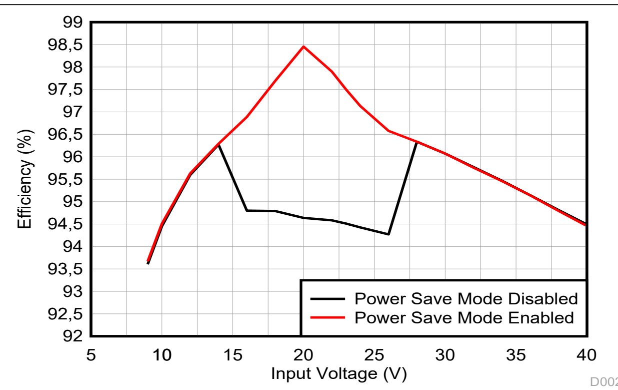


Figure 10-5. Efficiency Versus V_I (V_o = 20V, I_O = 5A)

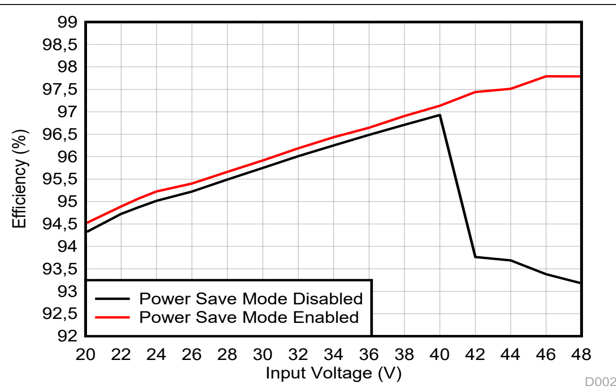


Figure 10-6. Efficiency Versus V_I (V_o = 48V, I_O = 5A)

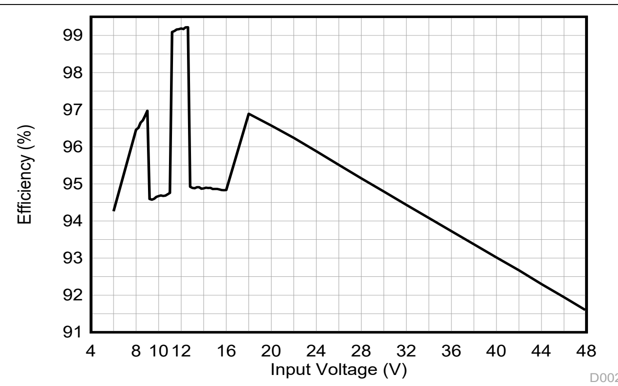


Figure 10-7. PCM Efficiency Versus V_I ($V_{(PCM,low)}$ = 11V, $V_{(PCM,high)}$ = 13V, I_O = 5A, MODE = VCC2)

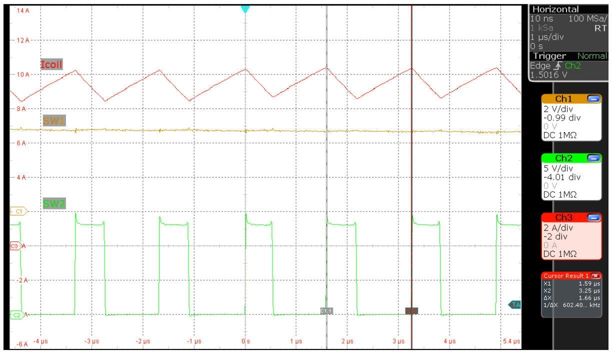


Figure 10-8. Inductor Current Boost Mode ($V_{(VIN)}$ = 5V, $V_{(VOUT)}$ = 12V I_O = 5A, MODE = VCC2)

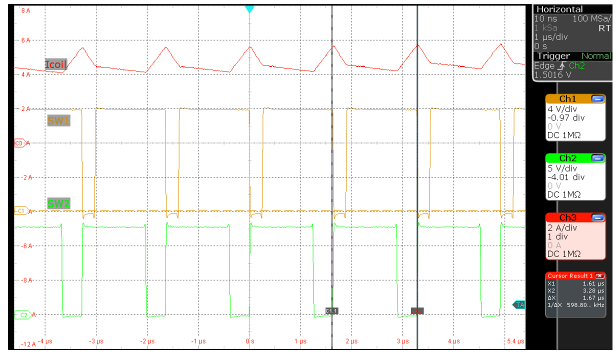


Figure 10-9. Inductor Current Buck-Boost Mode, ($V_{(VIN)}$ = 12V, $V_{(VOUT)}$ = 12V I_O = 5A, MODE = VCC2)

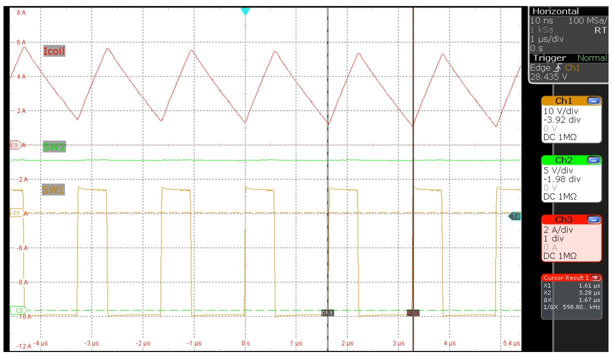


Figure 10-10. Inductor Current Buck Mode, $V_{(VIN)}$ = 36V, $V_{(VOUT)}$ = 12V I_O = 5A, MODE = VCC2)

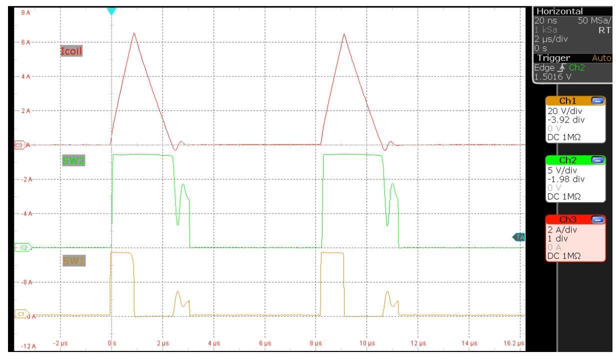


Figure 10-11. Inductor Current Boost Mode ($V_{(VIN)}$ = 5V, $V_{(VOUT)}$ = 12V I_O = 0.05A, MODE = GND)

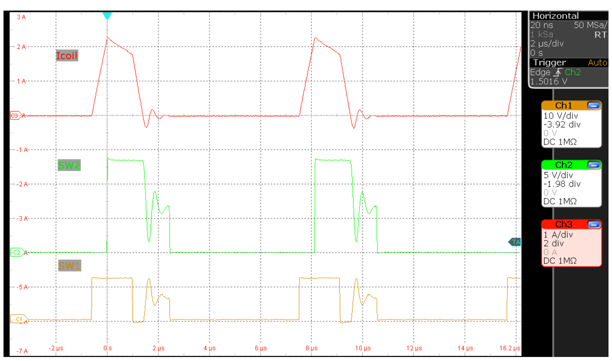


Figure 10-12. Inductor Current Boost Mode ($V_{(VIN)}$ = 12V, $V_{(VOUT)}$ = 12V I_O = 0.05A, MODE = GND)

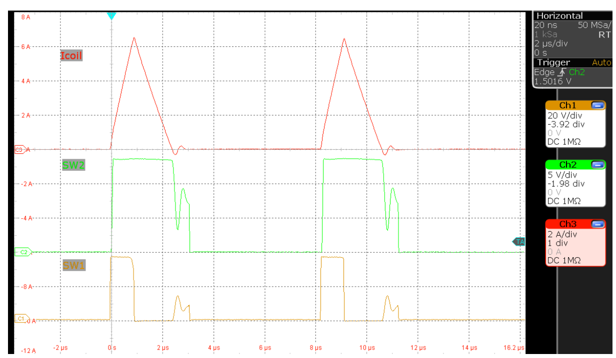


Figure 10-13. Inductor Current Boost Mode ($V_{(VIN)}$ = 36V, $V_{(VOUT)}$ = 12V I_O = 0.05A, MODE = GND)

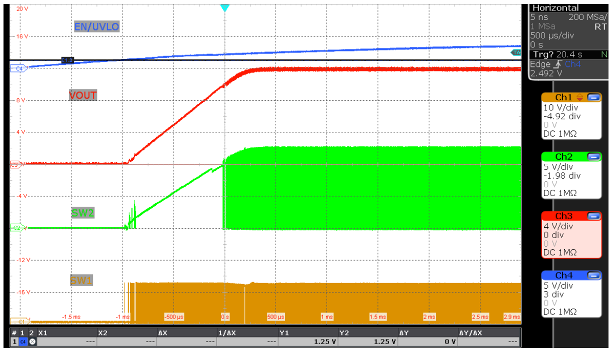


Figure 10-14. Device Start-up , $V_{(VIN)}$ = 12V, $V_{(VOUT)}$ = 12V I_O = 5A, MODE = VCC2)

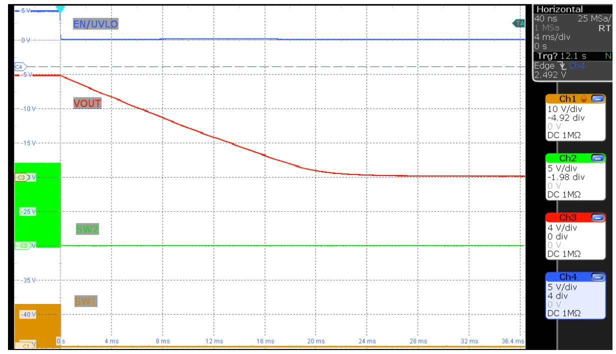


Figure 10-15. Device Shutdown (Discharge Enabled , $V_{(VIN)}$ = 12V, $V_{(VOUT)}$ = 12V I_O = 0A MODE = GND)

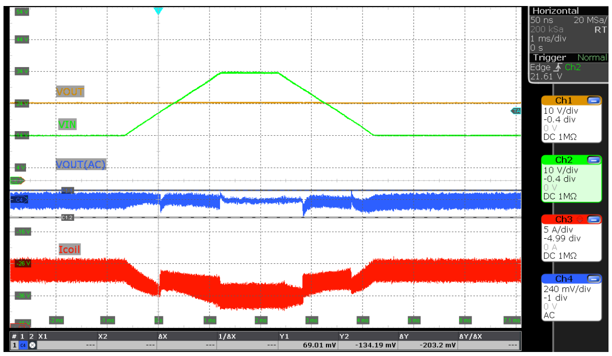


Figure 10-16. Input Voltage Ramp ($V_{(VIN)}$ = 14V ↔ 24V, $V_{(VOUT)}$ = 24V I_O = 5A MODE = GND)

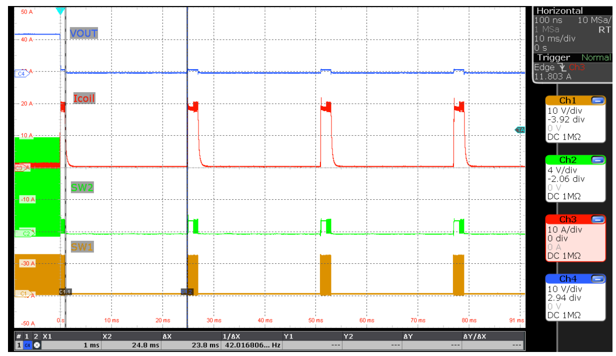


Figure 10-17. SCP-Hiccup protection ($V_{(VIN)}$ = 12V, $V_{(VOUT)}$ = 12V I_O = short, MODE = VCC2)

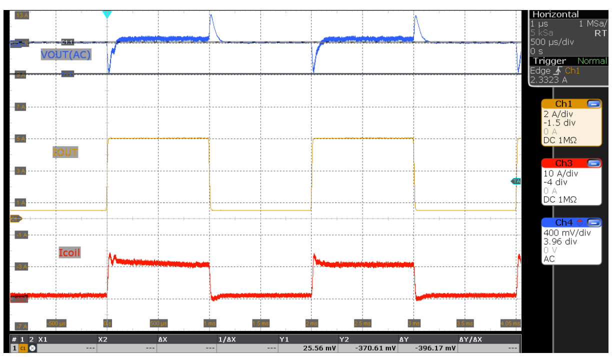


Figure 10-18. Load Transient ($V_{(VIN)}$ = 12V, $V_{(VOUT)}$ = 24V I_O = 0.5A ↔ 5A, MODE = VCC2)

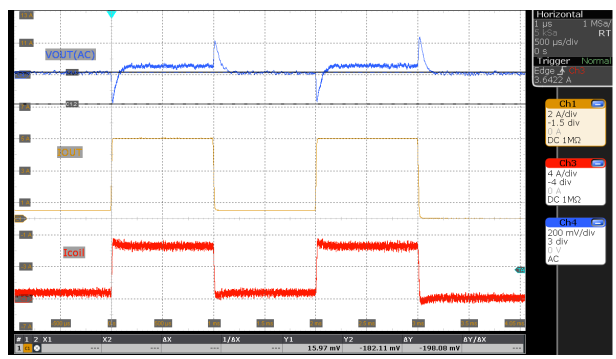


Figure 10-19. Load Transient ($V_{(VIN)}$ = 24V, $V_{(VOUT)}$ = 24V I_O = 0.5A ↔ 5A, MODE = VCC2)

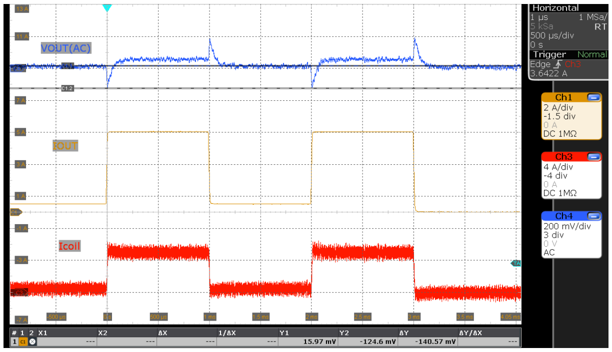


Figure 10-20. Load Transient ($V_{(VIN)}$ = 36V, $V_{(VOUT)}$ = 24V I_O = 0.5A ↔ 5A, MODE = VCC2)

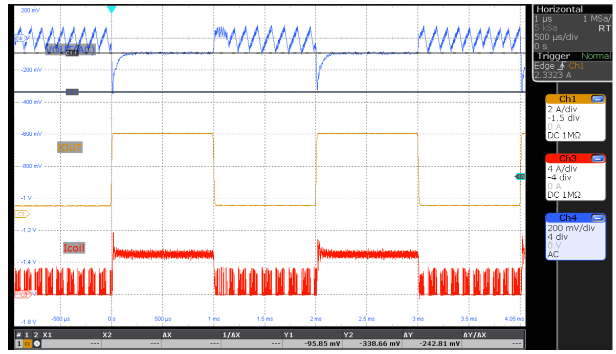


Figure 10-21. Load Transient ($V_{(VIN)}$ = 12V, $V_{(VOUT)}$ = 24V I_O = 0.5A ↔ 5A, MODE = GND)

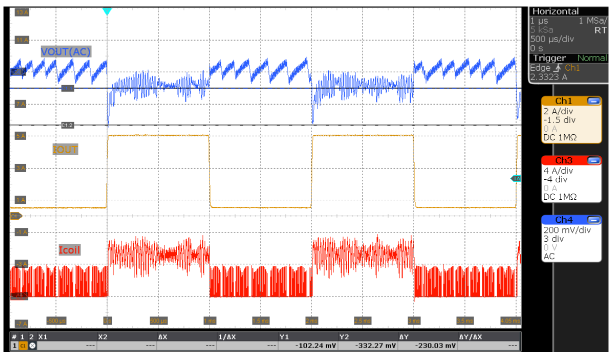


Figure 10-22. Load Transient ($V_{(VIN)}$ = 24V, $V_{(VOUT)}$ = 24V I_O = 0.5A ↔ 5A, MODE = GND)

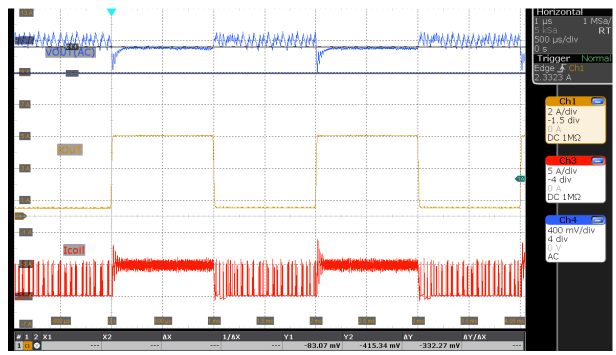


Figure 10-23. Load Transient ($V_{(VIN)}$ = 36V, $V_{(VOUT)}$ = 24V I_O = 0.5A ↔ 5A, MODE = GND)

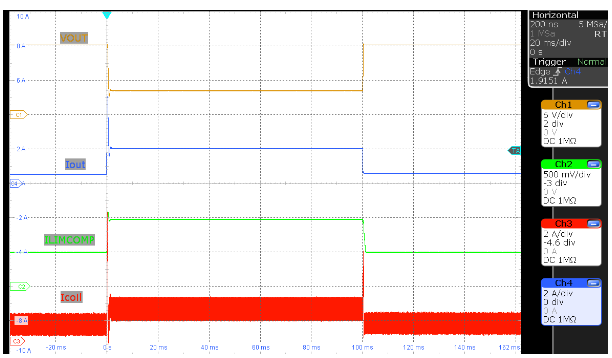


Figure 10-24. Average Output Current Limit ($V_{(VIN)}$ = 12V, $V_{(VOUT)}$ = 12V I_O = 0.5A ↔ 5A, MODE = VCC2, ILIM_THRESHOLD = 0x28 (2A))

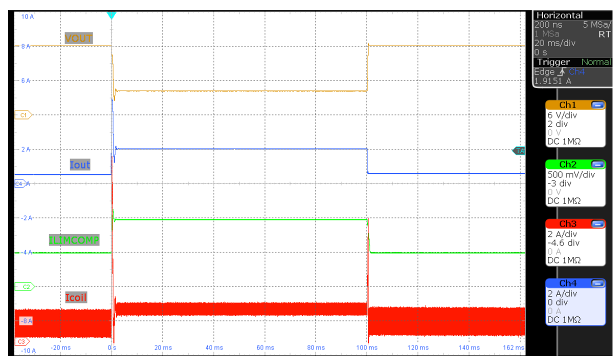


Figure 10-25. Average Output Current Limit ($V_{(VIN)}$ = 6V, $V_{(VOUT)}$ = 12V I_O = 0.5A ↔ 5A, MODE = VCC2, ILIM_THRESHOLD = 0x28 (2A))

10.3 USB-PD Source with Power Path

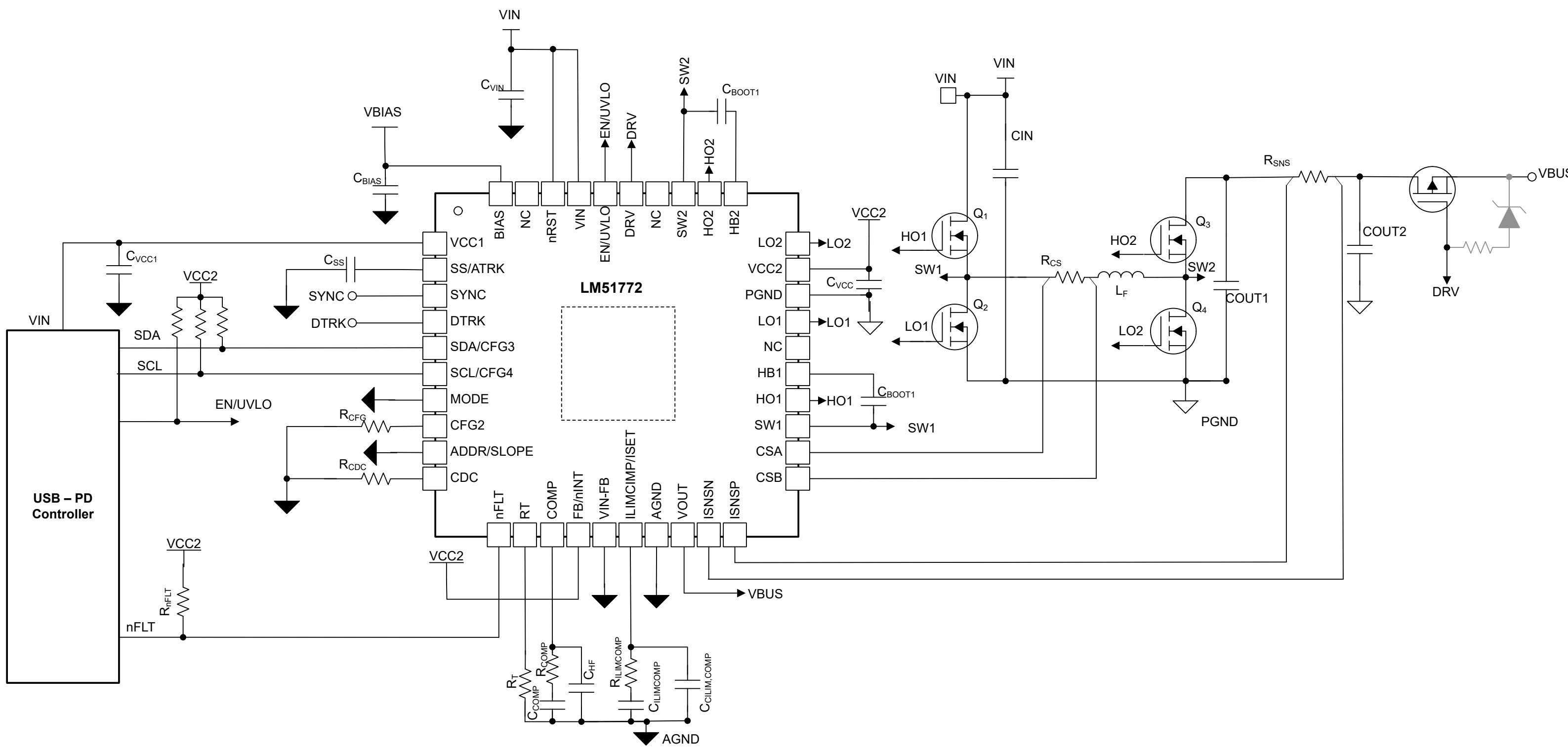


Figure 10-26. Simplified Schematic of USB-PD Source with Power Path

10.4 Parallel (Multiphase) Operation

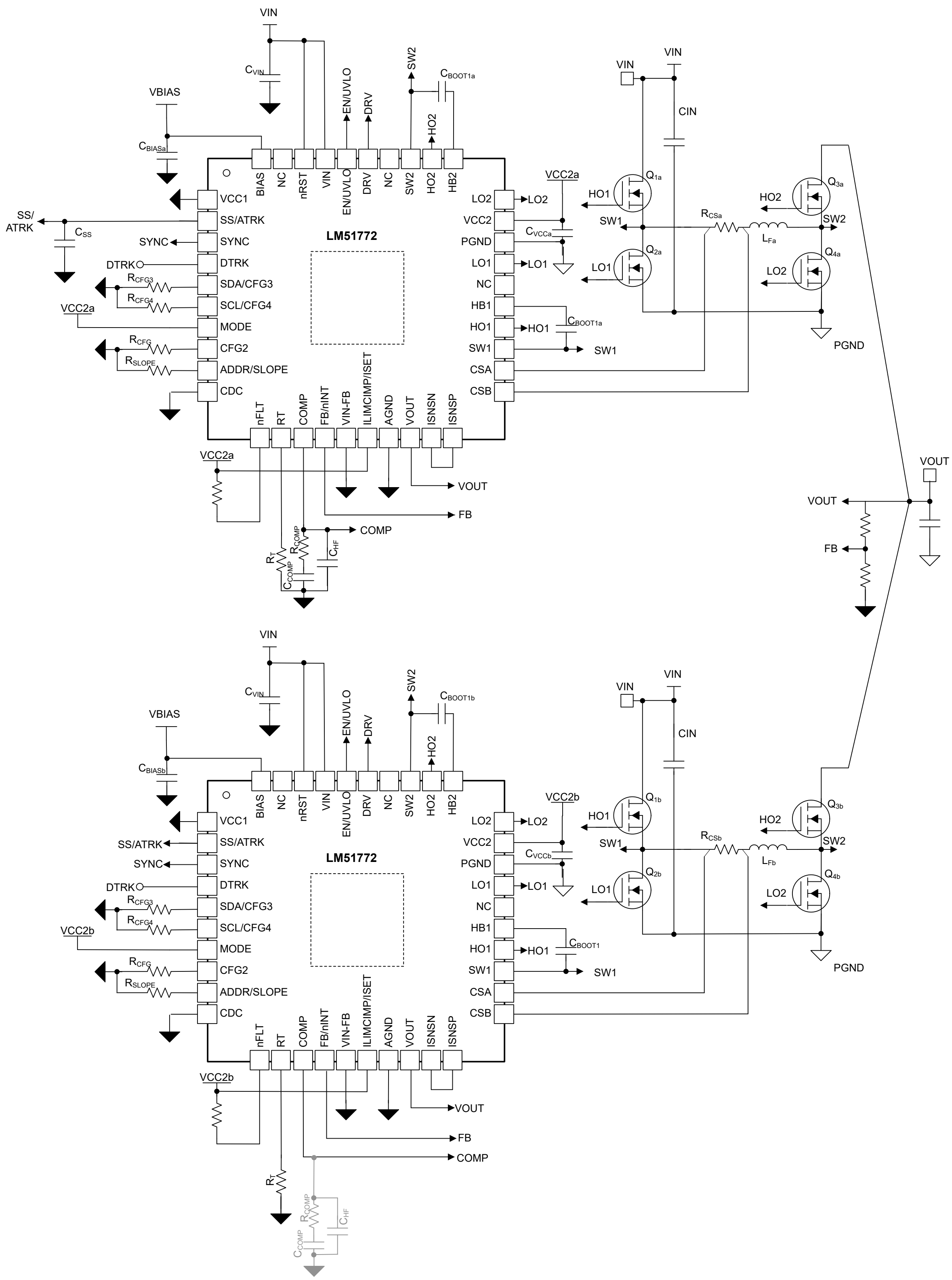


Figure 10-27. Simplified Schematic of a Two phase operation

10.5 Wireless Charging Supply

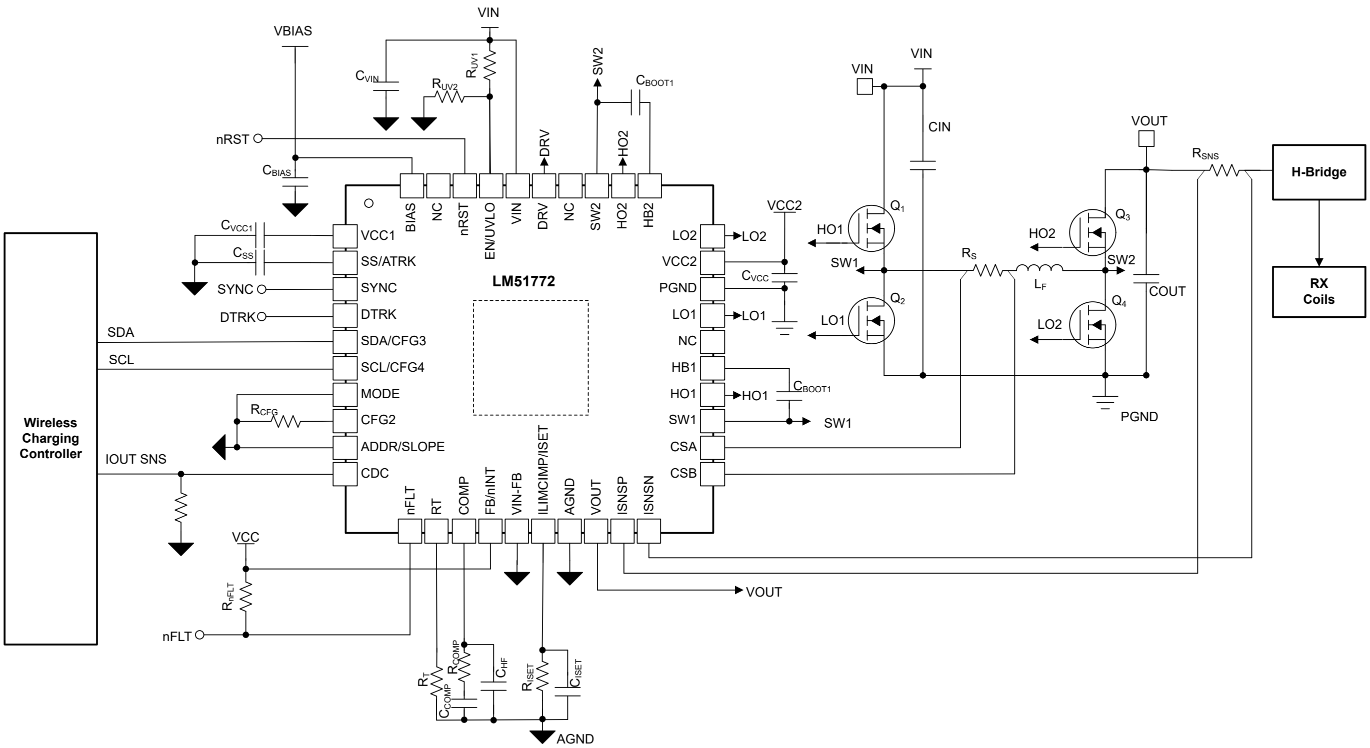


Figure 10-28. Simplified Schematic of a Wireless Charging Supply

10.6 Power Supply Recommendations

The LM251772-Q1 is designed to operate over a wide input voltage range. The device is not allowed to be operated with an input supply, which characteristics are not compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions*. Select, a input supply that is capable of delivering the required input current to the fully loaded regulator. Use Equation 60 to estimate the average input current.

$$I_I = \frac{P_O}{V_I \eta} \quad (60)$$

where

- η the efficiency.

If the device is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables possible have an adverse effect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an under-damped resonant circuit. In some cases this circuit cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. One way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. An EMI input filter is often used in front of the controller power stage. Unless carefully designed, the filter has the potential to lead to instability as well as some of the previously mentioned affects.

10.7 Layout

10.7.1 Layout Guidelines

10.7.1.1 Power Stage Layout

Input capacitors, output capacitors, and MOSFETs are the constituent components of the power stage of the buck-boost regulator and are typically placed on the top side of the PCB. The benefits of convective heat transfer are maximized when leveraging any system-level airflow. In a two-sided PCB layout, small-signal components are typically placed on the bottom side. Insert at least one inner plane, connected to ground, to shield, and isolate the small-signal traces from noisy power traces.

The DC/DC regulator has several high-current loops. Minimize the area of these loops to suppress generated switching noise and optimize switching performance.

- The most important loop areas to minimize are the path from the input capacitors through the buck high-side and low-side MOSFETs, and back to the ground connection of the input capacitor and the path from the output capacitors through the boost high-side and low-side MOSFETs, and back to the ground connection of the output capacitor. Connect the negative terminal of the capacitor close to the source of the low-side MOSFETs (at ground). Similarly, connect the positive terminal of the capacitor or capacitors close to the drain of the high-side MOSFETs of both loops.
- In addition to these recommendation, follow any layout considerations of the MOSFETs as recommended by the MOSFET manufacturer, including pad geometry and solder paste stencil design.

10.7.1.2 Gate Driver Layout

The LM251772-Q1 high-side and low-side gate drivers incorporate short propagation delays, frequency depended dead-time control, and low-impedance output stages capable of delivering large peak currents with very fast rise and fall times to facilitate rapid turn-on and turn-off transitions of the external power MOSFETs. Very high di/dt probably cause unacceptable ringing if the trace lengths are not well controlled. Minimization of stray or parasitic gate loop inductance is key to optimizing gate drive switching performance, whether the inductance is series gate inductance that resonates with MOSFET gate capacitance or common source inductance (common to gate and power loops) that provides a negative feedback component opposing the gate drive command, and thereby increasing MOSFET switching times.

Connections from the gate driver outputs, HO1 and HO2, to the respective gates of the high-side MOSFETs are necessary to be as short as possible to reduce series parasitic inductance. Route HO1 and HO2 and SW1 and SW2 gate traces as a differential pair from the device pin to the high-side MOSFET, taking advantage of flux cancellation by reducing the loop area.

Connections from gate driver outputs, LO1 and LO2, to the respective gates of the low-side MOSFETs are necessary to be as short as possible to reduce series parasitic inductance. Route LO1 and LO2, and PGND traces as a differential pair from the device pin to the low-side MOSFET, taking advantage of flux cancellation by reducing the loop area.

Minimize the current loop path from the VCC, HB1, and HB2 pins through the respective capacitors as these provide the high instantaneous current.

10.7.1.3 Controller Layout

With the provision to locate the controller as close as possible to the power MOSFETs to minimize gate driver trace runs, the components related to the analog and feedback signals as well as current sensing are considered in the following:

- Separate power and signal traces, and use a ground plane to provide noise shielding.
- Place all sensitive analog traces and components related to COMP, FB, SLOPE, SS/ATRK, and RT away from high-voltage switching nodes such as the following to avoid mutual coupling:
  - SW1
  - SW2
  - HO1
  - HO2
  - LO1
  - LO2
  - HB1
  - HB2
- Use an internal layer or layers as ground plane or planes. Pay particular attention to shielding the feedback (FB) trace from power traces and components.
- Route the CSA and CSB and ISNSP and ISNSN traces as differential pairs to minimize noise pickup and use Kelvin connections to the applicable shunt resistor.
- Locate the upper and lower feedback resistors close to the FB pins, keeping the FB traces as short as possible. Route the trace from the upper feedback resistor or resistors to the output voltage sense point.
- Use a common ground node for power ground and a different one for analog ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.
- The HTSSOP package offers a means of removing heat from the semiconductor die through the exposed thermal pad at the base of the package. While the exposed pad of the package is not directly connected to any leads of the package, the package is thermally connected to the substrate (ground) of the device. This connection allows a significant improvement in heat sinking. Designing the PCB with thermal lands, thermal vias, and a ground plane is imperative for completing the heat removal subsystem.

10.7.2 Layout Example

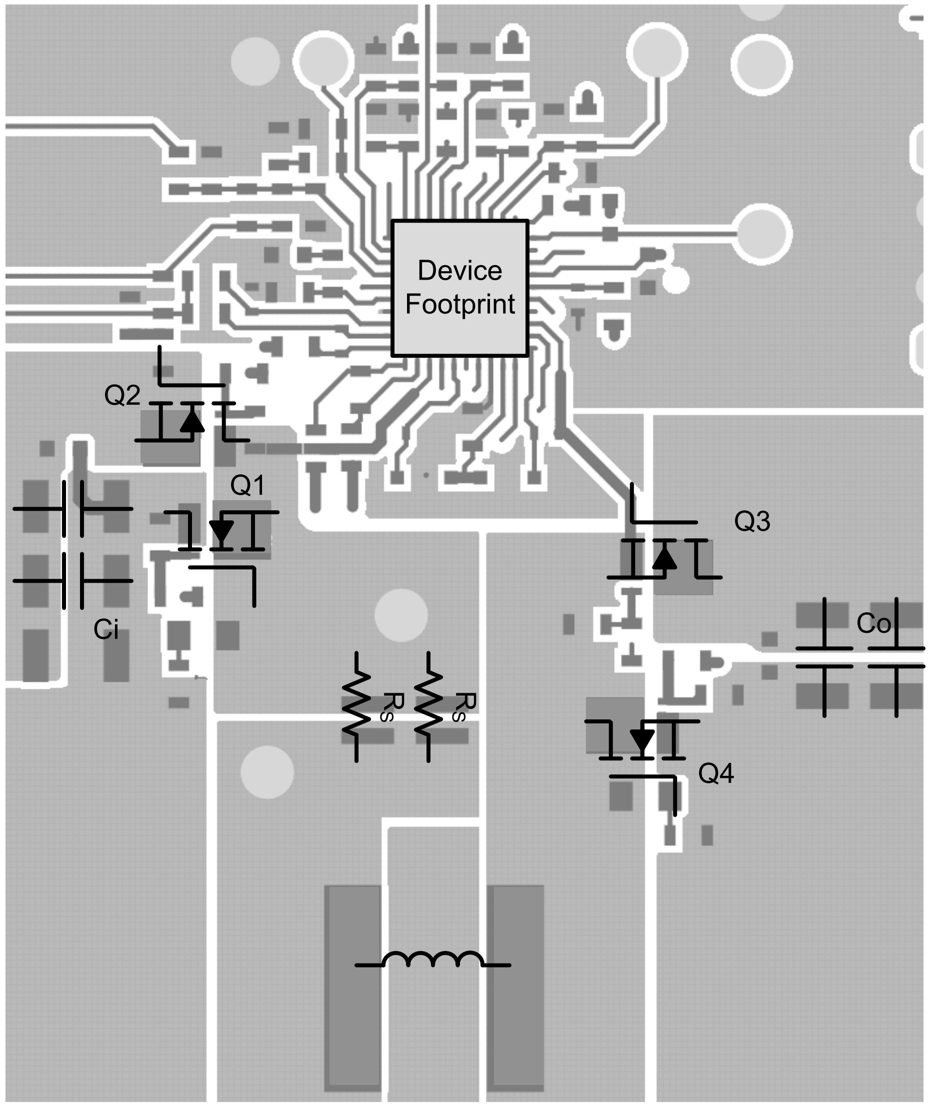


Figure 10-29. LM251772-Q1 Simplified Top Layer Example

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

- Texas Instruments, *LM51772-Q1 and LM251772-Q1 Functional Safety FIT Rate and FMD*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2025	*	Initial Release

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM251772QRHARQ1	Active	Production	VQFN (RHA) | 40	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	LM251772 QRHARQ1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM251772-Q1 :

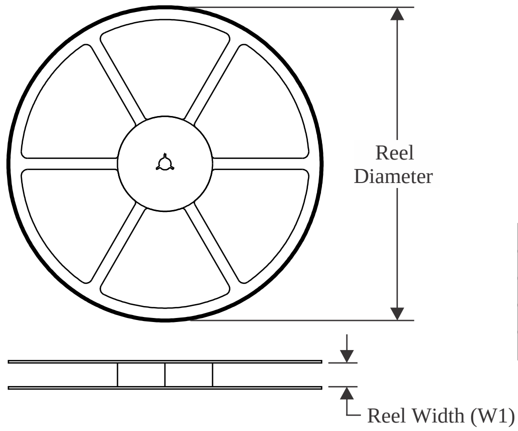
- Catalog : LM251772

NOTE: Qualified Version Definitions:

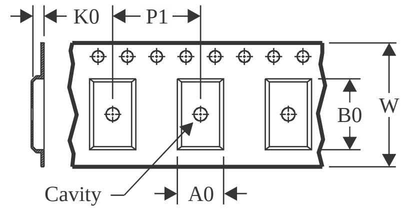
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

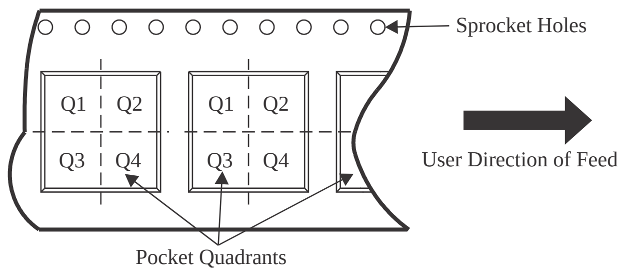


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

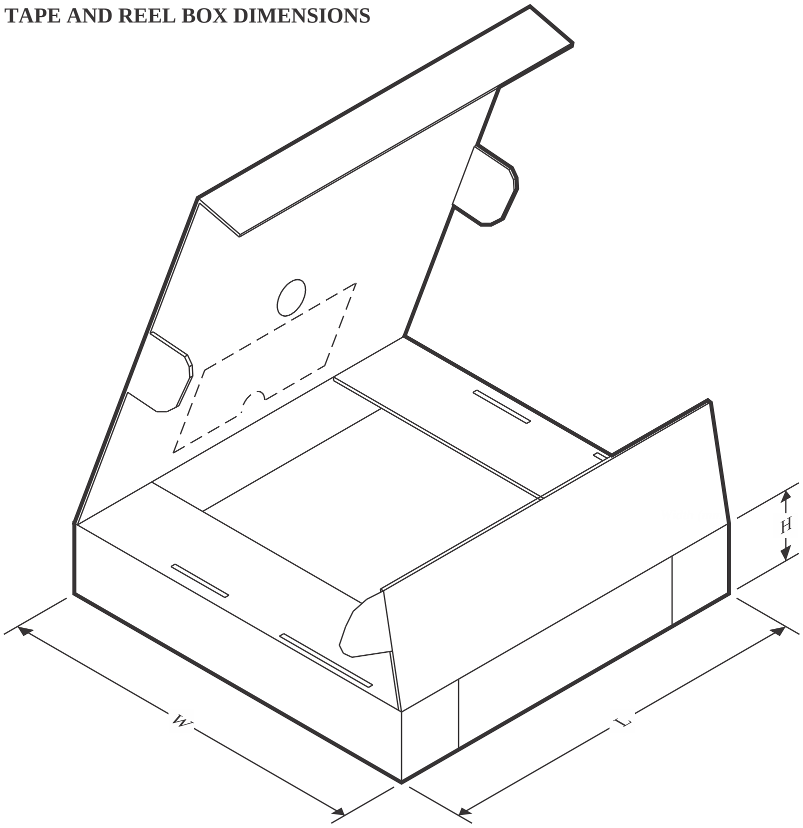
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM251772QRHARQ1	VQFN	RHA	40	4000	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

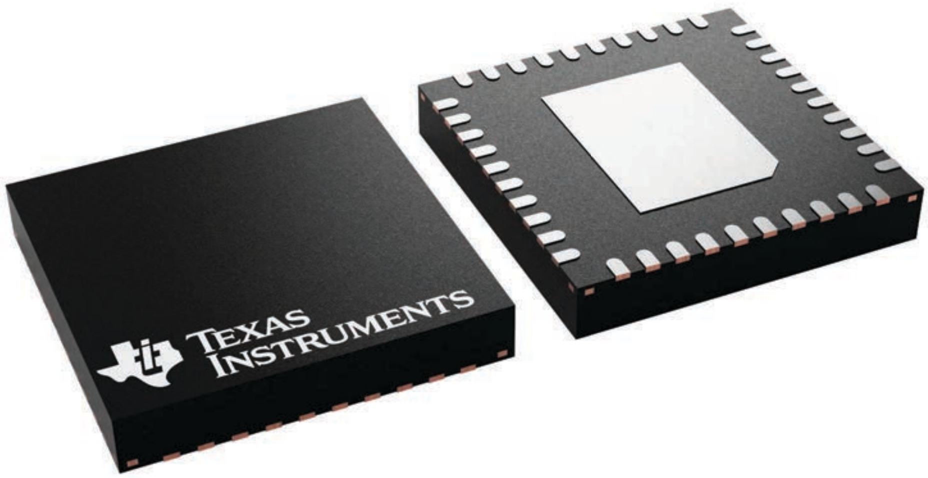
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM251772QRHARQ1	VQFN	RHA	40	4000	360.0	360.0	36.0

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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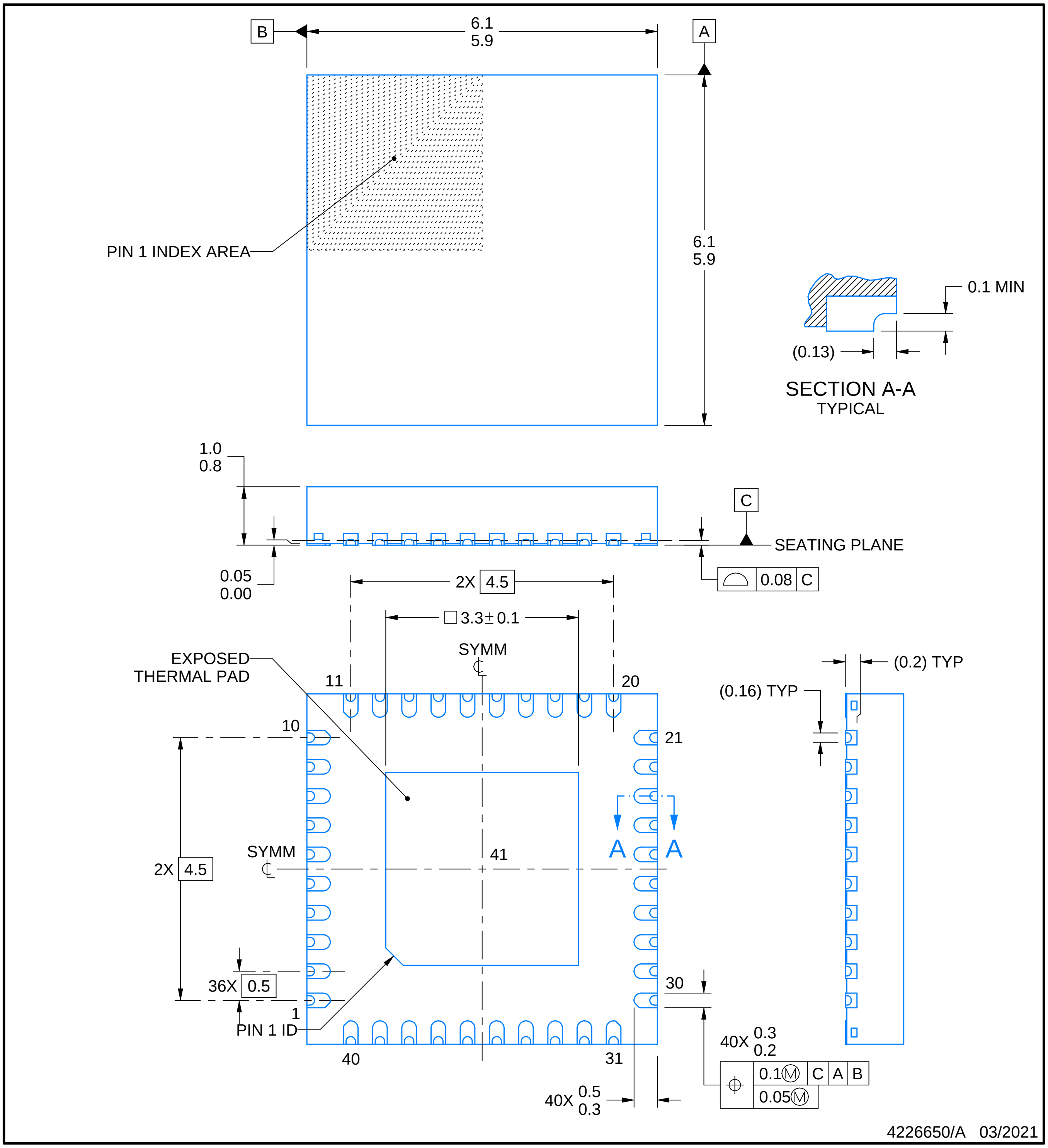
PACKAGE OUTLINE

RHA0040N

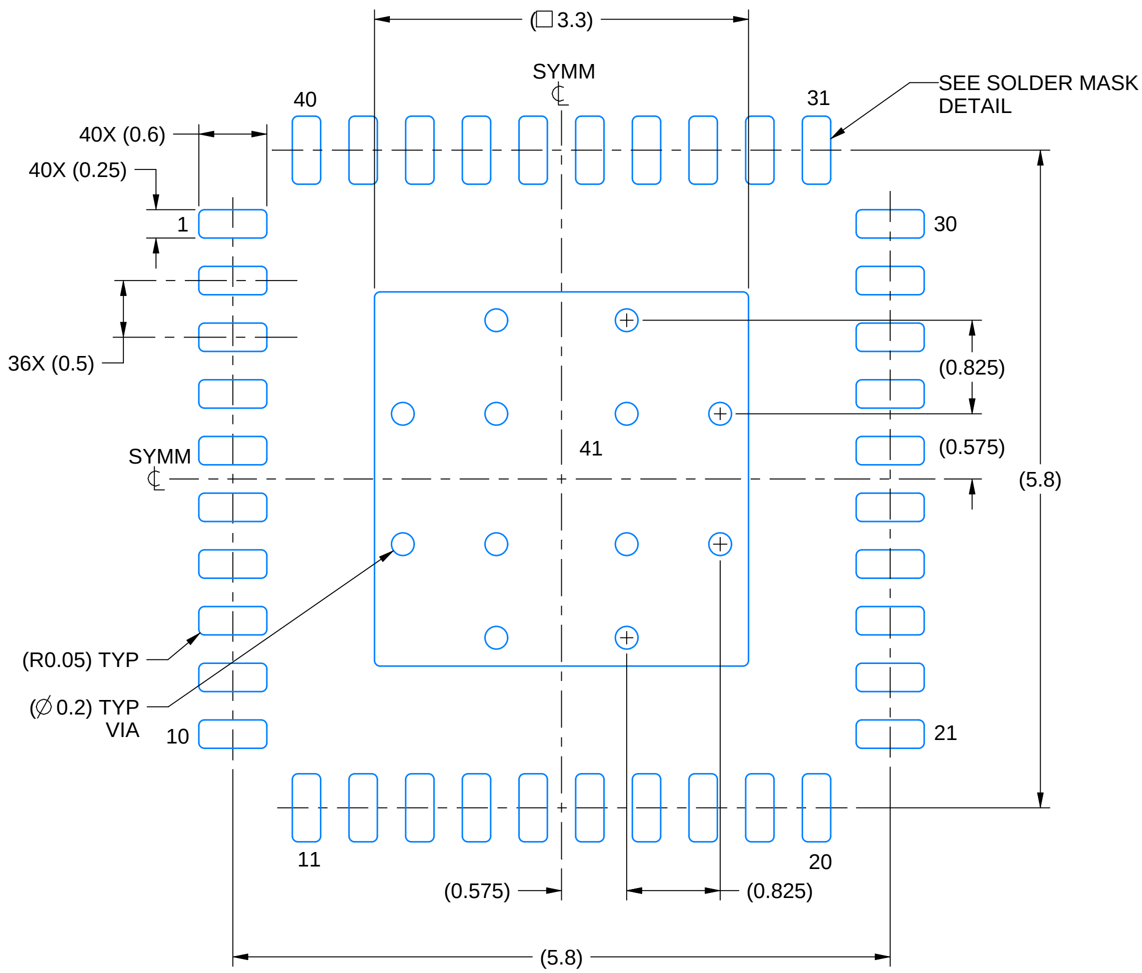
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

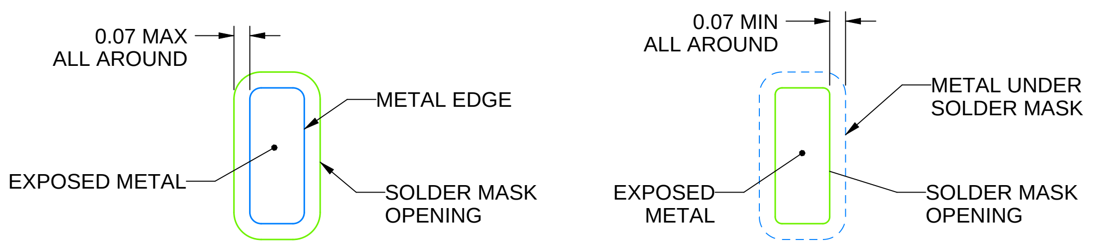


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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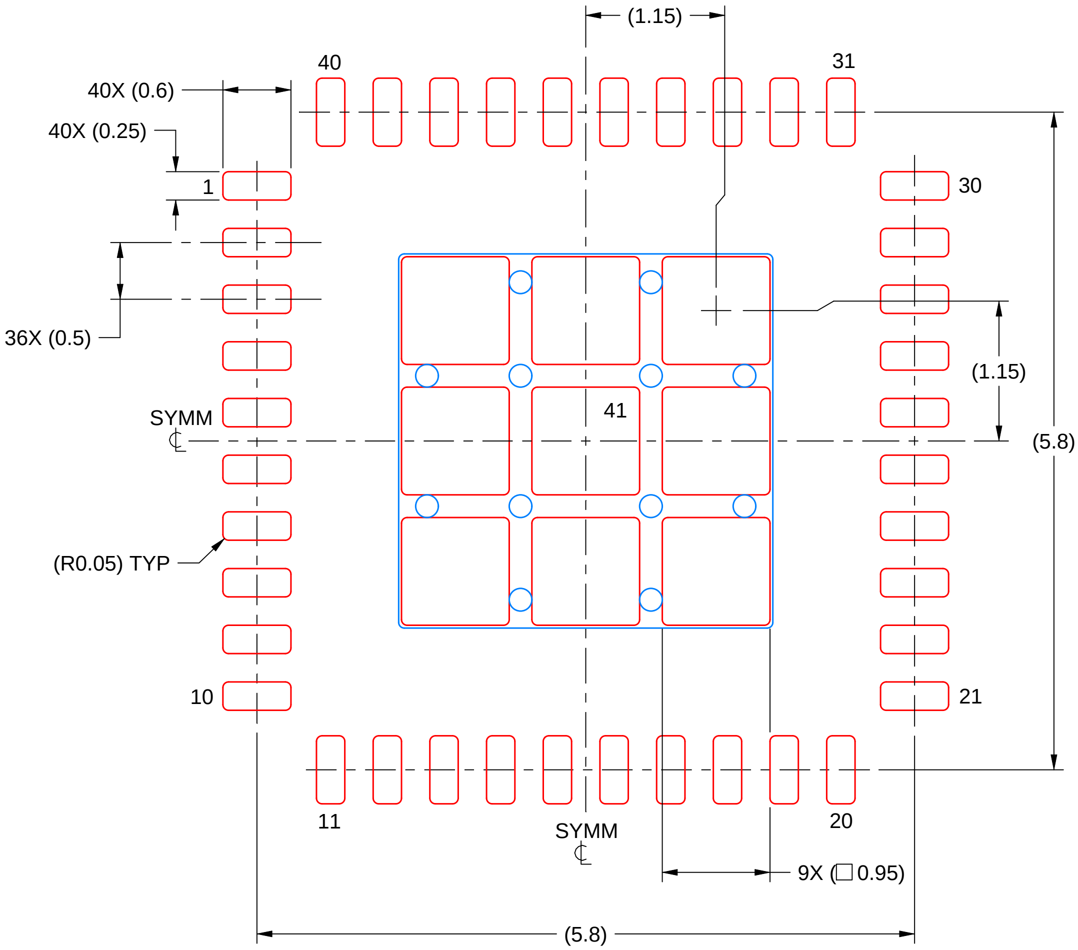
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 41
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.