LM25101 3-A, 2-A, and 1-A 80-V Half-Bridge Gate Drivers

1 Features

- Independent High and Low Driver Logic Inputs
- Bootstrap Supply Voltage up to 100-V DC
- Drives Both a High-Side and Low-Side N-Channel MOSFETs
- Fast Propagation Times (25 ns Typical)
- Drives 1000-pF Load With 8-ns Rise and Fall Times
- Excellent Propagation Delay Matching (3 ns Typical)
- Supply Rail Undervoltage Lockout
- Low Power Consumption
- Pin Compatible With HIP2100 and HIP2101

2 Applications

- Motor-Controlled Drivers
- Half and Full Bridge Power Converters
- Synchronous Buck Converters
- Two Switch Forward Power Converters
- Forward With Active Clamp Converters
- 48-V Server Power
- Solar DC-DC and DC-AC Converters

3 Description

The LM25101 high-voltage gate driver is designed to drive both the high-side and the low-side N-Channel MOSFETs in a synchronous buck or a half-bridge configuration. The A version provides a full 3-A of gate drive while the B and C versions provide 2-A and 1-A, respectively. The outputs are independently controlled with TTL input thresholds. An integrated high voltage diode is provided to charge the high-side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control logic to the high-side gate driver. Undervoltage lockout is provided on both the low-side and the high-side power rails.

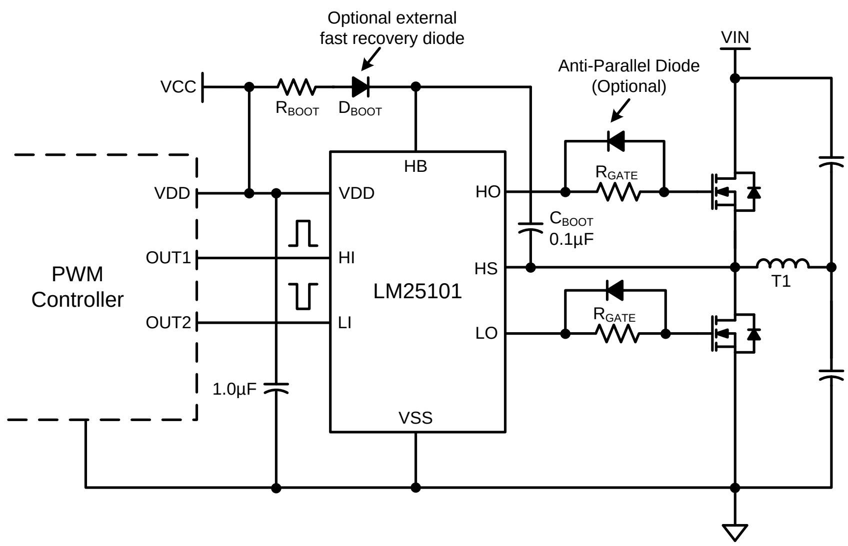
These devices are available in the standard 8-pin SOIC, 8-pin SO-PowerPAD, 8-pin WSON, 10-pin WSON, and 8-pin MSOP PowerPAD packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM25101	MSOP PowerPAD (8)	3 mm × 3 mm
	WSON (8)	4 mm × 4 mm
	WSON (10)	4 mm × 4 mm
	SO PowerPAD (8)	3.9 mm × 4.89 mm
	SOIC (8)	3.91 mm × 4.9 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2013) to Revision C — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1
- Added *Thermal Information* table 5

Changes from Original (March 2013) to Revision A — **Page**

- Changed layout of National Semiconductor Data Sheet to TI format 1

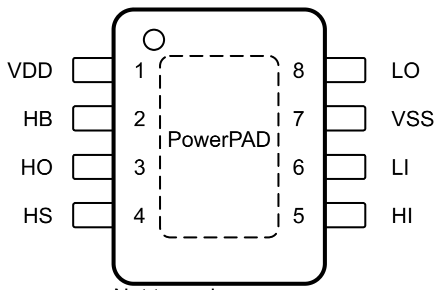
5 Device Options

Table 1. Input/Output Options

Part Number	Input Thresholds	Peak Output Current
LM25101A	TTL	3 A
LM25101B	TTL	2 A
LM25101C	TTL	1 A

6 Pin Configuration and Functions

DGN and DDA Packages
8-Pin MSOP and SO PowerPAD
Top View



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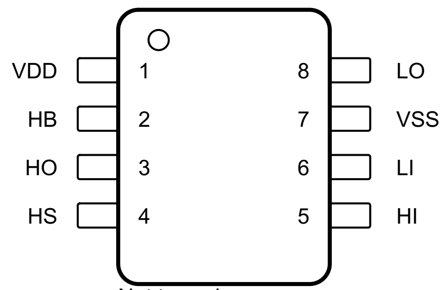
D Package
8-Pin SOIC
Top View



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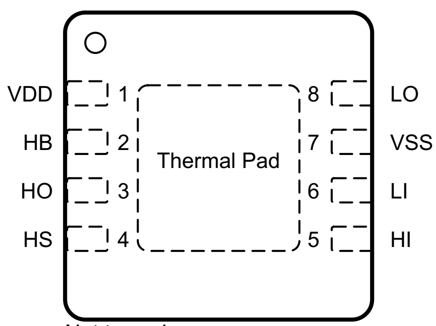
NGT Package
8-Pin WSON
Top View



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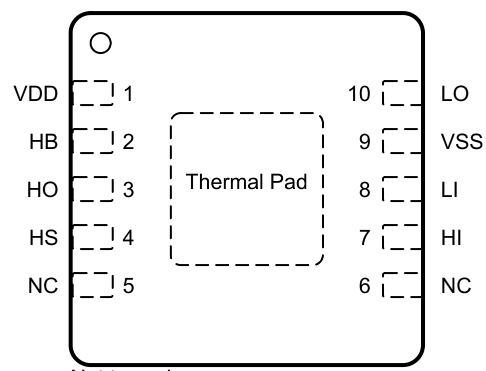
DPR Package
10-Pin WSON
Top View



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Pin Functions

PIN						TYPE	DESCRIPTION
NAME	MSOP PowerPAD	WSON (8)	WSON (10)	SO PowerPAD	SOIC		
HB	2	2	2	2	2	PWR	High-side gate driver bootstrap rail. Connect the positive terminal of the bootstrap capacitor to HB and the negative terminal to HS. The bootstrap capacitor should be placed as close to the IC as possible.
HI	5	5	7	5	5	I	High-side driver control input. The LM25101 inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
HO	3	3	3	3	3	O	High-side gate driver output. Connect to the gate of high-side MOSFET with a short, low inductance path.
HS	4	4	4	4	4	GND	High-side MOSFET source connection. Connect to the bootstrap capacitor negative terminal and the source of the high-side MOSFET.
LI	6	6	8	6	6	I	Low-side driver control input. The LM25101 inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
LO	8	8	10	8	8	O	Low-side gate driver output. Connect to the gate of the low-side MOSFET with a short, low inductance path.
NC	—	—	5, 6	—	—	—	No connection
VDD	1	1	1	1	1	PWR	Positive gate drive supply. Locally decouple to VSS using a low ESR and ESL capacitor located as close to the IC as possible.
VSS	7	7	9	7	7	GND	Ground return. All signals are referenced to this ground.
Thermal Pad	PowerPAD	Thermal Pad	Thermal Pad	PowerPAD	—	—	Solder to the ground plane under the IC to aid in heat dissipation.[1]

(1) TI recommends that the exposed thermal pad on the bottom of the applicable packages is soldered to ground plane of the PCB, and the ground plane should extend out from beneath the IC to help dissipate heat.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
VDD to VSS	−0.3	18	V
HB to HS	−0.3	18	V
LI or HI Input	−0.3	V_{DD} + 0.3	V
LO Output	−0.3	V_{DD} + 0.3	V
HO Output	V_{HS} - 0.3	V_{HB} + 0.3	V
HS to VSS[2]	–5	100	V
HB to VSS		100	V
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. For performance limits and associated test conditions, see the *Electrical Characteristics* tables.

(2) In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS node will generally not exceed –1 V. However, in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur, the HS voltage must never be more negative than V_{DD} – 15 V. For example, if V_{DD} = 10 V, the negative transients at HS must not exceed –5 V.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	All pins except 2, 3, and 4	±2000	V
			Pins 2, 3, and 4	±1000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 [2]		±250	
		Machine model (MM)		±100	

(1) The Human Body Model (HBM) is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage	VDD	9	14	V
V_{HS}	Voltage	HS	–1	100 – V_{DD}	V
V_{HB}	Voltage	HB	V_{HS} + 8	V_{HS} + 14	V
	HS slew rate			50	V/ns
T_J	Junction temperature		–40	125	°C

7.4 Thermal Information

THERMAL METRIC [1]		LM25101A, LM25101B				LM25101C			UNIT
		D (SOIC)	DDA (SO PowerPAD)	NGT (WSON)	DPR (WSON)	D (SOIC)	DPR (WSON)	DGN (MSOP PowerPAD)	
		8 PINS	8 PINS	8 PINS	10 PINS	8 PINS	10 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.2	46.1	38.2	37.8	111.5	39.8	54.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.6	53.5	36.3	35.8	54.2	39.1	55.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.1	13.8	15.2	15.0	52.3	17.1	15.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.6	4.2	0.3	0.3	9.0	0.4	2.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.5	13.9	15.4	15.3	51.7	17.3	15.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	3.9	4.5	4.4	—	6.1	4.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Typical values apply for T_J = 25°C only. Minimum and maximum limits apply for T_J= –40°C to 125°C.(1) Unless otherwise specified, V_{DD} = V_{HB} = 12 V, V_{SS} = V_{HS} = 0 V, No Load on LO or HO.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENTS							
I_{DD}	VDD quiescent current	V_{LI} = V_{HI} = 0 V			0.25	0.4	mA
I_{DDO}	VDD operating current	f = 500 kHz			2.0	3	mA
I_{HB}	Total HB quiescent current	V_{LI} = V_{HI} = 0 V			0.06	0.2	mA
I_{HBO}	Total HB operating current	f = 500 kHz			1.6	3	mA
I_{HBS}	HB to VSS current (quiescent)	V_{HS} = V_{HB} = 100 V			0.1	10	µA
I_{HBSO}	HB to VSS current (operating)	f = 500 kHz			0.4		mA
INPUT PINS							
V_{IL}	Input voltage threshold	Rising Edge		1.3	1.8	2.3	V
V_{IHYS}	Input voltage hysteresis				50		mV
R_I	Input pulldown resistance			100	200	400	kΩ
UNDER VOLTAGE PROTECTION							
V_{DDR}	VDD rising threshold			6.0	6.9	7.4	V
V_{DDH}	VDD threshold hysteresis				0.5		V
V_{HBR}	HB rising threshold			5.7	6.6	7.1	V
V_{HBH}	HB threshold hysteresis				0.4		V
BOOT STRAP DIODE							
V_{DL}	Low-current forward voltage	I_{VDD-HB} = 100 µA			0.52	0.85	V
V_{DH}	High-current forward voltage	I_{VDD-HB} = 100 mA			0.8	1	V
RD	Dynamic resistance	I_{VDD-HB} = 100 mA			1.0	1.65	Ω
LO AND HO GATE DRIVER							
V_{OL}	Low-level output voltage	I_{HO} = I_{LO} = 100 mA	A version		0.12	0.25	V
			B version		0.16	0.4	
			C version		0.28	0.65	
V_{OH}	High-level output voltage	I_{HO} = I_{LO} = 100 mA V_{OH} = V_{DD} – V_{LO} or V_{OH} = V_{HB} – V_{HO}	A version		0.24	0.45	V
			B version		0.28	0.60	
			C version		0.60	1.10	
I_{OHL}	Peak pullup current	HO, V_{LO} = 0 V	A version		3		A
			B version		2		
			C version		1		
I_{OLL}	Peak pulldown current	HO, V_{LO} = 12 V	A version		3		A
			B version		2		
			C version		1		

(1) Minimum and maximum limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

7.6 Switching Characteristics

Typical values apply for T_J = 25°C only. Minimum and maximum limits apply for T_J= –40°C to 125°C.(1) Unless otherwise specified, V_{DD} = V_{HB} = 12 V, V_{SS} = V_{HS} = 0 V, No Load on LO or HO.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{LPHL}	LO turnoff propagation delay	LI falling to LO falling			22	56	ns
t_{LPLH}	LO turnon propagation delay	LI rising to LO rising			26	56	ns
t_{HPHL}	HO turnoff propagation delay	HI falling to HO falling			22	56	ns
t_{HPLH}	LO turnon propagation delay	HI rising to HO rising			26	56	ns
t_{MON}	Delay matching	LO ON and HO OFF			4	10	ns
t_{MOFF}	Delay matching	LO OFF and HO ON			4	10	ns
t_{RC}, t_{FC}	Either output rise and fall time	C_L = 1000 pF			8		ns
t_R	Output rise time (3 V to 9 V)	C_L = 0.1 µF	A version		430		ns
			B version		570		
			C version		990		
t_F	Output fall time (3 V to 9 V)	C_L = 0.1 µF	A version		260		ns
			B version		430		
			C version		715		
t_{PW}	Minimum input pulse duration that changes the output				50		ns
t_{BS}	Bootstrap diode reverse recovery time	I_F = 100 mA, I_R = 100 mA			37		ns

(1) Minimum and maximum limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

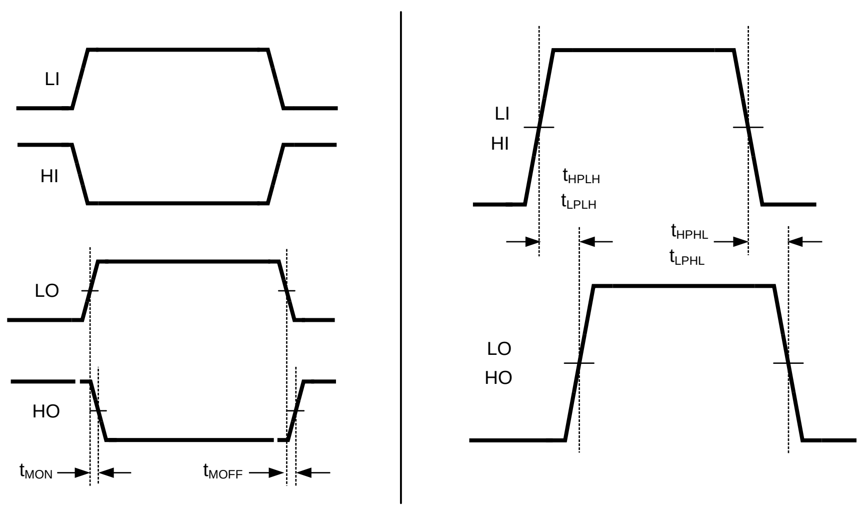


Figure 1. Timing Diagram

7.7 Typical Characteristics

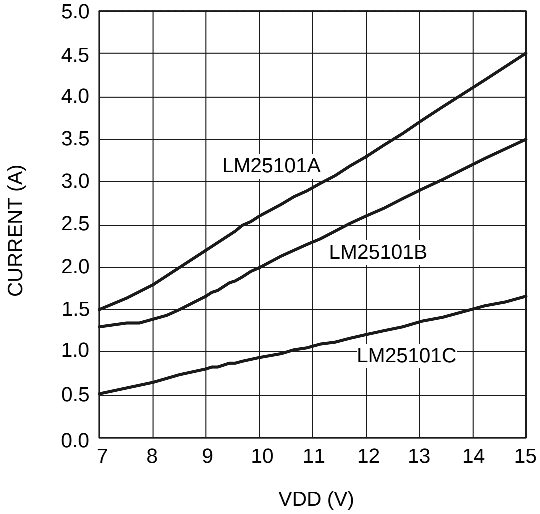


Figure 2. Peak Sourcing Current vs Supply Voltage

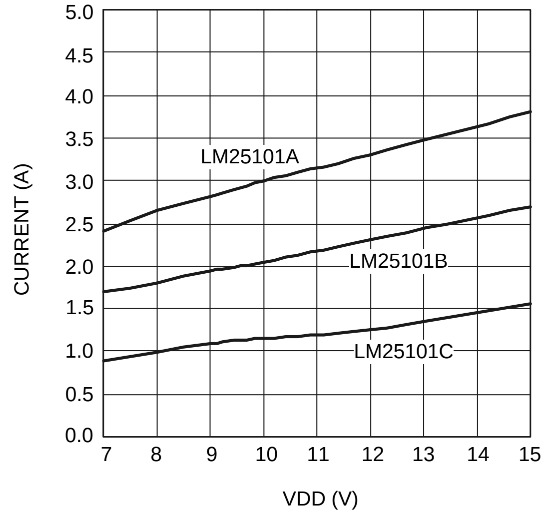


Figure 3. Peak Sinking Current vs Supply Voltage

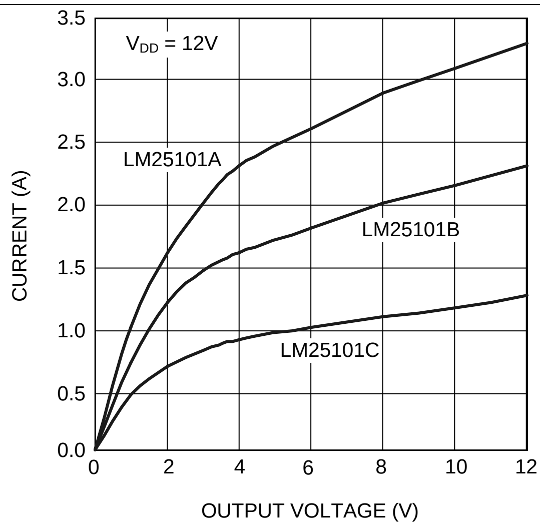


Figure 4. Sink Current vs Output Voltage

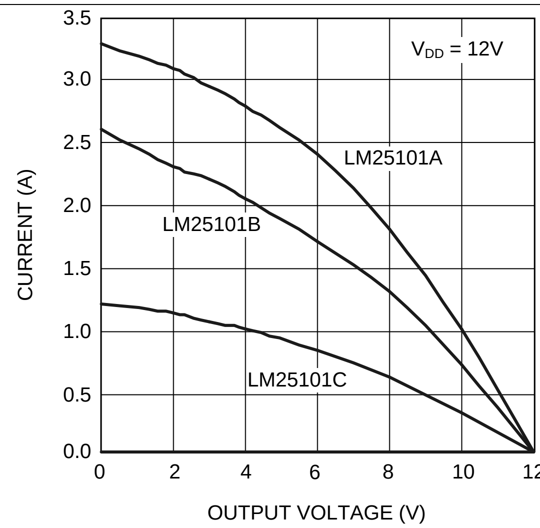


Figure 5. Source Current vs Output Voltage

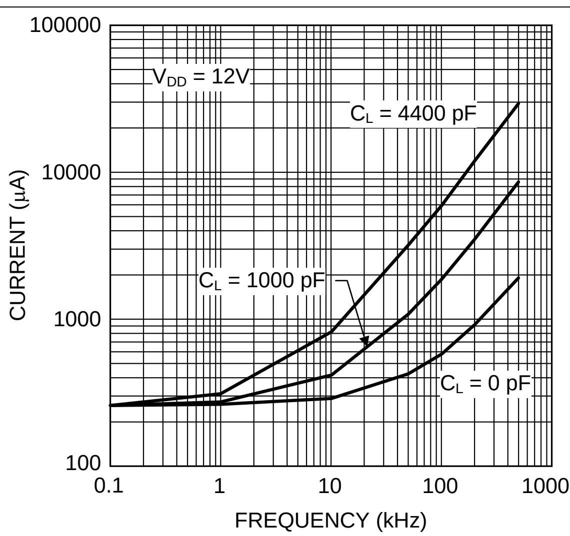


Figure 6. I_{DD} vs Frequency

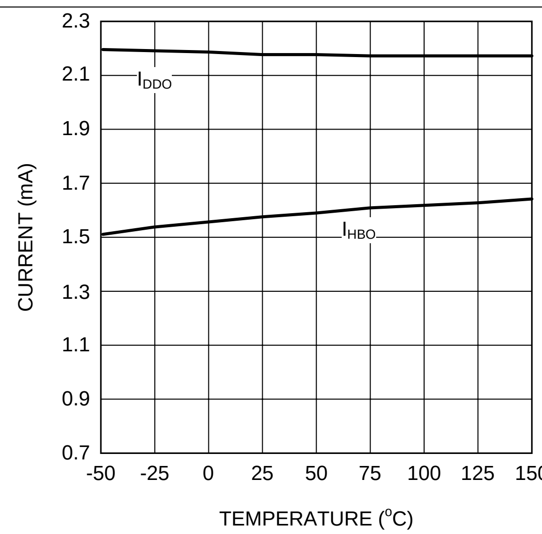


Figure 7. Operating Current vs Temperature

Typical Characteristics (continued)

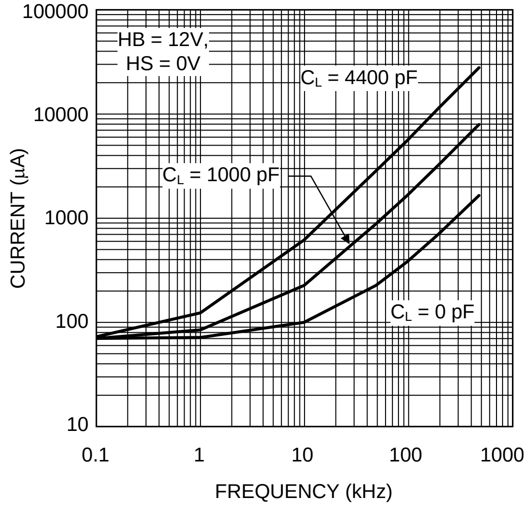


Figure 8. I_{HB} vs Frequency

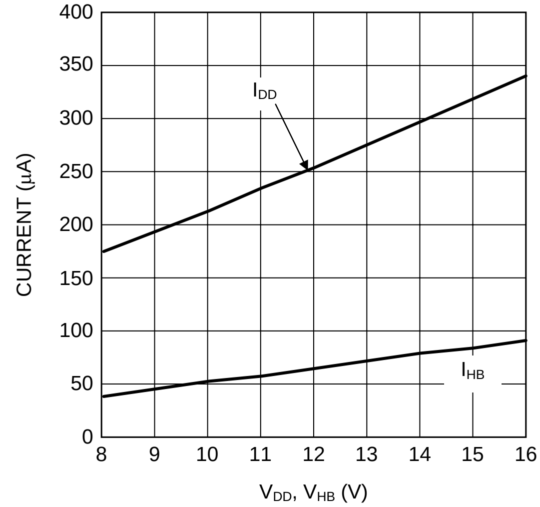


Figure 9. Quiescent Current vs Supply Voltage

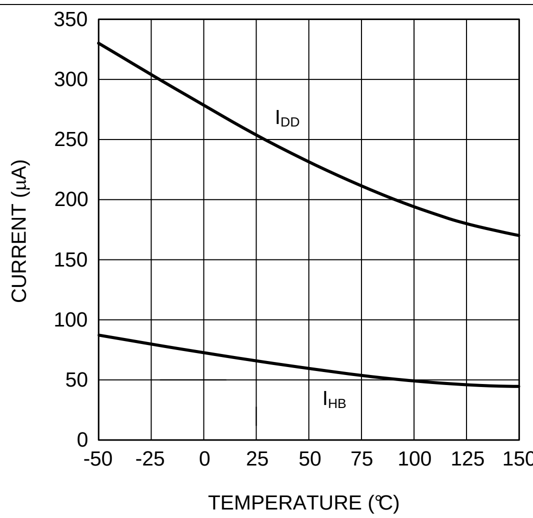


Figure 10. Quiescent Current vs Temperature

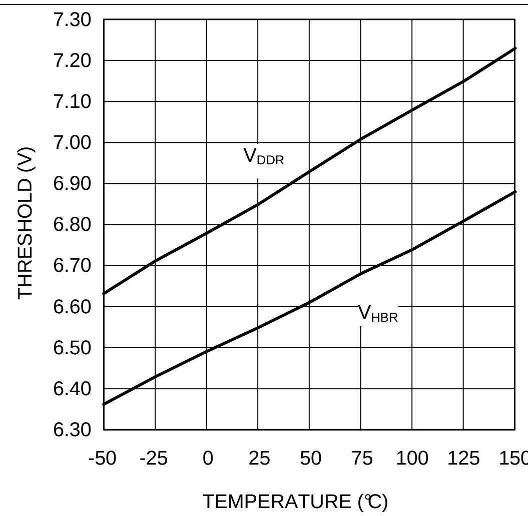


Figure 11. Undervoltage Rising Thresholds vs Temperature

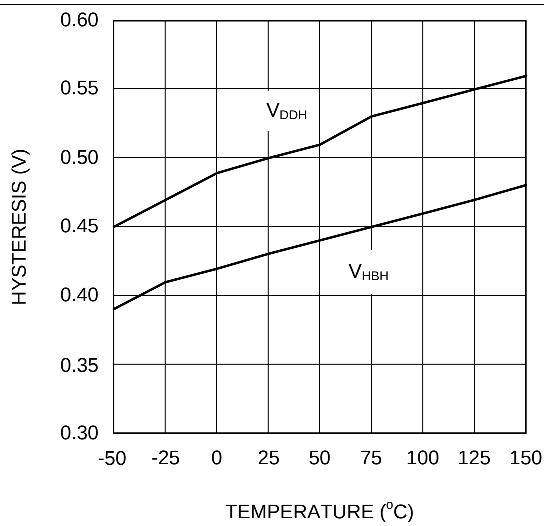


Figure 12. Undervoltage Threshold Hysteresis vs Temperature

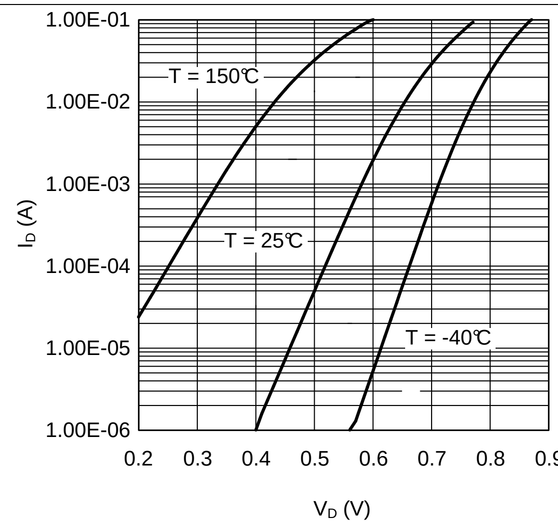


Figure 13. Bootstrap Diode Forward Voltage

Typical Characteristics (continued)

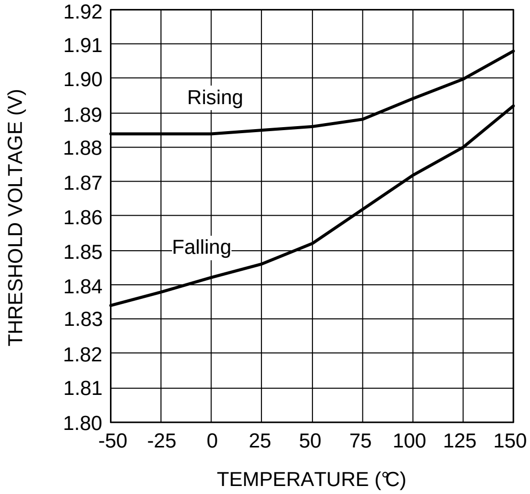


Figure 14. Input Threshold vs Temperature

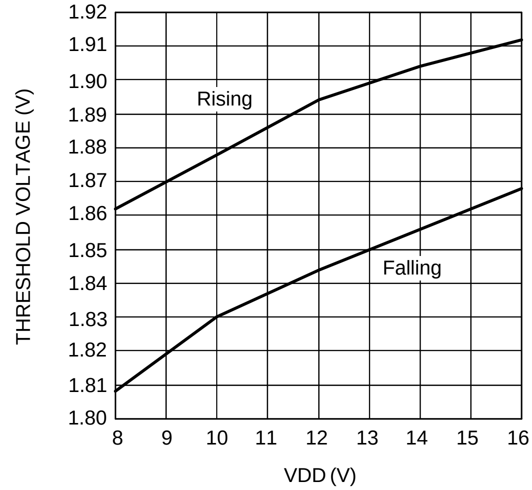


Figure 15. Input Threshold vs Supply Voltage

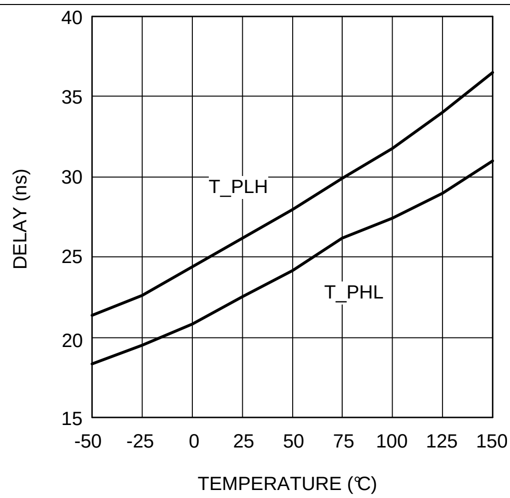


Figure 16. Propagation Delay vs Temperature

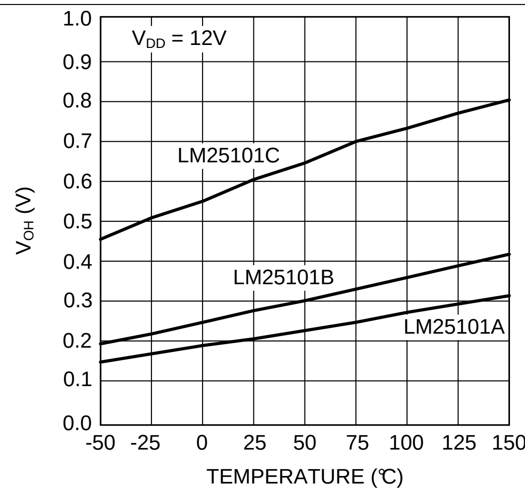


Figure 17. LO and HO Gate Drive: High Level Output Voltage vs Temperature

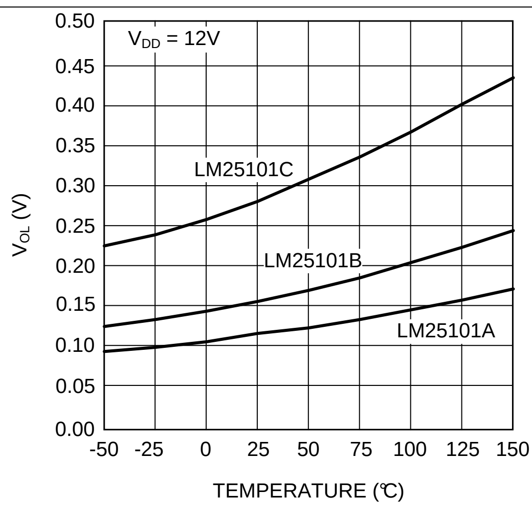


Figure 18. LO and HO Gate Drive: Low Level Output Voltage vs Temperature

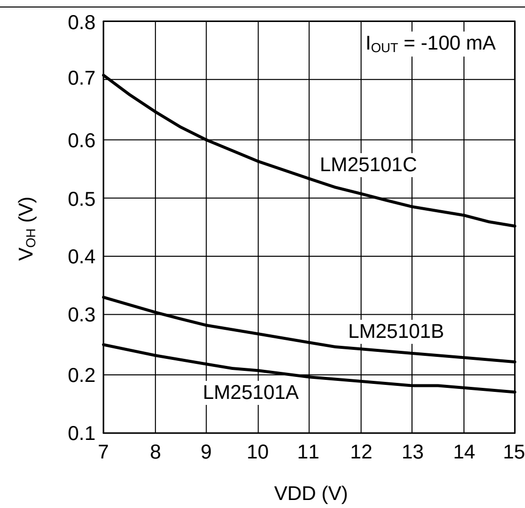


Figure 19. LO and HO Gate Drive: Output High Voltage vs Supply Voltage

Typical Characteristics (continued)

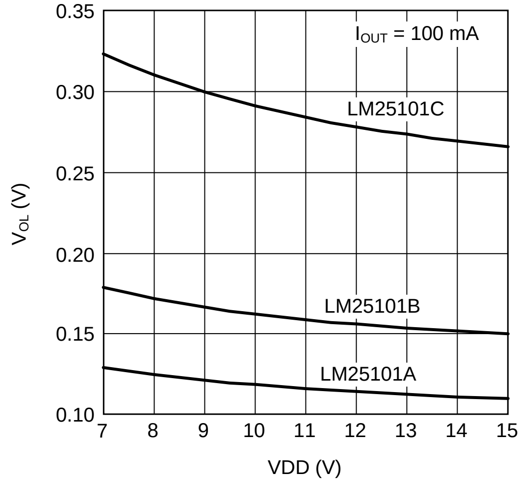


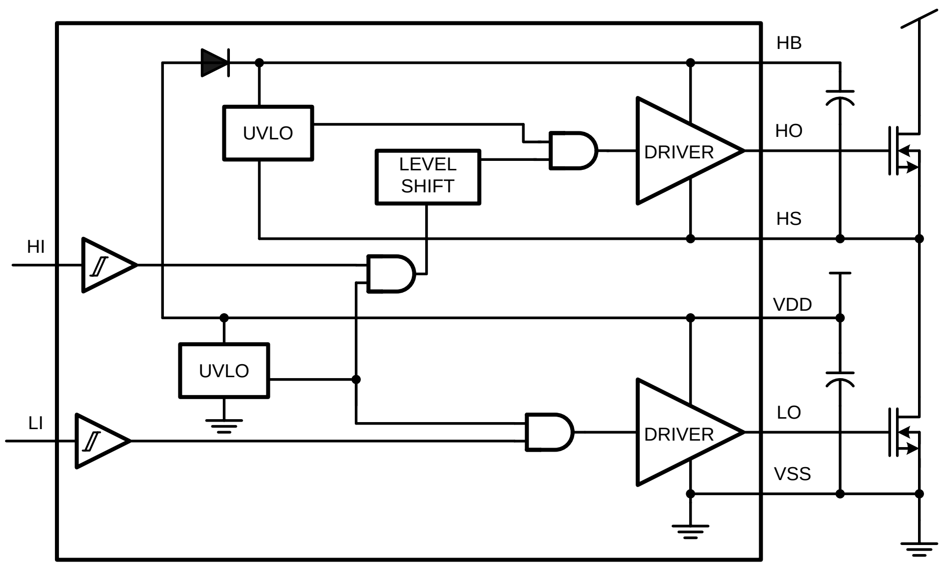
Figure 20. LO and HO Gate Drive: Output Low Voltage vs Supply Voltage

8 Detailed Description

8.1 Overview

To operate fast switching of power MOSFETs at high switching frequencies and to reduce associated switching losses, a powerful gate driver is employed between the PWM output of controller and the gates of the power semiconductor devices. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3 V logic signal which cannot effectively turn on a power switch. Level shift circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN or PNP bipolar transistors in totem-pole arrangement prove inadequate with digital power because they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise (by placing the high-current driver IC physically close to the power switch), driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Start-Up and UVLO

Both top and bottom drivers include UVLO protection circuitry which monitors the supply voltage (V_{DD}) and bootstrap capacitor voltage (V_{HB-HS}) independently. The UVLO circuit inhibits each output until sufficient supply voltage is available to turn on the external MOSFETs, and the built-in UVLO hysteresis prevents chattering during supply voltage variations. When the supply voltage is applied to the VDD pin of the LM25101, the top and bottom gates are held low until V_{DD} exceeds the UVLO threshold, typically about 6.9 V. Any UVLO condition on the bootstrap capacitor (V_{HB-HS}) will only disable the high-side output (HO).

Table 2. VDD UVLO Feature Logic Operation

CONDITION (1)	HI	LI	HO	LO
$V_{DD} - V_{SS} < V_{DDR}$ during device start-up	H	L	L	L
$V_{DD} - V_{SS} < V_{DDR}$ during device start-up	L	H	L	L
$V_{DD} - V_{SS} < V_{DDR}$ during device start-up	H	H	L	L
$V_{DD} - V_{SS} < V_{DDR}$ during device start-up	L	L	L	L
$V_{DD} - V_{SS} < V_{DDR} - V_{DDH}$ after device start-up	H	L	L	L
$V_{DD} - V_{SS} < V_{DDR} - V_{DDH}$ after device start-up	L	H	L	L
$V_{DD} - V_{SS} < V_{DDR} - V_{DDH}$ after device start-up	H	H	L	L
$V_{DD} - V_{SS} < V_{DDR} - V_{DDH}$ after device start-up	L	L	L	L

(1) $V_{HB\text{-}HS} > V_{HBR}$

Table 3. VHB-HS UVLO Feature Logic Operation

CONDITION (1)	HI	LI	HO	LO
$V_{HB\rightarrow HS} < V_{HBR}$ during device start-up	H	L	L	L
$V_{HB-HS} < V_{HBR}$ during device start-up	L	H	L	H
$V_{HB-HS} < V_{HBR}$ during device start-up	H	H	L	H
$V_{HB-HS} < V_{HBR}$ during device start-up	L	L	L	L
$V_{HB-HS} < V_{HBR} - V_{HBH}$ after device start-up	H	L	L	L
$V_{HB-HS} < V_{HBR} - V_{HBH}$ after device start-up	L	H	L	H
$V_{HB-HS} < V_{HBR} - V_{HBH}$ after device start-up	H	H	L	H
$V_{HB-HS} < V_{HBR} - V_{HBH}$ after device start-up	L	L	L	L

(1) $V_{DD}>V_{DDR}$

8.3.2 Level Shift

The level shift circuit is the interface from the high-side input to the high-side driver stage which is referenced to the switch node (HS). The level shift allows control of the HO output which is referenced to the HS pin and provides excellent delay matching with the low-side driver.

8.3.3 Output Stages

The output stages are the interface to the power MOSFETs in the power train. High slew rate, low resistance, and high peak current capability of both outputs allow for efficient switching of the power MOSFETs. The low-side output stage is referenced to VSS and the high-side is referenced to HS.

8.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See *Start-Up and UVLO* for more information on UVLO operation mode. In normal mode when the V_{DD} and V_{HB-HS} are above UVLO threshold, the output stage is dependent on the states of the HI and LI pins. Unused inputs should be tied to ground and not left open.

Table 4. INPUT and OUTPUT Logic Table

HI	LI	HO (1)	LO (2)
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H

(1) HO is measured with respect to the HS pin.
(2) LO is measured with respect to the VSS pin.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LM25101 is a high voltage gate driver designed to drive both the high-side and low-side N-Channel MOSFETs in a half or full bridge configuration or in a synchronous buck circuit. The floating high side driver is capable of operating with supply voltages up to 100 V. This allows for N-Channel MOSFETs control in half-bridge, full-bridge, push-pull, two switch forward, and active clamp topologies. The outputs are independently controlled. Each channel is controlled by its respective input pins (HI and LI), allowing full and independent flexibility to control the state (ON and OFF) of the output.

9.2 Typical Application

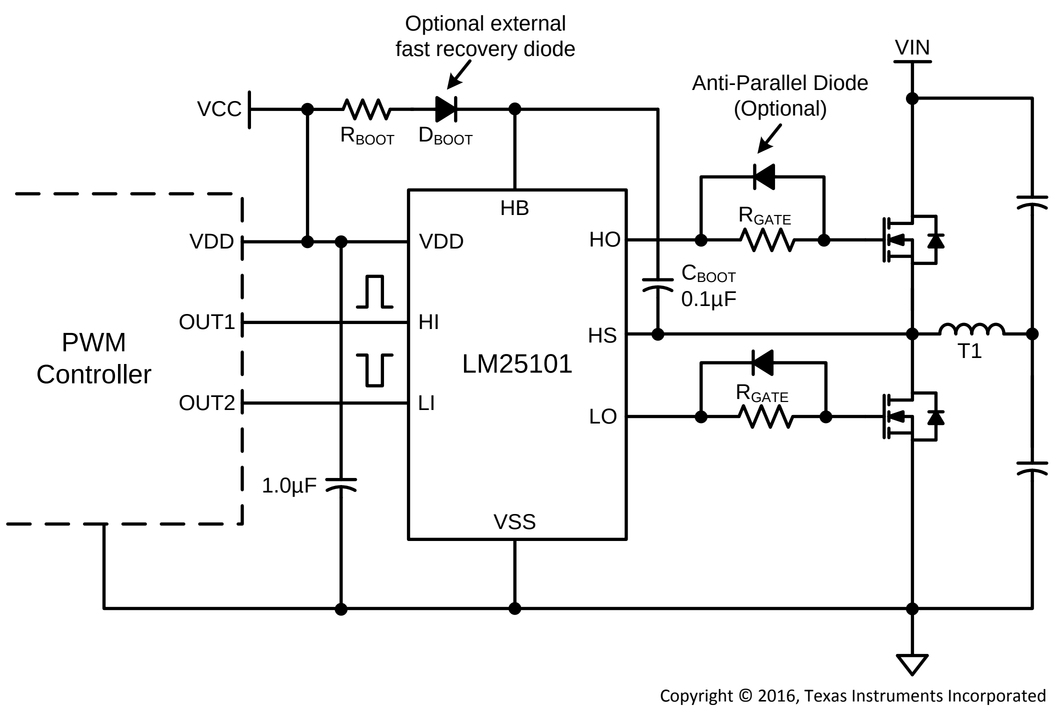


Figure 21. Application Diagram

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 5 as the input parameters.

Table 5. Design Parameters

PARAMETER	EXAMPLE VALUE
Gate driver	LM25101 (C version)
MOSFET	CSD19534KCS
V_{DD}	10 V
Q_G	17 nC
f_{SW}	500 kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Selecting External Gate Driver Resistor

External gate driver resistor (R_{GATE}) is sized to reduce ringing caused by parasitic inductances and capacitances and also to limit the current coming out of the gate driver.

Peak HO pullup current is calculated using Equation 1.

$$I_{OHH} = \frac{V_{DD} - V_{DH}}{R_{HOH} + R_{Gate} + R_{GFET\_Int}} = \frac{10V - 1.0V}{1.1V / 100mA + 4.7\Omega + 2.2\Omega} \approx 0.5A$$

where

- I_{OHH} is the peak pullup current
- V_{DH} is the bootstrap diode forward voltage drop
- R_{HOH} is the gate driver internal HO pullup resistance (1)
- R_{Gate} is the external gate drive resistance
- $R_{(GFET\_Int)}$ is the MOSFET internal gate resistance, provided by the transistor data sheet (1)

Similarly, Peak HO pulldown current is calculated using Equation 2.

$$I_{OLH} = \frac{V_{DD} - V_{DH}}{R_{HOL} + R_{Gate} + R_{GFET\_Int}}$$

where

- R_{HOL} is the HO pulldown resistance (2)

Peak LO pullup current is calculated using Equation 3.

$$I_{OHL} = \frac{V_{DD}}{R_{LOH} + R_{Gate} + R_{GFET\_Int}}$$

where

- R_{LOH} is the LO pullup resistance (3)

Peak LO pulldown current is calculated using Equation 4.

$$I_{OLL} = \frac{V_{DD}}{R_{LOL} + R_{Gate} + R_{FET\_Int}}$$

where

- R_{LOL} is the LO pulldown resistance (4)

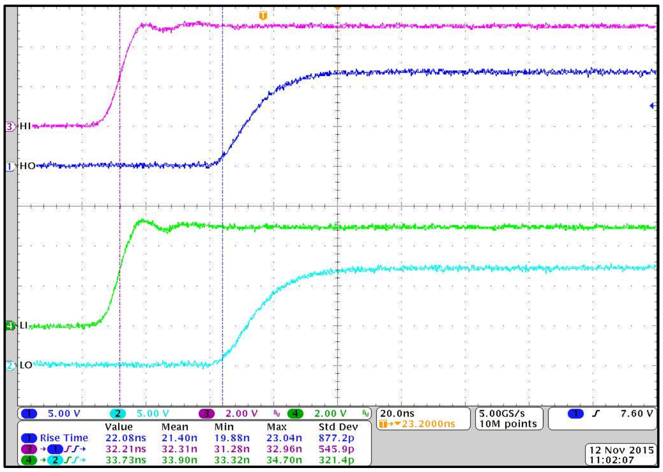
If the application requires fast turnoff, an anti-paralleled diode on R_{Gate} may be used to bypass the external gate drive resistor and speed up the turnoff transition.

(1) This value is either provided directly by the data sheet or is estimated from the testing conditions using $R_{HOH} = V_{OHH} / I_{HO}$.

9.2.3 Application Curves

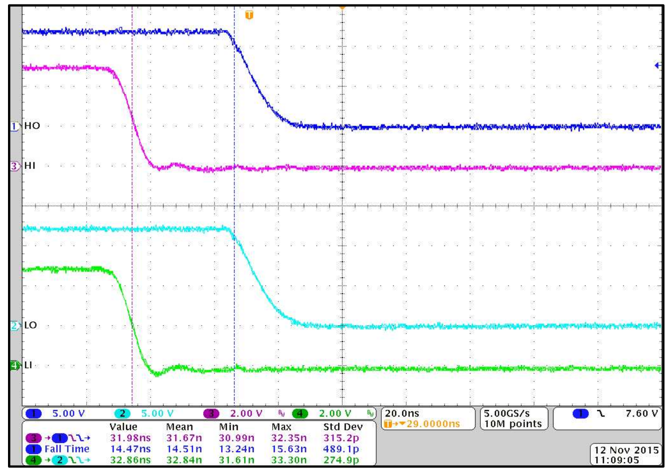
Figure 22 and Figure 23 show the rising and falling time and turnon and turnoff propagation delay testing waveform at room temperature. Each channel (HI, LI, HO, LO) is labeled and displayed on the left hand of the waveform.

The HI and LI pins are shorted together for these test waveforms. Therefore, the propagation delay matching between the channels can be measured and inspected.



C_L = 1 nF V_{DD} = 12 V f_{SW} = 500 kHz

Figure 22. Rising Time and Turnon Propagation Delay



C_L = 1 nF V_{DD} = 12 V f_{SW} = 500 kHz

Figure 23. Falling Time and Turnoff Propagation Delay

10 Power Supply Recommendations

The total IC power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are related to the switching frequency (f), output load capacitance on LO and HO (C_L), and supply voltage (V_{DD}), which can be roughly calculated using Equation 5.

$$P_{DGATES} = 2 \times f \times C_L \times V_{DD}^2 \quad (5)$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. Figure 24 shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with Equation 5. Figure 24 can be used to approximate the power losses due to the gate drivers.

The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to frequency. Larger capacitive loads require more energy to recharge the bootstrap capacitor resulting in more losses. Higher input voltages (V_{IN}) to the half bridge result in higher reverse recovery losses. Figure 25 was generated based on calculations and lab measurements of the diode recovery time and current under several operating conditions and can be used to approximate the diode power dissipation.

The total IC power dissipation can be estimated from these plots by summing the gate drive losses with the bootstrap diode losses for the intended application.

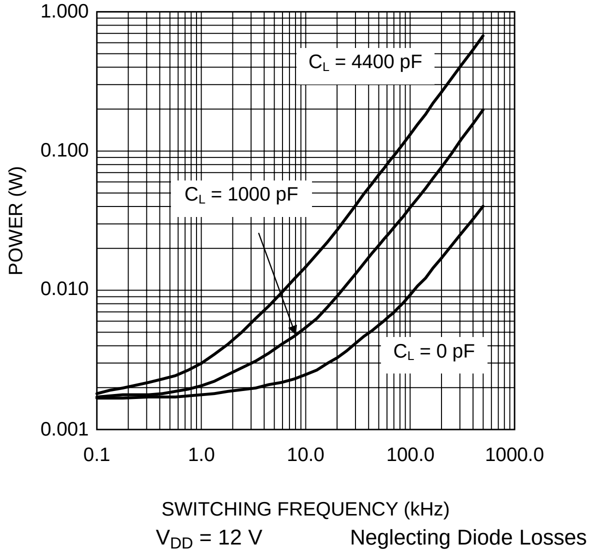


Figure 24. Gate Driver Power Dissipation (LO + HO)

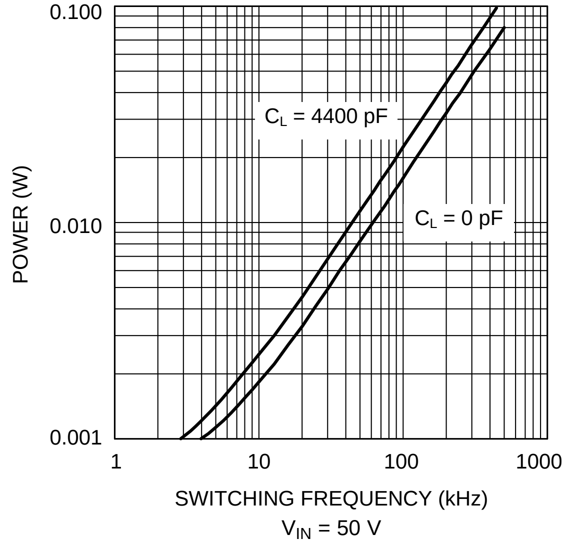


Figure 25. Diode Power Dissipation

11 Layout

11.1 Layout Guidelines

The optimum performance of high and low-side gate drivers cannot be achieved without following certain guidelines during circuit-board layout.

- Low ESR and ESL capacitors must be connected close to the IC, between the VDD and VSS pins and between the HB and HS pins to support the high peak currents being drawn from VDD during start-up of the external MOSFET.
- To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between the MOSFET drain and ground (VSS).
- To avoid large negative transients on the switch node (HS pin), the parasitic inductances must be minimized in the source of the top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier).
- Grounding Considerations:
  - The first priority in designing grounding connections is to confine to a minimal physical area the high peak currents that charge and discharge the MOSFET gate. This decreases the loop inductance and minimizes noise issues on the gate terminal of the MOSFET. The MOSFETs should be placed as close as possible to the gate driver.
  - The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor, and low-side MOSFET body diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

Figure 26 shows a recommended layout pattern for the driver. If possible a single layer placement is preferred.

11.2 Layout Example

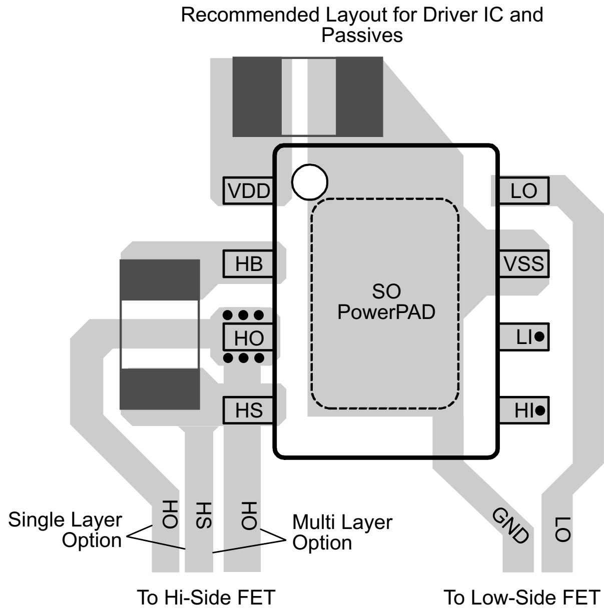


Figure 26. Recommended Layout Pattern

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM25101AM/NOPB	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	L25101 AM
LM25101AMR/NOPB	Obsolete	Production	SO PowerPAD (DDA) | 8	-	-	Call TI	Call TI	-40 to 125	L25101 AMR
LM25101AMRX/NOPB	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L25101 AMR
LM25101AMRX/NOPB.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L25101 AMR
LM25101AMRX/NOPB.B	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L25101 AMR
LM25101AMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25101 AM
LM25101AMX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25101 AM
LM25101AMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25101 AM
LM25101ASD-1/NOPB	Active	Production	WSON (NGT) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	25101A1
LM25101ASD-1/NOPB.A	Active	Production	WSON (NGT) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	25101A1
LM25101ASD-1/NOPB.B	Active	Production	WSON (NGT) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	25101A1
LM25101ASD/NOPB	Active	Production	WSON (DPR) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	25101A
LM25101ASD/NOPB.A	Active	Production	WSON (DPR) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	25101A
LM25101ASD/NOPB.B	Active	Production	WSON (DPR) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	25101A
LM25101ASDX-1/NOPB	Active	Production	WSON (NGT) | 8	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	25101A1
LM25101ASDX-1/NOPB.A	Active	Production	WSON (NGT) | 8	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	25101A1
LM25101ASDX-1/NOPB.B	Active	Production	WSON (NGT) | 8	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	25101A1
LM25101ASDX/NOPB	Active	Production	WSON (DPR) | 10	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	25101A
LM25101ASDX/NOPB.A	Active	Production	WSON (DPR) | 10	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	25101A
LM25101ASDX/NOPB.B	Active	Production	WSON (DPR) | 10	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	25101A
LM25101BMA/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25101 BMA
LM25101BMA/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25101 BMA

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM25101BMA/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25101 BMA
LM25101BMAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25101 BMA
LM25101BMAX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25101 BMA
LM25101BMAX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25101 BMA
LM25101BSD/NOPB	Active	Production	WSON (DPR) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	25101B
LM25101BSD/NOPB.A	Active	Production	WSON (DPR) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	25101B
LM25101BSD/NOPB.B	Active	Production	WSON (DPR) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	25101B
LM25101BSDX/NOPB	Active	Production	WSON (DPR) | 10	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	25101B
LM25101BSDX/NOPB.A	Active	Production	WSON (DPR) | 10	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	25101B
LM25101BSDX/NOPB.B	Active	Production	WSON (DPR) | 10	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	25101B
LM25101CMA/NOPB	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	L25101 CMA
LM25101CMAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25101 CMA
LM25101CMAX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25101 CMA
LM25101CMAX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25101 CMA
LM25101CMY/NOPB	Active	Production	HVSSOP (DGN) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	CMYN
LM25101CMY/NOPB.A	Active	Production	HVSSOP (DGN) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	CMYN
LM25101CMY/NOPB.B	Active	Production	HVSSOP (DGN) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	CMYN
LM25101CMYE/NOPB	Active	Production	HVSSOP (DGN) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	CMYN
LM25101CMYE/NOPB.A	Active	Production	HVSSOP (DGN) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	CMYN
LM25101CMYE/NOPB.B	Active	Production	HVSSOP (DGN) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	CMYN
LM25101CMYX/NOPB	Active	Production	HVSSOP (DGN) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	CMYN
LM25101CMYX/NOPB.A	Active	Production	HVSSOP (DGN) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	CMYN
LM25101CMYX/NOPB.B	Active	Production	HVSSOP (DGN) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	CMYN
LM25101CSD/NOPB	Active	Production	WSON (DPR) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	25101C
LM25101CSD/NOPB.A	Active	Production	WSON (DPR) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	25101C

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM25101CSD/NOPB.B	Active	Production	WSON (DPR) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	25101C
LM25101CSDX/NOPB	Active	Production	WSON (DPR) | 10	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	25101C
LM25101CSDX/NOPB.A	Active	Production	WSON (DPR) | 10	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	25101C
LM25101CSDX/NOPB.B	Active	Production	WSON (DPR) | 10	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	25101C

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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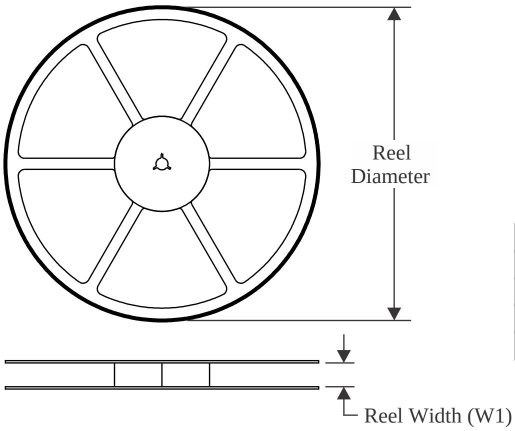
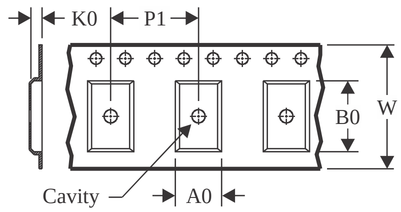
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

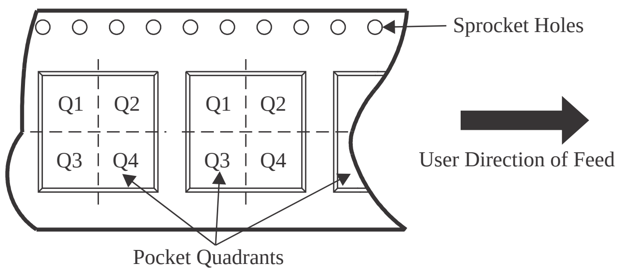


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

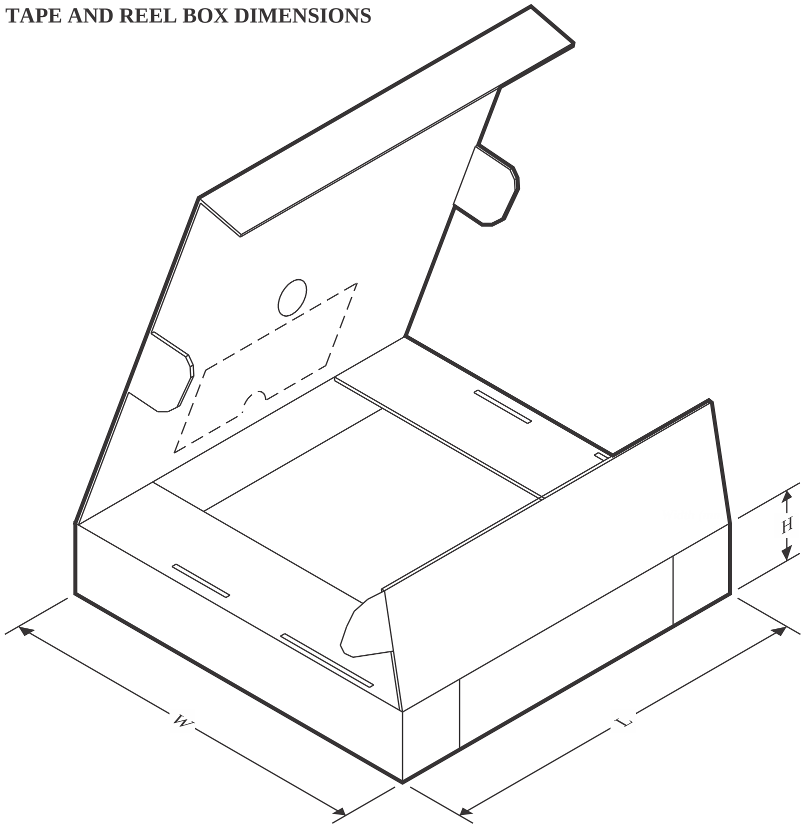
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM25101AMRX/NOPB	SO PowerPAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM25101AMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM25101ASD-1/NOPB	WSON	NGT	8	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM25101ASD/NOPB	WSON	DPR	10	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM25101ASDX-1/NOPB	WSON	NGT	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM25101ASDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM25101BMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM25101BSD/NOPB	WSON	DPR	10	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM25101BSDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM25101CMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM25101CMY/NOPB	HVSSOP	DGN	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM25101CMYE/NOPB	HVSSOP	DGN	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM25101CMYX/NOPB	HVSSOP	DGN	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM25101CSD/NOPB	WSON	DPR	10	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM25101CSDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

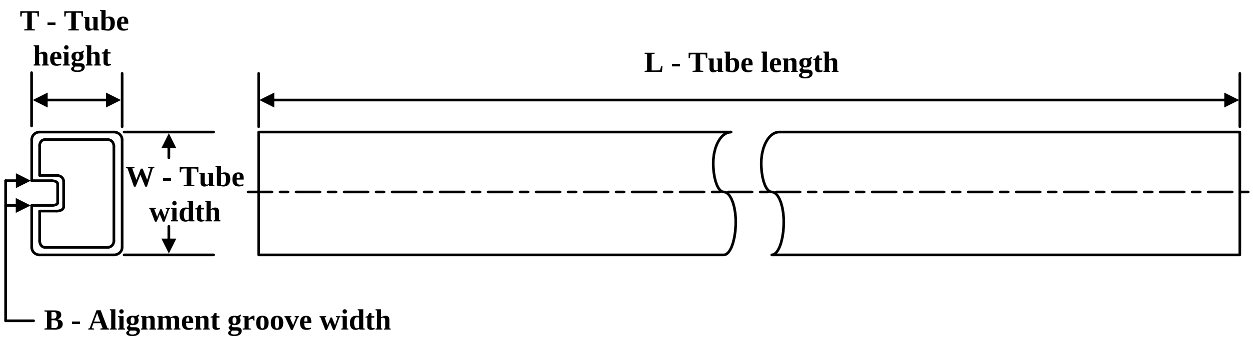
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

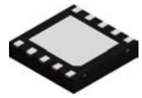
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM25101AMRX/NOPB	SO PowerPAD	DDA	8	2500	356.0	356.0	36.0
LM25101AMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM25101ASD-1/NOPB	WSON	NGT	8	1000	210.0	185.0	35.0
LM25101ASD/NOPB	WSON	DPR	10	1000	210.0	185.0	35.0
LM25101ASDX-1/NOPB	WSON	NGT	8	4500	367.0	367.0	35.0
LM25101ASDX/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0
LM25101BMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM25101BSD/NOPB	WSON	DPR	10	1000	210.0	185.0	35.0
LM25101BSDX/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0
LM25101CMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM25101CMY/NOPB	HVSSOP	DGN	8	1000	210.0	185.0	35.0
LM25101CMYE/NOPB	HVSSOP	DGN	8	250	210.0	185.0	35.0
LM25101CMYX/NOPB	HVSSOP	DGN	8	3500	367.0	367.0	35.0
LM25101CSD/NOPB	WSON	DPR	10	1000	210.0	185.0	35.0
LM25101CSDX/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

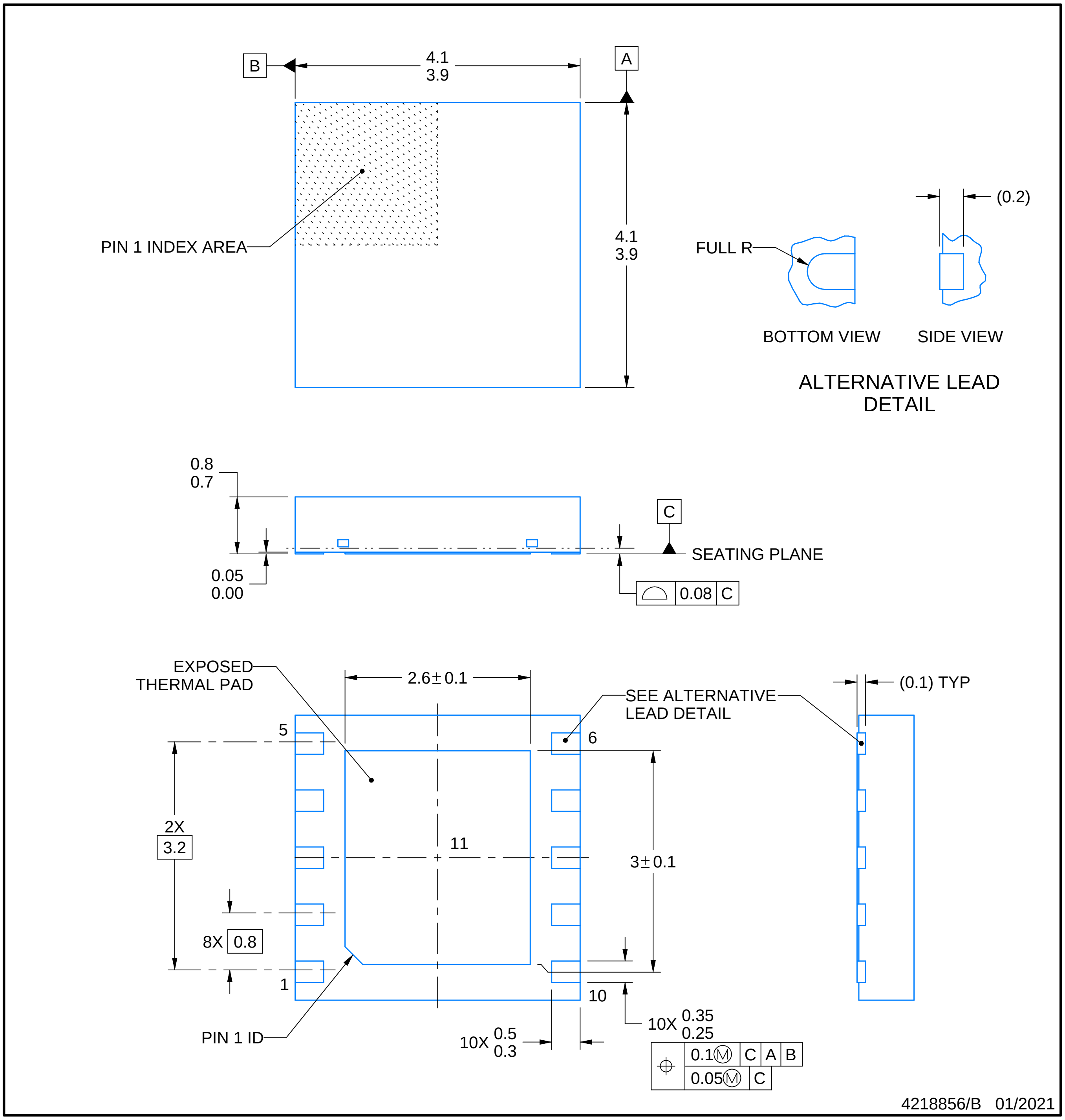
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM25101BMA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM25101BMA/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LM25101BMA/NOPB.B	D	SOIC	8	95	495	8	4064	3.05



PACKAGE OUTLINE

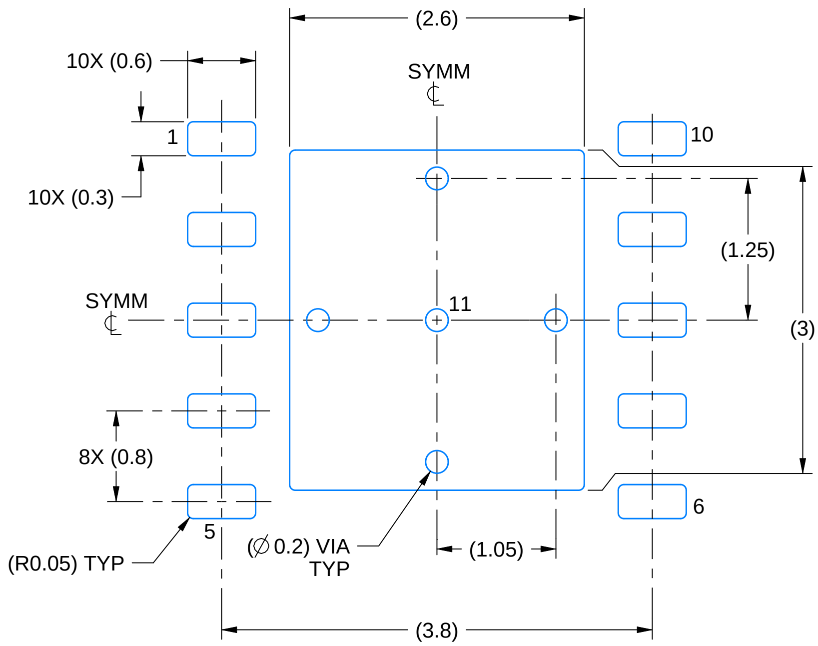
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

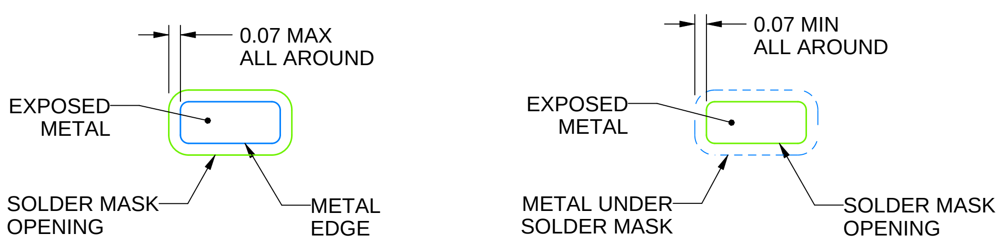


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

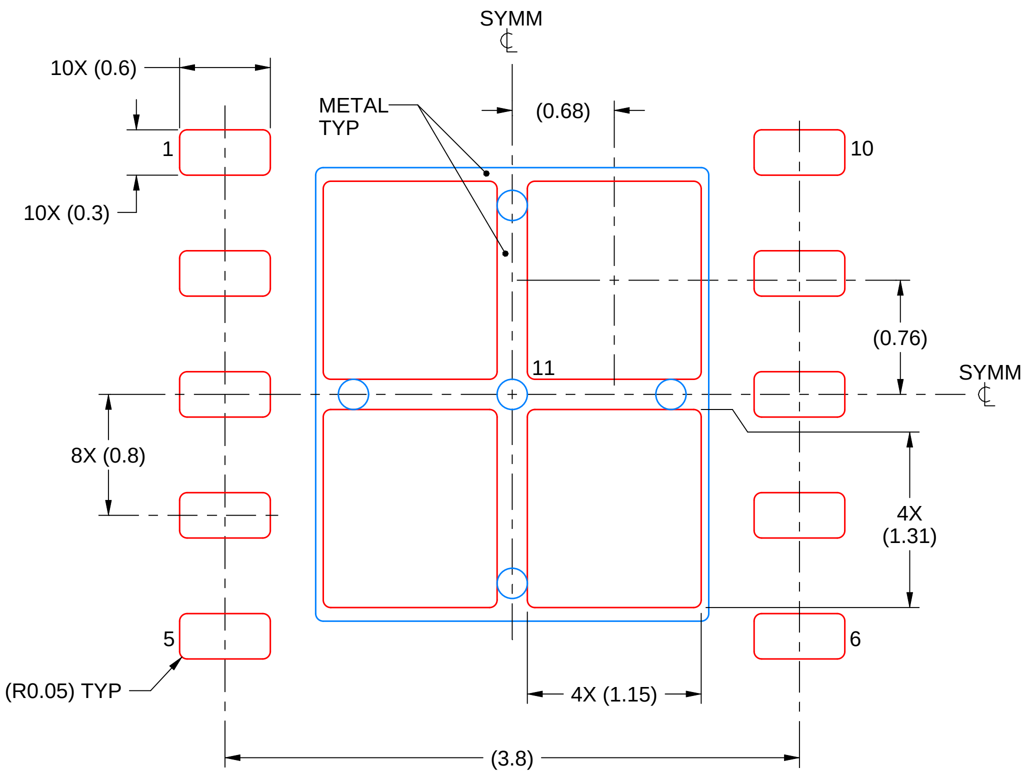
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218856/B 01/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



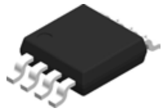
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4218856/B 01/2021

NOTES: (continued)

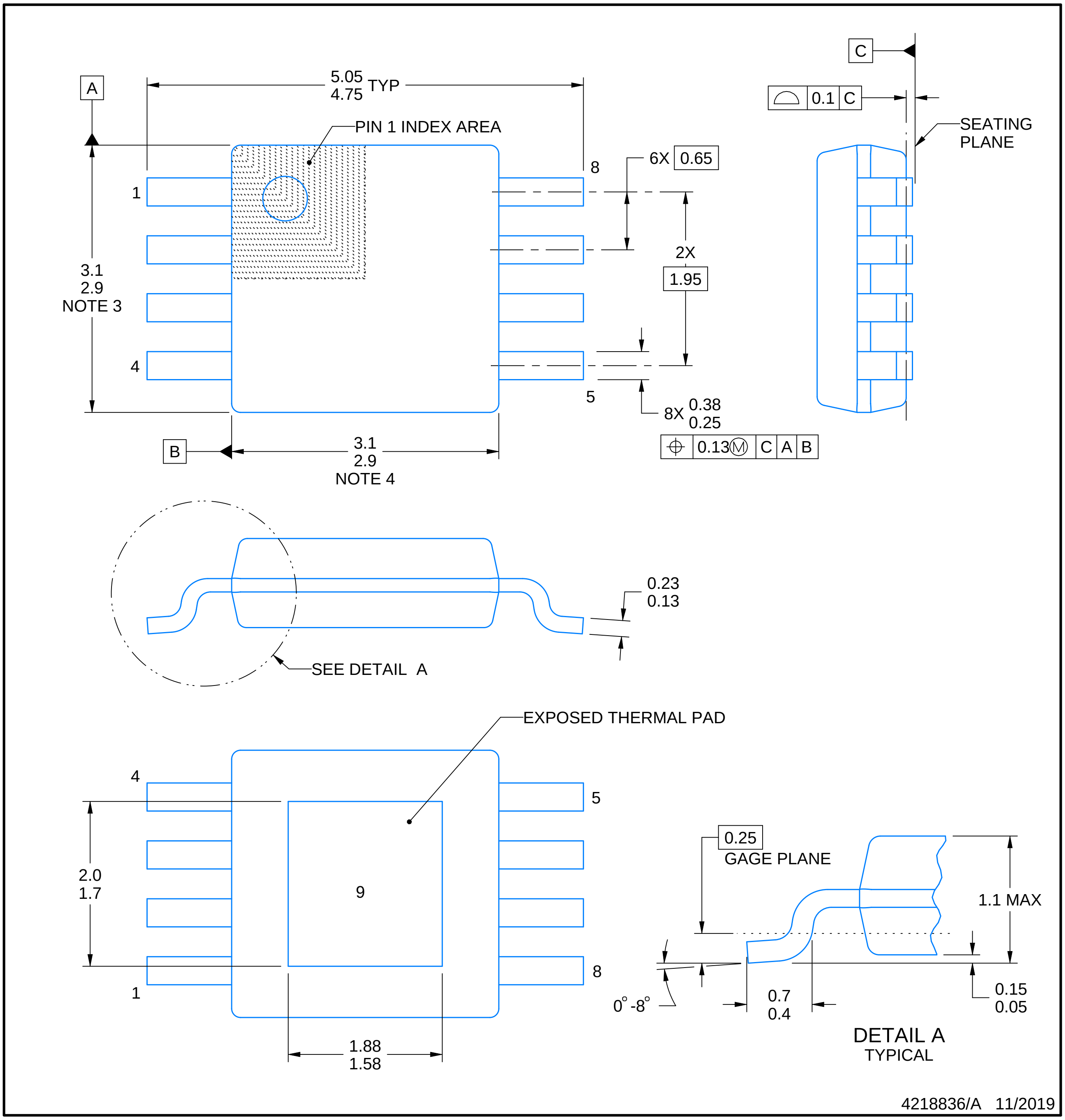
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



PACKAGE OUTLINE

PowerPAD™ VSSOP - 1.1 mm max height

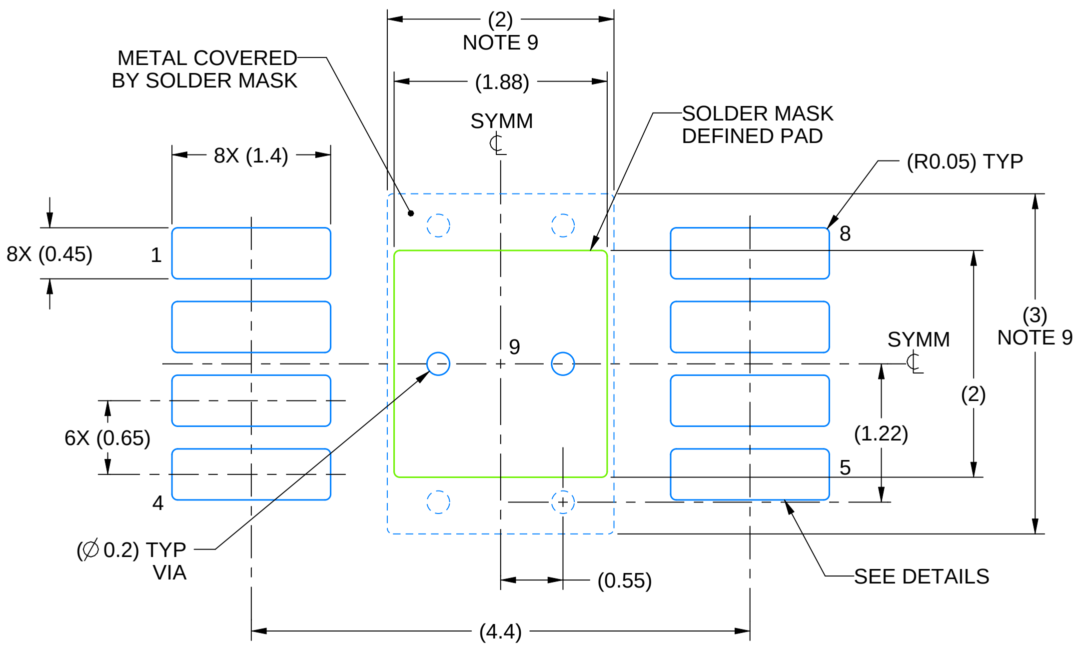
SMALL OUTLINE PACKAGE



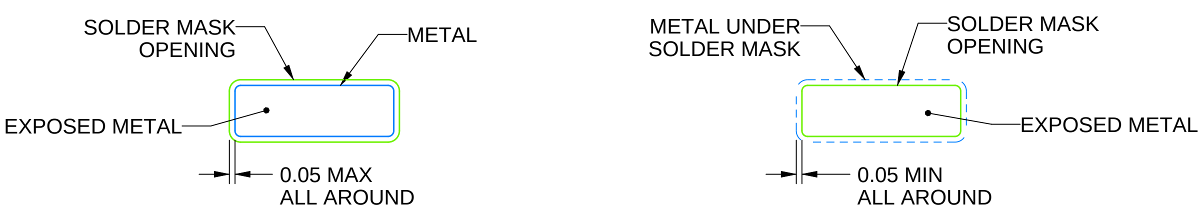
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON-SOLDER MASK
DEFINED
(PREFERRED)

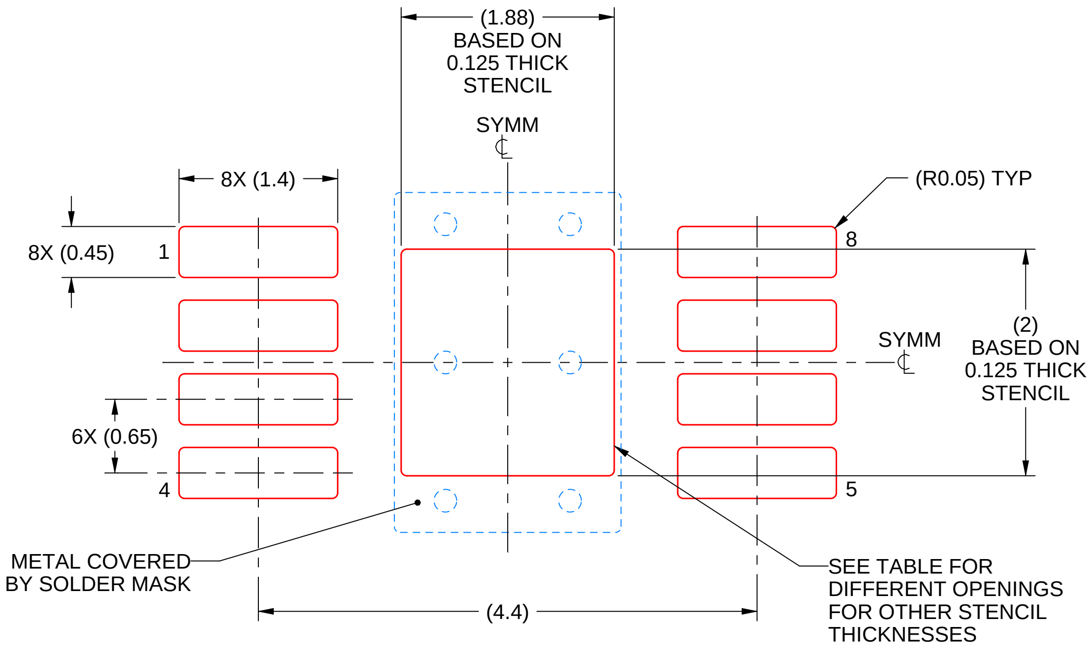
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218836/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



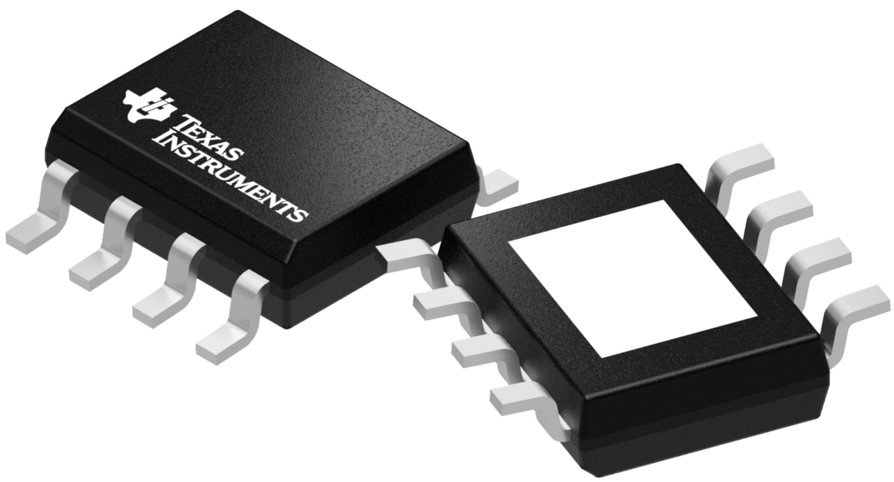
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.10 X 2.24
0.125	1.88 X 2.00 (SHOWN)
0.15	1.72 X 1.83
0.175	1.59 X 1.69

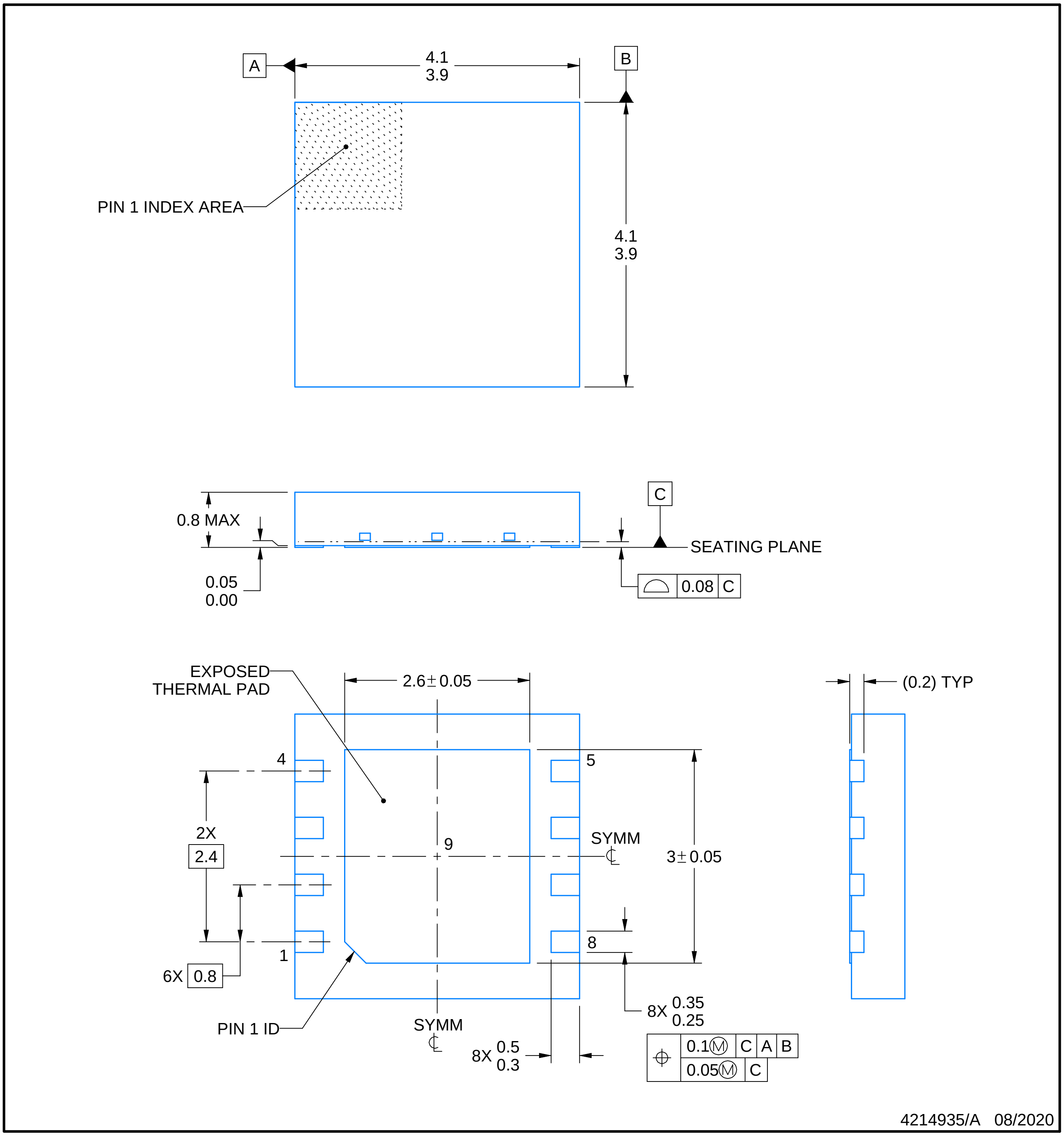
4218836/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

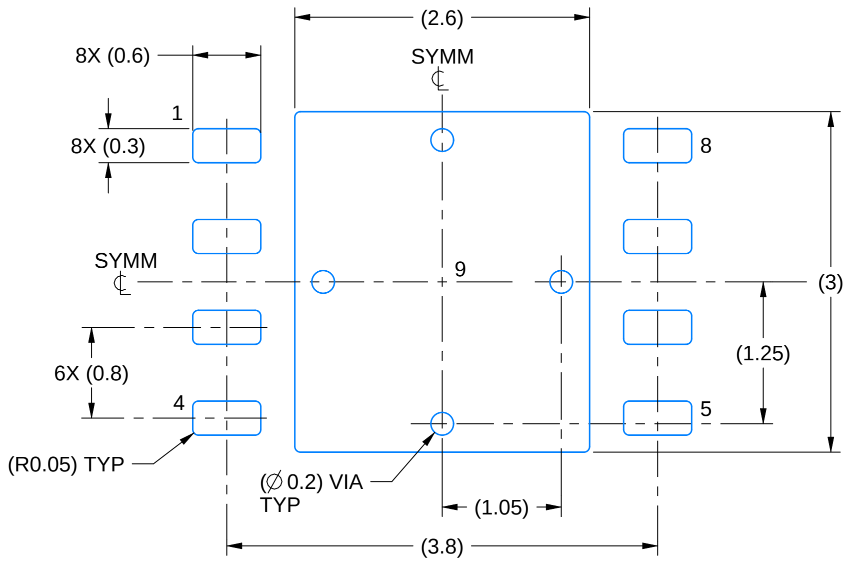


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

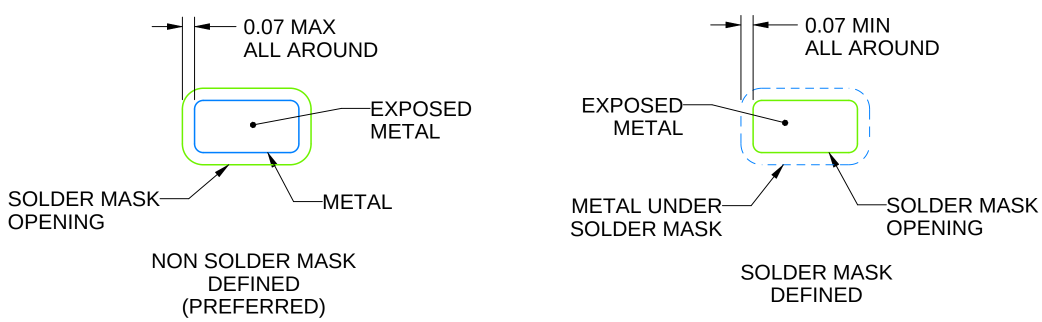


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

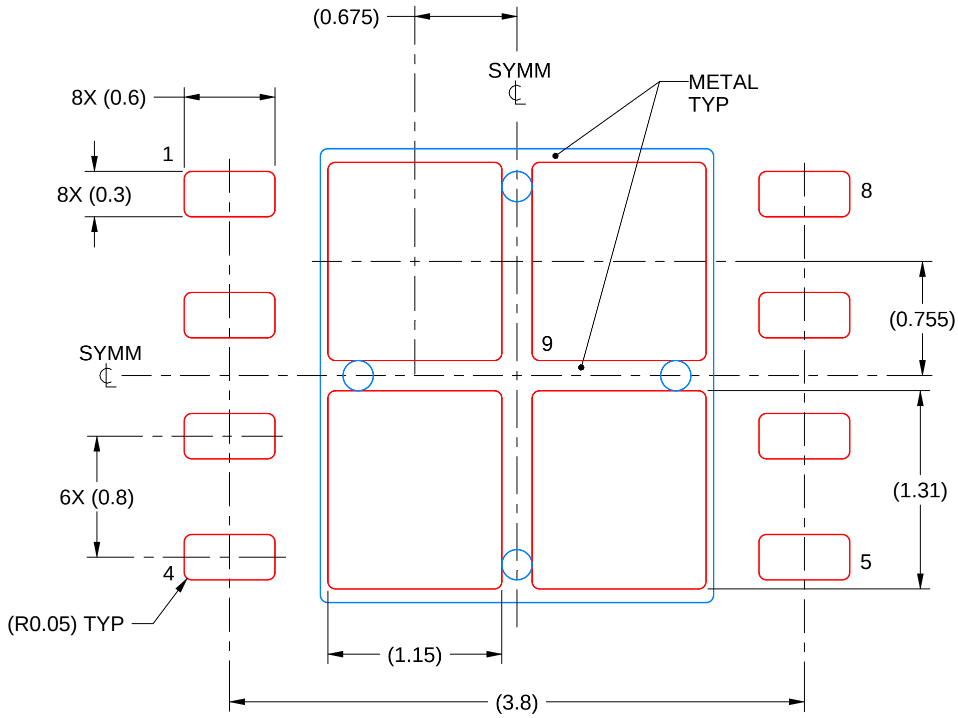


SOLDER MASK DETAILS

4214935/A 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



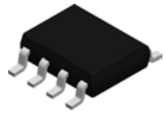
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214935/A 08/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

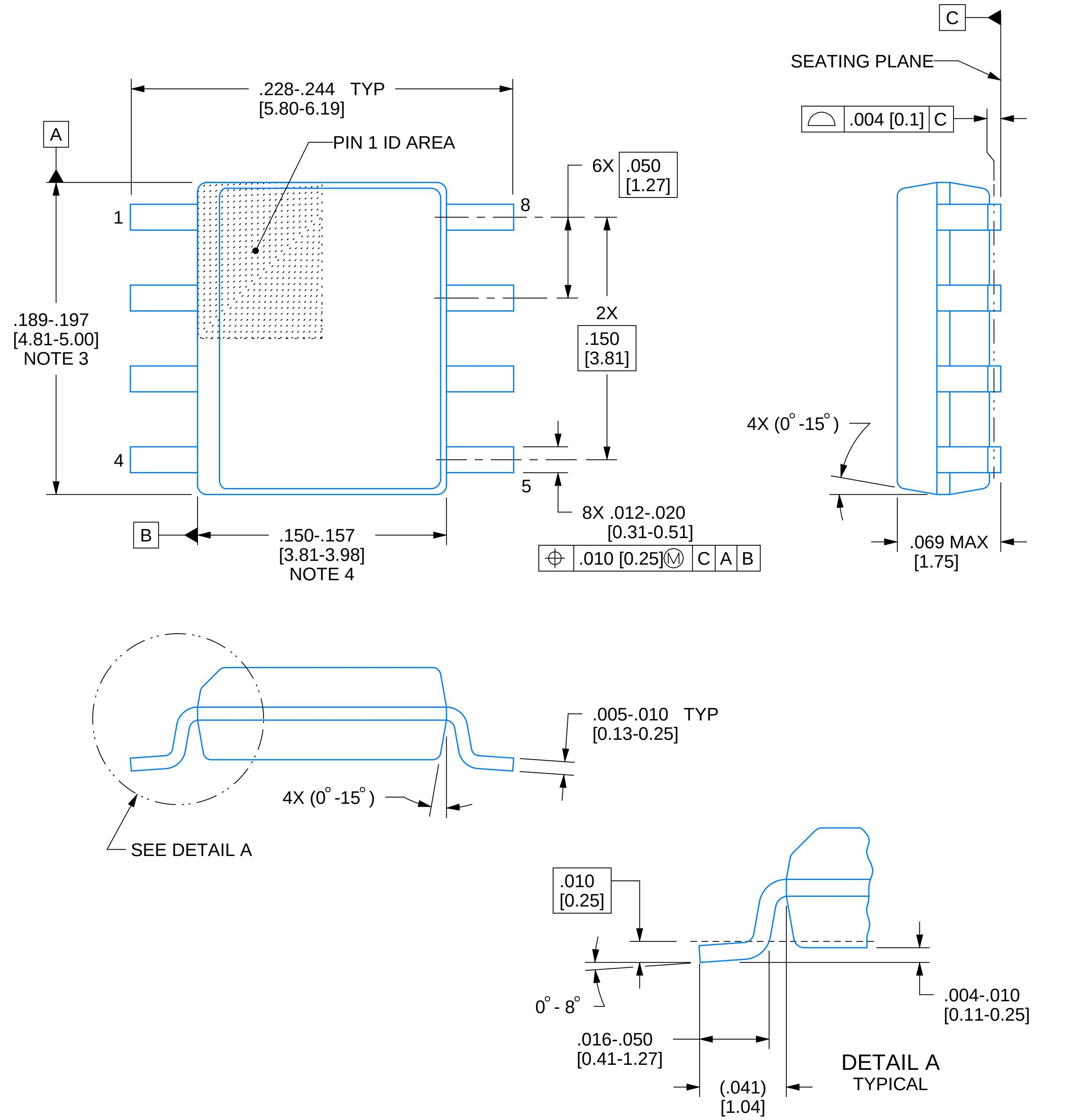


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

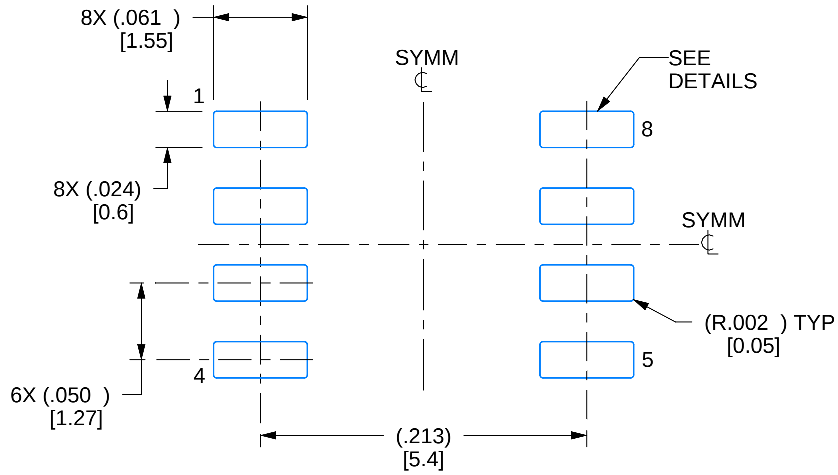
SMALL OUTLINE INTEGRATED CIRCUIT



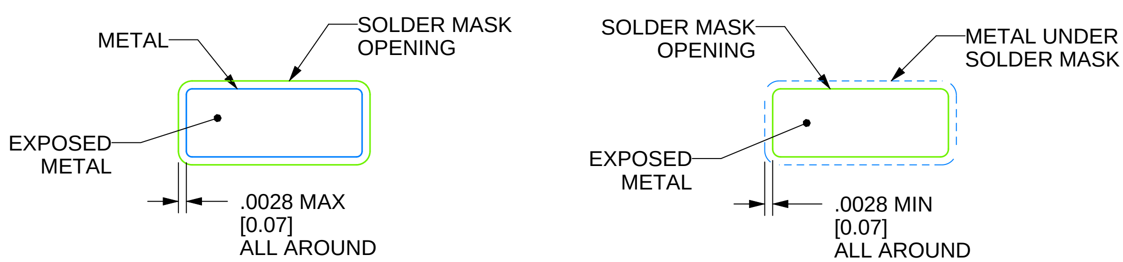
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

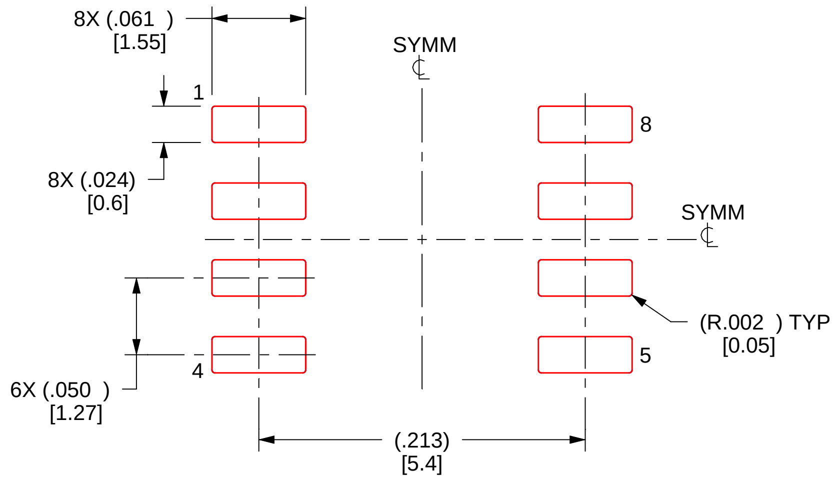
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

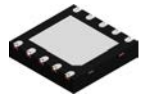


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

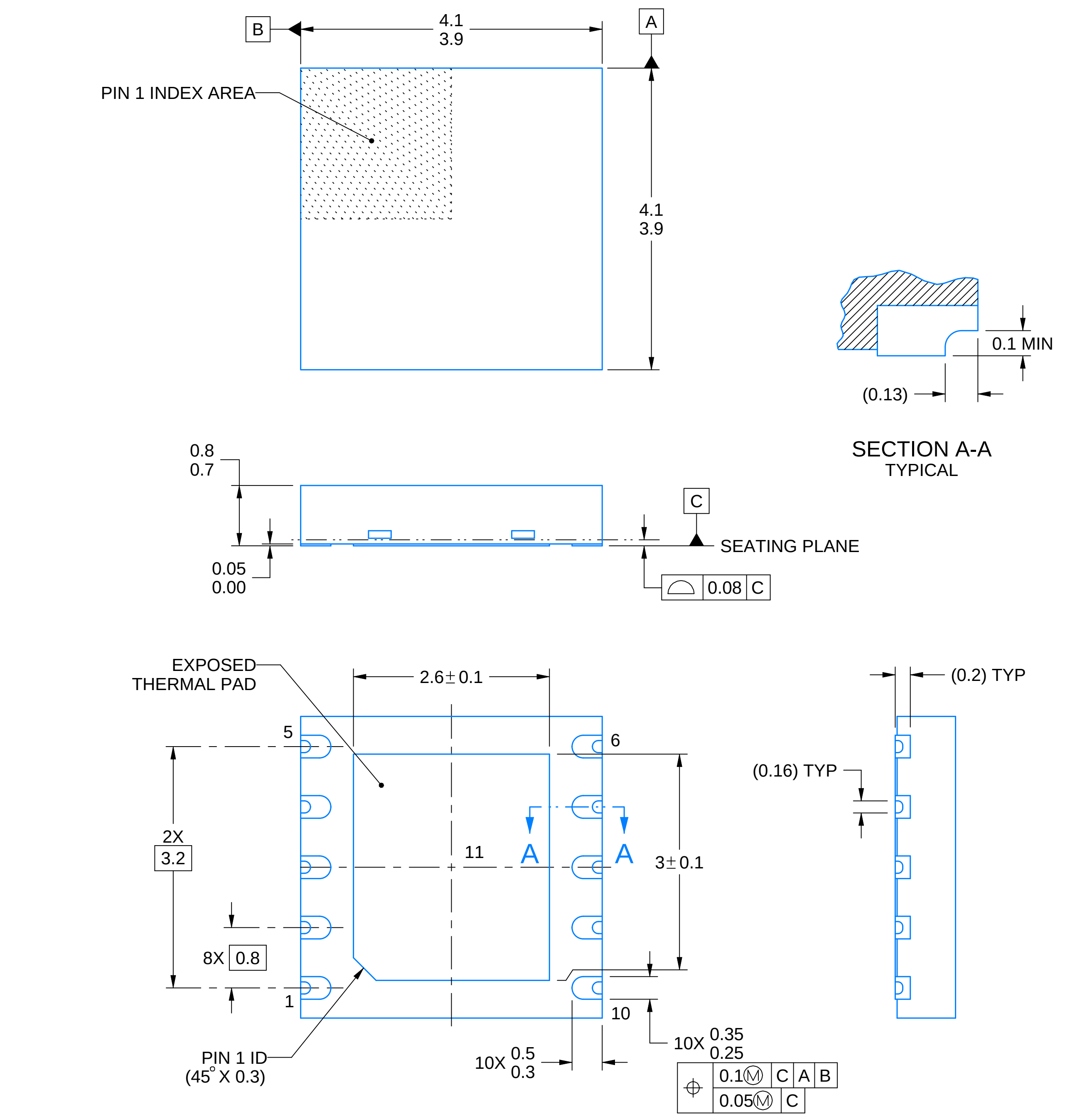
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

WSON - 0.8 mm max height

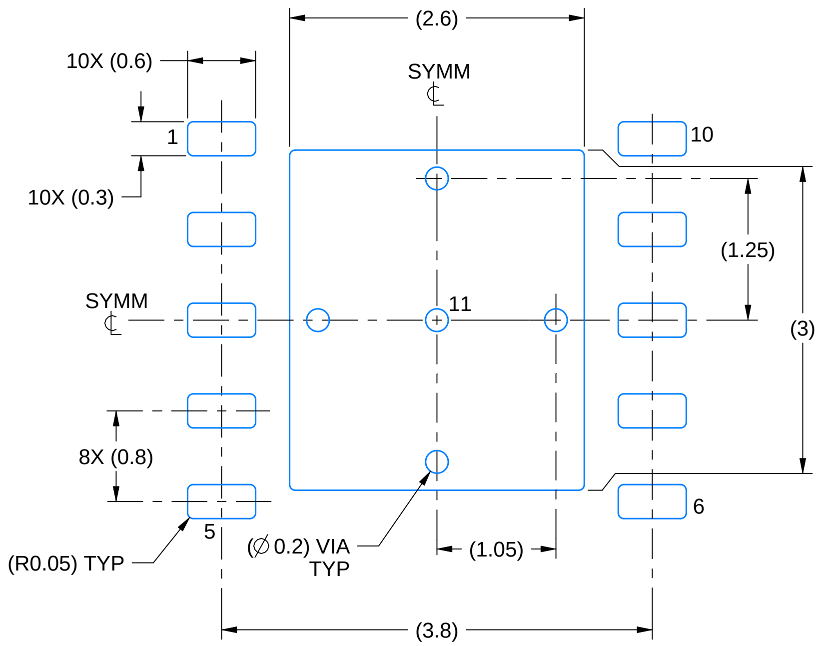
PLASTIC SMALL OUTLINE - NO LEAD



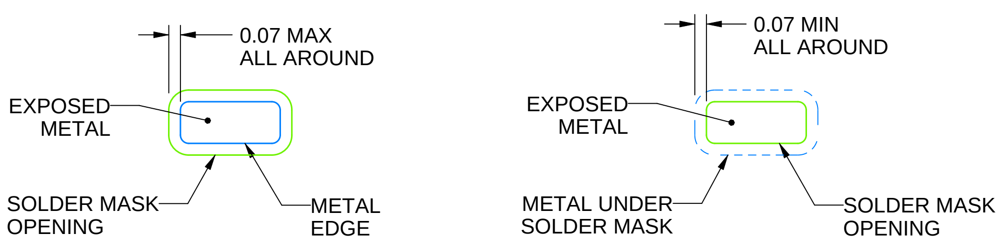
4232176/A 09/2025

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)

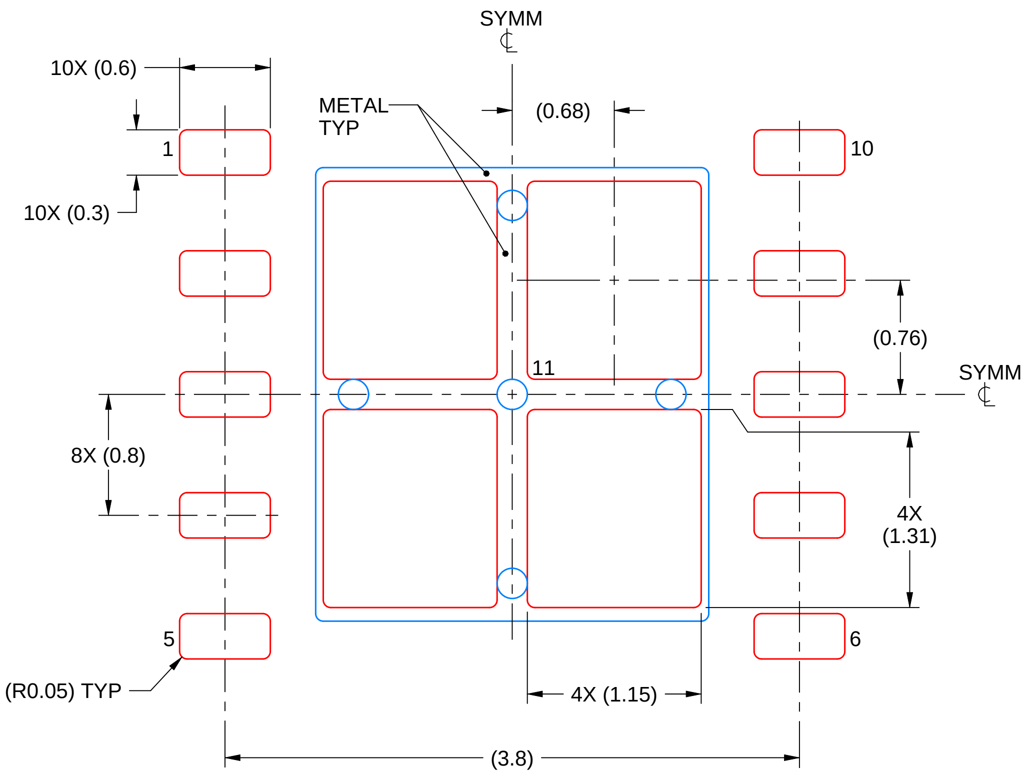
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4232176/A 09/2025

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4232176/A 09/2025

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265