ISOM811x-Q1 Automotive Reinforced Single-Channel Opto-Emulator With Analog Transistor Output

1 Features

- Footprint compatible, pin-to-pin upgrade to industry-standard phototransistor optocouplers
- AEC-Q100 qualified with the following results:
  - Device temperature Grade 1: -40°C to 125°C ambient operating temperature range
- 1-channel LED-emulator input
- Current transfer ratio (CTR) at I_F = 5mA, V_{CE} = 5V:
  - ISOM8110-Q1, ISOM8115-Q1: 100% to 155%
  - ISOM8111-Q1, ISOM8116-Q1: 150% to 230%
  - ISOM8112-Q1, ISOM8117-Q1: 255% to 380%
  - ISOM8113-Q1, ISOM8118-Q1: 375% to 560%
- High collector-emitter voltage: V_{CE} (max) = 80V
- Robust SiO_2 isolation barrier
  - Isolation rating: Up to 5000V_{RMS}
  - Working voltage: Up to 750V_{RMS} , 1061V_{PK}
  - Surge capability: Up to 10kV_{PK}
- Response time: 3µs (typical) at V_{CE} = 10V, I_C = 2mA, R_L = 100Ω
- Functional Safety-Capable
  - Documentation available to aid functional safety system design: ISOM811x-Q1
- Section 6.6 (Planned)
  - DIN EN IEC 60747-17 (VDE 0884-17) conformity per VDE
  - UL 1577 recognition, 5000V_{RMS}
  - IEC 62368-1, IEC 61010-1 certifications
  - CQC GB 4943.1 certification

2 Applications

- Switching power supply
- HEV/EV OBC & DC/DC converter
- Advanced driver assistance systems (ADAS)
- Body electronics & lighting
- Infotainment & cluster
- HEV/EV battery-management system (BMS)

3 Description

The ISOM811x-Q1 devices are single-channel optocoupler-emulators with LED-emulator input and transistor output. The devices are footprint compatible and pin-to-pin upgrades for many traditional optocouplers, allowing enhancement to existing systems with no PCB redesign.

ISOM811x-Q1 opto-emulators offer significant reliability and performance advantages compared to optocouplers, including high bandwidth, low turn-off delay, low power consumption, wider temperature ranges, flat CTR, and tight process controls resulting in small part-to-part skew. Since there is no aging effect or temperature variation to compensate for, the emulated LED input stage consumes less power than optocouplers.

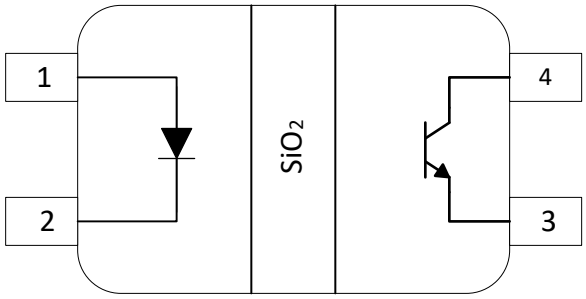
ISOM811x-Q1 devices are offered in small SOIC-4 packages with 2.54mm and 1.27mm pin pitches, supporting 3750V_{RMS} and 5000V_{RMS} isolation ratings with DC (ISOM811[0-3]-Q1) and bidirectional DC (ISOM811[5-8]-Q1) input options. The high performance and reliability of ISOM811x-Q1 enables these devices to be used in power supply feedback design, motor drives, I/O modules in industrial controllers, factory automation applications, and more.

Package Information

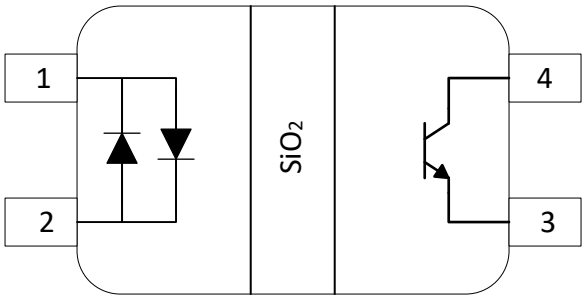
PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (NOM)
ISOM811x-Q1	SO-4 (DFG)	7.0mm × 3.5mm	4.8mm × 3.5mm
	SO-4 (DFH)	7.0mm × 2.7mm	4.8mm × 2.7mm
	SO-4 (DFS)	10.0mm × 3.6mm	7.5mm × 3.6mm

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

ISOM811(0-3)-Q1



ISOM811(5-8)-Q1



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Device Comparison....3
5 Pin Configuration and Functions....3
6 Specifications....4
6.1 Absolute Maximum Ratings....4
6.2 ESD Ratings....4
6.3 Recommended Operating Conditions....4
6.4 Thermal Information....4
6.5 Insulation Specifications....5
6.6 Safety-Related Certifications....6
6.7 Safety Limiting Values....6
6.8 Electrical Characteristics....7
6.9 Switching Characteristics....9
6.10 Typical Characteristics....11
7 Parameter Measurement Information....17
8 Detailed Description....18
8.1 Overview....18
8.2 Functional Block Diagram....18
8.3 Feature Description....19
8.4 Device Functional Modes....19
9 Application and Implementation....20
9.1 Application Information....20
9.2 Power Supply Recommendations....25
9.3 Layout....25
10 Device and Documentation Support....26
10.1 Documentation Support....26
10.2 Receiving Notification of Documentation Updates....26
10.3 Support Resources....26
10.4 Trademarks....26
10.5 Electrostatic Discharge Caution....26
10.6 Glossary....26
11 Revision History....26
12 Mechanical, Packaging, and Orderable Information....27

Copyright © 2025 Texas Instruments Incorporated

4 Device Comparison

Table 4-1. Device Selection

PART NUMBER	CTR (I_F = 5mA)	PACKAGE	PIN PITCH
ISOM8110-Q1, ISOM8115-Q1	100% to 155%	4-pin SOIC (DFG), 4-pin SOIC (DFH), 4-pin SOIC (DFS)	2.54mm, 1.27mm, 2.54mm
ISOM8111-Q1, ISOM8116-Q1	150% to 230%		
ISOM8112-Q1, ISOM8117-Q1	255% to 380%		
ISOM8113-Q1, ISOM8118-Q1	375% to 560%		

5 Pin Configuration and Functions

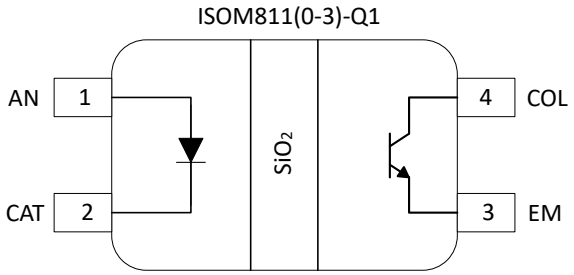


Figure 5-1. ISOM811[0-3]-Q1 4-Pin SOIC (Top View)

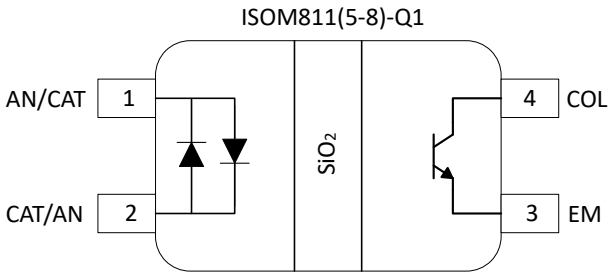


Figure 5-2. ISOM811[5-8]-Q1 4-Pin SOIC (Top View)

Table 5-1. Pin Functions

PIN		TYPE [1]	DESCRIPTION
NO.	NAME		
1	AN	I	Anode connection of input LED emulator
2	CAT	I	Cathode connection of input LED emulator
3	EM	O	Emitter for transistor
4	COL	O	Collector for transistor

(1) I = Input, O = Output

Copyright © 2025 Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

See(1) (2)

		MIN	MAX	UNIT
$I_{F(max)}$	Maximum Input forward current		50	mA
V_{CEO}	Collector-emitter voltage		80	V
V_{ECO}	Emitter-collector voltage		7	V
I_{FP}	Input pulse forward current (1µs width)		1	A
V_R	Input reverse voltage at I_R = 10µA (3)		7	V
P_I	Input power dissipation		140	mW
I_C	Collector current		50	mA
P_C	Collector power dissipation		150	mW
P_T	Total power dissipation		290	mW
T_A	Ambient temperature	–55	125	°C
T_J	Operating junction temperature		150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under the operational sections of this document. If used outside the listed operational conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All specifications are at T_A = 25°C unless otherwise noted
(3) Only applies to ISOM8110-Q1, ISOM8112-Q1, and ISOM8113-Q1

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 3A	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
$I_{F(ON)}$	Input ON-state forward current	0.7		20	mA
V_{CEO}	Collector-emitter voltage	-5		48	V
T_A	Ambient temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		ISOM811x-Q1			UNIT
		DFS (SOIC)	DFG (SOIC)	DFH (SOIC)	
		4 PINS	4 PINS	4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	269.1	283.9	288.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	156.7	173.1	173.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	194.2	201.4	192.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	128.4	125.1	121.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	191.0	198.0	190.0	°C/W

(1) For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics application note.

Copyright © 2025 Texas Instruments Incorporated

6.5 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE		UNIT
			4-DFG, 4-DFH	4-DFS	
IEC 60664-1					
CLR	External clearance(1)	Side 1 to side 2 distance through air	> 5	> 8	mm
CPG	External creepage(1)	Side 1 to side 2 distance across package surface	> 5	> 8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	>17	µm
CTI	Comparative tracking index	IEC 60112; UL 746A	>400	>400	V
	Material Group	According to IEC 60664-1	II	II	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}	I-IV	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-IV	I-IV	
		Rated mains voltage ≤ 500V_{RMS}	I-III	I-IV	
DIN EN IEC 60747-17 (VDE 0884-17) (6)					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	707	1061	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test. See Insulation Lifetime	500	750	V_{RMS}
		DC voltage	707	1061	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production)	5303	7071	V_{PK}
V_{IMP}	Maximum impulse voltage (2)	Tested in air, 1.2/50µs waveform per IEC 62368-1	7200	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	$V_{ISOM} \geq 1.3 \times V_{IMP}$; tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	10000	10400	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤ 5	≤ 5	
		Method b: At routine test (100% production) and preconditioning (type test), $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤ 5	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 × sin (2 πft), f = 1MHz	1	1	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500V, T_A = 25°C	> 10^{12}	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^9	> 10^9	
	Pollution degree		2	2	
	Climatic category		40/125/21	40/125/21	
UL 1577					
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)	3750	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) Testing is carried out in air to determine the surge immunity of the package.
(3) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

Copyright © 2025 Texas Instruments Incorporated

(6) This coupler is suitable for *safe electrical insulation only* within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

6.6 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 61010-1, IEC 62368-1 and IEC 60601-1	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1	Certified according to EN 61010-1 and EN 62368-1
Certificate pending	Master contract number: 220991	File number: E181974	Certificate: CQC24001426995	Client ID number: 77311

6.7 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SO-4 PACKAGE (DFG)						
I_S	Safety limiting input current	$R_{\theta JA}$= 283.9°C/W, V_F = 1.4V, T_J = 150°C, T_A = 25°C			300	mA
		$R_{\theta JA}$=283.9°C/W, V_{CEO} = 40V, T_J = 150°C, T_A = 25°C			10.5	mA
		$R_{\theta JA}$= 283.9°C/W, V_{CEO} = 24V, T_J =150°C, T_A = 25°C			17.5	mA
		$R_{\theta JA}$= 283.9°C/W, V_{CEO} = 15V, T_J = 150°C, T_A = 25°C			28	mA
P_S	Safety limiting total power	$R_{\theta JA}$= 283.9°C/W, T_J = 150°C, T_A = 25°C			420	mW
T_S	Maximum safety temperature				150	°C
SO-4 PACKAGE (DFH)						
I_S	Safety limiting input current	$R_{\theta JA}$= 288.8°C/W, V_F = 1.4V, T_J = 150°C, T_A = 25°C			300	mA
I_S	Safety limiting input current	$R_{\theta JA}$=288.8°C/W, V_{CEO} = 40V, T_J = 150°C, T_A = 25°C			10.5	mA
I_S	Safety limiting input current	$R_{\theta JA}$= 288.8°C/W, V_{CEO} = 24V, T_J =150°C, T_A = 25°C			17.5	mA
I_S	Safety limiting input current	$R_{\theta JA}$= 288.8°C/W, V_{CEO} = 15V, T_J = 150°C, T_A = 25°C			28	mA
P_S	Safety limiting total power	$R_{\theta JA}$= 288.8°C/W, T_J = 150°C, T_A = 25°C			420	mW
T_S	Maximum safety temperature				150	°C
SO-4 PACKAGE (DFS)						
I_S	Safety limiting input current	$R_{\theta JA}$= 269.1°C/W, V_F = 1.4V, T_J = 150°C, T_A = 25°C			320	mA
I_S	Safety limiting input current	$R_{\theta JA}$= 269.1°C/W, V_{CEO} = 40V, T_J = 150°C, T_A = 25°C			11	mA
I_S	Safety limiting input current	$R_{\theta JA}$= 269.1°C/W, V_{CEO} = 24V, T_J =150°C, T_A = 25°C			18	mA
I_S	Safety limiting input current	$R_{\theta JA}$= 269.1°C/W, V_{CEO} = 15V, T_J = 150°C, T_A = 25°C			30	mA
P_S	Safety limiting total power	$R_{\theta JA}$= 269.1°C/W, T_J = 150°C, T_A = 25°C			470	mW
T_S	Maximum safety temperature				150	°C

(1) The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S must not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.

Copyright © 2025 Texas Instruments Incorporated

$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

6.8 Electrical Characteristics

All specifications are at T_A = 25℃ unless otherwise noted

PARAMETER		TEST CONDITIONS	GPN	MIN	TYP	MAX	UNIT
INPUT							
V_F	Input forward voltage	I_F = 5mA	ISOM8110-Q1, ISOM8111-Q1, ISOM8112-Q1, ISOM8113-Q1		1.2	1.4	V
V_F	Input forward voltage	I_F = 5mA, T_A = -40 to 125°C	ISOM8110-Q1, ISOM8111-Q1, ISOM8112-Q1, ISOM8113-Q1		1.2	1.6	V
V_F	Input forward voltage	I_F = ±5mA	ISOM8115-Q1, ISOM8116-Q1, ISOM8117-Q1, ISOM8118-Q1		1.2	1.5	V
V_F	Input forward voltage	I_F = ±5mA, T_A = -40 to 125°C	ISOM8115-Q1, ISOM8116-Q1, ISOM8117-Q1, ISOM8118-Q1		1.2	1.5	V
I_R	Input reverse current	V_R = 5V, T_A = -40 to 125°C	ISOM8110-Q1, ISOM8111-Q1, ISOM8112-Q1, ISOM8113-Q1			10	µA
C_{IN}	Input capacitance	At 1MHz, V_F = 0V	ISOM8110-Q1, ISOM8111-Q1, ISOM8112-Q1, ISOM8113-Q1		19		pF
C_{IN}	Input capacitance	At 1MHz, V_F = 0V	ISOM8115-Q1, ISOM8116-Q1, ISOM8117-Q1, ISOM8118-Q1		6		pF
OUTPUT							
C_{CE}	Collector-emitter capacitance	1MHz, V_F = 0V	ISOM811x-Q1		10		pF
$V_{CE(SAT)}$	Collector-emitter saturation voltage	I_F = 20mA, I_C = 1mA, T_A = -40 to 125°C	ISOM811x-Q1			0.3	V
I_{C_DARK}	Collector dark current	V_{CE} = 20V, I_F = 0mA, T_A = -40 to 125°C	ISOM811x-Q1			100	nA
I_{EC}	Reverse current	V_{EC} = 7V, I_F = 0mA, T_A = -40 to 125°C	ISOM811x-Q1			50	µA
I_{C_OFF}	OFF_state collector current	V_F = 0.7V, V_{CE} = 48V, T_A = -40 to 125°C	ISOM811x-Q1			10	µA
CTR(1)							
CTR	Current Transfer Ratio	I_F = 2mA, V_{CE} = 5V, T_A = -40 to 125°C	ISOM8110-Q1	80	130	180	%
			ISOM8115-Q1	80	130	180	%
			ISOM8111-Q1	120	180	270	%
			ISOM8116-Q1	120	180	270	%
			ISOM8112-Q1	200	300	450	%
			ISOM8117-Q1	200	300	450	%
			ISOM8113-Q1	295	440	655	%
			ISOM8118-Q1	295	440	655	%

Copyright © 2025 Texas Instruments Incorporated

All specifications are at T_A = 25°C unless otherwise noted

PARAMETER		TEST CONDITIONS	GPN	MIN	TYP	MAX	UNIT
CTR	Current Transfer Ratio	I_F = 5mA, V_{CE} = 5V, T_A = -40 to 125°C	ISOM8110-Q1	100	120	155	%
			ISOM8115-Q1	100	120	155	%
			ISOM8111-Q1	150	180	230	%
			ISOM8116-Q1	150	180	230	%
			ISOM8112-Q1	255	300	380	%
			ISOM8117-Q1	255	300	380	%
			ISOM8113-Q1	375	440	560	%
			ISOM8118-Q1	375	440	560	%

(1) CTR (%) = (I_C / I_F) x 100%

Copyright © 2025 Texas Instruments Incorporated

6.9 Switching Characteristics

All specifications are at T_A = 25°C unless otherwise noted

PARAMETER		TEST CONDITIONS	GPN	MIN	TYP	MAX	UNIT
AC							
t_r	Rise time, see Figure 7-2 and Figure 7-3	V_{CC} = 10V, I_C = 2mA, R_L = 100Ω, C_L = 50pF	ISOM8110-Q1		3.2		µs
			ISOM8113-Q1		2.5		µs
t_f	Fall time, see Figure 7-2 and Figure 7-3		ISOM8110-Q1		4.0		µs
			ISOM8113-Q1		7.5		µs
T_{ON}	Turn on time, see Figure 7-2 and Figure 7-3		ISOM8110-Q1, ISOM8115-Q1		5.7		µs
			ISOM8111-Q1, ISOM8116-Q1		4.5		µs
			ISOM8112-Q1, ISOM8117-Q1		6.2		µs
			ISOM8113-Q1, ISOM8118-Q1		16.7		µs
T_{OFF}	Turn off time, see Figure 7-2 and Figure 7-3		ISOM8110-Q1, ISOM8115-Q1		3.6		µs
			ISOM8111-Q1, ISOM8116-Q1		3.7		µs
			ISOM8112-Q1, ISOM8117-Q1		3.1		µs
			ISOM8113-Q1, ISOM8118-Q1		2.7		µs
T_{ON}	Turn on time, see Figure 7-2 and Figure 7-3	V_{CC}=5V, R_L=4.7kΩ, I_F=1.6mA, C_L=50pF	ISOM8110-Q1, ISOM8115-Q1		3.5		µs
			ISOM8111-Q1, ISOM8116-Q1		2.7		µs
			ISOM8112-Q1, ISOM8117-Q1		2.1		µs
			ISOM8113-Q1, ISOM8118-Q1		1.8		µs
T_{OFF}	Turn off time, see Figure 7-2 and Figure 7-3		ISOM8110-Q1, ISOM8115-Q1		8		µs
			ISOM8111-Q1, ISOM8116-Q1		9		µs
			ISOM8112-Q1, ISOM8117-Q1		11.5		µs
			ISOM8113-Q1, ISOM8118-Q1		13.5		µs

Copyright © 2025 Texas Instruments Incorporated

All specifications are at T_A = 25°C unless otherwise noted

PARAMETER		TEST CONDITIONS	GPN	MIN	TYP	MAX	UNIT
T_{ON}	Turn on time, see Figure 7-2 and Figure 7-3	V_{CC}=5V, R_L=1.9kΩ, I_F=16mA, C_L=50pF	ISOM8110-Q1, ISOM8115-Q1		0.62		µs
			ISOM8111-Q1, ISOM8116-Q1		0.56		µs
			ISOM8112-Q1, ISOM8117-Q1		0.48		µs
			ISOM8113-Q1, ISOM8118-Q1		0.44		µs
T_{OFF}	Turn off time, see Figure 7-2 and Figure 7-3		ISOM8110-Q1, ISOM8115-Q1		10		µs
			ISOM8111-Q1, ISOM8116-Q1		11		µs
			ISOM8112-Q1, ISOM8117-Q1		12.3		µs
			ISOM8113-Q1, ISOM8118-Q1		14.5		µs
t_s	Storage time; time required for the output waveform to change from 0% (100%) to 10% (90%) when input is turned on and back off, see Figure 7-3	V_{CC} = 5V, I_F = 1.6mA, R_L = 4.7kΩ	ISOM811x-Q1			21	µs
BW	Bandwidth, see Figure 7-4 and Figure 7-5	V_{IN_DC} = 5V, V_{IN_AC} = 1Vpk, R_{IN} = 2kΩ V_{CC}= 5V, R_{LOAD} = 100Ω, C_L = 50pF, measured at V_{CE} –3dB sinewave	ISOM811x-Q1		680		kHz

Copyright © 2025 Texas Instruments Incorporated

6.10 Typical Characteristics

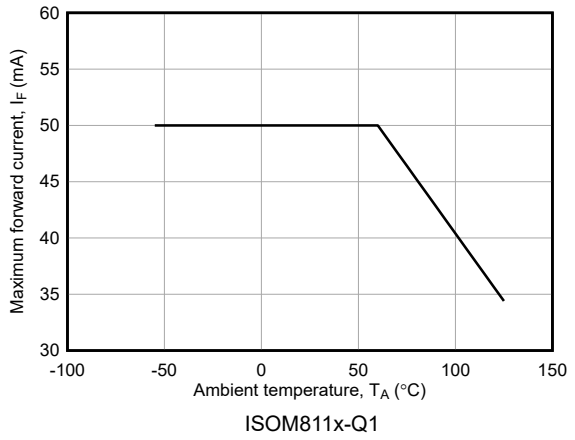


Figure 6-1. Maximum Forward Current vs Ambient Temperature

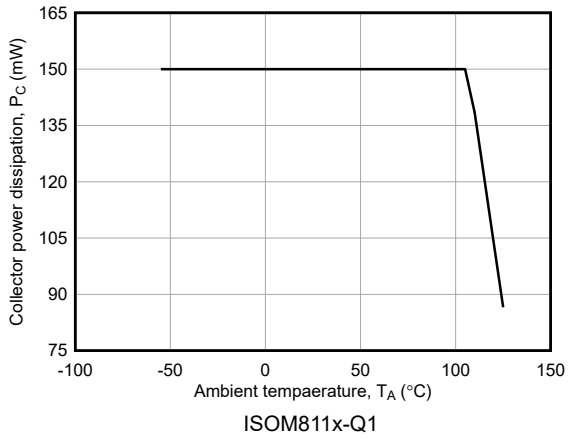


Figure 6-2. Maximum Collector Power Dissipation vs Ambient Temperature

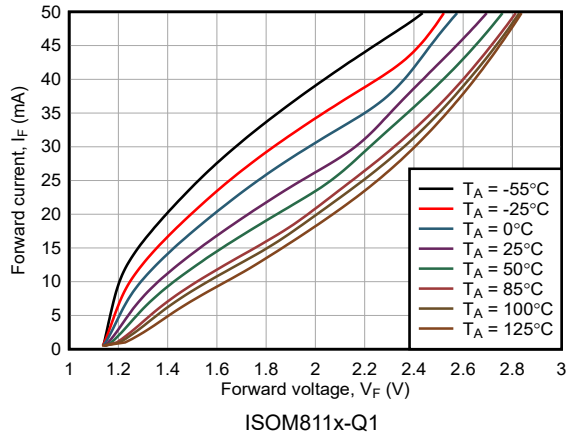


Figure 6-3. Forward Voltage vs Forward Current

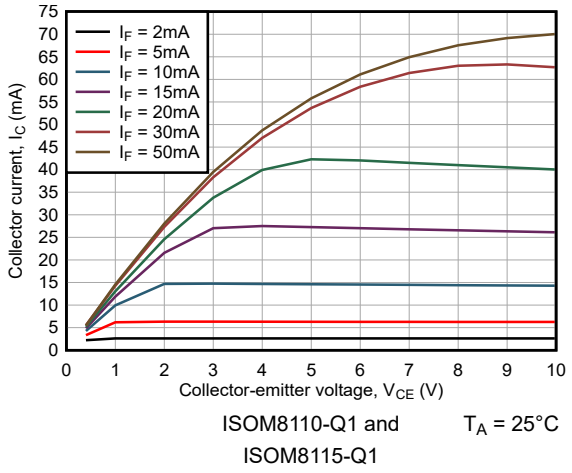


Figure 6-4. Collector Current vs Collector-Emitter Voltage

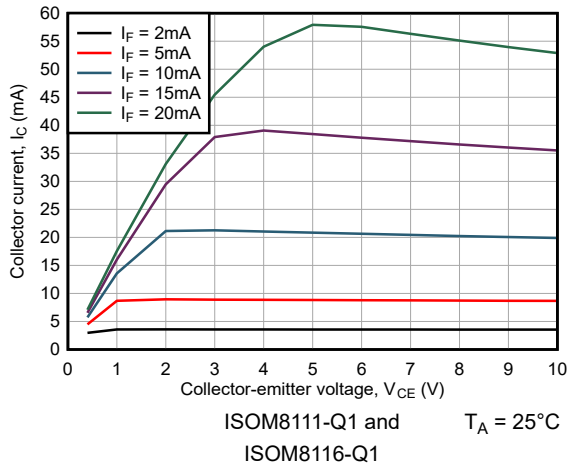


Figure 6-5. Collector Current vs Collector-Emitter Voltage

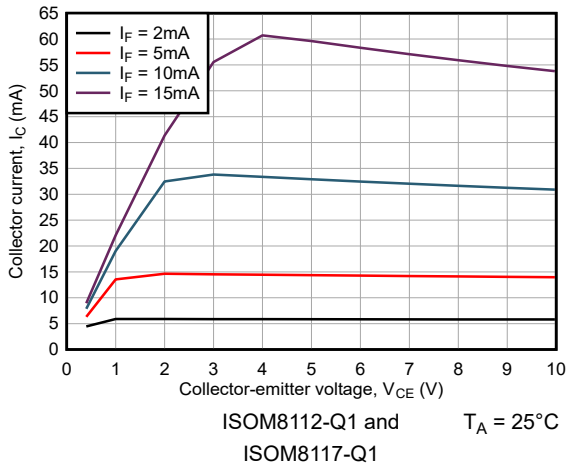


Figure 6-6. Collector Current vs Collector-Emitter Voltage

Copyright © 2025 Texas Instruments Incorporated

6.10 Typical Characteristics (continued)

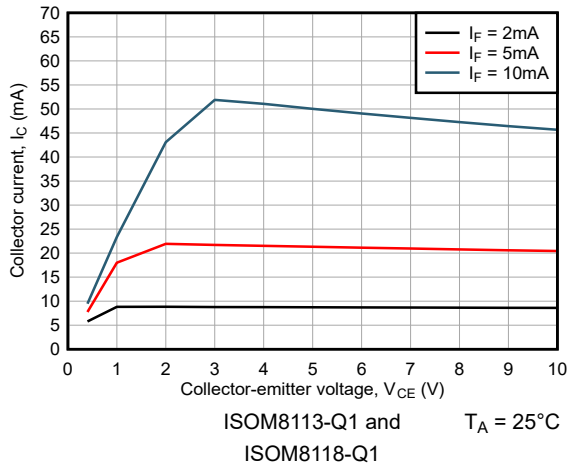


Figure 6-7. Collector Current vs Collector-Emitter Voltage

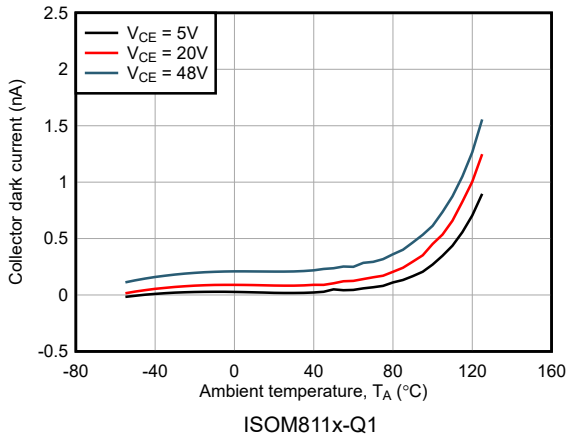


Figure 6-8. Collector Dark Current vs Ambient Temperature

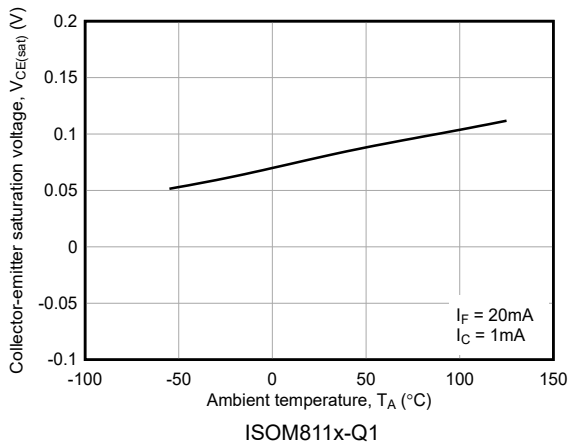


Figure 6-9. Collector-Emitter Saturation Voltage vs Ambient Temperature

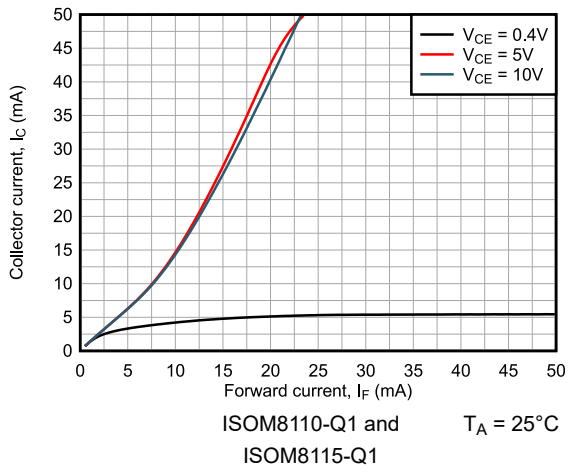


Figure 6-10. Collector Current vs Forward Current

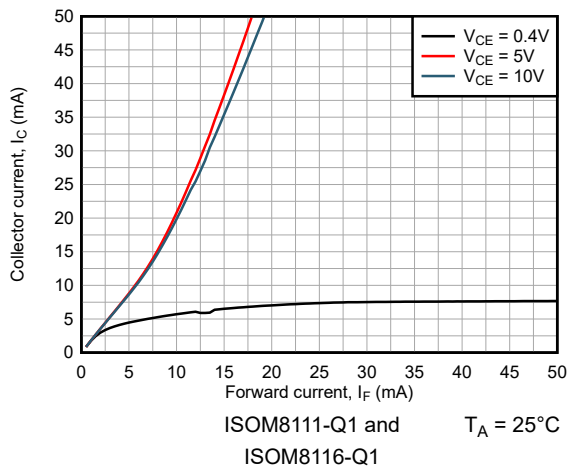


Figure 6-11. Collector Current vs Forward Current

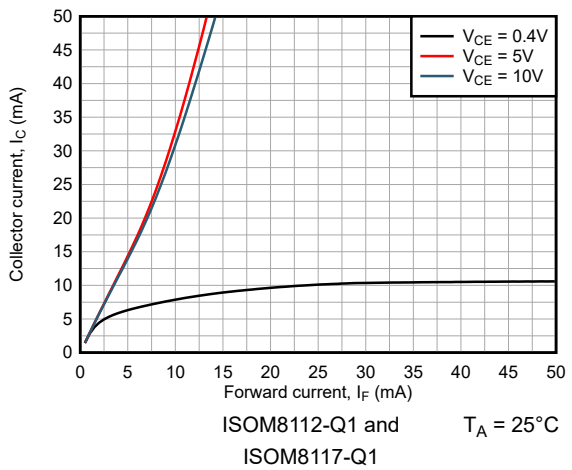


Figure 6-12. Collector Current vs Forward Current

Copyright © 2025 Texas Instruments Incorporated

6.10 Typical Characteristics (continued)

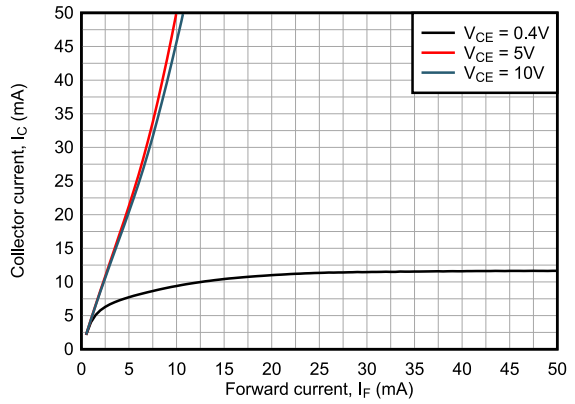


Figure 6-13. Collector Current vs Forward Current

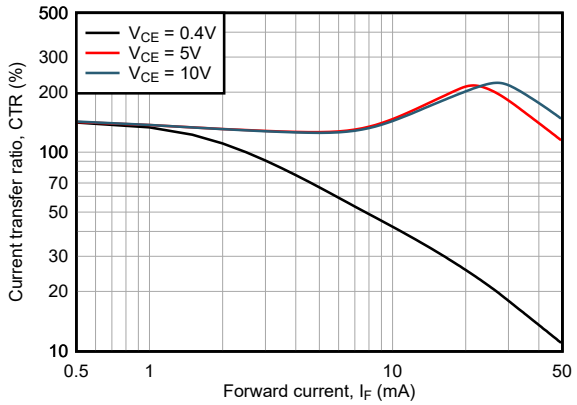


Figure 6-14. Current Transfer Ratio vs Forward Current

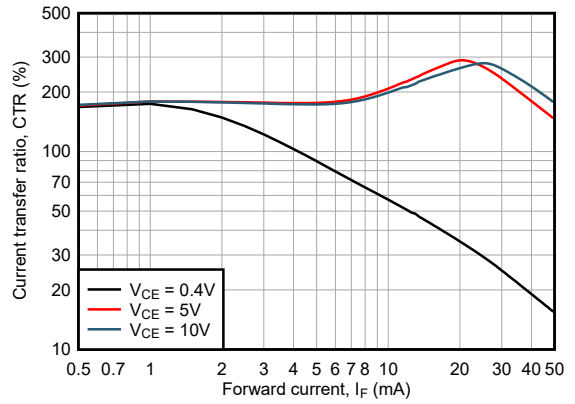


Figure 6-15. Current Transfer Ratio vs Forward Current

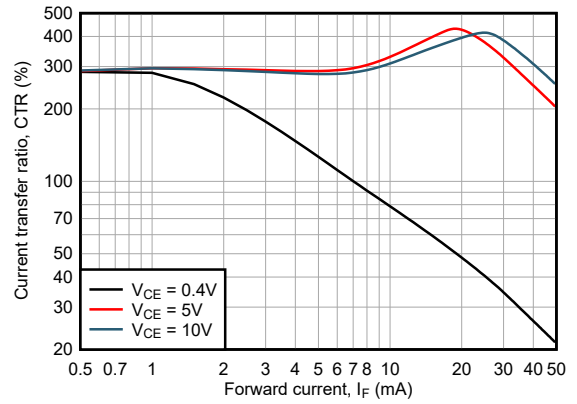


Figure 6-16. Current Transfer Ratio vs Forward Current

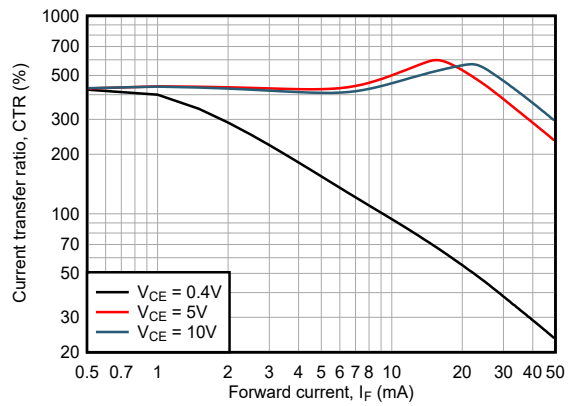


Figure 6-17. Current Transfer Ratio vs Forward Current

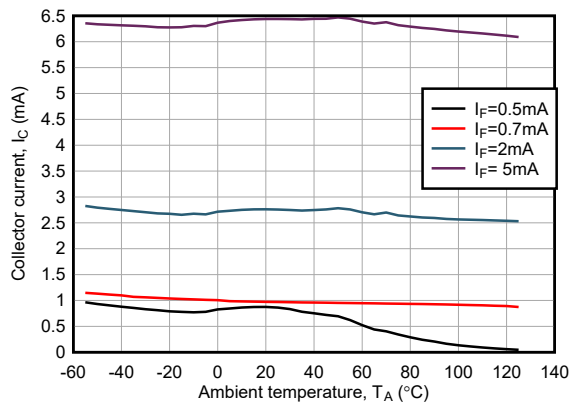
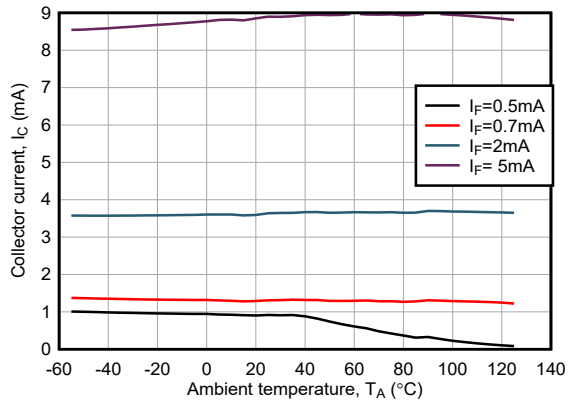


Figure 6-18. Collector Current vs Ambient Temperature

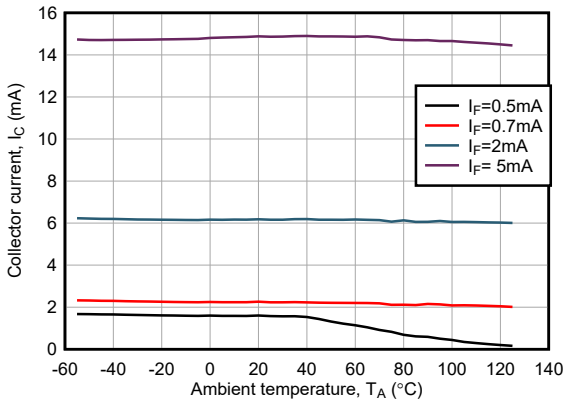
Copyright © 2025 Texas Instruments Incorporated

6.10 Typical Characteristics (continued)



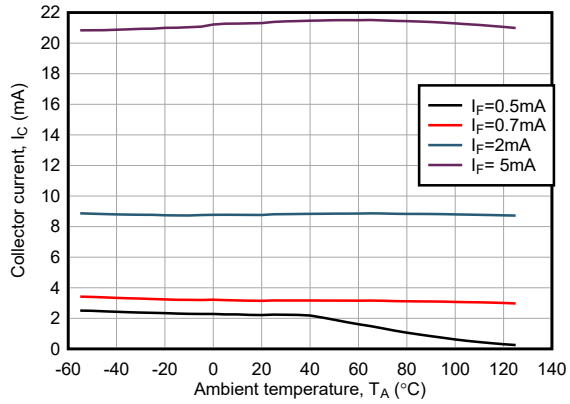
ISOM8111-Q1 and ISOM8116-Q1 V_{CE} = 5V

Figure 6-19. Collector Current vs Ambient Temperature



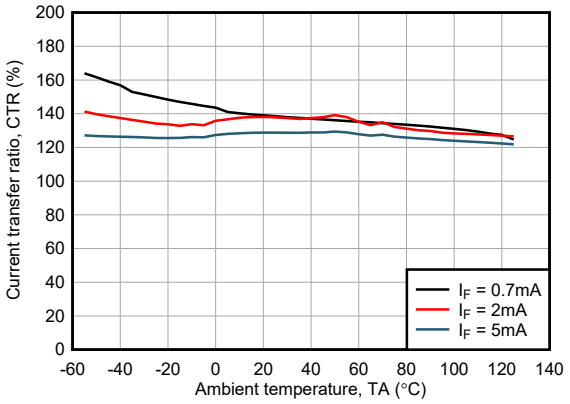
ISOM8112-Q1 and ISOM8117-Q1 V_{CE} = 5V

Figure 6-20. Collector Current vs Ambient Temperature



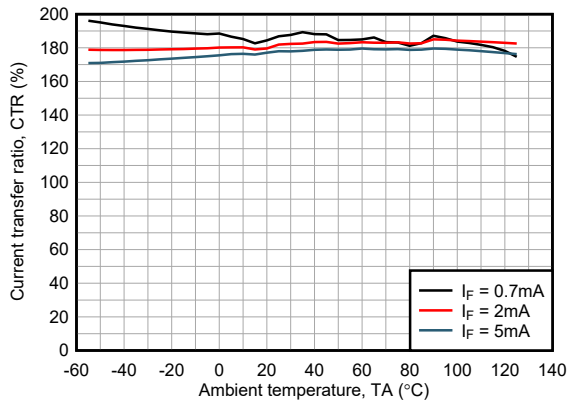
ISOM8113-Q1 and ISOM8118-Q1 V_{CE} = 5V

Figure 6-21. Collector Current vs Ambient Temperature



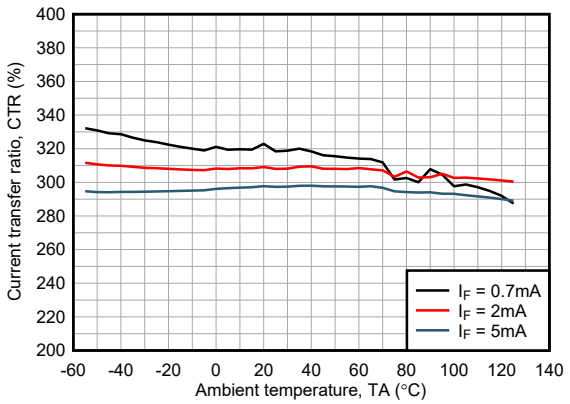
ISOM8110-Q1 and ISOM8115-Q1 V_{CE} = 5V

Figure 6-22. Current Transfer Ratio vs Ambient Temperature



ISOM8111-Q1 and ISOM8116-Q1 V_{CE} = 5V

Figure 6-23. Current Transfer Ratio vs Ambient Temperature

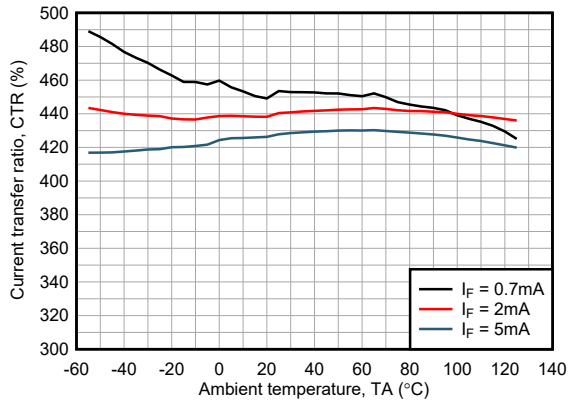


ISOM8112-Q1 and ISOM8117-Q1 V_{CE} = 5V

Figure 6-24. Current Transfer Ratio vs Ambient Temperature

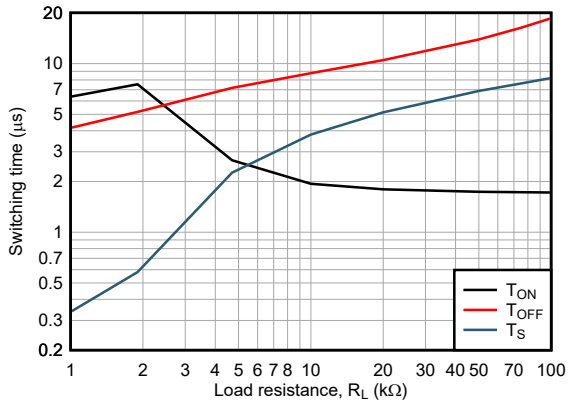
Copyright © 2025 Texas Instruments Incorporated

6.10 Typical Characteristics (continued)



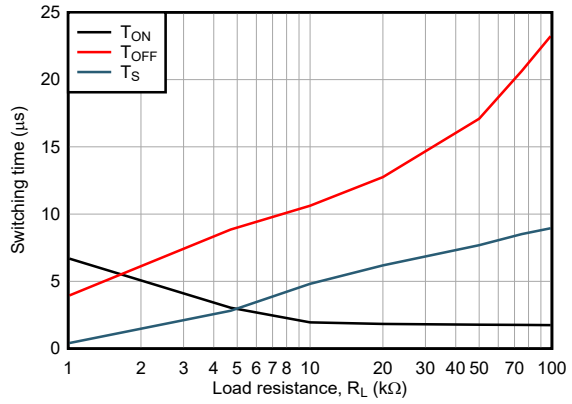
ISOM8113-Q1 and ISOM8118-Q1 V_{CE} = 5V

Figure 6-25. Current Transfer Ratio vs Ambient Temperature



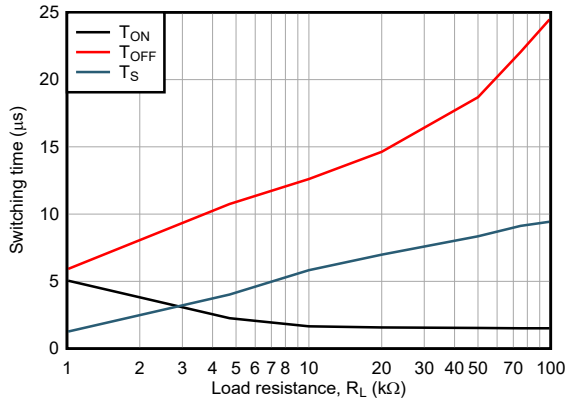
I_F = 1.6mA ISOM8110-Q1 and ISOM8115-Q1 V_{CC} = 5V

Figure 6-26. Switching Time vs Load Resistance



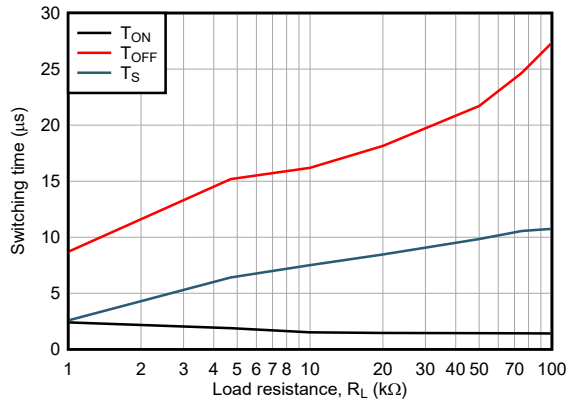
I_F = 1.6mA ISOM8111-Q1 and ISOM8116-Q1 V_{CC} = 5V

Figure 6-27. Switching Time vs Load Resistance



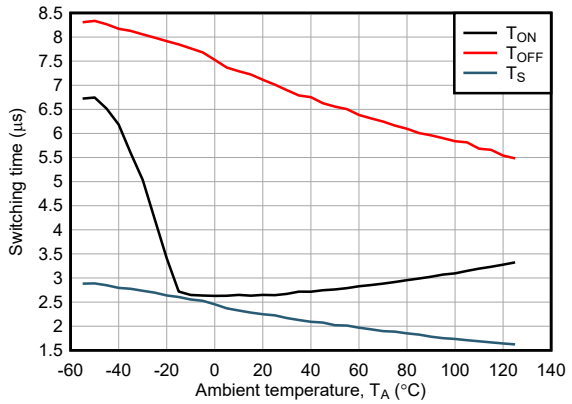
I_F = 1.6mA ISOM8112-Q1 and ISOM8117-Q1 V_{CC} = 5V

Figure 6-28. Switching Time vs Load Resistance



I_F = 1.6mA ISOM8113-Q1 and ISOM8118-Q1 V_{CC} = 5V

Figure 6-29. Switching Time vs Load Resistance



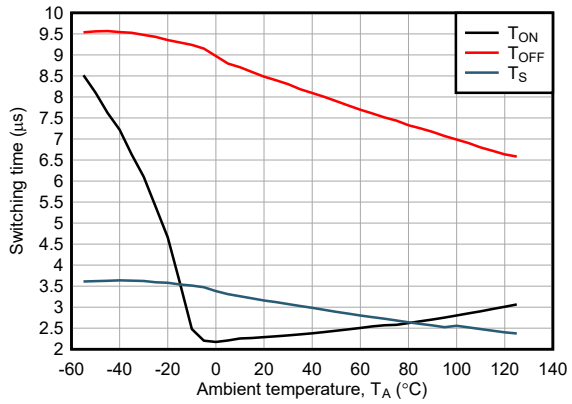
I_F = 1.6mA ISOM8110-Q1 and ISOM8115-Q1 V_{CC} = 5V

R_L = 4.7kΩ

Figure 6-30. Switching Time vs Ambient Temperature

Copyright © 2025 Texas Instruments Incorporated

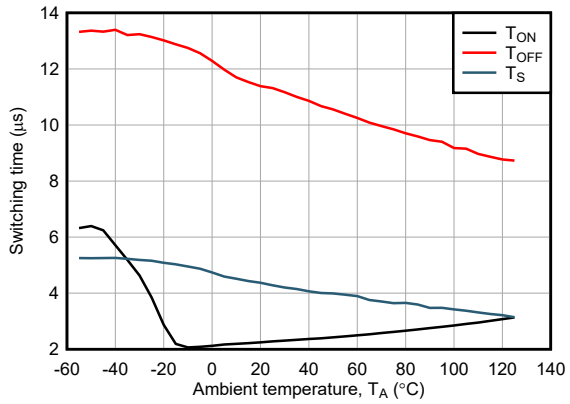
6.10 Typical Characteristics (continued)



I_F = 1.6mA ISOM8111-Q1 and ISOM8116-Q1 V_{CC} = 5V

R_L = 4.7kΩ

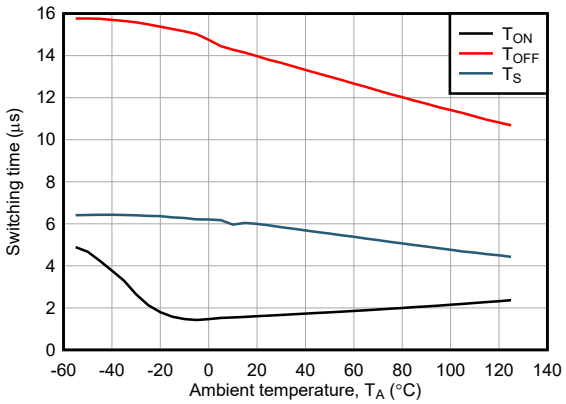
Figure 6-31. Switching Time vs Ambient Temperature



I_F = 1.6mA ISOM8112-Q1 and ISOM8117-Q1 V_{CC} = 5V

R_L = 4.7kΩ

Figure 6-32. Switching Time vs Ambient Temperature



I_F = 1.6mA ISOM8113-Q1 and ISOM8118-Q1 V_{CC} = 5V

R_L = 4.7kΩ

Figure 6-33. Switching Time vs Ambient Temperature

Copyright © 2025 Texas Instruments Incorporated

7 Parameter Measurement Information

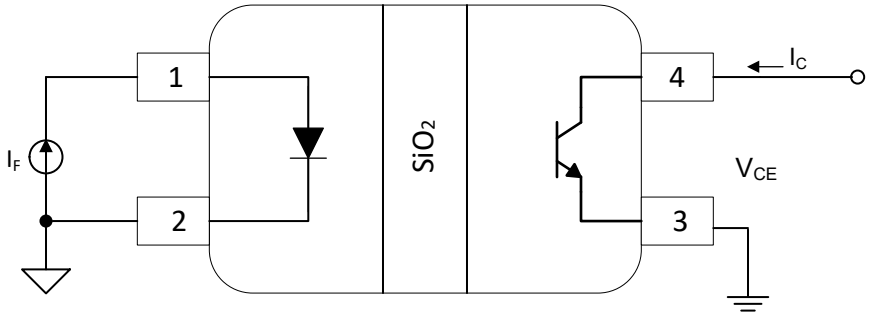


Figure 7-1. ISOM811x-Q1 Test Circuit for CTR

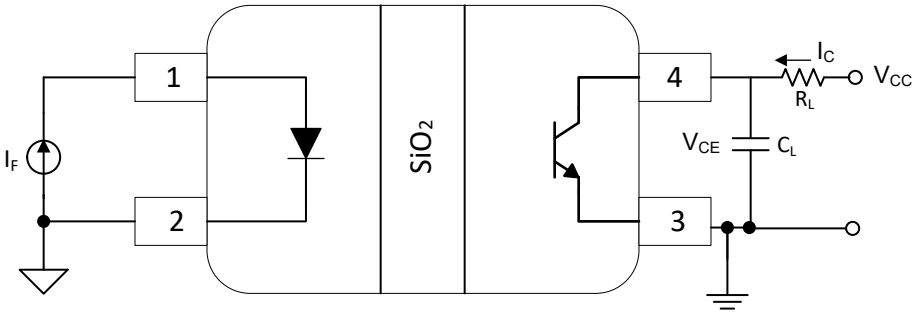


Figure 7-2. ISOM811x-Q1 Test Circuit for Switching Timing

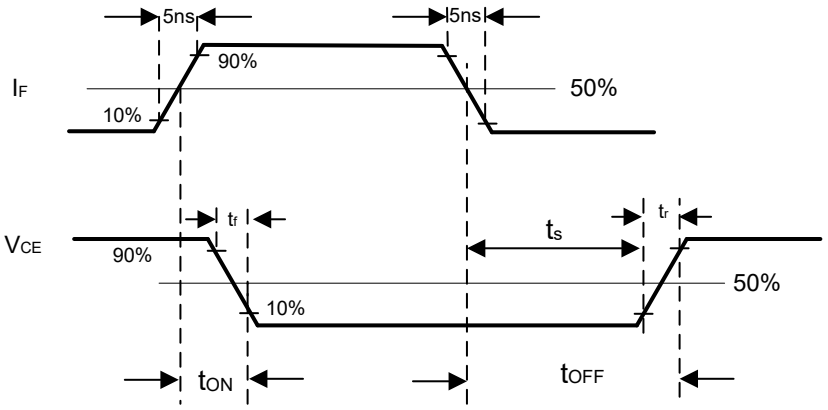


Figure 7-3. ISOM811x-Q1 Switching Timing Waveforms

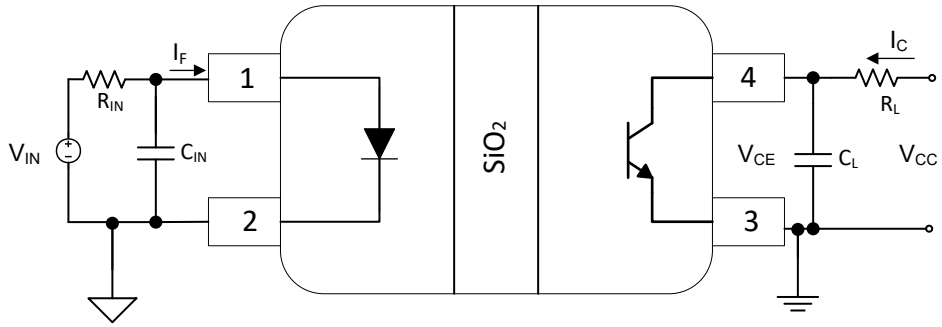


Figure 7-4. ISOM811[0-3]-Q1 Test Circuit for Bandwidth

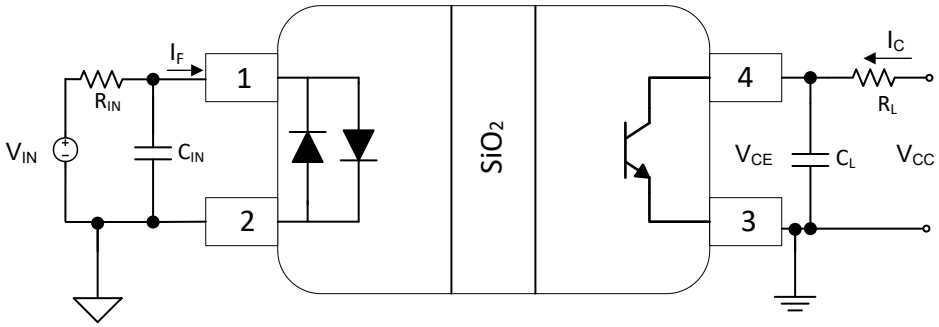


Figure 7-5. ISOM811[5-8]-Q1 Test Circuit for Bandwidth

8 Detailed Description

8.1 Overview

The ISOM811x-Q1 opto-emulators are single-channel, pin-to-pin upgrades for many traditional optocouplers. While standard optocouplers use an LED as the input stage, ISOM811x-Q1 uses an emulated LED as the input stage. The input and output stages are isolated by TI's proprietary silicon dioxide-based (SiO_2) isolation barrier. This isolation technology makes ISOM811x-Q1 resistant to the wear-out effects found in optocouplers that degrade performance with increasing temperature, forward current, and device age. Ordering options include four different ranges of current transfer ratio (CTR) and input options supporting uni-polar and bi-polar DC flow.

The ISOM811x-Q1 family of devices isolate DC and bidirectional DC signals and offer performance, reliability, and flexibility advantages not available with traditional optocouplers.

The functional block diagram of ISOM811x-Q1 devices are shown in Section 8.2. The input signal is transmitted across the isolation barrier using an on-off keying (OOK) modulation scheme. The transmitter sends a high-frequency carrier across the barrier that contains information on how much current is flowing through the input pins. The receiver demodulates the signal after advanced signal conditioning and produces the signal through the output stage. These devices also incorporate advanced circuit techniques to maximize bandwidth and minimize radiated emissions. Figure 8-3 shows conceptual details of how the OOK scheme works.

8.2 Functional Block Diagram

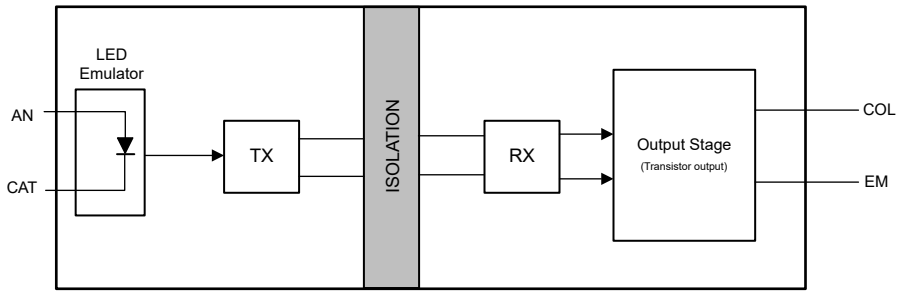


Figure 8-1. Conceptual Block Diagram of an Opto-emulator ISOM811[0-3]-Q1

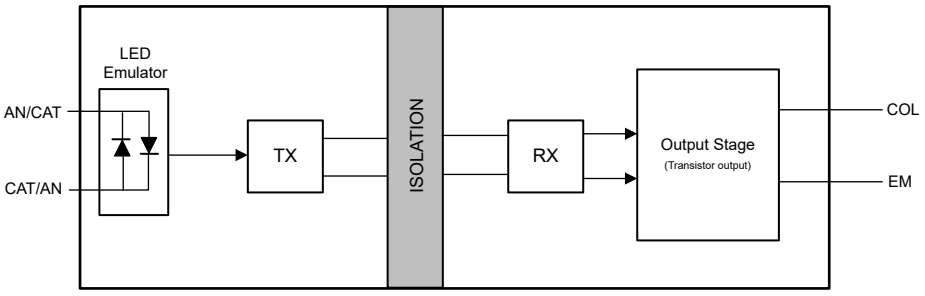


Figure 8-2. Conceptual Block Diagram of an Opto-emulator ISOM811[5-8]-Q1

Copyright © 2025 Texas Instruments Incorporated

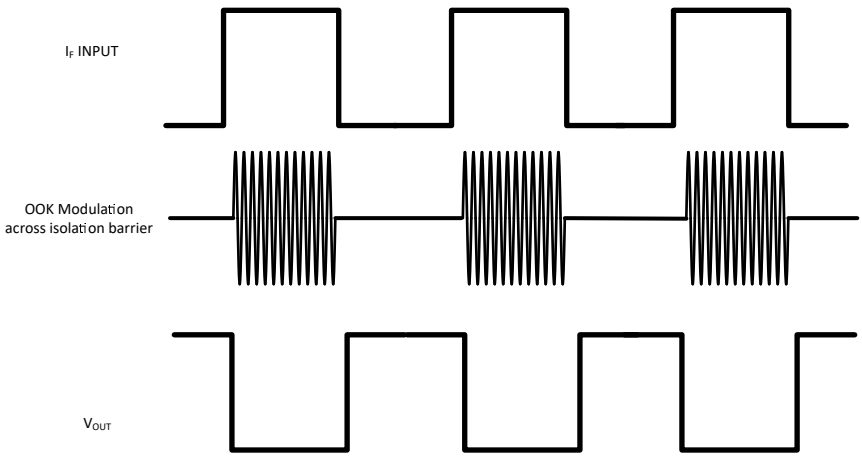


Figure 8-3. On-off Keying (OOK) Based Modulation Scheme

8.3 Feature Description

The ISOM811x-Q1 devices isolate DC and bidirectional DC signals. ISOM811x-Q1 has an open-collector output with multiple CTR options. Depending on the package option being used, these devices can support an isolation withstand voltage (V_{ISO}) up to 5000V_{RMS} between side 1 and side 2.

8.4 Device Functional Modes

Table 8-1 lists the functional modes for the ISOM811x-Q1 devices.

Table 8-1. Function Table

CTR [1]	PART NUMBER	Input type
100% to 155%	ISOM8110-Q1	DC
	ISOM8115-Q1	Bidirectional DC
150% to 230%	ISOM8111-Q1	DC
	ISOM8116-Q1	Bidirectional DC
255% to 380%	ISOM8112-Q1	DC
	ISOM8117-Q1	Bidirectional DC
375% to 560%	ISOM8113-Q1	DC
	ISOM8118-Q1	Bidirectional DC

1. I_F = 5mA, T_A = 25°C, V_{CE} = 5V.

Copyright © 2025 Texas Instruments Incorporated

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The ISOM811x-Q1 devices are single-channel opto-emulators with LED-emulator input and transistor output. The devices use on-off keying modulation to transmit data across the isolation barrier. The input stage is isolated from the driver stage by TI's proprietary silicon dioxide-based (SiO_2) isolation barrier which provides robust isolation. With wider temperature ratings than traditional optocouplers, ISOM811x-Q1 opto-emulators can provide reliable signal isolation in harsh environments.

The ISOM811x-Q1 devices are capable of sinking current when subjected to an external load being connected to the device. Like typical transistor output optocouplers, the output current depends on the input current level (I_F) and the current transfer ratio (CTR). With multiple CTR options (100% - 560%), low input current, high bandwidth, low turn-off delay, low power consumption, and wider temperature range, ISOM811x-Q1 devices are designed for use in a variety of industries such as factory automation, building automation, e-mobility, automotive, avionics, medical, and power delivery.

9.1.1 Typical Application

ISOM811x-Q1 opto-emulators are commonly used in the feedback control loops of isolated power supplies. These devices are used to solve the problem of feeding back current while isolating the primary and secondary domains to regulate the output voltage.

In power supplies, the output voltage is isolated from main input voltage using a transformer (for example: flyback converter). For analog power supply units, the controller IC is typically on the primary side of the transformer. For closed loop control, measuring the output voltage on the secondary side and feeding the voltage back to the controller on the primary is necessary. The most common method of achieving this design is using an opto-emulator such as ISOM811x-Q1, error amplifier (commonly TL431), and a voltage comparator to form a feedback loop across the isolation barrier

Figure 9-1 illustrates a typical isolated power supply. In this implementation, the output voltage is sensed by an error amplifier using the resistor divider (R1 and R2). Depending on the voltage level that the error amplifier senses, the TL431 can drive the current of the ISOM811x-Q1 higher or lower which is then compared to a voltage reference. The information is passed across the isolation barrier through ISOM811x-Q1 to the primary side, where the PWM control circuit modulates the power stage to regulate the output voltage. The TL431 and ISOM811x-Q1 play an important role for stable feedback and control loop.

The ISOM811x-Q1 devices enable improvements in transient response, reliability, and stability as compared to commonly used optocoupler as the CTR is stable over wide temperature range providing a small, low-cost, highly reliable, and easy-to-design implementation.

Copyright © 2025 Texas Instruments Incorporated

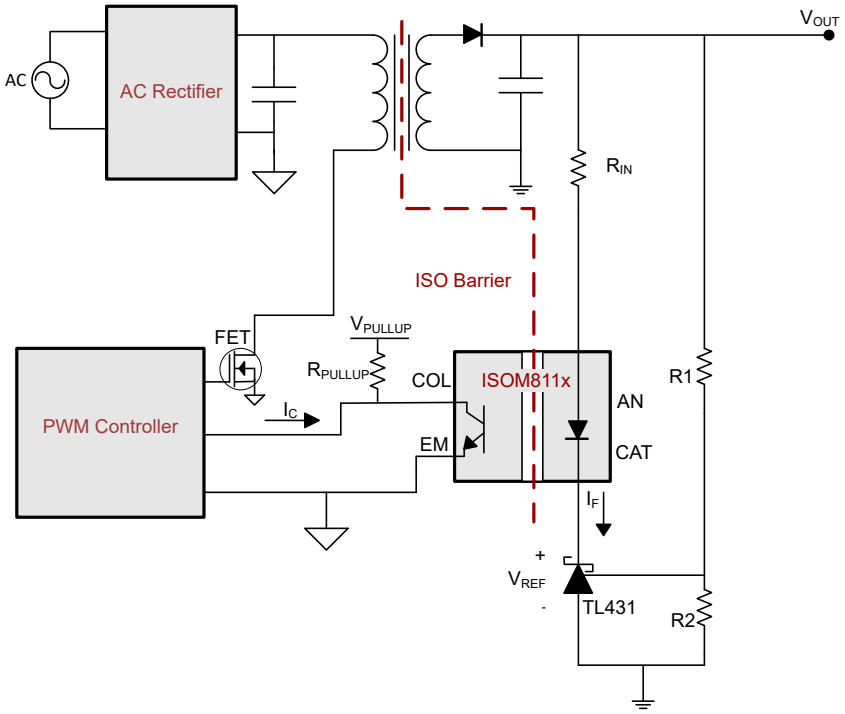


Figure 9-1. Typical Isolated Power Supply Application Using ISOM811x-Q1

9.1.1.1 Design Requirements

To design with ISOM811x-Q1 devices, use the parameters listed in Table 9-1.

Table 9-1. Design Parameters

PARAMETER	VALUE
Input forward current range, I_F	0.7mA (min), 20mA (max)
Current transfer ratio at I_F = 5mA, CTR	100% to 155%
Collector current tolerance, I_C	50mA (max)
Collector-emitter voltage (saturation), $V_{CE(SAT)}$	0.3V (max)
Input forward voltage, V_F	1.2V (typ)

9.1.1.2 Detailed Design Procedure

This section presents the design procedure for using the ISOM811x-Q1 opto-emulators. External components must be selected to operate ISOM811x-Q1 within the *Recommended Operating Conditions*. The following recommendations on component selection focus on the design of a typical feedback control loop for an isolated flyback converter.

When using an optocoupler in a feedback control loop for an isolated power supply, many variables can affect how to properly use the optocoupler, including the output voltage of the power supply and the type of controller the feedback signal is being sent to. For this example, assume that the output voltage of this power supply, V_{OUT}, is 5V, and the PWM controller being used has an integrated error amplifier with a COMP pin that acts as the output of this amplifier.

9.1.1.2.1 Sizing R_{PULLUP}

The transistor output of ISOM811x-Q1 operates in active, saturation, reverse, and cut-off regions, just like a regular transistor. To verify that the output does not get damaged when the output is saturated, the minimum value of R_{PULLUP} can be calculated for a given pull-up voltage, V_{PULLUP}, in Equation 1:

$$R_{PULLUP} > \frac{V_{PULLUP} - V_{CE(SAT)}}{I_{C(MAX)}} \quad (1)$$

For the example of a feedback loop application, we can calculate the minimum required value for R_{PULLUP} for a given V_{PULLUP} of 10V, the maximum output voltage of the error amplifier ($V_{COMP(MAX)}$ of 2.5V, and the maximum output current of the error amplifier is internally clamped at 1.6mA. The equation to calculate R_{PULLUP} is shown in Equation 2:

$$R_{PULLUP} > \frac{V_{PULLUP} - V_{COMP(MAX)}}{I_{COMP(CLAMP)}} = \frac{10V - 2.5V}{1.6mA} = 4.66k\Omega \quad (2)$$

9.1.1.2.2 Sizing R_{IN}

The input side of ISOM811x-Q1 is current-driven. To limit the amount of current flowing into the AN pin, placing a series resistor, R_{IN}, in series with the input as shown in Figure 9-1 is recommended.

Depending on how the ISOM811x-Q1 device is being used, the value of R_{IN} can vary quite a bit. However, at a high level, to make sure the input does not get damaged, the minimum value of R_{IN} can be calculated for a given input voltage, V_{IN}, in Equation 3:

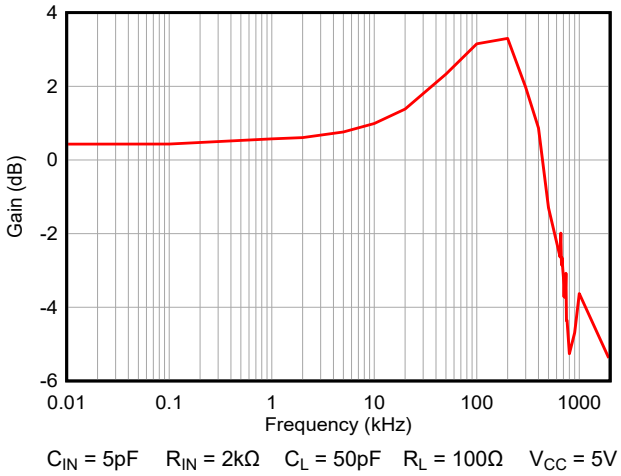
$$R_{IN} > \frac{V_{IN} - V_F}{I_{C(MAX)}} \quad (3)$$

However, in the use case of a feedback loop, R_{IN} directly affects the mid-band gain of the loop. Assuming that the TL431 has been configured to give a reference voltage, V_{REF}, of 2.5V and R_{PULLUP} is 5kΩ, Equation 4 is used to calculate the maximum value of R_{IN} verifying that the V_{COMP} voltage on the primary side can be pulled to the saturation voltage of the ISOM811x-Q1, $V_{CE(SAT)}$.

$$R_{IN} < \frac{(V_{OUT} - V_{REF} - V_F) \times R_{PULLUP} \times CTR_{MIN}}{V_{PULLUP} - V_{CE(SAT)}} = \frac{(5V - 2.5V - 1.2V) \times 5k\Omega \times 100\%}{10V - 0.3V} = 670\Omega \quad (4)$$

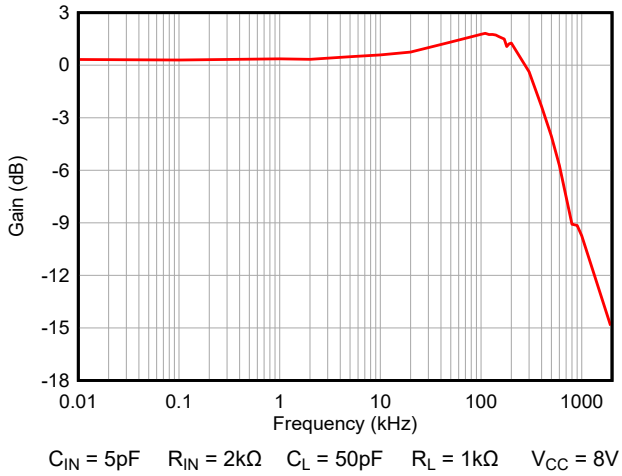
9.1.1.3 Application Curves

The following curves show ISOM8110-Q1 bandwidth performance over different loading conditions where V_{IN} = $5V_{DC}$ + $2V_{PK}$. See Figure 7-4 for setup details.



C_{IN} = 5pF R_{IN} = 2kΩ C_L = 50pF R_L = 100Ω V_{CC} = 5V

Figure 9-2. Bandwidth at R_L = 100Ω



C_{IN} = 5pF R_{IN} = 2kΩ C_L = 50pF R_L = 1kΩ V_{CC} = 8V

Figure 9-3. Bandwidth at R_L = 1kΩ

Copyright © 2025 Texas Instruments Incorporated

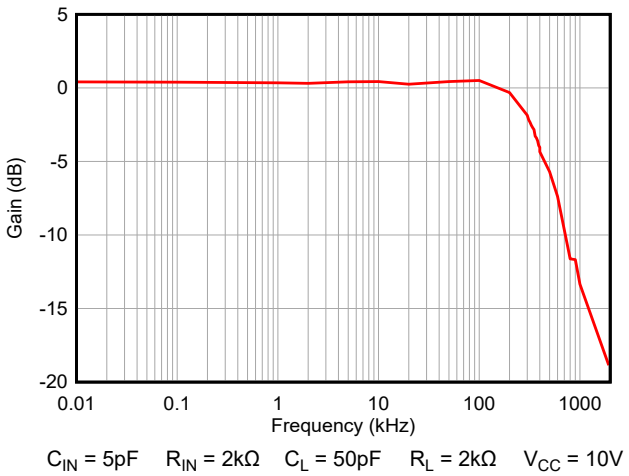


Figure 9-4. Bandwidth at R_L = 2kΩ

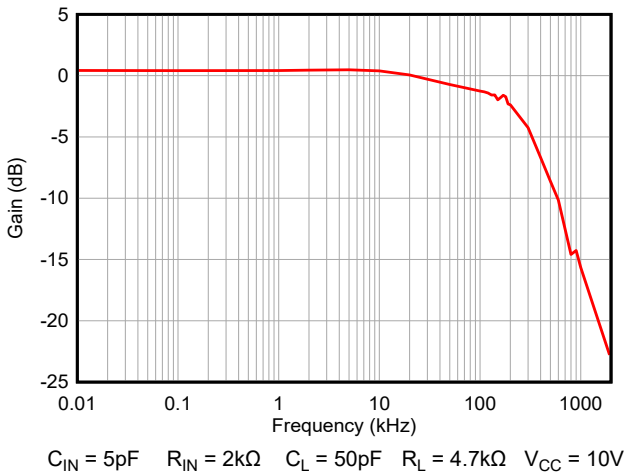


Figure 9-5. Bandwidth at R_L = 4.7kΩ

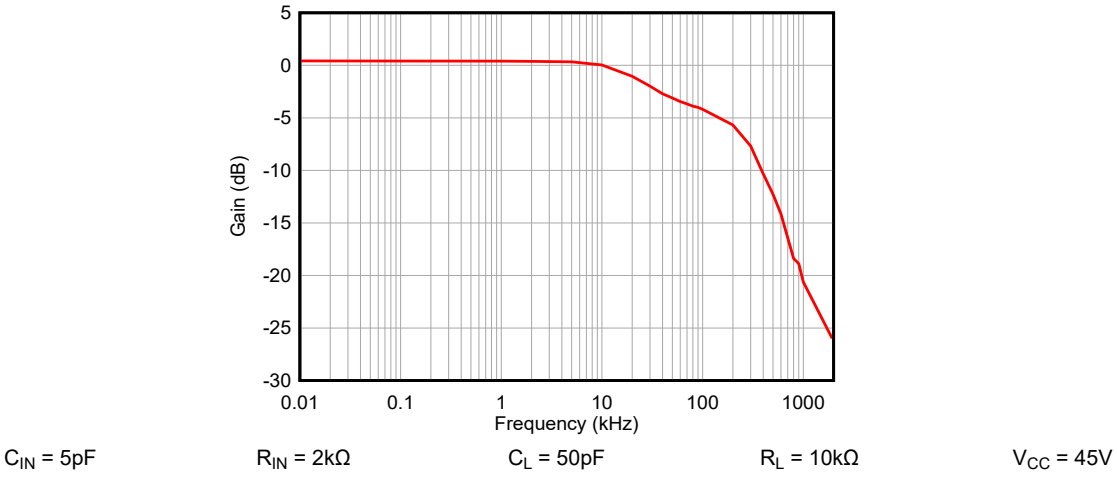


Figure 9-6. Bandwidth at R_L = 10kΩ

9.1.1.3.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; see Figure 9-7 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that's 20% higher than the specified value.

Figure 9-8 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over the lifetime of the barrier. Based on the TDDB data, the intrinsic capability of the insulation is 500V_{RMS} with a lifetime of 44. Other factors such as package size, pollution degree, and material group can further limit the working voltage of a component.

Copyright © 2025 Texas Instruments Incorporated

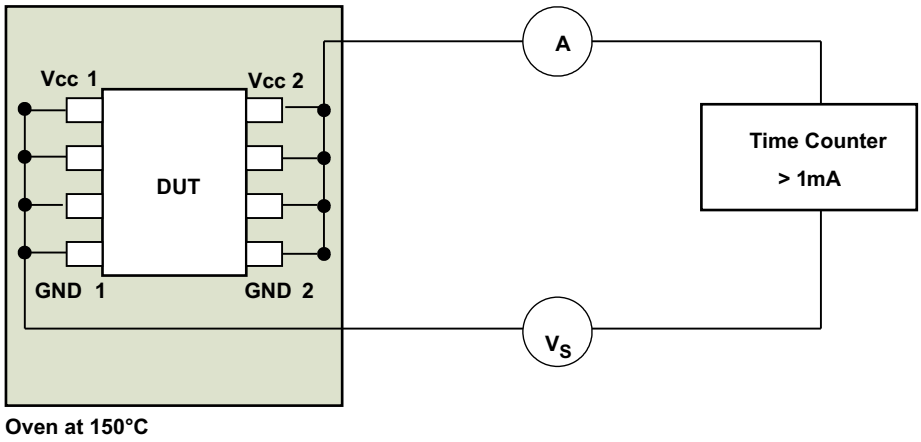


Figure 9-7. Test Setup for Insulation Lifetime Measurement

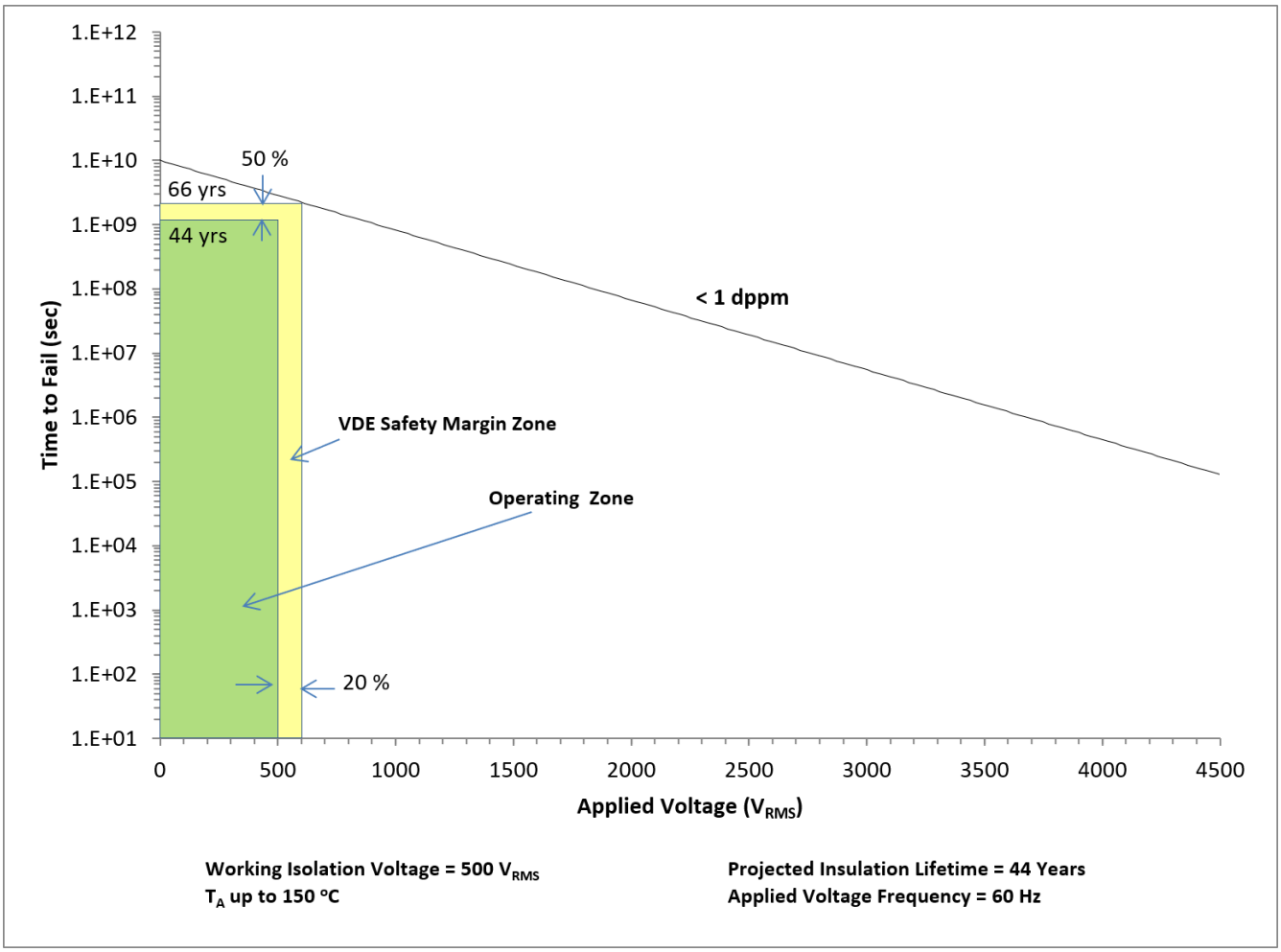


Figure 9-8. Insulation Lifetime Projection Data

Copyright © 2025 Texas Instruments Incorporated

9.2 Power Supply Recommendations

ISOM811x-Q1 does not require a dedicated power supply to operate since there is no supply pin. Take care to not violate recommended I/O specifications for proper device functionality.

9.3 Layout

9.3.1 Layout Guidelines

- The device connections to ground must be tied to the PCB ground plane using a direct connection or two vias to help minimize inductance.
- The connections of capacitors and other components to the PCB ground plane must use a direct connection or two vias for minimum inductance.

9.3.2 Layout Example

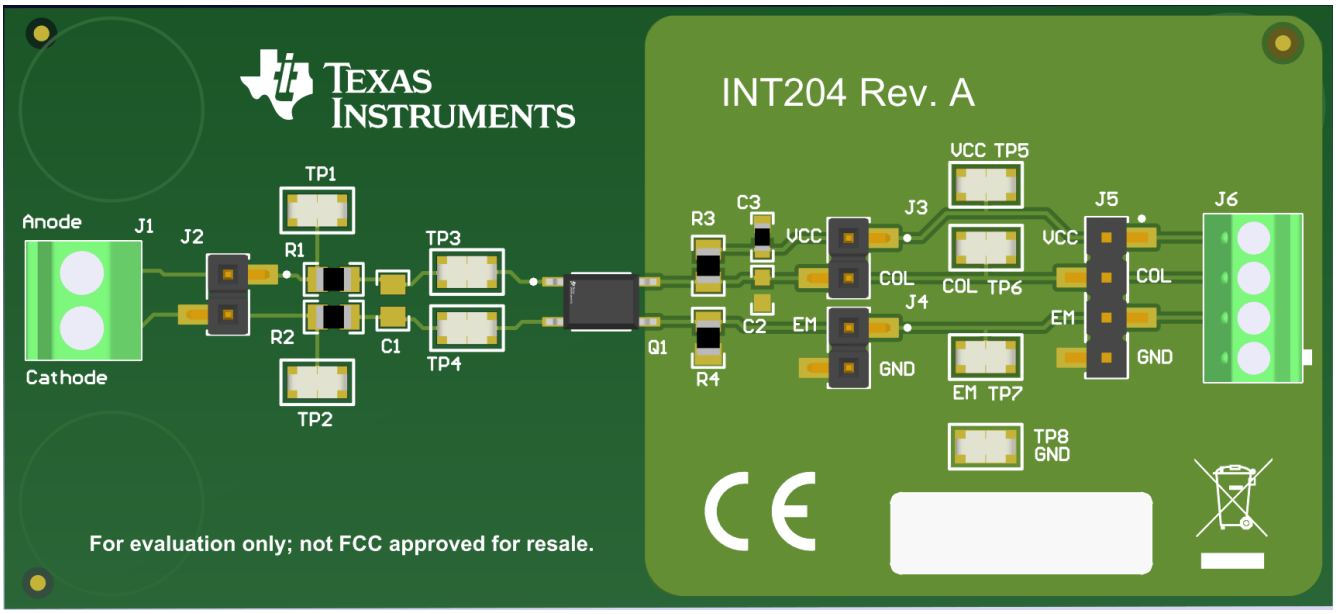


Figure 9-9. Layout Example of ISOM811x-Q1 With a Single Layer Board

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Isolation Glossary,* application note
- Texas Instruments, *Introduction to Opto-Emulators,* application note
- Texas Instruments, *ISOM8110 Single-Channel Opto-Emulator with Analog Transistor Output Evaluation Module,* EVM user's guide

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (April 2025) to Revision E (September 2025)	Page
• Updated the number formatting for figures, tables, and cross-references throughout the document	1
• Updated with released DFS package information	1
• Changed to 500Vrms to match VIOWM	5
• Removed 'planned' added certificate information	6
• Added Insulation Lifetime section	23

Changes from Revision C (October 2024) to Revision D (April 2025)	Page
• Updated the number formatting for figures, tables, and cross-references throughout the document	1
• Updated with preview DFS package information	1

Copyright © 2025 Texas Instruments Incorporated

Changes from Revision B (August 2024) to Revision C (October 2024)	Page
• Updated the number formatting for figures, tables, and cross-references throughout the document	1

Changes from Revision A (December 2023) to Revision B (August 2024)	Page
• Updated the number formatting for figures, tables, and cross-references throughout the document	1
• Added *Device and Documentation Support* section	26

Changes from Revision * (April 2024) to Revision A (July 2024)	Page
• Updated the number formatting for figures, tables, and cross-references throughout the document	1
• Updated the package and device information throughout the document	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2025 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISOM8110DFGRQ1	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8110
ISOM8110DFGRQ1.A	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8110
ISOM8110DFGRQ1.B	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISOM8110DFHRQ1	Active	Production	SOIC (DFH) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8110
ISOM8110DFHRQ1.A	Active	Production	SOIC (DFH) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8110
ISOM8110DFHRQ1.B	Active	Production	SOIC (DFH) | 4	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISOM8110DFSRQ1	Active	Production	SOIC (DFS) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8110
ISOM8110DFSRQ1.A	Active	Production	SOIC (DFS) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8110
ISOM8110DFSRQ1.B	Active	Production	SOIC (DFS) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8110
ISOM8111DFGRQ1	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8111
ISOM8111DFGRQ1.A	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8111
ISOM8111DFGRQ1.B	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISOM8111DFHRQ1	Active	Production	SOIC (DFH) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8111
ISOM8111DFHRQ1.A	Active	Production	SOIC (DFH) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8111
ISOM8111DFHRQ1.B	Active	Production	SOIC (DFH) | 4	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISOM8111DFSRQ1	Active	Production	SOIC (DFS) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8111
ISOM8111DFSRQ1.A	Active	Production	SOIC (DFS) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8111
ISOM8111DFSRQ1.B	Active	Production	SOIC (DFS) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8111
ISOM8112DFGRQ1	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8112
ISOM8112DFGRQ1.A	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8112
ISOM8112DFGRQ1.B	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISOM8112DFHRQ1	Active	Production	SOIC (DFH) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8112
ISOM8112DFHRQ1.A	Active	Production	SOIC (DFH) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8112
ISOM8112DFHRQ1.B	Active	Production	SOIC (DFH) | 4	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISOM8112DFSRQ1	Active	Production	SOIC (DFS) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8112
ISOM8112DFSRQ1.A	Active	Production	SOIC (DFS) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8112
ISOM8112DFSRQ1.B	Active	Production	SOIC (DFS) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8112
ISOM8113DFGRQ1	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8113
ISOM8113DFGRQ1.A	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8113

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISOM8113DFGRQ1.B	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISOM8113DFHRQ1	Active	Production	SOIC (DFH) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8113
ISOM8113DFHRQ1.A	Active	Production	SOIC (DFH) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8113
ISOM8113DFHRQ1.B	Active	Production	SOIC (DFH) | 4	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISOM8113DFSRQ1	Active	Production	SOIC (DFS) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8113
ISOM8113DFSRQ1.A	Active	Production	SOIC (DFS) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8113
ISOM8113DFSRQ1.B	Active	Production	SOIC (DFS) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8113
ISOM8115DFGRQ1	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8115
ISOM8115DFGRQ1.A	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8115
ISOM8115DFGRQ1.B	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISOM8115DFHRQ1	Active	Production	SOIC (DFH) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8115
ISOM8115DFHRQ1.A	Active	Production	SOIC (DFH) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8115
ISOM8115DFHRQ1.B	Active	Production	SOIC (DFH) | 4	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISOM8115DFSRQ1	Active	Production	SOIC (DFS) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8115
ISOM8115DFSRQ1.A	Active	Production	SOIC (DFS) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8115
ISOM8115DFSRQ1.B	Active	Production	SOIC (DFS) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8115
ISOM8116DFGRQ1	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8116
ISOM8116DFGRQ1.A	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8116
ISOM8116DFGRQ1.B	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISOM8116DFHRQ1	Active	Production	SOIC (DFH) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8116
ISOM8116DFHRQ1.A	Active	Production	SOIC (DFH) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8116
ISOM8116DFHRQ1.B	Active	Production	SOIC (DFH) | 4	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISOM8116DFSRQ1	Active	Production	SOIC (DFS) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8116
ISOM8116DFSRQ1.A	Active	Production	SOIC (DFS) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8116
ISOM8116DFSRQ1.B	Active	Production	SOIC (DFS) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8116
ISOM8117DFGRQ1	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8117
ISOM8117DFGRQ1.A	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8117
ISOM8117DFGRQ1.B	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISOM8117DFHRQ1	Active	Production	SOIC (DFH) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8117
ISOM8117DFHRQ1.A	Active	Production	SOIC (DFH) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8117
ISOM8117DFHRQ1.B	Active	Production	SOIC (DFH) | 4	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISOM8117DFSRQ1	Active	Production	SOIC (DFS) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8117
ISOM8117DFSRQ1.A	Active	Production	SOIC (DFS) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8117
ISOM8117DFSRQ1.B	Active	Production	SOIC (DFS) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8117
ISOM8118DFGRQ1	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8118
ISOM8118DFGRQ1.A	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8118
ISOM8118DFGRQ1.B	Active	Production	SOIC (DFG) | 4	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISOM8118DFHRQ1	Active	Production	SOIC (DFH) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8118
ISOM8118DFHRQ1.A	Active	Production	SOIC (DFH) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8118
ISOM8118DFHRQ1.B	Active	Production	SOIC (DFH) | 4	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISOM8118DFSRQ1	Active	Production	SOIC (DFS) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8118
ISOM8118DFSRQ1.A	Active	Production	SOIC (DFS) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8118
ISOM8118DFSRQ1.B	Active	Production	SOIC (DFS) | 4	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8118

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ISOM8110-Q1, ISOM8111-Q1, ISOM8112-Q1, ISOM8113-Q1, ISOM8115-Q1, ISOM8116-Q1, ISOM8117-Q1, ISOM8118-Q1 :

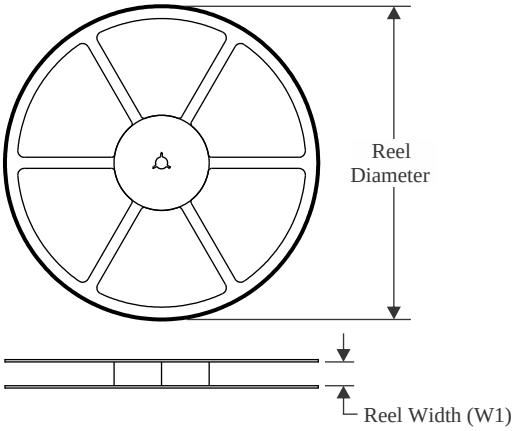
- Catalog : ISOM8110, ISOM8111, ISOM8112, ISOM8113, ISOM8115, ISOM8116, ISOM8117, ISOM8118
- Enhanced Product : ISOM8110-EP

NOTE: Qualified Version Definitions:

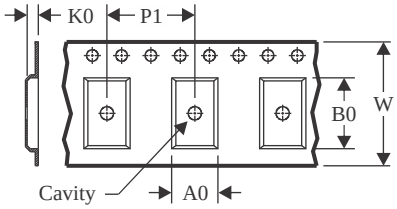
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

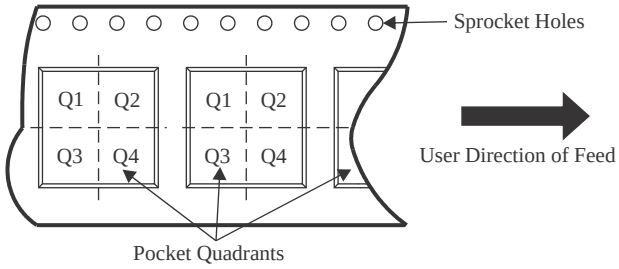


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

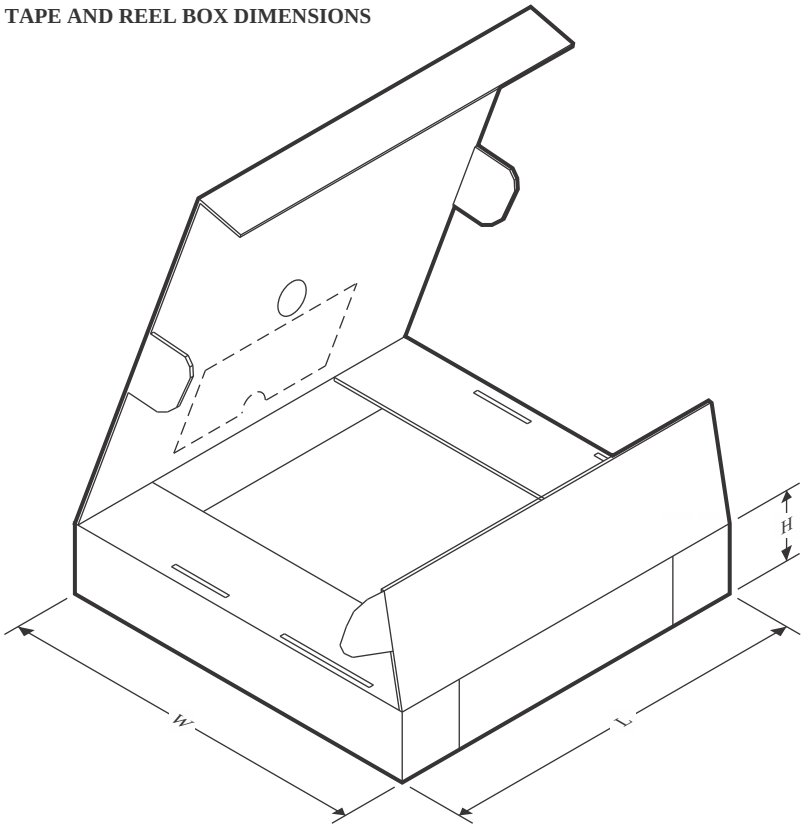


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISOM8110DFGRQ1	SOIC	DFG	4	2000	330.0	12.4	8.0	3.8	2.7	12.0	12.0	Q1
ISOM8110DFHRQ1	SOIC	DFH	4	2000	330.0	12.4	8.0	3.0	2.7	12.0	12.0	Q1
ISOM8110DFSRQ1	SOIC	DFS	4	2000	330.0	12.4	10.9	3.98	2.7	12.0	12.0	Q1
ISOM8111DFGRQ1	SOIC	DFG	4	2000	330.0	12.4	8.0	3.8	2.7	12.0	12.0	Q1
ISOM8111DFHRQ1	SOIC	DFH	4	2000	330.0	12.4	8.0	3.0	2.7	12.0	12.0	Q1
ISOM8111DFSRQ1	SOIC	DFS	4	2000	330.0	12.4	10.9	3.98	2.7	12.0	12.0	Q1
ISOM8112DFGRQ1	SOIC	DFG	4	2000	330.0	12.4	8.0	3.8	2.7	12.0	12.0	Q1
ISOM8112DFHRQ1	SOIC	DFH	4	2000	330.0	12.4	8.0	3.0	2.7	12.0	12.0	Q1
ISOM8112DFSRQ1	SOIC	DFS	4	2000	330.0	12.4	10.9	3.98	2.7	12.0	12.0	Q1
ISOM8113DFGRQ1	SOIC	DFG	4	2000	330.0	12.4	8.0	3.8	2.7	12.0	12.0	Q1
ISOM8113DFHRQ1	SOIC	DFH	4	2000	330.0	12.4	8.0	3.0	2.7	12.0	12.0	Q1
ISOM8113DFSRQ1	SOIC	DFS	4	2000	330.0	12.4	10.9	3.98	2.7	12.0	12.0	Q1
ISOM8115DFGRQ1	SOIC	DFG	4	2000	330.0	12.4	8.0	3.8	2.7	12.0	12.0	Q1
ISOM8115DFHRQ1	SOIC	DFH	4	2000	330.0	12.4	8.0	3.0	2.7	12.0	12.0	Q1
ISOM8115DFSRQ1	SOIC	DFS	4	2000	330.0	12.4	10.9	3.98	2.7	12.0	12.0	Q1
ISOM8116DFGRQ1	SOIC	DFG	4	2000	330.0	12.4	8.0	3.8	2.7	12.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISOM8116DFHRQ1	SOIC	DFH	4	2000	330.0	12.4	8.0	3.0	2.7	12.0	12.0	Q1
ISOM8116DFSRQ1	SOIC	DFS	4	2000	330.0	12.4	10.9	3.98	2.7	12.0	12.0	Q1
ISOM8117DFGRQ1	SOIC	DFG	4	2000	330.0	12.4	8.0	3.8	2.7	12.0	12.0	Q1
ISOM8117DFHRQ1	SOIC	DFH	4	2000	330.0	12.4	8.0	3.0	2.7	12.0	12.0	Q1
ISOM8117DFSRQ1	SOIC	DFS	4	2000	330.0	12.4	10.9	3.98	2.7	12.0	12.0	Q1
ISOM8118DFGRQ1	SOIC	DFG	4	2000	330.0	12.4	8.0	3.8	2.7	12.0	12.0	Q1
ISOM8118DFHRQ1	SOIC	DFH	4	2000	330.0	12.4	8.0	3.0	2.7	12.0	12.0	Q1
ISOM8118DFSRQ1	SOIC	DFS	4	2000	330.0	12.4	10.9	3.98	2.7	12.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



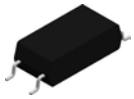
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISOM8110DFGRQ1	SOIC	DFG	4	2000	353.0	353.0	32.0
ISOM8110DFHRQ1	SOIC	DFH	4	2000	353.0	353.0	32.0
ISOM8110DFSRQ1	SOIC	DFS	4	2000	353.0	353.0	32.0
ISOM8111DFGRQ1	SOIC	DFG	4	2000	353.0	353.0	32.0
ISOM8111DFHRQ1	SOIC	DFH	4	2000	353.0	353.0	32.0
ISOM8111DFSRQ1	SOIC	DFS	4	2000	353.0	353.0	32.0
ISOM8112DFGRQ1	SOIC	DFG	4	2000	353.0	353.0	32.0
ISOM8112DFHRQ1	SOIC	DFH	4	2000	353.0	353.0	32.0
ISOM8112DFSRQ1	SOIC	DFS	4	2000	353.0	353.0	32.0
ISOM8113DFGRQ1	SOIC	DFG	4	2000	353.0	353.0	32.0
ISOM8113DFHRQ1	SOIC	DFH	4	2000	353.0	353.0	32.0
ISOM8113DFSRQ1	SOIC	DFS	4	2000	353.0	353.0	32.0
ISOM8115DFGRQ1	SOIC	DFG	4	2000	353.0	353.0	32.0
ISOM8115DFHRQ1	SOIC	DFH	4	2000	353.0	353.0	32.0
ISOM8115DFSRQ1	SOIC	DFS	4	2000	353.0	353.0	32.0
ISOM8116DFGRQ1	SOIC	DFG	4	2000	353.0	353.0	32.0
ISOM8116DFHRQ1	SOIC	DFH	4	2000	353.0	353.0	32.0
ISOM8116DFSRQ1	SOIC	DFS	4	2000	353.0	353.0	32.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISOM8117DFGRQ1	SOIC	DFG	4	2000	353.0	353.0	32.0
ISOM8117DFHRQ1	SOIC	DFH	4	2000	353.0	353.0	32.0
ISOM8117DFSRQ1	SOIC	DFS	4	2000	353.0	353.0	32.0
ISOM8118DFGRQ1	SOIC	DFG	4	2000	353.0	353.0	32.0
ISOM8118DFHRQ1	SOIC	DFH	4	2000	353.0	353.0	32.0
ISOM8118DFSRQ1	SOIC	DFS	4	2000	353.0	353.0	32.0

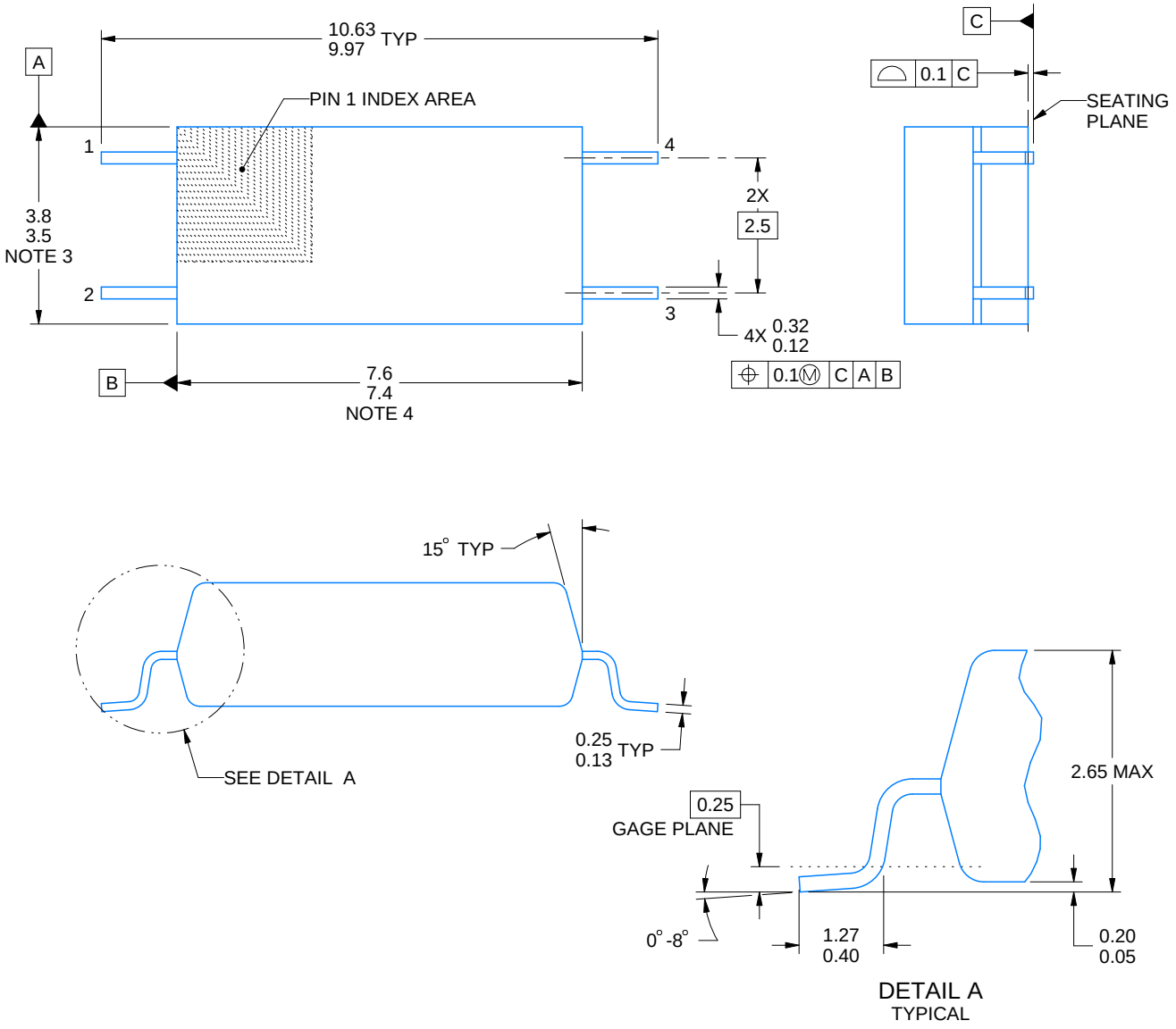
PACKAGE OUTLINE

DFS0004A



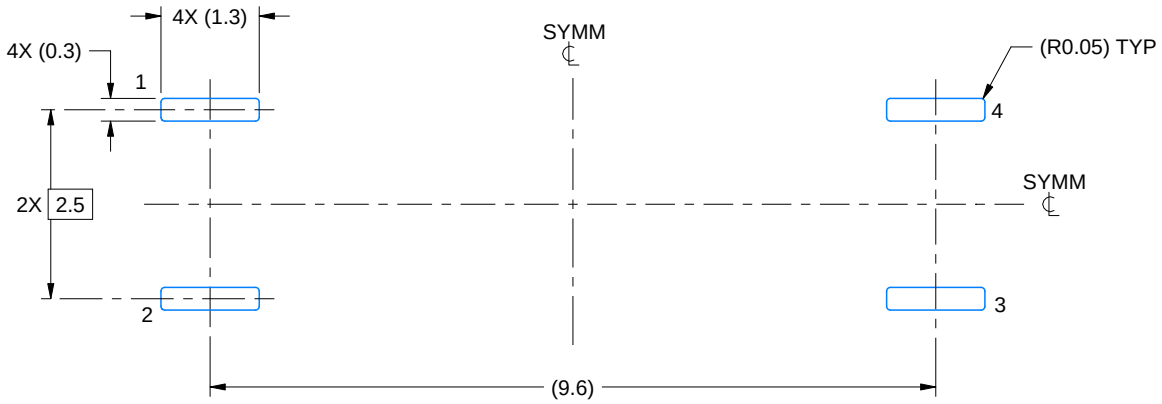
SOIC - 2.65 mm max height

SMALL OUTLINE PACKAGE

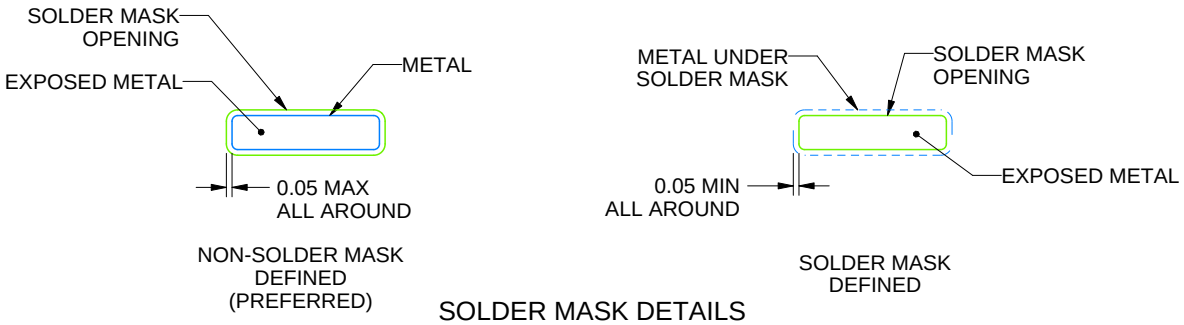


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4230286/C 07/2025

NOTES: (continued)

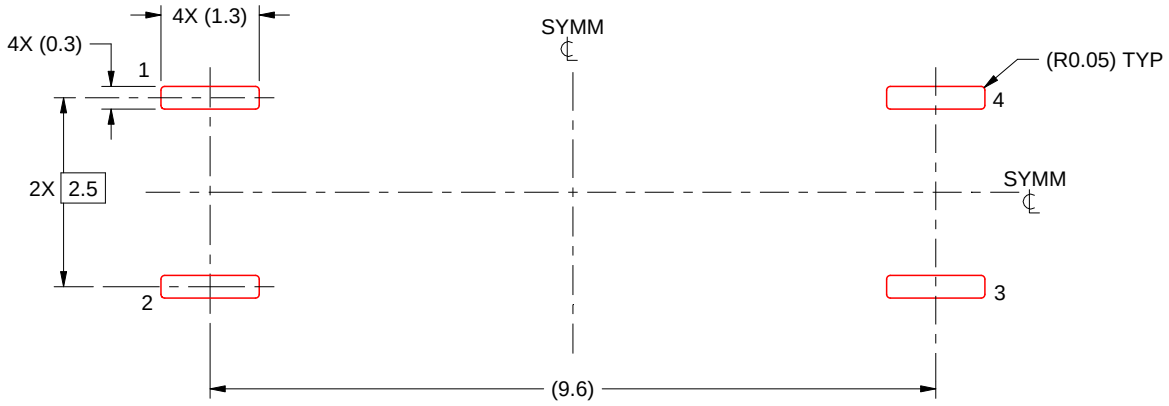
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DFS0004A

SOIC - 2.65 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4230286/C 07/2025

NOTES: (continued)

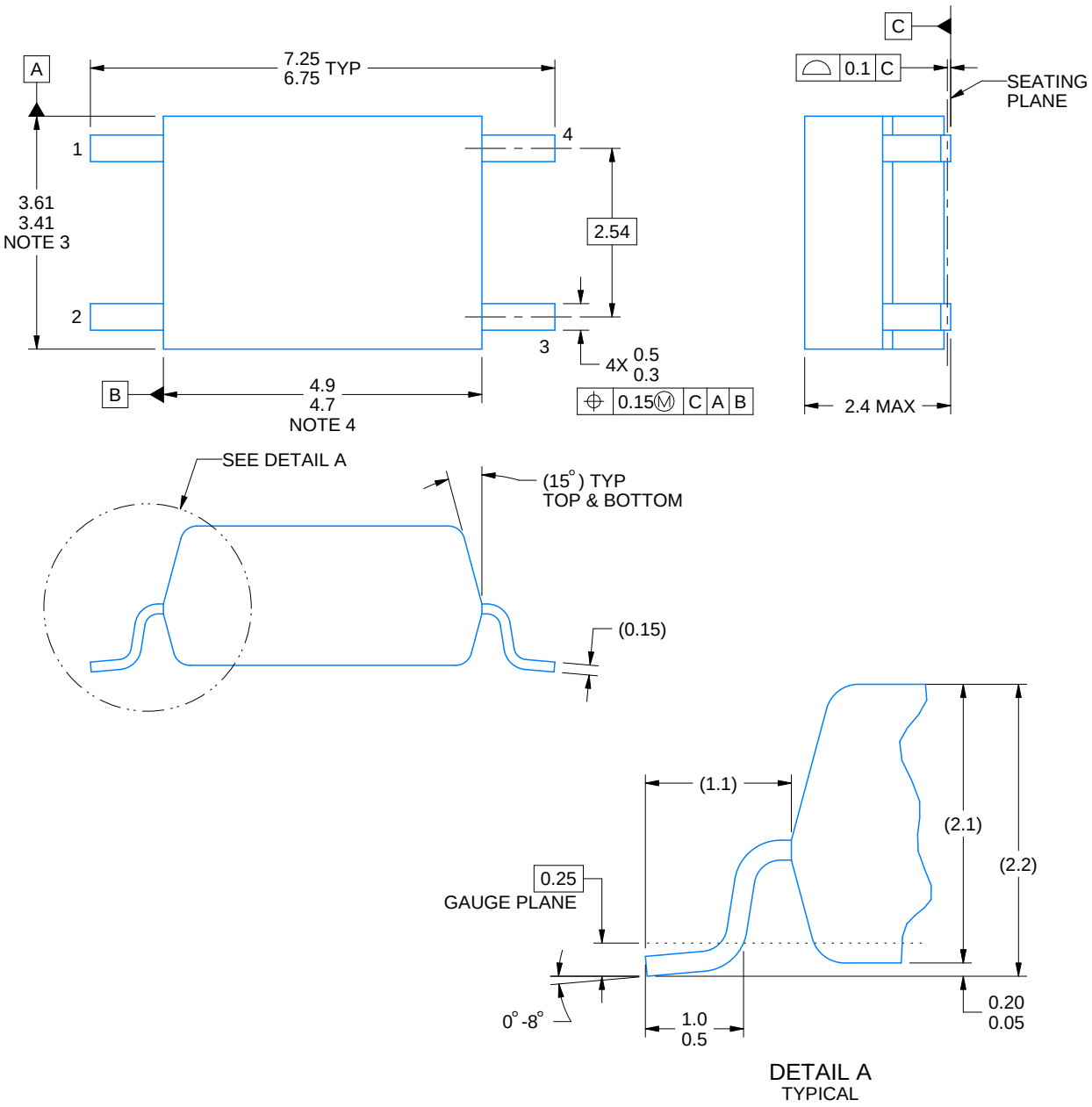
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DFG0004A

SOIC - 2.4 mm max height

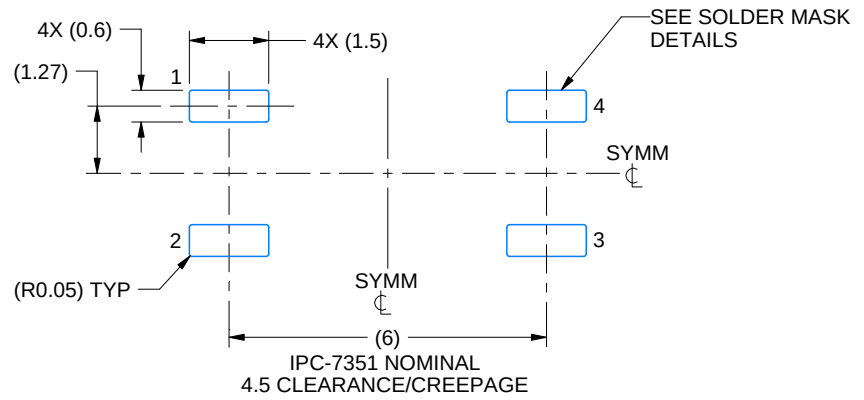
SMALL OUTLINE INTEGRATED CIRCUIT



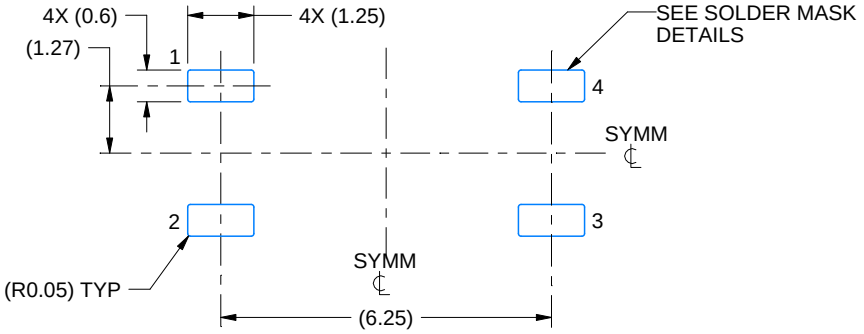
4227022/C 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 mm per side.
4. This dimension does not include interlead flash.

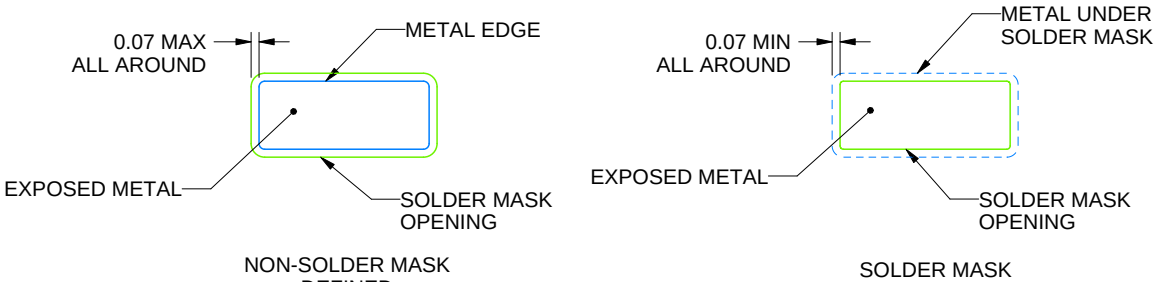


IPC-7351 NOMINAL
4.5 CLEARANCE/CREEPAGE



HV/ISOLATION OPTION
5.0 CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 7X



NON-SOLDER MASK DEFINED (PREFERRED)

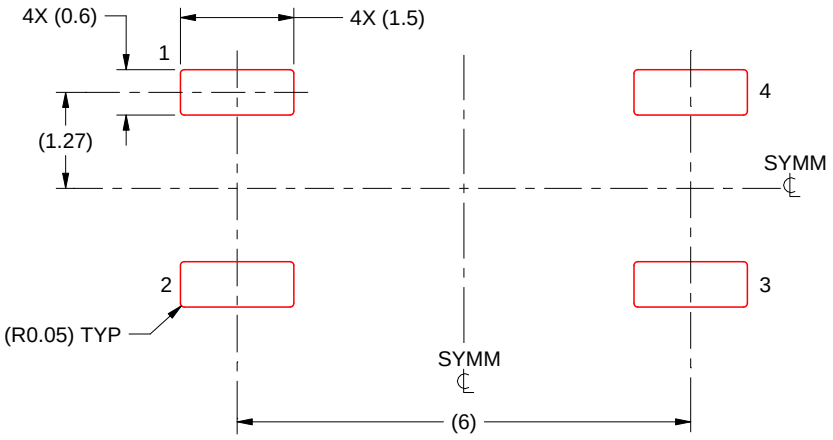
SOLDER MASK DEFINED

SOLDER MASK DETAILS

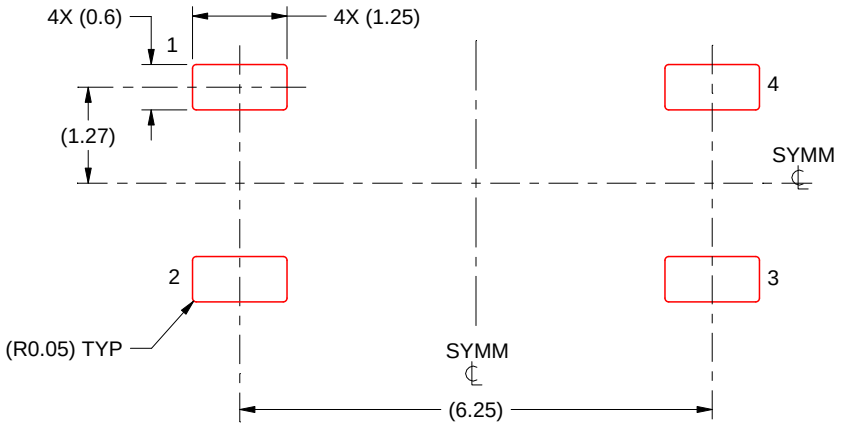
4227022/C 07/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
4.5 CLEARANCE/CREEPAGE



HV/ISOLATION OPTION
5.0 CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4227022/C 07/2024

NOTES: (continued)

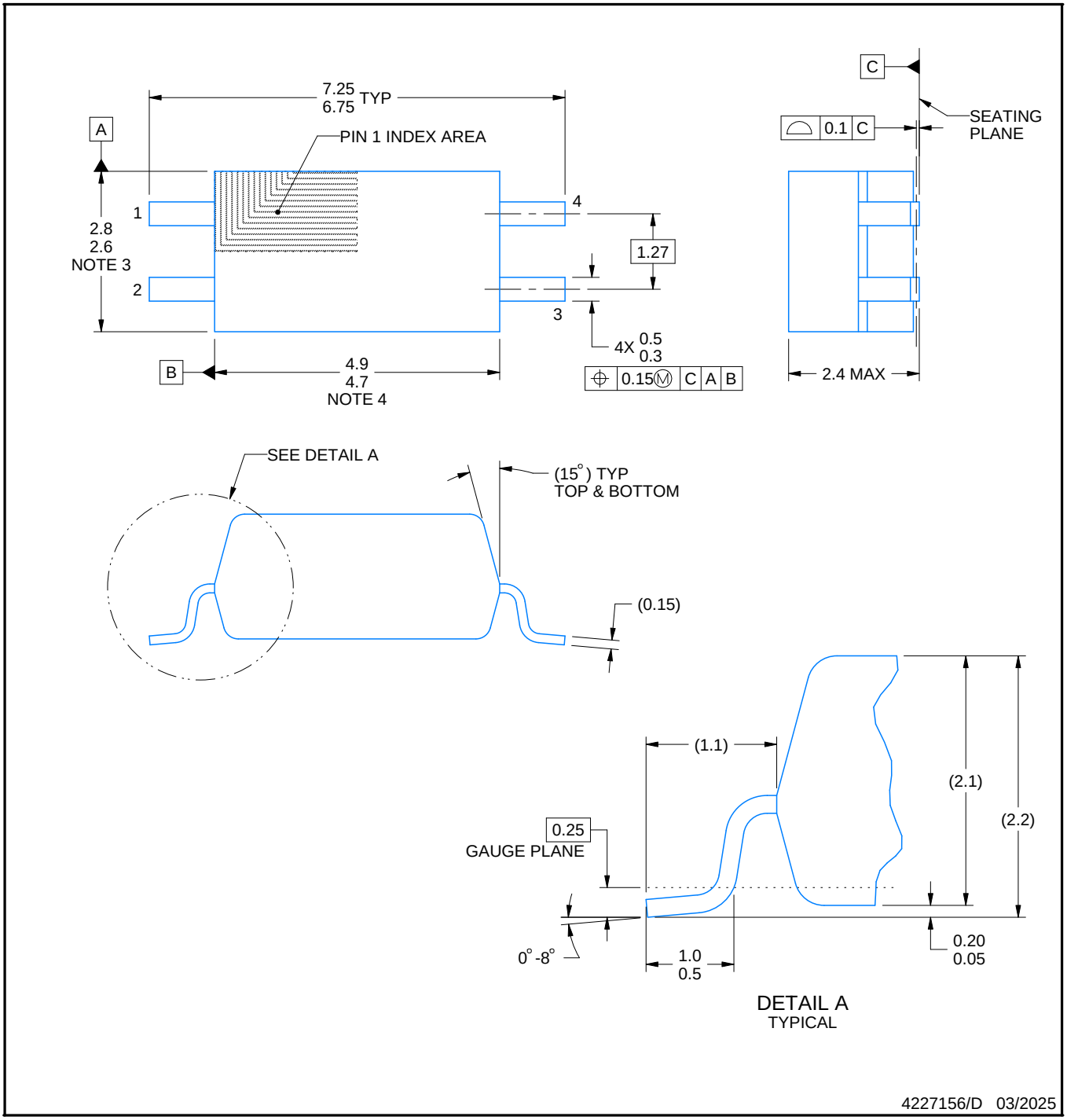
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DFH0004A

PACKAGE OUTLINE

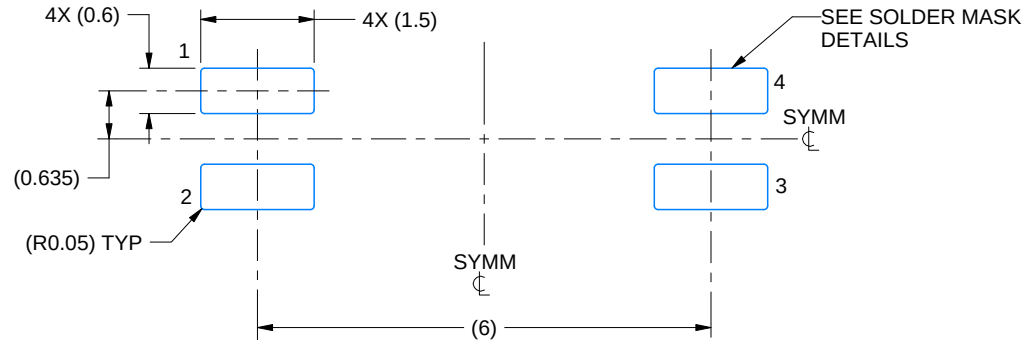
SOIC - 2.4 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

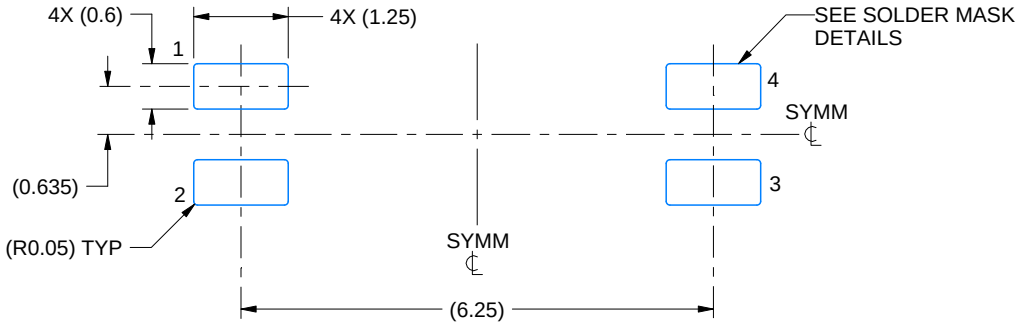


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 mm per side.
4. This dimension does not include interlead flash.

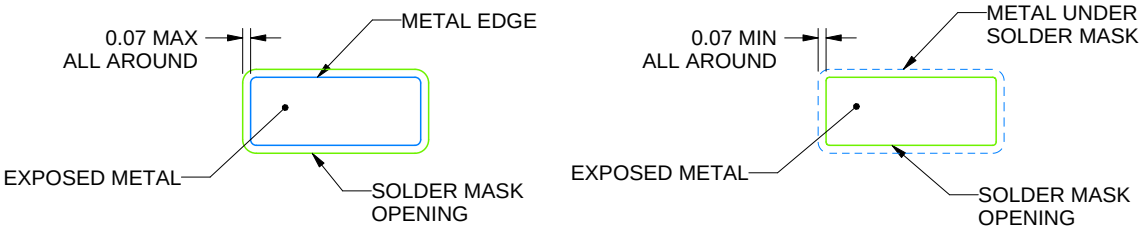


IPC-7351 NOMINAL
4.5 CLEARANCE/CREEPAGE



HV/ISOLATION OPTION
5.0 CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

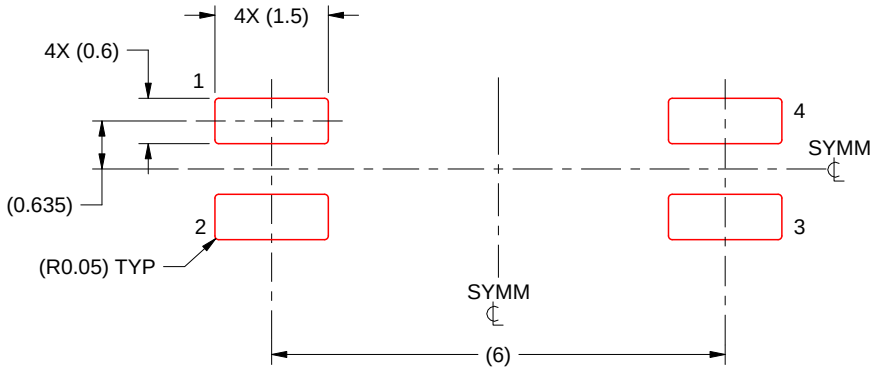


SOLDER MASK DETAILS

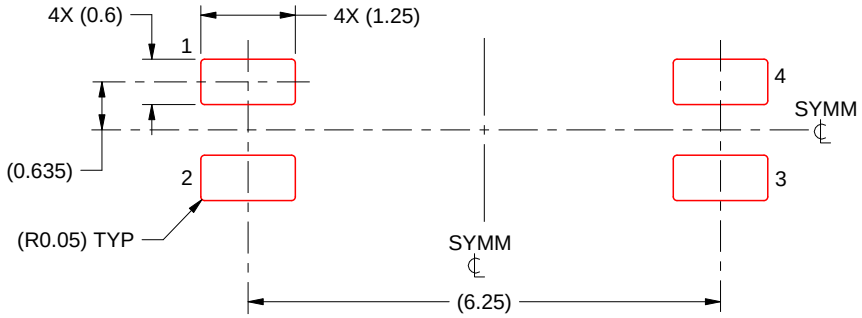
4227156/D 03/2025

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
4.5 CLEARANCE/CREEPAGE



HV/ISOLATION OPTION
5.0 CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4227156/D 03/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025