

# ISO773x High-Speed, Robust-EMC Reinforced and Basic Triple-Channel Digital **Isolators**

#### 1 Features

- 100Mbps data rate
- Robust isolation barrier:
  - >30-year projected lifetime at 1500V<sub>RMS</sub> working voltage
  - Up to 5000V<sub>RMS</sub> isolation rating
  - Up to 12.8kV surge capability
  - ±100kV/µs typical CMTI
- Wide supply range: 2.25V to 5.5V
- 2.25V to 5.5V Level translation
- Default output high (ISO773x) and low (ISO773xF)
- Wide temperature range: -55°C to +125°C
- Low power consumption, typical 1.5mA per channel at 1Mbps
- Low propagation delay: 11ns Typical (5V Supplies)
- Robust electromagnetic compatibility (EMC)
  - System-level ESD, EFT, and surge immunity
  - ±8 kV IEC 61000-4-2 contact discharge protection across isolation barrier
  - Low emissions
- Wide-SOIC (DW-16) and QSOP (DBQ-16) package options
- Automotive version available: ISO773x-Q1
- Safety-Related Certifications:
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 component recognition program
  - IEC 61010-1, IEC 62368-1, IEC60601-1, and GB 4943.1 certifications

## 2 Applications

- Industrial automation
- Motor control
- Power supplies
- Solar inverters
- Medical equipment

#### 3 Description

The ISO773x devices are high-performance, triplechannel digital isolators with 5000V<sub>RMS</sub> (DW package) and 3000V<sub>RMS</sub> (DBQ package) isolation ratings per UL 1577.

This family includes devices with reinforced insulation ratings according to VDE, CSA, TUV and CQC. The ISO7731B device is designed for applications that require basic insulation ratings only.

The ISO773x family of devices provides high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO<sub>2</sub>) insulation barrier. This device comes with enable pins which can be used to put the respective outputs in high impedance for multi-controller driving applications and to reduce power consumption.

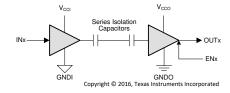
The ISO7730 device has all three channels in the same direction and the ISO7731 device has two forward and one reverse-direction channel. If the input power or signal is lost, the default output is high for devices without suffix F and low for devices with suffix F. See the Device Functional Modes section for further details.

Used in conjunction with isolated power supplies, this family of devices helps prevent noise currents on data buses, such as RS-485, RS-232, and CAN, or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through innovative chip design and layout techniques, electromagnetic compatibility of the ISO773x device has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. The ISO773x family of devices is available in 16-pin wide-SOIC and QSOP packages.

#### **Package Information**

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
ISO7730	SOIC (DW)	10.30mm × 7.50mm
ISO7731	SSOP (DBQ)	4.90mm × 3.90mm
ISO7731B	SOIC (DW)	10.30mm × 7.50mm

- For all available packages, see the orderable addendum at the end of the data sheet.
- The package size (length × width) is a nominal value and includes pins, where applicable.



V<sub>CCI</sub>=Input supply, V<sub>CCO</sub>=Output supply GNDI=Input ground, GNDO=Output ground

#### Simplified Schematic



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## **4 Pin Configuration and Functions**

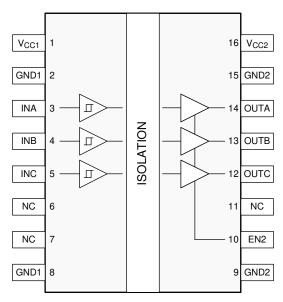


Figure 4-1. ISO7730 DW and DBQ Packages 16-Pin SOIC-WB and QSOP Top View



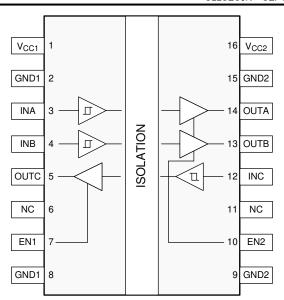


Figure 4-2. ISO7731 DW and DBQ Packages 16-Pin SOIC-WB and QSOP Top View

**Table 4-1. Pin Functions** 

	PIN		Tubic 4	
NAME	N	10.	Type <sup>(1)</sup>	DESCRIPTION
NAME	ISO7730	ISO7731		
EN1	_	7	1	Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
EN2	10	10	I	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
GND1	2, 8	2, 8	_	Ground connection for V <sub>CC1</sub>
GND2	9, 15	9, 15	_	Ground connection for V <sub>CC2</sub>
INA	3	3	I	Input, channel A
INB	4	4	I	Input, channel B
INC	5	12	I	Input, channel C
NC	6, 7, 11	6, 11	_	Not connected
OUTA	14	14	0	Output, channel A
OUTB	13	13	0	Output, channel B
OUTC	12	5	0	Output, channel C
V <sub>CC1</sub>	1	1		Power supply, V <sub>CC1</sub>
V <sub>CC2</sub>	16	16	_	Power supply, V <sub>CC2</sub>



## **5 Specifications**

### 5.1 Absolute Maximum Ratings

See<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC1</sub> , V <sub>CC2</sub>	Supply voltage <sup>(2)</sup>	-0.5	6	V
V	Voltage at INx, OUTx, ENx	-0.5	V <sub>CCX</sub> + 0.5 (3)	V
Io	Output current	-15	15	mA
T <sub>J</sub>	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
- (3) Maximum voltage must not exceed 6 V.

### 5.2 ESD Ratings

			VALUE	UNIT
	Human body model (HBM), per ANSI/ ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±6000		
V <sub>(ESD)</sub>	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1500	V
		Contact discharge per IEC 61000-4-2; Isolation barrier withstand test <sup>(3)</sup> (4)	±8000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
- (3) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
- (4) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

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# **5.3 Recommended Operating Conditions**

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V <sub>CC1</sub> , V <sub>CC2</sub>	Supply voltage		2.25		5.5	V
V <sub>CC(UVLO+)</sub>	UVLO threshold when supply	voltage is rising		2	2.25	V
V <sub>CC(UVLO-)</sub>	UVLO threshold when supply	voltage is falling	1.7	1.8		V
V <sub>HYS(UVLO)</sub>	Supply voltage UVLO hystere	sis	100	200		mV
		V <sub>CCO</sub> <sup>(1)</sup> = 5 V	-4			
Гон	High level output current	V <sub>CCO</sub> = 3.3 V	-2			mA
		V <sub>CCO</sub> = 2.5 V	-1	-1		
		V <sub>CCO</sub> = 5 V			4	mA mA V
l <sub>OL</sub>	Low level output current	V <sub>CCO</sub> = 3.3 V			2	
		V <sub>CCO</sub> = 2.5 V			1	
V <sub>IH</sub>	High-level input voltage	•	0.7 x V <sub>CCI</sub> <sup>(1)</sup>		V <sub>CCI</sub>	V
V <sub>IL</sub>	Low-level input voltage		0	(	0.3 x V <sub>CCI</sub>	V
DR <sup>(2)</sup>	Data rate		0		100	Mbps
T <sub>A</sub>	Ambient temperature		-55	25	125	°C

 $V_{CCI}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$  100 Mbps is the maximum specified data rate, although higher data rates are possible.



### **5.4 Thermal Information**

		ISO	ISO773x			
THERMAL METRIC(1)		DW (SOIC)	DBQ (QSOP)	UNIT		
		16 PINS	16 PINS			
R <sub>0JA</sub>	Junction-to-ambient thermal resistance	81.4	109	°C/W		
R <sub>0JC(top)</sub>	Junction-to-case (top) thermal resistance	44.9	46.8	°C/W		
R <sub>0JB</sub>	Junction-to-board thermal resistance	45.9	60.6	°C/W		
$\Psi_{JT}$	Junction-to-top characterization parameter	28.1	35.9	°C/W		
ΨЈВ	Junction-to-board characterization parameter	45.5	60	°C/W		
R <sub>0JC(bot)</sub>	Junction-to-case (bottom) thermal resistance	-	-	°C/W		

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

# 5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO773	)					
P <sub>D</sub>	Maximum power dissipation (both sides)	V <sub>CC1</sub> = V <sub>CC2</sub> = 5.5 V, T <sub>J</sub> = 150°C, C <sub>J</sub> =			160	mW
P <sub>D1</sub>	Maximum power dissipation (side-1)	15 pF, input a 50-MHz 50% duty cycle		30		mW
P <sub>D2</sub>	Maximum power dissipation (side-2)	square wave			130	mW
ISO773	1				<u> </u>	
P <sub>D</sub>	Maximum power dissipation (both sides)	V <sub>CC1</sub> = V <sub>CC2</sub> = 5.5 V, T <sub>J</sub> = 150°C, C <sub>J</sub> =			160	mW
P <sub>D1</sub>	Maximum power dissipation (side-1)	15 pF, input a 50-MHz 50% duty cycle			60	mW
P <sub>D2</sub>	Maximum power dissipation (side-2)	square wave			100	mW

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# **5.6 Insulation Specifications**

	DADAMETER	TEST CONDITIONS		VALUE		UNIT
	PARAMETER	TEST CONDITIONS		DW-16	DBQ-16	UNIT
CLR	External clearance <sup>(1)</sup>	Shortest terminal-to-terminal distance through air		>8	>3.7	mm
CPG	External creepage <sup>(1)</sup>	Shortest terminal-to-terminal distance across the	package surface	>8	>3.7	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)		>17	>17	μm
СТІ	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112, UL 746	6A	>600	>600	V
	Material group	According to IEC 60664-1		I	I	
		Rated mains voltage ≤ 150 V <sub>RMS</sub>		I-IV	I-IV	
	Overvoltage category per	Rated mains voltage ≤ 300 V <sub>RMS</sub>		I-IV	I-III	
	IEC 60664-1	Rated mains voltage ≤ 600 V <sub>RMS</sub>		I-IV	n/a	
		Rated mains voltage ≤ 1000 V <sub>RMS</sub>		I-III	n/a	
DIN EN	I IEC 60747-17 (VDE 0884-1	<b>17)</b> <sup>(2)</sup>				
$V_{IORM}$	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	ISO773x	2121	566	V <sub>PK</sub>
$V_{IORM}$	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	ISO7731B	1414	n/a	V <sub>PK</sub>
V <sub>IOWM</sub>	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test; See Section 8.2.3.1	ISO773x	1500	400	V <sub>RMS</sub>
V <sub>IOWM</sub>	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test; See Section 8.2.3.1	ISO7731B	1000	n/a	V <sub>RMS</sub>
V <sub>IOWM</sub>	Maximum working isolation voltage	DC voltage	ISO773x	2121	566	V <sub>DC</sub>
V <sub>IOWM</sub>	Maximum working isolation voltage	DC voltage	ISO7731B	1414	n/a	V <sub>DC</sub>
$V_{IOTM}$	Maximum transient isolation voltage	V <sub>TEST</sub> = V <sub>IOTM</sub> , t = 60 s (qualification); V <sub>TEST</sub> = 1.2 x V <sub>IOTM</sub> , t= 1 s (100% production)		8000	4242	V <sub>PK</sub>
V <sub>IMP</sub>	Maximum impulse voltage <sup>(3)</sup>	Tested in air, 1.2/50-µs waveform per IEC 62368-1	ISO773x	8000	5000	V <sub>PK</sub>
V <sub>IMP</sub>	Maximum impulse voltage <sup>(3)</sup>	Tested in air, 1.2/50-µs waveform per IEC 62368-1	ISO7731B	6000	n/a	V <sub>PK</sub>
V <sub>IOSM</sub>	Maximum surge isolation voltage <sup>(4)</sup>	V <sub>IOSM</sub> ≥ 1.3 x V <sub>IMP</sub> ; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	ISO773x	12800	10000	V <sub>PK</sub>
V <sub>IOSM</sub>	Maximum surge isolation voltage <sup>(4)</sup>	V <sub>IOSM</sub> ≥ 1.3 x V <sub>IMP</sub> ; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	ISO7731B	7800	n/a	V <sub>PK</sub>
q <sub>pd</sub>	Apparent charge <sup>(5)</sup>	Method a, After Input/Output safety test subgroup $V_{ini} = V_{IOTM}$ , $t_{ini} = 60 \text{ s}$ ; $V_{pd(m)} = 1.2 \text{ x } V_{IORM}$ , $t_m = 10 \text{ s}$	2/3,	≤5	≤5	pC
q <sub>pd</sub>	Apparent charge <sup>(5)</sup>	Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$ , $t_{ini} = 60$ s;	$V_{pd(m)} = 1.6 \text{ x } V_{IORM},$ $t_m = 10 \text{ s } (ISO773x)$	≤5	≤5	рС
q <sub>pd</sub>	Apparent charge <sup>(5)</sup>	Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$ , $t_{ini} = 60 \text{ s}$ ;	$V_{pd(m)} = 1.3 \times V_{IORM},$ $t_m = 10 \text{ s (ISO7731B)}$	≤5	n/a	рС
q <sub>pd</sub>	Apparent charge <sup>(5)</sup>	Method b; At routine test (100% production) and preconditioning (type test); $V_{ini} = 1.2 \times V_{IOTM}, t_{ini} = 1 \text{ s}; \\ V_{pd(m)} = 1.875 \times V_{IORM} (ISO773x) \text{ or } \\ V_{pd(m)} = 1.5 \times V_{IORM} (ISO7731B), t_m = 1 \text{ s (method b1) or } \\ V_{pd(m)} = V_{ini}, t_m = t_{ini} \text{ (method b2)}$		≤5	≤5	pC
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(6)</sup>	V <sub>IO</sub> = 0.4 x sin (2πft), f = 1 MHz		≅0.7	≅0.7	pF
	1					



PARAMETER		TEST CONDITIONS		VALUE				
	PARAIVIETER	TEST CONDITIONS	DW-16	DBQ-16	UNIT			
		V <sub>IO</sub> = 500 V, T <sub>A</sub> = 25°C	>10 <sup>12</sup>	>10 <sup>12</sup>				
R <sub>IO</sub>	.	V <sub>IO</sub> = 500 V, 100°C ≤ T <sub>A</sub> ≤ 125°C	>10 <sup>11</sup>	>10 <sup>11</sup>	Ω			
		V <sub>IO</sub> = 500 V at T <sub>S</sub> = 150°C	>10 <sup>9</sup>	>10 <sup>9</sup>				
	Pollution degree		2	2				
	Climatic category		55/125/ 21	55/125/21				
UL 157	UL 1577							
V <sub>ISO</sub>	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$ , t = 60 s (qualification), $V_{TEST} = 1.2$ x $V_{ISO}$ , t = 1 s (100% production)	5000	3000	V <sub>RMS</sub>			

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* (ISO773x) and basic electrical insulation (ISO7731B) only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air to determine the surge immunity of the package
- (4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
- (5) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (6) All pins on each side of the barrier tied together creating a two-terminal device.

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# 5.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 62368-1 and IEC 60601	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1	Certified according to EN 61010-1 and EN 62368-1
Maximum transient isolation voltage, 8000 V <sub>PK</sub> (DW-16) and 4242 V <sub>PK</sub> (DBQ-16); Maximum repetitive peak isolation voltage, 2121 V <sub>PK</sub> (DW-16, Reinforced), 1414 V <sub>PK</sub> (DW-16, Basic) and 566 V <sub>PK</sub> (DBQ-16); Maximum surge isolation voltage, 12800 V <sub>PK</sub> (DW-16, Reinforced), 7800 V <sub>PK</sub> (DW-16, Basic) and 10000 V <sub>PK</sub> (DBQ-16)	Reinforced insulation per CSA 62368-1 and IEC 62368-1, 600 V <sub>RMS</sub> (DW-16) and 370 V <sub>RMS</sub> (DBQ-16) max working voltage (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1 and IEC 60601-1, 250 V <sub>RMS</sub> (DW-16) max working voltage	DW-16: Single protection, 5000 V <sub>RMS</sub> ; DBQ-16: Single protection, 3000 V <sub>RMS</sub>	DW-16: Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V <sub>RMS</sub> maximum working voltage; DBQ-16: Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 400 V <sub>RMS</sub> maximum working voltage	5000 V <sub>RMS</sub> (DW-16) and 3000 V <sub>RMS</sub> (DBQ-16) Reinforced insulation per EN 61010-1 up to working voltage of 600 V <sub>RMS</sub> (DW-16) and 300 V <sub>RMS</sub> (DBQ-16) 5000 V <sub>RMS</sub> (DW-16) and 3000 V <sub>RMS</sub> (DBQ-16) Reinforced insulation per EN 62368-1 up to working voltage of 600 V <sub>RMS</sub> (DW-16) and 370 V <sub>RMS</sub> (DBQ-16) of 600 V <sub>RMS</sub> (DBQ-16) of 600 V <sub>RMS</sub> (DBQ-16) of 600
Certificate numbers: 40040142 (Reinforced) 40047657 (Basic)	Master contract number: 220991	File number: E181974	Certificate numbers: CQC21001304083 (DW-16) CQC18001199097 (DBQ-16)	Client ID number: 077311

### 5.8 Safety Limiting Values

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16	S PACKAGE					
		$R_{\theta JA} = 81.4^{\circ}\text{C/W}, V_I = 5.5 \text{ V}, T_J = 150^{\circ}\text{C}, T_A = 25^{\circ}\text{C},$ see Figure 5-1	27		279	
I <sub>S</sub>	Safety input, output, or supply current.	$R_{\theta JA} = 81.4^{\circ} \text{C/W}, V_I = 3.6 \text{ V}, T_J = 150^{\circ} \text{C}, T_A = 25^{\circ} \text{C},$ see Figure 5-1			427	mA
		$R_{\theta JA} = 81.4^{\circ}\text{C/W}, V_I = 2.75 \text{ V}, T_J = 150^{\circ}\text{C}, T_A = 25^{\circ}\text{C},$ see Figure 5-1			558	
Ps	Safety input, output, or total power	R <sub>0JA</sub> = 81.4°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, see Figure 5-3			1536	mW
T <sub>S</sub>	Maximum safety temperature				150	°C
DBQ-1	16 PACKAGE					
		$R_{\theta JA} = 109.0^{\circ}\text{C/W}, V_I = 5.5 \text{ V}, T_J = 150^{\circ}\text{C}, T_A = 25^{\circ}\text{C},$ see Figure 5-2			209	
I <sub>S</sub>	Safety input, output, or supply current	$R_{\theta JA}$ = 109.0°C/W, $V_I$ = 3.6 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 5-2			319	mA
		$R_{\theta JA}$ = 109.0°C/W, $V_I$ = 2.75 V, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 5-2		41	417	
Ps	Safety input, output, or total power	$R_{\theta JA} = 109.0$ °C/W, $T_J = 150$ °C, $T_A = 25$ °C, see Figure 5-4			1147	mW
T <sub>S</sub>	Maximum safety temperature				150	°C

The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The  $I_S$  and  $P_S$  parameters represent the safety current and safety power respectively. The maximum limits of  $I_S$  and  $P_S$  should not be exceeded. These limits vary with the ambient temperature, T<sub>A</sub>.

The junction-to-air thermal resistance, R<sub>BJA</sub>, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

 $T_J = T_A + R_{\theta JA} \times P$ , where P is the power dissipated in the device.  $T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$ , where  $T_{J(max)}$  is the maximum allowed junction temperature.  $P_S = I_S \times V_I$ , where  $V_I$  is the maximum input voltage.



## 5.9 Electrical Characteristics—5-V Supply

 $V_{CC1} = V_{CC2} = 5 \text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -4 mA; See Figure 6-1	V <sub>CCO</sub> - 0.4 (1)	4.8		V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 4 mA; See Figure 6-1		0.2	0.4	V
V <sub>IT+(IN)</sub>	Rising input switching threshold			0.6 x V <sub>CCI</sub>	0.7 x V <sub>CCI</sub>	V
V <sub>IT-(IN)</sub>	Falling input switching threshold		0.3 x V <sub>CCI</sub>	0.4 x V <sub>CCI</sub>		V
V <sub>I(HYS)</sub>	Input threshold voltage hysteresis		0.1 x V <sub>CCI</sub>	0.2 x V <sub>CCI</sub>		V
I <sub>IH</sub>	High-level input current	V <sub>IH</sub> = V <sub>CCI</sub> <sup>(1)</sup> at INx			10	μΑ
I <sub>IL</sub>	Low-level input current	V <sub>IL</sub> = 0 V at INx	-10			μΑ
I <sub>IH</sub>	High-level input current	V <sub>IH</sub> = V <sub>CCI</sub> <sup>(1)</sup> at ENx			28	μA
I <sub>IL</sub>	Low-level input current	V <sub>IL</sub> = 0 V at ENx	-28			μΑ
CMTI	Common mode transient immunity	V <sub>I</sub> = V <sub>CCI</sub> or 0 V, V <sub>CM</sub> = 1200 V; See Figure 6-4	85	100		kV/μs
Cı	Input capacitance (2)	$V_1 = V_{CC}/2 + 0.4 \times \sin(2\pi ft), f = 1$ MHz, $V_{CC} = 5 \text{ V}$		2		pF

 $V_{CCI}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$  Measured from input pin to same side ground.



## 5.10 Supply Current Characteristics—5-V Supply

V<sub>CC1</sub> = V<sub>CC2</sub> = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITION	s	SUPPLY CURRENT	MIN TYP	MAX	UNIT	
ISO7730							
	EN2 = 0 V; V <sub>I</sub> = V <sub>CC1</sub> (ISO7730);		I <sub>CC1</sub>	1	2.3	mA	
Supply current - disable	V <sub>I</sub> = 0 V (ISO7730 with F suffix)		I <sub>CC2</sub>	0.3	1 2.3	mA	
	EN2 = 0 V; V <sub>I</sub> = 0 V (ISO7730);		I <sub>CC1</sub>	4.3	6	mA	
	$V_I = V_{CC1}$ (ISO7730 with F suffix)		I <sub>CC2</sub>	0.3	0.8	mA	
	$EN2 = V_{CC2}$ ; $V_I = V_{CC1}$ (ISO7730);		I <sub>CC1</sub>	1	2.3	mA	
Supply current - DC signal	V <sub>I</sub> = 0 V (ISO7730 with F suffix)		I <sub>CC2</sub>	1.6	3.7	mA	
Supply surrent 20 signal	$EN2 = V_{CC2}$ ; $V_1 = 0 V (ISO7730)$ ;			4.3	6	mA	
	$V_I = V_{CC1}$ (ISO7730 with F suffix)		I <sub>CC2</sub>	1.8	3.9	mA	
		1 Mbps	I <sub>CC1</sub>	2.6	4.1	mA	
Supply current - AC signal			I <sub>CC2</sub>	1.9	4	mA	
	EN2 = V <sub>CCI</sub> ; All channels switching with square wave clock input; C <sub>I</sub> =	10 Mbps	I <sub>CC1</sub>	2.7	4.3	mA	
	15 pF		I <sub>CC2</sub>	I <sub>CC2</sub> 3.3			
		100 Mbps	001		5.6	mA	
		100 Mapo	I <sub>CC2</sub>	17.5	23.2	mA	
ISO7731							
	EN1 = EN2 = 0 V; V <sub>I</sub> = V <sub>CCI</sub> (1)(ISO7	07731); I <sub>CC1</sub> 0.8		2.2	mA		
Supply current - disable	V <sub>I</sub> = 0 V (ISO7731 with F suffix)		I <sub>CC2</sub>	0.7	1.6	mA	
cupply current alouble	EN1 = EN2 = 0 V; V <sub>I</sub> = 0 V (ISO7731);		I <sub>CC1</sub>	3	4.6	mA	
	$V_I = V_{CCI}$ (ISO7731 with F suffix)		I <sub>CC2</sub>	1.8	2.8	mA	
	EN1 = EN2 = V <sub>CCI</sub> ; V <sub>I</sub> = V <sub>CCI</sub> (1)(ISO	7731);	I <sub>CC1</sub>	1.3	2.9	mA	
0 1 1 10 1	$V_I = 0 V (ISO7731 \text{ with F suffix})$		I <sub>CC2</sub>	1.6	mA		
Supply current - DC signal	EN1 = EN2 = $V_{CCI}$ ; $V_I$ = 0 V (ISO773	31);	I <sub>CC1</sub>	3.5	5.4	mA	
	$V_I = VCC_I$ (ISO7731 with F suffix)		I <sub>CC2</sub>	2.8	1 2.3   3 0.8   3 0.8   3   6   3   3.7   3   6   3   3.9   6   4.1   9   4   7   4.3   3   5.7   5   5.6   5   23.2   7   1.6   3   2.8   3   2.9   5   3.7   5   5.4   3   5.1   7   4.2   3   4.6   3   4.9   3   5.8   5   11.5	mA	
		4 Mb = -	I <sub>CC1</sub>	1 2.3   0.3 0.8   4.3 6   0.3 0.8   1 2.3   1.6 3.7   4.3 6   1.8 3.9   2.6 4.1   1.9 4   2.7 4.3   3.3 5.7   3.6 5.6   17.5 23.2   1.6 3.7   4.6   1.8 2.8   1.3 2.9   1.6 3.7   3.5 5.4   2.8 5.1   2.7 4.2   2.3 4.6   3 4.9   3.3 5.8   8.5 11.5   1.5		mA	
		1 Mbps	I <sub>CC2</sub>	2.3	4.6	mA	
Supply ourrent AC signal	EN1 = EN2 = V <sub>CCI</sub> ; All channels	40 Mh = =	I <sub>CC1</sub>	3	4.9	mA	
Supply current - AC signal	switching with square wave clock input; C <sub>L</sub> = 15 pF	10 Mbps	I <sub>CC2</sub>	3.3	5.8	mA	
		100 Mbss	I <sub>CC1</sub>	8.5	11.5	mA	
		100 Mbps	I <sub>CC2</sub>	13.1	17.8	mA	

<sup>(1)</sup>  $V_{CCI} = Input-side V_{CC}$ 



## 5.11 Electrical Characteristics—3.3-V Supply

 $V_{CC1} = V_{CC2} = 3.3 \text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -2mA; See Figure 6-1	V <sub>CCO</sub> - 0.3 <sup>(1)</sup>	3.2		V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 2mA; See Figure 6-1		0.1	0.3	V
V <sub>IT+(IN)</sub>	Rising input switching threshold			0.6 x V <sub>CCI</sub>	0.7 x V <sub>CCI</sub>	V
V <sub>IT-(IN)</sub>	Falling input switching threshold		0.3 x V <sub>CCI</sub>	0.4 x V <sub>CCI</sub>		V
V <sub>I(HYS)</sub>	Input threshold voltage hysteresis		0.1 x V <sub>CCI</sub>	0.2 x V <sub>CCI</sub>		V
I <sub>IH</sub>	High-level input current	V <sub>IH</sub> = V <sub>CCI</sub> <sup>(1)</sup> at INx			10	μA
I <sub>IL</sub>	Low-level input current	V <sub>IL</sub> = 0 V at INx	-10			μΑ
I <sub>IH</sub>	High-level input current	V <sub>IH</sub> = V <sub>CCI</sub> <sup>(1)</sup> at ENx			30	μΑ
I <sub>IL</sub>	Low-level input current	V <sub>IL</sub> = 0 V at ENx	-30			μΑ
СМТІ	Common mode transient immunity	V <sub>I</sub> = V <sub>CCI</sub> or 0 V, V <sub>CM</sub> = 1200 V; See Figure 6-4	85	100		kV/µs

<sup>(1)</sup>  $V_{CCI}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$ 



# 5.12 Supply Current Characteristics—3.3-V Supply

 $V_{CC1} = V_{CC2} = 3.3 \text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITION	S	SUPPLY CURRENT	MIN TYP	MAX	UNIT	
ISO7730							
	EN2 = 0 V; V <sub>I</sub> = V <sub>CC1</sub> (ISO7730);		I <sub>CC1</sub>	1	2.3	mA	
Supply current - disable	V <sub>I</sub> = 0 V (ISO7730 with F suffix)		I <sub>CC2</sub>	0.3	1 2.3 0.3 0.8 4.3 5.9 0.3 0.7 1 2.3 1.6 3.6 4.3 5.8 1.8 3.8 2.6 4.1 1.8 3.9 2.7 4.1 2.8 5.1 3.3 4.9 13 17.7 0.8 2.1 0.7 1.5 3 4.5 1.8 2.8 1.3 2.8 1.6 3.7 3.5 5.3 2.8 5	mA	
oupply current - disable	EN2 = 0 V; V <sub>I</sub> = 0 V (ISO7730);	I <sub>CC1</sub>		4.3	5.9	mA	
	V <sub>I</sub> = V <sub>CC1</sub> (ISO7730 with F suffix)		I <sub>CC2</sub>	0.3	1 2.3 r 0.3 0.8 r 4.3 5.9 r 0.3 0.7 r 1 2.3 r 1.6 3.6 r 1.8 3.8 r 2.6 4.1 r 1.8 3.9 r 2.7 4.1 r 2.8 5.1 r 3.3 4.9 r 13 17.7 r 0.8 2.1 r 0.7 1.5 r 3 4.5 r 1.8 2.8 r 1.3 2.8 r 1.3 2.8 r 1.6 3.7 r 3.5 5.3 r 2.8 5 r 2.4 4.1 r 2.2 4.5 r		
EN2 = V <sub>CC2</sub> ; V <sub>I</sub> = V <sub>CC1</sub> (ISO7730			I <sub>CC1</sub>	1	2.3	mA	
Supply current - DC signal	V <sub>I</sub> = 0 V (ISO7730 with F suffix)		I <sub>CC2</sub>	1.6	3.6	mA	
Supply surrent 20 signal	EN2 =V <sub>CC2</sub> ; V <sub>I</sub> = 0 V (ISO7730);		I <sub>CC1</sub>	4.3	5.8	mA	
	$V_I = V_{CC1}$ (ISO7730 with F suffix)		I <sub>CC2</sub>	1.8	3.8	mA	
		1 Mbps	I <sub>CC1</sub>	2.6	4.1	mA	
			I <sub>CC2</sub>	0.002     0.3       0.001     4.3       0.002     0.3       0.001     1       0.002     1.6       0.001     4.3       0.002     1.8       0.002     1.8       0.001     2.6       0.002     1.8       0.001     2.7       0.002     2.8       0.001     3.3       0.002     1.3       0.002     1.8       0.002     1.8       0.001     1.3       0.002     1.6       0.001     3.5       0.002     2.8       0.001     2.4			
Supply current - AC signal	EN2 = V <sub>CCI</sub> ; All channels switching with square wave clock input; C <sub>I</sub> =	10 Mbps	0 Mbps	2.7	4.1	mA	
	15 pF			5.1	mA		
		100 Mbps	I <sub>CC1</sub>	3.3			
		Too Mapo	I <sub>CC2</sub>	13	17.7	mA	
ISO7731							
	EN1 = EN2 = 0 V; V <sub>I</sub> = V <sub>CCI</sub> (1)(ISO7	731);	I <sub>CC1</sub>	0.8	2.1	mA	
Supply current - disable	V <sub>I</sub> = 0 V (ISO7731 with F suffix)		I <sub>CC2</sub>	0.7	1.5	mA	
cappiy carrone alcabic	EN1 = EN2 = 0 V; V <sub>I</sub> = 0 V (ISO773 <sup>2</sup>	1);	I <sub>CC1</sub>	3	4.5	mA	
	$V_I = V_{CCI}$ (ISO7731 with F suffix)		I <sub>CC2</sub>	1.8	2.8	mA	
	EN1 = EN2 = V <sub>CCI</sub> ; V <sub>I</sub> = V <sub>CCI</sub> (ISO77	31);	I <sub>CC1</sub>	1.3	2.8	mA	
Supply current - DC signal	V <sub>I</sub> = 0 V (ISO7731with F suffix)		I <sub>CC2</sub>	1.6	3.7	mA	
Supply surrent 20 signal	EN1 = EN2 = V <sub>CCI</sub> ; V <sub>I</sub> = 0 V (ISO773	31);	I <sub>CC1</sub>	3.5	5.3	mA	
	$V_I = V_{CCI}$ (ISO7731 with F suffix)		I <sub>CC2</sub>	2.8	5	mA	
		1 Mbps	I <sub>CC1</sub>	2.4	4.1	mA	
			I <sub>CC2</sub>	2.2	4.5	mA	
Supply current - AC signal	EN1 = EN2 = V <sub>CCI</sub> ; All channels switching with square wave clock	10 Mbps	I <sub>CC1</sub>	2.8	4.6	mA	
	input; C <sub>L</sub> = 15 pF		I <sub>CC2</sub>	2.9	5.3	mA	
		100 Mbps	I <sub>CC1</sub>	6.7	9.2	mA	
		. co mapo	I <sub>CC2</sub>	10	14	mA	

<sup>(1)</sup>  $V_{CCI} = Input-side V_{CC}$ 



## 5.13 Electrical Characteristics—2.5-V Supply

 $V_{CC1} = V_{CC2} = 2.5 \text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -1mA; See Figure 6-1	V <sub>CCO</sub> - 0.2 (1)	2.45		V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 1mA; See Figure 6-1		0.05	0.2	V
V <sub>IT+(IN)</sub>	Rising input switching threshold			0.6 x V <sub>CCI</sub>	0.7 x V <sub>CCI</sub> <sup>(1)</sup>	V
V <sub>IT-(IN)</sub>	Falling input switching threshold		0.3 x V <sub>CCI</sub>	0.4 x V <sub>CCI</sub>		V
V <sub>I(HYS)</sub>	Input threshold voltage hysteresis		0.1 x V <sub>CCI</sub>	0.2 x V <sub>CCI</sub>		V
I <sub>IH</sub>	High-level input current	V <sub>IH</sub> = V <sub>CCI</sub> <sup>(1)</sup> at INx			10	μA
I <sub>IL</sub>	Low-level input current	V <sub>IL</sub> = 0 V at INx	-10			μΑ
I <sub>IH</sub>	High-level input current	V <sub>IH</sub> = V <sub>CCI</sub> <sup>(1)</sup> at ENx			30	μΑ
I <sub>IL</sub>	Low-level input current	V <sub>IL</sub> = 0 V at ENx	-30			μΑ
СМТІ	Common mode transient immunity	V <sub>I</sub> = V <sub>CCI</sub> or 0 V, V <sub>CM</sub> = 1200 V; See Figure 6-4	85	100		kV/µs

<sup>(1)</sup>  $V_{CCI}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$ 



# 5.14 Supply Current Characteristics—2.5-V Supply

 $V_{CC1} = V_{CC2} = 2.5 \text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITION	S	SUPPLY CURRENT	MIN TYP	MAX	UNIT	
ISO7730							
	EN2 = 0 V; V <sub>I</sub> = V <sub>CC1</sub> (ISO7730);		I <sub>CC1</sub>	1	2.2	mA	
Supply current - disable	V <sub>I</sub> = 0 V (ISO7730 with F suffix)		I <sub>CC2</sub>	0.3	1 2.2 3 0.7 3 5.8 3 0.7 1 2.2 5 3.6 3 3.8 5 4 3 3.8 6 4.1 5 4.8 1 4.7 2 14.3 3 2.1 7 1.5 3 2.7 3 3.8 6 4.1 5 4.8 1 4.7 2 14.3	mA	
Supply current - disable	EN2 = 0 V; V <sub>I</sub> = 0 V (ISO7730);		I <sub>CC1</sub>	4.3	5.8	mA	
	$V_I = V_{CC1}$ (ISO7730 with F suffix)		I <sub>CC2</sub>	0.3	0.7	mA	
	EN2 = V <sub>CC2</sub> ; V <sub>I</sub> = V <sub>CC1</sub> (ISO7730);		I <sub>CC2</sub>			mA	
Supply current - DC signal	V <sub>I</sub> = 0 V (ISO7730 with F suffix)		I <sub>CC2</sub>	1.6	3.6	mA	
cappi, carrent 20 oigna.	EN2 =V <sub>CC2</sub> ; V <sub>I</sub> = 0 V (ISO7730);			4.3	5.8	mA	
	$V_I = V_{CC1}$ (ISO7730 with F suffix)		I <sub>CC2</sub>	1.8	3.8	mA	
		1 Mbps	I <sub>CC1</sub>	2.6	4	mA	
	ENG V AU I VIII		I <sub>CC2</sub>	1 0.3 4.3 0.3 1.6 4.3 1.8 2.6 1.8 2.6 2.5 3.1 10.2			
Supply current - AC signal	EN2 = V <sub>CCI;</sub> All channels switching with square wave clock input; C <sub>I</sub> =	10 Mbps	I <sub>CC1</sub>	4.1	mA		
	15 pF		I <sub>CC2</sub>	1.6 3.6 4.3 5.8 1.8 3.8 2.6 4.1 2.5 4.8 3.1 4.7 10.2 14.3  0.8 2.1 3.1 4.5  1.8 2.7 1.8 3.6 2.6 4.1 2.5 4.8 3.1 4.7 2.5 4.8 3.1 4.7 3.1 4.3	4.8	mA	
		100 Mbps	I <sub>CC1</sub>	3.1	-		
			I <sub>CC2</sub>	10.2	14.3	mA	
ISO7731							
	EN1 = EN2 = 0 V; V <sub>I</sub> = V <sub>CCI</sub> (1)(ISO7	731);	I <sub>CC1</sub>	0.8	2.1	mA	
Supply current - disable	V <sub>I</sub> = 0 V (ISO7731 with F suffix)		I <sub>CC2</sub>	0.7	1.5	mA	
cappi, carrein alcabie	EN1 = EN2 = 0 V; V <sub>I</sub> = 0 V (ISO773	1);	I <sub>CC1</sub>	3	4.5	mA	
	V <sub>I</sub> = V <sub>CCI</sub> (ISO7731 with F suffix)		I <sub>CC2</sub>	1.8	2.7	mA	
	EN1 = EN2 = V <sub>CCI</sub> ; V <sub>I</sub> = V <sub>CCI</sub> (ISO77	'31);	I <sub>CC1</sub>	1.3	2.8	mA	
Supply current - DC signal	V <sub>I</sub> = 0 V (ISO7731 with F suffix)		I <sub>CC2</sub>	1.6	3.7	mA	
cappi, caironi 20 cignai	EN1 = EN2 = V <sub>CCI</sub> ; V <sub>I</sub> = 0 V (ISO773	31);	I <sub>CC1</sub>	3.5	5.3	mA	
	$V_I = V_{CCI}$ (ISO7731 with F suffix)		I <sub>CC2</sub>	2.8	5	mA	
		1 Mbps	I <sub>CC1</sub>	2.4	1 2.2 m/4 0.3 0.7 m/4 4.3 5.8 m/4 0.3 0.7 m/4 1 2.2 m/4 1.6 3.6 m/4 4.3 5.8 m/4 1.8 3.8 m/4 2.6 4 m/4 2.5 4.8 m/4 3.1 4.7 m/4 10.2 14.3 m/4 0.8 2.1 m/4 0.7 1.5 m/4 3 4.5 m/4 1.8 2.7 m/4 1.3 2.8 m/4 1.6 3.7 m/4 2.8 5 m/4 2.4 4.1 m/4 2.2 4.4 m/4 2.7 5.1 m/4 5.6 8 m/4	mA	
			I <sub>CC2</sub>	2.2	4.4	mA	
Supply current - AC signal	EN1 = EN2 = V <sub>CCI</sub> ; All channels switching with square wave clock	10 Mbps	I <sub>CC1</sub>	2.7	4.4	mA	
	input; C <sub>L</sub> = 15 pF		I <sub>CC2</sub>	2.7	5.1	mA	
		100 Mbps	I <sub>CC1</sub>	5.6	8	mA	
			I <sub>CC2</sub>	8	11.6	mA	

<sup>(1)</sup>  $V_{CCI} = Input-side V_{CC}$ 

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## 5.15 Switching Characteristics—5-V Supply

V<sub>CC1</sub> = V<sub>CC2</sub> = 5 V ±10% (over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay time	Con Figure C. 4	6	11	17	ns
PWD	Pulse width distortion <sup>(1)</sup>  t <sub>PHL</sub> - t <sub>PLH</sub>	See Figure 6-1		0.6	5.9	ns
t <sub>sk(o)</sub>	Channel-to-channel output skew time <sup>(2)</sup>	Same-direction channels			4	ns
t <sub>sk(pp)</sub>	Part-to-part skew time <sup>(3)</sup>				4.5	ns
t <sub>r</sub>	Output signal rise time	See Figure 6.4		1.3	3.9	ns
t <sub>f</sub>	Output signal fall time	See Figure 6-1		1.4	3.9	ns
t <sub>PHZ</sub>	Disable propagation delay, high-to-high impedance output			8	22	ns
t <sub>PLZ</sub>	Disable propagation delay, low-to-high impedance output			8	20	ns
	Enable propagation delay, high impedance-to-high output for ISO773x			7	20	ns
t <sub>PZH</sub>	Enable propagation delay, high impedance-to-high output for ISO773x with F suffix	See Figure 6-2		3	8.5	μs
	Enable propagation delay, high impedance-to-low output for ISO773x			3	8.5	μs
t <sub>PZL</sub>	Enable propagation delay, high impedance-to-low output for ISO773x with F suffix			7 20		ns
t <sub>DO</sub>	Default output delay time from input power loss	Measured from the time VCC goes below 1.7V. See Figure 6-3		0.1	0.3	μs
t <sub>ie</sub>	Time interval error	2 <sup>16</sup> – 1 PRBS data at 100 Mbps		0.6		ns

<sup>(1)</sup> Also known as pulse skew.

<sup>(2)</sup> t<sub>sk(o)</sub> is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

<sup>(3)</sup>  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 5.16 Switching Characteristics—3.3-V Supply

V<sub>CC1</sub> = V<sub>CC2</sub> = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay time	See Figure 6.1	6	11	18.5	ns
PWD	Pulse width distortion <sup>(1)</sup>  t <sub>PHL</sub> - t <sub>PLH</sub>	See Figure 6-1		0.1	5.9	ns
t <sub>sk(o)</sub>	Channel-to-channel output skew time <sup>(2)</sup>	Same-direction channels			4.4	ns
t <sub>sk(pp)</sub>	Part-to-part skew time <sup>(3)</sup>				5	ns
t <sub>r</sub>	Output signal rise time	See Figure 6.1		1.3	3	ns
t <sub>f</sub>	Output signal fall time	See Figure 6-1		1.3	3	ns
t <sub>PHZ</sub>	Disable propagation delay, high-to-high impedance output			17	31	ns
t <sub>PLZ</sub>	Disable propagation delay, low-to-high impedance output			17	30	ns
	Enable propagation delay, high impedance-to-high output for ISO773x			17	30	ns
t <sub>PZH</sub>	Enable propagation delay, high impedance-to-high output for ISO773x with F suffix	See Figure 6-2		3.2	8.5	μs
	Enable propagation delay, high impedance-to-low output for ISO773x			3.2	8.5	μs
t <sub>PZL</sub>	Enable propagation delay, high impedance-to-low output for ISO773x with F suffix			17		ns
t <sub>DO</sub>	Default output delay time from input power loss	Measured from the time VCC goes below 1.7V. See Figure 6-3		0.1	0.3	μs
t <sub>ie</sub>	Time interval error	2 <sup>16</sup> – 1 PRBS data at 100 Mbps		0.6		ns

<sup>(1)</sup> Also known as pulse skew.

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<sup>(2)</sup> t<sub>sk(o)</sub> is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

<sup>(3)</sup>  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.



## 5.17 Switching Characteristics—2.5-V Supply

 $V_{CC1} = V_{CC2} = 2.5 \text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay time	Con Figure C. 4	7.5	12	21	ns
PWD	Pulse width distortion <sup>(1)</sup>  t <sub>PHL</sub> - t <sub>PLH</sub>	See Figure 6-1		0.2	5.9	ns
t <sub>sk(o)</sub>	Channel-to-channel output skew time <sup>(2)</sup>	Same-direction channels			4.4	ns
t <sub>sk(pp)</sub>	Part-to-part skew time <sup>(3)</sup>				5.3	ns
t <sub>r</sub>	Output signal rise time	Con Firmum C. 4		1	3.5	ns
t <sub>f</sub>	Output signal fall time	See Figure 6-1		1	3.5	ns
t <sub>PHZ</sub>	Disable propagation delay, high-to-high impedance output			22	41	ns
t <sub>PLZ</sub>	Disable propagation delay, low-to-high impedance output			22	40	ns
	Enable propagation delay, high impedance-to-high output for ISO773x			18	40	ns
<sup>t</sup> PZH	Enable propagation delay, high impedance-to-high output for ISO773x with F suffix	See Figure 6-2		3.3	8.5	μs
	Enable propagation delay, high impedance-to-low output for ISO773x			3.3	21 5.9 4.4 5.3 3.5 3.5 41 40	μs
t <sub>PZL</sub>	Enable propagation delay, high impedance-to-low output for ISO773x with F suffix			18		ns
t <sub>DO</sub>	Default output delay time from input power loss	Measured from the time VCC goes below 1.7V. See Figure 6-3		0.1	0.3	μs
t <sub>ie</sub>	Time interval error	2 <sup>16</sup> – 1 PRBS data at 100 Mbps		0.6		ns

<sup>(1)</sup> Also known as pulse skew.

<sup>(2)</sup> t<sub>sk(o)</sub> is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

<sup>(3)</sup>  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.



#### 5.18 Insulation Characteristics Curves

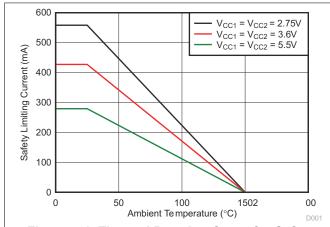


Figure 5-1. Thermal Derating Curve for Safety Limiting Current per VDE for DW-16 Package

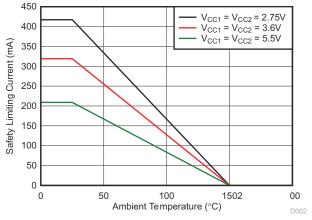


Figure 5-2. Thermal Derating Curve for Safety Limiting Current per VDE for DBQ-16 Package

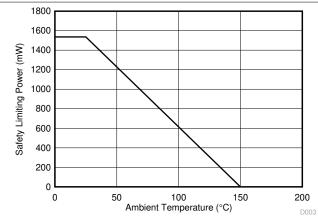


Figure 5-3. Thermal Derating Curve for Safety Limiting Power per VDE for DW-16 Package

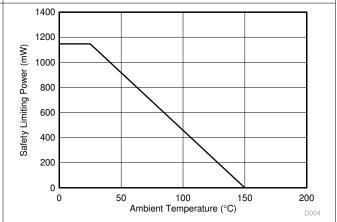
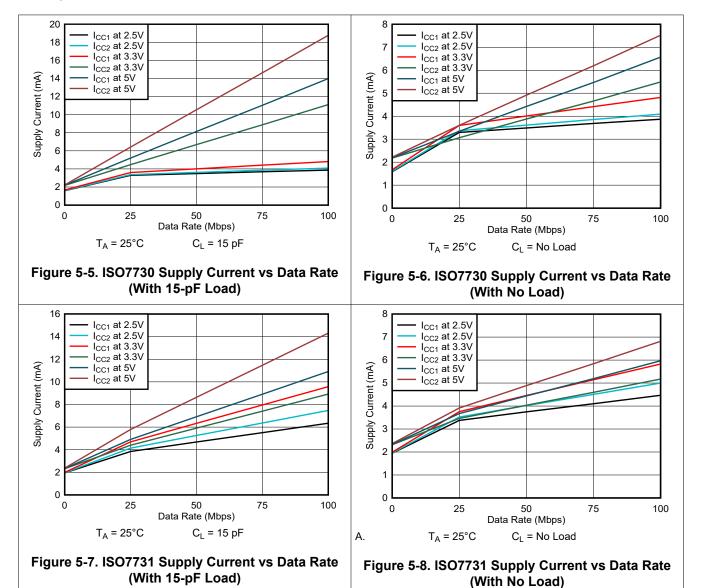


Figure 5-4. Thermal Derating Curve for Safety Limiting Power per VDE for DBQ-16 Package

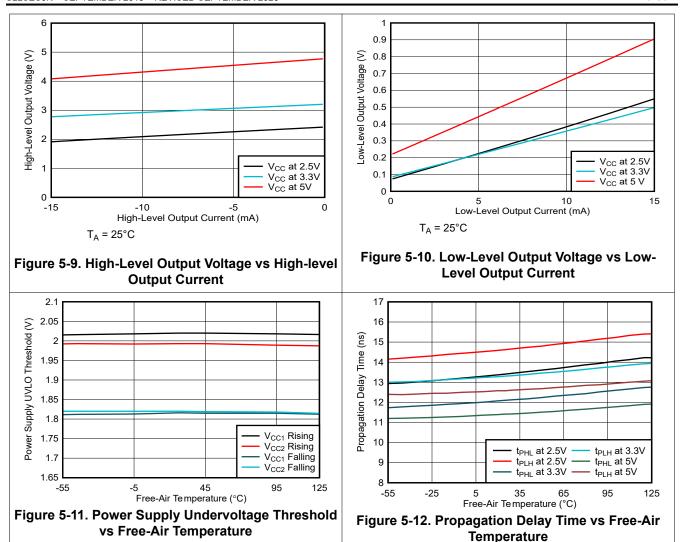
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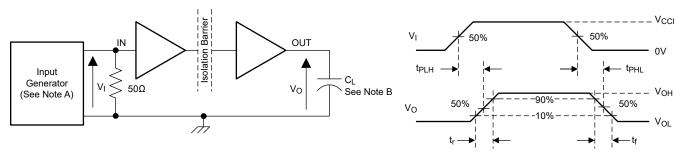
## **5.19 Typical Characteristics**





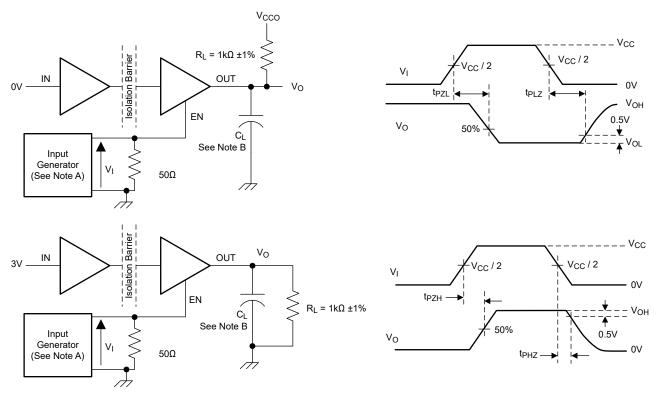


### **6 Parameter Measurement Information**



- A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle,  $t_r \le 3$  ns,  $t_f \le 3$ ns,  $t_f$
- B.  $C_L = 15 \text{ pF}$  and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

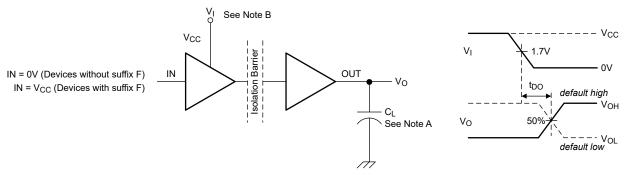
Figure 6-1. Switching Characteristics Test Circuit and Voltage Waveforms



- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  10 kHz, 50% duty cycle,  $t_r \leq$  3 ns,  $t_f \leq$  3 ns,  $Z_O =$  50  $\Omega$ .
- B.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

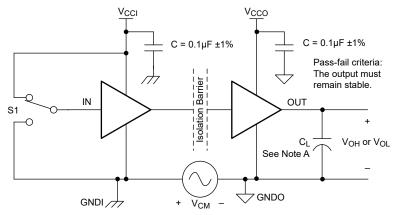
Figure 6-2. Enable/Disable Propagation Delay Time Test Circuit and Waveform





- A. C<sub>L</sub> = 15 pF and includes instrumentation and fixture capacitance within ±20%.
- B. Power Supply Ramp Rate = 10 mV/ns

Figure 6-3. Default Output Delay Time Test Circuit and Voltage Waveforms



A.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

Figure 6-4. Common-Mode Transient Immunity Test Circuit

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## 7 Detailed Description

#### 7.1 Overview

The ISO773x family of devices has an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. If the ENx pin is low then the output goes to high impedance. The ISO773x family of devices also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 7-1, shows a functional block diagram of a typical channel.

### 7.2 Functional Block Diagram

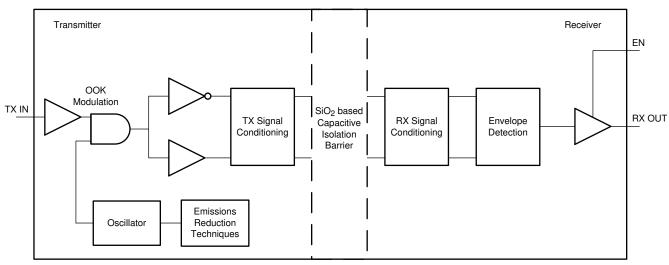


Figure 7-1. Conceptual Block Diagram of a Digital Capacitive Isolator

Figure 7-2 shows a conceptual detail of how the ON-OFF keying scheme works.

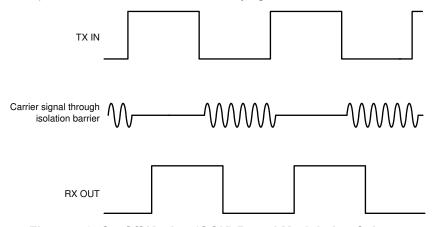


Figure 7-2. On-Off Keying (OOK) Based Modulation Scheme



#### 7.3 Feature Description

Table 7-1 provides an overview of the device features.

Table 7-1. Device Features

PART NUMBER	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT	PACKAGE	RATED ISOLATION(1)
ISO7730	3 Forward,	100 Mbps	High	DW-16	5000 V <sub>RMS</sub> / 8000 V <sub>PK</sub>
1307730	0 Reverse	roo waps	riigii	DBQ-16	3000 V <sub>RMS</sub> / 4242 V <sub>PK</sub>
ISO7730 with F	3 Forward,	100 Mbps	100 Mbps Low		5000 V <sub>RMS</sub> / 8000 V <sub>PK</sub>
suffix	0 Reverse	Reverse	LOW	DBQ-16	3000 V <sub>RMS</sub> / 4242 V <sub>PK</sub>
ISO7731	2 Forward, 1 Reverse	100 Mbps	High -	DW-16	5000 V <sub>RMS</sub> / 8000 V <sub>PK</sub>
1307731				DBQ-16	3000 V <sub>RMS</sub> / 4242 V <sub>PK</sub>
ISO7731 with F	2 Forward,	100 Mbps	Low	DW-16	5000 V <sub>RMS</sub> / 8000 V <sub>PK</sub>
suffix	1 Reverse	100 Mbps	LOW	DBQ-16	3000 V <sub>RMS</sub> / 4242 V <sub>PK</sub>
ISO7731B	2 Forward, 1 Reverse	100 Mbps	High	DW-16	5000 V <sub>RMS</sub> / 8000 V <sub>PK</sub>
ISO7731B with F suffix	2 Forward, 1 Reverse	100 Mbps	Low	DW-16	5000 V <sub>RMS</sub> / 8000 V <sub>PK</sub>

<sup>(1)</sup> See Section 5.7 for detailed isolation ratings.

#### 7.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO773x family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- · Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by providing purely differential internal operation.

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#### 7.4 Device Functional Modes

Table 7-2 lists the functional modes for the ISO773x devices.

<b>Table</b>	7-2	Fun	ction	Table

V <sub>CCI</sub>	V <sub>cco</sub>	INPUT (INx) <sup>(2)</sup>	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)	COMMENTS	
		Н	H or open	Н	Normal Operation:	
		L	H or open	L	A channel output assumes the logic state of the input.	
PU	PU	Open	H or open	Default	Default mode: When INx is open, the corresponding channel output goes to the default logic state. Default is <i>High</i> for ISO773x and <i>Low</i> for ISO773x with F suffix.	
Х	PU	X	L	Z	A low value of Output Enable causes the outputs to be high-impedance	
PD	PU	×	H or open	Default	Default mode: When $V_{CCl}$ is unpowered, a channel output assumes the logic state based on the selected default option. Default is $\mathit{High}$ for ISO773x and $\mathit{Low}$ for ISO773x with F suffix. When $V_{CCl}$ transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When $V_{CCl}$ transitions from powered-up to unpowered, channel output assumes the selected default state.	
Х	PD	х	Х	Undetermined	When V <sub>CCO</sub> is unpowered, a channel output is undetermined <sup>(1)</sup> . When V <sub>CCO</sub> transitions from unpowered to powered-up, a channel output assumes the logic state of the input	

- (1) The outputs are in undetermined state when 1.7 V <  $V_{CCI}$ ,  $V_{CCO}$  < 2.25 V.
- (2) A strongly driven input signal can weakly power the floating V<sub>CC</sub> using an internal protection diode and cause undetermined output.

#### 7.4.1 Device I/O Schematics

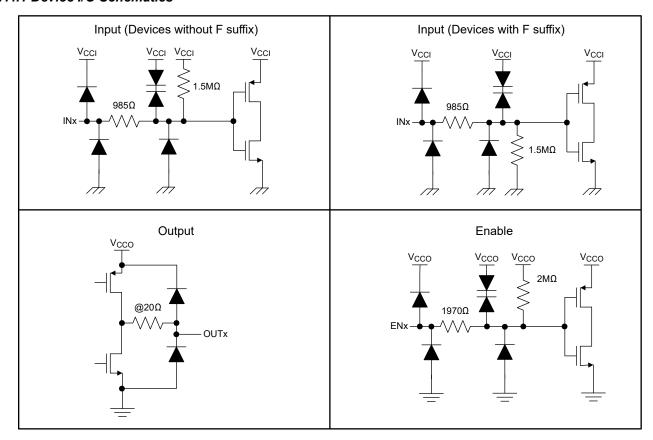


Figure 7-3. Device I/O Schematics

## 8 Application and Implementation

#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The ISO773x devices are high-performance, triple-channel digital isolators. These devices come with enable pins on each side which can be used to put the respective outputs in high impedance for multi-controller driving applications and reduce power consumption. The ISO773x family of devices use single-ended CMOS-logic switching technology. The voltage range is from 2.25 V to 5.5 V for both supplies,  $V_{CC1}$  and  $V_{CC2}$ . When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is,  $\mu$ C or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

#### 8.2 Typical Application

The ISO7731 device, combined with Texas Instruments' mixed-signal microcontroller, RS-485 transceiver, transformer driver, and voltage regulator, can create an isolated RS-485 system as shown in Figure 8-1.

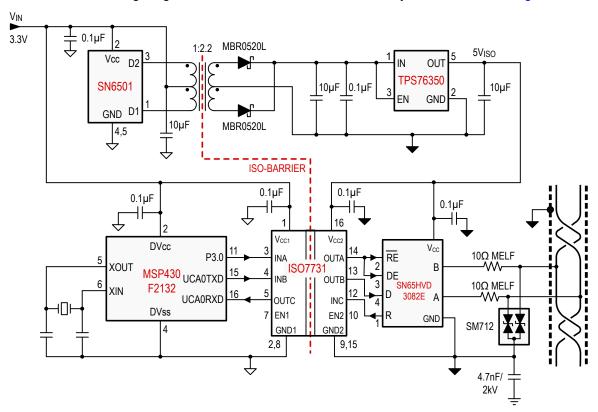


Figure 8-1. Isolated RS-485 Interface Circuit



#### 8.2.1 Design Requirements

To design with these devices, use the parameters listed in Table 8-1.

Table 8-1. Design Parameters

PARAMETER	VALUE
Supply voltage, V <sub>CC1</sub> and V <sub>CC2</sub>	2.25 to 5.5 V
Decoupling capacitor between V <sub>CC1</sub> and GND1	0.1 μF
Decoupling capacitor from V <sub>CC2</sub> and GND2	0.1 μF

### 8.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO773x family of devices only requires two external bypass capacitors to operate. Figure 8-2 and Figure 8-3 show the typical circuit hook-up for the devices.

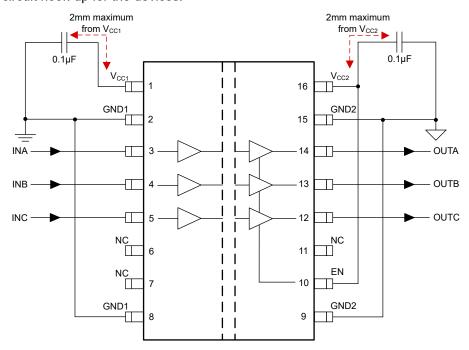


Figure 8-2. Typical ISO7730 Circuit Hook-Up



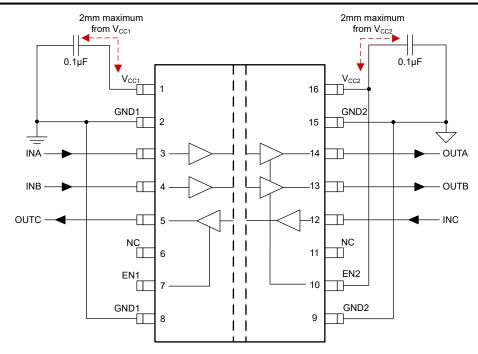
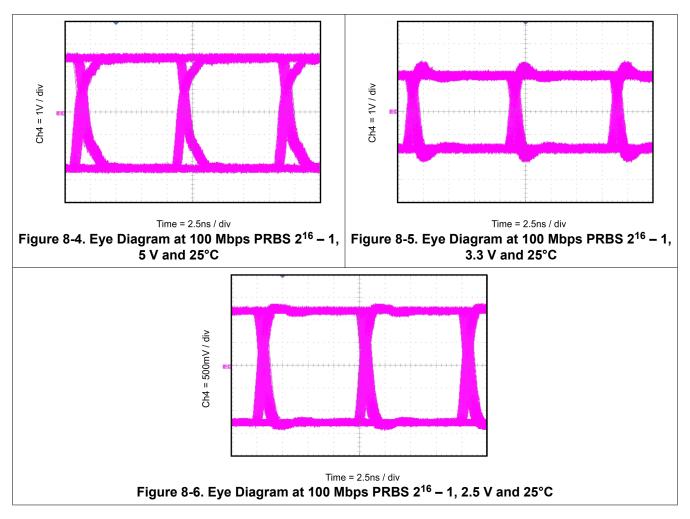


Figure 8-3. Typical ISO7731 Circuit Hook-Up

#### 8.2.3 Application Curves

The following typical eye diagrams of the ISO773x family of devices indicate low jitter and wide open eye at the maximum data rate of 100 Mbps.



#### 8.2.3.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See Figure 8-7 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that is 20% higher than the specified value.

Figure 8-8 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over the lifetime of the barrier. Based on the TDDB data, the intrinsic capability of the insulation is 1500  $V_{RMS}$  with a lifetime of 36 years. Other factors, such as package size, pollution degree, material group, and more can further limit the working voltage of the component. The working voltage of DW-16 package is specified up to 1500  $V_{RMS}$ . At the lower working voltages, the corresponding insulation lifetime is much longer than 36 years. DBQ-16 package at 400  $V_{RMS}$  working voltage has a much longer lifetime than DW-16 package.



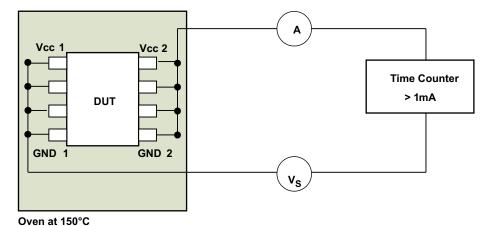


Figure 8-7. Test Setup for Insulation Lifetime Measurement

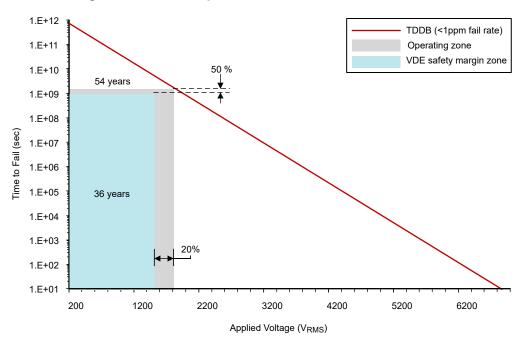


Figure 8-8. Insulation Lifetime Projection Data

#### 8.3 Power Supply Recommendations

To help provide reliable operation at data rates and supply voltages, a  $0.1-\mu F$  bypass capacitor is recommended at the input and output supply pins ( $V_{CC1}$  and  $V_{CC2}$ ). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501 or SN6505A. For such applications, detailed power supply design and transformer selection recommendations are available in the SN6501 Transformer Driver for Isolated Power Supplies data sheet or SN6505A Low-Noise 1-A Transformer Drivers for Isolated Power Supplies (SLLSEP9).

#### 8.4 Layout

#### 8.4.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 8-9). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

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- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch<sup>2</sup>.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. This makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide*.

#### 8.4.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit boards. This PCB is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and self-extinguishing flammability-characteristics.

#### 8.4.2 Layout Example

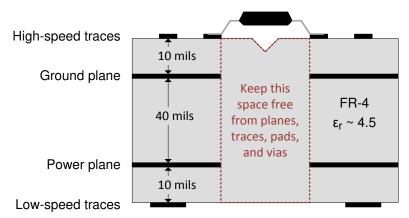


Figure 8-9. Layout Example Schematic



## 9 Device and Documentation Support

#### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, Digital Isolator Design Guide
- Texas Instruments, Isolation Glossary
- Texas Instruments, How to use isolation to improve ESD, EFT, and Surge immunity in industrial systems application report
- Texas Instruments, SN6501 Transformer Driver for Isolated Power Supplies data sheet
- Texas Instruments, SNx5HVD308xE Low-Power RS-485 Transceivers, Available in a Small MSOP-8 Package data sheet
- Texas Instruments, TPS76350 Low-Power 150-mA Low-Dropout Linear Regulators data sheet
- Texas Instruments, MSP430F2132 Mixed Signal Microcontroller data sheet

#### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 9.4 Trademarks

TI E2E<sup>™</sup> is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

#### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

#### 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

## Changes from Revision J (October 2024) to Revision K (September 2025)

Page

Added Low-level input current for INx and High-level Input current for ENx throughout the Specifications .....4

## Changes from Revision I (August 2023) to Revision J (October 2024)

Pag

Product Folder Links: ISO7730 ISO7731

w				

Updated the TDDB plot and the projected lifetime	
Deleted the Community Resources section and added the Support Resources section	ion34
Changes from Revision H (March 2023) to Revision I (August 2023)	Page
<ul> <li>Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Cu accurate system-level thermal calculations</li> </ul>	•
Updated electrical and switching characteristics to match device performance	17
Changes from Revision G (March 2020) to Revision H (March 2023)	Page
Changed standard name from: "DIN V VDE V 0884-11:2017-01" to: "DIN EN IEC 60 throughout the document	,
• Removed references to standard IEC/EN/CSA 60950-1 throughout the document	1
• Removed standard revision and year references from all standard names throughout the dead Maximum impulses veltage (1/2) and distribution from DIN EN ISC 60747.47 (1/2)	
<ul> <li>Added Maximum impulse voltage (V<sub>IMP</sub>) specification per DIN EN IEC 60747-17 (V</li> <li>Changed test conditions and values of Maximum surge isolation voltage (V<sub>IOSM</sub>) specification</li> </ul>	DE 0884-17)7 ecification per DIN EN IEC
<ul> <li>Added Maximum impulse voltage (V<sub>IMP</sub>) specification per DIN EN IEC 60747-17 (V</li> </ul>	DE 0884-17)7 ecification per DIN EN IEC 7

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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3-Sep-2025

## **PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
ISO7730DBQR	Active	Production	SSOP (DBQ)   16	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7730
ISO7730DBQR.A	Active	Production	SSOP (DBQ)   16	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7730
ISO7730DBQR.B	Active	Production	SSOP (DBQ)   16	2500   LARGE T&R	-	Call TI	Call TI	-55 to 125	
ISO7730DWR	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7730
ISO7730DWR.A	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7730
ISO7730DWR.B	Active	Production	SOIC (DW)   16	2000   LARGE T&R	-	Call TI	Call TI	-55 to 125	
ISO7730FDBQR	Active	Production	SSOP (DBQ)   16	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7730F
ISO7730FDBQR.A	Active	Production	SSOP (DBQ)   16	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7730F
ISO7730FDBQR.B	Active	Production	SSOP (DBQ)   16	2500   LARGE T&R	-	Call TI	Call TI	-55 to 125	
ISO7730FDWR	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7730F
ISO7730FDWR.A	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7730F
ISO7730FDWR.B	Active	Production	SOIC (DW)   16	2000   LARGE T&R	-	Call TI	Call TI	-55 to 125	
ISO7731BDWR	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7731B
ISO7731BDWR.A	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7731B
ISO7731BDWR.B	Active	Production	SOIC (DW)   16	2000   LARGE T&R	-	Call TI	Call TI	-55 to 125	
ISO7731DBQR	Active	Production	SSOP (DBQ)   16	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7731
ISO7731DBQR.A	Active	Production	SSOP (DBQ)   16	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7731
ISO7731DBQR.B	Active	Production	SSOP (DBQ)   16	2500   LARGE T&R	-	Call TI	Call TI	-55 to 125	
ISO7731DBQRG4	Active	Production	SSOP (DBQ)   16	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7731
ISO7731DBQRG4.A	Active	Production	SSOP (DBQ)   16	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7731
ISO7731DBQRG4.B	Active	Production	SSOP (DBQ)   16	2500   LARGE T&R	-	Call TI	Call TI	-55 to 125	
ISO7731DWR	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7731
ISO7731DWR.A	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7731
ISO7731DWR.B	Active	Production	SOIC (DW)   16	2000   LARGE T&R	-	Call TI	Call TI	-55 to 125	
ISO7731FBDWR	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7731FB
ISO7731FBDWR.A	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7731FB
ISO7731FBDWR.B	Active	Production	SOIC (DW)   16	2000   LARGE T&R	-	Call TI	Call TI	-55 to 125	
ISO7731FDBQR	Active	Production	SSOP (DBQ)   16	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7731F
ISO7731FDBQR.A	Active	Production	SSOP (DBQ)   16	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7731F

-55 to 125

Call TI

Call TI

3-Sep-2025

ISO7731FDWR.B

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Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
ISO7731FDBQR.B	Active	Production	SSOP (DBQ)   16	2500   LARGE T&R	-	Call TI	Call TI	-55 to 125	
ISO7731FDWR	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7731F
ISO7731FDWR.A	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7731F

2000 | LARGE T&R

Active

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

Production

- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

SOIC (DW) | 16

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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#### OTHER QUALIFIED VERSIONS OF ISO7730, ISO7731:

Automotive: ISO7730-Q1, ISO7731-Q1

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.



### **PACKAGE OPTION ADDENDUM**

www.ti.com 3-Sep-2025

NOTE: C	Qualified (	Version	Definitions
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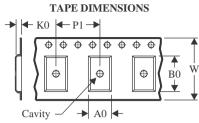
• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



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### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7730DBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7730DBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7730DBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7730DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7730DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7730FDBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7730FDBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7730FDBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7730FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7730FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7731BDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7731BDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7731DBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7731DBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7731DBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7731DBQRG4	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



# **PACKAGE MATERIALS INFORMATION**

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Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7731DBQRG4	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7731DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7731FBDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7731FBDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7731FDBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7731FDBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7731FDBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7731FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1



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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7730DBQR	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7730DBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO7730DBQR	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7730DWR	SOIC	DW	16	2000	356.0	356.0	45.0
ISO7730DWR	SOIC	DW	16	2000	353.0	353.0	32.0
ISO7730FDBQR	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7730FDBQR	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7730FDBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO7730FDWR	SOIC	DW	16	2000	356.0	356.0	45.0
ISO7730FDWR	SOIC	DW	16	2000	353.0	353.0	32.0
ISO7731BDWR	SOIC	DW	16	2000	356.0	356.0	36.0
ISO7731BDWR	SOIC	DW	16	2000	353.0	353.0	32.0
ISO7731DBQR	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7731DBQR	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7731DBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO7731DBQRG4	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7731DBQRG4	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7731DWR	SOIC	DW	16	2000	353.0	353.0	32.0



# **PACKAGE MATERIALS INFORMATION**

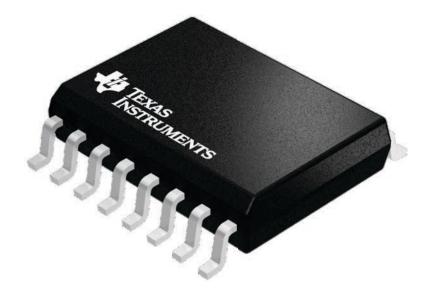
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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7731FBDWR	SOIC	DW	16	2000	353.0	353.0	32.0
ISO7731FBDWR	SOIC	DW	16	2000	356.0	356.0	36.0
ISO7731FDBQR	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7731FDBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO7731FDBQR	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7731FDWR	SOIC	DW	16	2000	353.0	353.0	32.0

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





SOIC



### NOTES:

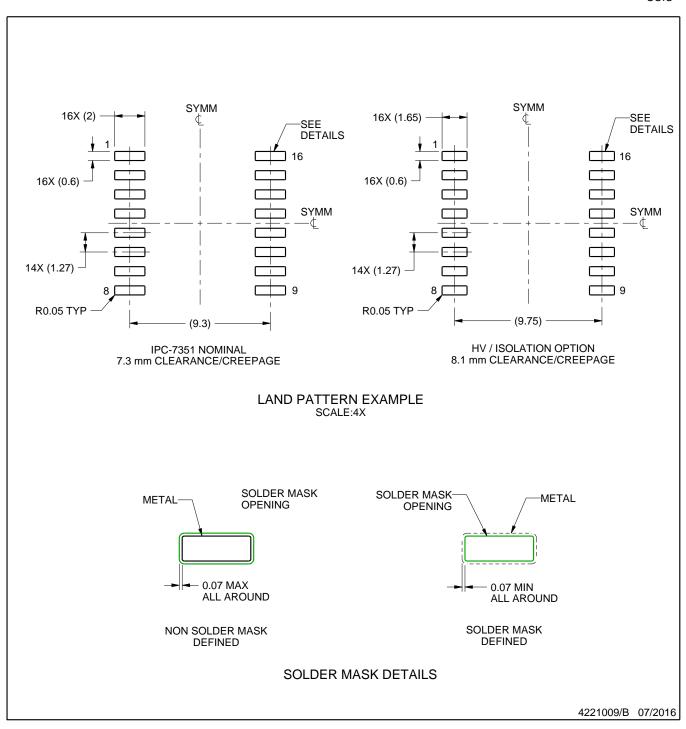
- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
- 5. Reference JEDEC registration MS-013.



SOIC



### NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



### NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





SHRINK SMALL-OUTLINE PACKAGE



### NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
- 4. This dimension does not include interlead flash.5. Reference JEDEC registration MO-137, variation AB.



SHRINK SMALL-OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SHRINK SMALL-OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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