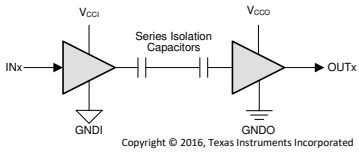
ISO676x-Q1 General-Purpose Six-Channel Automotive Reinforced Digital Isolators with Robust EMC

1 Features

- AEC-Q100 qualified with the following results:
  - Device temperature Grade 1: –40°C to +125°C ambient operating temperature range
- Meets VDA320 isolation requirements
- 50 Mbps data rate
- Robust isolation barrier:
  - High lifetime at 1500 V_{RMS} working voltage
  - Up to 5000 V_{RMS} isolation rating
  - Up to 10 kV surge capability
  - ±150 kV/µs typical CMTI
- Wide supply range: 1.71 V to 1.89 V and 2.25 V to 5.5 V
- 1.71 V to 5.5 V level translation
- Default output *high* (ISO676x-Q1) and *low* (ISO676xF-Q1) options
- 1.6 mA per channel typical at 1 Mbps
- Low propagation delay: 11 ns typical
- Robust electromagnetic compatibility (EMC)
  - System-level ESD, EFT, and surge immunity
  - Low emissions
- Wide-SOIC (DW-16) Package
- Safety-Related Certifications:
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 component recognition program
  - IEC 62368-1, IEC 61010-1, IEC 60601-1 and GB 4943.1 certifications

2 Applications

- Hybrid, electric and power train system (EV/HEV)
  - Battery management system (BMS)
  - On-board charger
  - DC/DC converter
  - Inverter and motor control



V_{CCI}=Input supply, V_{CCO}=Output supply
GNDI=Input ground, GNDO=Output ground

Simplified Schematic

3 Description

The ISO676x-Q1 devices are high-performance, six-channel digital isolators ideal for cost-sensitive applications requiring up to 5000 V_{RMS} isolation ratings per UL 1577. These devices are also certified by VDE, TUV, CSA, and CQC.

The ISO676x-Q1 devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by TI's double capacitive silicon dioxide (SiO_2) insulation barrier. The ISO676x family of devices is available in all possible pin configurations such that all six channels are in the same direction, or one, two, or three channels are in reverse direction while the remaining channels are in forward direction. In the event of input power or signal loss, the default output is *high* for devices without suffix F and *low* for devices with suffix F. See Device Functional Modes section for further details.

Used in conjunction with isolated power supplies, these devices help prevent noise currents on data buses, such as CAN and LIN from damaging sensitive circuitry. Through innovative chip design and layout techniques, the electromagnetic compatibility of the ISO676x-Q1 devices has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. The ISO676x-Q1 family of devices is available in a 16-pin SOIC wide-body (DW) package and is a pin-to-pin upgrade to the older generations.

Device Description

Part Number (1)	Package	Body Size
ISO6760-Q1, ISO6760F-Q1, ISO6761-Q1, ISO6761F-Q1, ISO6762-Q1, ISO6762F-Q1, ISO6763-Q1, ISO6763F-Q1	SOIC (DW)	10.30 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2022) to Revision C (May 2023)	Page
• Changed standard name from: "DIN VDE V 0884-11:2017-01" to: "DIN EN IEC 60747-17 (VDE 0884-17)" throughout the document	1
• Updated standards marked as 'planned' to include certificate numbers throughout the document	1
• Removed standard revision and year references from all standard names throughout the document	1
• Added Maximum impulse voltage (V_{IMP}) specification per DIN EN IEC 60747-17 (VDE 0884-17)	8
• Changed test conditions and values of Maximum surge isolation voltage (V_{IOSM}) specification per DIN EN IEC 60747-17 (VDE 0884-17)	8
• Clarified method b test conditions of Apparent charge (q_{PD})	8
• Changed working voltage lifetime margin from: 87.5% to: 50%, minimum required insulation lifetime from: 37.5 years to: 30 years and insulation lifetime per TDDB from: 220 years to: 36 years per DIN EN IEC 60747-17 (VDE 0884-17)	32
• Changed Figure 9-8 per DIN EN IEC 60747-17 (VDE 0884-17)	32
• Updated to DW0016B mechanical drawing	36

Changes from Revision A (November 2021) to Revision B (May 2022)	Page
• Updated CMTI spec for 5-V, 3.3-V and 2.5-V supply conditions	5

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5 Pin Configuration and Functions

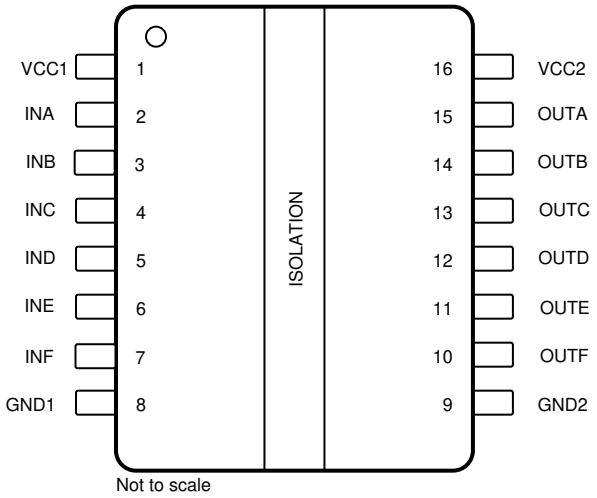

Figure 5-1. ISO6760-Q1 DW Package 16-Pin SOIC-WB Top View

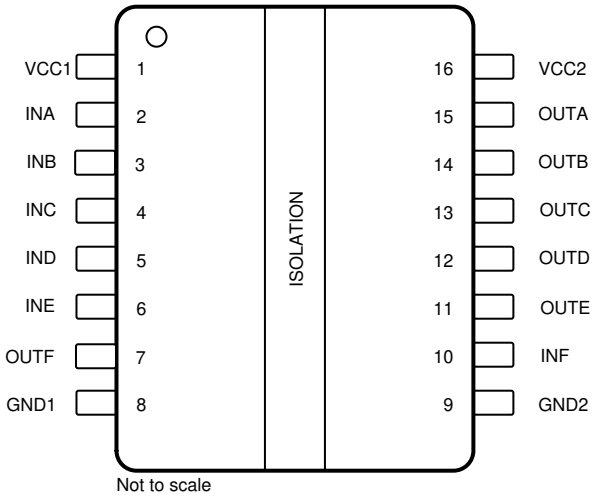

Figure 5-2. ISO6761-Q1 DW Package 16-Pin SOIC-WB Top View

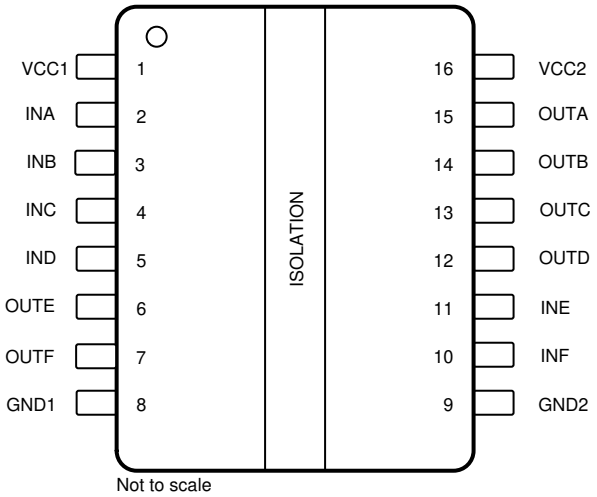

Figure 5-3. ISO6762-Q1 DW Package 16-Pin SOIC-WB Top View

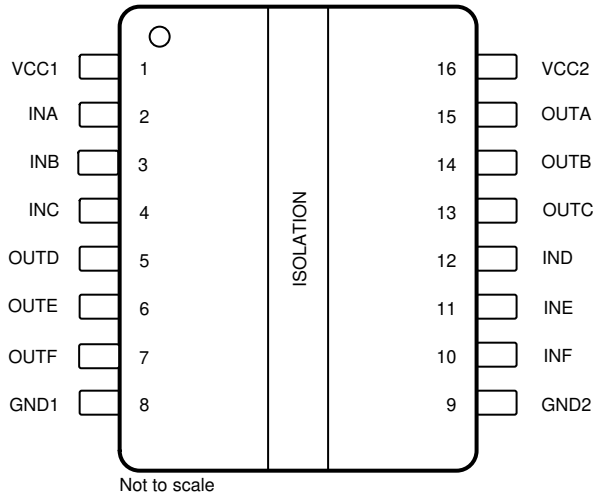

Figure 5-4. ISO6763-Q1 DW Package 16-Pin SOIC-WB Top View

Table 5-1. Pin Functions

PIN					I/O	DESCRIPTION
NAME	NO.					
	ISO6760-Q1	ISO6761-Q1	ISO6762-Q1	ISO6763-Q1		
GND1	8	8	8	8	—	Ground connection for V_{CC1}
GND2	9	9	9	9	—	Ground connection for V_{CC2}
INA	2	2	2	2	I	Input, channel A
INB	3	3	3	3	I	Input, channel B
INC	4	4	4	4	I	Input, channel C
IND	5	5	5	12	I	Input, channel D
INE	6	6	11	11	I	Input, channel E
INF	7	10	10	10	I	Input, channel F
OUTA	15	15	15	15	O	Output, channel A
OUTB	14	14	14	14	O	Output, channel B
OUTC	13	13	13	13	O	Output, channel C
OUTD	12	12	12	5	O	Output, channel D
OUTE	11	11	6	6	O	Output, channel E
OUTF	10	7	7	7	O	Output, channel F
V_{CC1}	1	1	1	1	—	Power supply, side 1
V_{CC2}	16	16	16	16	—	Power supply, side 2

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6 Specifications

6.1 Absolute Maximum Ratings

See[1]

		MIN	MAX	UNIT
Supply Voltage [2]	V_{CC1} to GND1	-0.5	6	V
	V_{CC2} to GND2	-0.5	6	
Input/Output Voltage	INx to GNDx	-0.5	V_{CCX} + 0.5 [3]	V
	OUTx to GNDx	-0.5	V_{CCX} + 0.5 [3]	
Output Current	I_o	-15	15	mA
Temperature	Operating junction temperature, T_J		150	°C
	Storage temperature, T_{stg}	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

(1) (2)

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC1} (1)	Supply Voltage Side 1	V_{CC} = 1.8V(3)	1.71		1.89	V
		V_{CC} = 2.5V to 5V(3)	2.25		5.5	V
V_{CC2} (1)	Supply Voltage Side 2	V_{CC} = 1.8V(3)	1.71		1.89	V
		V_{CC} = 2.5V to 5V(3)	2.25		5.5	V
$V_{cc\ (UVLO+)}$	UVLO threshold when supply voltage is rising			1.53	1.71	V
$V_{cc(UVLO-)}$	UVLO threshold when supply voltage is falling		1.1	1.41		V
$V_{hys(UVLO)}$	Supply voltage UVLO hysteresis		0.08	0.13		V
V_{IH}	High level Input voltage		0.7 x V_{CCI} (2)		V_{CCI}	V
V_{IL}	Low level Input voltage		0		0.3 x V_{CCI}	V
I_{OH}	High level output current	V_{CCO} (2) = 5 V	-4			mA
		V_{CCO} = 3.3 V	-2			mA
		V_{CCO} = 2.5 V	-1			mA
		V_{CCO} = 1.8 V	-1			mA
I_{OL}	Low level output current	V_{CCO} = 5 V			4	mA
		V_{CCO} = 3.3 V			2	mA
		V_{CCO} = 2.5 V			1	mA
		V_{CCO} = 1.8 V			1	mA
DR	Data Rate		0		50	Mbps
T_A	Ambient temperature		-40	25	125	°C

(1) V_{CC1} and V_{CC2} can be set independent of one another
(2) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(3) The channel outputs are in undetermined state when 1.89 V < V_{CC1}, V_{CC2} < 2.25 V and 1.05 V < V_{CC1}, V_{CC2} < 1.71 V

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6.4 Thermal Information

THERMAL METRIC [1]		ISO676x DW (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO6760						
P_D	Maximum power dissipation (both sides)	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L =$ 15 pF, Input a 25-MHz 50% duty cycle square wave			192	mW
P_{D1}	Maximum power dissipation (side-1)				45	mW
P_{D2}	Maximum power dissipation (side-2)				147	mW
ISO6761						
P_D	Maximum power dissipation (both sides)	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L =$ 15 pF, Input a 25-MHz 50% duty cycle square wave			197	mW
P_{D1}	Maximum power dissipation (side-1)				63	mW
P_{D2}	Maximum power dissipation (side-2)				134	mW
ISO6762						
P_D	Maximum power dissipation (both sides)	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L =$ 15 pF, Input a 25-MHz 50% duty cycle square wave			197	mW
P_{D1}	Maximum power dissipation (side-1)				81	mW
P_{D2}	Maximum power dissipation (side-2)				116	mW
ISO6763						
P_D	Maximum power dissipation (both sides)	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L =$ 15 pF, Input a 25-MHz 50% duty cycle square wave			196	mW
P_{D1}	Maximum power dissipation (side-1)				98	mW
P_{D2}	Maximum power dissipation (side-2)				98	mW

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6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			DW-16	
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test; See Figure 9-8	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1 s (100% production)	7071	V_{PK}
V_{IMP}	Maximum impulse voltage[3]	Tested in air, 1.2/50-us waveform per IEC 62368-1	7692	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[4]	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge[5]	Method a, After Input-output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤5	
		Method b: At routine test (100% production) and preconditioning (type test); $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s (method b1) or $V_{pd(m)} = V_{ini}$, $t_m = t_{ini}$ (method b2)	≤5	
C_{IO}	Barrier capacitance, input to output[6]	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1 MHz	~1	pF
R_{IO}	Isolation resistance[6]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier tied together creating a two-terminal device.

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6.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 62368-1, IEC 61010-1 and IEC 60601	Certified according to UL 1577 Component Recognition Program	Certified according to GB 4943.1	Certified according to EN 61010-1 and EN 62368-1
Maximum transient isolation voltage, 7071 V_{PK}; Maximum repetitive peak isolation voltage, 2121 V_{PK}; Maximum surge isolation voltage, 10000 V_{PK}	600 V_{RMS} reinforced insulation per CSA 62368-1 and IEC 62368-1; 600 V_{RMS} reinforced insulation per CSA 61010-1 and IEC 61010-1 (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1 and IEC 60601-1, 250 V_{RMS} max working voltage	Single protection, 5000 V_{RMS}	Reinforced insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V_{RMS} maximum working voltage	5000 V_{RMS} reinforced insulation per EN 61010-1 and EN 62368-1 up to working voltage of 600 V_{RMS}
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate number: CQC21001304083	Client ID number: 077311

6.8 Safety Limiting Values

Safety limiting[(1)] intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I_S	Safety input, output, or supply current [(1)]	$R_{\theta JA}$ =68.8°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			330	mA
		$R_{\theta JA}$ = 68.8°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			504	mA
		$R_{\theta JA}$ = 68.8°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C			660	mA
		$R_{\theta JA}$ = 68.8°C/W, V_I = 1.89 V, T_J = 150°C, T_A = 25°C			956	mA
P_S	Safety input, output, or total power [(1)]	$R_{\theta JA}$ = 68.8°C/W, T_J = 150°C, T_A = 25°C			1820	mW
T_S	Maximum safety temperature [(1)]				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

6.9 Electrical Characteristics—5-V Supply

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -4 mA; See Figure 7-1	V_{CCO} - 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; See Figure 7-1			0.4	V
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0 V, V_{CM} = 1200 V; See Figure 7-3	100	150		kV/µs
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2 MHz, V_{CC} = 5 V		2.8		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

6.10 Supply Current Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6760							
Supply current - DC signal	V_I = VCC1 (ISO6760); V_I = 0 V (ISO6760 with F suffix)		I_{CC1}		2.2	2.8	mA
			I_{CC2}		3.1	5.2	
	V_I = 0 V (ISO6760); V_I = VCC1 (ISO6760 with F suffix)		I_{CC1}		8.3	11.1	
			I_{CC2}		3.4	5.7	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		5.3	7.0	
			I_{CC2}		3.7	5.9	
		10 Mbps	I_{CC1}		5.4	7.2	
			I_{CC2}		7.0	9.7	
		50 Mbps	I_{CC1}		6.3	8.1	
			I_{CC2}		21.9	26.6	
ISO6761							
Supply current - DC signal	V_I = VCC1 (ISO6761); V_I = 0 V (ISO6761 with F suffix)		I_{CC1}		2.4	3.5	mA
			I_{CC2}		3.6	5.8	
	V_I = 0 V (ISO6761); V_I = VCC1 (ISO6761 with F suffix)		I_{CC1}		7.6	10.4	
			I_{CC2}		5.0	7.6	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		5.1	7.0	
			I_{CC2}		4.6	7.0	
		10 Mbps	I_{CC1}		5.8	7.8	
			I_{CC2}		7.4	10.2	
		50 Mbps	I_{CC1}		8.9	11.4	
			I_{CC2}		20.0	24.4	
ISO6762							

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V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - DC signal	V_I = VCC1 (ISO6762); V_I = 0 V (ISO6762 with F suffix)		I_{CC1}		2.7	4.1	mA
			I_{CC2}		3.3	5.2	
	V_I = 0 V (ISO6762); V_I = VCC1 (ISO6762 with F suffix)		I_{CC1}		6.9	9.7	
			I_{CC2}		5.6	8.3	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		5	7	
			I_{CC2}		4.7	7	
		10 Mbps	I_{CC1}		6.2	8.4	
			I_{CC2}		7	9.6	
		50 Mbps	I_{CC1}		11.7	14.6	
			I_{CC2}		17.2	21.1	
ISO6763							
Supply current - DC signal	V_I = V_{CCI} (ISO6763); V_I = 0 V (ISO6763 with F suffix)		I_{CC1}, I_{CC2}		3	4.7	mA
	V_I = 0 V (ISO6763); V_I = V_{CCI} (ISO6763 with F suffix)		I_{CC1}, I_{CC2}		6.3	9	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}, I_{CC2}		4.8	7	
		10 Mbps	I_{CC1}, I_{CC2}		6.6	9	
		50 Mbps	I_{CC1}, I_{CC2}		14.4	17.8	

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6.11 Electrical Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -2mA ; See Figure 7-1	V_{CCO} - 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 2mA ; See Figure 7-1			0.2	V
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0 V, V_{CM} = 1200 V; See Figure 7-3	100	150		kV/µs
C_i	Input Capacitance(2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2 MHz, V_{CC} = 3.3 V		2.8		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

6.12 Supply Current Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6760							
Supply current - DC signal	V_I = VCC1 (ISO6760); V_I = 0 V (ISO6760 with F suffix)		I_{CC1}		2.2	2.8	mA
			I_{CC2}		3.1	5.1	
	V_I = 0 V (ISO6760); V_I = VCC1 (ISO6760 with F suffix)		I_{CC1}		8.3	10.9	
			I_{CC2}		3.4	5.6	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		5.3	6.9	
			I_{CC2}		3.5	5.7	
		10 Mbps	I_{CC1}		5.3	7	
			I_{CC2}		5.9	8.5	
		50 Mbps	I_{CC1}		5.9	7.6	
			I_{CC2}		16.6	20.9	
ISO6761							
Supply current - DC signal	V_I = VCC1 (ISO6761); V_I = 0 V (ISO6761 with F suffix)		I_{CC1}		2.4	3.5	mA
			I_{CC2}		3.6	5.8	
	V_I = 0 V (ISO6761); V_I = VCC1 (ISO6761 with F suffix)		I_{CC1}		7.5	10.3	
			I_{CC2}		4.9	7.5	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		5	7	
			I_{CC2}		4.5	6.9	
		10 Mbps	I_{CC1}		5.5	7.5	
			I_{CC2}		6.5	9.2	
		50 Mbps	I_{CC1}		7.7	10	
			I_{CC2}		15.5	19.6	
ISO6762							

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V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - DC signal	V_I = VCC1 (ISO6762); V_I = 0 V (ISO6762 with F suffix)		I_{CC1}		2.7	4.1	mA
			I_{CC2}		3.3	5.2	
	V_I = 0 V (ISO6762); V_I = VCC1 (ISO6762 with F suffix)		I_{CC1}		6.9	9.6	
			I_{CC2}		5.6	8.2	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		4.9	6.9	
			I_{CC2}		4.6	6.9	
		10 Mbps	I_{CC1}		5.7	7.9	
			I_{CC2}		6.2	8.8	
		50 Mbps	I_{CC1}		9.6	12.4	
			I_{CC2}		13.5	17.1	
ISO6763							
Supply current - DC signal	V_I = V_{CCI} (ISO6763); V_I = 0 V (ISO6763 with F suffix)		I_{CC1}, I_{CC2}		3	4.6	mA
	V_I = 0 V (ISO6763); V_I = V_{CCI} (ISO6763 with F suffix)		I_{CC1}, I_{CC2}		6.2	8.9	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}, I_{CC2}		4.8	6.9	
		10 Mbps	I_{CC1}, I_{CC2}		6	8.4	
		50 Mbps	I_{CC1}, I_{CC2}		11.6	14.7	

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6.13 Electrical Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -1mA ; See Figure 7-1	V_{CCO} - 0.1			V
V_{OL}	Low-level output voltage	I_{OL} = 1mA ; See Figure 7-1			0.1	V
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0 V, V_{CM} = 1200 V; See Figure 7-3	100	150		kV/µs
C_i	Input Capacitance(2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2 MHz, V_{CC} = 2.5 V		2.8		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

6.14 Supply Current Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6760							
Supply current - DC signal	V_I = VCC1 (ISO6760); V_I = 0 V (ISO6760 with F suffix)		I_{CC1}		2.2	2.8	mA
			I_{CC2}		3.1	5.1	
	V_I = 0 V (ISO6760); V_I = VCC1 (ISO6760 with F suffix)		I_{CC1}		8.3	10.8	
			I_{CC2}		3.4	5.6	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		5.2	6.8	
			I_{CC2}		3.5	5.6	
		10 Mbps	I_{CC1}		5.3	6.9	
			I_{CC2}		5.3	7.7	
		50 Mbps	I_{CC1}		5.7	7.5	
			I_{CC2}		13.2	16.9	
ISO6761							
Supply current - DC signal	V_I = VCC1 (ISO6761); V_I = 0 V (ISO6761 with F suffix)		I_{CC1}		2.4	3.5	mA
			I_{CC2}		3.6	5.7	
	V_I = 0 V (ISO6761); V_I = VCC1 (ISO6761 with F suffix)		I_{CC1}		7.5	10.3	
			I_{CC2}		4.9	7.5	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		5	6.9	
			I_{CC2}		4.4	6.8	
		10 Mbps	I_{CC1}		5.3	7.3	
			I_{CC2}		5.9	8.5	
		50 Mbps	I_{CC1}		7	9.3	
			I_{CC2}		12.7	16.3	
ISO6762							

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V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - DC signal	V_I = VCC1 (ISO6762); V_I = 0 V (ISO6762 with F suffix)		I_{CC1}		2.7	4	mA
			I_{CC2}		3.3	5.2	
	V_I = 0 V (ISO6762); V_I = VCC1 (ISO6762 with F suffix)		I_{CC1}		6.9	9.6	
			I_{CC2}		5.6	8.2	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		4.9	6.9	
			I_{CC2}		4.6	6.8	
		10 Mbps	I_{CC1}		5.5	7.6	
			I_{CC2}		5.8	8.2	
		50 Mbps	I_{CC1}		8.4	11	
			I_{CC2}		11.2	14.5	
ISO6763							
Supply current - DC signal	V_I = V_{CCI} (ISO6763); V_I = 0 V (ISO6763 with F suffix)		I_{CC1}, I_{CC2}		3	4.6	mA
	V_I = 0 V (ISO6763); V_I = V_{CCI} (ISO6763 with F suffix)		I_{CC1}, I_{CC2}		6.2	8.9	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}, I_{CC2}		4.7	6.9	
		10 Mbps	I_{CC1}, I_{CC2}		5.6	7.9	
		50 Mbps	I_{CC1}, I_{CC2}		9.8	12.7	

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6.15 Electrical Characteristics—1.8-V Supply

V_{CC1} = V_{CC2} = 1.8 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -1mA ; See Figure 7-1	V_{CCO} - 0.1			V
V_{OL}	Low-level output voltage	I_{OL} = 1mA ; See Figure 7-1			0.1	V
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0 V, V_{CM} = 1200 V; See Figure 7-3	50	75		kV/µs
C_i	Input Capacitance(2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2 MHz, V_{CC} = 1.8 V		2.8		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

6.16 Supply Current Characteristics—1.8-V Supply

V_{CC1} = V_{CC2} = 1.8 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6760							
Supply current - DC signal	V_I = VCC1 (ISO6760); V_I = 0 V (ISO6760 with F suffix)		I_{CC1}		1.5	2.1	mA
			I_{CC2}		3	5.1	
	V_I = 0 V (ISO6760); V_I = VCC1 (ISO6760 with F suffix)		I_{CC1}		7.3	10.3	
			I_{CC2}		3.3	5.6	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		4.4	6.2	
			I_{CC2}		3.3	5.5	
		10 Mbps	I_{CC1}		4.5	6.3	
			I_{CC2}		4.6	7	
		50 Mbps	I_{CC1}		4.8	6.7	
			I_{CC2}		10.1	13	
ISO6761							
Supply current - DC signal	V_I = VCC1 (ISO6761); V_I = 0 V (ISO6761 with F suffix)		I_{CC1}		1.8	2.9	mA
			I_{CC2}		3.4	5.7	
	V_I = 0 V (ISO6761); V_I = VCC1 (ISO6761 with F suffix)		I_{CC1}		6.7	9.8	
			I_{CC2}		4.6	7.4	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		4.3	6.4	
			I_{CC2}		4.1	6.7	
		10 Mbps	I_{CC1}		4.6	6.7	
			I_{CC2}		5.2	7.9	
		50 Mbps	I_{CC1}		5.8	8.1	
			I_{CC2}		9.9	13	
ISO6762							

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V_{CC1} = V_{CC2} = 1.8 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - DC signal	V_I = VCC1 (ISO6762); V_I = 0 V (ISO6762 with F suffix)		I_{CC1}		2.2	3.6	mA
			I_{CC2}		3	5	
	V_I = 0 V (ISO6762); V_I = VCC1 (ISO6762 with F suffix)		I_{CC1}		6.2	9.2	
			I_{CC2}		5.1	8	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		4.3	6.5	
			I_{CC2}		4.2	6.6	
		10 Mbps	I_{CC1}		4.7	7	
			I_{CC2}		5	7.6	
		50 Mbps	I_{CC1}		6.8	9.3	
			I_{CC2}		8.9	11.8	
ISO6763							
Supply current - DC signal	V_I = V_{CCI} (ISO6763); V_I = 0 V (ISO6763 with F suffix)		I_{CC1}, I_{CC2}		2.6	4.3	mA
	V_I = 0 V (ISO6763); V_I = V_{CCI} (ISO6763 with F suffix)		I_{CC1}, I_{CC2}		5.7	8.6	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}, I_{CC2}		4.2	6.5	
		10 Mbps	I_{CC1}, I_{CC2}		4.9	7.3	
		50 Mbps	I_{CC1}, I_{CC2}		7.9	10.5	

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6.17 Switching Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO676x						
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 7-1		11	18	ns
PWD	Pulse width distortion[(1)] $\lvert t_{PHL} – t_{PLH} \rvert$				7	ns
$t_{sk(o)}$	Channel-to-channel output skew time[(2)]	Same-direction channels			6	ns
$t_{sk(pp)}$	Part-to-part skew time[(3)]				6	ns
t_r	Output signal rise time	See Figure 7-1			4.5	ns
t_f	Output signal fall time				4.5	ns
t_{PU}	Time from UVLO to valid output data				300	µs
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.2V. See Figure 7-2		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 50 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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6.18 Switching Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO676x						
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 7-1		11	18	ns
PWD	Pulse width distortion[(1)] $\lvert t_{PHL} – t_{PLH} \rvert$				7	ns
$t_{sk(o)}$	Channel-to-channel output skew time[(2)]	Same-direction channels			6	ns
$t_{sk(pp)}$	Part-to-part skew time[(3)]				7	ns
t_r	Output signal rise time	See Figure 7-1			3.2	ns
t_f	Output signal fall time				3.2	ns
t_{PU}	Time from UVLO to valid output data				300	µs
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.2V. See Figure 7-2		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 50 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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6.19 Switching Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO676x						
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 7-1		12	20.5	ns
PWD	Pulse width distortion[(1)] $\lvert t_{PHL} – t_{PLH} \rvert$				7.1	ns
$t_{sk(o)}$	Channel-to-channel output skew time[(2)]	Same-direction channels			6	ns
$t_{sk(pp)}$	Part-to-part skew time[(3)]				7	ns
t_r	Output signal rise time	See Figure 7-1			4	ns
t_f	Output signal fall time				4	ns
t_{PU}	Time from UVLO to valid output data				300	µs
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.2V. See Figure 7-2		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 50 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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6.20 Switching Characteristics—1.8-V Supply

V_{CC1} = V_{CC2} = 1.8 V ±5% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO676x						
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 7-1		15	24	ns
PWD	Pulse width distortion $\lvert t_{PHL} – t_{PLH} \rvert$				8.2	ns
$t_{sk(o)}$	Channel-to-channel output skew time(1)	Same-direction channels			6	ns
$t_{sk(pp)}$	Part-to-part skew time(2)				8.8	ns
t_r	Output signal rise time	See Figure 7-1			4.7	ns
t_f	Output signal fall time				4.7	ns
t_{PU}	Time from UVLO to valid output data				300	µs
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.2V. See Figure 7-2		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 50 Mbps		1		ns

(1) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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6.21 Insulation Characteristics Curves

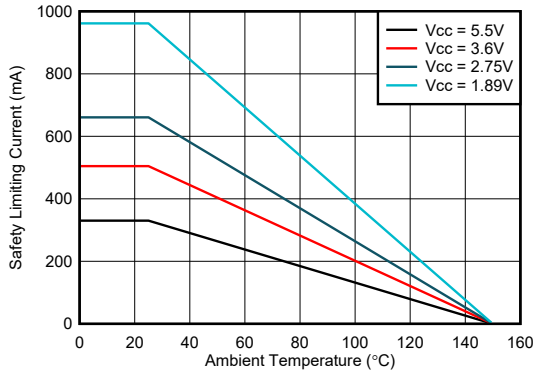

Figure 6-1. Thermal Derating Curve for Safety Limiting Current for DW-16 Package

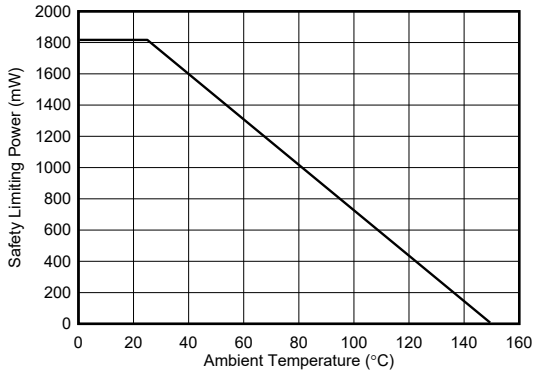

Figure 6-2. Thermal Derating Curve for Safety Limiting Power for DW-16 Package

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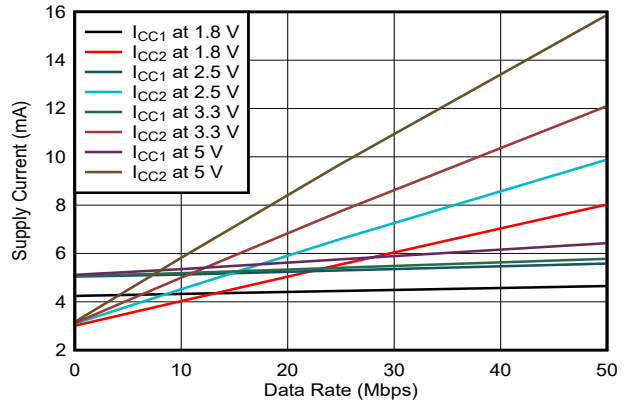
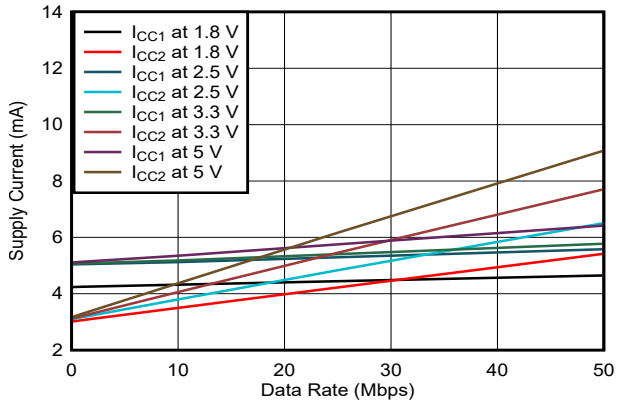
6.22 Typical Characteristics



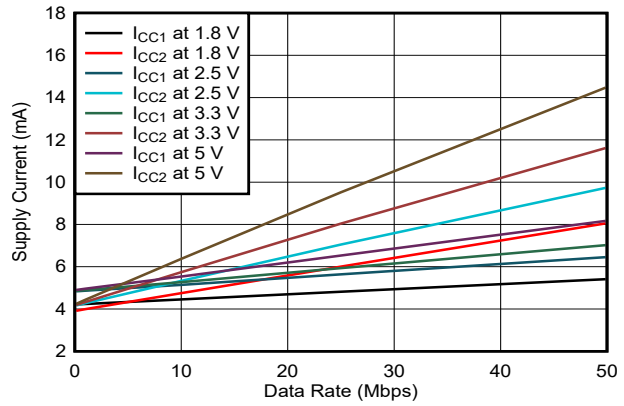
T_A = 25°C C_L = 15 pF

Figure 6-3. ISO6760-Q1 Supply Current vs Data Rate (With 15-pF Load)



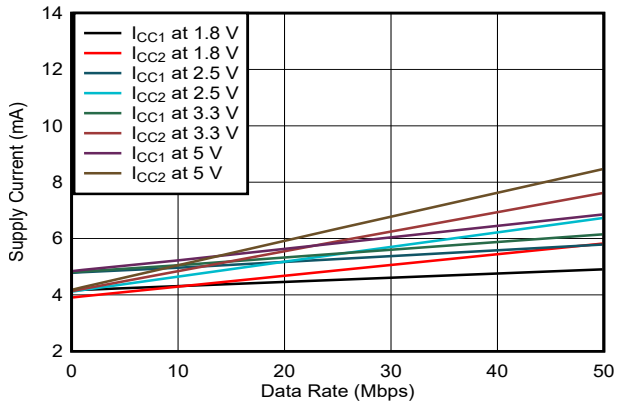
T_A = 25°C C_L = No Load

Figure 6-4. ISO6760-Q1 Supply Current vs Data Rate (With No Load)



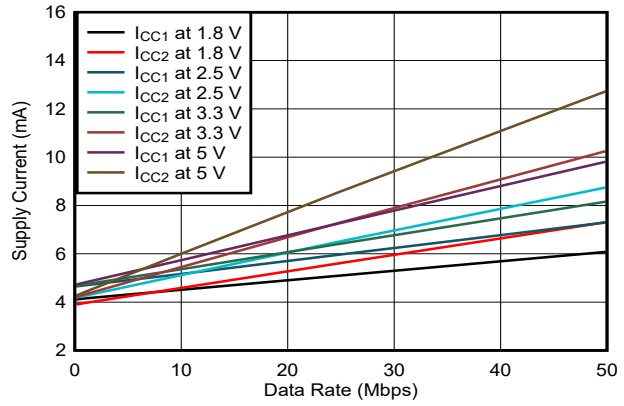
T_A = 25°C C_L = 15 pF

Figure 6-5. ISO6761-Q1 Supply Current vs Data Rate (With 15-pF Load)



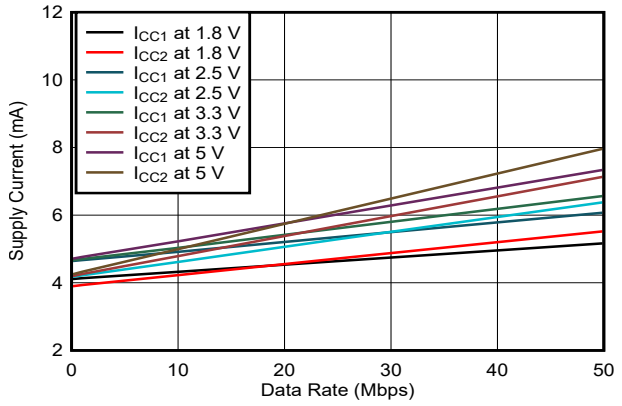
T_A = 25°C C_L = No Load

Figure 6-6. ISO6761-Q1 Supply Current vs Data Rate (With No Load)



T_A = 25°C C_L = 15 pF

Figure 6-7. ISO6762-Q1 Supply Current vs Data Rate (With 15-pF Load)



T_A = 25°C C_L = No Load

Figure 6-8. ISO6762-Q1 Supply Current vs Data Rate (With No Load)

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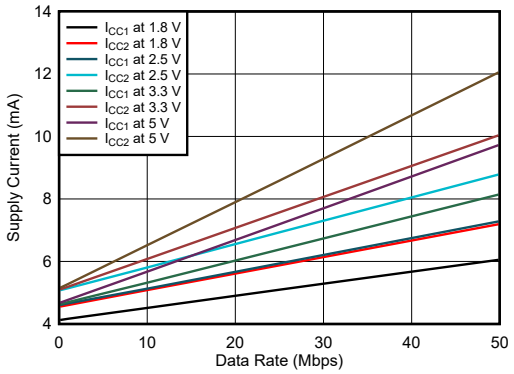
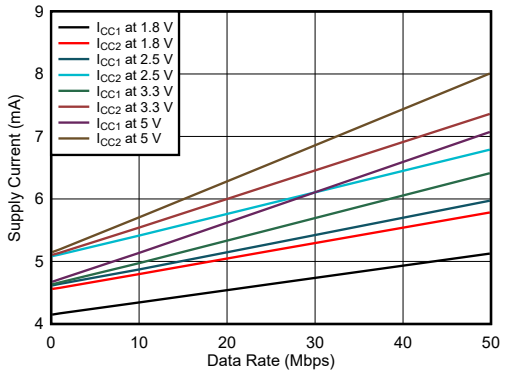


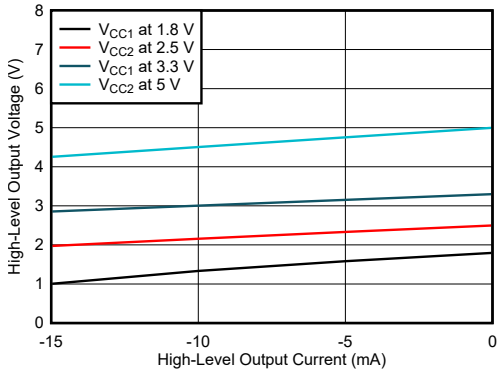
T_A = 25°C C_L = 15 pF

Figure 6-9. ISO6763-Q1 Supply Current vs Data Rate (With 15-pF Load)



T_A = 25°C C_L = No Load

Figure 6-10. ISO6763-Q1 Supply Current vs Data Rate (With No Load)



T_A = 25°C

Figure 6-11. High-Level Output Voltage vs High-level Output Current

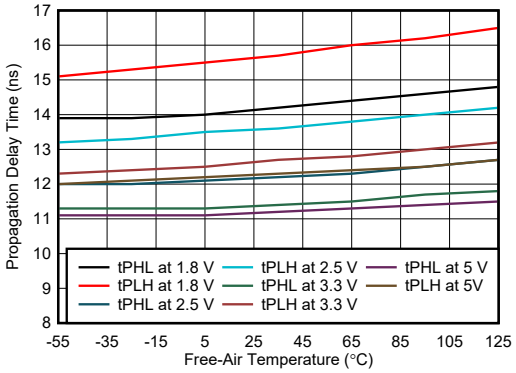


Figure 6-12. Propagation Delay Time vs Free-Air Temperature

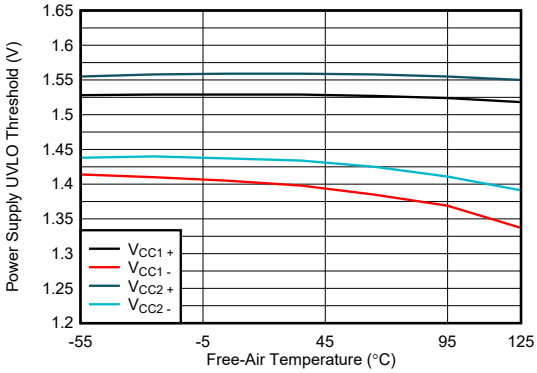
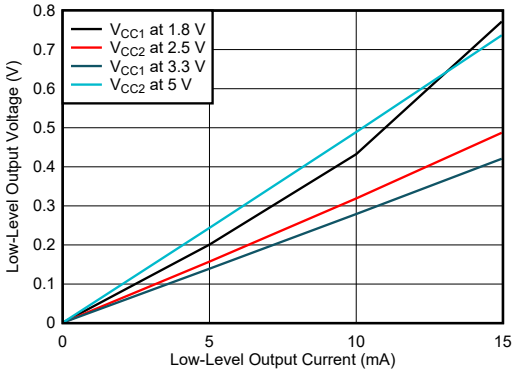


Figure 6-13. Power Supply Undervoltage Threshold vs Free-Air Temperature



T_A = 25°C

Figure 6-14. Low-Level Output Voltage vs Low-Level Output Current

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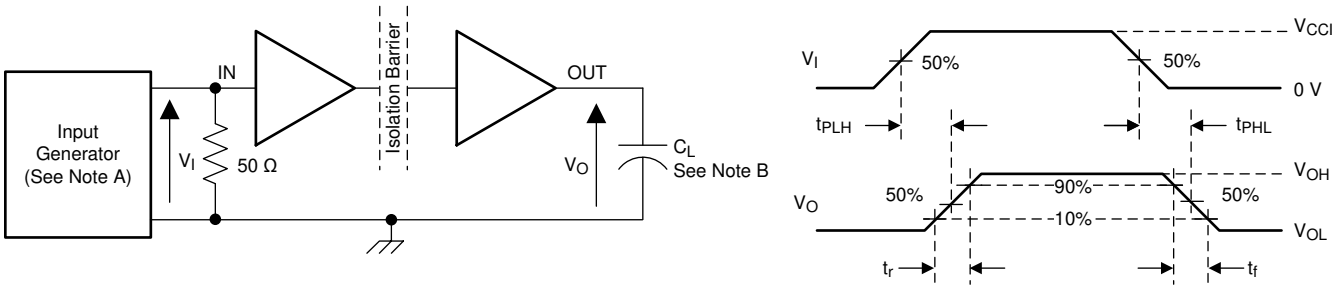
7 Parameter Measurement Information



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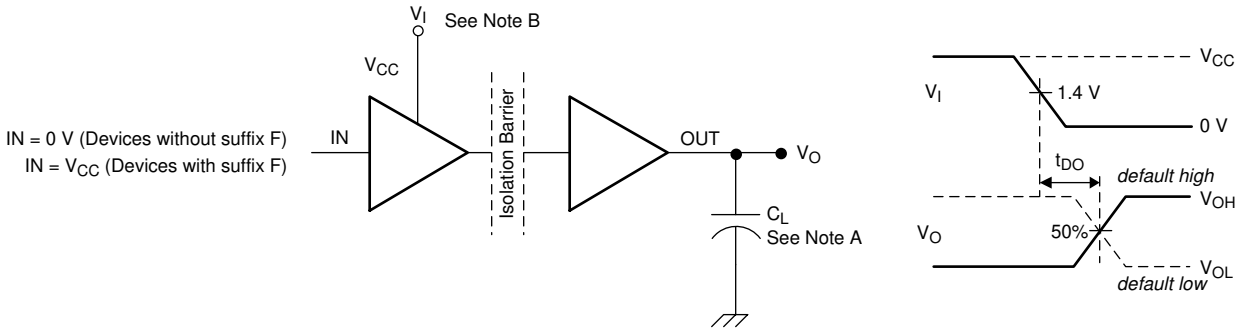
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

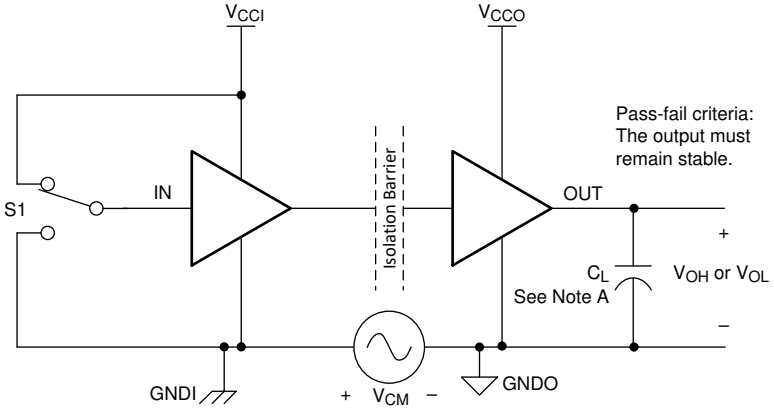
Figure 7-1. Switching Characteristics Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. Power Supply Ramp Rate = 10 mV/ns

Figure 7-2. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. For optimized CMTI performance, a 0.1 µF + 1 µF decoupling capacitor should be placed close to V_{CC1} and V_{CC2}. Please see Section 11.2 for capacitor placement details. A recommended 0.1µF capacitor is LLL185R71A104MA11L (CAP CER 0.1UF 10V X7R 0306 - LW Reversed Low ESL Chip Ceramic Capacitors) or equivalent.

Figure 7-3. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The ISO676x-Q1 family of devices have an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. If the ENx pin is low then the output goes to high impedance. The ISO676x-Q1 devices also incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 8-1, shows a functional block diagram of a typical channel.

8.2 Functional Block Diagram

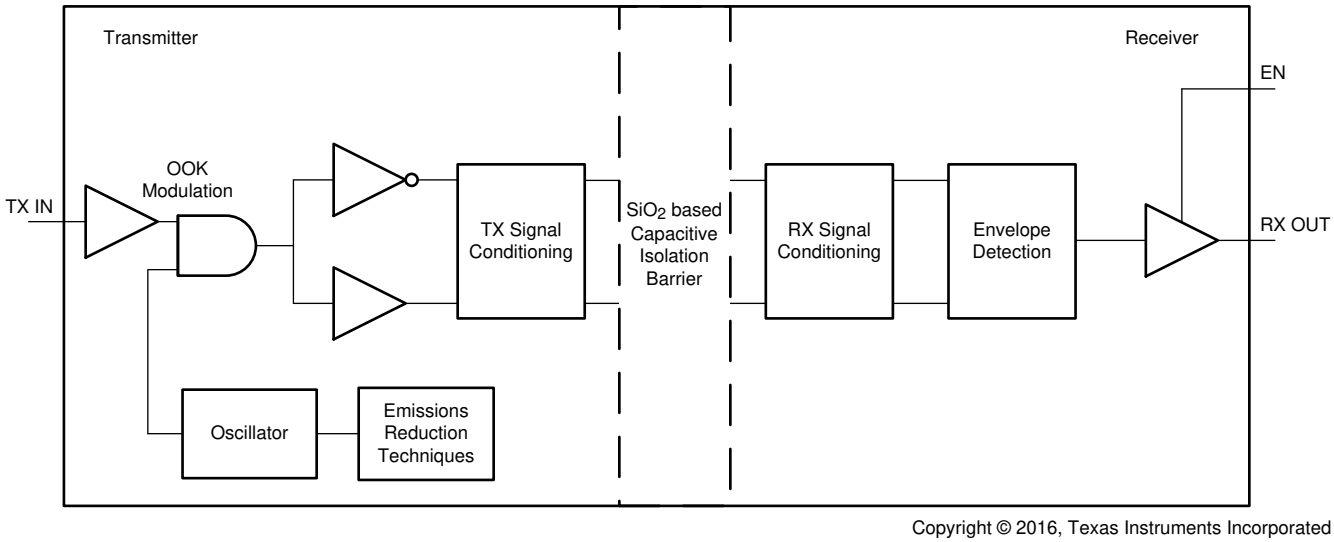


Figure 8-1. Conceptual Block Diagram of a Digital Capacitive Isolator

Figure 8-2 shows a conceptual detail of how the ON-OFF keying scheme works.

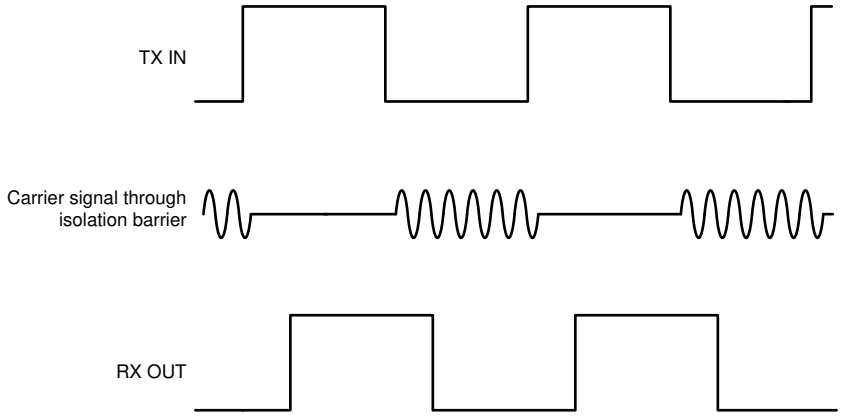


Figure 8-2. On-Off Keying (OOK) Based Modulation Scheme

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8.3 Feature Description

Table 8-1 provides an overview of the device features.

Table 8-1. Device Features

PART NUMBER	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT	PACKAGE	RATED ISOLATION[(1)]
ISO6760-Q1	6 Forward, 0 Reverse	50 Mbps	High	DW-16	5000 V_{RMS} / 7071 V_{PK}
ISO6760F-Q1	6 Forward, 0 Reverse	50 Mbps	Low	DW-16	5000 V_{RMS} / 7071 V_{PK}
ISO6761-Q1	5 Forward, 1 Reverse	50 Mbps	High	DW-16	5000 V_{RMS} / 7071 V_{PK}
ISO6761F-Q1	5 Forward, 1 Reverse	50 Mbps	Low	DW-16	5000 V_{RMS} / 7071 V_{PK}
ISO6762-Q1	4 Forward, 2 Reverse	50 Mbps	High	DW-16	5000 V_{RMS} / 7071 V_{PK}
ISO6762F-Q1	4 Forward, 2 Reverse	50 Mbps	Low	DW-16	5000 V_{RMS} / 7071 V_{PK}
ISO6763-Q1	3 Forward, 3 Reverse	50 Mbps	High	DW-16	5000 V_{RMS} / 7071 V_{PK}
ISO6763F-Q1	3 Forward, 3 Reverse	50 Mbps	Low	DW-16	5000 V_{RMS} / 7071 V_{PK}

(1) See Safety-Related Certifications for detailed isolation ratings.

8.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 25. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO676x-Q1 family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

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8.4 Device Functional Modes

Table 8-2 lists the functional modes for the ISO676x-Q1 devices.

Table 8-2. Function Table

V_{CCI} (1)	V_{CCO}	INPUT (INx) (3)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H	Normal Operation: A channel output assumes the logic state of its input.
		L	L	
		Open	Default	Default mode: When INx is open, the corresponding channel output goes to its default logic state. Default is *High* for ISO676x-Q1 and *Low* for ISO676x-Q1 with F suffix.
PD	PU	X	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is *High* for ISO676x-Q1 and *Low* for ISO676x-Q1 with F suffix. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined(2). When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input.

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ 1.71 V); PD = Powered down (V_{CC} ≤ 1.05 V); X = Irrelevant; H = High level; L = Low level ; Z = High Impedance
(2) The outputs are in undetermined state when 1.05 V < V_{CCI}, V_{CCO} < 1.71 V and 1.89 V < V_{CCI}, V_{CCO} < 2.25 V
(3) A strongly driven input signal can weakly power the floating V_{CC} through an internal protection diode and cause undetermined output

8.4.1 Device I/O Schematics

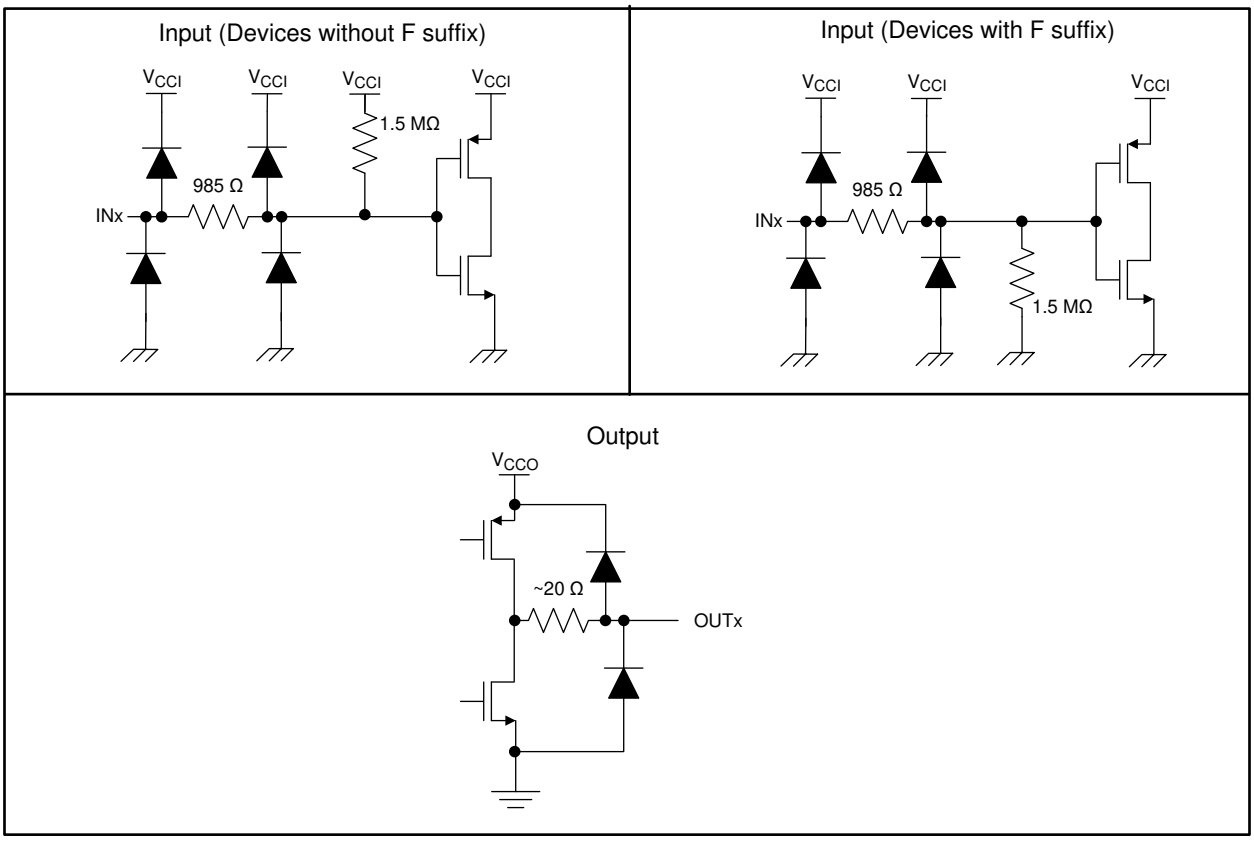

Figure 8-3. Device I/O Schematics

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO676x-Q1 devices are high-performance, six-channel digital isolators. The ISO676x-Q1 devices use single-ended CMOS-logic switching technology. The supply voltage range is from 1.71 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. Since an isolation barrier separates the two sides, each side can be sourced independently with any voltage within recommended operating conditions. As an example, it is possible to supply ISO676x-Q1 V_{CC1} with 3.3 V (which is within 1.71 V to 5.5 V) and V_{CC2} with 5V (which is also within 1.71 V to 5.5 V). You can use the digital isolator as a logic-level translator in addition to providing isolation. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, MCU or FPGA), and a data converter or a line transceiver, regardless of the interface type or standard.

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9.2 Typical Application

Figure 9-1 shows the isolated serial-peripheral interface (SPI) and controller-area network (CAN) interface implementation.

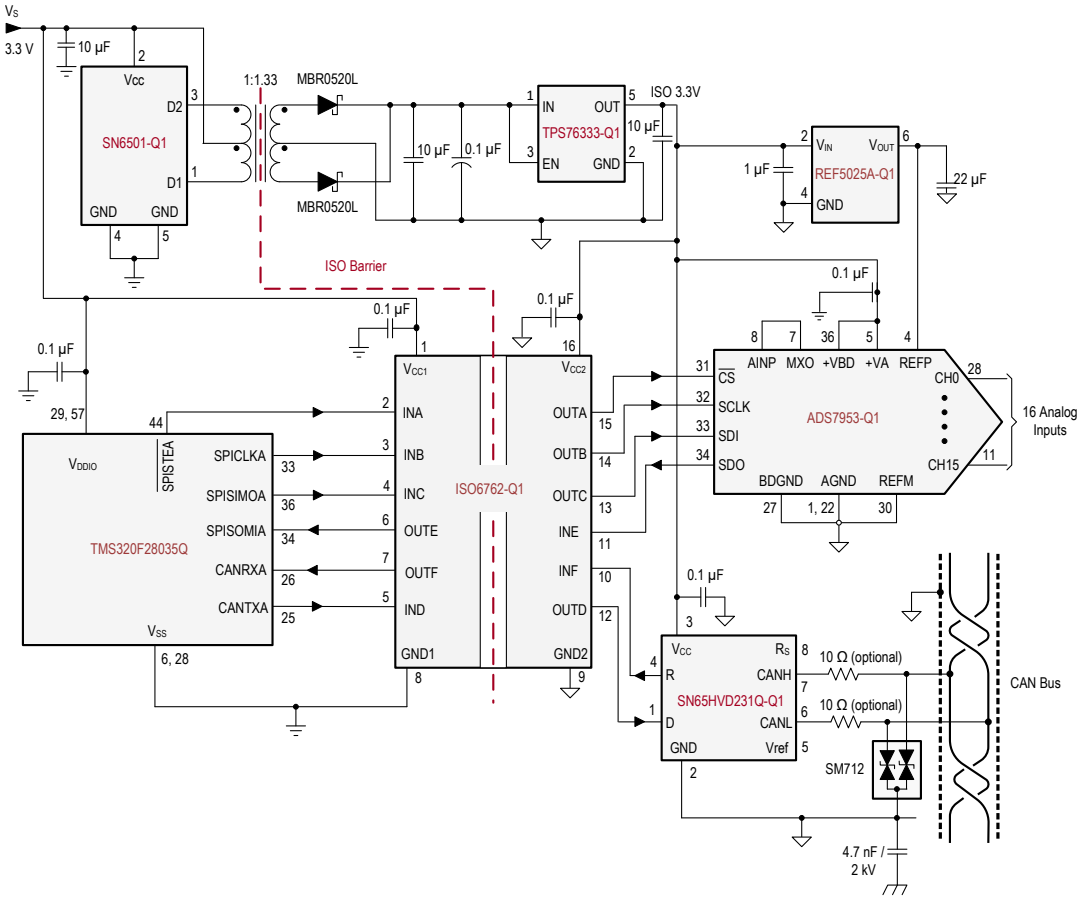

Figure 9-1. Isolated SPI and CAN Interface

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9.2.1 Design Requirements

To design with these devices, use the parameters listed in Table 9-1.

Table 9-1. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	1.71 V to 1.89 V and 2.25 V to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO676x-Q1 family of devices only require two external bypass capacitors to operate.

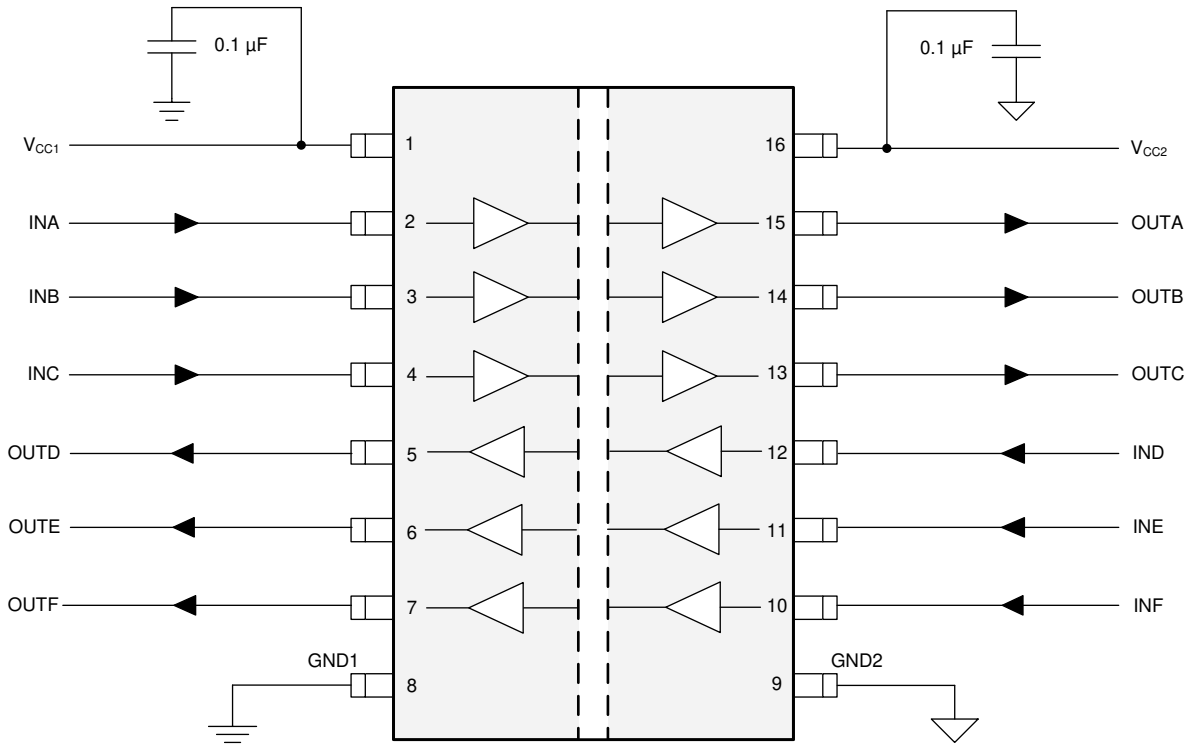

Figure 9-2. Typical ISO676x-Q1 Circuit Hook-up

9.2.3 Application Curve

The following typical eye diagrams of the ISO676x-Q1 family of devices indicates low jitter and wide open eye at the maximum data rate of 50 Mbps.

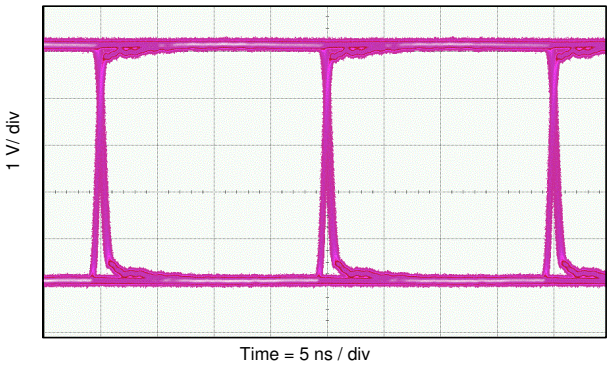

Figure 9-3. Eye Diagram at 50 Mbps PRBS 2^{16} – 1, 5 V and 25°C

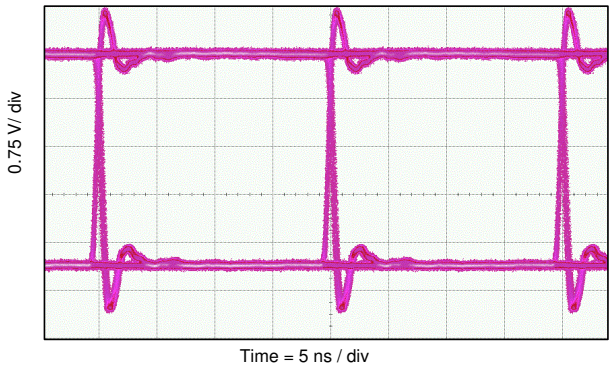

Figure 9-4. Eye Diagram at 50 Mbps PRBS 2^{16} – 1, 3.3 V and 25°C

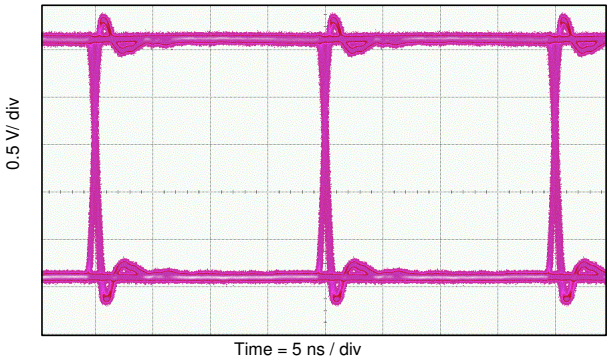

Figure 9-5. Eye Diagram at 50 Mbps PRBS 2^{16} – 1, 2.5 V and 25°C

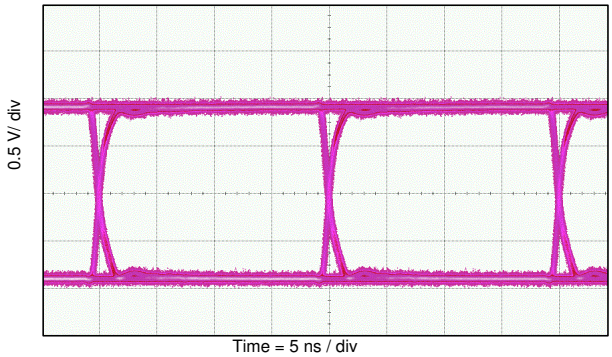

Figure 9-6. Eye Diagram at 50 Mbps PRBS 2^{16} – 1, 1.8 V and 25°C

9.2.3.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See Figure 9-7 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that's 20% higher than the specified value.

Figure 9-8 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1500 V_{RMS} with a lifetime of 36 years. Other factors, such as package size, pollution degree, material group, etc. can further limit the working voltage of the component. The working voltage of DW-16 package is specified upto 1500 V_{RMS}. At the lower working voltages, the corresponding insulation lifetime is much longer than 36 years.

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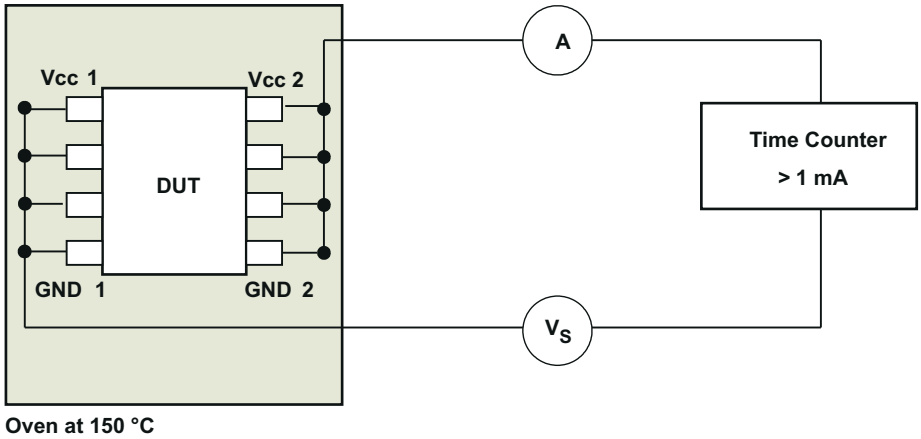

Figure 9-7. Test Setup for Insulation Lifetime Measurement

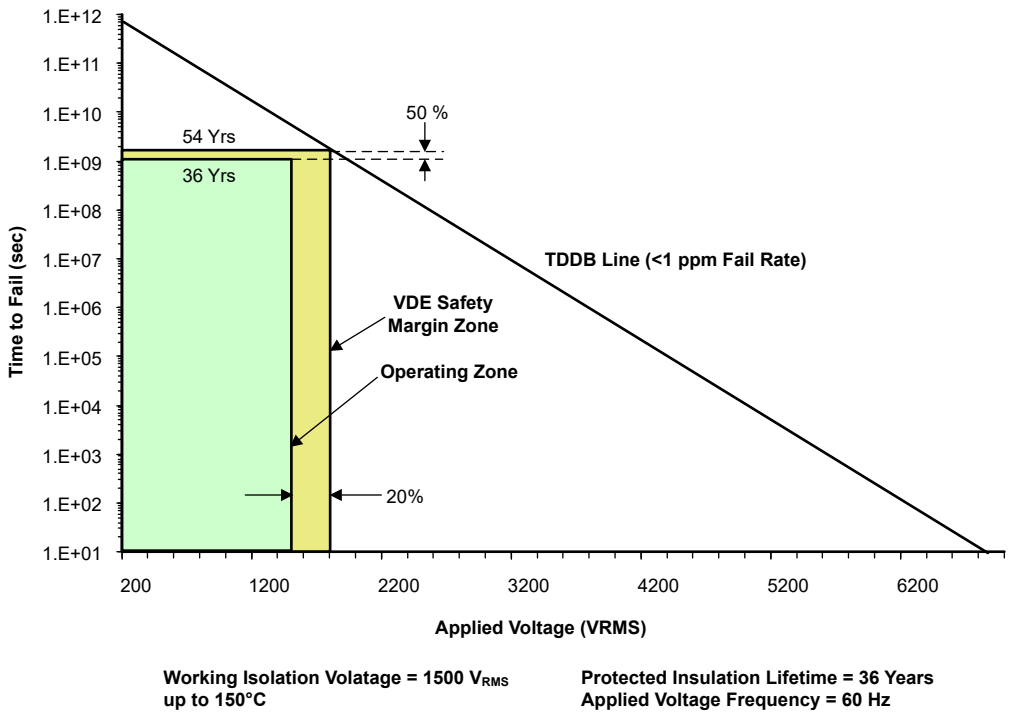

Figure 9-8. Insulation Lifetime Projection Data

10 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver. For automotive applications, please use SN6501-Q1 or SN6505B-Q1. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501-Q1 Transformer Driver for Isolated Power Supplies* or *SN6505B-Q1 Automotive, low-noise, 1-A, 420-kHz transformer driver with soft start for isolated power supplies*.

11 Layout

11.1 Layout Guidelines

A minimum of two layers is required to accomplish a low EMI PCB design. To further improve EMI, a four layer board can be used (see Figure 11-2). Layer stacking for a four layer board should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide*.

11.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit boards. This PCB is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and self-extinguishing flammability-characteristics.

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11.2 Layout Example

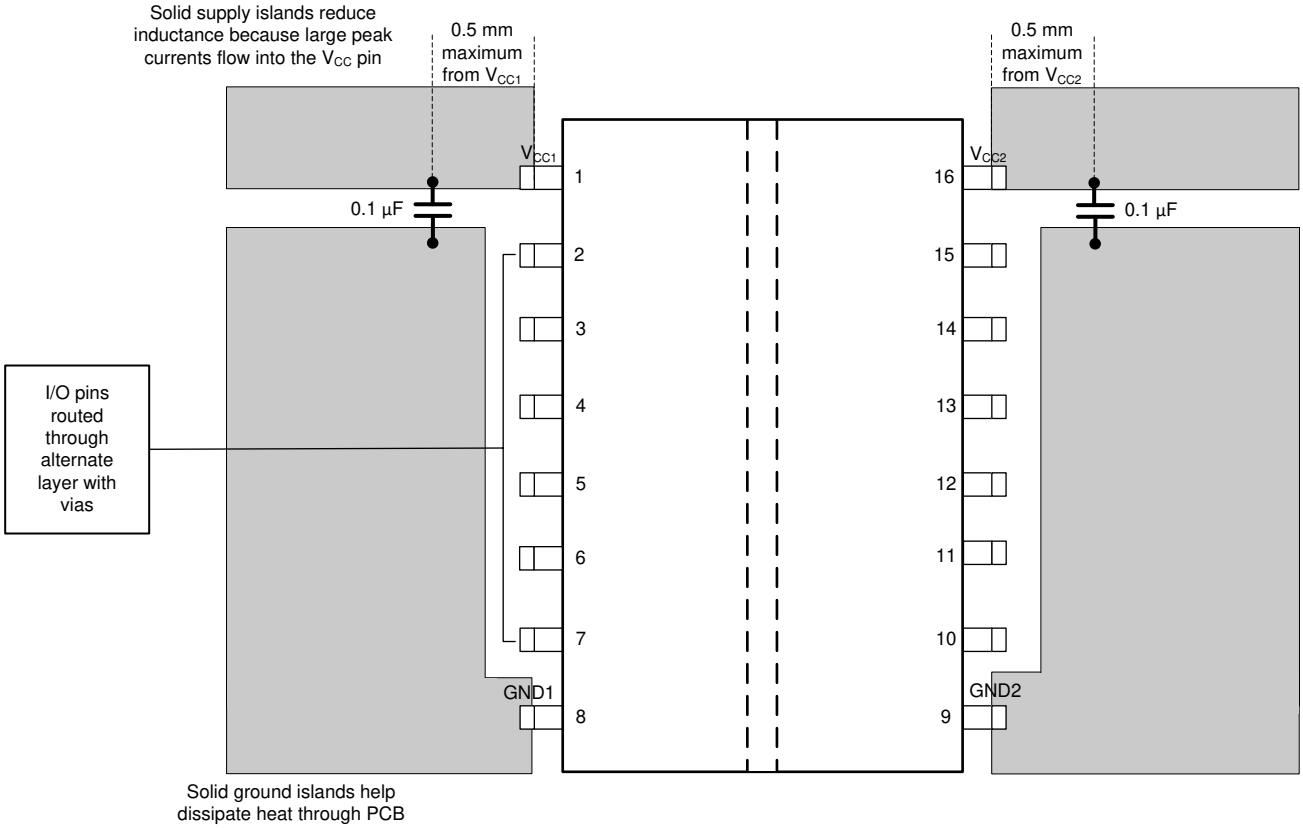

Figure 11-1. Layout Example

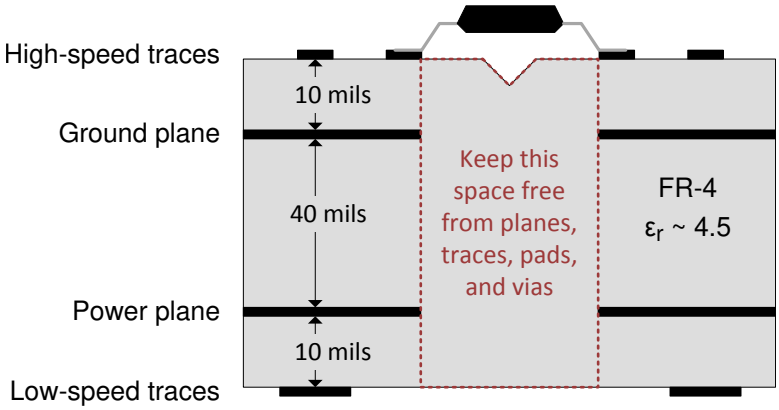

Figure 11-2. Four Layer Board Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*
- Texas Instruments, *How to use isolation to improve ESD, EFT, and Surge immunity in industrial systems* application report
- Texas Instruments, *SN6505x-Q1 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies*
- Texas Instruments, *TCAN1044-Q1 Automotive Fault-Protected CAN FD Transceiver*
- Texas Instruments, *TPS763xx-Q1 Low-Power, 150-mA, Low-Dropout Linear Regulators* data sheet
- Texas Instruments, *TMS320F2803x Piccolo™ Microcontrollers* data sheet

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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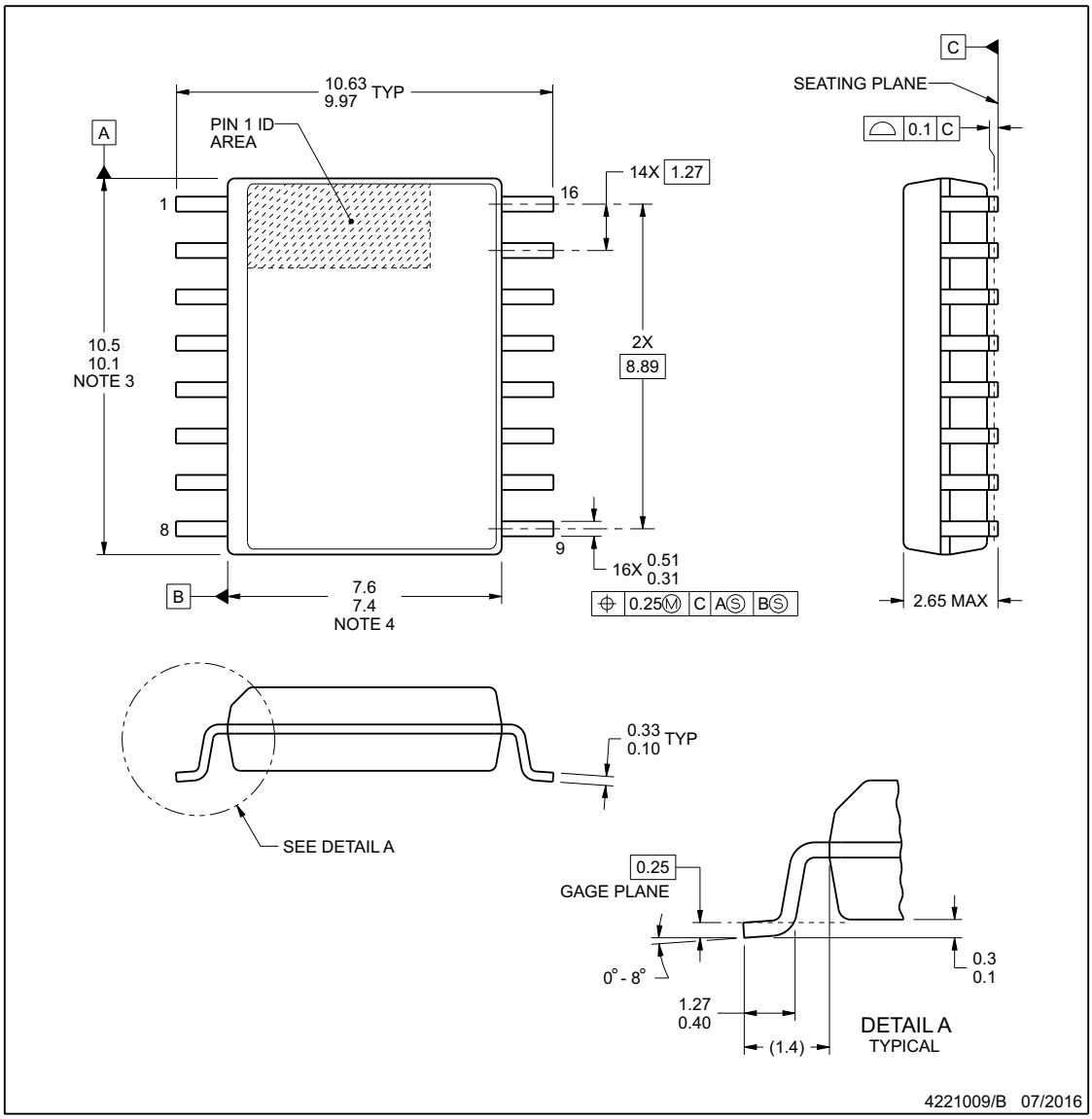
PACKAGE OUTLINE

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

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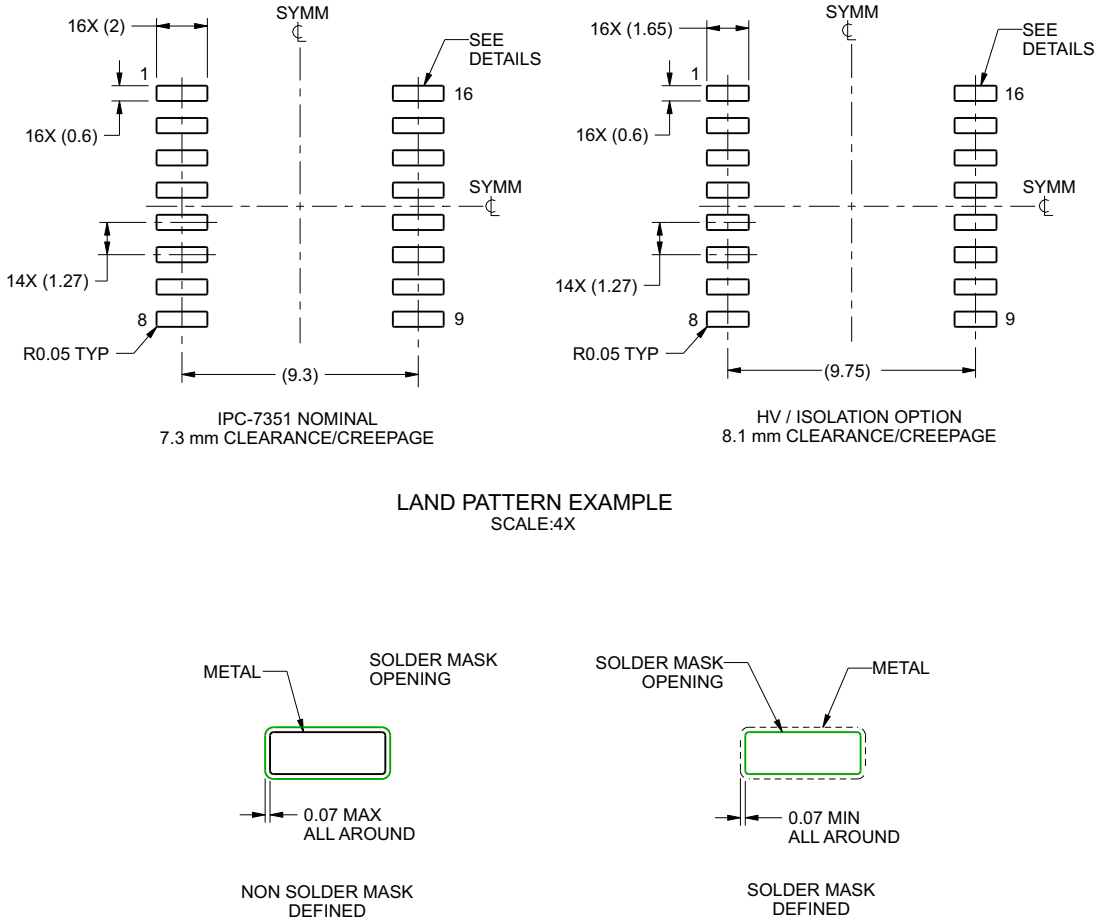
EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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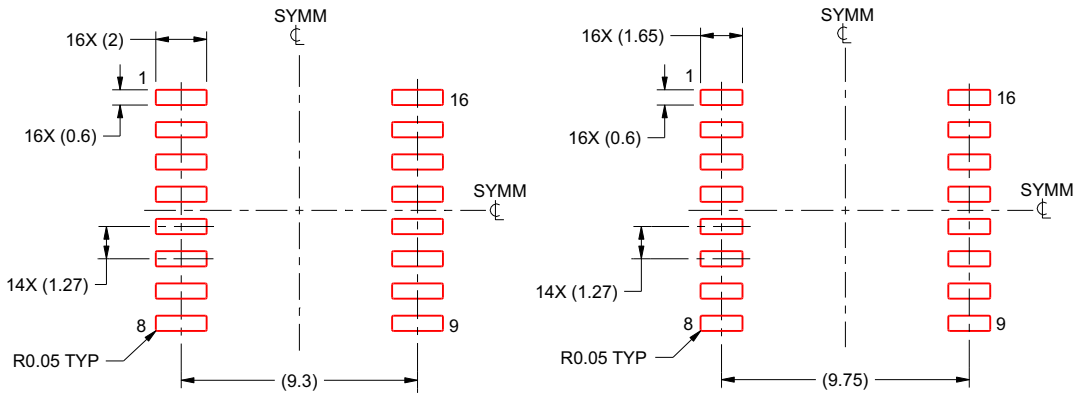
EXAMPLE STENCIL DESIGN

DW0016B **SOIC - 2.65 mm max height**

SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO6760FQDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6760F
ISO6760FQDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6760F
ISO6760FQDWRQ1.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISO6760QDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6760
ISO6760QDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6760
ISO6760QDWRQ1.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISO6761FQDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6761F
ISO6761FQDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6761F
ISO6761FQDWRQ1.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISO6761QDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6761
ISO6761QDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6761
ISO6761QDWRQ1.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISO6762FQDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6762F
ISO6762FQDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6762F
ISO6762FQDWRQ1.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISO6762QDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6762
ISO6762QDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6762
ISO6762QDWRQ1.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISO6763FQDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6763F
ISO6763FQDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6763F
ISO6763FQDWRQ1.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISO6763QDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6763
ISO6763QDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6763
ISO6763QDWRQ1.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF ISO6760-Q1, ISO6761-Q1, ISO6762-Q1, ISO6763-Q1 :

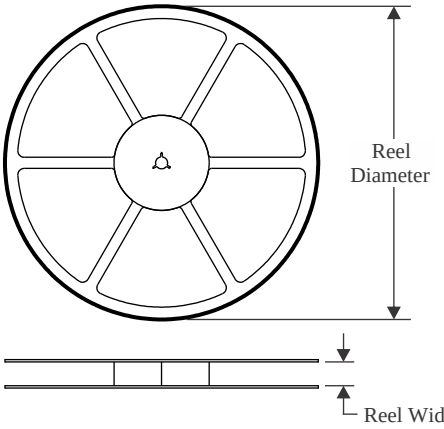
- Catalog : ISO6760, ISO6761, ISO6762, ISO6763

NOTE: Qualified Version Definitions:

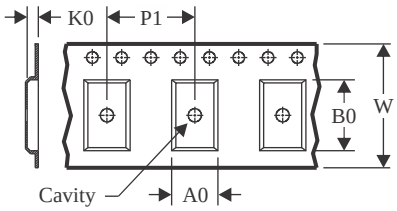
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

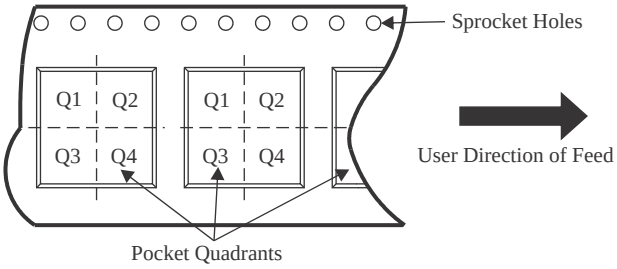


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

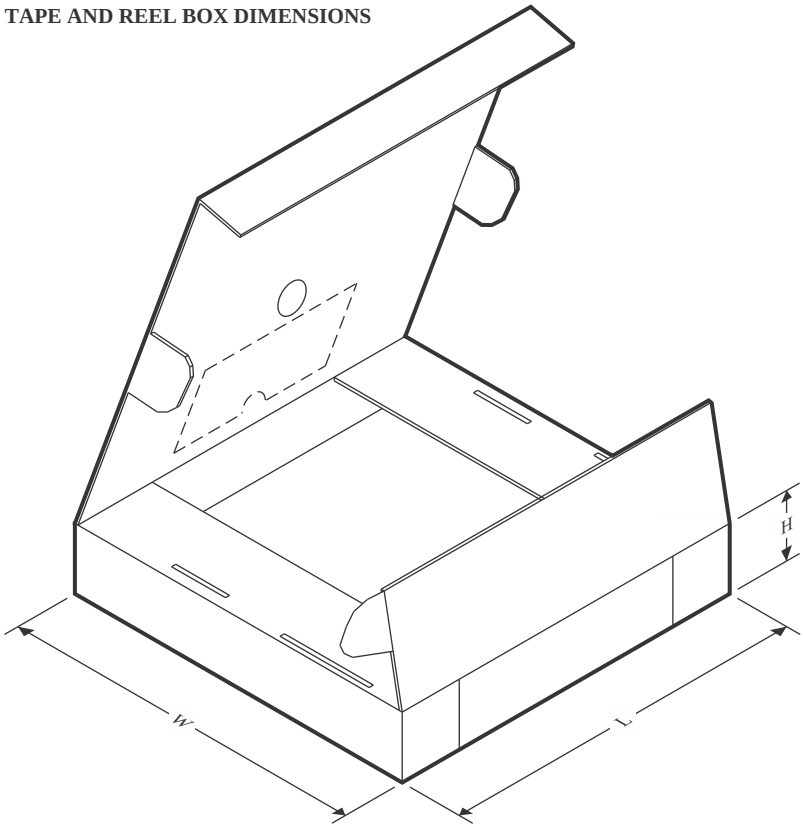
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO6760FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6760QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6761FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6761QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6762FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6762QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6763FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6763QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO6760FQDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6760QDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6761FQDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6761QDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6762FQDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6762QDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6763FQDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6763QDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

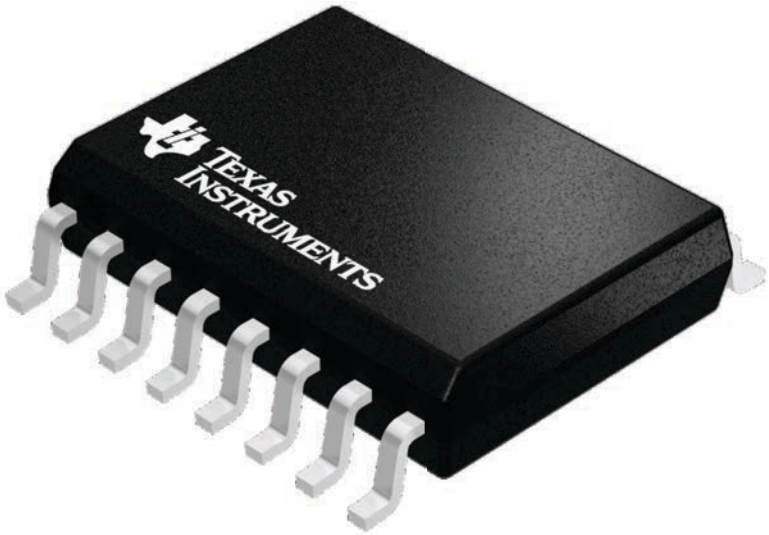
DW 16

SOIC - 2.65 mm max height

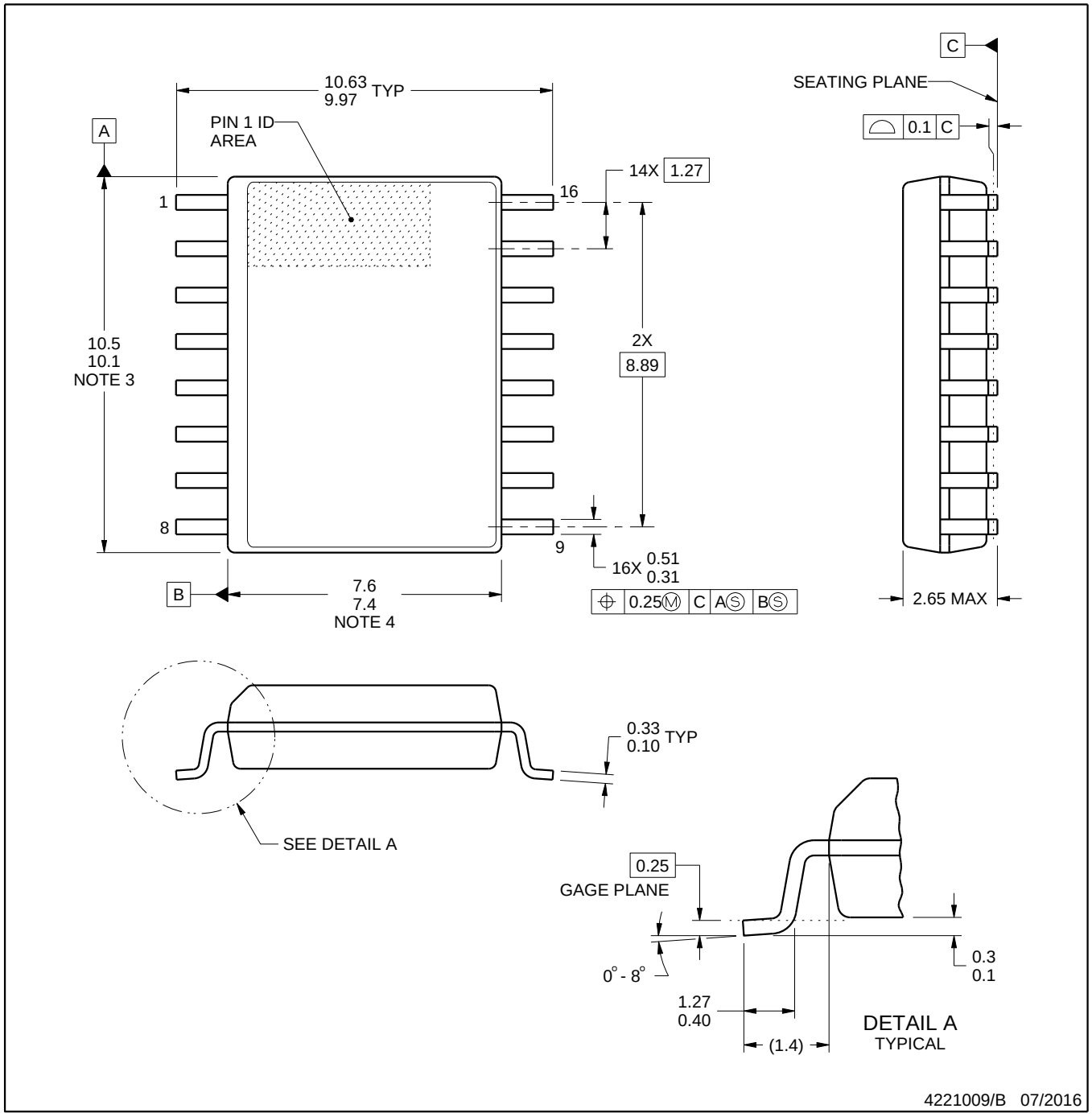
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
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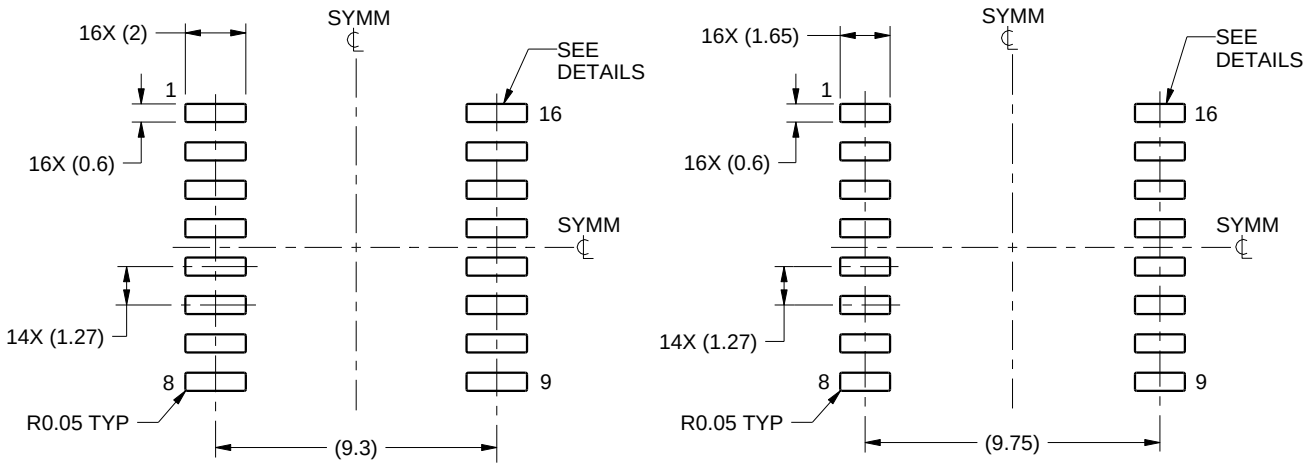
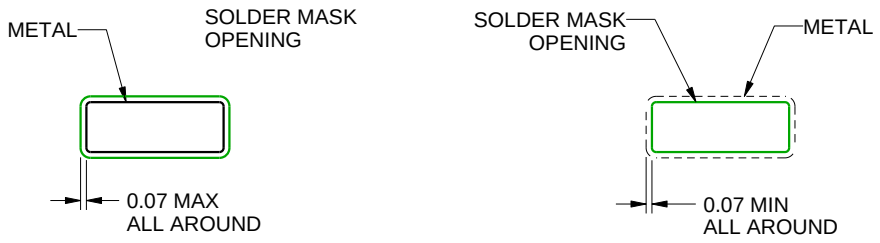
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

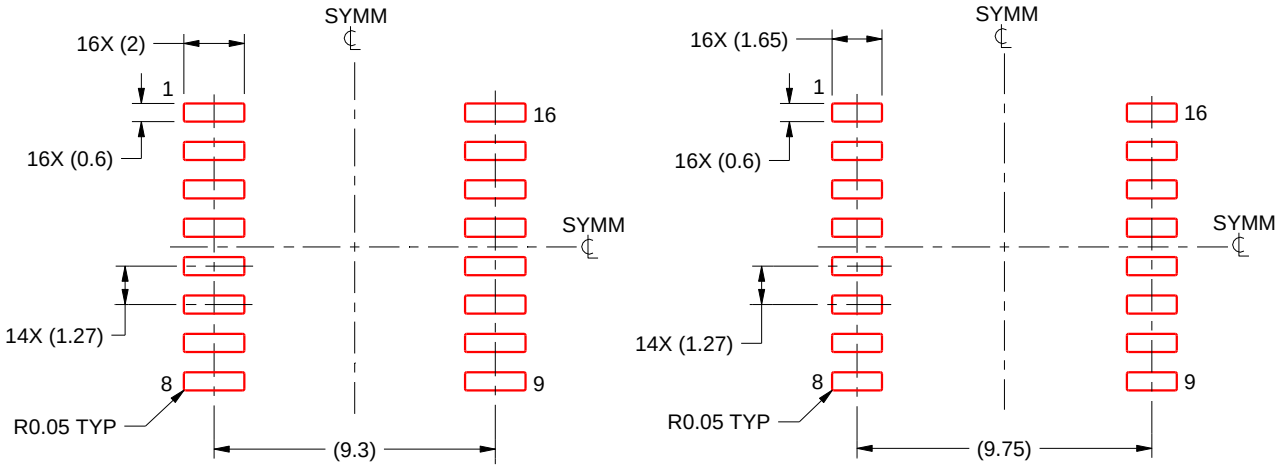
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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