

# ISO674x General-Purpose Reinforced Quad-Channel Digital Isolators with Robust **EMC**

#### 1 Features

- Functional Safety-Capable
  - Documentation available to aid functional safety system design: ISO6740, ISO6741, ISO6742
- 50 Mbps data rate
- Robust isolation barrier:
  - High lifetime at 1500 V<sub>RMS</sub> working voltage
  - Up to 5000 V<sub>RMS</sub> isolation rating
  - Up to 10 kV surge capability
  - ±150 kV/µs typical CMTI
- Wide supply range: 1.71 V to 1.89 V and 2.25 V to 5.5 V
- 1.71 V to 5.5 V level translation
- Default output high (ISO674x) and low (ISO674xF)
- Wide temperature range: -40°C to 125°C
- 1.6 mA per channel typical at 1 Mbps
- Low propagation delay: 11 ns typical
- Robust electromagnetic compatibility (EMC)
  - System-level ESD, EFT, and surge immunity
  - ±8 kV IEC 61000-4-2 contact discharge protection across isolation barrier
  - Low emissions
- Wide-SOIC (DW-16) Package
- Safety-Related Certifications:
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 component recognition program
  - IEC 62368-1, IEC 61010-1, IEC 60601-1
  - GB 4943.1

## 2 Applications

- Power supplies
- Grid, Electricity meter
- Motor drives
- **Factory automation**
- **Building automation**
- Lighting
- **Appliances**

### 3 Description

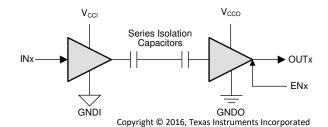
The ISO674x devices are high-performance, guadchannel digital isolators ideal for cost-sensitive applications requiring up to 5000 V<sub>RMS</sub> isolation ratings per UL 1577. These devices are also certified by VDE, TUV, CSA, and CQC.

The ISO674x devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by TI's double capacitive silicon dioxide (SiO<sub>2</sub>) insulation barrier. These devices come with enable pins which can be used to put the respective outputs in high impedance for multi-master driving applications. The ISO6740 device has all four channels in the same direction, ISO6741 device has three forward and one reverse-direction channels, and ISO6742 device has two forward and two reversedirection channels. In the event of input power or signal loss, the default output is high for devices without suffix F and low for devices with suffix F. See Device Functional Modes section for further details.

#### **Device Information**

PART NUMBER <sup>(1)</sup>	PACKAGE	BODY SIZE (NOM)
ISO6740, ISO6740F	SOIC (DW)	10.30 mm × 7.50 mm
ISO6741, ISO6741F		
ISO6742, ISO6742F		

For all available packages, see the orderable addendum at the end of the data sheet.



V<sub>CCI</sub>=Input supply, V<sub>CCO</sub>=Output supply GNDI=Input ground, GNDO=Output ground

#### Simplified Schematic



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# **4 Revision History**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

C	hanges from Revision F (May 2022) to Revision G (February 2023)	Page
•	Changed standard name from "DIN V VDE V 0884-11:2017-01" to "DIN EN IEC 60747-17 (VDE 0884-	17)"
	throughout the document	1
•	Removed references to standard IEC/EN/CSA 60950-1 throughout the document	
•	Removed standard revision and year references from all standard names thoughout the document	1
•	Added Maximum impulse voltage V <sub>IMP</sub> specification per DIN EN IEC 60747-17 (VDE 0884-17)	10
•	Changed test conditions and values of Maximum surge isolation voltage (V <sub>IOSM</sub> ) specification per DIN I	EN IEC
	60747-17 (VDE 0884-17)	10
•	Clarified method b test conditions of Apparent charge (q <sub>PD</sub> )	10
•	Changed maximum surge isolation voltage from 6250 V <sub>PK</sub> to 10000 V <sub>PK</sub>	11
•	Changed working voltage lifetime margin from 87.5% to 50%, minimum required insulation lifetime from years to 30 years, and insulation lifetime per TDDB from 135 years to 36 years per DIN EN IEC 60747-(VDE 0884-17)	
	Changed Figure 10-8 per DIN EN IEC 60747-17 (VDE 0884-17)	3/1

CI	hanges from Revision E (June 2021) to Revision F (May 2022)	Page
•	Updated CMTI typical to 150 kV/us and minimum to 100 kV/us	7

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С	hanges from Revision D (March 2021) to Revision E (June 2021)	Page
•	Updated high lifetime working voltage	1
•	Insulation Specifications table 7.6 has been updated with VIOWM 1500Vrms, VIORM at 2121Vpk	7
•	Updated Safety-Related Certification table	
•	Updated switching characteristics tables with test conditions for "Default output delay time from input	power
	loss" line item	
•	Switched the labels for V <sub>CC1</sub> falling and V <sub>CC2</sub> rising in the graph legend of <i>Power Supply Undervoltage</i>	
	Threshold vs Free-Air Temperature	
•	Updated Typical Application diagram to reflect 5.5Viso	
•	Updated Insulation Lifetime Projection Data image	
•	Updated SN6505A reference with SN6505B in Power Supply Recommendations	36
-	Added ISO6742 data under Specifications	7
С	hanges from Revision B (December 2020) to Revision C (January 2021)	Page
<u>.</u>	Added ISO674x to data sheet.	1
	hanges from Revision A (October 2020) to Revision B (December 2020)	Page
•	Updated device status to Production Data	1
С	hanges from Revision * (August 2020) to Revision A (October 2020)	Page
_	Pre-RTM adjustments	
	•	



## **5 Description Continued**

Used in conjunction with isolated power supplies, the ISO674x devices help prevent noise currents on data buses, such as UART, SPI, RS-485, RS-232, and CAN from damaging sensitive circuitry. Through innovative chip design and layout techniques, the electromagnetic compatibility of the ISO674x devices has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. The ISO674x family of devices is available in a 16-pin SOIC wide-body (DW) package and is a pin-to-pin upgrade to the older generations.



# **6 Pin Configuration and Functions**

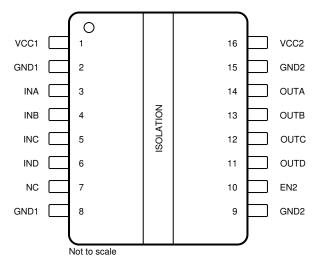


Figure 6-1. ISO6740 DW Package 16-Pin SOIC-WB Top View

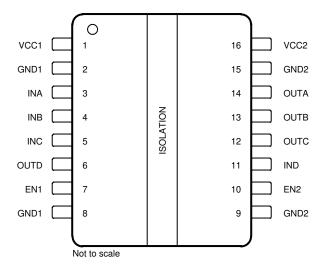


Figure 6-2. ISO6741 DW Package 16-Pin SOIC-WB Top View

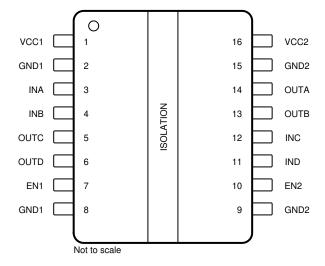


Figure 6-3. ISO6742 DW Package 16-Pin SOIC-WB Top View



## **Table 6-1. Pin Functions**

			iable 0-	I. FIIII C			
		PIN		1/0	DESCRIPTION		
NAME	ISO6740	ISO6741	ISO6742	"0	DESCRIPTION		
EN1	-	7	7	ı	Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.		
EN2	10	10	10	ı	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.		
GND1	2, 8	2,8	2,8	_	Ground connection for V <sub>CC1</sub>		
GND2	9, 15	9,15	9,15	_	Ground connection for V <sub>CC2</sub>		
INA	3	3	3	I	Input, channel A		
INB	4	4	4	I	Input, channel B		
INC	5	5	12	I	Input, channel C		
IND	6	11	11	I	Input, channel D		
NC	7	-	-		Not connected		
OUTA	14	14	14	0	Output, channel A		
OUTB	13	13	13	0	Output, channel B		
OUTC	12	12	5	0	Output, channel C		
OUTD	11	6	6	0	Output, channel D		
V <sub>CC1</sub>	1	1	1	_	Power supply, side 1		
V <sub>CC2</sub>	16	16	16	_	Power supply, side 2		
002		_			11.37		

## 7 Specifications

Updated switching characteristics tables with test conditions for "Default output delay time from input power loss" line item

## 7.1 Absolute Maximum Ratings

See(1)

		MIN	MAX	UNIT
Supply voltage (2)	V <sub>CC1</sub> to GND1	-0.5	6	V
	V <sub>CC2</sub> to GND2	-0.5	6	V
Input/Output Voltage	INx to GNDx	-0.5	V <sub>CCX</sub> + 0.5 (3)	V
	OUTx to GNDx	-0.5	V <sub>CCX</sub> + 0.5 (3)	V
Output current	lo	-15	15	mA
Temperature	Operating junction temperature, T <sub>J</sub>		150	°C
	Storage temperature, T <sub>stg</sub>	-65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
- (3) Maximum voltage must not exceed 6 V.

## 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>		Human body model (HBM), per ANSI/ ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±6000	
	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1500	V
		Contact discharge per IEC 61000-4-2; Isolation barrier withstand test <sup>(3)</sup> (4)	±8000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
- (3) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
- (4) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.



## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	<u> </u>		MIN	NOM	MAX	UNIT
V <sub>CC1</sub> (1)	Supply Voltage Side 1	V <sub>CC</sub> = 1.8 V <sup>(3)</sup>	1.71		1.89	V
V <sub>CC1</sub> (1)	Supply Voltage Side 1	$V_{CC} = 2.5 \text{ V to 5 V}^{(3)}$	2.25		5.5	V
V <sub>CC2</sub> (1)	Supply Voltage Side 2	V <sub>CC</sub> = 1.8 V <sup>(3)</sup>	1.71		1.89	V
V <sub>CC2</sub> (1)	Supply Voltage Side 2	V <sub>CC</sub> = 2.5 V to 5 V <sup>(3)</sup>	2.25		5.5	V
Vcc (UVLO+)	UVLO threshold when supply vo	oltage is rising		1.53	1.71	V
Vcc (UVLO-)	UVLO threshold when supply voltage is falling		1.1	1.41		V
Vhys (UVLO)	Supply voltage UVLO hysteresis		0.08	0.13		V
V <sub>IH</sub>	High level Input voltage		0.7 x V <sub>CCI</sub>		V <sub>CCI</sub>	V
V <sub>IL</sub>	Low level Input voltage		0		0.3 x V <sub>CCI</sub>	V
	High lavel autout average	V <sub>CCO</sub> = 5 V <sup>(2)</sup>	-4			mA
1		V <sub>CCO</sub> = 3.3 V	-2			mA
I <sub>OH</sub>	High level output current	V <sub>CCO</sub> = 2.5 V	-1			mA
		V <sub>CCO</sub> = 1.8 V	-1			mA
		V <sub>CCO</sub> = 5 V			4	mA
	Low level output current	V <sub>CCO</sub> = 3.3 V			2	mA
I <sub>OL</sub>	Low level output current	V <sub>CCO</sub> = 2.5 V			1	mA
		V <sub>CCO</sub> = 1.8 V			1	mA
DR	Data Rate		0		50	Mbps
T <sub>A</sub>	Ambient temperature		-40	25	125	°C

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 <sup>(1)</sup> V<sub>CC1</sub> and V<sub>CC2</sub> can be set independent of one another
 (2) V<sub>CCI</sub> = Input-side V<sub>CC</sub>; V<sub>CCO</sub> = Output-side V<sub>CC</sub>
 (3) The channel outputs are in undetermined state when 1.89 V < V<sub>CC1</sub>, V<sub>CC2</sub> < 2.25 V and 1.05 V < V<sub>CC1</sub>, V<sub>CC2</sub> < 1.71 V</li>



## 7.4 Thermal Information

		ISO674x	
	THERMAL METRIC <sup>(1)</sup>	DW (SOIC)	UNIT
		16 PINS	
R <sub>0JA</sub>	Junction-to-ambient thermal resistance	73	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	36.1	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	40.4	°C/W
ΨЈТ	Junction-to-top characterization parameter	17	°C/W
ΨЈВ	Junction-to-board characterization parameter	39.9	°C/W
R <sub>0JC(bot)</sub>	Junction-to-case (bottom) thermal resistance	_	°C/W

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 7.5 Power Ratings

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO6740	0					
P <sub>D</sub>	Maximum power dissipation (both sides)	V <sub>CC1</sub> = V <sub>CC2</sub> = 5.5 V, T <sub>J</sub> = 150°C, C <sub>J</sub> =	130.9		130.9	mW
P <sub>D1</sub>	Maximum power dissipation (side-1)	15 pF, Input a 25-MHz 50% duty cycle			33	mW
P <sub>D2</sub>	Maximum power dissipation (side-2)	square wave			97.9	mW
ISO674	1		•		'	
P <sub>D</sub>	Maximum power dissipation (both sides)	V <sub>CC1</sub> = V <sub>CC2</sub> = 5.5 V, T <sub>.I</sub> = 150°C, C <sub>I</sub> =			134.9	mW
P <sub>D1</sub>	Maximum power dissipation (side-1)	15 pF, Input a 25-MHz 50% duty cycle			50.8	mW
P <sub>D2</sub>	Maximum power dissipation (side-2)	square wave			84.1	mW
ISO6742	2		•			
P <sub>D</sub>	Maximum power dissipation (both sides)	V <sub>CC1</sub> = V <sub>CC2</sub> = 5.5 V, T <sub>J</sub> = 150°C, C <sub>J</sub> =			137.5	mW
P <sub>D1</sub>	Maximum power dissipation (side-1)	15 pF, Input a 25-MHz 50% duty cycle			68.75	mW
P <sub>D2</sub>	Maximum power dissipation (side-2)	square wave			68.75	mW



### 7.6 Insulation Specifications

			VALUE	
PARAMETER		TEST CONDITIONS	DW-16	UNIT
CLR	External clearance <sup>(1)</sup>	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External creepage <sup>(1)</sup>	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	um
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material group	According to IEC 60664-1	I	
	Over-18-18-18-18-18-18-18-18-18-18-18-18-18-	Rated mains voltage ≤ 600 V <sub>RMS</sub>	I-IV	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 1000 V <sub>RMS</sub>	1-111	
DIN EN	IEC 60747-17 (VDE 0884-17) (2)		1	
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V <sub>PK</sub>
V <sub>IOWM</sub>	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test; See Figure 10-8	1500	V <sub>RMS</sub>
		DC voltage	2121	V <sub>DC</sub>
V <sub>IOTM</sub>	Maximum transient isolation voltage	V <sub>TEST</sub> = V <sub>IOTM</sub> , t = 60 s (qualification); V <sub>TEST</sub> = 1.2 x V <sub>IOTM</sub> , t= 1 s (100% production)	7071	V <sub>PK</sub>
V <sub>IMP</sub>	Maximum impulse voltage <sup>(3)</sup>	Tested in air, 1.2/50-us waveform per IEC 62368-1	7692	V <sub>PK</sub>
V <sub>IOSM</sub>	Maximum surge isolation voltage <sup>(4)</sup>	V <sub>IOSM</sub> ≥ 1.3 x V <sub>IMP</sub> ; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	10000	V <sub>PK</sub>
	Apparent charge <sup>(5)</sup>	Method a, After Input-output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$ , $t_{ini} = 60 \text{ s}$ ; $V_{pd(m)} = 1.2 \text{ x } V_{IORM}$ , $t_m = 10 \text{ s}$	≤5	
q <sub>pd</sub>		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$ , $t_{ini} = 60 \text{ s}$ ; $V_{pd(m)} = 1.6 \text{ x } V_{IORM}$ , $t_m = 10 \text{ s}$	≤5	рС
		Method b: At routine test (100% production) and preconditioning (type test); $V_{ini} = 1.2 \times V_{IOTM}, \ t_{ini} = 1 \text{ s}; \\ V_{pd(m)} = 1.875 \times V_{IORM}, \ t_{m} = 1 \text{ s (method b1) or } \\ V_{pd(m)} = V_{ini}, \ t_{m} = t_{ini} \text{ (method b2)}$	≤5	
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(6)</sup>	$V_{IO} = 0.4 \text{ x sin } (2\pi \text{ft}), \text{ f} = 1 \text{ MHz}$	~1	pF
		V <sub>IO</sub> = 500 V, T <sub>A</sub> = 25°C	>10 <sup>12</sup>	
R <sub>IO</sub>	Isolation resistance <sup>(6)</sup>	V <sub>IO</sub> = 500 V, 100°C ≤ T <sub>A</sub> ≤ 125°C	>10 <sup>11</sup>	Ω
		V <sub>IO</sub> = 500 V at T <sub>S</sub> = 150°C	>10 <sup>9</sup>	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577			·	
V <sub>ISO</sub>	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$ , $t = 60$ s (qualification), $V_{TEST} = 1.2$ x $V_{ISO}$ , $t = 1$ s (100% production)	5000	V <sub>RMS</sub>

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air to determine the surge immunity of the package.
- (4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
- (5) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (6) All pins on each side of the barrier tied together creating a two-terminal device.

#### 7.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 62368-1, IEC 61010-1 and IEC 60601	Certified according to UL 1577 Component Recognition Program	Certified according to GB 4943.1	Certified according to EN 61010-1 and EN 62368-1
Maximum transient isolation voltage, 7071 V <sub>PK</sub> ; Maximum repetitive peak isolation voltage, 2121 V <sub>PK</sub> ; Maximum surge isolation voltage, 10000 V <sub>PK</sub>	5000 V <sub>RMS</sub> insulation per CSA 62368-1, IEC 62368-1, CSA 61010-1 and IEC 61010-1, 1000 V <sub>RMS</sub> basic and 600 V <sub>RMS</sub> reinforced working voltage (pollution degree 2, material group I); 5000 V <sub>RMS</sub> insulation per CSA 60601-1 and IEC 60601-1, 2 MOPP for 250 V <sub>RMS</sub>	Single protection, 5000 V <sub>RMS</sub>	Reinforced insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V <sub>RMS</sub> maximum working voltage	5000 V <sub>RMS</sub> reinforced insulation per EN 61010-1 and EN 62368-1 up to working voltage of 600 V <sub>RMS</sub> and EN 60950- 1 up to working voltage of 800 V <sub>RMS</sub>
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate number: CQC21001304083	Client ID number: 077311

## 7.8 Safety Limiting Values

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
DW-16 F	PACKAGE						
		R <sub>θJA</sub> =73°C/W, V <sub>I</sub> = 5.5 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			311.4	mA	
I <sub>S</sub> S	Cofety input output or cumply current	$R_{\theta JA} = 73^{\circ}C/W, V_I = 3.6 \text{ V}, T_J = 150^{\circ}C, T_A$ = 25°C	475.7		475.7	A	
	Safety input, output, or supply current	$R_{\theta JA} = 73^{\circ}C/W, V_I = 2.75 \text{ V}, T_J = 150^{\circ}C, T_A = 25^{\circ}C$			622	mA	
		$R_{\theta JA} = 73^{\circ}C/W$ , $V_{I} = 1.89 \text{ V}$ , $T_{J} = 150^{\circ}C$ , $T_{A} = 25^{\circ}C$			905.1	mA	
Ps	Safety input, output, or total power	$R_{\theta JA} = 73^{\circ}C/W, T_{J} = 150^{\circ}C, T_{A} = 25^{\circ}C$			1712.4	mW	
T <sub>S</sub>	Maximum safety temperature				150	°C	

<sup>(1)</sup> The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power respectively. The maximum limits of I<sub>S</sub> and P<sub>S</sub> should not be exceeded. These limits vary with the ambient temperature, T<sub>A</sub>.

exceeded. These limits vary with the ambient temperature,  $T_A$ . The junction-to-air thermal resistance,  $R_{\theta JA}$ , in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

 $T_J = T_A + R_{\theta JA} \times P$ , where P is the power dissipated in the device.

 $T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$ , where  $T_{J(max)}$  is the maximum allowed junction temperature.

 $P_S = I_S \times V_I$ , where  $V_I$  is the maximum input voltage.



## 7.9 Electrical Characteristics—5-V Supply

V<sub>CC1</sub> = V<sub>CC2</sub> = 5 V ±10% (over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP MAX	UNIT
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -4 mA; See Figure 8-1	V <sub>CCO</sub> - 0.4 (1)		V
$V_{OL}$	Low-level output voltage	I <sub>OL</sub> = 4 mA; See Figure 8-1		0.4	V
V <sub>IT+(IN)</sub>	Rising input switching threshold			0.7 x V <sub>CCI</sub> <sup>(1)</sup>	V
V <sub>IT-(IN)</sub>	Falling input switching threshold		0.3 x V <sub>CCI</sub>		V
V <sub>I(HYS)</sub>	Input threshold voltage hysteresis		0.1 x V <sub>CCI</sub>		V
I <sub>IH</sub>	High-level input current	V <sub>IH</sub> = V <sub>CCI</sub> <sup>(1)</sup> at INx		10	μA
I <sub>IL</sub>	Low-level input current	V <sub>IL</sub> = 0 V at INx	-10		μA
I <sub>IH</sub>	High-level input current	V <sub>IH</sub> = V <sub>CCI</sub> <sup>(1)</sup> at ENx		28	uA
I <sub>IL</sub>	Low-level input current	V <sub>IL</sub> = 0 V at ENx	-28		uA
СМТІ	Common mode transient immunity	V <sub>I</sub> = V <sub>CC</sub> or 0 V, V <sub>CM</sub> = 1200 V; See Figure 8-4	100	150	kV/us
C <sub>i</sub>	Input Capacitance (2)	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft), f = 2$ MHz, $V_{CC} = 5 \text{ V}$		2.8	pF

 $<sup>\</sup>begin{array}{ll} \hbox{(1)} & V_{CCI} = Input\text{-side } V_{CC}; \, V_{CCO} = Output\text{-side } V_{CC} \\ \hbox{(2)} & Measured from input pin to same side ground. \\ \end{array}$ 

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# 7.10 Supply Current Characteristics—5-V Supply

V<sub>CC1</sub> = V<sub>CC2</sub> = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITION	S	SUPPLY CURRENT	MIN TYP	MAX	UNIT
ISO6740						
	$V_I = V_{CC1}$ (1)(ISO6740); $V_I = 0 \text{ V (ISO}$	06740 with F	I <sub>CC1</sub>	1.6	2.2	
Supply current - DC signal Supply current - AC signal SO6741 Supply current - DC signal	suffix)		I <sub>CC2</sub>	2.1	3.4	İ
(2)	V <sub>I</sub> = 0 V (ISO6740); V <sub>I</sub> = V <sub>CC1</sub> (ISO6	740 with F suffix)	I <sub>CC1</sub>	5.8	2.2	l
	V  = 0 V (1300740), V  = V661 (1300	740 Willi Sullix)	I <sub>CC2</sub>	2.3	5.8 8 2.3 3.7 3.7 5.1 2.4 3.8 3.8 5.3 4.8 6.4 4.4 6 15 17.8  1.9 2.8 2.2 3.5 5.1 7.2 3.4 5.1 3.6 5.1	Ì
		1 Mbps	I <sub>CC1</sub>	3.7	5.1 3.8 5.3 6.4 6 17.8	mA
Supply current - AC signal (3)  All channels switching with square wave clock input; $C_L = 15 \text{ pF}$	2.4	3.8	1111/			
		10 Mbps	I <sub>CC1</sub>	3.8	5.3	İ
(3)		TO IVIDPS	I <sub>CC2</sub>	4.8	6.4	İ
		50 Mbps	I <sub>CC1</sub>	4.4	6	l
		oo ivibpa	I <sub>CC2</sub>	15	17.8	
ISO6741						
Supply current - DC signal	$V_1 = V_{0.01} (1)(15.06741) \cdot V_2 = 0.00 (15.06741)$ with F suffix)		I <sub>CC1</sub>	1.9	2.8	
	VI = VCCI ((1300741), VI = 0 V (130	0741 WILLI F SUIIIX)	I <sub>CC2</sub>	2.2	3.5	Ì
(2)	V. = 0 V (ISO6741): V. = V (ISO6:	\( \ = 0 \\ \langle \( \langle \) \( \ \ = \\ \\ \\ \\ \\ \\ \ \\ \\ \\ \\ \		5.1	3.7 5.1 3.8 5.3 6.4 6 17.8 2.8 3.5 7.2 5.1 4.5 5.8 6.5 9.3 15.3	l
	V <sub>1</sub> = 0 V (1300741), V <sub>1</sub> = V <sub>CCI</sub> (1300	741 WILLI F SUIIIX)	I <sub>CC2</sub>	3.4	5.1 7.2 3.4 5.1	İ
		1 Mbps	I <sub>CC1</sub>	3.6	2.8 3.5 7.2 5.1 4.5 5.8 6.5	mA
		1 Mbps	I <sub>CC2</sub>	3		IIIA
Supply current - DC signal (2) $ V_{I} = V_{CCI} \text{ (ISO6741); } V_{I} = 0 \text{ V (ISO6741 with F suffix)}                                    $	4.2	5.8	l			
(3)	wave clock input; C <sub>L</sub> = 15 pF	TO Mbps	I <sub>CC2</sub>	4.8	6.5	l
		EO Mbno	I <sub>CC1</sub>	7.3	9.3	l
		SQ MDDS	I <sub>CC2</sub>	12.6	15.3	l
ISO6742						
Supply current - DC	V <sub>I</sub> = V <sub>CCI</sub> <sup>(1)</sup> (ISO6742); V <sub>I</sub> = 0 V (ISC	6742 with F suffix)	I <sub>CC1</sub> , I <sub>CC2</sub>	2.2	3.3	
signal (2) $V_1 = 0 \text{ V (ISO6742)}; V_1 = V_{CCI} \text{ (ISO6742 with F suffix)} $ $I_{CC1}$ $I_{CC2}$	4.4	6.3				
		1 Mbps	I <sub>CC1</sub> , I <sub>CC2</sub>	3.4	5	mA
Supply current - AC signal <sup>(3)</sup>		10 Mbps	I <sub>CC1</sub> , I <sub>CC2</sub>	4.7	6.4	Ì
signal • /	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	12.5	İ			

 <sup>(1)</sup> V<sub>CCI</sub> = Input-side V<sub>CC</sub>
 (2) Supply current valid for ENx = V<sub>CCx</sub> and ENx = 0V
 (3) Supply current valid for ENx = V<sub>CCx</sub>



## 7.11 Electrical Characteristics—3.3-V Supply

V<sub>CC1</sub> = V<sub>CC2</sub> = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -2mA; See Figure 8-1	V <sub>CCO</sub> - 0.2 <sup>(1)</sup>			V
$V_{OL}$	Low-level output voltage	I <sub>OL</sub> = 2mA; See Figure 8-1			0.2	V
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V <sub>CCI</sub> <sup>(1)</sup>	V
V <sub>IT-(IN)</sub>	Falling input switching threshold		0.3 x V <sub>CCI</sub>			V
V <sub>I(HYS)</sub>	Input threshold voltage hysteresis		0.1 x V <sub>CCI</sub>			V
I <sub>IH</sub>	High-level input current	V <sub>IH</sub> = V <sub>CCI</sub> <sup>(1)</sup> at INx			10	μΑ
I <sub>IL</sub>	Low-level input current	V <sub>IL</sub> = 0 V at INx	-10			μΑ
I <sub>IH</sub>	High-level input current	V <sub>IH</sub> = V <sub>CCI</sub> <sup>(1)</sup> at ENx			30	uA
I <sub>IL</sub>	Low-level input current	V <sub>IL</sub> = 0 V at ENx	-30			uA
CMTI	Common mode transient immunity	V <sub>I</sub> = V <sub>CC</sub> or 0 V, V <sub>CM</sub> = 1200 V; See Figure 8-4	100	150		kV/us
Ci	Input Capacitance (2)	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft), f = 2$ MHz, $V_{CC} = 3.3 \text{ V}$		2.8		pF

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 $<sup>\</sup>begin{array}{ll} \text{(1)} & \text{$V_{\text{CCI}}$ = Input-side $V_{\text{CC}}$; $V_{\text{CCO}}$ = Output-side $V_{\text{CC}}$} \\ \text{(2)} & \text{Measured from input pin to same side ground.} \\ \end{array}$ 

# 7.12 Supply Current Characteristics—3.3-V Supply

V<sub>CC1</sub> = V<sub>CC2</sub> = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITION	S	SUPPLY CURRENT	MIN TYP	MAX	UNIT
ISO6740	•					
	V <sub>I</sub> = V <sub>CC1</sub> (1)(ISO6740); V <sub>I</sub> = 0 V (IS	O6740 with F	I <sub>CC1</sub>	1.6	2.2	
Supply current - DC	suffix)		I <sub>CC2</sub>	2.1	3.3	
signal (2)	V <sub>I</sub> = 0 V (ISO6740); V <sub>I</sub> = V <sub>CC1</sub> (ISO6	740 with E cuffix)	I <sub>CC1</sub>	5.7	1.6 2.2 2.1 3.3 5.7 8 2.3 3.6 3.7 5.1 2.4 3.7 3.8 5.2 4 5.6 4.2 5.7 11.2 13.8 1.9 2.7 2.2 3.4 5 7.1 3.5 5 2.9 4.4 4 5.5 4.2 5.8 6.1 8 9.7 12.1 2.2 3.3 4.4 6.3 3.4 4.9 4.2 5.9	Ì
Supply current - AC signal (3) SO6741 Supply current - DC signal	V  = 0 V (1300740); V  = V <sub>CC1</sub> (1300	740 Will F Sullix)	I <sub>CC2</sub>	2.3	3.6	Ì
		1 Mbps	I <sub>CC1</sub>	3.7	5.1	mA
		1 Mbps	I <sub>CC2</sub>	2.4	3.7	1117
Supply current - AC	All channels switching with square wave clock input; C <sub>L</sub> = 15 pF	10 Mbps	I <sub>CC1</sub>	3.8	5.2	İ
signal <sup>(3)</sup>		10 Mbps	I <sub>CC2</sub>	4	5.6	l
		50 Mbps	I <sub>CC1</sub>	4.2	5.7	İ
		oo ivinha	I <sub>CC2</sub>	11.2	13.8	
ISO6741						
Supply current - DC signal	$V_I = V_{CCI}$ (1)(ISO6741); $V_I = 0$ V (ISO6741 with F		I <sub>CC1</sub>	1.9	2.7	
	suffix)	suffix)		2.2	3.4	
(1)	V. = 0 V (ISO6741): V. = V (ISO6	7/11 with E cuffix)	I <sub>CC1</sub>	5	4 5.6 4.2 5.7 11.2 13.8 1.9 2.7 2.2 3.4 5 7.1 3.4 5.1 3.5 5 2.9 4.4 4 5.5	İ
	V  = 0 V (1300741); V  = VCCI (1300	741 WILLI F SUIIX)	I <sub>CC2</sub>	3.4	5.1	İ
		1 Mbps	I <sub>CC1</sub>	3.5	5	mA
	$V_{I} = V_{CCI} \   ^{(1)}(ISO6741); \   V_{I} = 0 \   V \   (ISO6741 \   with \   F) \   \frac{I_{CC1}}{I_{CC2}} \   \frac{1.9}{I_{CC2}} \   \frac{2.2}{2.2} \   V_{I} = 0 \   V \   (ISO6741); \   V_{I} = V_{CCI} \   (ISO6741 \   with \   F \   suffix) \   \frac{I_{CC1}}{I_{CC2}} \   \frac{5}{3.4} \   \frac{1}{I_{CC2}} \   \frac{3.4}{I_{CC2}} \   \frac{3.5}{I_{CC2}} \   \frac{1}{I_{CC2}} \  $	4.4	ı			
Supply current - DC signal  V  Supply current - AC signal		10 Mbps	I <sub>CC1</sub>	4	5.5	l
(2)	wave clock input; C <sub>L</sub> = 15 pF	TO MDPS	I <sub>CC2</sub>	4.2	5.8	İ
		50 Mbps	I <sub>CC1</sub>	6.1	8	İ
		50 Mbps	I <sub>CC2</sub>	9.7	12.1	İ
ISO6742						
Supply current - DC	V <sub>I</sub> = V <sub>CCI</sub> <sup>(1)</sup> (ISO6742); V <sub>I</sub> = 0 V (ISO	06742 with F suffix)	I <sub>CC1</sub> , I <sub>CC2</sub>	2.2	3.3	
signal (2)	V <sub>I</sub> = 0 V (ISO6742); V <sub>I</sub> = V <sub>CCI</sub> (ISO6	742 with F suffix)	I <sub>CC1</sub> , I <sub>CC2</sub>	4.4	6.3	Ì
		1 Mbps	I <sub>CC1</sub> , I <sub>CC2</sub>	3.4	4.9	mA
	All channels switching with square wave clock input; $C_L = 15 \text{ pF}$	10 Mbps	I <sub>CC1</sub> , I <sub>CC2</sub>	4.2	5.9	Ì
Supply current - AC signal (2)  ISO6742  Supply current - DC	mare stock input, of the pi	50 Mbps	I <sub>CC1</sub> , I <sub>CC2</sub>	8.2	10.3	

 <sup>(1)</sup> V<sub>CCI</sub> = Input-side V<sub>CC</sub>
 (2) Supply current valid for ENx = V<sub>CCx</sub> and ENx = 0V
 (3) Supply current valid for ENx = V<sub>CCx</sub>



## 7.13 Electrical Characteristics—2.5-V Supply

V<sub>CC1</sub> = V<sub>CC2</sub> = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -1mA; See Figure 8-1	V <sub>CCO</sub> - 0.1 <sup>(1)</sup>			V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 1mA; See Figure 8-1			0.1	V
V <sub>IT+(IN)</sub>	Rising input switching threshold				0.7 x V <sub>CCI</sub> <sup>(1)</sup>	V
V <sub>IT-(IN)</sub>	Falling input switching threshold		0.3 x V <sub>CCI</sub>			V
V <sub>I(HYS)</sub>	Input threshold voltage hysteresis		0.1 x V <sub>CCI</sub>			V
I <sub>IH</sub>	High-level input current	V <sub>IH</sub> = V <sub>CCI</sub> <sup>(1)</sup> at INx			10	μA
I <sub>IL</sub>	Low-level input current	V <sub>IL</sub> = 0 V at INx	-10			μΑ
I <sub>IH</sub>	High-level input current	V <sub>IH</sub> = V <sub>CCI</sub> <sup>(1)</sup> at ENx			30	uA
I <sub>IL</sub>	Low-level input current	V <sub>IL</sub> = 0 V at ENx	-30			uA
CMTI	Common mode transient immunity	V <sub>I</sub> = V <sub>CC</sub> or 0 V, V <sub>CM</sub> = 1200 V; See Figure 8-4	100	150		kV/us
Ci	Input Capacitance (2)	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft), f = 2$ MHz, $V_{CC} = 2.5 \text{ V}$		2.8		pF

 $<sup>\</sup>begin{array}{ll} \text{(1)} & \text{$V_{\text{CCI}}$ = Input-side $V_{\text{CC}}$; $V_{\text{CCO}}$ = Output-side $V_{\text{CC}}$} \\ \text{(2)} & \text{Measured from input pin to same side ground.} \\ \end{array}$ 

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# 7.14 Supply Current Characteristics—2.5-V Supply

 $V_{CC1} = V_{CC2} = 2.5 \text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITION	s	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6740							
	$V_I = V_{CC1}$ (1)(ISO6740); $V_I = 0$ V (ISO	D6740 with F	I <sub>CC1</sub>		1.6	2.2	
Supply current - DC signal	suffix)		I <sub>CC2</sub>		2.1	3.3	
Supply current - DC signal  Supply current - AC signal (3)  SO6741  Supply current - DC signal (2)  Supply current - DC signal (3)	$V_{I} = 0 \text{ V (ISO6740)}; V_{I} = V_{CC1} \text{ (ISO6740 with F suffix)}$		I <sub>CC1</sub>		5.7	7.9	
	V  = 0 V (1880/ 40); V  = V881 (1880		I <sub>CC2</sub>		2.3	3.6	
	All channels switching with square wave clock input; $C_L = 15 \text{ pF}$	1 Mbps	I <sub>CC1</sub>		3.7	5.1	mA
		Тибра	I <sub>CC2</sub>		2.3	3.6	ША
Supply current - AC		10 Mbps	I <sub>CC1</sub>		3.7	5.1	
signal <sup>(3)</sup>		10 Mbps	I <sub>CC2</sub>		3.5	5.1	
		50 Mbps	I <sub>CC1</sub>		4.1	5.6	
		OO IVIDPO	I <sub>CC2</sub>		9	11.2	
ISO6741							
Supply current - DC signal	$V_I = V_{CCI}$ (1)(ISO6741); $V_I = 0$ V (ISO6741 with F suffix)		I <sub>CC1</sub>		1.9	2.7	
			I <sub>CC2</sub>		2.2	3.4	
	V <sub>I</sub> = 0 V (ISO6741); V <sub>I</sub> = V <sub>CCI</sub> (ISO6741 with F suffix)		I <sub>CC1</sub>		5	7.1	
			I <sub>CC2</sub>		3.4	5.1	
		1 Mhno	I <sub>CC1</sub>		3.5	5	mA
		1 Mbps	I <sub>CC2</sub>		2.9	4.4	MA
Supply current - AC signal	All channels switching with square	40 Mb = =	I <sub>CC1</sub>		3.9	5.4	
(3)	wave clock input; C <sub>L</sub> = 15 pF	10 Mbps	I <sub>CC2</sub>		3.8	5.4	
		FO Missis	I <sub>CC1</sub>		5.5	7.2	
		50 Mbps	I <sub>CC2</sub>		8.1	10.2	
ISO6742		-1	1		,	·	
Supply current - DC signal	V <sub>I</sub> = V <sub>CCI</sub> <sup>(1)</sup> (ISO6742); V <sub>I</sub> = 0 V (ISC	06742 with F suffix)	I <sub>CC1</sub> , I <sub>CC2</sub>		2.2	3.3	
(2)	V <sub>I</sub> = 0 V (ISO6742); V <sub>I</sub> = V <sub>CCI</sub> (ISO6	742 with F suffix)	I <sub>CC1</sub> , I <sub>CC2</sub>		4.3	6.3	
		1 Mbps	I <sub>CC1,</sub> I <sub>CC2</sub>		3.3	4.8	mA
Supply current - AC signal <sup>(3)</sup>	All channels switching with square wave clock input; $C_L = 15 \text{ pF}$	10 Mbps	I <sub>CC1</sub> , I <sub>CC2</sub>		4	5.6	
Signal (7)	wave clock iliput, CL = 15 pr	50 Mbps	I <sub>CC1</sub> , I <sub>CC2</sub>		7	9	

 <sup>(1)</sup> V<sub>CCI</sub> = Input-side V<sub>CC</sub>
 (2) Supply current valid for ENx = V<sub>CCx</sub> and ENx = 0V
 (3) Supply current valid for ENx = V<sub>CCx</sub>



## 7.15 Electrical Characteristics—1.8-V Supply

V<sub>CC1</sub> = V<sub>CC2</sub> = 1.8 V ±5% (over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP MAX	UNIT
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -1mA; See Figure 8-1	V <sub>CCO</sub> - 0.1 (1)		V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 1mA; See Figure 8-1		0.1	V
V <sub>IT+(IN)</sub>	Rising input switching threshold			0.7 x V <sub>CCI</sub> <sup>(1)</sup>	V
V <sub>IT-(IN)</sub>	Falling input switching threshold		0.3 x V <sub>CCI</sub>		V
V <sub>I(HYS)</sub>	Input threshold voltage hysteresis		0.1 x V <sub>CCI</sub>		V
I <sub>IH</sub>	High-level input current	V <sub>IH</sub> = V <sub>CCI</sub> <sup>(1)</sup> at INx		10	μΑ
I <sub>IL</sub>	Low-level input current	V <sub>IL</sub> = 0 V at INx	-10		μΑ
I <sub>IH</sub>	High-level input current	V <sub>IH</sub> = V <sub>CCI</sub> <sup>(1)</sup> at ENx		30	μΑ
I <sub>IL</sub>	Low-level input current	V <sub>IL</sub> = 0 V at ENx	-30		μΑ
СМТІ	Common mode transient immunity	V <sub>I</sub> = V <sub>CC</sub> or 0 V, V <sub>CM</sub> = 1200 V; See Figure 8-4	100	150	kV/us
Ci	Input Capacitance (2)	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi f t), f = 2$ MHz, $V_{CC} = 1.8 \text{ V}$		2.8	pF

 $V_{CCI}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$  Measured from input pin to same side ground. (1)

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# 7.16 Supply Current Characteristics—1.8-V Supply

V<sub>CC1</sub> = V<sub>CC2</sub> = 1.8 V ±5% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITION	S	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6740							
	$V_I = V_{CC1}$ (1)(ISO6740); $V_I = 0$ V (ISO	06740 with F	I <sub>CC1</sub>		1.2	1.8	
Supply current - DC signal (2)  Supply current - AC signal (3)  SO6741  Supply current - DC signal (2)  Supply current - AC signal (3)	suffix)		I <sub>CC2</sub>		2	3.4	
signal <sup>(2)</sup>	V. = 0 V (ISO6740): V. = V (ISO6	740 with F suffix)	I <sub>CC1</sub>		5.1	1.8 3.4 7.6 3.7 4.7 3.7 4.8 4.6 5.1 8.9 2.4 3.4 6.9 5 4.7 4.3 5 5 6.3 8.3	
	$V_I = 0 \text{ V (ISO6740)}; V_I = V_{CC1} \text{ (ISO6740 with F suffix)} \frac{ V_I }{ V_{CC2} }$		I <sub>CC2</sub>		2 3.4 5.1 7.6 2.2 3.7 3.1 4.7 2.2 3.7 3.2 4.8 3.1 4.6 3.4 5.1 7 8.9 1.5 2.4 2 3.4 4.5 6.9 3.2 5 3.1 4.7 2.7 4.3 3.3 5 3.4 5		
		1 Mbps	I <sub>CC1</sub>		3.1	4.7	mA
		1 Mbps	I <sub>CC2</sub>		2.2	3.7	ША
Supply current - AC	All channels switching with square wave clock input; C <sub>L</sub> = 15 pF	10 Mbps	I <sub>CC1</sub>		3.2	4.8	
signal <sup>(3)</sup>		TO MIDPS	I <sub>CC2</sub>	,	3.1	4.6	
		50 Mbps	I <sub>CC1</sub>		3.4	5.1	
		30 Minhs	I <sub>CC2</sub>		7	8.9	
ISO6741							
Supply current - DC signal	V <sub>I</sub> = V <sub>CCI</sub> <sup>(1)</sup> (ISO6741); V <sub>I</sub> = 0 V (ISO6741 with F suffix)		I <sub>CC1</sub>		1.5	2.4	
	V <sub>1</sub> = V <sub>CC1</sub> (V <sub>1</sub> (1506741), V <sub>1</sub> = 0 V (150	00741 WILLI F SUIIIX)	I <sub>CC2</sub>		2	3.4	
(2)	V = 0 V (ISO6741); V = V (ISO6	744 with Fouffix	I <sub>CC1</sub>		4.5	3.1 4.6 3.4 5.1 7 8.9 1.5 2.4 2 3.4 4.5 6.9 3.2 5 3.1 4.7 2.7 4.3 3.3 5	
	$V_{I} = 0 \text{ V (ISO6741)}; V_{I} = V_{CCI} (ISO6741);$	741 WILLI F SUIIIX)	I <sub>CC2</sub>		3.2		
		1 Mbno	I <sub>CC1</sub>		3.1	4.7	m 1
		1 Mbps	I <sub>CC2</sub>		2.7	2.4 3.4 6.9 5 4.7 4.3 5	mA
Supply current - AC signal	All channels switching with square	40 Mb = =	I <sub>CC1</sub>		3.3	5	
(3)	wave clock input; C <sub>L</sub> = 15 pF	10 Mbps	I <sub>CC2</sub>		3.4	5	
		50 Mb a c	I <sub>CC1</sub>		4.5	6.3	
		50 Mbps	I <sub>CC2</sub>		6.4	8.3	
ISO6742						1	
Supply current - DC	V <sub>I</sub> = V <sub>CCI</sub> <sup>(1)</sup> (ISO6742); V <sub>I</sub> = 0 V (ISC	06742 with F suffix)	I <sub>CC1</sub> , I <sub>CC2</sub>		1.9	3.1	
signal <sup>(2)</sup>	V <sub>I</sub> = 0 V (ISO6742); V <sub>I</sub> = V <sub>CCI</sub> (ISO67	742 with F suffix)	I <sub>CC1</sub> , I <sub>CC2</sub>	,	4	6.1	
		1 Mbps	I <sub>CC1</sub> , I <sub>CC2</sub>		3	4.7	mA
Supply current - AC signal <sup>(3)</sup>	All channels switching with square wave clock input; $C_L = 15 \text{ pF}$	10 Mbps	I <sub>CC1</sub> , I <sub>CC2</sub>		3.5	5.2	
Signal • /	wave clock input, or = 10 pr	50 Mbps	I <sub>CC1</sub> , I <sub>CC2</sub>		5.6	7.6	

 <sup>(1)</sup> V<sub>CCI</sub> = Input-side V<sub>CC</sub>
 (2) Supply current valid for ENx = V<sub>CCx</sub> and ENx = 0V
 (3) Supply current valid for ENx = V<sub>CCx</sub>



## 7.17 Switching Characteristics—5-V Supply

V<sub>CC1</sub> = V<sub>CC2</sub> = 5 V ±10% (over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay time	@100kbps		11	18	ns
PWD	Pulse width distortion <sup>(1)</sup>  t <sub>PHL</sub> - t <sub>PLH</sub>	See Figure 8-1		0.2	7	ns
t <sub>sk(o)</sub>	Channel-to-channel output skew time <sup>(2)</sup>	Same-direction channels			6	ns
t <sub>sk(pp)</sub>	Part-to-part skew time <sup>(3)</sup>				6	ns
t <sub>r</sub>	Output signal rise time	See Figure 9.4	8-1 11 18 8-1 0.2 7 tion channels 6 8-1 2.6 4.5 8-1 2.6 4.5 18.6 25.8 18.6 25.8 18.6 25.8 14.2 21.1 14.2 21.1 14.2 21.1 16 300 rom the time VCC goes See Figure 8-3	ns		
t <sub>f</sub>	Output signal fall time	See Figure 6-1		4.5	ns	
t <sub>PHZ</sub>	Disable propagation delay, high-to-high impedance output	put		18.6	25.8	ns
t <sub>PLZ</sub>	Disable propagation delay, low-to-high impedance output			18.6	25.8	ns
t <sub>PZH</sub>	Enable propagation delay, high impedance-to-high output for ISO674x	ce output gh output for See Figure 8-2		14.2	21.1	ns
t <sub>PZL</sub>	Enable propagation delay, high impedance-to-low output for ISO674x			14.2	21.1	ns
t <sub>PU</sub>	Time from UVLO to valid output data				300	us
t <sub>DO</sub>	Default output delay time from input power loss	Measured from the time VCC goes below 1.2V. See Figure 8-3		0.1	0.3	us
t <sub>ie</sub>	Time interval error	2 <sup>16</sup> – 1 PRBS data at 50 Mbps		1		ns

<sup>(1)</sup> Also known as pulse skew.

Product Folder Links: ISO6740 ISO6741 ISO6742

<sup>(2)</sup>  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

<sup>(3)</sup> t<sub>sk(pp)</sub> is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 7.18 Switching Characteristics—3.3-V Supply

V<sub>CC1</sub> = V<sub>CC2</sub> = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay time	@100kbps		11	18	ns
PWD	Pulse width distortion <sup>(1)</sup>  t <sub>PHL</sub> - t <sub>PLH</sub>	See Figure 8-1		0.5	7	ns
t <sub>sk(o)</sub>	Channel-to-channel output skew time <sup>(2)</sup>	Same-direction channels			6	ns
t <sub>sk(pp)</sub>	Part-to-part skew time <sup>(3)</sup>				7	ns
t <sub>r</sub>	Output signal rise time	See Figure 9.4	11 18 0.5 7	ns		
t <sub>f</sub>	Output signal fall time	@100kbps	3.2	ns		
t <sub>PHZ</sub>	Disable propagation delay, high-to-high impedance output	ce output ce output gh output for See Figure 8-2		23.2	34.4	ns
t <sub>PLZ</sub>	Disable propagation delay, low-to-high impedance output			23.2	34.4	ns
t <sub>PZH</sub>	Enable propagation delay, high impedance-to-high output for ISO674x			16.6	23	ns
t <sub>PZL</sub>	Enable propagation delay, high impedance-to-low output for ISO674x			16.6	23	ns
t <sub>PU</sub>	Time from UVLO to valid output data				300	us
t <sub>DO</sub>	Default output delay time from input power loss			0.1	0.3	us
t <sub>ie</sub>	Time interval error	2 <sup>16</sup> – 1 PRBS data at 50 Mbps		1		ns

<sup>(1)</sup> Also known as pulse skew.

<sup>(2)</sup>  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

<sup>(3)</sup>  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.



## 7.19 Switching Characteristics—2.5-V Supply

 $V_{CC1} = V_{CC2} = 2.5 \text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay time	@100kbps		12	20.5	ns
PWD	Pulse width distortion <sup>(1)</sup>  t <sub>PHL</sub> - t <sub>PLH</sub>	See Figure 8-1		0.6	7.1	ns
t <sub>sk(o)</sub>	Channel-to-channel output skew time <sup>(2)</sup>	Same-direction channels			6	ns
t <sub>sk(pp)</sub>	Part-to-part skew time <sup>(3)</sup>				7	ns
t <sub>r</sub>	Output signal rise time	Con Firmer 0.4		2	4	ns
t <sub>f</sub>	Output signal fall time	See Figure 8-1		2	4	ns
t <sub>PHZ</sub>	Disable propagation delay, high-to-high impedance output			28.1	43	ns
t <sub>PLZ</sub>	Disable propagation delay, low-to-high impedance output			28.1	43	ns
t <sub>PZH</sub>	Enable propagation delay, high impedance-to-high output for ISO674x	See Figure 8-2		20.4	36.3	ns
t <sub>PZL</sub>	Enable propagation delay, high impedance-to-low output for ISO674x			20.4	36.3	ns
t <sub>PU</sub>	Time from UVLO to valid output data				300	us
t <sub>DO</sub>	Default output delay time from input power loss	Measured from the time VCC goes below 1.2V. See Figure 8-3		0.1	0.3	us
t <sub>ie</sub>	Time interval error	2 <sup>16</sup> – 1 PRBS data at 50 Mbps		1		ns

<sup>(1)</sup> Also known as pulse skew.

Product Folder Links: ISO6740 ISO6741 ISO6742

<sup>(2)</sup>  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

<sup>(3)</sup>  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

# 7.20 Switching Characteristics—1.8-V Supply

V<sub>CC1</sub> = V<sub>CC2</sub> = 1.8 V ±5% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay time	@100kbps		15	24	ns
PWD	Pulse width distortion <sup>(1)</sup>  t <sub>PHL</sub> - t <sub>PLH</sub>	See Figure 8-1		0.7	8.2	ns
t <sub>sk(o)</sub>	Channel-to-channel output skew time <sup>(2)</sup>	Same-direction channels			6	ns
t <sub>sk(pp)</sub>	Part-to-part skew time <sup>(3)</sup>				8.8	ns
t <sub>r</sub>	Output signal rise time	Con Figure 9.4		2.7	5.3	ns
t <sub>f</sub>	Output signal fall time	See Figure 8-1		2.7	5.3	ns
t <sub>PHZ</sub>	Disable propagation delay, high-to-high impedance output			40.3	63	ns
t <sub>PLZ</sub>	Disable propagation delay, low-to-high impedance output			40.3	63	ns
t <sub>PZH</sub>	Enable propagation delay, high impedance-to-high output for ISO674x	See Figure 8-2		30	51.4	ns
t <sub>PZL</sub>	Enable propagation delay, high impedance-to-low output for ISO674x			30	51.4	ns
t <sub>PU</sub>	Time from UVLO to valid output data				300	us
t <sub>DO</sub>	Default output delay time from input power loss	Measured from the time VCC goes below 1.2V. See Figure 8-3		0.1	0.3	us
t <sub>ie</sub>	Time interval error	2 <sup>16</sup> – 1 PRBS data at 50 Mbps		1		ns

<sup>(1)</sup> Also known as pulse skew.

<sup>(2)</sup>  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

<sup>(3)</sup>  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.



## 7.21 Insulation Characteristics Curves

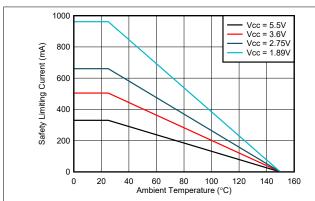


Figure 7-1. Thermal Derating Curve for Safety Limiting Current for DW-16 Package

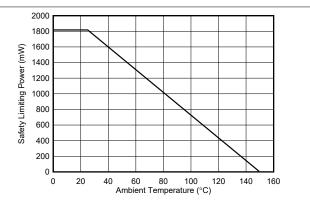
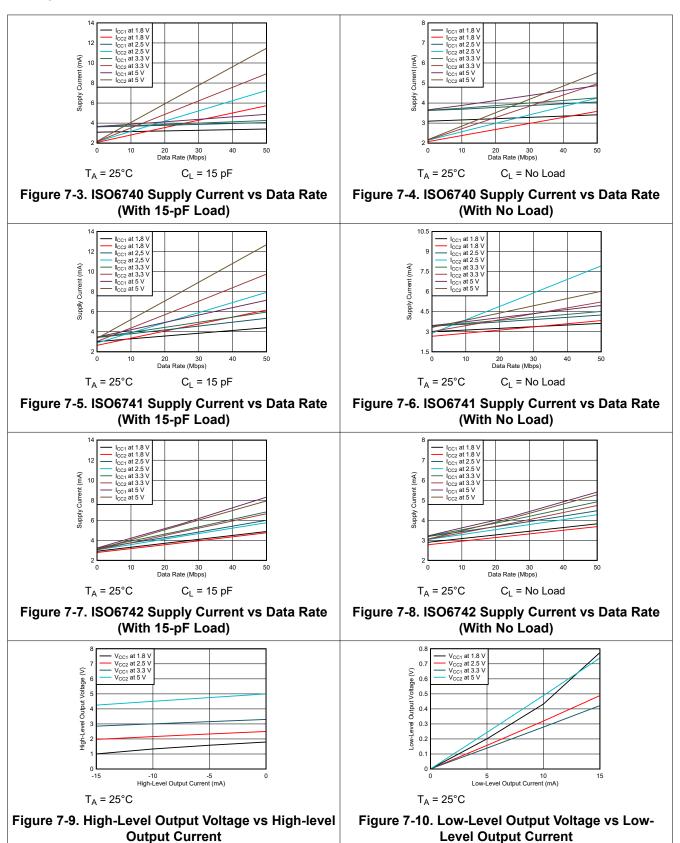


Figure 7-2. Thermal Derating Curve for Safety Limiting Power for DW-16 Package



### 7.22 Typical Characteristics





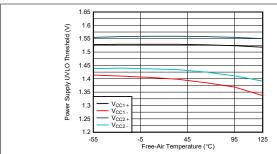


Figure 7-11. Power Supply Undervoltage Threshold vs Free-Air Temperature

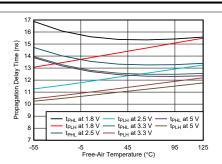
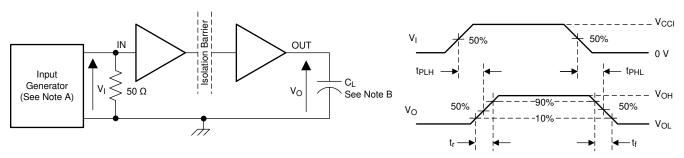


Figure 7-12. Propagation Delay Time vs Free-Air Temperature

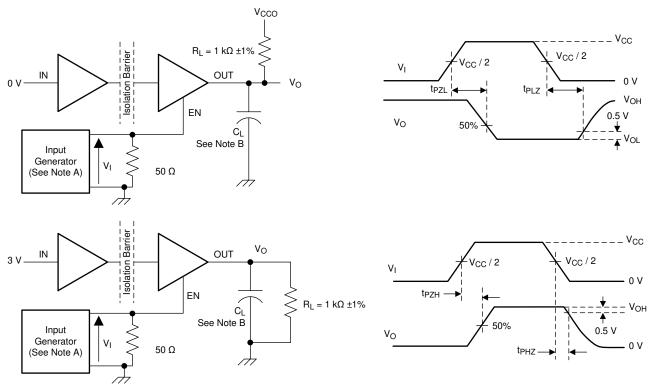
## **8 Parameter Measurement Information**



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- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  50 kHz, 50% duty cycle,  $t_r \leq$  3 ns,  $t_f \leq$  3ns,  $Z_O =$  50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.
- B.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within ±20%.

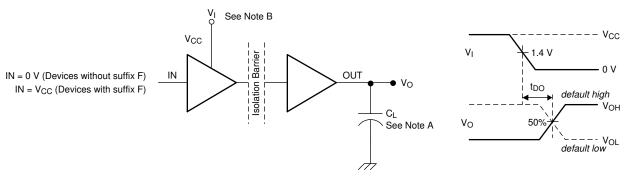
Figure 8-1. Switching Characteristics Test Circuit and Voltage Waveforms



- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  10 kHz, 50% duty cycle,  $t_r \leq$  3 ns,  $t_f \leq$  3 n
- B. C<sub>L</sub> = 15 pF and includes instrumentation and fixture capacitance within ±20%.

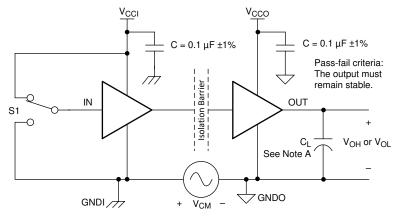
Figure 8-2. Enable/Disable Propagation Delay Time Test Circuit and Waveform





- C<sub>L</sub> = 15 pF and includes instrumentation and fixture capacitance within ±20%.
- B. Power Supply Ramp Rate = 10 mV/ns

Figure 8-3. Default Output Delay Time Test Circuit and Voltage Waveforms



A.  $C_L = 15 \text{ pF}$  and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

Figure 8-4. Common-Mode Transient Immunity Test Circuit

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## 9 Detailed Description

#### 9.1 Overview

The ISO674x family of devices have an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. If the ENx pin is low then the output goes to high impedance. The ISO674x devices also incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 9-1, shows a functional block diagram of a typical channel.

## 9.2 Functional Block Diagram

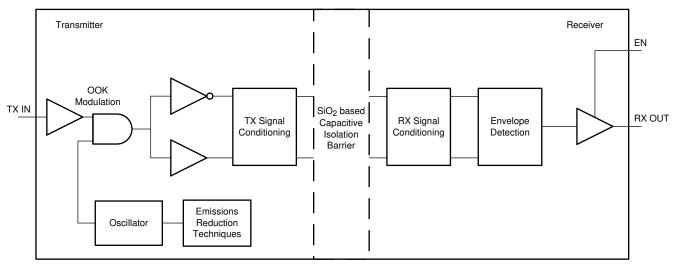


Figure 9-1. Conceptual Block Diagram of a Digital Capacitive Isolator

Figure 9-2 shows a conceptual detail of how the ON-OFF keying scheme works.

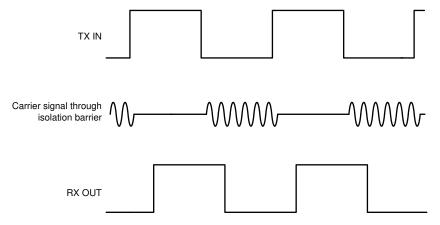


Figure 9-2. On-Off Keying (OOK) Based Modulation Scheme



### 9.3 Feature Description

Table 9-1 provides an overview of the device features.

**Table 9-1. Device Features** 

PART NUMBER	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT	PACKAGE	RATED ISOLATION(1)
ISO6740	4 Forward, 0 Reverse	50 Mbps	High	DW-16	5000 V <sub>RMS</sub> / 8000 V <sub>PK</sub>
ISO6740F	4 Forward, 0 Reverse	50 Mbps	Low	DW-16	5000 V <sub>RMS</sub> / 8000 V <sub>PK</sub>
ISO6741	3 Forward, 1 Reverse	50 Mbps	High	DW-16	5000 V <sub>RMS</sub> / 8000 V <sub>PK</sub>
ISO6741F	3 Forward, 1 Reverse	50 Mbps	Low	DW-16	5000 V <sub>RMS</sub> / 8000 V <sub>PK</sub>
ISO6742	2 Forward, 2 Reverse	50 Mbps	High	DW-16	5000 V <sub>RMS</sub> / 8000 V <sub>PK</sub>
ISO6742F	2 Forward, 2 Reverse	50 Mbps	Low	DW-16	5000 V <sub>RMS</sub> / 8000 V <sub>PK</sub>

<sup>(1)</sup> See Safety-Related Certifications for detailed isolation ratings.

### 9.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 32. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO674x family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- · Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

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#### 9.4 Device Functional Modes

Table 9-2 lists the functional modes for the ISO674x devices.

Table 9-2. Function Table

Table 9 2.1 diletter Table						
V <sub>CCI</sub> <sup>(1)</sup>	V <sub>cco</sub>	INPUT (INx) <sup>(3)</sup>	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)	COMMENTS	
		Н	H or open	Н	Normal Operation: A channel output assumes the logic state of its	
5	5	L	H or open	L	input.	
PU	PU	Open	H or open	Default	Default mode: When INx is open, the corresponding channel output goes to its default logic state. Default is <i>High</i> for ISO674x and <i>Low</i> for ISO674x with F suffix.	
Х	PU	X	L	Z	A low value of output enable causes the outputs to be high-impedance.	
PD	PU	x	H or open	Default	Default mode: When $V_{\rm CCI}$ is unpowered, a channel output assumes the logic state based on the selected default option. Default is High for ISO674x and Low for ISO674x with F suffix. When $V_{\rm CCI}$ transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When $V_{\rm CCI}$ transitions from powered-up to unpowered, channel output assumes the selected default state.	
Х	PD	х	х	Undetermined	When $V_{\rm CCO}$ is unpowered, a channel output is undetermined <sup>(2)</sup> . When $V_{\rm CCO}$ transitions from unpowered to powered-up, a channel output assumes the logic state of the input.	

- $V_{CCI}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$ ; PU = Powered up ( $V_{CC} \ge 1.71 \text{ V}$ ); PD = Powered down ( $V_{CC} \le 1.05 \text{ V}$ ); X = Irrelevant; H = High level; L = Low level ; Z = High Impedance
- The outputs are in undetermined state when 1.89 V <  $V_{CCI}$ ,  $V_{CCO}$  < 2.25 V and 1.05 V <  $V_{CCI}$ ,  $V_{CCO}$  < 1.71 V A strongly driven input signal can weakly power the floating  $V_{CC}$  through an internal protection diode and cause undetermined output

### 9.4.1 Device I/O Schematics

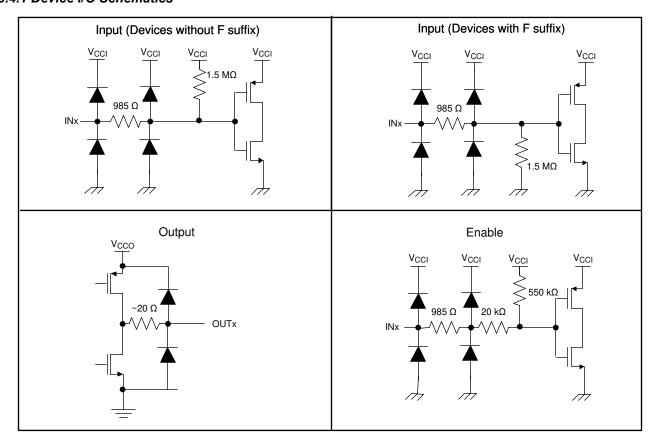


Figure 9-3. Device I/O Schematics

## 10 Application and Implementation

#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The ISO674x devices are high-performance, quad-channel digital isolators. These devices come with enable pins on each side which can be used to put the respective outputs in high impedance for multi master driving applications. The ISO674x devices use single-ended CMOS-logic switching technology. The supply voltage range is from 1.71 V to 5.5 V for both supplies,  $V_{\rm CC1}$  and  $V_{\rm CC2}$ . Since an isolation barrier separates the two sides, each side can be sourced independently with any voltage within recommended operating conditions. As an example, it is possible to supply ISO674x  $V_{\rm CC1}$  with 3.3 V (which is within 1.71 V to 5.5 V) and  $V_{\rm CC2}$  with 5V (which is also within 1.71 V to 5.5 V). You can use the digital isolator as a logic-level translator in addition to providing isolation. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, MCU or FPGA), and a data converter or a line transceiver, regardless of the interface type or standard.

### 10.2 Typical Application

Figure 10-1 shows the isolated serial peripheral interface (SPI).

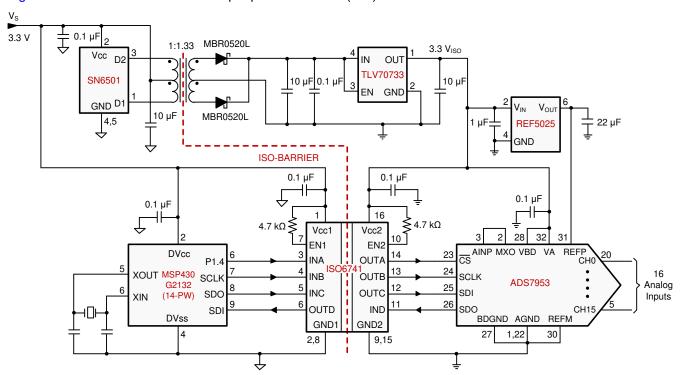


Figure 10-1. Isolated SPI for an Analog Input Module With 16 Inputs



## 10.2.1 Design Requirements

To design with these devices, use the parameters listed in Table 10-1.

Table 10-1. Design Parameters

PARAMETER	VALUE
Supply voltage, V <sub>CC1</sub> and V <sub>CC2</sub>	1.71 V to 1.89 V and 2.25 V to 5.5 V
Decoupling capacitor between V <sub>CC1</sub> and GND1	0.1 μF
Decoupling capacitor from V <sub>CC2</sub> and GND2	0.1 μF

## 10.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO674x family of devices only require two external bypass capacitors to operate.

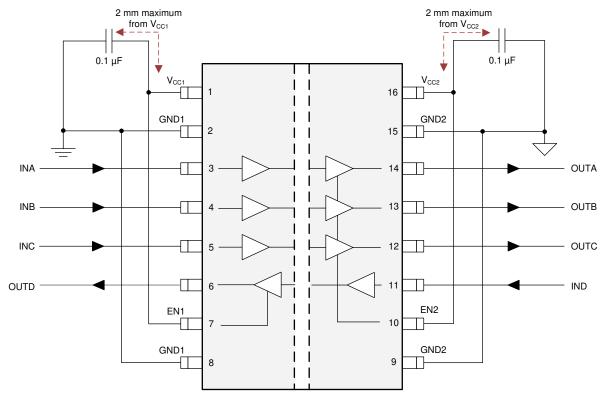
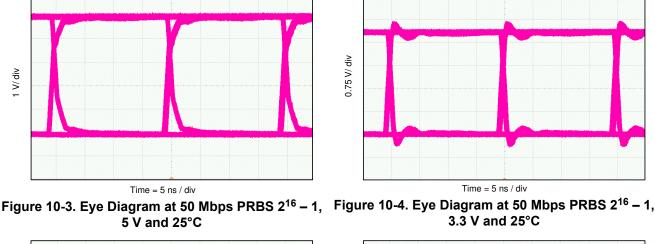


Figure 10-2. Typical ISO674x Circuit Hook-up



#### 10.2.3 Application Curve

The following typical eye diagrams of the ISO674x family of devices indicates low jitter and wide open eye at the maximum data rate of 50 Mbps.



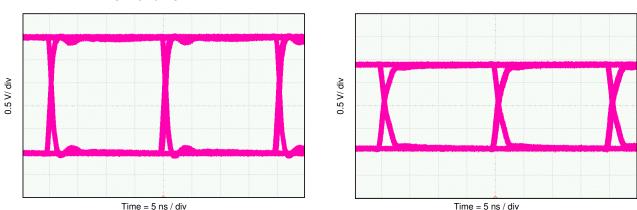


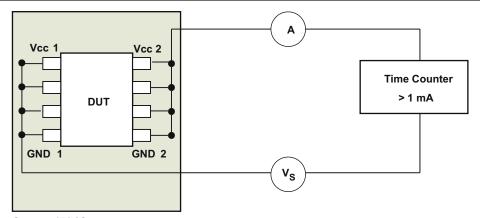
Figure 10-5. Eye Diagram at 50 Mbps PRBS  $2^{16}$  – 1, Figure 10-6. Eye Diagram at 50 Mbps PRBS  $2^{16}$  – 1, 2.5 V and 25°C 1.8 V and 25°C

#### 10.2.3.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See Figure 10-7 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that's 20% higher than the specified value.

Figure 10-8 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1500  $V_{RMS}$  with a lifetime of 36 years. Other factors, such as package size, pollution degree, material group, etc. can further limit the working voltage of the component. The working voltage of DW-16 package is specified upto 1500  $V_{RMS}$ . At the lower working voltages, the corresponding insulation lifetime is much longer than 36 years.





Oven at 150 °C

Figure 10-7. Test Setup for Insulation Lifetime Measurement

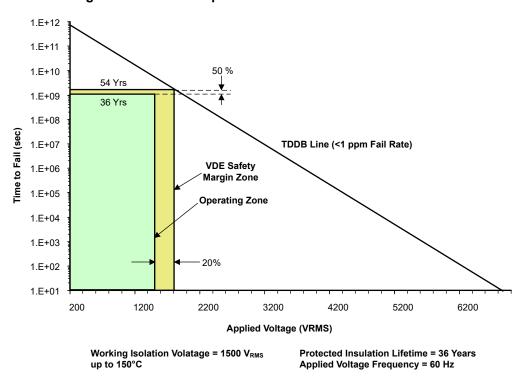


Figure 10-8. Insulation Lifetime Projection Data



## 11 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1- $\mu$ F bypass capacitor is recommended at the input and output supply pins ( $V_{CC1}$  and  $V_{CC2}$ ). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver. For industrial applications, please use Texas Instruments' SN6501 or SN6505B. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 Transformer Driver for Isolated Power Supplies or SN6505B-Q1 Low-noise, 1-A Transformer Drivers for Isolated Power Supplies .

# 12 Layout

## 12.1 Layout Guidelines

A minimum of two layers is required to accomplish a cost optimized and low EMI PCB design. To further improve EMI, a four layer board can be used (see Figure 12-2). Layer stacking for a four layer board should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch<sup>2</sup>.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the Digital Isolator Design Guide.

#### 12.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit boards. This PCB is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and self-extinguishing flammability-characteristics.

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# 12.2 Layout Example

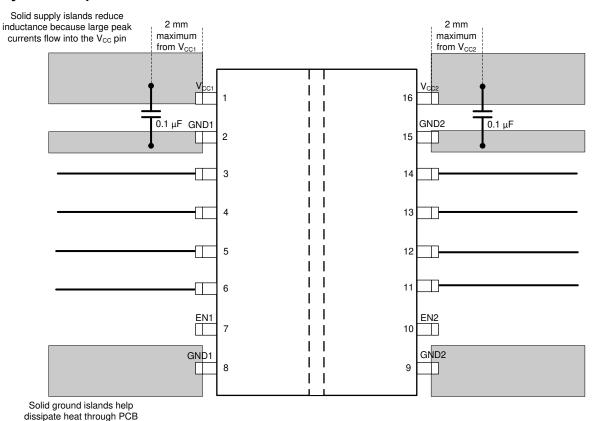


Figure 12-1. Layout Example

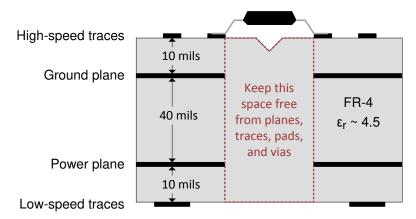


Figure 12-2. Layout Example Schematic

Submit Document Feedback

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# 13 Device and Documentation Support

## 13.1 Documentation Support

#### 13.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, Digital Isolator Design Guide
- · Texas Instruments, Digital Isolator Design Guide
- Texas Instruments, Isolation Glossary
- Texas Instruments, How to use isolation to improve ESD, EFT, and Surge immunity in industrial systems application report
- Texas Instruments, ADS79xx 12/10/8-Bit, 1 MSPS, 16/12/8/4-Channel, Single-Ended, MicroPower, Serial Interface ADCs data sheet
- Texas Instruments, DAC161P997 Single-Wire 16-bit DAC for 4- to 20-mA Loops data sheet
- Texas Instruments, MSP430G2132Mixed Signal Microcontroller data sheet
- Texas Instruments, SN6501 Transformer Driver for Isolated Power Supplies data sheet
- Texas Instruments, TPS76333Low-Power 150-mA Low-Dropout Linear Regulators data sheet

# 13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 13.3 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 13.4 Trademarks

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# 13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 13.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

# 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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#### PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
ISO6740DWR	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6740
ISO6740DWR.A	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6740
ISO6740DWR.B	Active	Production	SOIC (DW)   16	2000   LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISO6740FDWR	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6740F
ISO6740FDWR.A	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6740F
ISO6740FDWR.B	Active	Production	SOIC (DW)   16	2000   LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISO6741DWR	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6741
ISO6741DWR.A	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6741
ISO6741DWR.B	Active	Production	SOIC (DW)   16	2000   LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISO6741FDWR	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6741F
ISO6741FDWR.A	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6741F
ISO6741FDWR.B	Active	Production	SOIC (DW)   16	2000   LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISO6742DWR	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6742
ISO6742DWR.A	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6742
ISO6742DWR.B	Active	Production	SOIC (DW)   16	2000   LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISO6742FDWR	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6742F
ISO6742FDWR.A	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6742F
ISO6742FDWR.B	Active	Production	SOIC (DW)   16	2000   LARGE T&R	-	Call TI	Call TI	-40 to 125	

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

# **PACKAGE OPTION ADDENDUM**

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(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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#### OTHER QUALIFIED VERSIONS OF ISO6740, ISO6741, ISO6742:

Automotive: ISO6740-Q1, ISO6741-Q1, ISO6742-Q1

NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



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## TAPE AND REEL INFORMATION



# TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO6740DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6740FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6741DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6741DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6741FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6741FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6742DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6742DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6742FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6742FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1



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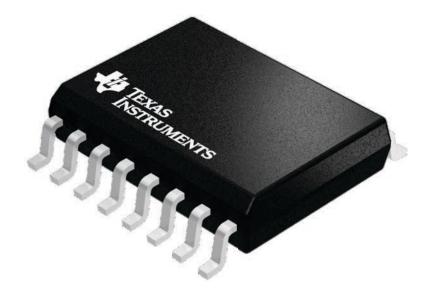
\*All dimensions are nominal

	Annother and the first that									
Device	Package Type	Package Drawing	Pins SPQ		Length (mm)	Width (mm)	Height (mm)			
ISO6740DWR	SOIC	DW	16	2000	353.0	353.0	32.0			
ISO6740FDWR	SOIC	DW	16	2000	353.0	353.0	32.0			
ISO6741DWR	SOIC	DW	16	2000	356.0	356.0	45.0			
ISO6741DWR	SOIC	DW	16	2000	353.0	353.0	32.0			
ISO6741FDWR	SOIC	DW	16	2000	356.0	356.0	45.0			
ISO6741FDWR	SOIC	DW	16	2000	353.0	353.0	32.0			
ISO6742DWR	SOIC	DW	16	2000	353.0	353.0	32.0			
ISO6742DWR	SOIC	DW	16	2000	356.0	356.0	45.0			
ISO6742FDWR	SOIC	DW	16	2000	353.0	353.0	32.0			
ISO6742FDWR	SOIC	DW	16	2000	356.0	356.0	45.0			

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





SOIC



## NOTES:

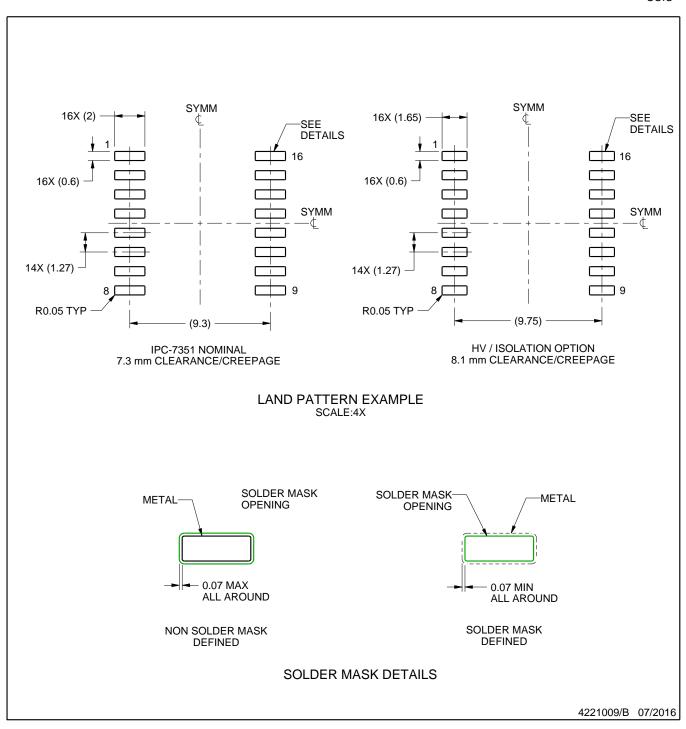
- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
- 5. Reference JEDEC registration MS-013.



SOIC



## NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



#### NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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