







ISO1176T SLLSE28H - OCTOBER 2010 - REVISED AUGUST 2023

# ISO1176T Isolated Profibus RS-485 Transceiver with Integrated Transformer Driver

#### 1 Features

- Meets or Exceeds the Requirements of EN 50170 and TIA/EIA-485-A
- Signaling Rates up to 40 Mbps
- Easy Isolated Power Design with Integrated **Transformer Driver**
- Typical Efficiency > 60% (I<sub>I OAD</sub> = 100 mA) see **SLUU471**
- Differential Output exceeds 2.1 V (54-Ω Load)
- Low Bus Capacitance 10 pF (Maximum)
- Fail-safe Receiver for Bus Open, Short, or Idle
- 50-kV/µs Typical Transient Immunity
- Safety and Regulatory Approvals
  - 4242 V<sub>PK</sub> Basic Insulation per DIN EN IEC 60747-17 (VDE 0884-17)
  - 2500 V<sub>RMS</sub> Isolation for 1 minute per UL 1577
  - CSA 60950-1 and CSA 61010-1 Standards

# 2 Applications

- Profibus®
- **Factory Automation**
- **Networked Sensors**
- Motor/motion Control
- **HVAC** and Building Automation Networks
- **Networked Security Stations**

# 3 Description

The ISO1176T is an isolated differential transceiver with integrated oscillator outputs that provide the primary voltage for an isolation transformer. The device is ideal for long transmission lines because the ground loop is broken to allow the device to operate with a much larger common-mode voltage range.

The symmetrical isolation barrier of each device is tested to provide 4242V<sub>PK</sub> of isolation per VDE for 60 seconds between the line transceiver and the logiclevel interface.

The galvanically isolated differential bus transceiver is an integrated circuit designed for bi-directional data communication on multipoint bus-transmission lines. The transceiver combines a galvanically isolated differential line driver and differential input line receiver. The driver has an active-high enable with isolated enable-state output on the ISODE pin (pin 10) to facilitate direction control. The driver differential outputs and the receiver differential inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or  $V_{CC2} = 0$ .

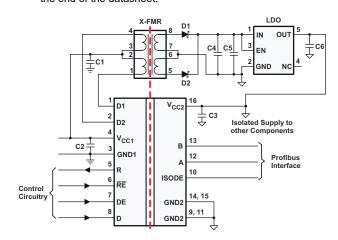
Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the transceiver and/or near-by sensitive circuitry if they are of sufficient magnitude and duration. The ISO1176T can significantly reduce the risk of data corruption and damage to expensive control circuits.

The device is characterized for operation over the ambient temperature range of -40°C to 85°C.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO1176T	SOIC (16)	10.30 mm × 7.50 mm

For all available packages, see the orderable addendum at the end of the datasheet.



**Typical Application** 



# **Table of Contents**

1 Features	
3 Description17 Parameter Measurement Information4 Revision History28 Detailed Description5 Pin Configuration and Functions48.1 Overview	
4 Revision History	
<b>5 Pin Configuration and Functions</b> 4 8.1 Overview	
Pin Functions	23
<b>6 Specifications</b> 8.3 Device Functional Modes	24
6.1 Absolute Maximum Ratings	27
6.2 ESD Ratings	27
6.3 Recommended Operating Conditions	<mark>27</mark>
6.4 Thermal Information	30
6.5 Power Ratings	30
6.6 Insulation Specifications	30
6.7 Safety-Related Certifications	
6.8 Safety Limiting Values	32
6.9 Electrical Characteristics: ISODE-Pin8 12.1 Documentation Support	32
6.10 Electrical Characteristics: Driver	32
6.11 Electrical Characteristics: Receiver9 12.3 Trademarks	32
6.12 Supply Current	32
6.13 Transformer Driver Characteristics	
6.14 Switching Characteristics: Driver	
6.15 Switching Characteristics: Receiver	32
Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations.      Updated electrical and switching characteristics to match device performance.  Changes from Revision E (October 2013) to Revision C (October 2015).	8
<del> </del>	<b>7</b>
<ul> <li>Added Pin Configuration and Functions section, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, La section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information</li> <li>VDE standard changed to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12</li> </ul>	Page
	yout tion 1
Changes from Revision E (August 2011) to Revision F (October 2012)	yout tion 1
<ul> <li>Changes from Revision E (August 2011) to Revision F (October 2012)</li> <li>Changed From "ISO1176T Reference Design SLLU471" To: "ISO1176T Reference Design SLUU471"</li> </ul>	yout tion 1
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# **5 Pin Configuration and Functions**

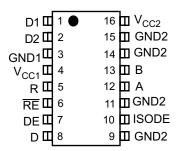


Figure 5-1. DW Package 16-Pin SOIC Top View

#### **Pin Functions**

	PIN	I/O	DESCRIPTION
NAME	NO.	1/0	DESCRIPTION
A	12	I/O	Non-inverting Driver Output / Receiver Input
В	13	I/O	Inverting Driver Output / Receiver Input
D	8	I	Driver Input
D1	1	0	Transformer Driver Terminal 1, Open Drain Output
D2	2	0	Transformer Driver Terminal 2, Open Drain Output
DE	7	I	Driver Enable Input
GND1	3	_	Logic-side Ground
GND2	9, 11, 14, 15	_	Bus-side Ground. All pins are internally connected.
ISODE	10	0	Bus-side Driver Enable Output Status
R	5	0	Receiver Output
RE	6	I	Receiver Enable Input. This pin has complementary logic.
V <sub>CC1</sub>	4	_	Logic-side Power Supply
V <sub>CC2</sub>	16	_	Bus-side Power Supply

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# **6 Specifications**

# **6.1 Absolute Maximum Ratings**

Over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage <sup>(2)</sup>	V <sub>CC1</sub> , V <sub>CC2</sub>	-0.5	6	V
V	Voltage at any bus I/O terminal		-9	14	V
Vo	Voltage at D1, D2			14	V
VI	Voltage input	D, DE or RE	-0.5	6	V
Io	Receiver output current	Receiver output current	-10	10	mA
I <sub>D1</sub> , I <sub>D2</sub>	, I <sub>D2</sub> Transformer Driver Output Current			450	mA
TJ	Junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# 6.2 ESD Ratings

			VALUE	UNIT
		Bus pins and GND1	±6000	V
	Human body model (HBM), per ANSI/ ESDA/JEDEC JS-001 <sup>(1)</sup>	Bus pins and GND2	±10000	V
		All pins	±4000	V
V <sub>(ESD)</sub> Electros tatic Discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>		±1500	V
	Machine model (MM), ANSI/ ESDS5.2-1996		±200	V

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## **6.3 Recommended Operating Conditions**

			MIN	NOM MAX	UNIT
V <sub>CC</sub>	Logic-side supply voltage, V <sub>CC1</sub> (with respect to GND1)		3	5.5	V
V <sub>CC</sub>	Bus-side supply voltage, V <sub>CC2</sub> (with respect to GND2)		4.75	5.25	V
V <sub>CM</sub>	Voltage at either bus I/O terminal	A or B	-7	12	V
V <sub>IH</sub>	High-level input voltage	PV, RE	2	5.5	V
V <sub>IH</sub>	High-level input voltage	D, DE	0.7*V <sub>CC1</sub>		V
V <sub>IL</sub>	Low-level input voltage	PV, RE	0	0.8	V
V <sub>IL</sub>	Low-level input voltage	D, DE		0.3*Vcc	V
V <sub>ID</sub>	Differential input voltage	A with respect to B	-12	12	V
Io	Output current	Driver	-70	70	mA
Io	Output current	Receiver	-8	8	mA
T <sub>A</sub>	Ambient temperature		-40	85	°C

<sup>(2)</sup> All voltage values except differential I/O bus voltages are with respect to the referenced network ground terminal and are peak voltage values.

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



		MIN	NOM	MAX	UNIT
1 / t <sub>UI</sub>	Signaling Rate			40	Mbps



#### **6.4 Thermal Information**

		ISO1176T	
	THERMAL METRIC(1)	DW (SOIC)	UNIT
		16 PINS	
R <sub>0JA</sub>	Junction-to-ambient thermal resistance	76	°C/W
R <sub>0JC(top)</sub>	Junction-to-case (top) thermal resistance	37.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.6	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	13.9	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	37.9	°C/W
R <sub>0JC(bot)</sub>	Junction-to-case (bottom) thermal resistance	-	°C/W

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the no.

# 6.5 Power Ratings

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P <sub>D</sub> Maximum power dissipation (both sides)	$V_{\rm CC1}$ = $V_{\rm CC2}$ = 5.25 V, $T_{\rm J}$ = 150°C, $C_{\rm L}$ = 15 pF, Input at 20 MHz 50% duty cycle square wave			719	mW

# **6.6 Insulation Specifications**

	PARAMETER	TEST CONDITIONS	VALUE	UNIT	
	TANAMETER	1231 GONEMIONS	DW-16		
CLR	External clearance <sup>(1)</sup>	Shortest terminal-to-terminal distance through air	8	mm	
CPG	External creepage <sup>(1)</sup>	Shortest terminal-to-terminal distance across the package surface	8	mm	
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	8	um	
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>400	V	
	Material group	According to IEC 60664-1	П		
	Over 15 to 25 and 25 an	Rated mains voltage ≤ 150 V <sub>RMS</sub>	I-IV		
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V <sub>RMS</sub>	1-111	1	
DIN EN IEC 60747-17 (VDE 0884-17) (2)		'			
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	566	$V_{PK}$	
V <sub>IOTM</sub>	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ , t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$ , t= 1 s (100% production)	4242	V <sub>PK</sub>	
q <sub>pd</sub>	Apparent charge <sup>(3)</sup>	Method b; At routine test (100% production) $V_{ini} = 1.2 \times V_{IOTM}$ , $t_{ini} = 1 \text{ s}$ ; $V_{pd(m)} = 1.5 \times V_{IORM}$ , $t_m = 1 \text{ s}$	≤5	pC	
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(4)</sup>	V <sub>IO</sub> = 0.4 x sin (2πft), f = 1 MHz	2	pF	
Cı	Input capacitance to ground	$V_I = VCC/2 + 0.4 \times \sin(2\pi ft), f = 1 \text{ MHz}, VCC = 5 \text{ V}$	2	pF	
_	Isolation resistance <sup>(4)</sup>	V <sub>IO</sub> = 500 V, T <sub>A</sub> = 25°C	>10 <sup>12</sup>		
R <sub>IO</sub>	Isolation resistance(4)	V <sub>IO</sub> = 500 V, T <sub>S</sub> = 150°C	>10 <sup>9</sup>	Ω	
	Pollution degree		2		
	Climatic category		40/085/21		
UL 1577	,	ı	II.		
V <sub>ISO</sub>	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$ , t = 60 s (qualification), $V_{TEST} = 1.2 \text{ x } V_{ISO}$ , t = 1 s (100% production)	2500	V <sub>RMS</sub>	

<sup>(1)</sup> Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of



the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.

- (2) This coupler is suitable for *basic electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (4) All pins on each side of the barrier tied together creating a two-terminal device.

#### 6.7 Safety-Related Certifications

VDE	CSA	UL
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 60950-1 and IEC 61010-1	Certified according to UL 1577 Component Recognition Program
Basic Insulation Maximum Transient Isolation Voltage, 4242 V <sub>PK</sub> Maximum Surge Isolation Voltage, 4000 V <sub>PK</sub> Maximum repetitive peak isolation Voltage, 566 V <sub>PK</sub>	$3000~V_{RMS}$ Isolation Rating; Reinforced insulation per CSA 61010-1 and IEC 61010-1 150 $V_{RMS}$ working voltage; Basic insulation per CSA 61010-1 and IEC 61010-1 600 $V_{RMS}$ working voltage; Basic insulation per CSA 60950-1 and IEC 60950-1 760 $V_{RMS}$ working voltage	Single protection, 2500 V <sub>RMS</sub>
Certificate number: 40047657	Master contract number: 220991	File number: E181974

### 6.8 Safety Limiting Values

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I <sub>S</sub>	Safety input, output, or supply current	$R_{\theta JA} = 76$ °C/W, $V_I = 5.5$ V, $T_J = 150$ °C, $T_A = 25$ °C,			299	mA
T <sub>S</sub>	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power respectively. The maximum limits of I<sub>S</sub> and P<sub>S</sub> should not be exceeded. These limits vary with the ambient temperature, T<sub>A</sub>.

The junction-to-air thermal resistance, R<sub>BJA</sub>, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

 $T_J = T_A + R_{\theta JA} \times P$ , where P is the power dissipated in the device.

 $T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$ , where  $T_{J(max)}$  is the maximum allowed junction temperature.

 $P_S = I_S \times V_I$ , where  $V_I$  is the maximum input voltage.

#### 6.9 Electrical Characteristics: ISODE-Pin

All typical specs are at V<sub>CC1</sub>=3.3V, V<sub>CC2</sub>=5V, T<sub>A</sub>=27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V	High level output voltage	I <sub>OH</sub> = -8 mA	V <sub>CC2</sub> - 0.8	4.6		V
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -20 μA	V <sub>CC2</sub> – 0.1	5		V
V	Low lovel output voltage	$I_{OL} = -8 \text{ mA}$		0.2	0.4	V
V <sub>OL</sub>	Low-level output voltage	$I_{OL} = -20 \mu A$		0	0.1	V

Product Folder Links: ISO1176T

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#### **6.10 Electrical Characteristics: Driver**

All typical specs are at  $V_{CC1}$ =3.3V,  $V_{CC2}$ =5V,  $T_A$ =27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
V <sub>OD</sub>	Open-circuit differential output voltage	V <sub>A</sub> -V <sub>B</sub>  , Figure 9	1.5	V <sub>CC2</sub>	V
	Steady state differential output voltage magnitude	See Figure 10 and Figure 14	2.1		V
$ V_{OD(SS)} $	Steady state differential output voltage magnitude	Common mode loading with V <sub>test</sub> from -7V to 12V, See figure 10	2.1		V
$\Delta  V_{ODSS} $	Change in differential output voltage between two states	R <sub>L</sub> = 54 ohms, See Figure 12 and Figure 13	-200	200	mV
V <sub>OC(SS)</sub>	Steady state common-mode output voltage	R <sub>L</sub> = 54 ohms, See Figure 12 and Figure 13	2	3	V
$\Delta V_{OC(SS)}$	change in steady-state common-mode output voltage between two states	R <sub>L</sub> = 54 ohms, See Figure 12 and Figure 13	-200	200	mV
V <sub>OC(PP)</sub>	Peak-to-peak common-mode output voltage	R <sub>L</sub> = 54 ohms, See Figure 12 and Figure 13	0.5		V
V <sub>OD(RING)</sub>	Differential output voltage over and undershoot	See Figure 14 and Figure 17		10	%V <sub>OD(PP)</sub>
l <sub>l</sub>	Input current	D, DE at 0 V or V <sub>CC1</sub>	-10	10	μA
I <sub>O(OFF)</sub>	Output current with power off	Vcc <sub>2</sub> = 0 V	See receiver input curren	t	μA
l <sub>oz</sub>	High-impedance state output current	DE at 0 V	See receiver input curren	t	μA
I <sub>OS(P)</sub>	Peak short circuit output current	DE at $V_{CC}$ , See Figure 15 and Figure 16: $V_{OS}$ = -7 to 12 V	-250	250	mA
	Steady state short-circuit output	DE at $V_{CC}$ , See Figure 15 and Figure 16: $V_{OS}$ = 12 V, D at GND1		150	mA
I <sub>OS(SS)</sub>	current	DE at $V_{CC}$ , See Figure 15 and Figure 16: $V_{OS}$ = -7 V, D at $V_{CC1}$	-150		mA
C <sub>OD</sub>	Differential output capacitance		7	18.8	pF
CMTI	Common-mode transient immunity	See Figure 27	25		kV/μs

## 6.11 Electrical Characteristics: Receiver

All typical specs are at  $V_{CC1}$ =3.3V,  $V_{CC2}$ =5V,  $T_A$ =27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>IT+</sub>	Positive-going input threshold voltage	I <sub>O</sub> = -8 mA, See Figure 22		-80	-10	mV
V <sub>IT</sub>	Negative-going input threshold voltage	I <sub>O</sub> = 8 mA, See Figure 22	-200	-120		mV
V <sub>hys</sub>	Input hysteresis (V <sub>IT+</sub> – V <sub>IT-</sub> )			40		mV
V <sub>OH</sub>	Output Voltage	$V_{\rm CC1}$ at 3.3 V and $V_{\rm CC2}$ at 5V, $V_{\rm ID}$ = 200mV, $I_{\rm O}$ = -8mA	V <sub>CC1</sub> -0.4	3		V
V <sub>OH</sub>	Output Voltage	$\rm V_{CC1}$ at 3.3 V and $\rm V_{CC2}$ at 5V, $\rm V_{ID}$ = 200mV, $\rm I_{O}$ = $-20\rm uA$	V <sub>CC1</sub> -0.1	3.3		V
V <sub>OL</sub>	Output Voltage	$\rm V_{CC1}$ at 3.3 V and $\rm V_{CC2}$ at 5V, $\rm V_{ID}$ = -200mV, $\rm I_{O}$ = 8mA		0.2	0.4	V
V <sub>OL</sub>	Output Voltage	$V_{\rm CC1}$ at 3.3 V and $V_{\rm CC2}$ at 5V, $V_{\rm ID}$ = -200mV, $I_{\rm O}$ = 20uA		0	0.1	V
V <sub>OH</sub>	Output Voltage	$V_{\rm CC1}$ at 5 V and $V_{\rm CC2}$ at 5V, $V_{\rm ID}$ = 200mV, $I_{\rm O}$ = -8mA	V <sub>CC1</sub> -0.8	4.6		V
V <sub>OH</sub>	Output Voltage	$V_{\rm CC1}$ at 5 V and $V_{\rm CC2}$ at 5V, $V_{\rm ID}$ = 200mV, $I_{\rm O}$ = -20uA	V <sub>CC1</sub> -0.1	5		V
V <sub>OL</sub>	Output Voltage	$V_{\rm CC1}$ at 5 V and $V_{\rm CC2}$ at 5V, $V_{\rm ID}$ = -200mV, $I_{\rm O}$ = 8mA		0.2	0.4	V
V <sub>OL</sub>	Output Voltage	$V_{\rm CC1}$ at 5 V and $V_{\rm CC2}$ at 5V, $V_{\rm ID}$ = -200mV, $I_{\rm O}$ = 20uA		0	0.1	V



All typical specs are at  $V_{CC1}$ =3.3V,  $V_{CC2}$ =5V,  $T_A$ =27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>A</sub> or I <sub>B</sub>	Bus pin input current	V <sub>I</sub> = -7 V or 12 V, other input = 0V: V <sub>CC</sub> = 4.75 V or 5.25 V			200	μA
		V <sub>I</sub> = -7 V or 12 V, other input = 0V: V <sub>CC2</sub> = 0 V	-160		200	μA
I <sub>I</sub>	Receiver enable input current	RE = 0 V or V <sub>CC1</sub>	-50		50	μA
I <sub>OZ</sub>	High impedance state output current	RE = V <sub>CC1</sub>	-1		1	μA
R <sub>ID</sub>	Differential input resistance	A, B	60			kohm
C <sub>ID</sub>	Differential input capacitance	Test input signal is a 1.5MHz sine wave with $1V_{PP}$ amplitude, $C_D$ is measured across A and B		7	18.8	pF
CMR	Common mode rejection	See Figure 26		4		V

## 6.12 Supply Current

Bus loaded or unloaded (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	YP MAX	UNIT		
DRIVER ENABLE	D, RECEIVER DISABLED					
	$V_{CC1} = 3.3 \text{ V} \pm 10\%$ , DE, $\overline{\text{RE}} = 0\text{V}$ or $V_{CC1}$ , No Load		4.5 8	mA		
ICC1 \ /	V <sub>CC1</sub> = 5 V ± 10%, DE, RE = 0V or V <sub>CC1</sub> , No Load					
I <sub>CC2</sub> <sup>(1)</sup>	$V_{CC2} = 5 \text{ V} \pm 5\%$ , DE, $\overline{RE} = 0 \text{V}$ or $V_{CC1}$ , No Load		3.5 18	mA		

I<sub>CC1</sub> and I<sub>CC2</sub> are measured when device is connected to external power supplies. D1 and D2 are disconnected from external transformer.

## **6.13 Transformer Driver Characteristics**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>osc</sub>	Oscillator frequency	V <sub>CC1</sub> = 5 V ± 10%, D1 and D2 connected to transformer	350	450	610	kHz
	Oscillator frequency	V <sub>CC1</sub> = 3.3 V ± 10%, D1 and D2 connected to transformer	300	400	550	kHz
R <sub>ON</sub>	Switch on resistance	D1 and D2 connected to 50Ω pullup resistors		1	2.5	ohm
t <sub>r_D</sub>	D4 D2 cutout vice time	V <sub>CC1</sub> = 5 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		80		ns
	D1, D2 output rise time	$V_{CC1}$ = 3.3 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		70		ns
t <sub>f_D</sub>	D1, D2 output fall time	V <sub>CC1</sub> = 5 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		55		ns
<u>-</u>	D1, D2 output fail time	$V_{CC1}$ = 3.3 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		80		ns
f <sub>St</sub>	Startup frequency	V <sub>CC1</sub> = 2.4 V, D1 and D2 connected to transformer		350		kHz
t <sub>BBM</sub>	Break before make time delay	V <sub>CC1</sub> = 5 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		38		ns
	break before make time delay	$V_{CC1}$ = 3.3 V ± 10%, See Figure 28, D1 and D2 connected to 50-Ω pullup resistors		140		ns



# 6.14 Switching Characteristics: Driver

All typical specs are at  $V_{CC1}$ =3.3V,  $V_{CC2}$ =5V,  $T_A$ =27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO1176						
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation delay	V <sub>CC1</sub> at 5 V, <sub>VCC2</sub> at 5 V		23	35	ns
tsk(p)	Pulse skew ( t <sub>PHL</sub> - t <sub>PLH</sub>  )	V <sub>CC1</sub> at 5 V, <sub>VCC2</sub> at 5 V		2	7.5	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation delay	V <sub>CC1</sub> at 3.3 V, V <sub>CC2</sub> at 5 V			40	ns
tsk(p)	Pulse skew ( t <sub>PHL</sub> - t <sub>PLH</sub>  )	V <sub>CC1</sub> at 3.3 V, V <sub>CC2</sub> at 5 V		2	7.5	ns
t <sub>r</sub> , t <sub>f</sub>	Differential output rise time and fall time	See Figure 17	2	3	7.5	ns
t <sub>pDE</sub>	DE to ISODE prop delay	See Figure 21			30	ns
t <sub>t(MLH)</sub> , t <sub>t(MHL)</sub>	Output transition skew	See Figure 18			1	ns
t <sub>P(AZH)</sub> , t <sub>P(BZH)</sub> , t P(AZL), t <sub>P(BZL)</sub>	Propagation delay, high-impedance-to-active output	$C_L$ = 50 pF, $\overline{RE}$ at 0 V, See Fgure 19 and Figure 20			80	ns
t <sub>P(AHZ)</sub> , t <sub>P(BHZ)</sub> , t P(ALZ), t <sub>P(BLZ)</sub>	Propagation delay time, active-to-high-impedance output	$C_L$ = 50 pF, $\overline{RE}$ at 0 V, See Fgure 19 and Figure 20			80	ns
$\begin{aligned}  t_{P(AZL)} - \\ t_{P(BZH)} ,   \\ t_{P(AZH)} - \\ t_{P(BZL)}  \end{aligned}$	Enable skew time	$C_L$ = 50 pF, $\overline{RE}$ at 0 V, See Fgure 19 and Figure 20		0.55	1.5	ns
t <sub>(CFB)</sub>	Time from application of short-circuit to current foldback	See Figure 16		0.5		μs
t <sub>(TSD)</sub>	Time from application of short-circuit to thermal shutdown	T <sub>A</sub> = 25°C, See Figure 16	100			μs

# 6.15 Switching Characteristics: Receiver

All typical specs are at  $V_{CC1}$ =3.3V,  $V_{CC2}$ =5V,  $T_A$ =27°C, (Min/Max specs are over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO1176					-	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation delay	V <sub>CC1</sub> at 5 V, V <sub>CC2</sub> at 5 V			50	ns
tsk(p)	Pulse skew ( t <sub>PHL</sub> - t <sub>PLH</sub>  )	V <sub>CC1</sub> at 5 V, V <sub>CC2</sub> at 5 V		2	7.5	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation delay	V <sub>CC1</sub> at 3.3 V, V <sub>CC2</sub> at 5 V			55	ns
tsk(p)	Pulse skew ( t <sub>PHL</sub> - t <sub>PLH</sub>  )	V <sub>CC1</sub> at 3.3 V, V <sub>CC2</sub> at 5 V		2	7.5	ns
t <sub>r</sub> , t <sub>f</sub>	Differential output rise time and fall time	See Figure 17		2	4	ns
t <sub>PZH</sub>	Propagation delay time, high-impedance-to-high-level output	DE at V <sub>CC1</sub> , See Figure 24		13	25	ns
t <sub>PHZ</sub>	Propagation delay time, high-level-to- high-impedance output	DE at V <sub>CC1</sub> , See Figure 24		13	25	ns
t <sub>PZL</sub>	Propagation delay time, high-impedance-to-low-level output	DE at V <sub>CC</sub> , See Figure 25		13	25	ns
t <sub>PLZ</sub>	Propagation delay time, low-level-to-high-impedance output	DE at V <sub>CC</sub> , See Figure 25		13	25	ns

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# **6.16 Insulation Characteristics Curves**

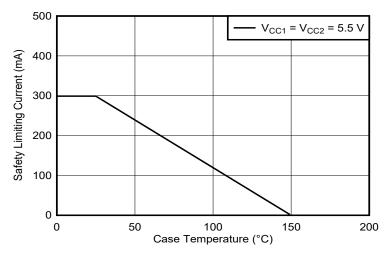


Figure 6-1. Thermal Derating Curve for Safety Limiting Power for DW-16 Package



### 6.17 Typical Characteristics

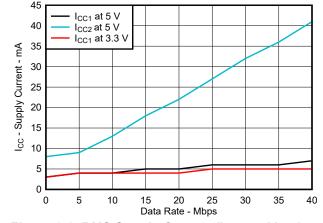


Figure 6-2. RMS Supply Current (I<sub>CC1</sub> and I<sub>CC2</sub>) vs Signaling Rate With No Load

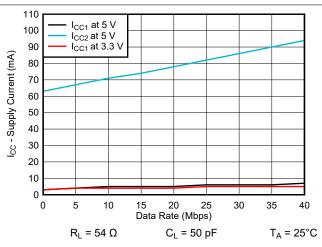


Figure 6-3. RMS Supply Current (I<sub>CC1</sub> and I<sub>CC2</sub>) vs Signaling Rate With Load

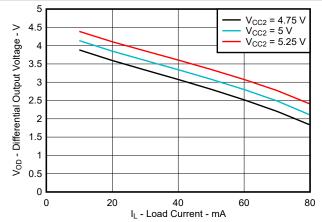


Figure 6-4. Differential Output Voltage vs Load Current

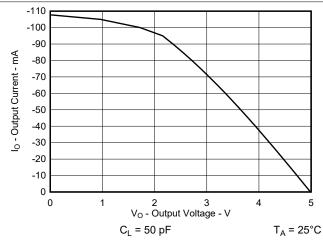


Figure 6-5. Receiver High-Level Output Voltage Vs High-Level Output Current

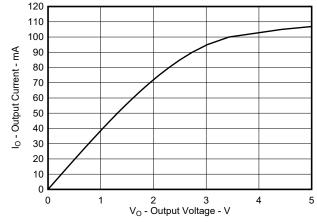


Figure 6-6. Receiver Low-Level Output Voltage vs Low-Level Output Current

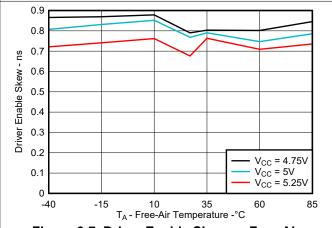
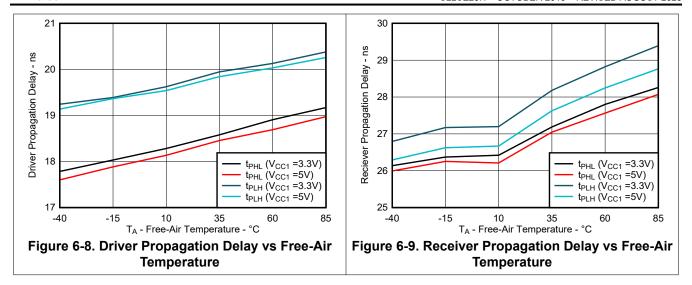


Figure 6-7. Driver Enable Skew vs Free-Air Temperature

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# 7 Parameter Measurement Information

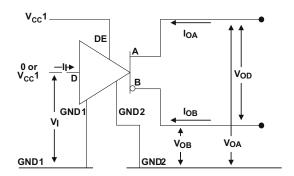


Figure 7-1. Open Circuit Voltage Test Circuit



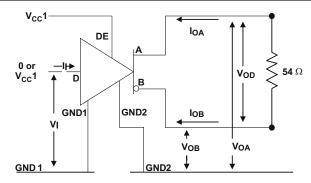


Figure 7-2.  $V_{\text{OD}}$  Test Circuit

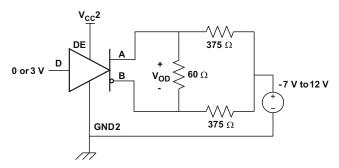


Figure 7-3. Driver  $V_{\text{OD}}$  with Common-mode Loading Test Circuit



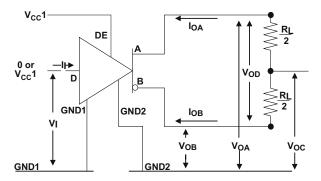


Figure 7-4. Driver  $V_{\text{OD}}$  and  $V_{\text{OC}}$  Without Common-Mode Loading Test Circuit

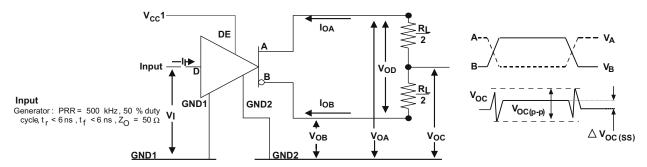


Figure 7-5. Steady-State Output Voltage Test Circuit and Voltage Waveforms

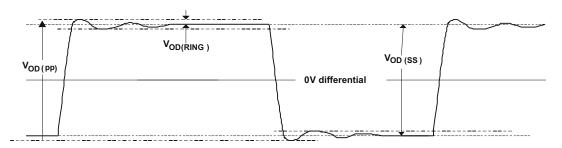


Figure 7-6. V<sub>OD(RING)</sub> Waveform and Definitions

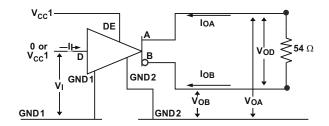


Figure 7-7. Input Voltage Hysteresis Test Circuit

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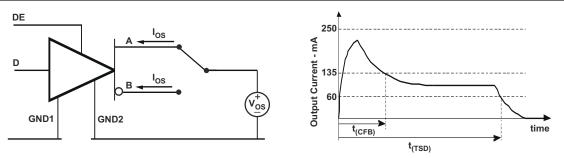


Figure 7-8. Driver Short-Circuit Test Circuit and Waveforms (Short Circuit applied at Time t=0)

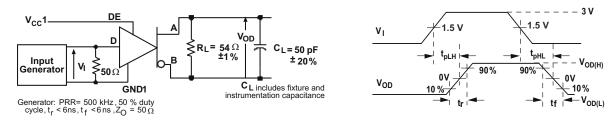


Figure 7-9. Driver Switching Test Circuit and Waveforms

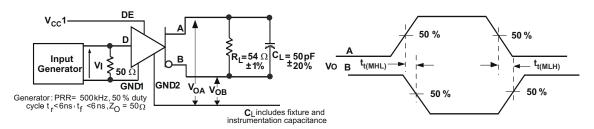


Figure 7-10. Driver Output Transition Skew Test Circuit and Waveforms

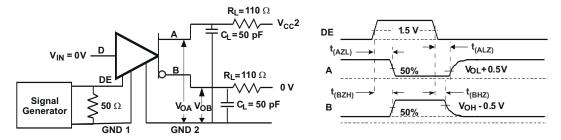


Figure 7-11. Driver Enable/Disable Test, D at Logic Low Test Circuit and Waveforms

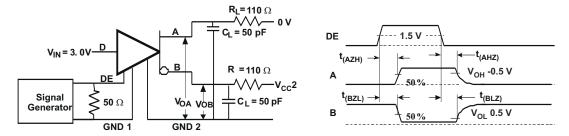


Figure 7-12. Driver Enable/Disable Test, D at Logic High Test Circuit and Waveforms



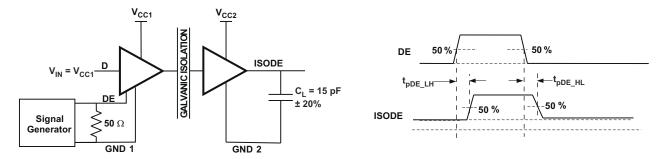


Figure 7-13. DE to ISODE Prop Delay Test Circuit and Waveforms

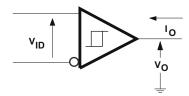


Figure 7-14. Receiver DC Parameter Definitions

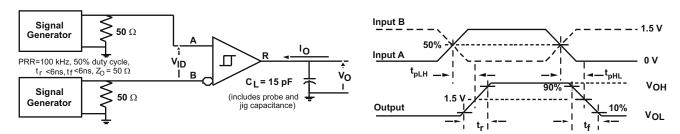


Figure 7-15. Receiver Switching Test Circuit and Waveforms

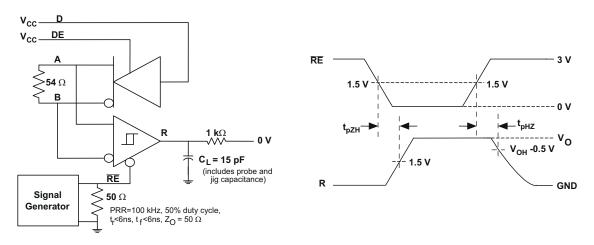


Figure 7-16. Receiver Enable Test Circuit and Waveforms, Data Output High

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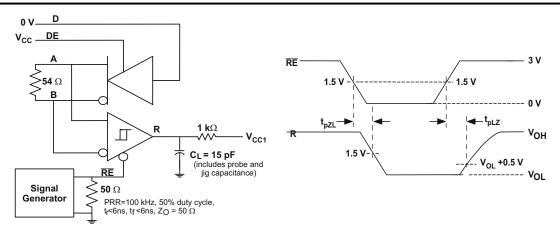


Figure 7-17. Receiver Enable Test Circuit and Waveforms, Data Output Low

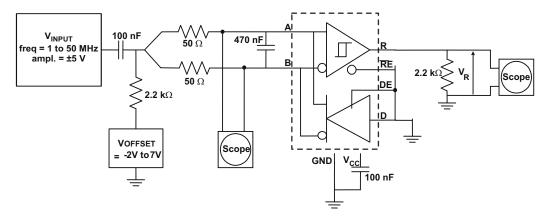


Figure 7-18. Common-Mode Rejection Test Circuit

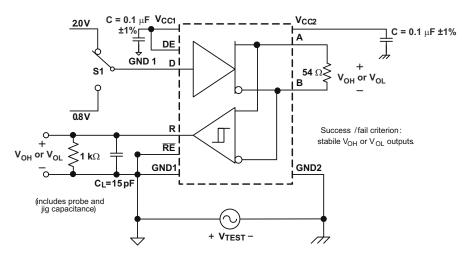


Figure 7-19. Common-Mode Transient Immunity Test Circuit



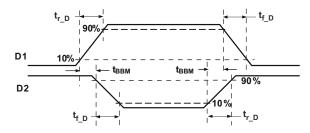


Figure 7-20. Transition Times and Break-Before-Make Time Delay for D1, D2 Outputs

# 8 Detailed Description

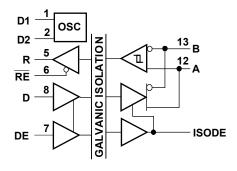
#### 8.1 Overview

The ISO1176T is an isolated half-duplex differential line transceiver that meets the requirements of EN 50170 and TIA/EIA 485/422 applications. It has integrated transformer driver for convenient secondary power supply design. The device is rated to provide galvanic isolation of up to 4242  $V_{PK}$  per VDE and 2500  $V_{RMS}$  per UL 1577. The device has active-high driver enable and active-low receiver enable functions to control the data flow. It has maximum data transmission speed of 40 Mbps.

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case, the differential output voltage defined as  $V_{OD} = V_{(A)} - V_{(B)}$  is positive. When D is low, the output states reverse, B turns high, A becomes low, and  $V_{OD}$  is negative. When DE is low, both outputs turn high-impedance. In this condition, the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to  $V_{CC}$ , thus, when left open while the driver is enabled, output A turns high and B turns low.

When the receiver enable pin,  $\overline{RE}$ , is logic low, the receiver is enabled. When the differential input voltage defined as  $V_{ID} = V_{(A)} - V_{(B)}$  is positive and higher than the positive input threshold,  $V_{IT+}$ , the receiver output, R, turns high. When  $V_{ID}$  is negative and lower than the negative input threshold,  $V_{IT-}$ , the receiver output, R, turns low. If  $V_{ID}$  is between  $V_{IT+}$  and  $V_{IT-}$  the output is indeterminate. When  $\overline{RE}$  is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of  $V_{ID}$  are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

### 8.2 Functional Block Diagram





#### 8.3 Device Functional Modes

Table 8-1 and Table 8-2 are the function tables for the ISO1176T driver and receiver.

Table 8-1. Driver Function Table<sup>(1)</sup>

V	V	V <sub>CC2</sub> INPUT ENABLE INPU		ENABLE OUTPUT	OUTPUTS	
V <sub>CC1</sub>	VCC2	(D)	(DE)	(ISODE)	Α	В
PU	PU	Н	Н	Н	Н	L
PU	PU	L	Н	Н	L	Н
PU	PU	Х	L	L	Z	Z
PU	PU	Х	open	L	Z	Z
PU	PU	open	Н	Н	Н	L
PD	PU	Х	X	L	Z	Z
PU	PD	Х	X	L	Z	Z
PD	PD	Х	X	L	Z	Z

<sup>(1)</sup> PU = Powered Up, PD = Powered Down, H = High Level, L= Low Level, X = Don't Care, Z = High Impedance (off)

Table 8-2. Receiver Function Table<sup>(1)</sup>

Table 0-2. Receiver I diletion Table								
V <sub>CC1</sub>	V <sub>CC2</sub>	DIFFERENTIAL INPUT V <sub>ID</sub> = (V <sub>A</sub> – V <sub>B</sub> )	ENABLE (RE)	OUTPUT (R)				
PU	PU	-0.01V ≤ V <sub>ID</sub>	L	Н				
PU	PU	-0.2V < V <sub>ID</sub> < - 0.01V	L	?				
PU	PU	V <sub>ID</sub> ≤ -0.2V	L	L				
PU	PU	Х	Н	Z				
PU	PU	Х	open	Z				
PU	PU	Open circuit	L	Н				
PU	PU	Short Circuit	L	Н				
PU	PU	Idle (terminated) bus	L	Н				
PD	PU	Х	Х	Z				
PU	PD	Х	L	Н				
PD	PD	Х	Х	Z				

<sup>(1)</sup> PU = Powered Up, PD = Powered Down, H = High Level, L= Low Level, X = Don't Care, Z = High Impedance (off), ? = Indeterminate

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## 8.3.1 Device I/O Schematics

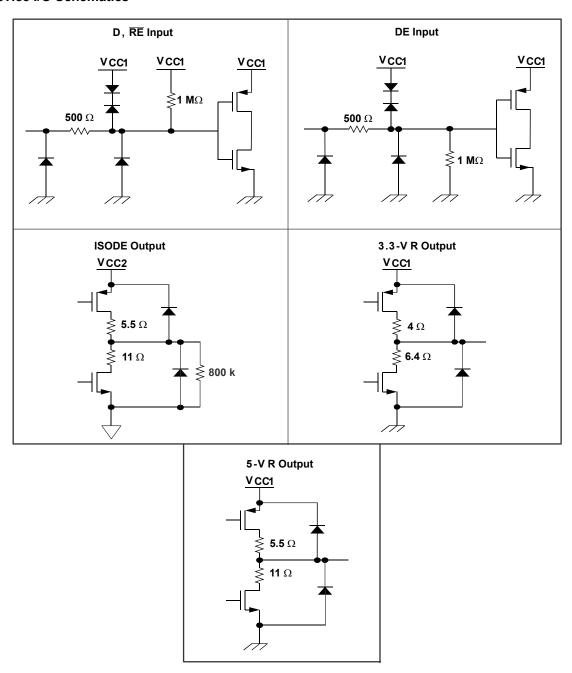


Figure 8-1. Equivalent Circuit Schematics



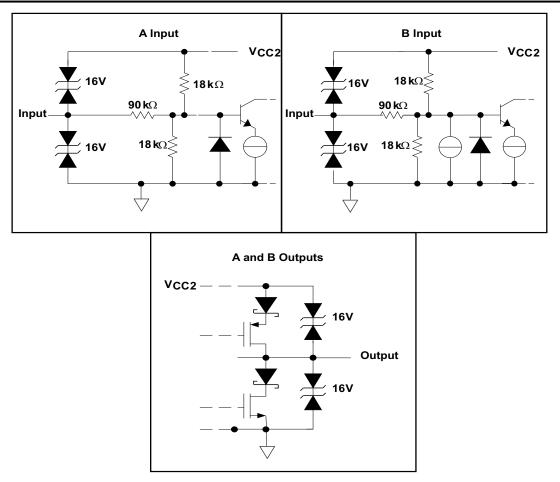


Figure 8-2. Equivalent Circuit Schematics



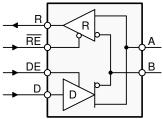
# 9 Application and Implementation

#### Note

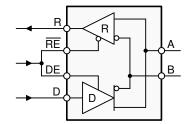
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

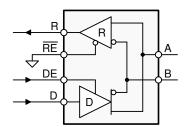
The ISO1176T device consists of a RS-485 transceiver, commonly used for asynchronous data transmissions. For half-duplex transmission, only one pair is shared for both transmission and reception of data. To eliminate line reflections, each cable end is terminated with a termination resistor, R(T), whose value matches the characteristic impedance, Z0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.



a) Independent driver and receiver enable signals



b) Combined enable signals for use as directional control pin



c) Receiver always on

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Figure 9-1. Half-Duplex Transceiver Configurations

#### 9.2 Typical Application

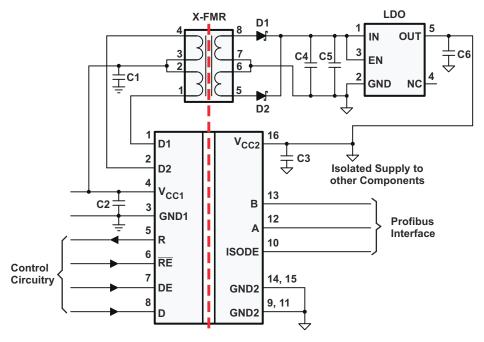


Figure 9-2. Typical Application



### 9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

**Table 9-1. Design Parameters** 

	<u> </u>
PARAMETER	VALUE
Pullup and Pulldown Resistors	1 kΩ to 10 kΩ
Decoupling Capacitors	100 nF

#### 9.2.2 Detailed Design Procedure

#### 9.2.2.1 Transient Voltages

#### 9.2.2.1.1

Isolation of a circuit insulates it from other circuits and earth so that noise develops across the insulation rather than circuit components. The most common noise threat to data-line circuits is voltage surges or electrical fast transients that occur after installation and the transient ratings of ISO1176T are sufficient for all but the most severe installations. However, some equipment manufacturers use their ESD generators to test transient susceptibility of their equipment and can exceed insulation ratings. ESD generators simulate static discharges that may occur during device or equipment handling with low-energy but high voltage transients.

Figure 9-3 models the ISO1176T bus IO connected to a noise generator.  $C_{IN}$  and  $R_{IN}$  is the device and any other stray or added capacitance or resistance across the A or B pin to GND2,  $C_{ISO}$  and  $R_{ISO}$  is the capacitance and resistance between GND1 and GND2 of ISO1176T plus those of any other insulation (transformer, or similar), and we assume stray inductance negligible. From this model, the voltage at the isolated bus return is shown in Equation 1:

$$v_{GND2} = v_N \frac{Z_{ISO}}{Z_{ISO} + Z_{IN}}$$
(1)

and will always be less than 16 V from  $V_N$ . If ISO1176T is tested as a stand-alone device,  $R_{IN}$  = 6 ×  $10^4\Omega$ ,  $C_{IN}$  =  $16 \times 10^{-12}$  F,  $R_{ISO}$  =  $10^9\Omega$  and  $C_{ISO}$  =  $10^{-12}$  F.

Note from Figure 9-3 that the resistor ratio determines the voltage ratio at low frequency and it is the inverse capacitance ratio at high frequency. In the stand-alone case and for low frequency, as shown in Equation 2,

$$\frac{v_{GND2}}{v_N} = \frac{R_{ISO}}{R_{ISO} + R_{IN}} = \frac{10^9}{10^9 + 6 \times 10^4}$$
 (2)

or essentially all of noise appears across the barrier. At high frequency, as shown in Equation 3,

$$\frac{v_{GND2}}{v_N} = \frac{\frac{1}{C_{ISO}}}{\frac{1}{C_{ISO}} + \frac{1}{C_{IN}}} = \frac{1}{1 + \frac{C_{ISO}}{C_{IN}}} = \frac{1}{1 + \frac{1}{16}} = 0.94$$
(3)

and 94% of  $V_N$  appears across the barrier. As long as  $R_{ISO}$  is greater than  $R_{IN}$  and  $C_{ISO}$  is less than  $C_{IN}$ , most of transient noise appears across the isolation barrier, as it should.

We recommend the reader not test equipment transient susceptibility with ESD generators or consider product claims of ESD ratings above the barrier transient ratings of an isolated interface. ESD is best managed through recessing or covering connector pins in a conductive connector shell and installer training.

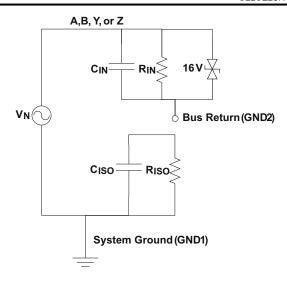


Figure 9-3. Noise Model

# 9.2.3 Application Curve

At maximum working voltage, ISO1176T isolation barrier has more than 28 years of life.

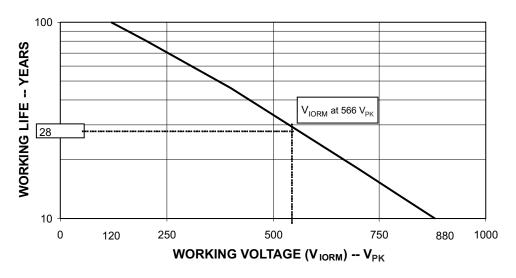


Figure 9-4. Time-Dependent Dielectric Breakdown Test Results



# 10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, TI recommends a  $0.1-\mu F$  bypass capacitor at input and output supply pins ( $V_{CC1}$  and  $V_{CC2}$ ). The capacitors should be placed as close to the supply pins as possible. This device is used in applications where only a single primary-side power supply is available. Isolated power can be generated for the secondary-side with the help of integrated transformer driver.

### 11 Layout

## 11.1 Layout Guidelines

ON-chip IEC-ESD protection is good for laboratory and portable equipment but never sufficient for EFT and surge transients occurring in industrial environments. Therefore, robust and reliable bus node design requires the use of external transient protection devices. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, high-frequency layout techniques must be applied during PCB design. A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 11-1).

- Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane, and low-frequency signal layer.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in<sup>2</sup>.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
- Use V<sub>CC</sub> and ground planes to provide low-inductance. High-frequency currents might follow the path of least inductance and not necessarily the path of least resistance.
- Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
- Apply 0.1-µF bypass capacitors as close as possible to the V<sub>CC</sub>-pins of transceiver, UART, and controller ICs on the board.
- Use at least two vias for V<sub>CC</sub> and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
- Use 1-k $\Omega$  to 10-k $\Omega$  pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events.
- Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified
  maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the
  transceiver and prevent it from latching up.
- While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.
- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.

If an additional supply voltage plane or signal layer is needed, add a second power and ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

#### Note

For detailed layout recommendations, see Application Note Digital Isolator Design Guide, SLLA284.



# 11.2 Layout Example

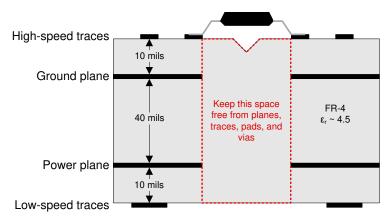


Figure 11-1. Recommended Layer Stack



# 12 Device and Documentation Support

# 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

- Isolated, 40-Mbps, 3.3-V to 5-V Profibus Interface (SLUU471)
- Digital Isolator Design Guide (SLLA284)
- Isolation Glossary (SLLA353)

#### 12.2 Community Resources

#### 12.3 Trademarks

Profibus® is a registered trademark of Profibus International. All trademarks are the property of their respective owners.

#### 12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
ISO1176TDW	Obsolete	Production	SOIC (DW)   16	-	-	Call TI	Call TI	-40 to 85	ISO1176T
ISO1176TDWR	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO1176T
ISO1176TDWR.A	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO1176T
ISO1176TDWR.B	Active	Production	SOIC (DW)   16	2000   LARGE T&R	-	Call TI	Call TI	-40 to 85	
ISO1176TDWRG4	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO1176T
ISO1176TDWRG4.A	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO1176T
ISO1176TDWRG4.B	Active	Production	SOIC (DW)   16	2000   LARGE T&R	-	Call TI	Call TI	-40 to 85	

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



# **PACKAGE OPTION ADDENDUM**

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# **PACKAGE MATERIALS INFORMATION**

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## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO1176TDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO1176TDWRG4	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

www.ti.com 18-Jun-2025



## \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO1176TDWR	SOIC	DW	16	2000	353.0	353.0	32.0
ISO1176TDWRG4	SOIC	DW	16	2000	353.0	353.0	32.0

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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