INA848 Ultra-Low-Noise (1.5 nV/√Hz), High-Bandwidth Instrumentation Amplifier With Fixed Gain of 2000

1 Features

- Fixed gain of 2000 V/V
- Access to internal nodes for filtering
- Ultra-low noise: 1.5 nV/√Hz input voltage noise (maximum)
- Precision super-beta input performance:
  - Low offset voltage: 35 µV (maximum)
  - Low offset voltage drift: 0.45 µV/°C (maximum)
  - Low input bias current: 25 nA (typical)
  - Low gain drift: 5 ppm/°C (maximum)
- Bandwidth: 2.8 MHz
- Slew rate: 45 V/µs
- Common-mode rejection: 132 dB (minimum)
- Supply range:
  - Single supply: 8 V to 36 V
  - Dual supply: ±4 V to ±18 V
- Specified temperature range: –40°C to +125°C
- Package: 8-pin SOIC

2 Applications

- Surgical equipment
- Electrocardiogram (ECG)
- Ultrasound scanner
- Semiconductor test
- Data acquisition (DAQ)
- Vibrational analysis

3 Description

The INA848 is a fixed-gain instrumentation amplifier optimized for high-precision measurements, such as very-small, fast, differential input signals. TI's super-beta topology provides a very low input bias current and current noise. The well-matched transistors help achieve a very low offset and offset drift. Matching of the internal resistors yields a high common-mode rejection ratio of 132 dB across the full input-voltage range, and a very low gain drift error of 5 ppm/ºC (max).

The current-feedback topology of the INA848 produces a wide bandwidth of 2.8 MHz at a fixed gain of 2000, thereby eliminating the need for subsequent gain stages. The very-low noise floor of 1.3 nV/√Hz minimizes the impact on the equivalent number of bits (ENOB) when interfacing with high-resolution analog-to-digital converters (ADCs). The INA848 provides the flexibility of adding filters between the gain stages (pins 2 and 3) to maintain an adequate signal integrity.

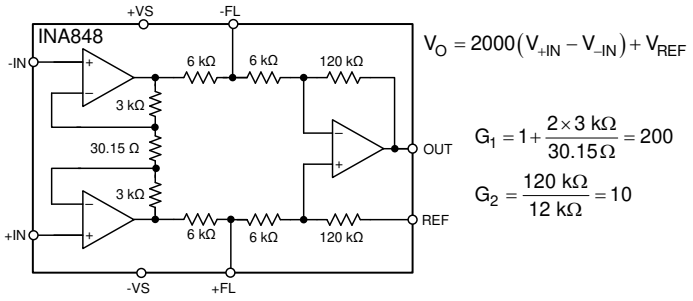
These unique features of the INA848 make this device an excellent choice for applications requiring high-precision measurements, such as high-end medical instrumentation, electroencephalography, vibration sensing, and displacement measurements.

This device is designed for 8-V to 36-V single supplies, or ±4-V to ±18-V on dual supplies.

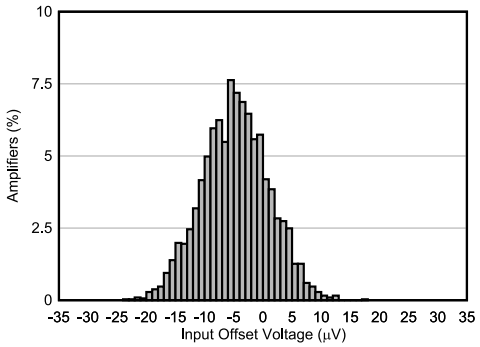
Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
INA848	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



INA848 Simplified Internal Schematic



Typical Distribution of Input Offset Voltage

Table of Contents

4 Revision History

DATE	REVISION	NOTES
September 2020	*	Initial release

5 Device Comparison Table

DEVICE	DESCRIPTION
INA821	35-µV V_{OS}, 0.4 µV/°C V_{OS} drift, 7-nV/√Hz Noise, HighBandwidth, Precision Instrumentation Amplifier
INA819	35-µV V_{OS}, 0.4 µV/°C V_{OS} Drift, 8-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier
INA333	25-µV V_{OS}, 0.1 µV/°C V_{OS} drift, 1.8-V to 5-V, RRO, 50-µA I_Q, chopper-stabilized INA
PGA280	20-mV to ±10-V programmable gain IA with 3-V or 5-V differential output; analog supply up to ±18 V
PGA112	Precision programmable gain op amp with SPI

6 Pin Configuration and Functions

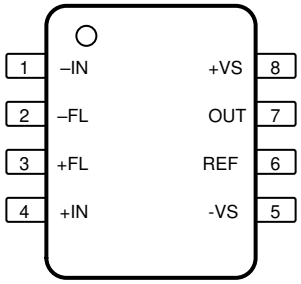


Figure 6-1. D Package, 8-Pin SOIC, Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN	1	I	Negative (inverting) input
+IN	4	I	Positive (noninverting) input
OUT	7	O	Output
–FL	2	I	Negative Filter Terminal.
+FL	3	I	Positive Filter Terminal.
REF	6	I	Reference input. This pin must be driven by a low impedance source.
–VS	5	—	Negative supply
+VS	8	—	Positive supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage	Single supply, $V_S = (+V_S)$		40	V
		Dual supply, $V_S = (+V_S) – (–V_S)$		±20	
V_{IN}	Signal input pins	Common Mode (2)	$(–V_S) – 0.5$	$(+V_S) + 0.5$	V
		Differential (3)		±0.5	
V_{REF}	VREF pin		$(–V_S) – 0.5$	$(+V_S) + 0.5$	V
V_{FL}	Filter input pins +FL, –FL		$(–V_S) – 0.5$	$(+V_S) + 0.5$	V
V_O	Signal output pins maximum voltage		$(–V_S) – 0.5$	$(+V_S) + 0.5$	V
I_O	Signal output pins maximum current		–50	50	mA
I_S	Output short-circuit(4)		–50	50	mA
T_A	Operating temperature (5)			125	°C
T_J	Junction temperature (5)			175	°C
T_{stg}	Storage temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that swing more than 0.5 V beyond the supply rails must be current-limited to 10 mA or less.

(3) Input terminals are anti-parallel diode-clamped to each other. Input signals that cause differential voltages of swing more than ± 0.5 V must be current-limited to 10 mA or less.

(4) Short-circuit to V_S / 2.

(5) As a result of the quiescent current, a supply voltage and load-dependent self-heating of the device must be considered.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Supply voltage	Single supply, $V_S = (+V_S)$	8	36	V
		Dual supply, $V_S = (+V_S) – (–V_S)$	±4	±18	
T_A	Specified temperature		–40	125	°C

7.4 Thermal Information

THERMAL METRIC[1]		INA848 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, G = 2000 (fixed) and V_{REF} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{OSI}	Input offset voltage			±10	±35	µV
		T_A = –40°C to +125°C[1]			±80	
	Input offset voltage drift	T_A = –40°C to +125°C		±0.1	±0.45	µV/°C
PSRR	Power-supply rejection ratio	±4 V ≤ (V_S) ≤ ±18 V	125	150		dB
Z_{in}	Input impedance			1 || 7		GΩ || pF
	RFI filter, –3-dB frequency			250		MHz
V_{CM}	Operating input voltage[3]	V_S = ±4 V to ±18 V	(–V_S) + 2.5		(+V_S) – 2.5	V
		V_S = ±4 V to ±18 V, T_A = –40°C to +125°C		See Figure 7-9		
CMRR	Common-mode rejection ratio	At dc to 60 Hz, RTI (–V_S) + 2.5 V < V_{CM} < (+V_S) – 2.5 V	132	150		dB
		At 50 kHz, RTI (–V_S) + 2.5 V < V_{CM} < (+V_S) – 2.5 V		110		
BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S / 2		25	50	nA
	Input bias current dift	T_A = –40°C to +125°C		40		pA/°C
I_{OS}	Input offset current	V_{CM} = V_S / 2		2	10	nA
	Input offset current drift	T_A = –40°C to +125°C		10		pA/°C
NOISE VOLTAGE						
e_{NI}	Input voltage noise	f = 1 kHz, R_S = 0 Ω		1.3	1.5[2]	nV/√Hz
		f_B = 0.1 Hz to 10 Hz, R_S = 0 Ω		55		nV_{PP}
I_n	Input current noise	f = 1 kHz		1.85		pA/√Hz
		f_B = 0.1 Hz to 10 Hz		75		pA_{PP}
GAIN						
G	First stage gain			200		V/V
	Subtractor stage gain			10		V/V
GE	Total gain error	V_O = ±10 V		0.05	0.15[1] [2]	%
	Total gain drift	T_A = –40°C to +125°C			5[1] [2]	ppm/°C
	Total gain nonlinearity	V_O = –10 V to +10 V, no load		10		ppm

7.5 Electrical Characteristics (continued)

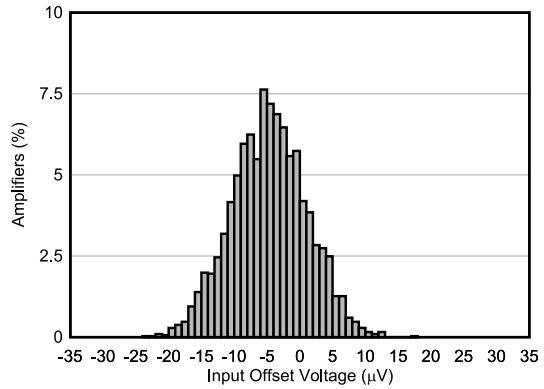
at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, G = 2000 (fixed) and V_{REF} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD+N	Total harmonic distortion and noise	f = 20 kHz, V_O = 10 V_{pp}		–109		dBc
HD2	Second-order harmonic distortion	f = 20 kHz, V_O = 10 V_{pp}		–112		dBc
HD3	Third-order harmonic distortion	f = 20 kHz, V_O = 10 V_{pp}		–119		dBc
THD+N	Total harmonic distortion and noise	R_L = 1 MΩ, f = 20 kHz, V_O = 10 V_{pp}		–111		dBc
HD2	Second-order harmonic distortion	R_L = 1 MΩ, f = 20 kHz, V_O = 10 V_{pp}		–117		dBc
HD3	Third-order harmonic distortion	R_L = 1 MΩ, f = 20 kHz, V_O = 10 V_{pp}		–118		dBc
OUTPUT						
	Output voltage swing		($-V_S$) + 0.15		($+V_S$) – 0.15	V
C_L	Load capacitance	In stable condition		1000		pF
I_{SC}	Short-circuit current	Continuous to V_S / 2		±30		mA
FREQUENCY RESPONSE						
BW	Bandwidth, –3 dB			2.8		MHz
SR	Slew rate	V_{STEP} = 10 V	35[1]	45		V/µs
t_S	Settling time	0.01%, V_{STEP} = 10 V		0.5		µs
		0.001%, V_{STEP} = 10 V		0.9		
REFERENCE INPUT						
R_{IN}	Input impedance			132		kΩ
I_{IN}	Input current			6.5		µA
	Reference input voltage		$-V_S$		$+V_S$	V
	Gain to output			1		V/V
	Reference gain error			0.01		%
FILTER INPUTS						
R_{FIL}	Input impedance, filter terminal			6		kΩ
	Voltage range, filter terminal		$-V_S$		$+V_S$	V
POWER SUPPLY						
I_Q	Quiescent current	V_{IN} = 0 V		6.2	6.6	mA
		T_A = –40°C to +85°C			7.9	
		T_A = –40°C to +125°C			8.8	

(1) Specified by characterization.
(2) Specified by design.
(3) The input voltage range depends on the common-mode voltage, differential voltage, gain, and reference voltage.

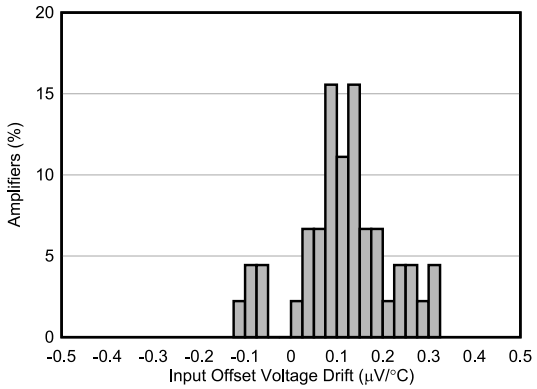
7.6 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 2000 (unless otherwise noted)



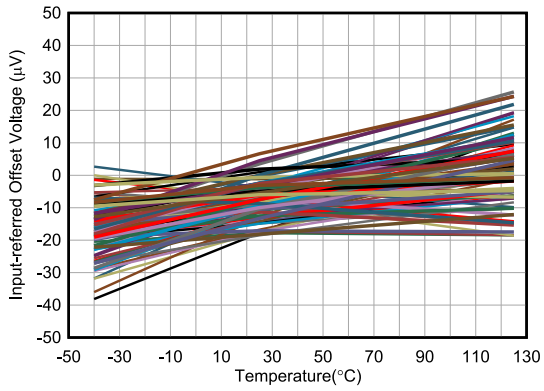
N = 3172, mean = –4.678 µV, std dev = 5.715 µV

Figure 7-1. Typical Distribution of Input Offset Voltage



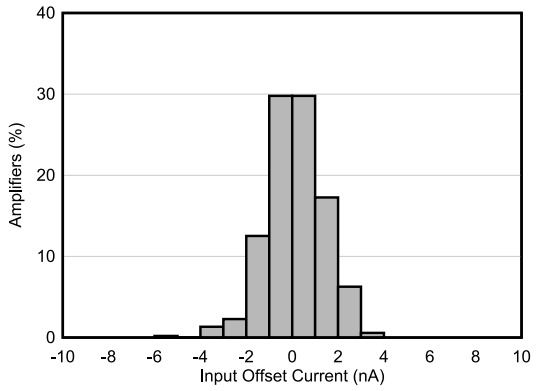
N = 45, mean = 0.116 µV/°C, std dev = 0.102 µV/°C

Figure 7-2. Typical Distribution of Input Offset Voltage Drift



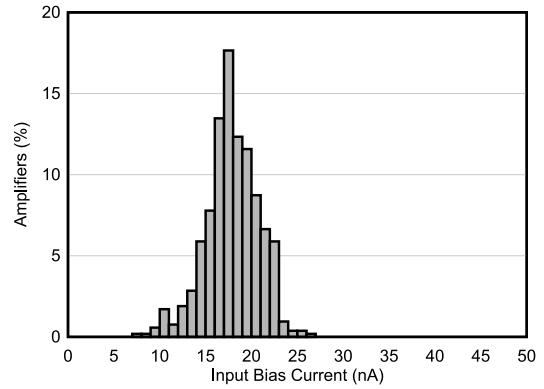
N = 48

Figure 7-3. Input-referred Offset Voltage vs Temperature



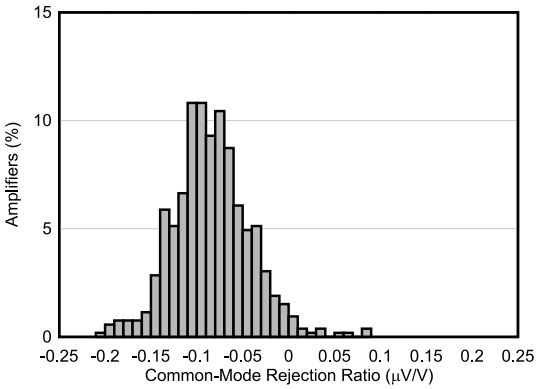
N = 527, mean = 0.1369 nA, std dev = 1.222 nA

Figure 7-4. Typical Distribution of Input Offset Current



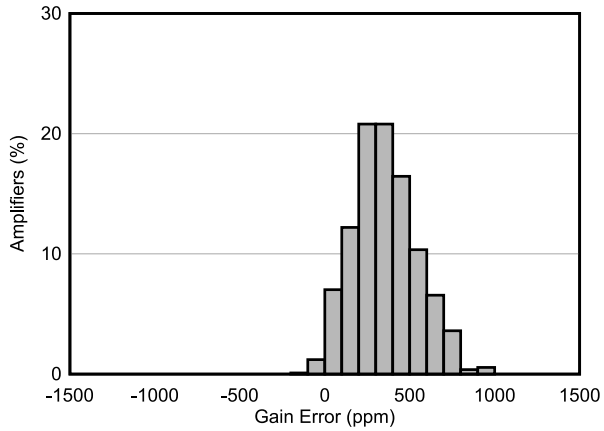
N = 527, mean = 17.876 nA, std dev = 2.875 nA

Figure 7-5. Typical Distribution of Input Bias Current



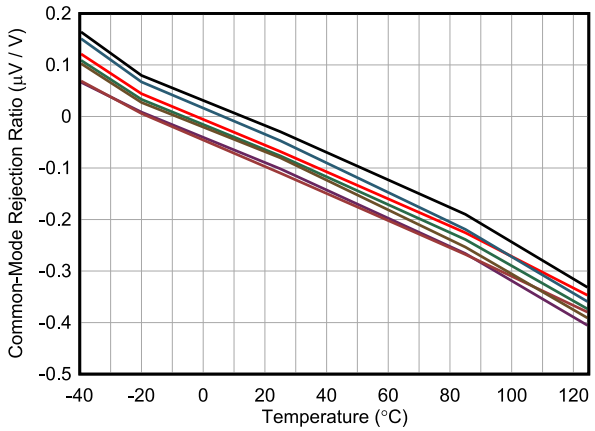
N = 527, mean = -0.0840 µV/V, std dev = 0.0420 µV/V

Figure 7-6. Typical CMRR Distribution



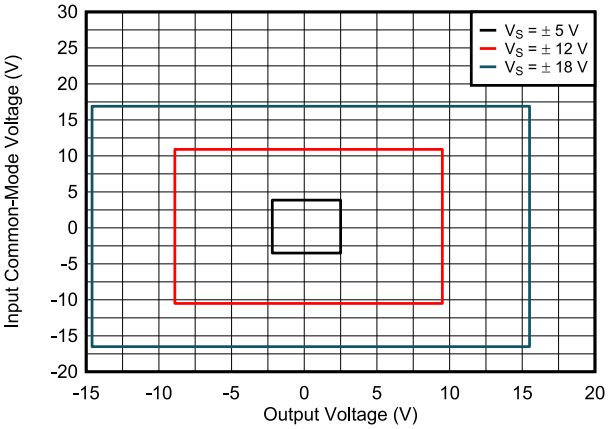
N = 1080, mean = 356.396 ppm, std dev = 186.085 ppm

Figure 7-7. Typical Distribution of Gain Error



N = 7

Figure 7-8. CMRR vs Temperature



VREF = 0 V

Figure 7-9. Input Common-Mode Voltage vs Output Voltage

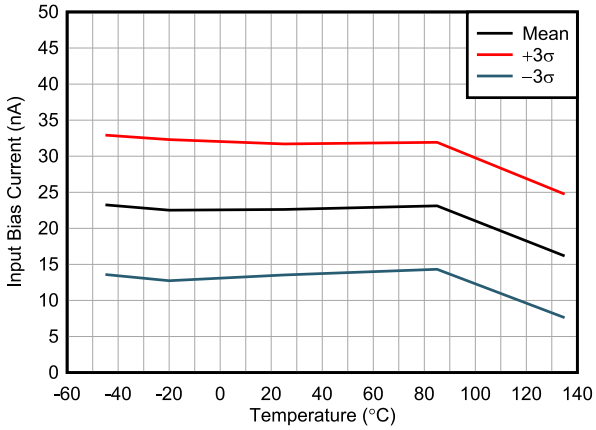


Figure 7-10. Input Bias Current vs Temperature

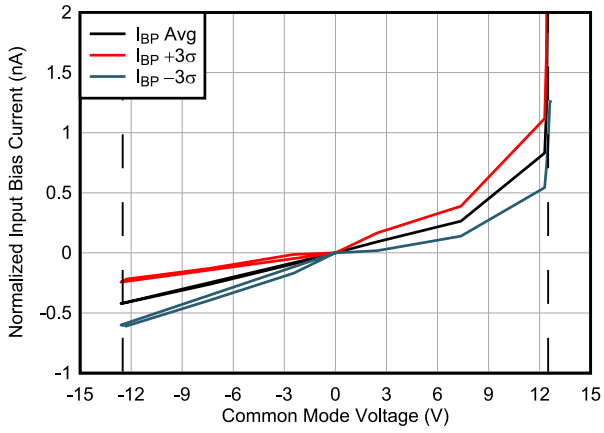


Figure 7-11. Positive Input Bias Current vs Input Common-Mode Voltage

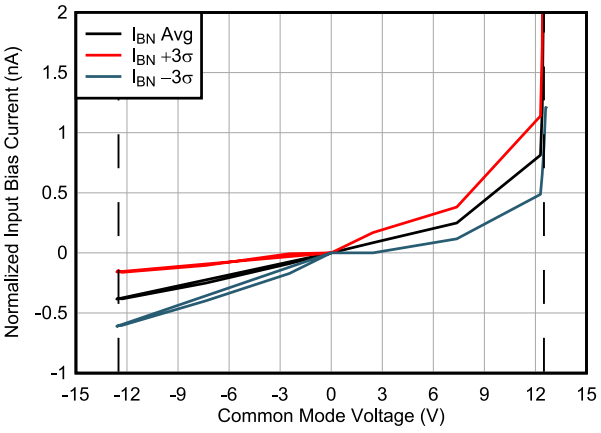


Figure 7-12. Negative Input Bias Current vs Input Common-Mode Voltage

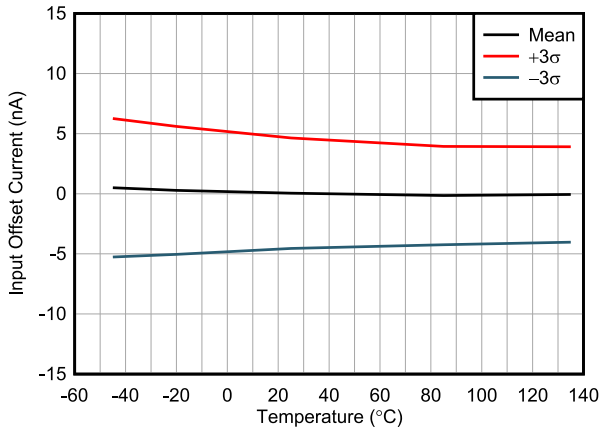


Figure 7-13. Input Offset Current vs Temperature

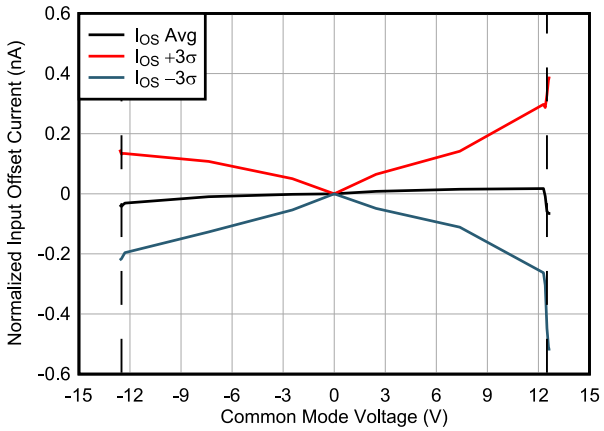


Figure 7-14. Input Offset Current vs Input Common-Mode Voltage

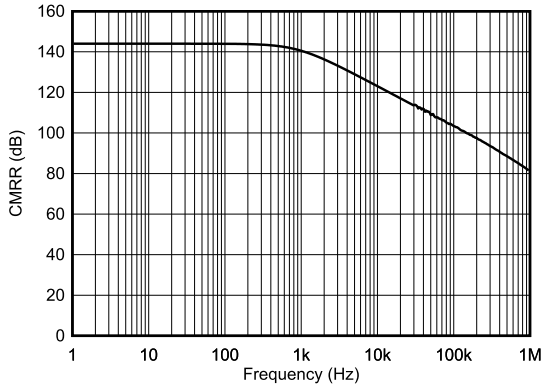


Figure 7-15. CMRR vs Frequency (RTI)

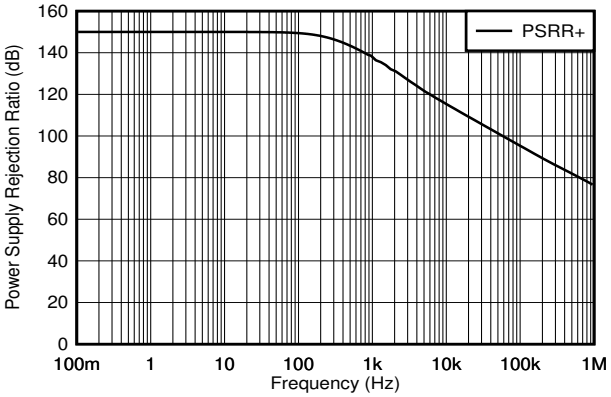


Figure 7-16. Positive PSRR vs Frequency (RTI)

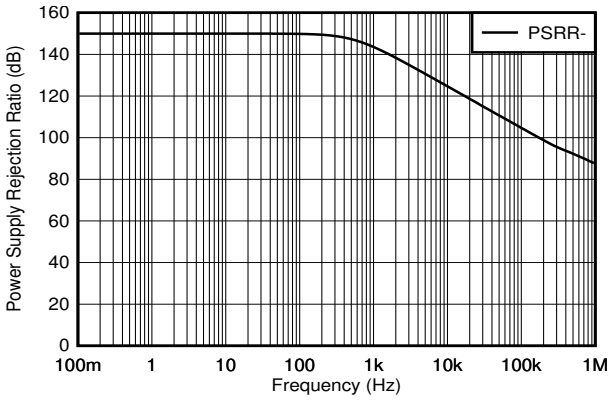


Figure 7-17. Negative PSRR vs Frequency (RTI)

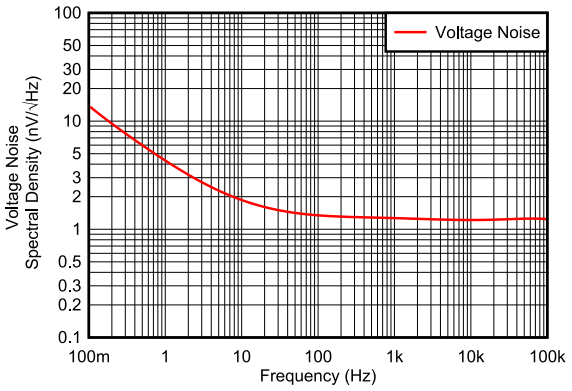


Figure 7-18. Voltage Noise Spectral Density vs Frequency (RTI)

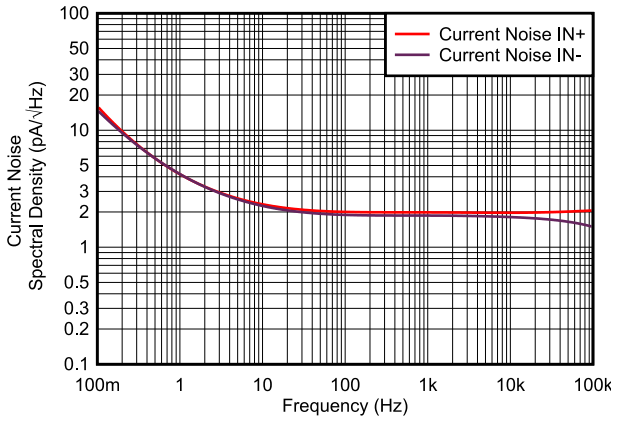


Figure 7-19. Current Noise Spectral Density vs Frequency (RTI)

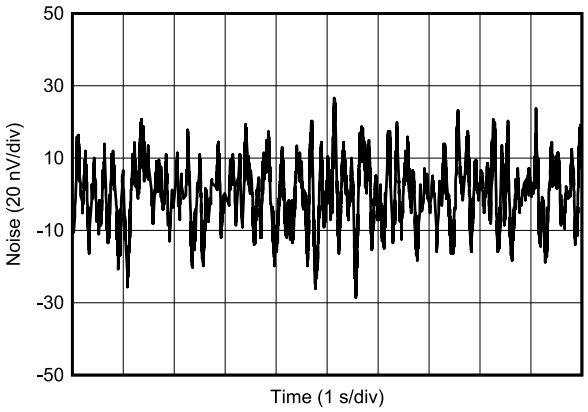
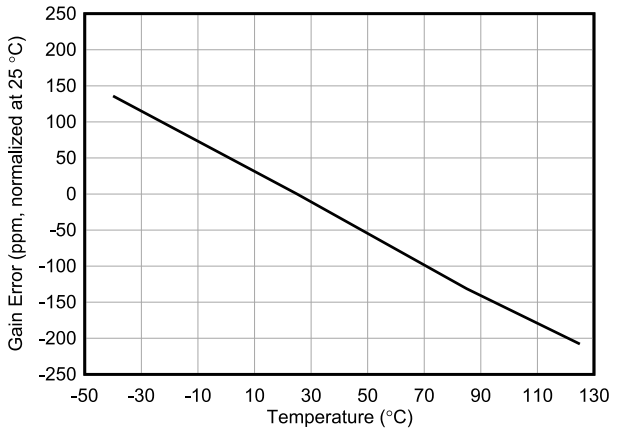


Figure 7-20. 0.1-Hz to 10-Hz RTI Voltage Noise



No Load

Figure 7-21. Gain Error vs Temperature

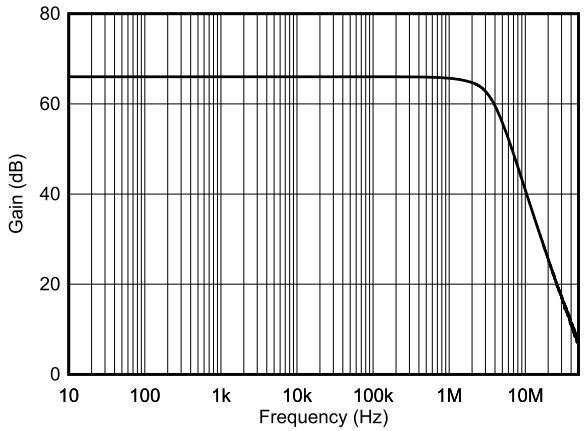


Figure 7-22. Closed Loop Gain vs Frequency

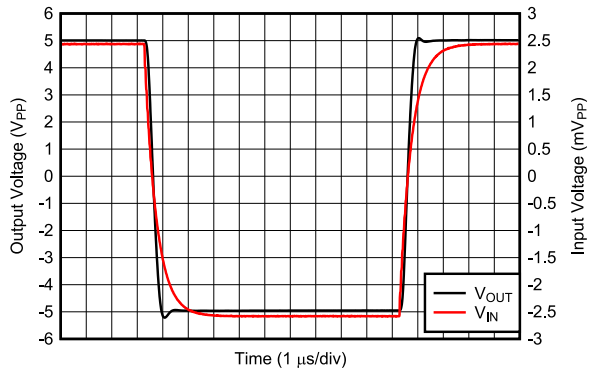


Figure 7-23. Large-Signal Step Response

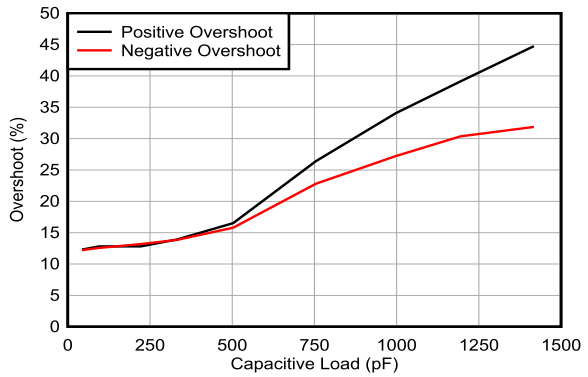


Figure 7-24. Small Signal Response vs Capacitive Loads

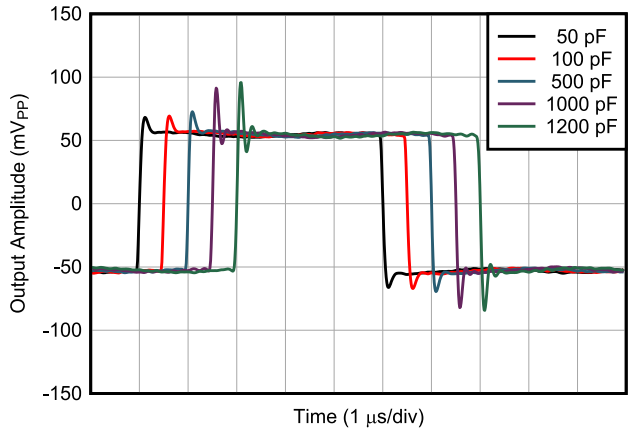


Figure 7-25. Small Signal Response

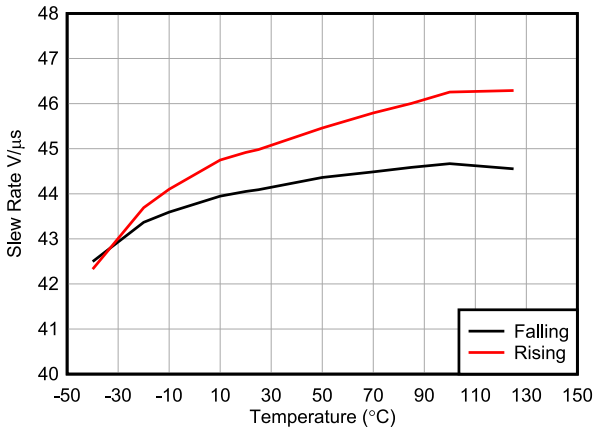


Figure 7-26. Slew Rate vs Temperature

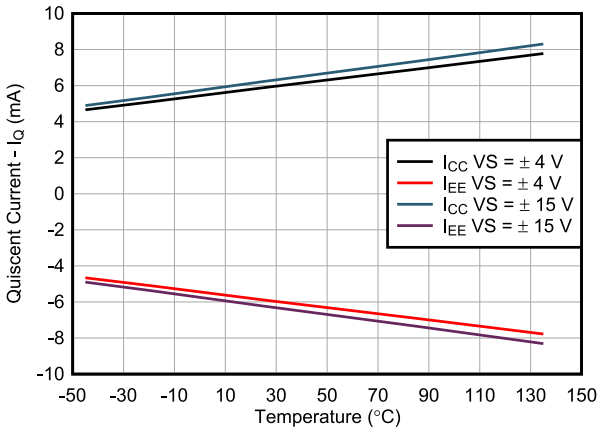


Figure 7-27. Supply Current vs Temperature

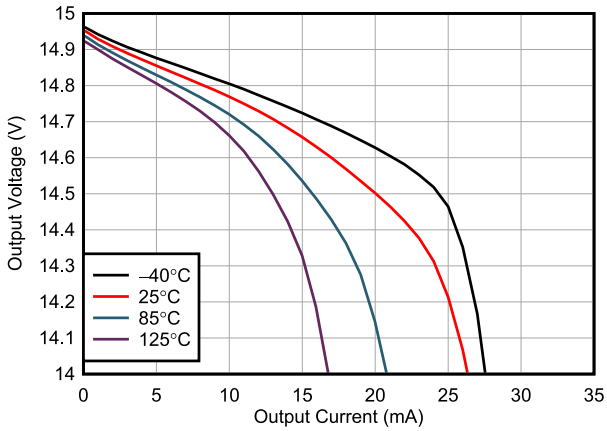


Figure 7-28. Positive Output Voltage Swing vs Output Current

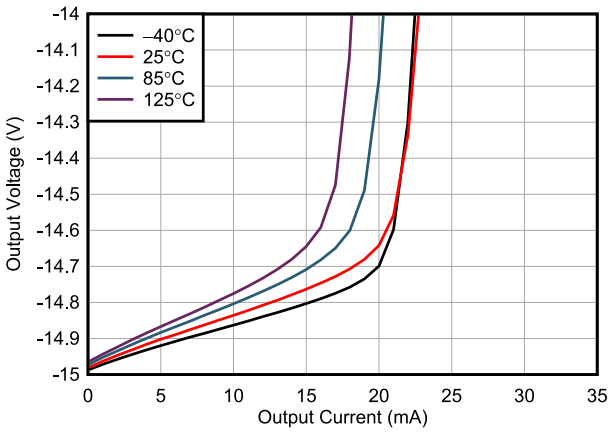


Figure 7-29. Negative Output Voltage Swing vs Output Current

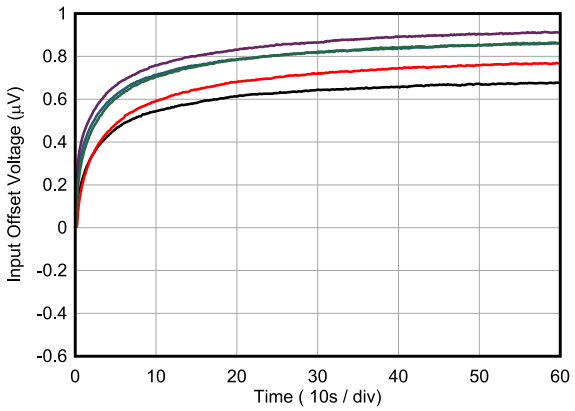


Figure 7-30. Input-Referred Offset Voltage vs Settling Time

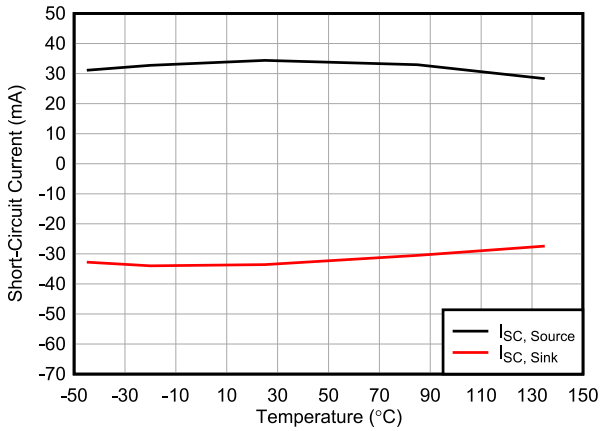


Figure 7-31. Short Circuit Current (Source + Sink) vs Temperature

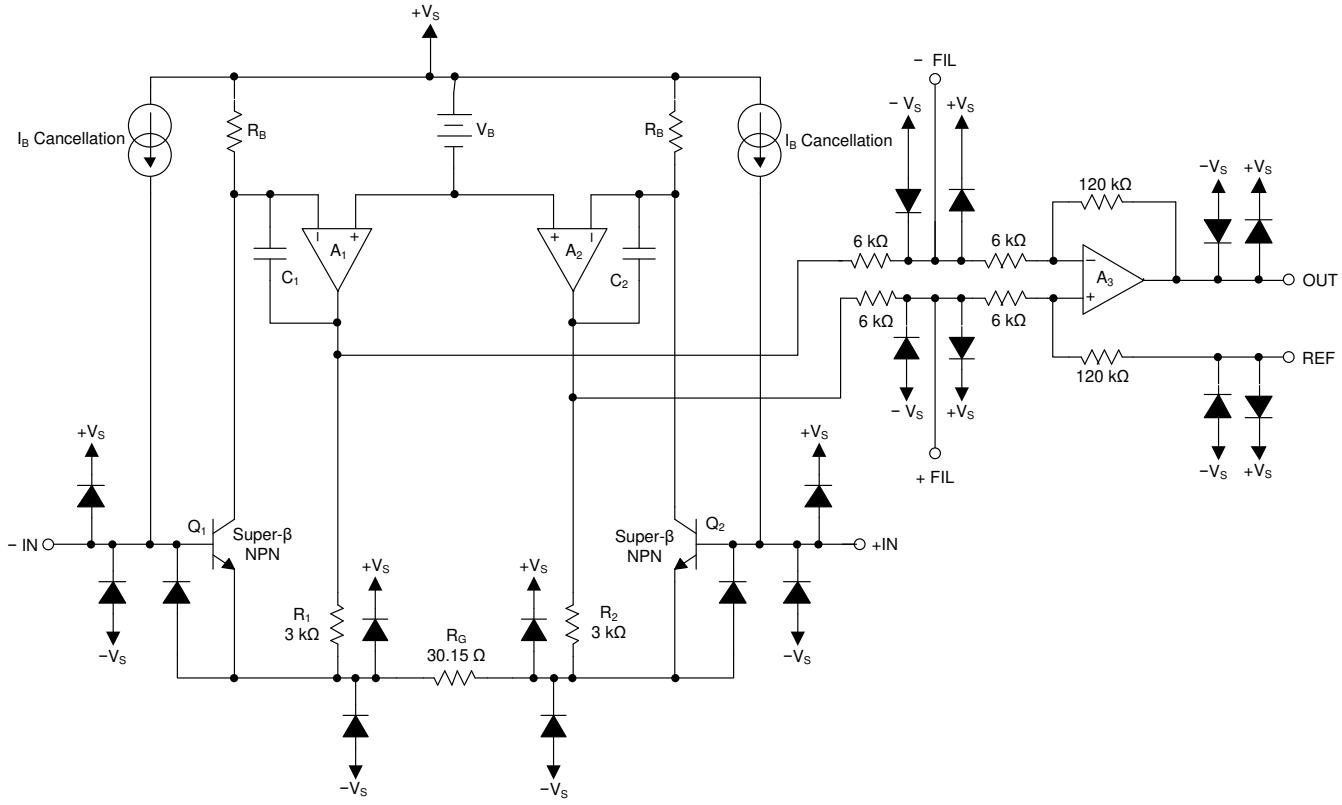
8 Detailed Description

8.1 Overview

The INA848 is a monolithic precision instrumentation amplifier incorporating a current-feedback input stage and a four-resistor difference amplifier output stage. The differential input voltage is buffered by Q_1 and Q_2 and is forced across R_G, which causes a signal current to flow through R_G, R_1, and R_2. The output difference amplifier (A_3) removes the common-mode component of the input signal and refers the output signal to the REF pin. The V_{BE} and voltage drop across R_1 and R_2 produce output voltages on A_1 and A_2 that are approximately 0.8 V lower than the input voltages.

In common instrumentation amplifiers, an external gain resistor is used to set the gain. However, this external gain resistor affects the gain drift due to the mismatch in tempertature coefficient between the external and internal resistors. The INA848 integrates the gain setting resistor with a fixed gain of 2000, thus matching the temperature drifts of the resistor network. This integration results in an total gain accuracy of 5 ppm/°C (maximum).

8.2 Functional Block Diagram



8.3 Feature Description

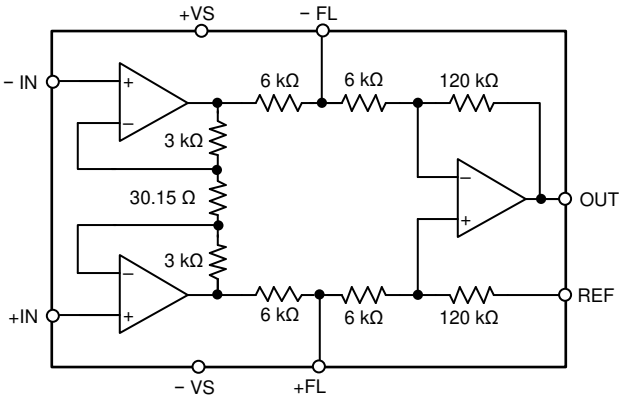
8.3.1 Topology

The INA848 is designed with TI's modern bipolar process that features super-beta input transistors.

Traditional bipolar transistors feature excellent voltage noise and offset drift, but suffer a tradeoff in high input bias current and high input bias current noise.

TI`s super-beta transistors offer the benefits of low voltage noise, low offset voltage drift with an additional improvement in reduction of the input bias current noise.

As shown in Figure 8-1, the INA848 is designed with a current feedback input stage that is optimized for high bandwidth in high gains. The device consists of three operational amplifiers configured at the front with a gain stage that integrates the gain resistor. This input stage preamplifies the differential input signal at a gain of 200. The output stage with the difference amplifier provides additional amplification of a gain of 10.



$$V_O = 2000\left(V_{+IN} - V_{-IN}\right) + V_{REF}$$

$$G_1 = 1 + \frac{2 \times 3\ k\Omega}{30.15\ \Omega} = 200$$

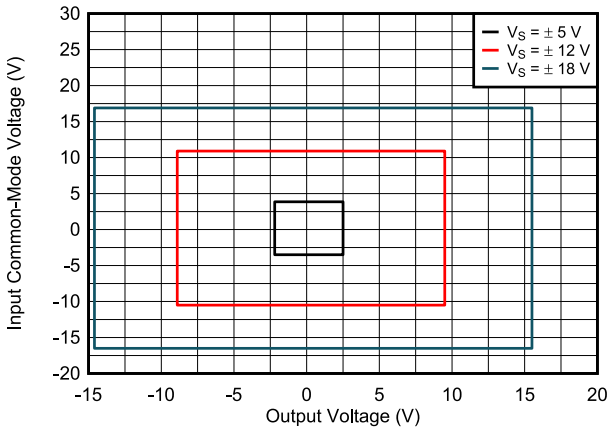
$$G_2 = \frac{120\ k\Omega}{12\ k\Omega} = 10$$

Figure 8-1. Simplified Diagram of the INA848 With Gain and Output Equations

8.3.2 Input Common-Mode Range

The typical three-op-amp topology gains up the input differential signal in the front stage and rejects the common-mode signals in the back end at the difference amplifier stage. The difficulty in particular is to excel driving high gains, and thus tiny input signals, and still be able to reject high common-mode signals. A low-noise instrumentation amplifier such as the INA848 is designed for such requirementsh, with the ability to measure the smallest input signals surrounded by noisy or large common-mode voltages.

The methodology here is achieved by splitting up the gain stages. The front end preamplifies the input signal at a gain of 200, and the difference amplifier further amplifiers at a gain of 10. The resulting advantage is that the common-mode range versus the differential signal is improved compared to single gain stage approach, as shown in Figure 8-2.



V_S = ± 5 V, ± 12 V, ± 18 V, VREF = 0 V

Figure 8-2. Input Common-Mode Voltage vs Output Voltage

The INA848 gives the super-beta input stage features very low input bias current as compared to standard bipolar technology. The low input bias current and current noise make the INA848 an excellent choice for high-performance applications. See Figure 7-10 through Figure 7-12 for reference.

8.3.3 Input Protection

The inputs of the INA848 device are individually protected for voltages up to ±20 V which is stated in Section 7.1. If these rating cannot be met, additional protection circuitry must be considered at the input pins to minimize the current flowing in case of fault.

During an input overvoltage condition, current flows through the input protection diodes into the power supplies; see Figure 8-3 . If the power supplies are unable to sink current, then Zener diode clamps (ZD1 and ZD2) must be placed on the power supplies to provide a current pathway to ground.

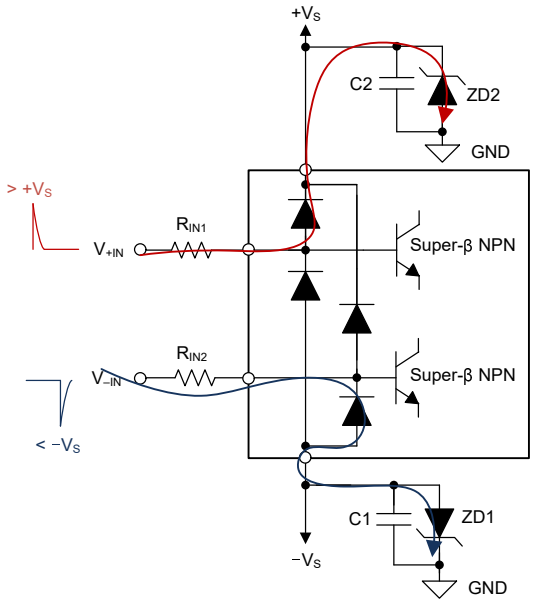


Figure 8-3. Input Current Path During an Overvoltage Condition

For an overvoltage condition, use an external resistor (R_{IN1}, R_{IN2}) to limit the current. The following equation gives the calculation for the protection resistors:

$$R_{IN1} = \frac{(V_{+IN}) - (+V_S)}{I_{MAX}} \quad (1)$$

where:

- V_{+IN} is the maximum input voltage
- $+V_S$ is the positive supply rail
- I_{MAX} is the maximum current allowed = 10 mA

Calclate R_{IN2} using the same method, substituting with $V_{–IN}$, $–V_S$, and $–I_{MAX}$.

Any additional resistance to the input pins adds more noise to the system. For more details, see Section 9.2.2.2.

8.4 Device Functional Modes

The INA848 has a single functional mode and is operational when the power supply voltage is greater than 4.5 V (±2.25 V). The maximum power-supply voltage for the INA848 is 36 V (±18 V).

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Filter Pin

The INA848 allows access between the two amplification stages. In applications surrounded from high input noise, adding filter stages can be of high benefit. Figure 9-1 and Figure 9-2 show two different filter scenarios that help filter out undesired differential signals.

9.1.1.1 RC Filter Network

In environments where known high-frequency noise must be eliminated, use a low-pass filter containing a capacitor, and optionally, a resistor.

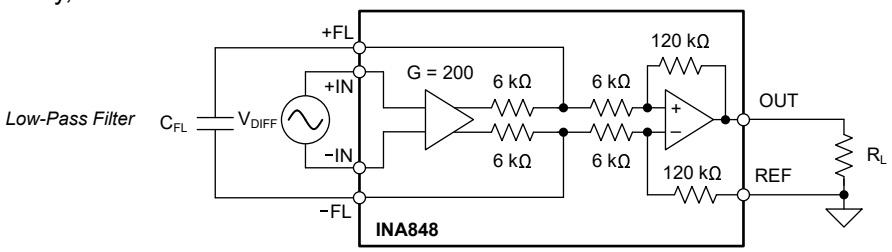


Figure 9-1. Low-pass Filter

The –3-dB cross frequency is determined given following equation:

$$f_{FL1} = \frac{1}{2\pi \cdot 6k\Omega \cdot C_{FL}} \quad (2)$$

Where 6 kΩ represents the internal resistor network. Use the Analog Engineer's Calculator for fast and easy bode plot visualization.

9.1.1.2 RLC Filter Network

In environments where a known, narrow-frequency band must be attenuated, a series LC filter network can be added between the filter pins, as shown in Figure 9-2. The connection adds to the internal resistor network, and results in a RLC filter network that is also commonly known as bandstop filter.

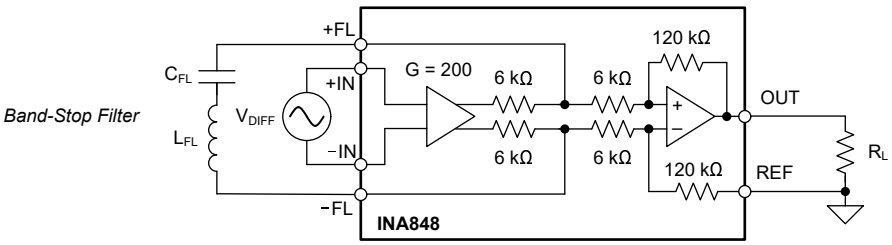


Figure 9-2. Bandstop Filter

Use Equation 3 to calculate the middle frequency of the filter:

$$f_{FL2} = \frac{1}{2\pi \cdot \sqrt{(C_{FL} \cdot L_{FL})}} \quad (3)$$

In general, the width of the stopband is between one and two decades, meaning that the highest attenuation is between 10 to 100 around the middle frequency. This indication is commonly defined as the quality factor (Q factor) of the filter and is calculated by:

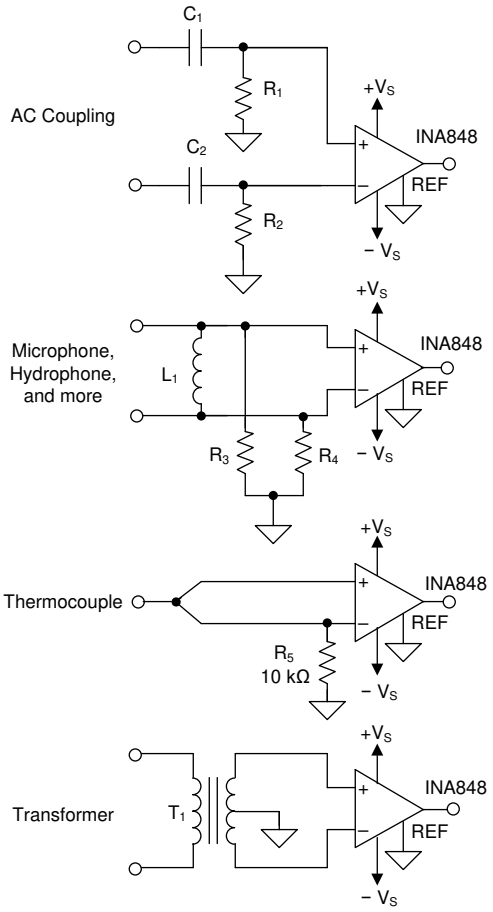
$$Q = \frac{1}{R} \cdot \sqrt{\frac{L_{FL}}{C_{FL}}} \tag{4}$$

The resistor is given by the internal resistor of 6 kΩ; therefore, the damping factor of the filter can further be affected of the series resistance of the inductor L_{FL}. For stable operation of the filter, choose an inductor in the range of 100 µH.

9.1.2 Input Bias Current Return Path

The input impedance of the INA848 is extremely high (approximately 100 GΩ). However, a path must be provided for the input bias current of both inputs. This input bias current is typically 25 nA. High input impedance means that this input bias current changes little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 9-3 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA848, and the input amplifiers saturate. If the differential source resistance is low, the bias current return path connects to one input (as shown in the thermocouple example in Figure 9-3). With a higher source impedance, using two equal resistors provides a balanced input with possible advantages of a lower input offset voltage as a result of bias current, and better high-frequency common-mode rejection.



NOTE: Center tap in the transformer provides bias current return.

Figure 9-3. Providing an Input Common-Mode Current Path

9.2 Typical Application

Figure 9-4 shows a typical application for the INA848.

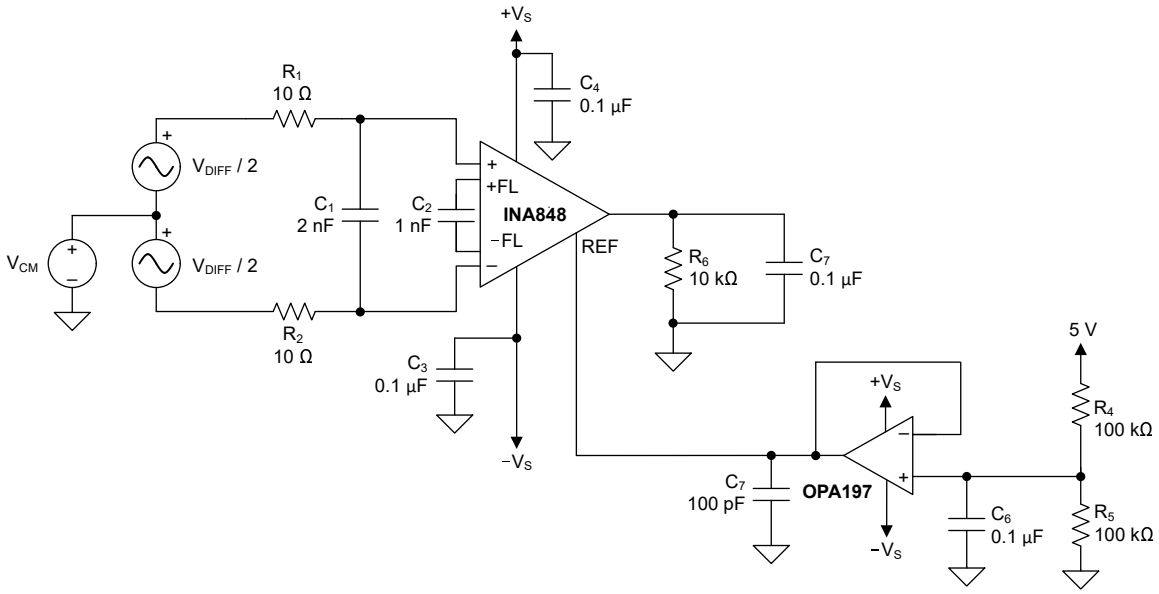


Figure 9-4. Sensor Conditioning (V_{DIFF} < 5 mV, $V_{S±}$ = 15 V)

9.2.1 Design Requirements

For this application, the design requirements are:

- Differential input signal of V_{DIFF} = 2.5 mV
- Common-mode input voltage of V_{CM} = 10 V
- Power-supply voltage of V_S = ± 15 V
- Reference voltage buffered to V_{REF} = 2.5 V
- Output range within 0 V to 5 V
- First-order filter stage with –3-dB frequency of 27 kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Reference Pin

The output voltage of the INA848 is developed with respect to the voltage on the reference pin (REF.)

The voltage source applied to the reference pin of the INA848 must have a low output impedance (R_{REF} > 5 Ω). Any additional resistance at the reference pin creates an imbalance in the four resistors of the internal difference amplifier, resulting in degraded common-mode rejection ratio (CMRR).

Voltage reference devices are an excellent option for providing a low-impedance voltage source for the reference pin. However, if a resistor voltage divider generates a reference voltage, the divider must be buffered by an op amp, as shown in Figure 9-5, to avoid CMRR degradation.

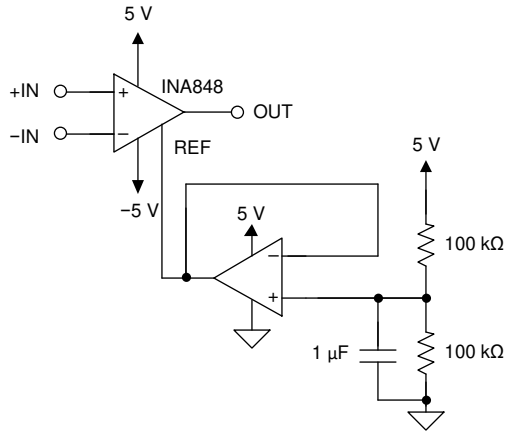


Figure 9-5. Buffer to drive the Reference Voltage

Often in dual-supply operation, the reference pin connects to the low-impedance system ground. The degradation effect of common-mode rejection ratio is thus negligible as long as the output voltage (V_{OUT}) is referred to the reference pin (REF).

In single-supply operation, the output signal is offset to a precise midsupply level (for example, 2.5 V in a 5-V supply environment). In applications where the output voltage is offset to a reference voltage but referred to system ground, the degradation effect of common-mode rejection ratio must be considered.

9.2.2.2 Noise Analysis

Low-noise instrumentation amplifiers such as the INA848 are designed to serve stringent and sensitive applications, such as surgical tools, microphones or other precision monitoring systems. A througough noise analysis is a key element in the design process.

TI`s super-beta transistors offer the benefits of low voltage noise and low current noise, thus allowing the INA848 excellent noise performance.

Figure 9-6 shows a simplified noise model including the gain stages of the INA848.

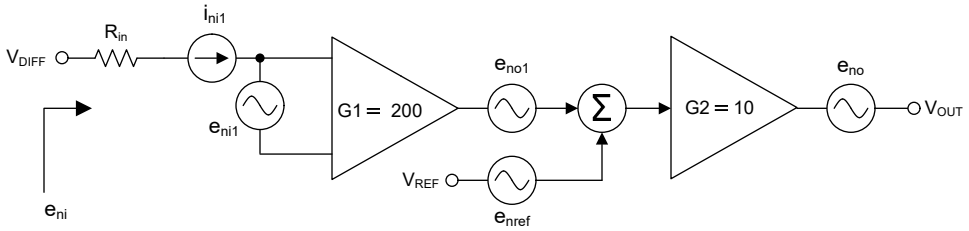


Figure 9-6. Simplified Noise Model

To get the total input-referred noise, e_{ni}, consider the source resistance seen by the positive and negative input pins of the instrumentation amplifier. The key elements that must be considered for a noise analysis in an instrumenation amplifier are:

- Current noise density $i_{ni1}$of the INA, see Section 7.5
- Voltage noise denisty e_{ni1} of the INA, see Section 7.5
- Voltage noise density caused by source resistance i_{ni}× R_{in}
- Resistor noise from source resistance e_{nRin} , given by: $\sqrt{Rin}$ × 4.04 nV/$\sqrt{Hz}$
- Reference voltage noise e_{nref}

The noise sources are uncorrelated (that is, the noise signal is unpredictable). The result of mutliple uncorrelated noise sources is the square root of the sum of their squares (RSS). Thus, the total RTI noise density, e_{ni}, in nV/$\sqrt{Hz}$ can be derived from the following equation:

$$e_{ni} = \sqrt{e_{ni1}^2 + e_{n(Rin)}^2 + (i_{ni1} \cdot R_{in})^2 + \left(\frac{e_{n(REF)}}{G1}\right)^2} \quad (5)$$

9.2.2.2.1 Reference Voltage Noise Contribution

Figure 9-7 shows the noise model of the reference buffer circuit given by Figure 9-5 using the OPA197 amplifier.

To compute the total noise for the reference buffer circuit, consider the thermal noise of the divider (that is a parallel network from noise perspective), the amplifier voltage noise (that is, e_{nOPA} = 5.5 nV/√Hz), and the voltage noise developed from the current noise of the amplifier (that is, i_{nOPA} = 1.5 fA/√Hz) through the divider.

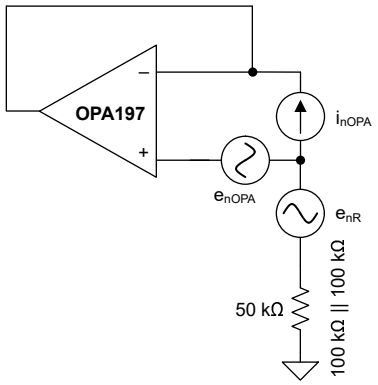


Figure 9-7. Reference Voltage Noise Model

Thus the total reference noise can be derived from following equation:

$$e_{n(REF)} = \sqrt{e_{nOPA}^2 + \left(\sqrt{R} \cdot 4.04\ nV/\sqrt{Hz}\right)^2 + \left(i_{nOPA} \cdot R\right)^2} \quad (6)$$

The reference noise is divided by the first gain stage of 200 at the INA848 to compute the input-referred noise. For reference noise less than 80 nV/√Hz, this contribution can be neglected in the analysis. The given example results in a total reference noise of 29 nV/√Hz, and thus is neglected.

9.2.3 Application Curves

From Figure 9-6, the source resistance is shown to be one main contributor. Figure 9-8 plots all the individual noise contributors depending on the source resistance. The reference voltage noise is negligible.

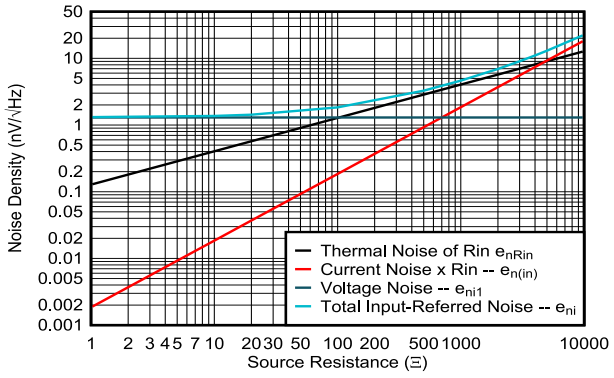


Figure 9-8. Noise Density vs Source Resistance

If the source resistance is below 20 Ω, the voltage noise of the INA (typically 1.3 nV/√Hz) is dominating. If the source resistance is increasing (> 20 Ω) the thermal noise of the source resistance is dominating. At this point the low-noise advantage of the INA848 does not provide additional value. In applications with even higher source resistance (> 1 kΩ), the current noise of the INA starts to dominate, and thus, should be optimized.

10 Power Supply Recommendations

The nominal performance of the INA848 is specified with a supply voltage of ±15 V and midsupply reference voltage. The device operates using power supplies from ±4 V (8 V) to ±18 V (36 V) and non-midsupply reference voltages with excellent performance.

CAUTION

Supply voltages higher than 40 V (±20 V) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in *Section 7.6* of this data sheet.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Take care to make sure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals.
- Noise propagates into analog circuitry through the power pins of the circuit as a whole and of the device. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from +VS to ground is applicable for single-supply applications.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Place the external components (filter components, load) as close to the device as possible.
- Use ground layer to minimize the parasitic inductance of the board.
- Keep the traces as short as possible.

11.2 Layout Example

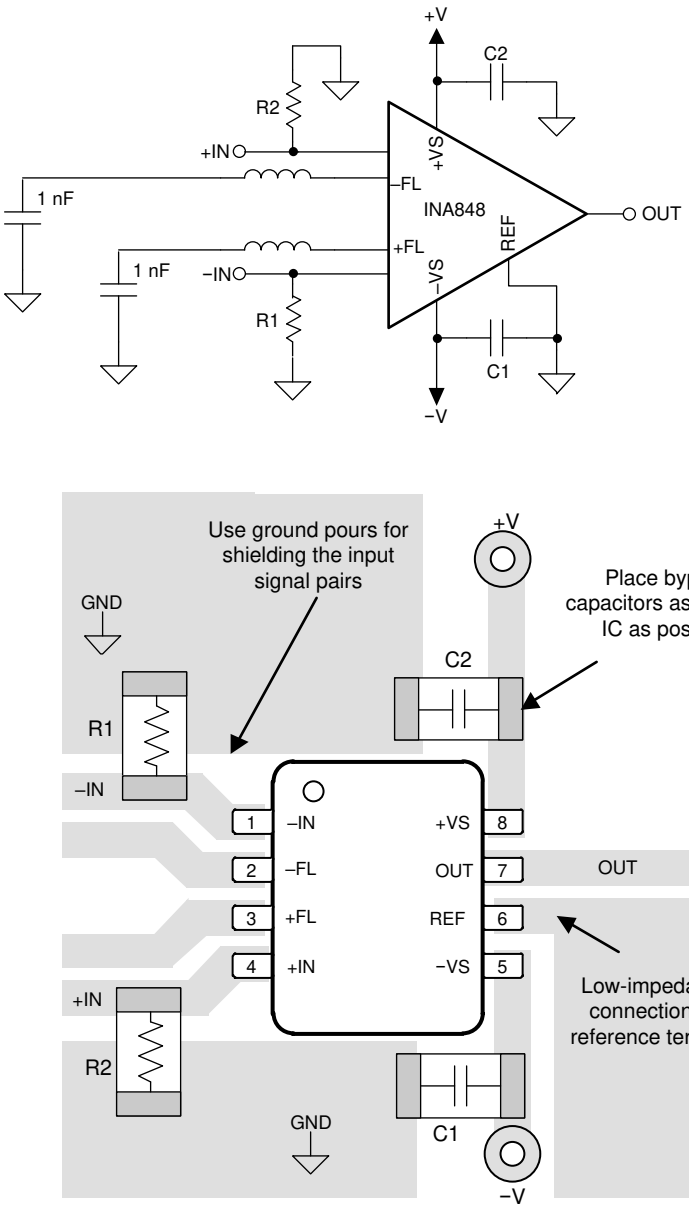


Figure 11-1. Example Schematic and Associated PCB Layout (inductors and capacitors shown on FL pins are optional)

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference*
- Texas Instruments, *OPA191 Low-Power, Precision, 36-V, e-trim CMOS Amplifier*
- Texas Instruments, TINA-TI software folder
- Texas Instruments, INA Common-Mode Range Calculator

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA848ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA848
INA848ID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA848
INA848IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA848
INA848IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA848

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

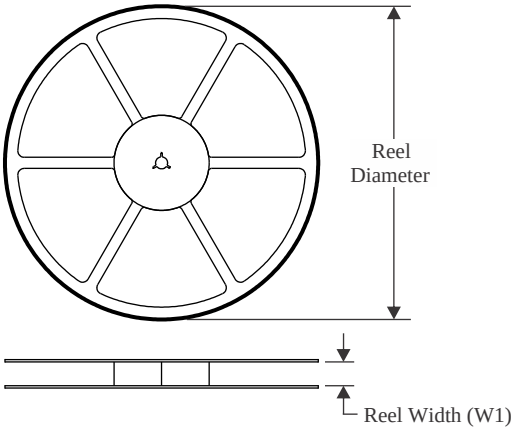
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

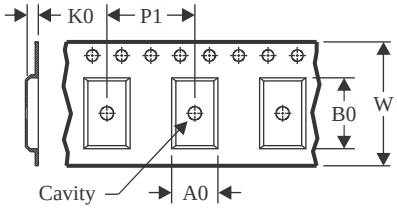
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

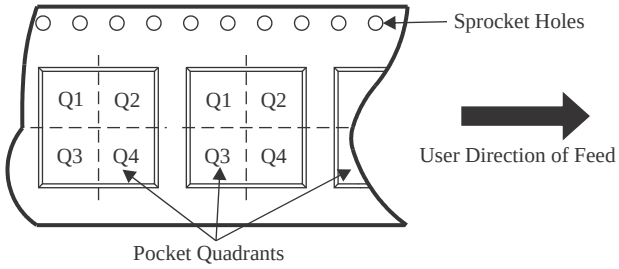


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

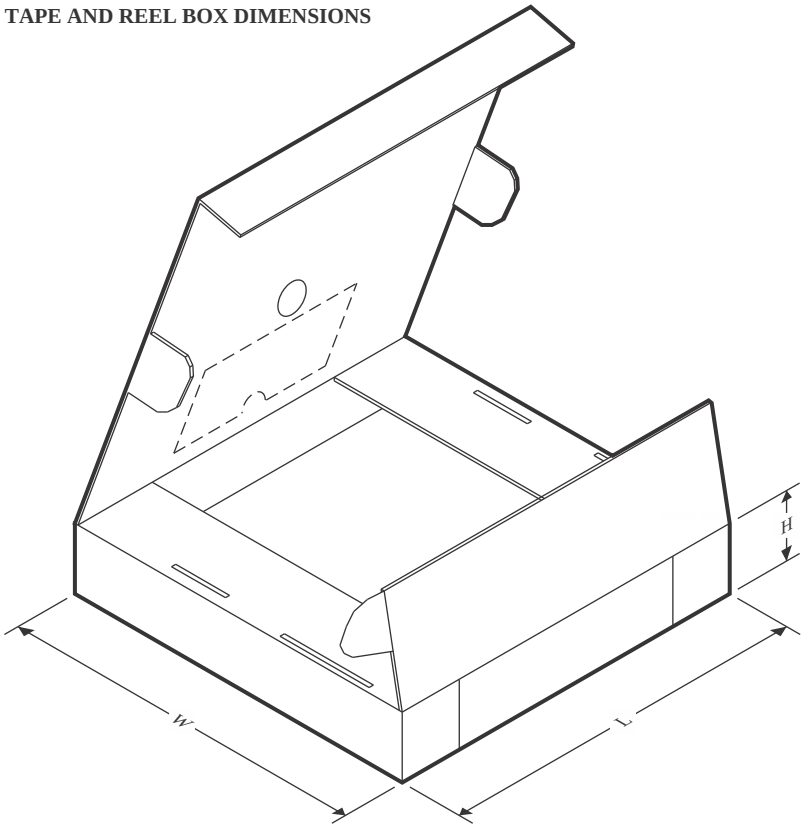
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA848IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

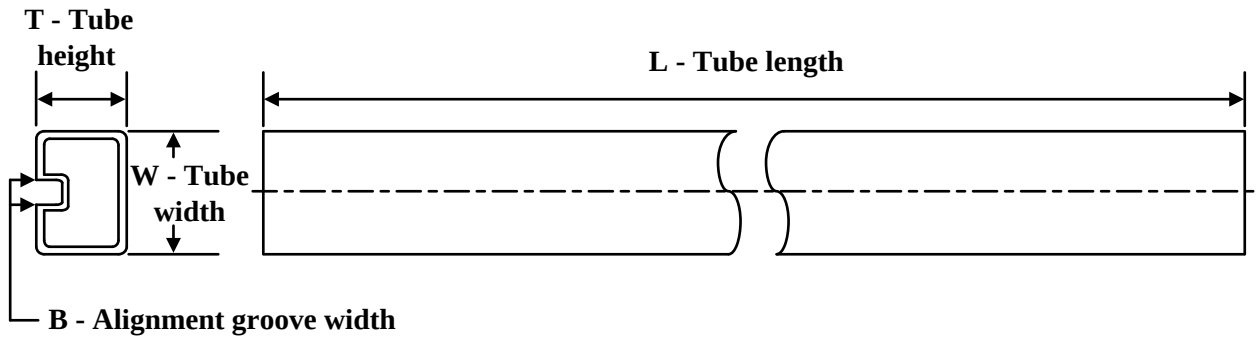
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

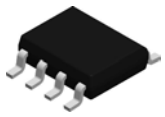
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA848IDR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA848ID	D	SOIC	8	75	506.6	8	3940	4.32
INA848ID.B	D	SOIC	8	75	506.6	8	3940	4.32

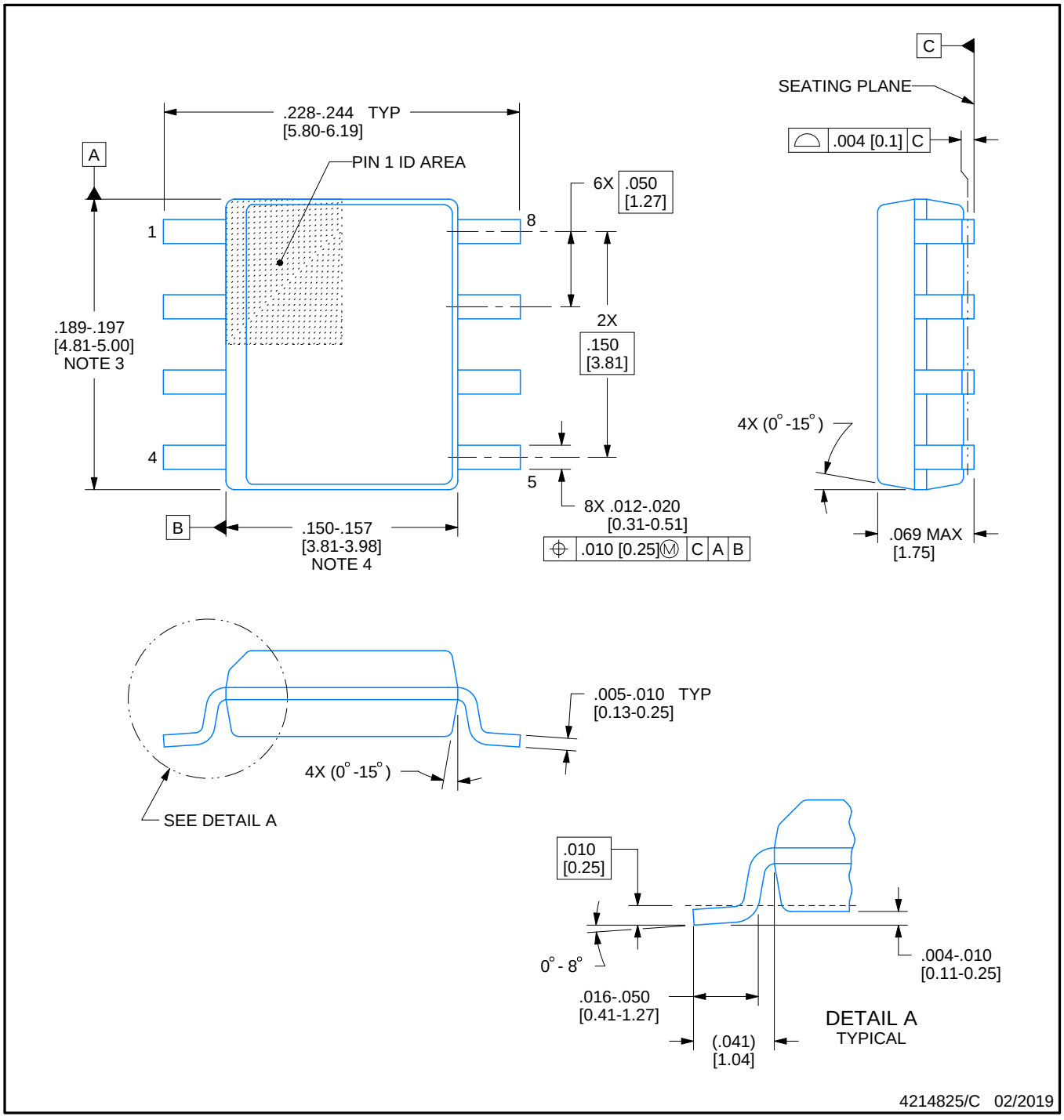


PACKAGE OUTLINE

D0008A

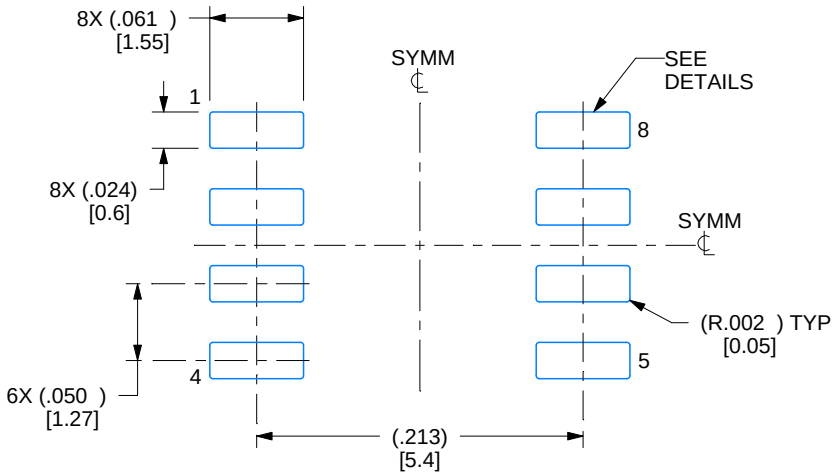
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

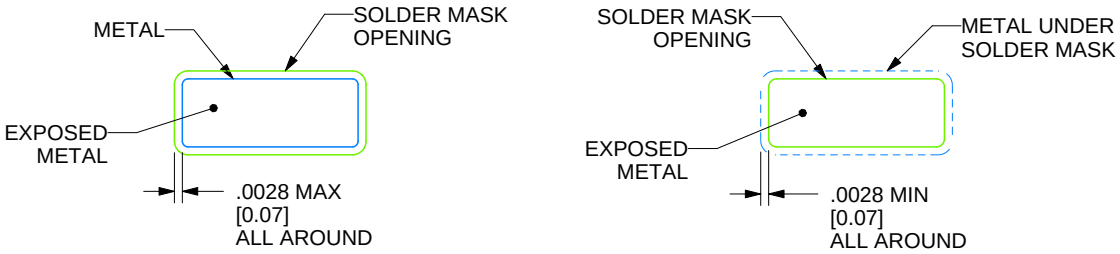


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

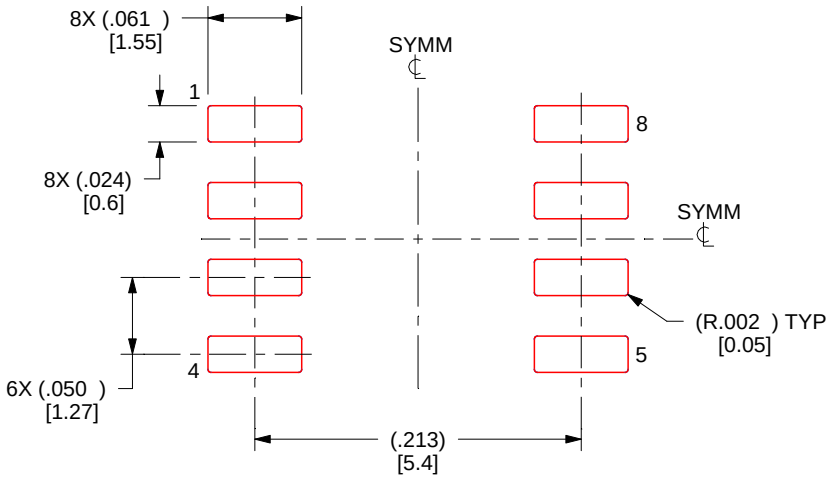
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265