













**INA828** 

#### SBOS792A - AUGUST 2017-REVISED JANUARY 2018

# INA828 50-µV Offset, 7-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier

#### Features

Precision Instrumentation Amplifier Evolution:

 Second Generation: INA828 First Generation: INA128

Low Offset Voltage: 50 µV, MAX

Gain Drift: 5 ppm/ $^{\circ}$ C (G = 1), 50 ppm/ $^{\circ}$ C (G > 1)

Noise: 7 nV/√Hz

Bandwidth: 2 MHz (G = 1), 260 kHz (G = 100)

Stable with 1-nF Capacitive Loads

Inputs Protected Up to ±40 V

Common-Mode Rejection:

- 110 dB, MIN (G = 10)

Power-Supply Rejection: 100 dB, MIN (G = 1)

Supply Current: 650 µA, MAX

Supply Range:

 Single Supply: 4.5 V to 36 V Dual Supply: ±2.25 V to ±18 V

Specified Temperature Range:

-40°C to +125°C

Package: 8-Pin SOIC

## **Applications**

- Industrial Process Controls
- Circuit Breakers
- **Battery Testers**
- **ECG Amplifiers**
- **Power Automation**
- Medical Instrumentation
- Portable Instrumentation

#### 3 Description

The INA828 is a high-precision instrumentation amplifier that offers low power consumption and operates over a very wide single- or dual-supply range. A single external resistor sets any gain from 1 to 1000. The device offers excellent precision due to the use of new super-beta input transistors which provide exceptionally low input offset voltage, offset voltage drift, input bias current, and input voltage and current noise. Additional circuitry protects the inputs against overvoltage up to ±40 V.

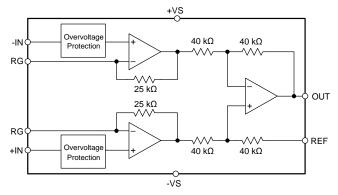
The INA828 is optimized to provide excellent common-mode rejection ratio. At G = 1, the commonmode rejection ratio exceeds 90 dB across the full input common-mode range. The device is well-suited for low-voltage operation from a 5-V single supply as well as dual supplies up to ±18 V. Finally, INA828 is available in an 8-pin SOIC package and specified over the -40°C to +125°C temperature range.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA828	SOIC (8)	4.90 mm × 3.91 mm

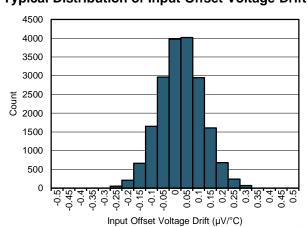
(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### **INA828 Simplified Internal Schematic**



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## Typical Distribution of Input Offset Voltage Drift





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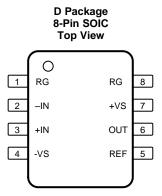
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# 4 Revision History

Cŀ	hanges from Original (August 2017) to Revision A	Page
•	Changed MAX value for G = 1 in "GE" row from "±0.020%" to "±0.025%"	5



# 5 Pin Configuration and Functions



#### **Pin Functions**

PIN		1/0	DESCRIPTION	
NAME	NO.	1/0	DESCRIPTION	
DC	1		Coin potting his Place a gain register between his 4 and his 9	
RG	8	_	Gain setting pin. Place a gain resistor between pin 1 and pin 8.	
-IN	2	I	Negative (inverting) input	
+IN	3	I	Positive (noninverting) input	
-VS	4	_	Negative supply	
REF	5	I	Reference input. This pin must be driven by a low impedance source.	
OUT	6	0	Output	
+VS	7	_	Positive supply	

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#### 6 Specifications

#### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage	Supply voltage		18	V
Cinnal innut nina	Voltage	-40	40	V
Signal input pins	REF pin	-18	18	V
Output short-circuit (2)		Conti	nuous	
	Operating, T <sub>A</sub>	-50	150	
Temperature	Junction, T <sub>J</sub>		175	°C
	Storage, T <sub>stg</sub>	-65	150	

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### 6.2 ESD Ratings

			VALUE	UNIT
V	Floatroatatia diaaharaa	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1500	\/
V <sub>(ESD)</sub>	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	V

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

#### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Cupply voltage	Single supply	4.5	36	V
Supply voltage	Dual supply	±2.25	±18	V
Specified temperature		-40	125	°C
Operating temperature		-50	150	°C

#### 6.4 Thermal Information

		INA828	
	THERMAL METRIC <sup>(1)</sup>	D (SOIC)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.9	°C/W
ΨЈТ	Junction-to-top characterization parameter	20.5	°C/W
ΨЈВ	Junction-to-board characterization parameter	61.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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<sup>(2)</sup> Short-circuit to V<sub>S</sub> / 2.

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



#### 6.5 Electrical Characteristics

at  $T_A = 25^{\circ}$ C.  $V_C = +15$  V.  $R_L = 10$  kO.  $V_{REF} = 0$  V. and G = 1 (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
		G = 100, RTI		20	50	μV
V <sub>osi</sub>	Input stage offset voltage (1)(2)	$T_A = -40$ °C to +125°C <sup>(3)</sup>			90	μV
	voltage	vs temperature, T <sub>A</sub> = -40°C to +125°C			0.5	μV/°C
		G = 1, RTI		50	250	μV
V <sub>oso</sub>	Output stage offset voltage (1)(2)	$T_A = -40$ °C to +125°C <sup>(3)</sup>			500	μV
	voilage	vs temperature, T <sub>A</sub> = -40°C to +125°C			5	μV/°C
	Power-supply rejection	G = 1, RTI	110	120		
DODD		G = 10, RTI	114	130		ID.
PSRR	ratio	G = 100, RTI	130	135		dB
		G = 1000, RTI	136	140		
z <sub>id</sub>	Differential impedance			100    1		GΩ    pF
Z <sub>ic</sub>	Common-mode impedance			100    10		GΩ    pF
	RFI filter, -3-dB frequency			53		MHz
	0(4)		(V-) + 2		(V+) - 2	
V <sub>CM</sub>	Operating input range (4)	$V_S = \pm 2.25 \text{ V to } \pm 18 \text{ V}, T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$	See Fig	jure 48 to Figure 51		V
	Input overvoltage range	$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$			±40	V
	Common-mode rejection ratio	At dc to 60 Hz, RTI, $V_{CM} = (V-) + 2 V$ to $(V+) - 2 V$ , $G = 1$	90	100		- dB
OMBB		At dc to 60 Hz, RTI, $V_{CM} = (V-) + 2 V$ to $(V+) - 2 V$ , $G = 10$	110	120		
CMRR		At dc to 60 Hz, RTI, $V_{CM} = (V-) + 2 V$ to $(V+) - 2 V$ , $G = 100$	130	140		
		At dc to 60 Hz, RTI, $V_{CM} = (V-) + 2 V$ to $(V+) - 2 V$ , $G = 1000$	140	145		
BIAS CU	JRRENT					
	1	$V_{CM} = V_S / 2$		0.15	0.6	
I <sub>B</sub>	Input bias current	$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$			2	nA
	l	$V_{CM} = V_S / 2$		0.15	0.6	A
los	Input offset current	$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$			2	nA
NOISE V	OLTAGE				•	
	Input stage voltage	$f = 1 \text{ kHz}, G = 100, R_S = 0 \Omega$		7		nV/√ <del>Hz</del>
e <sub>NI</sub>	noise <sup>(5)</sup>	$f_B$ = 0.1 Hz to 10 Hz, G = 100, $R_S$ = 0 $\Omega$		0.14		$\mu V_{PP}$
	Output stage voltage	$f = 1 \text{ kHz}, R_S = 0 \Omega$		90		nV/√ <del>Hz</del>
e <sub>NO</sub>	noise <sup>(5)</sup>	$f_B$ = 0.1 Hz to 10 Hz, $R_S$ = 0 $\Omega$		7.7		$\mu V_{PP}$
	Noise surrent	f = 1 kHz		170		fA/√Hz
I <sub>n</sub>	Noise current	f <sub>B</sub> = 0.1 Hz to 10 Hz, G = 100		4.7		pA <sub>PP</sub>
GAIN						
G	Gain equation		1	+ (50 k $\Omega$ / R $_{G}$ )		V/V
	Range of gain		1		1000	V/V
		$G = 1, V_0 = \pm 10 V$		±0.005%	±0.025%	
0.5	0 :	G = 10, V <sub>O</sub> = ±10 V		±0.025%	±0.15%	
GE	Gain error	G = 100, V <sub>O</sub> = ±10 V		±0.025%	±0.15%	
		G = 1000, V <sub>O</sub> = ±10 V		±0.05%		
	0 : 4 : (6)	$G = 1$ , $T_A = -40$ °C to $+125$ °C			±5	/0.0
	Gain vs temperature (6)	G > 1, T <sub>A</sub> = -40°C to +125°C			±50	ppm/°C

- (1) Total offset, referred-to-input (RTI): V<sub>OS</sub> = (V<sub>OSI</sub>) + (V<sub>OSO</sub> / G).
   (2) Offset drifts are uncorrelated. Input-referred offset drift is calculated using: ΔV<sub>OS(RTI)</sub> = √[ΔV<sub>OSI</sub><sup>2</sup> + (ΔV<sub>OSO</sub> / G)<sup>2</sup>]
- Specified by characterization.
- Input voltage range of the INA828 input stage. The input range depends on the common-mode voltage, differential voltage, gain, and reference voltage. See *Typical Characteristic* curves Figure 48 through Figure 51 for more information. Total RTI voltage noise is equal to:  $e_{N(RTI)} = \sqrt{[e_{NO} / G)^2]}$

Product Folder Links: INA828

- The values specified for G > 1 do not include the effects of the external gain-setting resistor, R<sub>G</sub>.



# **Electrical Characteristics (continued)**

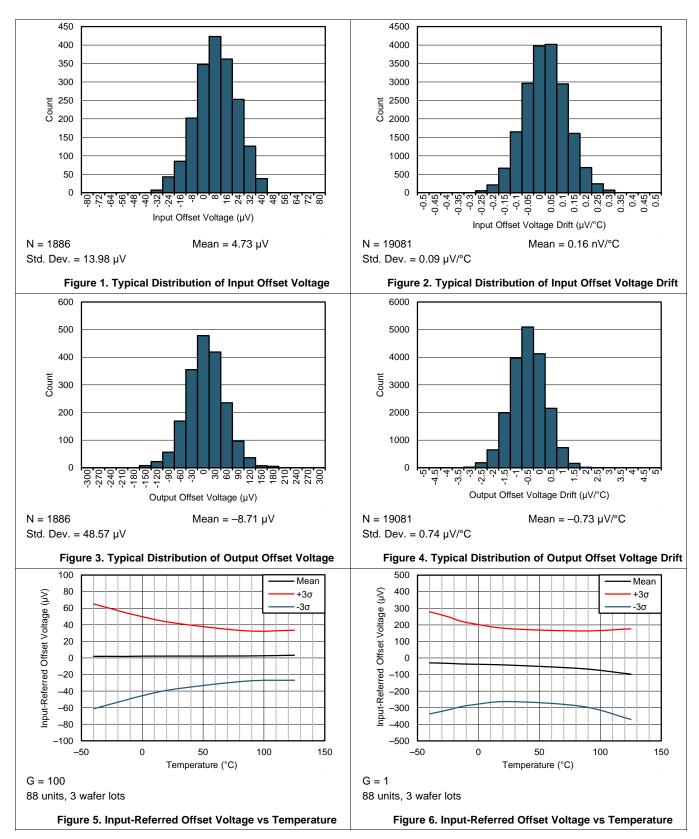
at  $T_A = 25$ °C,  $V_S = \pm 15$  V,  $R_L = 10$  k $\Omega$ ,  $V_{REF} = 0$  V, and G = 1 (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
		$G = 1$ to 10, $V_0 = -10$ V to +10 V, $R_L = 10$ kΩ		1	10		
	Cain nanlinaaritu	$G = 100$ , $V_O = -10$ V to +10 V, $R_L = 10$ k $\Omega$			15		
	Gain nonlinearity	$G = 1000, V_0 = -10 \text{ V to } +10 \text{ V}, R_L = 10 \text{ k}\Omega$			20	ppm	
		G = 1 to 100, $V_O = -10 \text{ V}$ to +10 V, $R_L = 2 \text{ k}\Omega$		30			
OUTP	UT				·		
	Voltage swing		(V-) + 0.15		(V+) - 0.15	V	
	Load capacitance stability			1000		pF	
Z <sub>O</sub>	Closed-loop output impedance	f = 10 kHz		1.3		Ω	
I <sub>SC</sub>	Short-circuit current	Continuous to V <sub>S</sub> / 2		±18		mA	
FREQ	UENCY RESPONSE						
		G = 1		2.0		MHz	
DW	Bandwidth, -3 dB	G = 10		640		kHz	
BW		G = 100		260			
		G = 1000		33			
SR	Slew rate	G = 1, V <sub>O</sub> = ±10 V		1.2		V/µs	
		0.01%, G = 1 to 100, V <sub>STEP</sub> = 10 V		12			
	Cattling time	0.01%, G = 1000, V <sub>STEP</sub> = 10 V		40		μs	
t <sub>S</sub>	Settling time	0.001%, G = 1 to 100, V <sub>STEP</sub> = 10 V		16			
		0.001%, G = 1000, V <sub>STEP</sub> = 10 V		50			
REFE	RENCE INPUT				·		
R <sub>IN</sub>	Input impedance			40		kΩ	
	Voltage range		(V-)		(V+)	V	
	Gain to output			1		V/V	
	Reference gain error			0.01%			
POWE	R SUPPLY						
\/	Power cumply volters	Single supply	4.5		36	V	
V <sub>S</sub>	Power-supply voltage	Dual supply	±2.25		±18	v	
	Ouissant ourrent	V <sub>IN</sub> = 0 V		600	650		
ΙQ	Quiescent current	vs temperature, $T_A = -40^{\circ}\text{C}$ to +125°C			850	μΑ	



#### 6.6 Typical Characteristics

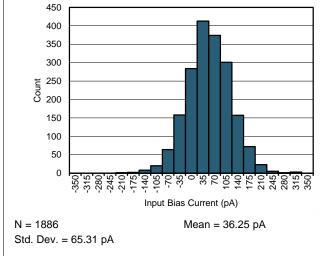
At  $T_A = 25$ °C,  $V_S = \pm 15$  V,  $R_L = 10$  k $\Omega$ ,  $V_{REF} = 0$  V, and G = 1 (unless otherwise noted)



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## **Typical Characteristics (continued)**

At  $T_A = 25$ °C,  $V_S = \pm 15$  V,  $R_L = 10$  k $\Omega$ ,  $V_{REF} = 0$  V, and G = 1 (unless otherwise noted)



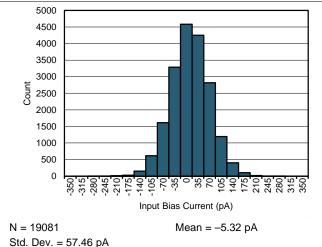
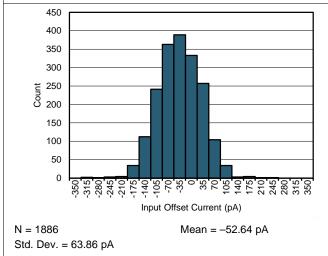


Figure 7. Typical Distribution of Input Bias Current (25°C)

Figure 8. Typical Distribution of Input Bias Current (90°C)



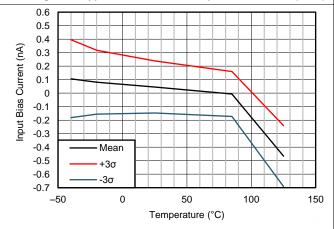


Figure 9. Typical Distribution of Input Offset Current

Figure 10. Input Bias Current vs Temperature

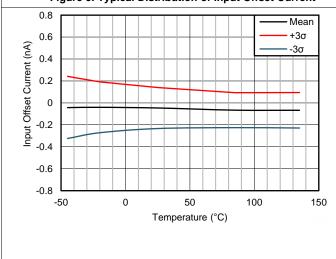


Figure 11. Input Offset Current vs Temperature

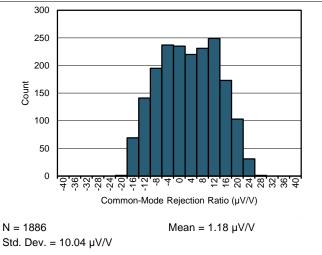
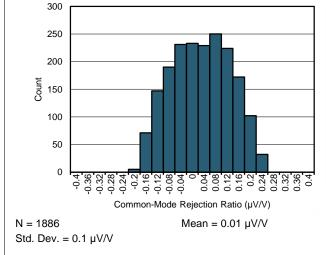


Figure 12. Typical CMRR Distribution (G = 1)



## **Typical Characteristics (continued)**

At  $T_A = 25$ °C,  $V_S = \pm 15$  V,  $R_L = 10$  k $\Omega$ ,  $V_{REF} = 0$  V, and G = 1 (unless otherwise noted)



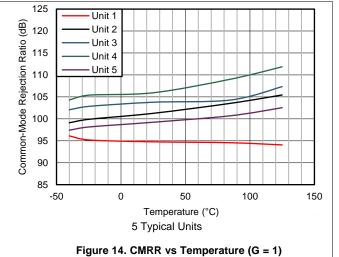
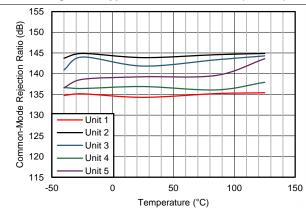
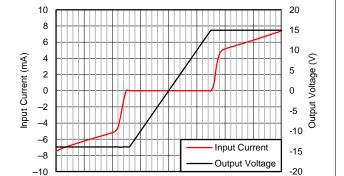


Figure 13. Typical CMRR Distribution (G = 100)





0

Input Voltage (V)

-10

-30

-40

-20

Figure 15. CMRR vs Temperature (G = 100)

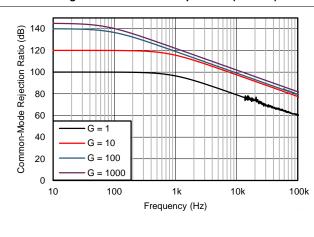
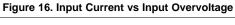


Figure 17. CMRR vs Frequency (RTI)



10

20

30

40

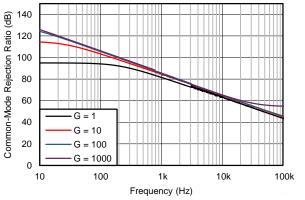
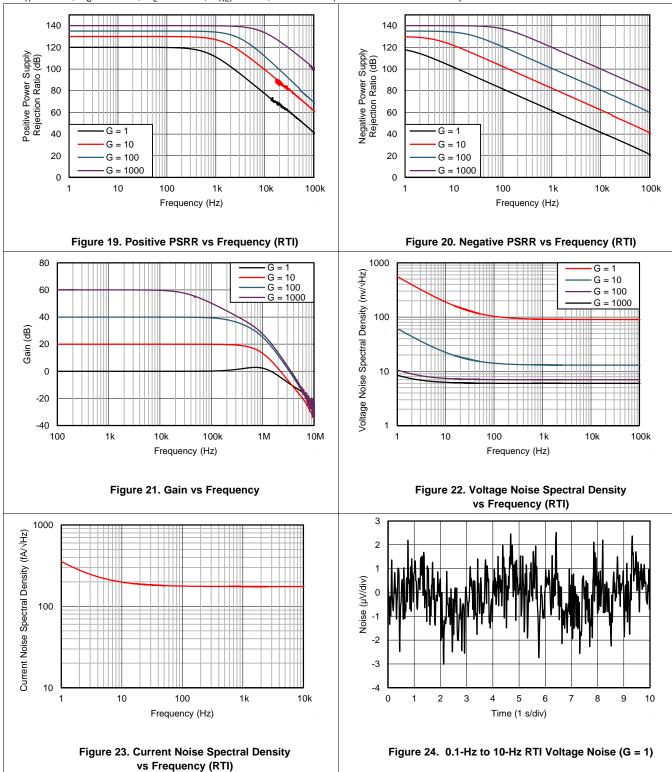


Figure 18. CMRR vs Frequency (RTI, 1-kΩ Source Imbalance)

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#### **Typical Characteristics (continued)**

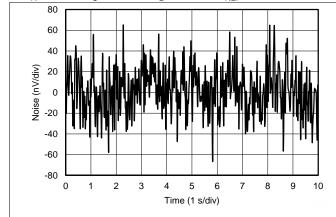
At  $T_A = 25$ °C,  $V_S = \pm 15$  V,  $R_L = 10$  k $\Omega$ ,  $V_{REF} = 0$  V, and G = 1 (unless otherwise noted)





#### **Typical Characteristics (continued)**

At  $T_A = 25$ °C,  $V_S = \pm 15$  V,  $R_L = 10$  k $\Omega$ ,  $V_{REF} = 0$  V, and G = 1 (unless otherwise noted)



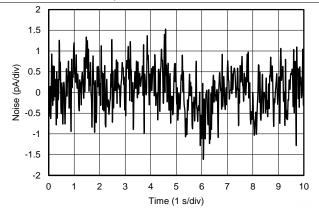
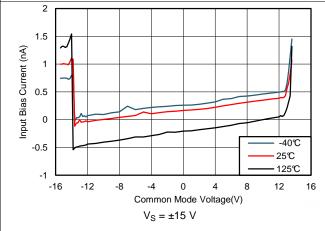


Figure 25. 0.1-Hz to 10-Hz RTI Voltage Noise (G = 1000)

Figure 26. 0.1-Hz to 10-Hz RTI Current Noise



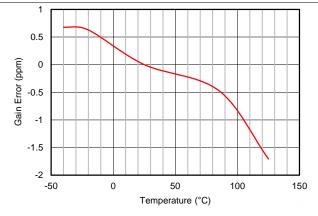
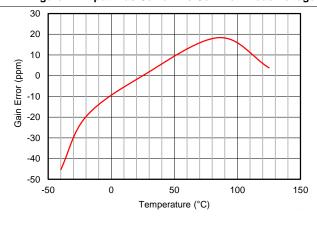


Figure 27. Input Bias Current vs Common-Mode Voltage

Figure 28. Gain Error vs Temperature (G = 1)



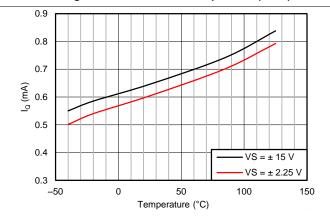


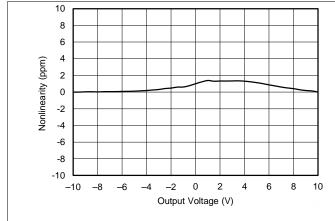
Figure 29. Gain Error vs Temperature (G = 100)

Figure 30. Supply Current vs Temperature

# **ISTRUMENTS**

#### **Typical Characteristics (continued)**

At  $T_A = 25$ °C,  $V_S = \pm 15$  V,  $R_L = 10$  k $\Omega$ ,  $V_{REF} = 0$  V, and G = 1 (unless otherwise noted)



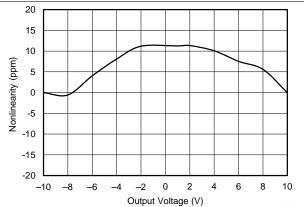
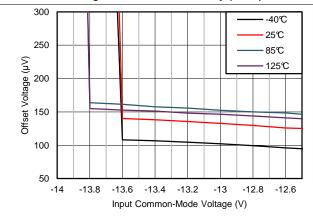


Figure 31. Gain Nonlinearity (G = 1)

Figure 32. Gain Nonlinearity (G = 100)



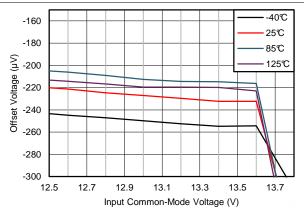


Figure 33. Offset Voltage vs Negative Common-Mode Voltage

Figure 34. Offset Voltage vs Positive Common-Mode Voltage

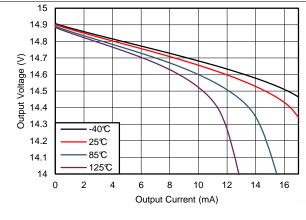


Figure 35. Positive Output Voltage Swing vs Output Current

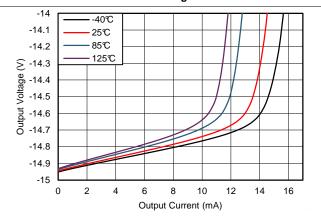
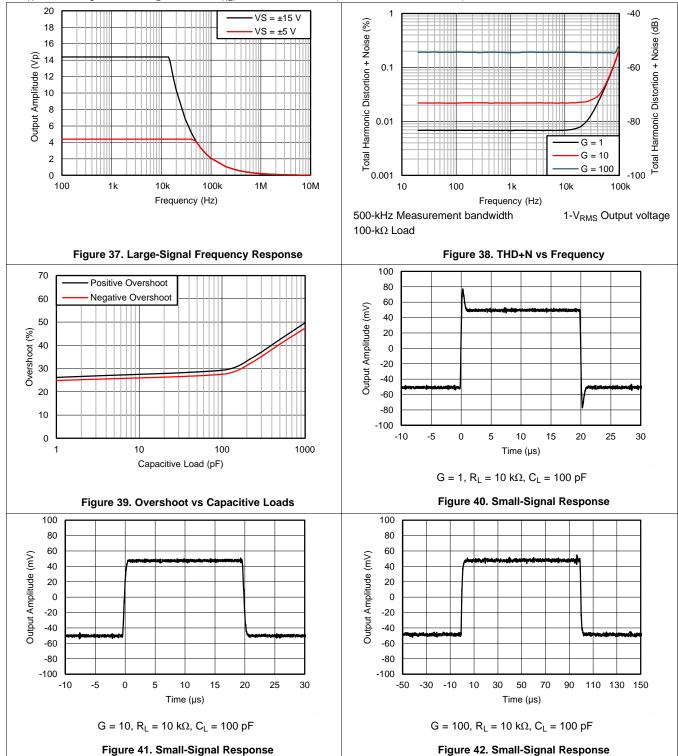


Figure 36. Negative Output Voltage Swing vs Output Current



#### **Typical Characteristics (continued)**

At  $T_A = 25$ °C,  $V_S = \pm 15$  V,  $R_L = 10$  k $\Omega$ ,  $V_{REF} = 0$  V, and G = 1 (unless otherwise noted)

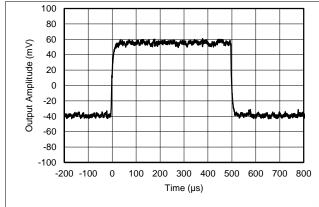


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#### **Typical Characteristics (continued)**

At  $T_A = 25$ °C,  $V_S = \pm 15$  V,  $R_L = 10$  k $\Omega$ ,  $V_{REF} = 0$  V, and G = 1 (unless otherwise noted)





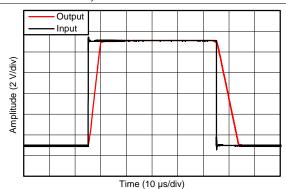


Figure 44. Large Signal Step Response



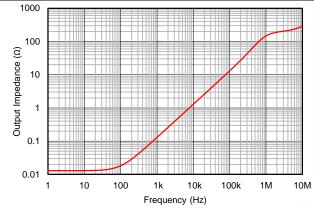


Figure 45. Closed-Loop Output Impedance

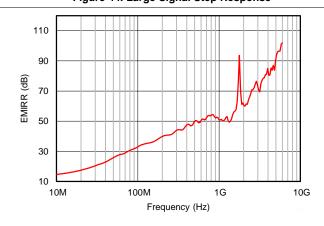


Figure 46. Differential-Mode EMI Rejection Ratio

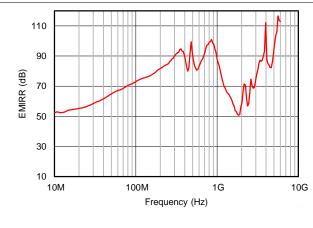


Figure 47. Common-Mode EMI Rejection Ratio

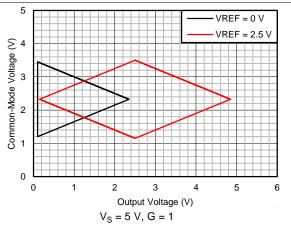
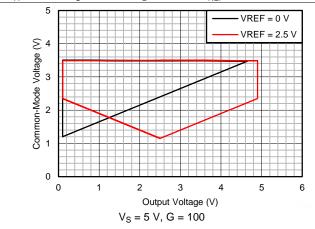


Figure 48. Input Common-Mode Voltage vs Output Voltage



#### **Typical Characteristics (continued)**

At  $T_A = 25$ °C,  $V_S = \pm 15$  V,  $R_L = 10$  k $\Omega$ ,  $V_{REF} = 0$  V, and G = 1 (unless otherwise noted)



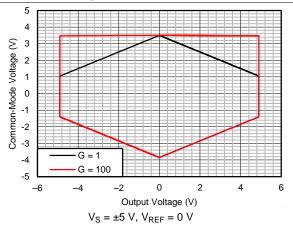


Figure 49. Input Common-Mode Voltage vs Output Voltage

Figure 50. Input Common-Mode Voltage vs Output Voltage

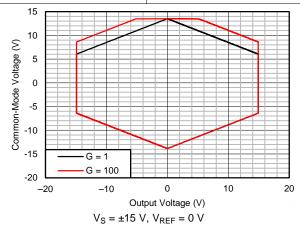


Figure 51. Input Common-Mode Voltage vs Output Voltage

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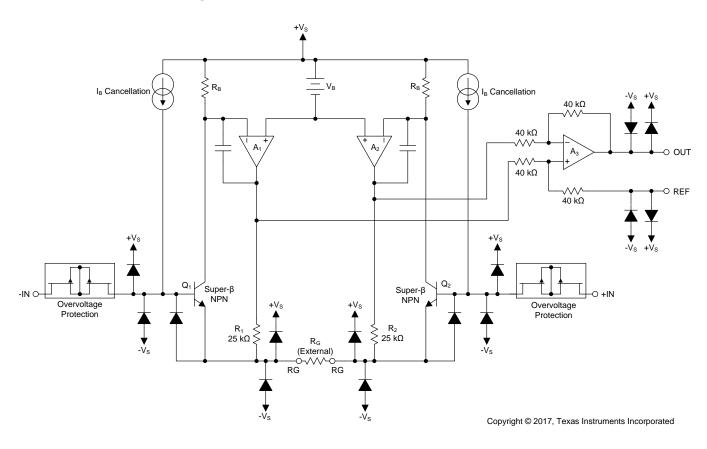
## 7 Detailed Description

#### 7.1 Overview

The INA828 is a monolithic precision instrumentation amplifier incorporating a current-feedback input stage and a 4-resistor difference amplifier output stage. The differential input voltage is buffered by  $Q_1$  and  $Q_2$  and is forced across  $R_G$ , which causes a signal current to flow through  $R_G$ ,  $R_1$ , and  $R_2$ . The output difference amplifier,  $A_3$ , removes the common-mode component of the input signal and refers the output signal to the REF terminal. The  $V_{BE}$  and voltage drop across  $R_1$  and  $R_2$  produce output voltages on  $A_1$  and  $A_2$  that are approximately 0.8 V lower than the input voltages.

Each input is protected by two field-effect transistors (FETs) that provide a low series resistance under normal signal conditions, and preserve excellent noise performance. When excessive voltage is applied, these transistors limit input current to approximately 8 mA.

#### 7.2 Functional Block Diagram





#### 7.3 Feature Description

#### 7.3.1 Setting the Gain

Figure 52 shows that the gain of the INA828 is set by a single external resistor, R<sub>G</sub>, connected between the RG pins (pins 1 and 8).

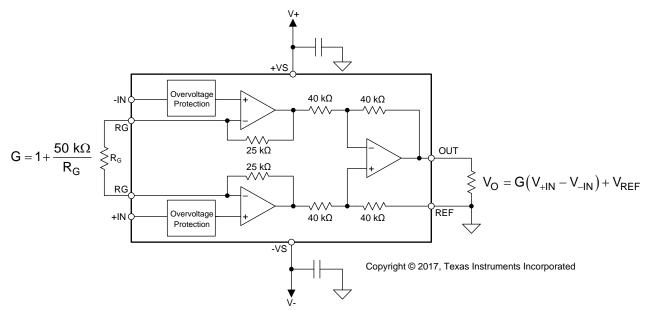


Figure 52. Simplified Diagram of the INA828 With Gain and Output Equations

The value of R<sub>G</sub> is selected according to:

$$G = 1 + \frac{50 \text{ k}\Omega}{R_G} \tag{1}$$

Table 1 lists several commonly-used gains and resistor values. The  $50-k\Omega$  term in Equation 1 comes from the sum of the two internal  $25-k\Omega$  feedback resistors. These on-chip resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficients of these resistors are included in the gain accuracy and drift specifications of the INA828.

**Table 1. Commonly-Used Gains and Resistor Values** 

DESIRED GAIN	R <sub>G</sub> (Ω)	NEAREST 1% R <sub>G</sub> (Ω)
1	NC	NC
2	50 k	49.9 k
5	12.5 k	12.4 k
10	5.556 k	5.49 k
20	2.632 k	2.61 k
50	1.02 k	1.02 k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9

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#### 7.3.1.1 Gain Drift

The stability and temperature drift of the external gain setting resistor,  $R_G$ , also affects gain. The contribution of  $R_G$  to gain accuracy and drift can be determined from Equation 1.

The best gain drift of 5 ppm/°C (maximum) can be achieved when the INA828 uses G=1 without  $R_G$  connected. In this case, gain drift is limited only by the slight mismatch of the temperature coefficient of the integrated  $40\text{-k}\Omega$  resistors in the differential amplifier ( $A_3$ ). At gains greater than 1, gain drift increases as a result of the individual drift of the 25-k $\Omega$  resistors in the feedback of  $A_1$  and  $A_2$ , relative to the drift of the external gain resistor  $R_G$ . The low temperature coefficient of the internal feedback resistors significantly improves the overall temperature stability of applications using gains greater than 1 V/V over alternate solutions.

Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance and contribute additional gain error (such as a possible unstable gain error) at gains of approximately 100 or greater. To assure stability, avoid parasitic capacitance of more than a few picofarads at  $R_G$  connections. Careful matching of any parasitics on both  $R_G$  pins maintains optimal CMRR over frequency; see *Typical Characteristics*, Figure 17.

#### 7.3.2 EMI Rejection

Texas Instruments developed a method to accurately measure the immunity of an amplifier over a broad frequency spectrum, extending from 10 MHz to 6 GHz. This method uses an EMI rejection ratio (EMIRR) to quantify the ability of the INA828 to reject EMI. The offset resulting from an input EMI signal can be calculated using Equation 2:

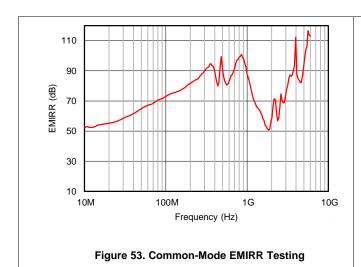
$$\Delta V_{OS} = \left(\frac{V_{RF\_PEAK}^2}{100 \text{ mV}_P}\right) \cdot 10^{-\left(\frac{EMIRR \text{ (dB)}}{20}\right)}$$

where

V<sub>RF PEAK</sub> is the peak amplitude of the input EMI signal.

(2)

Figure 53 and Figure 54 show the INA828 EMIRR graph for both differential and common-mode EMI rejection across this frequency range. Table 2 shows the EMIRR values for the INA828 at frequencies commonly encountered in real-world applications. Applications listed in Table 2 can be centered on or operated near the particular frequency shown. Depending on the end-system requirements, additional EMI filters may be required near the signal inputs of the system, as well as incorporating known good practices such as using short traces, low-pass filters, and damping resistors combined with parallel and shielded signal routing.



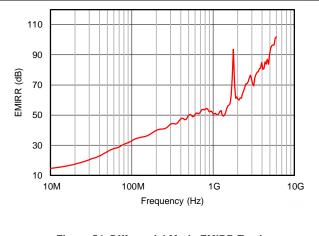


Figure 54. Differential Mode EMIRR Testing

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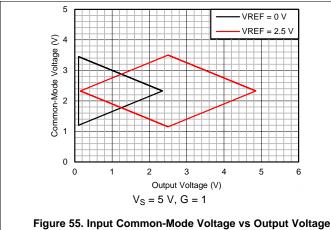


Table 2. INA828 EMIRR for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	DIFFERENTIAL EMIRR	COMMON-MODE EMIRR
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultrahigh-frequency (UHF) applications	48 dB	87 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (up to 1.6 GHz), GSM, aeronautical mobile, UHF applications		98 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	94 dB	51 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth <sup>®</sup> , mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	66 dB	57 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	79 dB	87 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	90 dB	92 dB

#### 7.3.3 Input Common-Mode Range

The linear input voltage range of the INA828 input circuitry extends within 2 Volts of both power supplies and maintains excellent common-mode rejection throughout this range. The common-mode range for the most common operating conditions are shown in Figure 55, Figure 50, and Figure 51. The common-mode range for other operating conditions is best calculated using the INA common-mode range calculating tool. The INA828 device can operate over a wide range of power supplies and VREF configurations, thus providing a comprehensive guide to common-mode range limits for all possible conditions is impractical.



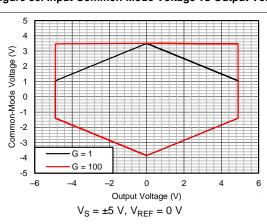


Figure 57. Input Common-Mode Voltage vs Output Voltage

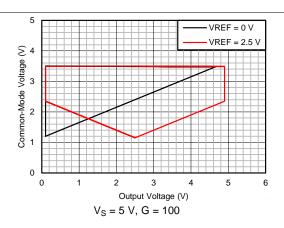


Figure 56. Input Common-Mode Voltage vs Output Voltage

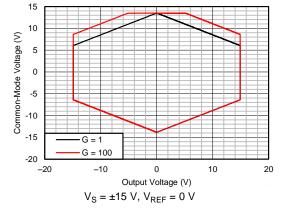


Figure 58. Input Common-Mode Voltage vs Output Voltage



#### 7.3.4 Input Protection

The inputs of the INA828 device are individually protected for voltages up to ±40 V. For example, a condition of -40 V on one input and 40 V on the other input does not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. If the input is overloaded, the protection circuitry limits the input current to a value of approximately 8 mA.

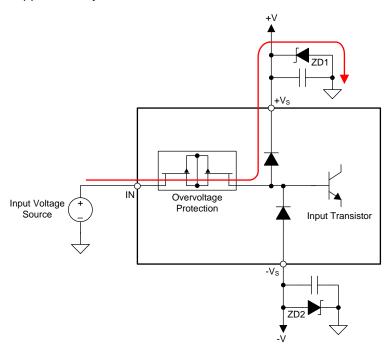


Figure 59. Input Current Path During an Overvoltage Condition

During an input overvoltage condition, current flows through the input protection diodes into the power supplies, see Figure 59. If the power supplies are unable to sink current, then Zener diode clamps (ZD1 and ZD2 in Figure 59) must be placed on the power supplies to provide a current pathway to ground. Figure 60 illustrates the input current for input voltages from -40 V to +40 V when the INA828 is powered by ±15-V supplies.

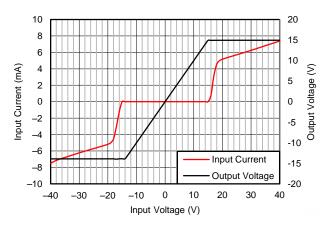


Figure 60. Input Current vs Input Overvoltage



#### 7.3.5 Operating Voltage

The INA828 operates over a power-supply range of 4.5 V to 36 V (±2.25 V to ±18 V).

#### **CAUTION**

Supply voltages higher than 40 V (±20 V) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in the *Typical Characteristics* section of this data sheet.

#### 7.4 Device Functional Modes

The INA828 has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V  $(\pm 2.25 \text{ V})$ . The maximum power-supply voltage for the INA828 is 36 V  $(\pm 18 \text{ V})$ .

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#### 8 Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

#### 8.1 Reference Terminal

The output voltage of the INA828 is developed with respect to the voltage on the reference terminal, REF. Often, in dual-supply operation, the reference pin (pin 6) is connected to the low-impedance system ground. In single-supply operation, offsetting the output signal to a precise mid-supply level is useful (for example, 2.5 V in a 5-V supply environment). To accomplish this level shift, a voltage source must be connected to the REF pin to level-shift the output so that the INA828 can drive a single-supply ADC.

The voltage source applied to the reference terminal must have a low output impedance. As illustrated in Figure 61, any resistance at the reference terminal (shown as  $R_{REF}$  in Figure 61) is in series with one of the internal 40-k $\Omega$  resistors.

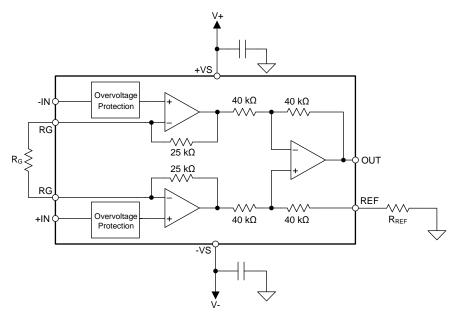


Figure 61. Parasitic Resistance Shown at the Reference Terminal

The parasitic resistance at the reference terminal,  $R_{REF}$ , creates an imbalance in the 4 resistors of the internal difference amplifier, resulting in degraded common-mode rejection ratio (CMRR). Figure 62 shows the degradation in CMRR of the INA828 for increasing resistance at the reference terminal. For the best performance, keep the source impedance to the REF terminal,  $R_{REF}$ , below 5  $\Omega$ .



#### **Reference Terminal (continued)**

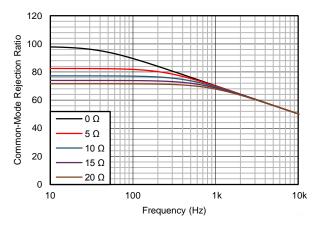


Figure 62. The Effect of Increasing Resistance at the Reference Terminal

Voltage reference ICs are an excellent option for providing a low-impedance voltage source for the reference terminal. However, if a resistor voltage divider is used to generate a reference voltage, it must be buffered by an op amp as shown in Figure 63 to avoid CMRR degradation.

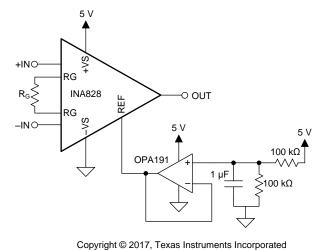


Figure 63. Using an Op Amp to Buffer Reference Voltages

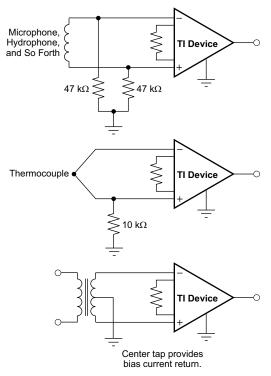
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#### 8.2 Input Bias Current Return Path

The input impedance of the INA828 is extremely high—approximately 100 G $\Omega$ . However, a path must be provided for the input bias current of both inputs. This input bias current is typically 150 pA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 64 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA828, and the input amplifiers saturate. If the differential source resistance is low, the bias current return path can be connected to one input (as shown in the thermocouple example in Figure 64). With a higher source impedance, using two equal resistors provides a balanced input with possible advantages of a lower input offset voltage as a result of bias current and better high-frequency common-mode rejection.



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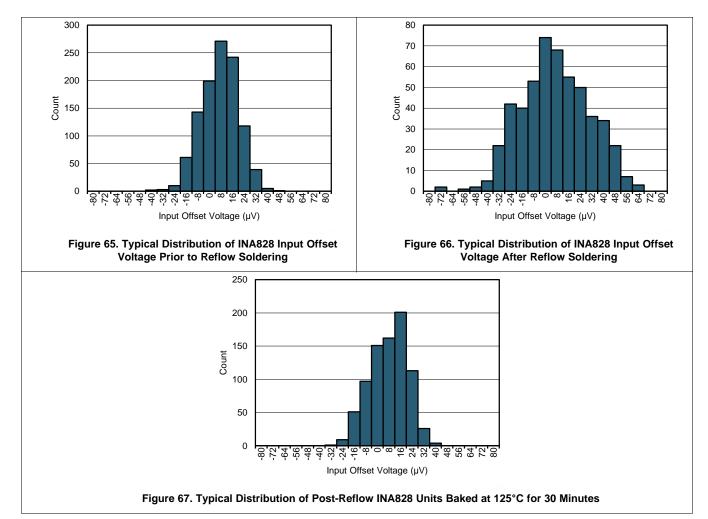
Figure 64. Providing an Input Common-Mode Current Path

24 Su



#### 8.3 PCB Assembly Effects on Precision

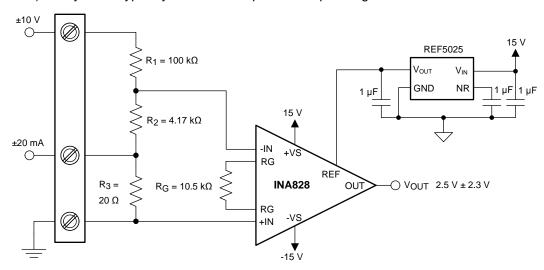
The printed-circuit board (PCB) assembly process, including reflow soldering, imparts thermal stresses on the INA828 which can degrade the precision of the device and must be considered in the development of very-high-precision systems. Baking the PCBs after the assembly process can restore the precision of the device to pre-assembly values. Figure 65, Figure 66, and Figure 67 illustrate the effect of reflow soldering on the typical distribution of input offset voltage of the INA828. Figure 65 shows the distribution of input offset voltage for a set of INA828 devices prior to the PCB assembly process. Exposing the INA828 to a JEDEC-standard thermal profile for reflow soldering produces the histogram shown in Figure 66 on another set of INA828 devices. The standard deviation of input offset voltage has almost doubled due to the thermal stress imparted to the INA828 from the reflow process. However, baking INA828 units for 30 minutes at 125°C after the reflow soldering process produced the distribution given in Figure 67. The post-reflow bake restored the standard deviation of the input offset voltage to pre-assembly levels.





#### 8.4 Typical Application

Figure 68 shows a three-terminal programmable-logic controller (PLC) design for the INA828. This PLC reference design accepts inputs of ±10 V or ±20 mA. The output is a single-ended voltage of 2.5 V ±2.3 V (or 200 mV to 4.8 V). Many PLCs typically have these input and output ranges.



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Figure 68. PLC Input (±10 V, 4 mA to 20 mA)

#### 8.4.1 Design Requirements

For this application, the design requirements are:

- 4-mA to 20-mA input with less than 20-Ω burden
- ±20-mA input with less than 20-Ω burden
- $\pm 10$ -V input with impedance of approximately 100 k $\Omega$
- Maximum 4-mA to 20-mA or ±20-mA burden voltage equal to ±0.4 V
- Output range within 0 V to 5 V

#### 8.4.2 Detailed Design Procedure

There are two modes of operation for the circuit shown in Figure 68: current input and voltage input. This design requires  $R_1 >> R_2 >> R_3$ . Given this relationship, Equation 3 calculates the current input mode transfer function.

$$V_{OUT-I} = V_D \times G + V_{REF} = -(I_{IN} \times R_3) \times G + V_{REF}$$

where

- G represents the gain of the instrumentation amplifier
- V<sub>D</sub> represents the differential voltage at the INA828 inputs
- V<sub>REF</sub> is the voltage at the INA828 REF pin

Equation 4 shows the transfer function for the voltage input mode.

$$V_{OUT-V} = V_D \times G + V_{REF} = -\left(V_{IN} \times \frac{R_2}{R_1 + R_2}\right) \times G + V_{REF}$$

where

V<sub>IN</sub> is the input voltage
 (4)

 $R_1$  sets the input impedance of the voltage input mode. The minimum typical input impedance is 100 k $\Omega$ . 100 k $\Omega$  is selected for  $R_1$  because increasing the  $R_1$  value also increases noise. The value of  $R_3$  must be extremely small compared to  $R_1$  and  $R_2$ . 20  $\Omega$  for  $R_3$  is selected because that resistance value is much smaller than  $R_1$  and yields an input voltage of ±400 mV when operated in current mode (±20 mA).



#### **Typical Application (continued)**

Use Equation 5 to calculate  $R_2$  given  $V_D = \pm 400$  mV,  $V_{IN} = \pm 10$  V, and  $R_1 = 100$  k $\Omega$ .

$$V_{D} = V_{IN} \times \frac{R_{2}}{R_{1} + R_{2}} \rightarrow R_{2} = \frac{R_{1} \times V_{D}}{V_{IN} - V_{D}} = 4.167 \text{ k}\Omega$$
(5)

The value obtained from Equation 5 is not a standard 0.1% value, so 4.17 k $\Omega$  is selected. R<sub>1</sub> and R<sub>2</sub> also use 0.1% tolerance resistors to minimize error.

Use Equation 6 to calculate the ideal gain of the instrumentation amplifier.

$$G = \frac{V_{OUT} - V_{REF}}{V_{D}} = \frac{4.8 \text{ V} - 2.5 \text{ V}}{400 \text{ mV}} = 5.75 \frac{\text{V}}{\text{V}}$$
(6)

Equation 7 calculates the gain-setting resistor value using the INA828 gain equation, Equation 1.

$$R_{G} = \frac{50 \text{ k}\Omega}{G - 1} = \frac{50 \text{ k}\Omega}{5.75 - 1} = 10.5 \text{ k}\Omega \tag{7}$$

10.5 k $\Omega$  is a standard 0.1% resistor value that can be used in this design.

#### 8.4.3 Application Curves

Figure 69 and Figure 70 show typical characteristic curves for the circuit in Figure 68.

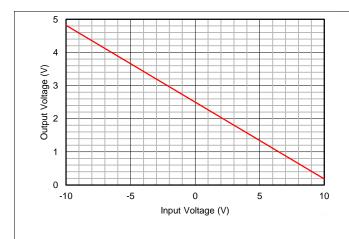


Figure 69. PLC Output Voltage vs Input Voltage

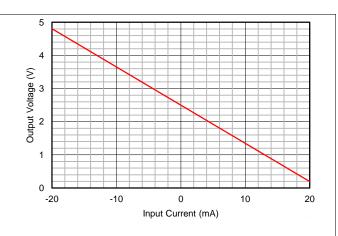


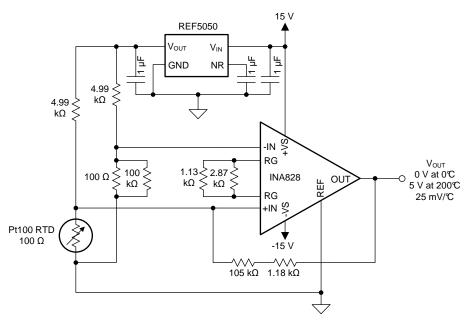
Figure 70. PLC Output Voltage vs Input Current



#### 8.5 Other Application Examples

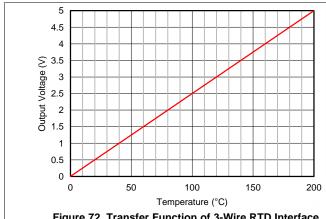
#### 8.5.1 Resistance Temperature Detector Interface

Figure 71 illustrates a 3-wire interface circuit for resistance temperature detectors (RTDs). The circuit incorporates analog linearization and has an output voltage range from 0 to 5 V. The linearization technique employed is described in Analog linearization of resistance temperature detectors. Series and parallel combinations of standard 1% resistor values are used to achieve less than 0.02°C of error over a 200°C temperature span.



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Figure 71. A 3-Wire Interface for RTDs With Analog Linearization



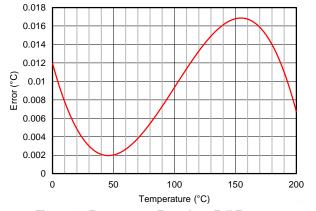


Figure 72. Transfer Function of 3-Wire RTD Interface

Figure 73. Temperature Error Over Full Temperature Range



#### 9 Power Supply Recommendations

The nominal performance of the INA828 is specified with a supply voltage of ±15 V and mid-supply reference voltage. The device can also be operated using power supplies from ±1.5 V (3 V) to ±18 V (36 V) and non mid-supply reference voltages with excellent performance. Parameters that can vary significantly with operating voltage and reference voltage are illustrated in the *Typical Characteristics* section.

#### 10 Layout

#### 10.1 Layout Guidelines

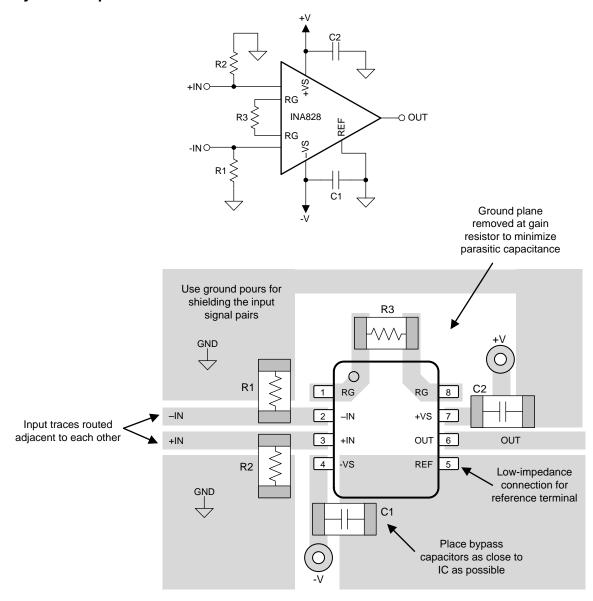
Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices, including:

- Care must be taken to assure that both input paths are well-matched for source impedance and capacitance
  to avoid converting common-mode signals into differential signals. In addition, parasitic capacitance at the
  gain-setting pins can also affect CMRR over frequency. For example, in applications that implement gain
  switching using switches or PhotoMOS<sup>®</sup> relays to change the value of R<sub>G</sub>, select the component so that the
  switch capacitance is as small as possible.
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the device itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for singlesupply applications.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If
  these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in
  parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 74, keeping R<sub>G</sub> close to the pins minimizes parasitic capacitance.
- Keep the traces as short as possible.

Product Folder Links: INA828



#### 10.2 Layout Example



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Figure 74. Example Schematic and Associated PCB Layout



#### 11 Device and Documentation Support

#### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

- REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference
- OPA191 Low-Power, Precision, 36-V, e-trim CMOS Amplifier
- TINA-TI software folder
- INA Common-Mode Range Calculator

#### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community T's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 11.4 Trademarks

E2E is a trademark of Texas Instruments.

Bluetooth is a registered trademark of Bluetooth SIG, Inc.

PhotoMOS is a registered trademark of Panasonic Electric Works Europe AG.

All other trademarks are the property of their respective owners.

#### 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 11.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

#### 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
INA828ID	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA828
INA828ID.B	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA828
INA828IDG4	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA828
INA828IDG4.B	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA828
INA828IDR	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA828
INA828IDR.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA828

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



# **PACKAGE OPTION ADDENDUM**

www.ti.com 10-Nov-2025

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 25-Jul-2025

#### TAPE AND REEL INFORMATION



# TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

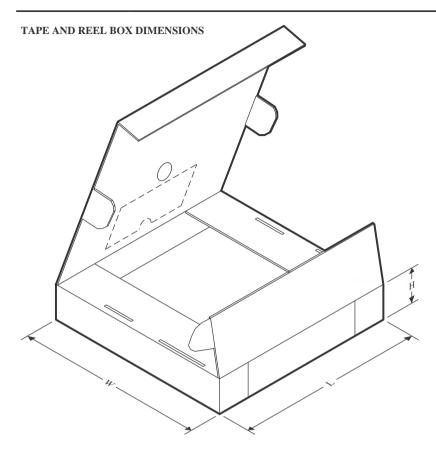


#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA828IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 25-Jul-2025



#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
INA828IDR	SOIC	D	8	2500	353.0	353.0	32.0	

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 25-Jul-2025

#### **TUBE**



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA828ID	D	SOIC	8	75	506.6	8	3940	4.32
INA828ID.B	D	SOIC	8	75	506.6	8	3940	4.32
INA828IDG4	D	SOIC	8	75	506.6	8	3940	4.32
INA828IDG4.B	D	SOIC	8	75	506.6	8	3940	4.32



SMALL OUTLINE INTEGRATED CIRCUIT



#### NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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