INA2227 48V, Dual Channel, 16-Bit, Current, Voltage, Power, and Energy Monitor With an I²C Interface

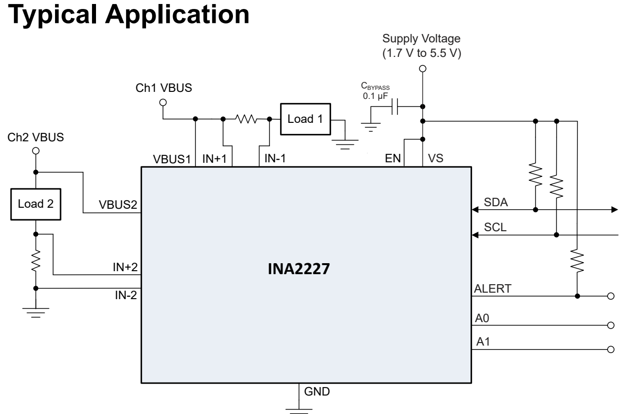
1 Features

- High-side or low-side current sensing
- Operates from a 1.7V to 5.5V power supply
- Reports current, voltage, power, and energy
- Programmable full scale range: 20mV / 80mV
- Input common mode range: –0.3V to 48V
- Current monitoring accuracy:
  - 16-bit ADC resolution
  - 0.5% gain error (maximum)
  - 75μV offset (maximum)
- Power monitoring accuracy:
  - 1% full scale (maximum)
- Energy monitoring accuracy:
  - 1.5% full scale (maximum)
- Low input bias currents: 5nA (maximum)
- Low disable current: 50nA (maximum)
- Configurable averaging options
- Alert limits for over and under current events
- 1.2V compliant I²C, SMBus interface
- 16-pin selectable addresses
- DSBGA-16 Package (1.5mm × 1.5mm)

2 Applications

- Notebook computers
- Security cameras
- Retail automation
- Power management
- Battery cell monitors and balancers
- Rack servers
- eFuse current and power monitoring

Typical Application



3 Description

The INA2227 device is a dual channel 16-bit digital current monitor with an I²C/SMBus-compatible interface that is compliant with digital bus voltages from 1.2V to 5V. The device monitors the voltage across an external sense resistor and reports values for shunt voltage, bus voltage, current, power, and energy for each channel.

The INA2227 features programmable ADC conversion times and averaging that is common for all channels. Each channel has a programmable calibration value with an internal multiplier that enables direct readouts of current in amperes, power in watts, and energy in joules. Each channel has a dedicated VBUS pin to monitor the bus voltage and can alert on overcurrent and undercurrent conditions, as well as on overvoltage and undervoltage conditions. High input impedance while in current measurement mode allows use of larger current sense resistors needed to measure small value system currents.

The INA2227 senses current on common-mode bus voltages that can vary from –0.3V to 48V, independent of the supply voltage. The device operates from a single 1.7V to 5.5V supply, drawing a typical supply current of 400μA in normal operation. The device can be placed in a low-power standby mode where the typical operating current is 2.5μA and can be fully disabled using the enable pin to achieve an supply current less than 50nA. The device is specified over the operating temperature range between –40°C and 125°C and features up to 16 programmable addresses.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
INA2227	YBJ (DSBGA, 16)	1.5mm × 1.5mm

(1) For all available packages, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

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4 Pin Configuration and Functions

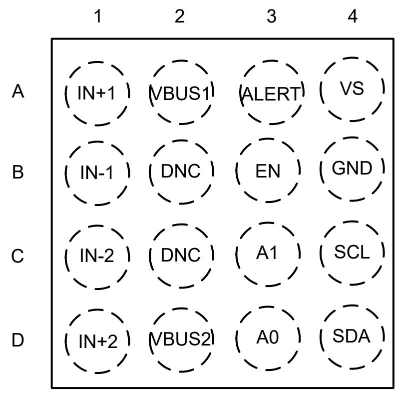


Figure 4-1. YBJ Package 16-Bump DSBGA (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	YBJ (DSBGA)		
A0	D3	Digital input	Address pin. Connect to GND, SCL, SDA, or VS. Table 6-1 lists the pin settings and corresponding addresses.
A1	C3	Digital input	Address pin. Connect to GND, SCL, SDA, or VS. Table 6-1 lists the pin settings and corresponding addresses.
ALERT	A3	Digital output	Multifunctional alert, open-drain output. This pin alerts to report fault conditions or can be configured to notify host when a conversion is complete.
DNC	B2, C2	-	Do not connect, leave floating.
EN	B3	Digital input	Enable pin. A logic high level enables the device; a logic low level disables the device.
GND	B4	Ground	Ground for both analog and digital.
IN–1	B1	Analog input	Channel 1 current sensing negative input. For high-side applications, connect to load side of sense resistor. For low-side applications, connect to ground side of sense resistor.
IN+1	A1	Analog input	Channel 1 current sensing positive input. For high-side applications, connect to bus voltage side of sense resistor. For low-side applications, connect to load side of sense resistor.
IN–2	C1	Analog input	Channel 2 current sensing negative input. For high-side applications, connect to load side of sense resistor. For low-side applications, connect to ground side of sense resistor.
IN+2	D1	Analog input	Channel 2 current sensing positive input. For high-side applications, connect to bus voltage side of sense resistor. For low-side applications, connect to load side of sense resistor.
SCL	C4	Digital input	Serial bus clock line, open-drain input.
SDA	D4	Digital input/output	Serial bus data line, open-drain input/output.
VBUS1	A2	Analog input	Bus voltage input for channel 1.
VBUS2	D2	Analog input	Bus voltage input for channel 2.
VS	A4	Power Supply	Power supply, 1.7V to 5.5V.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_s	Supply Voltage		6	V
V_{IN+}, V_{IN-}	Differential (V_{IN+}) - (V_{IN-})	–26	26	V
	Common - mode	GND – 0.3	50	V
V_{BUS}	Bus Voltage, VBUS1, VBUS2	GND – 0.3	50	V
V_{IO}	SDA, SCL, ALERT, A0, A1, EN	GND – 0.3	6	V
	Input current into any pin		5	mA
	Open-drain digital output current (SDA, ALERT)		10	mA
T_A	Operating Temperature	–55	150	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±3000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins[2]	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input range	GND – 0.3		48	V
V_{BUS}	VBUS input range	GND – 0.3		48	V
V_S	Operating supply range	1.7		5.5	V
T_A	Ambient temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC[1]		INA2227 DSBGA 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	82.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Y_{JB}	Junction-to-board characterization parameter	21.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

at T_A = 25°C, V_S = 3.3V, V_{SENSE} = V_{IN+} - V_{IN-} = 0mV, V_{IN-} = V_{BUS} = 12V, for all channels (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
CMRR	Common-mode rejection	V_{CM} = –0.3V to 48V, T_A = –40°C to 125°C	110	120		dB
	Shunt voltage input range	ADCRANGE = 0	–81.9175		81.92	mV
		ADCRANGE = 1	–20.4794		20.48	mV
V_{os}	Shunt offset voltage	V_{CM} = 12 V		±10	±75	µV
dV_{os}/dT	Shunt offset voltage drift	T_A = –40°C to 125°C		±0.1	±0.5	µV/°C
V_{os_b}	IN- bus offset Voltage			±5	±30	mV
dV_{os_b}/dT	IN- bus offset voltage drift	T_A = –40°C to 125°C		±10	±30	µV/°C
$PSRR_{SH}$	Power supply rejection ratio (Current measurements)	V_S = 1.7V to 5.5V, T_A = –40°C to 125°C		±0.2	±2.5	µV/V
$PSRR_{BUS}$	Power supply rejection ratio (Voltage measurements)	V_S = 1.7V to 5.5V, T_A = –40°C to 125°C		±0.5	±2.5	mV/V
Z_{IN-}	IN- input impedance	Bus Voltage Measurement Mode		1.14		MΩ
I_B	Input bias current	IN+, IN-, Current Measurement Mode		0.1	5	nA
DC ACCURACY						
R_{DIFF}	Differential Input Impedance (IN+ to IN-)	V_{IN+} - V_{IN-} < 82mV		140		kΩ
	ADC Resolution	T_A = –40°C to 125°C		16		Bits
	1 LSB step size	Shunt Voltage, ADCRANGE = 0		2.5		µV
		Shunt Voltage, ADCRANGE = 1		625		nV
		Bus Voltage		1.6		mV
	ADC Conversion-time (T_A = –40°C to 125°C)	CT bit = 000		140		µs
		CT bit = 001		204		µs
		CT bit = 010		332		µs
		CT bit = 011		588		µs
		CT bit = 100		1.100		ms
		CT bit = 101		2.116		ms
		CT bit = 110		4.156		ms
		CT bit = 111		8.244		ms
	Internal Oscillator Frequency	T_A = +25°C		500		kHz
	Internal Oscillator Tolerance	T_A = +25°C			0.5	%
		T_A = –40°C to +125°C			1	%
G_{SERR}	Shunt voltage gain error			±0.04	±0.5	%
G_{S_DRFT}	Shunt voltage gain error drift	T_A = –40°C to +125°C			50	ppm/°C
G_{BERR}	V_{IN-} voltage gain error			±0.05	±0.5	%
G_{B_DRFT}	V_{IN-} voltage gain error drift	T_A = –40°C to +125°C			50	ppm/°C
P_{TME}	Power total measurement error	At full scale voltage and current		±0.04	±1	%
E_{TME}	Energy total measurement error	At full scale voltage and current		±0.3	±1.5	%
INL	Integral Non-Linearity	ADCRANGE = 0, Linear best fit, T_A = –40°C to +125°C		±2	±6	m%
DNL	Differential Non-Linearity			±0.1		LSB

at T_A = 25°C, V_S = 3.3V, V_{SENSE} = V_{IN+} - V_{IN-} = 0mV, V_{IN-} = V_{BUS} = 12V, for all channels (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE						
I_{EN}	Input leakage current	0 V ≤ V_{EN} ≤ V_S		1	50	nA
V_{IH}	Logic input level, high	V_S = 1.7V to 3.6V, T_A = –40°C to +125°C	1.1		5.5	V
V_{IH}	Logic input level, high	V_S = 3.6V to 5.5V, T_A = –40°C to +125°C	1.3		5.5	V
V_{IL}	Logic input level, low	V_S = 1.7V to 5.5V, T_A = –40°C to +125°C	0		0.4	V
V_{HYS}	Hysteresis			125		mV
POWER SUPPLY						
I_Q	Quiescent current			400	500	µA
		I_Q vs temperature, T_A = –40°C to +125°C			600	µA
		Shutdown		2.5	4	µA
I_Q	Quiescent current disabled	V_{EN} = 0V		5	50	nA
V_{POR}	Power-on reset threshold	V_S falling		0.95		V
SMBUS						
	SMBUS timeout			28	35	ms
	Input capacitance			3		pF
DIGITAL INTERFACE						
V_{IH}	Logic input level, high	V_S = 1.7V to 5.5V, T_A = –40°C to +125°C	0.9		5.5	V
V_{IL}	Logic input level, low	V_S = 1.7V to 5.5V, T_A = –40°C to +125°C	0		0.4	V
V_{HYS}	Hysteresis			130		mV
V_{OL}	Logic output level, low	I_{OL} = 3mA, V_S = 1.7V to 5.5V, T_A = –40°C to +125°C	0		0.3	V
	Digital leakage input current	0 ≤ V_{INPUT} ≤ V_S			±50	nA

5.6 Timing Requirements (I²C)

		MIN	NOM	MAX	UNIT
I^2C BUS (FAST MODE)					
$F_{(SCL)}$	I^2C clock frequency	1		400	kHz
$t_{(BUF)}$	Bus free time between STOP and START conditions	600			ns
$t_{(HDSTA)}$	Hold time after a repeated START condition. After this period, the first clock is generated.	100			ns
$t_{(SUSTA)}$	Repeated START condition setup time	100			ns
$t_{(SUSTO)}$	STOP condition setup time	100			ns
$t_{(HDDAT)}$	Data hold time	10		900	ns
$t_{(SUDAT)}$	Data setup time	100			ns
$t_{(LOW)}$	SCL clock low period	1300			ns
$t_{(HIGH)}$	SCL clock high period	600			ns
t_F	Data fall time			300	ns
t_F	Clock fall time			300	ns
t_R	Clock rise time			300	ns
t_R	Clock rise time (SCLK ≤ 100 kHz)			1000	ns
I^2C BUS (HIGH-SPEED MODE)					
$F_{(SCL)}$	I^2C clock frequency	10		2940	kHz
$t_{(BUF)}$	Bus free time between STOP and START conditions	160			ns
$t_{(HDSTA)}$	Hold time after a repeated START condition. After this period, the first clock is generated.	100			ns
$t_{(SUSTA)}$	Repeated START condition setup time	100			ns
$t_{(SUSTO)}$	STOP condition setup time	100			ns
$t_{(HDDAT)}$	Data hold time	10		125	ns
$t_{(SUDAT)}$	Data setup time	20			ns
$t_{(LOW)}$	SCL clock low period	200			ns
$t_{(HIGH)}$	SCL clock high period	60			ns
t_F	Data fall time			80	ns
t_F	Clock fall time			40	ns
t_R	Clock rise time			40	ns

5.7 Timing Diagram

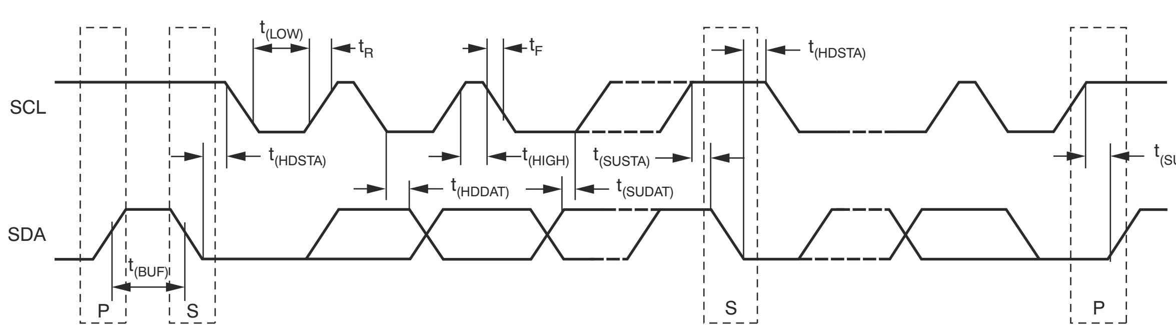


Figure 5-1. I²C Timing Diagram

5.8 Typical Characteristics

at T_A = 25°C, V_{VS} = 3.3V, V_{CM} = 12V, and V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0mV (unless otherwise noted)

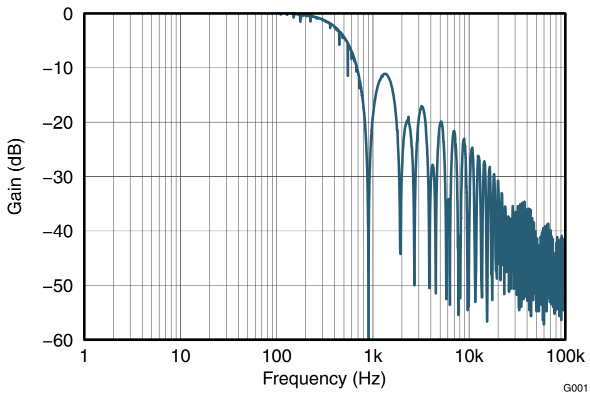


Figure 5-2. Frequency Response

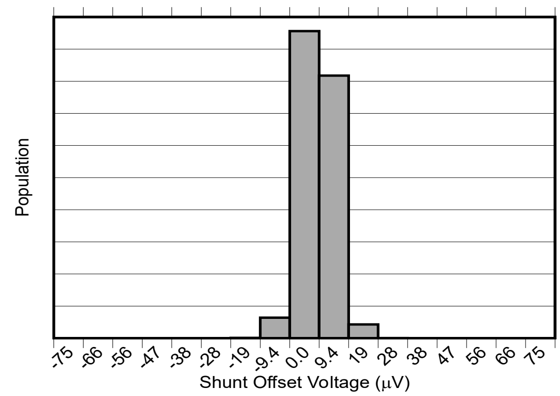


Figure 5-3. Shunt Input Offset Voltage Production Distribution

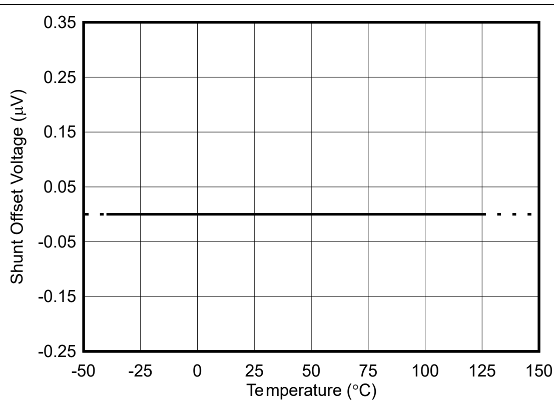


Figure 5-4. Shunt Input Offset Voltage vs. Temperature

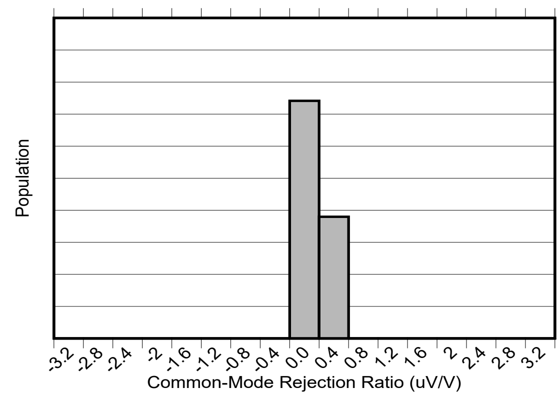


Figure 5-5. CMRR Production Distribution

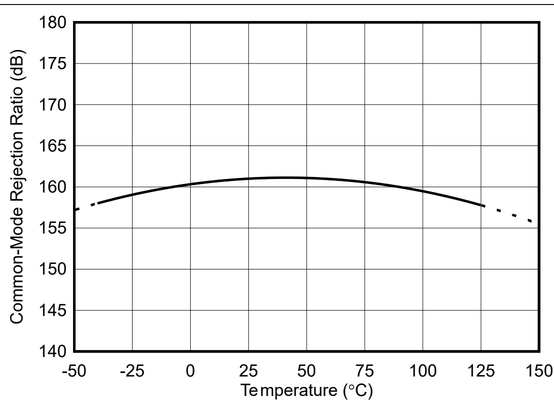


Figure 5-6. Shunt Input CMRR vs. Temperature

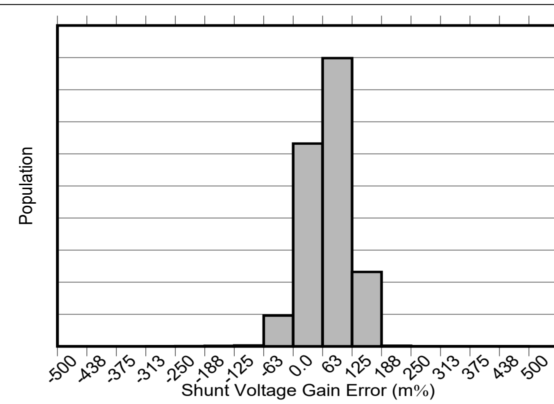


Figure 5-7. Shunt Voltage Gain Error Production Distribution

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_{VS} = 3.3V, V_{CM} = 12V, and V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0mV (unless otherwise noted)

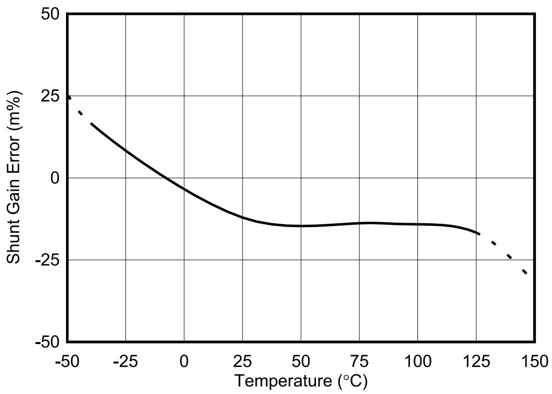


Figure 5-8. Shunt Gain Error vs. Temperature

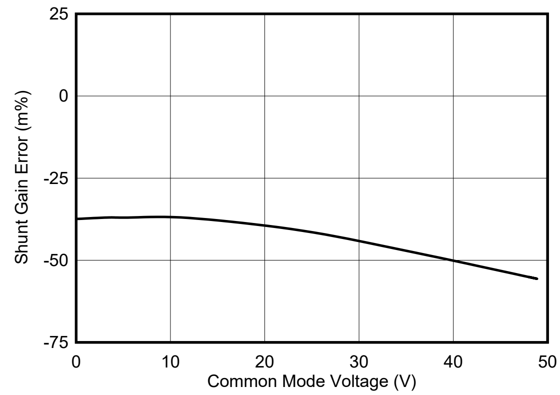


Figure 5-9. Shunt Gain Error vs. Common-Mode Voltage

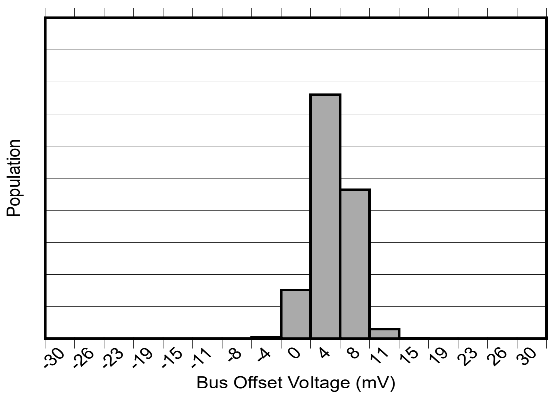


Figure 5-10. Bus Offset Voltage (V_{IN-}) Production Distribution

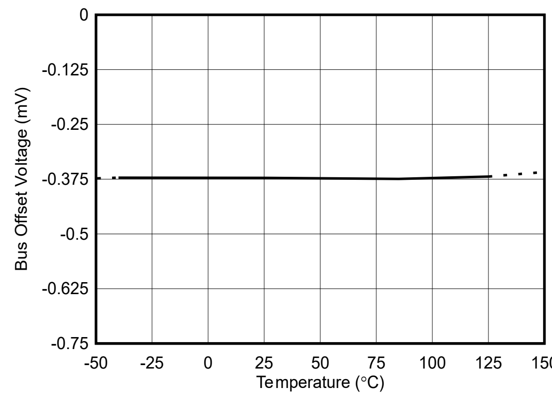


Figure 5-11. Bus Offset Voltage (V_{IN-}) vs. Temperature

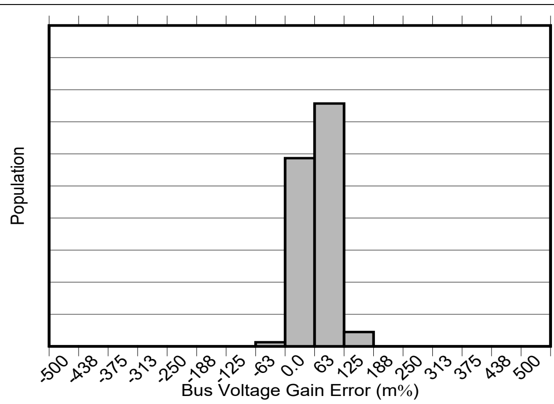


Figure 5-12. Bus Voltage (V_{IN-}) Gain Error Production Distribution

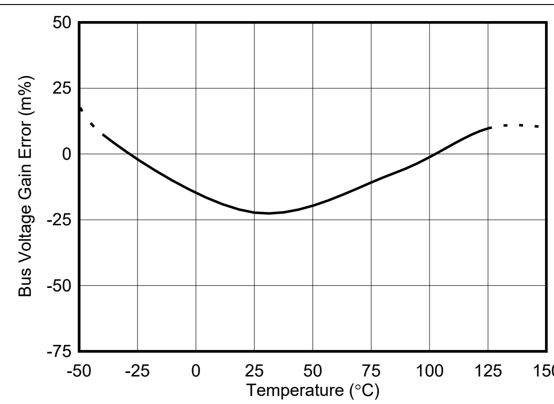


Figure 5-13. Bus Voltage (V_{IN-}) Gain Error vs. Temperature

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_{VS} = 3.3V, V_{CM} = 12V, and V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0mV (unless otherwise noted)

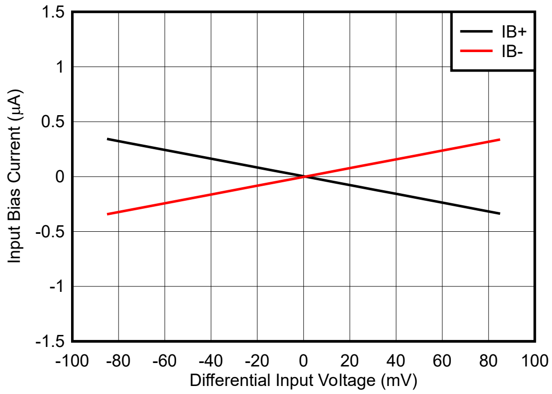


Figure 5-14. Input Bias Current vs. Differential Voltage

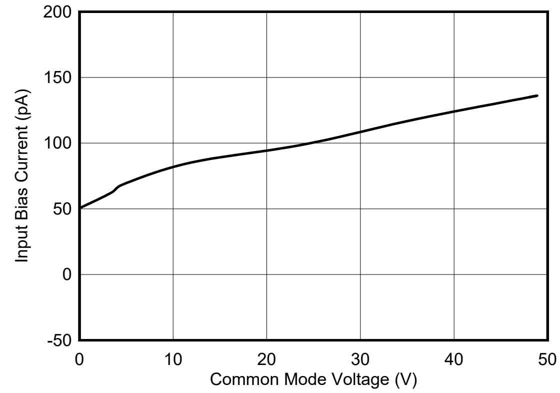


Figure 5-15. Input Bias Current vs. Common-Mode Voltage (IB+, IB-)

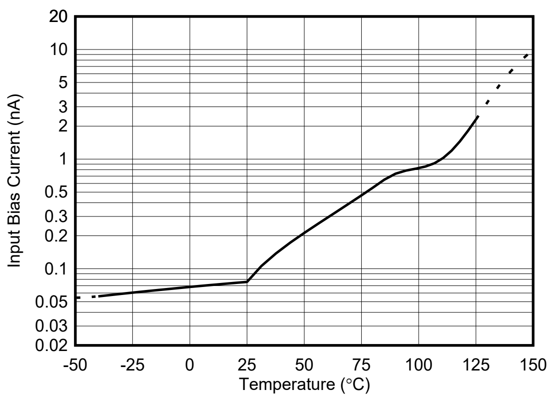


Figure 5-16. Input Bias Current vs. Temperature

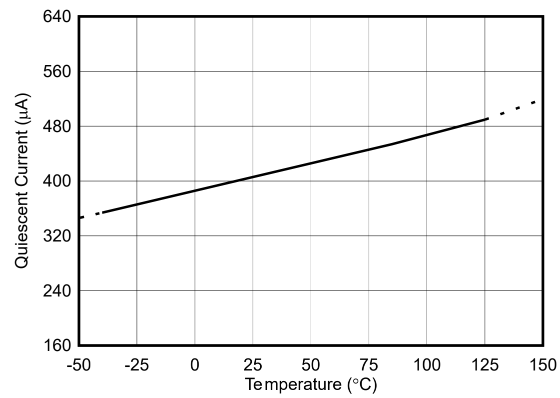


Figure 5-17. Quiescent Current vs. Temperature

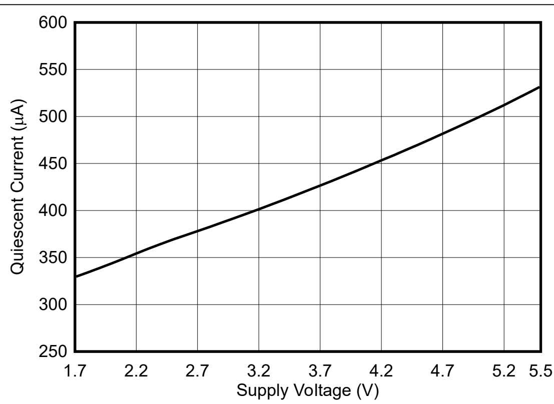


Figure 5-18. Quiescent Current vs. Supply Voltage

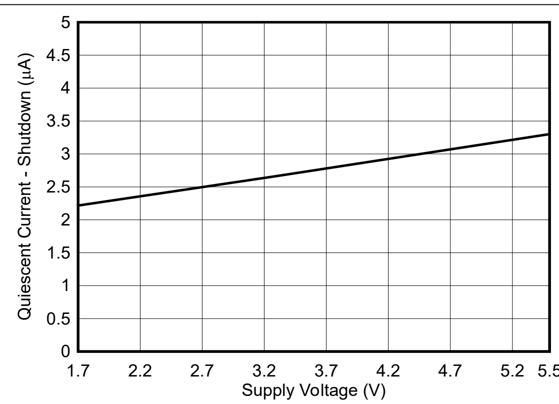


Figure 5-19. Quiescent Current - Shutdown vs. Supply Voltage

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_{VS} = 3.3V, V_{CM} = 12V, and V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0mV (unless otherwise noted)

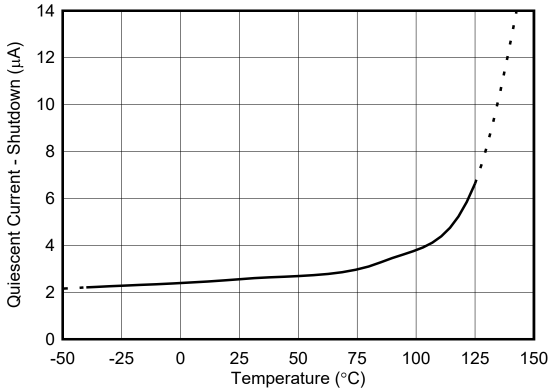


Figure 5-20. Quiescent Current - Shutdown vs. Temperature

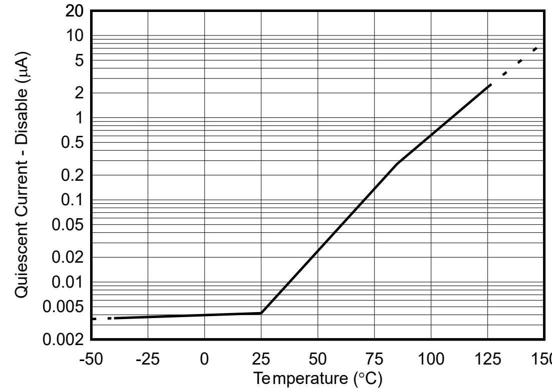


Figure 5-21. Quiescent Current - Disabled vs. Temperature

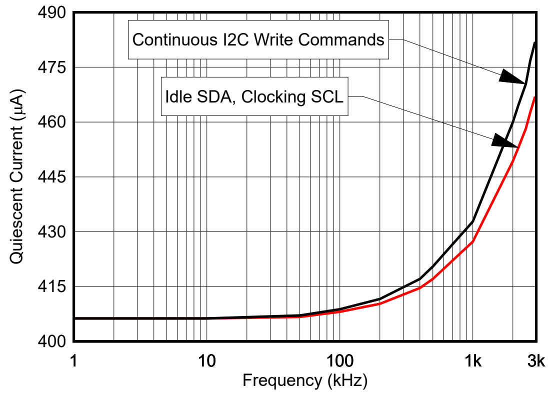


Figure 5-22. Quiescent Current vs. Clock(SCL) Frequency

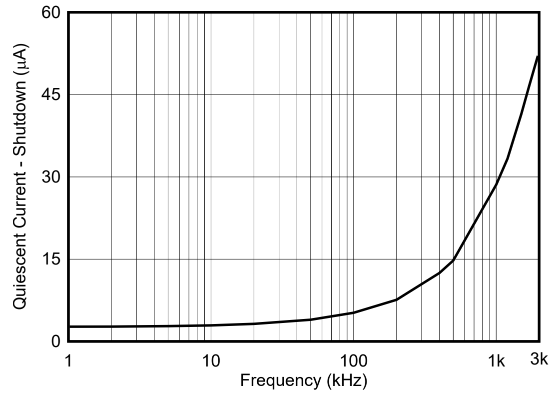


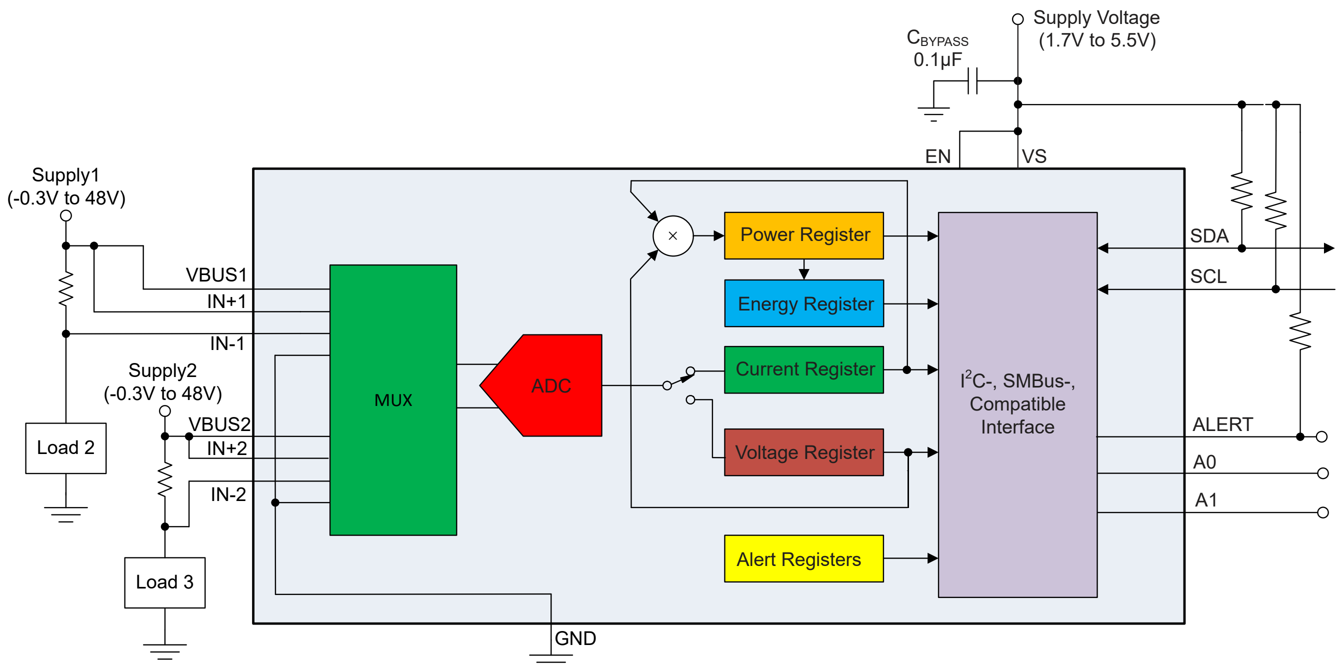
Figure 5-23. Quiescent Current - Shutdown vs. SCL Frequency

6 Detailed Description

6.1 Overview

The INA2227 is a dual channel digital current-sense amplifier with an I²C- and SMBus-compatible interface. The device reports current, voltage, power, and energy for each of the channels and features programmable out-of-range limits to issue alerts when selected parameters are outside the normal range of operation. The integrated analog-to-digital converter (ADC) can be set to different averaging modes and configured for continuous-versus-triggered operation. *Device Registers* provides detailed register information for the INA2227.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Integrated Analog-to-Digital Converter (ADC)

The INA2227 integrates a low offset 16-bit delta-sigma (ΔΣ) ADC. This ADC is multiplexed for each channel to process both the shunt voltage and bus voltage measurements. The shunt voltage measurement is a differential measurement of the voltage developed when the load current flows through a shunt resistor between the IN+ and IN– pins for each channel. The shunt voltage measurement has a maximum offset voltage of only 75µV and a maximum gain error of 0.5%. The low offset voltage of the shunt voltage measurement allows for increased accuracy at light load conditions for a given shunt resistor value. Another advantage of low offset is the ability to sense a lower voltage drop across the sense resistor accurately, thus allowing for a lower-value shunt resistor. Lower-value shunt resistors reduce power loss in the current-sense circuit and help improve the power efficiency of the end application. This device also features independent bus voltage pins that allow power and energy measurements for both high-side and low-side sensing applications.

There are no special considerations for power-supply sequencing because the bus common-mode at the IN+ and IN- pins and power-supply voltage at the VS pin are independent of each other; therefore, the bus common-mode voltage can be present with the supply voltage off, and so forth.

6.3.2 Internal Measurement and Calculation Engine

The internal round robin measurement scheme for the INA2227 is shown in Figure 6-1. For each channel the current, power, and energy registers are calculated from the shunt and bus voltage measurements and are not directly affected by ADC conversion times. Register values are updated for each channel before preceding to the next channel. When averaging is enabled, the registers for each channel updates once the number of averages is complete. Fault conditions are compared immediately after conversions or calculations based on the ADC conversion time and are independent of the number of averages set. Reducing the conversion times result in faster alert responses but at lower effective resolutions due to noise. Longer conversion times slow the alert response but are less sensitive to noise. Channels or measurements that are disabled are skipped in the round robin cycle. The conversion ready flag is set at the end of conversions after the selected number of averages are met.

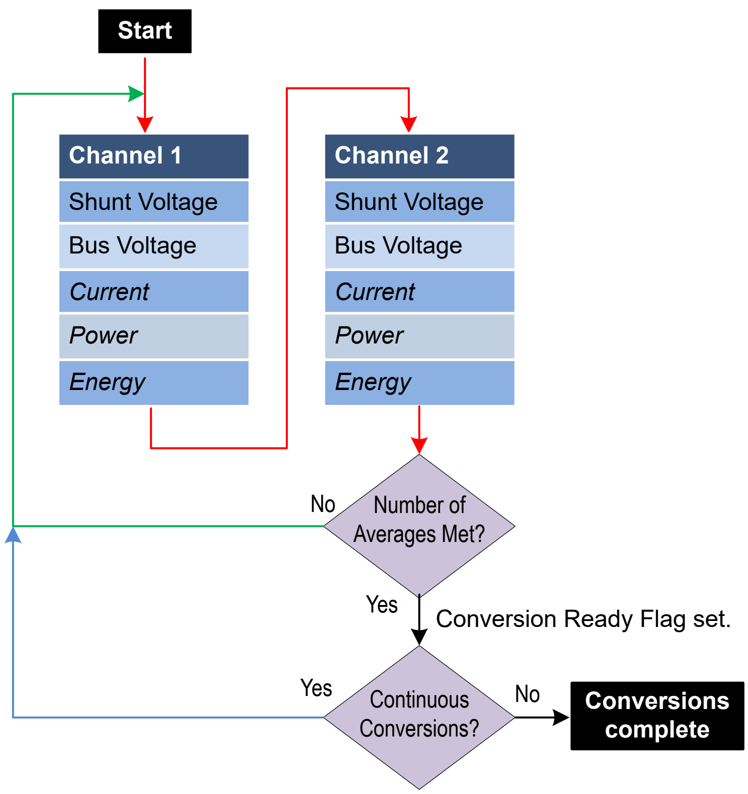


Figure 6-1. Internal Measurement and Calculation Scheme

In Figure 6-1, the *Italicized* registers are calculated values that do not depend on conversion times and occur in the background. Registers are updated independently for each channel once number of averages is met. Fault threshold comparisons are done immediately on a per result basis. Average values do not trigger alerts.

Current is calculated from the shunt voltage measurements and the value entered in the corresponding calibration register. Power is calculated based on the previous current calculation and the latest bus voltage measurement. Energy is accumulated by adding the previous power calculation multiplied by the current timebase interval. If the value loaded into the corresponding calibration register is zero, current, power, and energy values are reported as zero also. When the averaging is enabled, register values are updated once the number of averages are met. These calculations are performed in the background and do not add to the overall conversion time.

6.3.3 Low Bias Current

The INA2227 features very low input bias current which provides several benefits. The low input bias current of the INA2227 reduces the current consumed by the device in both active and shutdown state. Another benefit of low bias current is that low bias current allows the use of input filters to reject high-frequency noise before the signal is converted to digital data. In traditional digital current-sense monitors, the addition of input filters comes at the cost of reduced accuracy. However, as a result of the low bias current, the reduction in accuracy due to input filters is minimized. An additional benefit of low bias current is the ability to use a larger shunt resistor to accurately sense smaller currents. Use of a larger value for the shunt resistor allows the device to accurately monitor currents in the sub-mA range.

The bias current in the INA2227 is the smallest when the sensed current is zero. As the current starts to increase, the differential voltage drop across the shunt resistor increases which results in an increase in the bias current (see Figure 5-14).

6.3.4 Low Voltage Supply and Wide Common-Mode Voltage Range

The supply voltage range of the INA2227 is 1.7V to 5.5V. The ability to operate at 1.7V enables the device to be used in 1.8V supply rails. Even with a supply voltage of 1.7V, the device can monitor currents on voltage rails as high as 48V. This wide common-mode range of operation allows the device to be used in many applications where the common-mode voltage exceeds the supply voltage rail.

6.3.5 ALERT Pin

The INA2227 has two Alert Configuration Registers that can be assigned to the two channels as needed. Each alert register has a channel assignment field as well as an alert mask field. The alert mask field allows the selection from one of the five available functions for the alert response. Based on the function being monitored, a value can then be entered into the Alert Limit Registers to set the corresponding threshold value that asserts the ALERT pin.

The ALERT pin allows for one of several available alert functions to be monitored to determine if a user-defined threshold has been exceeded. The five alert functions that can be monitored are:

- Shunt voltage overlimit (SOL)
- Shunt voltage underlimit (SUL)
- Bus voltage overlimit (BOL)
- Bus voltage underlimit (BUL)
- Power overlimit (POL)

The ALERT pin is an open-drain output. This pin is asserted when the alert function selected in the Alert Configuration registers exceeds the value programmed into the Alert Limit register. Up to four alert functions can be enabled and monitored at a time.

The conversion-ready state of the device can also be monitored at the ALERT pin to inform the user when the device has completed the previous conversion and is ready to begin a new conversion. The conversion ready flag (CVRF) bit can be monitored at the ALERT pin along with one of the alert functions.

If the alert function is not used, the ALERT pin can be left floating without impacting the operation of the device.

The alert function compares the programmed alert limit value to the result of each corresponding conversion. Therefore, an alert can be issued during a conversion cycle where the averaged value of the signal does not exceed the alert limit. Triggering an alert based on this intermediate conversion allows for out-of-range events to be detected faster than the averaged output data registers are updated. This fast detection can be used to create alert limits for quickly changing conditions through the use of the alert function, as well as to create limits to longer-duration conditions through software monitoring of the averaged output values.

6.4 Device Functional Modes

6.4.1 Continuous Versus Triggered Operation

The INA2227 has two operating modes, continuous and triggered, that determine how the ADC operates after these conversions. When the INA2227 is in the normal operating mode (that is, the MODE bits of the CONFIG1 register are set to '111'), the device continuously converts a shunt voltage reading followed by a bus voltage reading for each channel.

In triggered mode, writing any of the triggered convert modes into the Section 7.1.1 (that is, the MODE bits of the CONFIG1 register are set to 001, 010, or 011) triggers a single-shot conversion of the selected parameters. This action produces a single set of measurements. To trigger another single-shot conversion, the Configuration register must be written to again, even if the mode does not change.

Although the INA2227 can be read at any time, and the data from the last conversion remain available, the conversion ready flag bit (CVRF bit, FLAGS register) is provided to help coordinate single-shot or triggered conversions. The CVRF bit is set after all conversions, averaging, and multiplication operations are complete for a single round robin cycle.

The CVRF bit clears under these conditions:

1. Writing to the CONFIG1 register, except when configuring the MODE bits for power-down mode; or
2. Reading the FLAGS register.

6.4.2 Device Low Power Modes

In addition to the two operating modes (continuous and triggered), the INA2227 also has two low power modes. In shutdown the device reduces the quiescent current and input bias current but is able to process I^2C bus communications. In this state the quiescent current is reduced to less than 4µA. Full recovery from shut-down mode requires 40µs. The device remains in shut-down mode until one of the active modes settings are written into the Configuration register. An even lower power mode is the disabled mode, which is initiated by forcing a logic low on the enable pin. In this mode the quiescent current is the lowest, with the device only drawing 1µA (max) of supply current, but the device does not recognize any I2C bus communications in this state. Also the device configuration gets reset when in the disabled state and needs to be reprogrammed when enabled. Recovery from the disabled state requires 100µs.

6.4.3 Power-On Reset

Power-on reset (POR) is asserted when V_S drops below 0.95V (typical) at which point all of the registers are reset to the default values. The default power-up register values are shown in the reset column for each register description.

6.4.4 Averaging and Conversion Time Considerations

The INA2227 has programmable conversion times for both the shunt voltage and bus voltage measurements that are applied across all channels. The conversion times for these measurements can be selected from as fast as 140µs to as long as 8.244ms. The conversion time settings, along with the programmable averaging mode, allow the INA2227 to be configured to optimize the available timing requirements in a given application. The INA2227 can also be configured with a different conversion time setting for the shunt and bus voltage measurements. This type of approach is common in applications where the bus voltage tends to be relatively stable. This situation allows for the time spent measuring the bus voltage to be reduced relative to the shunt voltage measurement.

There are trade-offs associated with the conversion time settings and the averaging mode used. The averaging feature can significantly improve the measurement accuracy by effectively filtering the signal. This approach allows the INA2227 to reduce noise in the measurement that can be caused by noise coupling into the signal. A greater number of averages enables the INA2227 to be more effective in reducing the noise component of the measurement.

The conversion times selected can also have an effect on the measurement accuracy. Figure 6-2 shows multiple conversion times to illustrate the effect of noise on the measurement. To achieve the highest accuracy measurement possible, use a combination of the longest allowable conversion times and highest number of averages, based on the timing requirements of the system.

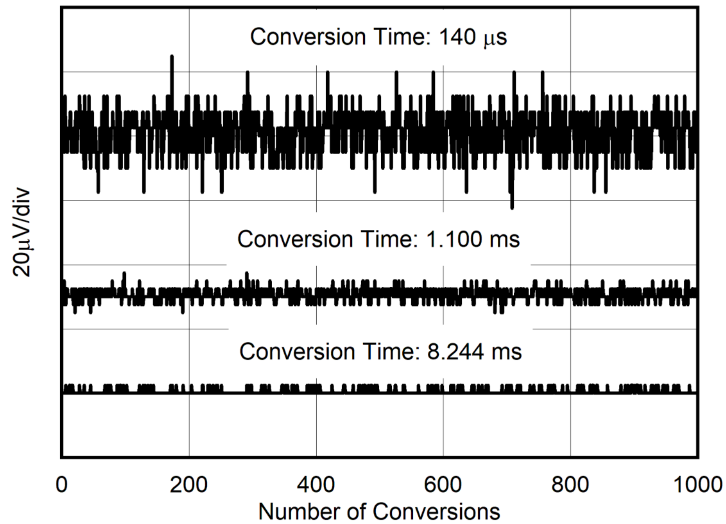


Figure 6-2. Noise vs. Conversion Time

6.5 Programming

6.5.1 I²C Serial Interface

The INA2227 operates only as a target on both the SMBus and I²C interfaces. Connections to the bus are made through the open-drain SDA and SCL lines. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. Although the device integrates spike suppression into the digital I/O lines, proper layout techniques help minimize the amount of coupling into the communication lines. This noise introduction can occur from capacitive coupling signal edges between the two communication lines themselves or from other switching noise sources present in the system. Routing traces in parallel with ground in between layers on a printed circuit board (PCB) typically reduces the effects of coupling between the communication lines. Shielded communication lines reduce the possibility of unintended noise coupling into the digital I/O lines that can be incorrectly interpreted as start or stop commands.

The INA2227 supports the transmission protocol for fast mode (1kHz to 400kHz) and high-speed mode (1kHz to 2.94MHz). All data bytes are transmitted most significant byte first and follow the SMBus 3.0 transfer protocol.

To communicate with the INA2227, the controller must first address targets through a target address byte. The target address byte consists of seven address bits and a direction bit that indicates whether the action is to be a read or write operation.

The device has two address pins, A0 and A1. Table 6-1 lists the pin connections required for each of the 16 possible addresses. The device samples the state of pins A0 and A1 on every bus communication. Establish the pin state before any activity on the interface occurs.

Table 6-1. Address Pins and Target Addresses

A1	A0	TARGET DEVICE ADDRESS
GND	GND	1000000
GND	VS	1000001
GND	SDA	1000010
GND	SCL	1000011
VS	GND	1000100
VS	VS	1000101
VS	SDA	1000110
VS	SCL	1000111
SDA	GND	1001000

Table 6-1. Address Pins and Target Addresses (continued)

A1	A0	TARGET DEVICE ADDRESS
SDA	VS	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	VS	1001101
SCL	SDA	1001110
SCL	SCL	1001111

6.5.2 Writing to and Reading Through the I²C Serial Interface

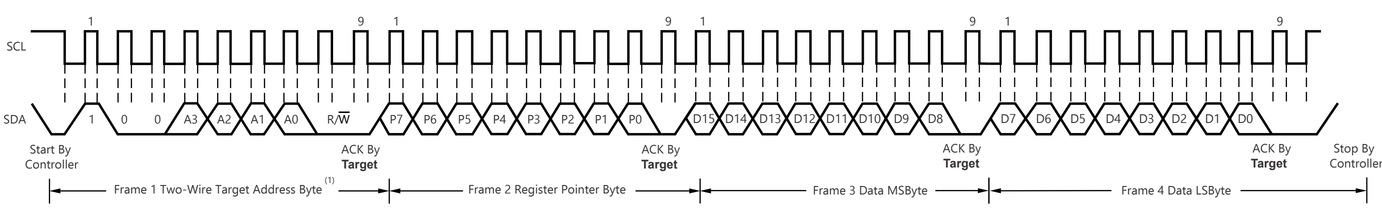
Accessing a specific register on the INA2227 is accomplished by writing the appropriate value to the register pointer. Refer to *Register Maps* for a complete list of registers and corresponding addresses. The value for the register pointer (see Figure 6-5) is the first byte transferred after the target address byte with the R/$\overline{W}$ bit low. Every write operation to the device requires a value for the register pointer.

Writing to a register begins with the first byte transmitted by the controller. This byte is the target address, with the R/$\overline{W}$ bit low. The device then acknowledges receipt of a valid address. The next byte transmitted by the controller is the address of the register to be accessed. This register address value updates the register pointer to the desired internal device register. The next two bytes are written to the register addressed by the register pointer. The device acknowledges receipt of each data byte. The controller can terminate data transfer by generating a start or stop condition.

When reading from the device, the last value stored in the register pointer by a write operation determines which register is read during a read operation. To change the register pointer for a read operation, a new value must be written to the register pointer. This write is accomplished by issuing a target address byte with the R/$\overline{W}$ bit low, followed by the register pointer byte. No additional data are required. The controller then generates a start condition and sends the address byte for the target with the R/$\overline{W}$ bit high to initiate the read command. The next byte is transmitted by the target and is the most significant byte of the register indicated by the register pointer. This byte is followed by an *Acknowledge* from the controller; then the target transmits the least significant byte. The controller can or can not acknowledge receipt of the second data byte. The controller can terminate data transfer by generating a *Not-Acknowledge* after receiving any data byte, or generating a start or stop condition. If repeated reads from the same register are desired, continually sending the register pointer bytes is not necessary. The device retains the register pointer value until the value is changed by the next write operation.

Figure 6-3 shows the write operation timing diagram. Figure 6-4 shows the read operation timing diagram. These diagrams are shown for reading/writing to 16 bit registers.

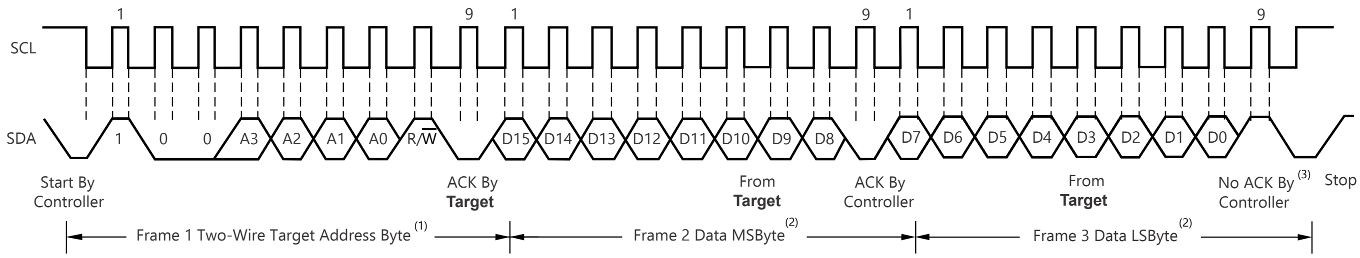
Register bytes are sent most-significant byte first, followed by the least significant byte.



A. The value of the Target Address byte is determined by the setting of the A0 address pin. Refer to Table 6-1.

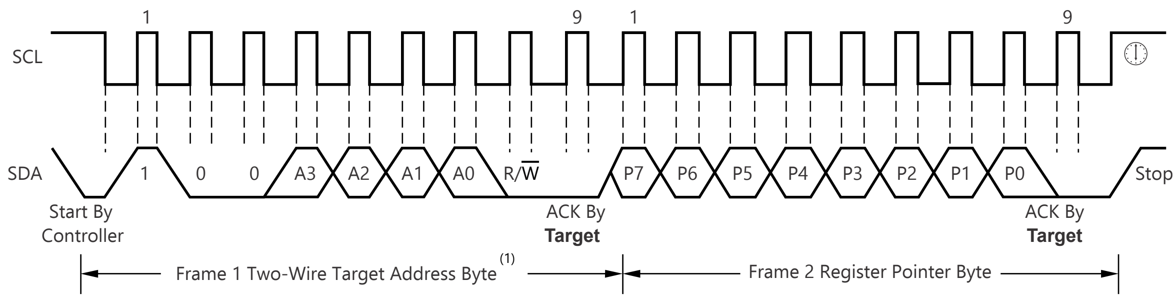
B. The device does not support packet error checking (PEC) or perform clock stretching.

Figure 6-3. Timing Diagram for Write Word Format



A. The value of the Target Address byte is determined by the setting of the A0 address pin. Refer to Table 6-1.
B. Read data is from the last register pointer location. If a new register is desired, the register pointer must be updated. See Figure 6-5.
C. ACK by the controller can also be sent.
D. The device does not support packet error checking (PEC) or perform clock stretching.

Figure 6-4. Timing Diagram for Read Word Format



A. The value of the Target Address byte is determined by the setting of the A0 address pin. Refer to Table 6-1.

Figure 6-5. Typical Register Pointer Set

6.5.3 High-Speed I²C Mode

When the bus is idle, both the SDA and SCL lines are pulled high by the pullup resistors. The controller generates a start condition followed by a valid serial byte containing high-speed (HS) controller code *00001XXX*. This transmission is made in fast (400kHz) or standard (100kHz) (F/S) mode at no more than 400kHz. The device does not acknowledge the HS controller code, but does recognize the code and switches the internal filters to support 2.94MHz operation.

The controller then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 2.94MHz are allowed. Instead of using a stop condition, use repeated start conditions to maintain the bus in HS-mode. A stop condition ends the HS-mode and switches all the internal filters of the device to support the F/S mode.

6.5.4 General Call Reset

A general call reset to multiple devices is implemented by addressing the general call address 0000 000, with the last R/W bit set to 0. This is then followed by the following data byte 0000 0110 (06h).

On receiving this 2-byte sequence, all devices designed to respond to the general call address are reset. All INA2227 devices on the bus perform a soft reset operation and return to the default power-up conditions

6.5.5 SMBus Alert Response

The INA2227 is designed to respond to the SMBus Alert Response address. The SMBus Alert Response provides a quick fault identification for simple targets. When an Alert occurs, the controller can broadcast the Alert Response target address (0001 100) with the Read/Write bit set high. Following this Alert Response, any target that generates an alert is identified by acknowledging the Alert Response and sending the address on the bus.

The Alert Response can activate several different target devices simultaneously, similar to the I2C General Call. If more than one target attempts to respond, bus arbitration rules apply. The device that is not prioritized during arbitration does not generate an acknowledge. The device continues to hold the Alert line lows until the device is prioritized as a result of the arbitration.

7 Register Maps

7.1 Device Registers

Table 7-1 lists the INA2227 registers. All register locations not listed in the table are considered as reserved locations and the register contents must not be modified.

Table 7-1. INA2227 Register Overview

Register Name	Address	Register Type	Register Size (bits)	Default Value
CONFIG1	0x10	R/W	16	0xF127
CONFIG2	0x11	R/W	16	0x0000
CALIBRATION_(CH1 - CH2)	0x05,0x0D	R/W	16	0x0000
ALERT_CONFIG(1 - 2)	0x07, 0x0F	R/W	16	0x0000
ALERT_LIMIT(1 - 2)	0x06, 0x0E	R/W	16	0x0000
SHUNT_VOLTAGE_(CH1 - CH2)	0x00, 0x08	R	16	0x0000
BUS_VOLTAGE_(CH1 - CH2)	0x01, 0x09	R	16	0x0000
CURRENT_(CH1 - CH2)	0x02, 0x0A	R	16	0x0000
POWER_(CH1 - Ch2)	0x03, 0x0B	R	16	0x0000
ENERGY_(CH1 - CH2)	0x04, 0x0C	R	32	0x0000
FLAGS	0x12	R	16	0x0000
MANUFACTURER_ID	0x7E	R	16	0x5449 ("TI" in ASCII)
DEVICE_ID	0x7F	R	16	0x2350

Complex bit access types are encoded to fit into small table cells. Table 7-2 shows the codes that are used for access types in this section.

Table 7-2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write

7.1.1 CONFIG1 Register (Address = 0x10h)

The configuration register is shown in Table 7-3.

Table 7-3. CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	ACTIVE_CHANNEL	R/W	0011b	These 4 bits determine which channels are active. Set this bit to '1' to enable each channel. Disabled channels are skipped in the round robin cycle. Bit15 = reserved. Bit14 = reserved. Bit13 = Channel 2 measurement enable/disable. Bit12 = Channel 1 measurement enable/disable. Power up default: **0011b = All channels active**

Table 7-3. CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-9	AVG	R/W	000b	Sets the number of ADC conversion results to be averaged. The read-back registers are updated after averaging is completed. **000b = 1** 001b = 4 010b = 16 011b = 64 100b = 128 101b = 256 110b = 512 111b = 1024
8-6	VBUSCT	R/W	100b	Sets the conversion time of the VBUS measurement 000b = 140µs 001b = 204µs 010b = 332µs 011b = 588µs **100b = 1100µs** 101b = 2116µs 110b = 4156µs 111b = 8244µs
5-3	VSHCT	R/W	100b	Sets the conversion time of the SHUNT measurement 000b = 140µs 001b = 204µs 010b = 332µs 011b = 588µs **100b = 1100µs** 101b = 2116µs 110b = 4156µs 111b = 8244µs
2-0	MODE	R/W	111b	Operating mode: Modes can be selected to operate the device either in Shutdown mode, continuous mode or triggered mode. The mode also allows user to select mux settings to set continuous or triggered mode on bus voltage and/or shunt voltage measurements. 000b = Shutdown 001b = Shunt voltage triggered, single shot 010b = Bus voltage triggered, single shot 011b = Shunt voltage and Bus voltage triggered, single shot 100b = Shutdown 101b = Continuous shunt voltage 110b = Continuous bus voltage **111b = Continuous shunt and bus voltage**

Return to the Summary Table.

7.1.2 CONFIG2 Register (Address = 0x11h)

The configuration register is shown in Table 7-4.

Table 7-4. CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RST	R/W	0b	Set this bit to '1' to generate a system reset that is the same as power-on reset. Resets all registers to default values and then self-clears.
14-12	Reserved	R	000b	These bits always read 0.

Table 7-4. CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-8	ACC_RST	R/W	0000b	Writing a one to these bits resets the energy registers and clears any overflow flags. Bit11 = reserved. Bit10 = reserved. Bit9 = Channel 2 energy reset, overflow clear. Bit8 = Channel 1 energy reset, overflow clear. Power up default: **0000b = All channels active** Bits are reset back to 0 after write.
7	CNVR_MASK	R/W	0b	Setting this bit high configures the ALERT pin to be asserted when conversions are complete. 0b = Disable conversion ready flag on ALERT pin 1b = Enables conversion ready flag on ALERT pin ALERT remains asserted until the CVRF field in the flags register is read.
6	ENOF_MASK	R/W	0b	When set to 1, the Alert pin toggles when an energy overflow condition occurs on any of the enabled channels
5	ALERT_LATCH	R/W	0b	When set to 1 the state of the Alert pin latches during fault conditions. To clear the alert the alert flags register must be read and the fault condition removed.
4	ALERT_POL	R/W	0b	When this bit is set to 1, the alert pin toggles from low to high during a fault condition. When set to 0 (default), the alert pin toggles from high to low during faults.
3-0	RANGE	R/W	0000b	Enables the selection of the shunt full scale input range for each channel. Bit3 = reserved. Bit2 = reserved. Bit1 = Channel 2 range selection. Bit0 = Channel 1 range selection. range selection bit = 0 selects ±81.92mV range selection bit = 1 selects ±20.48mV **0000b = all channels set to ±81.92mV range**

Return to the Summary Table.

7.1.3 CALIBRATION Registers

The calibration registers shown in Table 7-5 must be programmed to receive valid current, power, and energy results after initial power up, power cycle events, or on device enable.

Table 7-5. INA2227 Calibration Registers

Address	Register Name	Register Type	Register Size (bits)
0x05	CALIBRATION_CH1	R/W	16
0x0D	CALIBRATION_CH2	R/W	16

This register provides the device with the value of the shunt resistor that are present to create the measured differential voltage. This register also sets the resolution of the Current Register. Programming this register sets the Current_LSB and the Power_LSB.

Table 7-6. Calibration Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	

Table 7-6. Calibration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-0	SHUNT_CAL	R/W	0000h	Programmed value needed for doing the shunt voltage to current conversion.

Return to the Summary Table.

7.1.4 Alert Configuration Registers

The alert configuration registers are shown in Table 7-7.

Table 7-7. INA2227 ALERT_CONFIG Registers

Address	Register Name	Register Type	Register Size (bits)
0x07	ALERT1	R/W	16
0x0F	ALERT2	R/W	16

The format of each alert configuration register is shown in Table 7-8.

These registers configure what triggers an alert for each of the channels. The alert mask field sets the active alert.

Table 7-8. Alert Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	Reserved	R	000000000000b	Reserved
4-3	CHANNEL	R/W	00b	Selects 00b = Channel 1 01b = Channel 2 10b = reserved. 11b = reserved.
2-0	ALERT_MASK	R/W	000b	Sets the active alert for the assigned channel 000b = reserved, no effect 001b = Shunt Voltage over limit (SOL) 010b = Shunt Voltage under limit (SUL) 011b = Bus Voltage over limit (BOL) 100b = Bus Voltage under limit (BUL) 101b = Power over limit (POL) 110b = reserved, no effect 111b = reserved, no effect

The alert configuration registers set what triggers an alert for each of the channels. The alert mask field sets the active alert. Up to 2 alerts can be assigned to a given channel or spread as required across all channels depending on the application.

Return to the Summary Table.

7.1.5 Alert Limit Registers

The alert limit registers shown in Table 7-9 must be programmed to set the desired fault limit threshold.

Table 7-9. INA2227 ALERT_LIMIT Registers

Address	Register Name	Register Type	Reset	Register Size (bits)
0x06	LIMIT1	R/W	0000h	16
0x0E	LIMIT2	R/W	0000h	16

The format of the alert limit register follows the format of the corresponding result register.

Shunt voltage limits are represented as signed 16 bit, bus voltage limits are unsigned 15 bit, and power limits are unsigned 16 bit values.

Return to the Summary Table.

7.1.6 Shunt Voltage Registers

The Shunt Voltage Registers store the current shunt voltage reading, V_{SHUNT}. The shunt voltage measurement for each channel has a unique address as shown in Table 7-10.

Table 7-10. INA2227 SHUNT_VOLTAGE Registers

Address	Register Name	Register Type	Register Size (bits)
0x00	SHUNT_VOLTAGE_CH1	R	16
0x08	SHUNT_VOLTAGE_CH2	R	16

The format of each shunt voltage register is shown in Table 7-11.

If averaging is enabled, these registers contain the averaged shunt voltage value.

Table 7-11. Shunt Voltage Register Field Description

Bit	Field	Type	Reset	Description
15-0	VSHUNT	R	0000h	Differential voltage measured across the shunt output. 2's complement value.

Negative numbers are represented in two's complement format. Generate the two's complement of a negative number by complementing the absolute value binary number and adding 1. An MSB = '1' denotes a negative number.

Example: For a value of V_{SHUNT} = –80mV:

1. Take the absolute value: 80mV
2. Translate this number to a whole decimal number (80mV ÷ 2.5µV) = 32000
3. Convert this number to binary = 0111 1101 0000 0000
4. Complement the binary result = 1000 0010 1111 1111
5. Add '1' to the complement to create the two's complement result = 1000 0011 0000 0000 = 8300h

Return to the Summary Table.

7.1.7 Bus Voltage Registers

The bus voltage registers store the voltage measured at the bus pin for each of the channels. Bus voltage measurements are stored in an unique register addresses as shown in Table 7-12.

Table 7-12. INA2227 BUS_VOLTAGE Registers

Address	Register Name	Register Type	Register Size (bits)
0x01	BUS_VOLTAGE_CH1	R	16
0x09	BUS_VOLTAGE_CH2	R	16

The format of each bus voltage register is shown in Table 7-13.

The bus voltage registers only return positive values. If averaging is enabled, this register displays the averaged value.

Table 7-13. BUS_VOLTAGE Register Field Description

Bit	Field	Type	Reset	Description
15-0	VBUS	R	0000h	Bus voltage output. 2's complement value, however always positive.

Return to the Summary Table.

7.1.8 CURRENT Registers

The current registers store the calculated current value for each of the channels. Current measurements are stored in an unique register addresses as shown in Table 7-14.

Table 7-14. INA2227 CURRENT Registers

Address	Register Name	Register Type	Register Size (bits)
0x02	CURRENT_CH1	R	16
0x0A	CURRENT_CH2	R	16

The format of each current register is shown in Table 7-15.

If averaging is enabled, this register displays the averaged value. The value of the Current Register is calculated by multiplying the decimal value in the Shunt Voltage Register with the decimal value of the Calibration Register.

Table 7-15. CURRENT Register Field Description

Bit	Field	Type	Reset	Description
15-0	CURRENT	R	0000h	Calculated current output in Amperes. 2's complement value.

Return to the Summary Table.

7.1.9 POWER Registers

The power registers store the multiplied value of the bus voltage and current for each of the channels. Power measurements are stored in an unique register addresses as shown in Table 7-16.

Table 7-16. INA2227 POWER Registers

Address	Register Name	Register Type	Register Size (bits)
0x03	POWER_CH1	R	16
0x0B	POWER_CH2	R	16

The format of each power register is shown in Table 7-17.

If averaging is enabled, this register displays the averaged value. The Power Register records power in Watts by multiplying the decimal values of the Current Register with the decimal value of the Bus Voltage Register. This is an unsigned result.

Table 7-17. POWER Register Field Description

Bit	Field	Type	Reset	Description
15-0	POWER	R	0000h	This bit returns a calculated value of power in the system. This is an unsigned result.

Return to the Summary Table.

7.1.10 Energy Registers

The energy registers accumulate data from the power registers and with the internal precision timebase calculate and store the energy for each of the channels. Energy measurements are stored in an unique register addresses as shown in Table 7-18.

Table 7-18. INA2227 ENERGY Registers

Address	Register Name	Register Type	Register Size (bits)
0x04	ENERGY_CH1	R	32
0x0C	ENERGY_CH2	R	32

The format of each energy register is shown in Table 7-19.

The Energy register records energy in Joules and utilizes the precision oscillator as a timebase. This is an unsigned result.

Table 7-19. Energy Register Field Description

Bit	Field	Type	Reset	Description
31-0	ENERGY	R	00000000h	This bit returns a calculated value of energy in the system. This is an unsigned result.

Return to the Summary Table.

7.1.11 Flags Register

The Flags Register is shown in Table 7-20.

Table 7-20. Flags Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0b	Reserved, returns 0.
14	Reserved	R	0b	Reserved, returns 0.
13	LIMIT2_ALERT	R	0b	Indicates the second alert limit has been exceeded. This alert is independent of channel.
12	LIMIT1_ALERT	R	0b	Indicates the first alert limit has been exceeded. This alert is independent of channel.
11	Reserved	R	0b	Reserved, returns 0.
10	Reserved	R	0b	Reserved, returns 0.
9	ENERGYOF_CH2	R	0b	Indicates an the energy register has overflowed for channel 2
8	ENERGYOF_CH1	R	0b	Indicates an the energy register has overflowed for channel 1
7	CVRF (Conversion Ready Flag)	R	0b	Although the device can be read at any time, and the data from the last conversion is available, the Conversion Ready Flag bit is provided to help coordinate one-shot or triggered conversions. The Conversion Ready Flag bit is set after all conversions, averaging, and multiplications are complete. Conversion Ready Flag bit clears under the following conditions: 1.) Writing to the Config1 Register (except for Power-Down selection) 2.) Reading the Flags Register
6	OVF (Math Over-flow)	R	0b	This bit is set to '1' if an arithmetic operation results in an overflow error. This bit indicates that current and power data can be invalid.
5-0	Reserved	R	000000b	Reserved, returns 0.

Return to the Summary Table.

7.1.12 Manufacturer ID Register (Address = 7Eh)

The manufacturer ID register is shown in Table 7-21.

Table 7-21. MANUFACTURE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MANUFACTURE_ID	R	5449h	Reads back TI in ASCII

Return to the Summary Table.

7.1.13 Device Identification Register (Address = 7Fh)

The DEVICE_ID register is shown in Table 7-22.

Table 7-22. DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	DIE_ID	R	0x235	Stores the device identification bits
3-0	REV_ID	R	0h	Device revision identification.

Return to the Summary Table.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The INA2227 is a dual channel current shunt monitor with an I^2C- and SMBus-compatible interface. The device monitors a shunt voltage drop to calculate the current and bus voltage at VBUS pin to determine power and energy for up to two measurement channels. Programmable calibration value, conversion times, and averaging (combined with an internal multiplier) enable direct readouts of current in amperes, power in watts, and energy in joules.

8.1.1 Device Measurement Range and Resolution

The INA2227 device supports two input ranges for the shunt voltage measurements for each channel. The supported full scale differential input across the IN+ and IN– pins can be either ±81.92mV or ±20.48mV depending on the RANGE field in the CONFIG2 Register (Address = 0x11h) register. The range for the bus voltage measurement at the IN- pins is from 0V to 52.42V, but is limited by process ratings to the maximum operating voltage.

Table 8-1 provides a description of full scale voltage on shunt and bus voltage measurements, along with the associated resolution.

Table 8-1. ADC Full Scale Values

PARAMETER	FULL SCALE VALUE	RESOLUTION
Shunt voltage	±81.92mV (ADCRANGE = 0)	2.5µV/LSB
	±20.48mV (ADCRANGE = 1)	625nV/LSB
Bus voltage	0V to 52.4V (Limit usable range to recommended operating voltage)	1.6mV/LSB

The device shunt voltage and bus voltage measurements are read through the Shunt Voltage registers and Bus Voltage registers, respectively. The digital output in shunt voltage and bus voltage registers is 16 bits. The shunt voltage measurement can be positive or negative due to bidirectional currents in the system; therefore the data value in shunt voltage register can be positive or negative. The bus voltage register data value is always positive. The output data can be directly converted into voltage by multiplying the digital value by the respective resolution size.

Furthermore, the device provides the flexibility to report calculated current in Amperes, power in Watts, as described in *Current and Power Calculations*.

8.1.2 Current and Power Calculations

For the INA2227 to report current values in Amperes, a constant conversion value must be written in each of the calibration registers that is dependent on the selected CURRENT_LSB and the shunt resistance used in the application for each channel. The value of the calibration register is calculated based on Equation 1. The term CURRENT_LSB is the chosen LSB step size for the CURRENT register where the current is stored. Equation 2 shows the minimum value of CURRENT_LSB is based on the maximum expected current, and the equation directly defines the maximum resolution of the CURRENT register. While the smallest CURRENT_LSB value yields highest resolution, this value is common for selecting a higher round-number (no higher than 8x) value for the CURRENT_LSB to simplify the conversion of the CURRENT.

The R_{SHUNT} term is the resistance value of the external shunt used to develop the differential voltage across the IN+ and IN– pins. Use Equation 1 for ADCRANGE = 0. For ADCRANGE = 1, the value of SHUNT_CAL must be divided by 4.

$$SHUNT\_CAL = \frac{0.00512}{Current\_LSB \times R_{SHUNT}} \tag{1}$$

where

- 0.00512 is an internal fixed value used to verify that scaling is maintained properly.
- CURRENT_LSB is a selected value for the current step size in amperes. Must be greater than or equal to CURRENT_LSB (minimum), but less than 8 x CURRENT_LSB(minimum) to reduce resolution loss.
- The value of SHUNT_CAL must be divided by 4 for ADCRANGE = 1.

$$CURRENT\_LSB\ (minimum) = \frac{Maximum\ Expected\ Current}{2^{15}} \tag{2}$$

Note that the current is calculated following a shunt voltage measurement based on the value set in the SHUNT_CAL field. If the value loaded into the SHUNT_CAL field is zero, the current value reported through the CURRENT register is also zero.

After programming the SHUNT_CAL field with the calculated value, the measured current in Amperes can be read from the CURRENT register. Use Equation 3 to calculate the final value scaled by the CURRENT_LSB:

$$Current\ [A] = CURRENT\_LSB \times CURRENT \tag{3}$$

where

- CURRENT is the value read from the CURRENT register

The power value can be read from the POWER register as an unsigned 16-bit value. Use Equation 4 to convert the power to Watts:

$$Power\ [W] = 32 \times CURRENT\_LSB \times POWER \tag{4}$$

where

- POWER is the value read from the POWER register.
- CURRENT_LSB is chosen lsb size for the selected channel.

The energy values can be read from the each ENERGY register as a 32-bit unsigned value. Use Equation 5 to convert the energy to Joules:

$$\text{Energy [J]} = 32 \times \text{CURRENT\_LSB} \times \text{ENERGY} \tag{5}$$

where

- ENERGY is the value read from the each ENERGY register.
- CURRENT_LSB is chosen lsb size for the selected channel.

8.1.3 ADC Output Data Rate and Noise Performance

The INA2227 noise performance and effective resolution depend on the ADC conversion time. The device also supports digital averaging which can further help decrease digital noise. The flexibility of the device to select ADC conversion time and data averaging offers increased signal-to-noise ratio and achieves the highest dynamic range with lowest offset. The profile of the noise at lower signals levels is dominated by the system noise that is comprised mainly of 1/f noise or white noise. The effective resolution of the ADC can be increased by increasing the conversion time and increasing the number of averages.

Table 8-2 summarizes the output data rate conversion settings supported by the device. The fastest conversion setting is 140µs. Typical noise-free resolution is represented as Effective Number of Bits (ENOB) based on device measured data. The ENOB is calculated based on noise peak-to-peak values, which verifies that full noise distribution is taken into consideration.

Table 8-2. INA2227 Noise performance, current measurement, single channel enabled

ADC CONVERSION TIME PERIOD [µs]	OUTPUT SAMPLE AVERAGING [SAMPLES]	OUTPUT SAMPLE PERIOD [ms]	NOISE-FREE ENOB (±81.92mV) (ADCRANGE = 0)	NOISE-FREE ENOB (±20.48mV) (ADCRANGE = 1)
140	1	0.14	13.1	11.1
204	1	0.204	13.4	11.1
332	1	0.332	14.1	11.7
588	1	0.588	14.7	12.2
1100	1	1.1	14.7	12.5
2116	1	2.116	15.1	13.4
4156	1	4.156	15.7	14.1
8244	1	8.244	16.0	14.7
140	4	0.56	14.1	12.1
204	4	0.816	14.4	12.4
332	4	1.328	15.1	12.9
588	4	2.352	15.7	13.4
1100	4	4.4	15.7	13.7
2116	4	8.464	16.0	14.7
4156	4	16.624	16.0	14.7
8244	4	32.976	16.0	15.7
140	16	2.24	15.1	13.1
204	16	3.264	15.7	13.4
332	16	5.312	15.7	14.1
588	16	9.408	16.0	14.4
1100	16	17.6	16.0	15.1
2116	16	33.856	16.0	15.7

Table 8-2. INA2227 Noise performance, current measurement, single channel enabled (continued)

ADC CONVERSION TIME PERIOD [µs]	OUTPUT SAMPLE AVERAGING [SAMPLES]	OUTPUT SAMPLE PERIOD [ms]	NOISE-FREE ENOB (±81.92mV) (ADCRANGE = 0)	NOISE-FREE ENOB (±20.48mV) (ADCRANGE = 1)
4156	16	66.496	16.0	15.7
8244	16	131.904	16.0	16.0
140	64	8.96	15.7	13.7
204	64	13.056	16.0	14.4
332	64	21.248	16.0	15.1
588	64	37.632	16.0	15.7
1100	64	70.4	16.0	15.7
2116	64	135.424	16.0	16.0
4156	64	265.984	16.0	16.0
8244	64	527.616	16.0	16.0
140	128	17.92	16.0	14.1
204	128	26.112	16.0	15.1
332	128	42.496	16.0	15.7
588	128	75.264	16.0	15.7
1100	128	140.8	16.0	16.0
2116	128	270.848	16.0	16.0
4156	128	531.968	16.0	16.0
8244	128	1055.232	16.0	16.0
140	256	35.84	16.0	14.7
204	256	52.224	16.0	15.7
332	256	84.992	16.0	15.7
588	256	150.528	16.0	16.0
1100	256	281.6	16.0	16.0
2116	256	541.696	16.0	16.0
4156	256	1063.936	16.0	16.0
8244	256	2110.464	16.0	16.0
140	512	71.68	16.0	15.1
204	512	104.448	16.0	15.7
332	512	169.984	16.0	16.0
588	512	301.056	16.0	16.0
1100	512	563.2	16.0	16.0
2116	512	1083.392	16.0	16.0
4156	512	2127.872	16.0	16.0
8244	512	4220.928	16.0	16.0
140	1024	143.36	16.0	15.7
204	1024	208.896	16.0	16.0
332	1024	339.968	16.0	16.0
588	1024	602.112	16.0	16.0
1100	1024	1126.4	16.0	16.0
2116	1024	2166.784	16.0	16.0
4156	1024	4255.744	16.0	16.0
8244	1024	8441.856	16.0	16.0

8.1.4 Filtering and Input Considerations

Measuring current is often noisy and such noise can be difficult to define. The INA2227 offers several options for filtering by allowing the conversion times and number of averages to be selected independently in the Configuration register (0h). The conversion times can be set independently for the shunt voltage and bus voltage measurements to allow added flexibility when configuring the monitoring of the power-supply bus.

The internal ADC is based on a delta-sigma (ΔΣ) front-end with a 500kHz (±0.5% max) sampling rate. This architecture has good inherent noise rejection; however, transients that occur at or very close to the sampling rate harmonics can cause problems. These signals are at 1MHz and higher and can be managed by incorporating filtering at the device input. The high frequency enables the use of low-value series resistors on the filter with negligible effects on measurement accuracy. In general, filtering the device input is only necessary if there are transients at exact harmonics of the 500kHz (±0.5% max) sampling rate (greater than 1MHz). Filter using the lowest possible series resistance (typically 100Ω or less) and a ceramic capacitor. Recommended values for this capacitor are between 0.1µF and 1µF. Figure 8-1 illustrates the device with a filter added at the input.

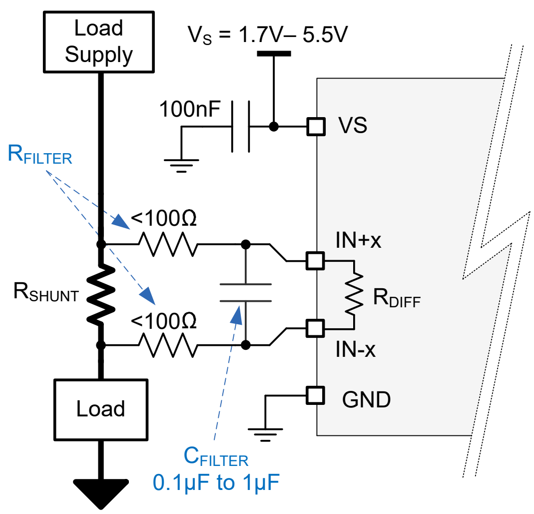


Figure 8-1. Input Filtering

Overload conditions are another consideration for the device inputs. The device inputs are specified to tolerate 26V across the inputs. A large differential scenario can be a short to ground on the load side of the shunt. This type of event can result in the full bus power-supply voltage across the shunt (as long the power supply or energy storage capacitors can support this voltage). Removing a short to ground can result in inductive kickbacks that can exceed the 26V differential and 48V common-mode rating of the device. Inductive kickback voltages are best controlled by Zener-type, transient-absorbing devices (commonly called *transzorbs*) combined with sufficient energy storage capacitance. The *Current Shunt Monitor with Transient Robustness Reference Design* describes a high-side, current-shunt monitor used to measure the voltage developed across a current-sensing resistor and how to better protect the current-sense device from transient overvoltage conditions.

In applications that do not have large energy storage electrolytics on one or both sides of the shunt, an input overstress condition can result from an excessive dV/dt of the voltage applied to the input. A hard physical short is the most likely cause of this event, and the excessive dV/dt can activate the ESD protection in systems with large currents. Testing demonstrates that the addition of 10Ω resistors in series with each input of the device sufficiently protects against dV/dt failures up to the 48V rating of the device. Selecting these resistors in the range noted has minimal effect on accuracy.

8.1.5 eFuse Current and Power Monitoring

The additional bus pin of the INA2227 allows the device to be used in a low-side sensing configuration. This configuration allows power and current monitoring in eFuse applications without the need for an additional power current sense resistor. To monitor the eFuse current, the inputs of the INA2227 are connected to a resistor that is in series with the CS or IMON pin as shown in Figure 8-2.

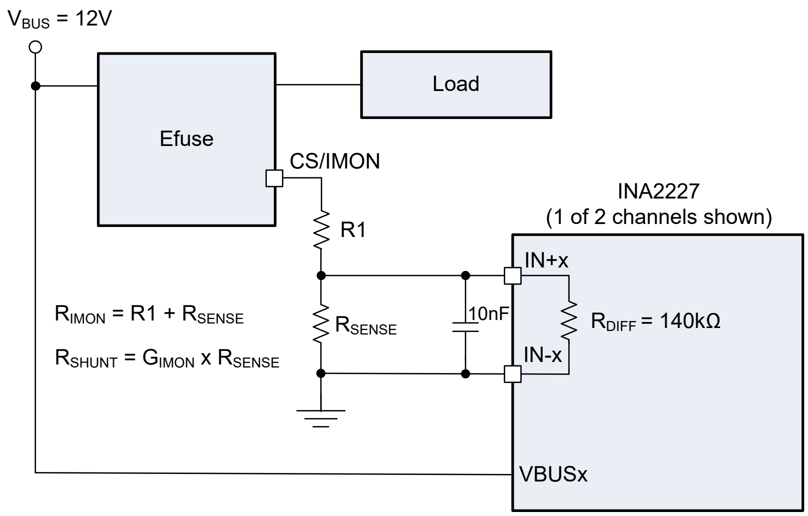


Figure 8-2. eFuse Application Circuit for Current and Power Monitoring

The R_{SENSE} resistor is sized so the full scale input range determined by the RANGE bit is not exceeded at the maximum eFuse IMON current. To allow adjustment of the IMON resistance and additional series resistor R1 is added above the R_{SENSE} resistor. The VBUS pin must connect to either the input or output of the eFuse to monitor the power sourced from the power supply or power delivered to the load.

Because the current monitored by the INA2227 is a scaled-down version of the actual load current, the value for the RSHUNT used in Section 8.1.2 is calculated by multiplying the current monitor gain (G_{IMON}) of the eFuse by the selected R_{SENSE} resistor.

To take advantage of the full scale input range of the device, the value for the RSENSE resistor is larger than what is typically used in traditional current sense applications. The differential input impedance of the INA2227, R_{DIFF}, results in some additional measurement error. The typical error induced is the result of the change in the RSENSE value with the parallel addition of the internal R_{DIFF} impedance of 140kΩ. For example, an RSENSE value of 75Ω in parallel with the internal 140kΩ resistor results in an effective sense resistor of 74.96Ω which is 0.054% lower than the expected resistance. This additional error adds to the overall gain error of the device. For most applications, this error is negligible when compared to the tolerance of eFuse current gain.

To minimize noise and errors induced by ADC sampling with larger than typical RSENSE values, a 10nF capacitor must be added across at the inputs of the INA2227 when used in eFuse applications. This additional capacitor must be placed as close to the device input pins as possible.

8.2 Typical Application

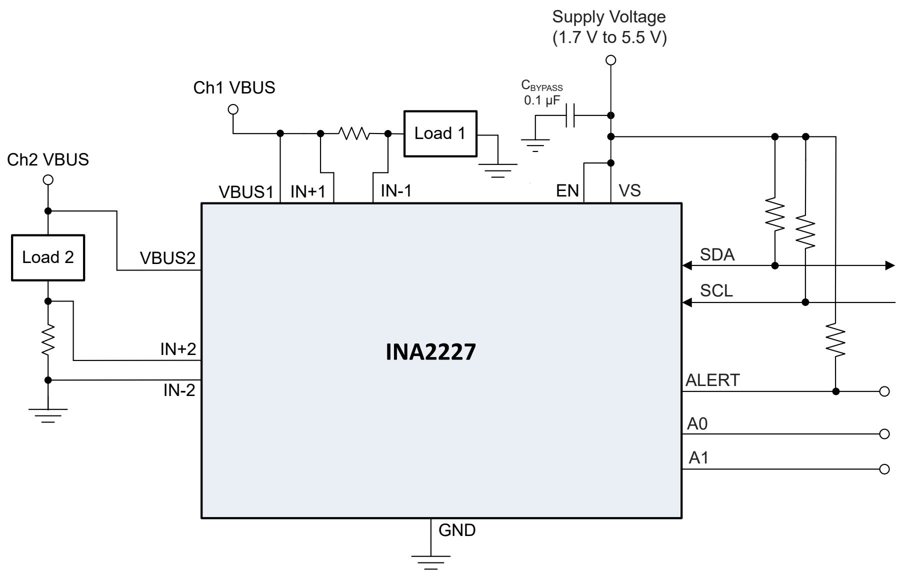


Figure 8-3. Typical Low-Side Sensing Circuit Configuration, INA2227

8.2.1 Design Requirements

The INA2227 features 2 channels that measure the voltage developed across a current-sensing resistor (R_{SHUNT}) when current passes through the resistor. The device also measures the bus supply voltage and calculates power and energy for each channel. The device also comes with alert capability, where the alert pin can be programmed to respond to a user-defined event or a conversion ready notification.

Table 8-3 lists the design requirements for a single channel of the circuit shown in Figure 8-3.

Table 8-3. Design Parameters for Channel 1

DESIGN PARAMETER	EXAMPLE VALUE
Power-supply voltage (V_S)	3.3V
Bus supply rail (V_{CM})	12V
Average Current	6A
Overcurrent fault threshold	9A
Maximum current monitored (I_{MAX})	10A
ADC Range Selection (V_{SENSE_MAX})	±81.92mV
Energy Accumulation Period	1 hour

8.2.2 Detailed Design Procedure

This design example walks through the process of selecting the shunt resistor, programming the calibration register, setting the correct fault thresholds, and how to properly scale returned values from the device for channel 1 of the device. The configuration of additional channels is similar with calculated values programmed into the registers corresponding to the appropriate channel.

8.2.2.1 Select the Shunt Resistor

Using values from Table 8-3, the maximum value of the shunt resistor is calculated based on the value of the maximum current to be sensed (I_{MAX}) and the maximum allowable sense voltage (V_{SENSE_MAX}) for the chosen ADC range. When operating at the maximum current, the differential input voltage must not exceed the maximum full scale range of the device, V_{SENSE_MAX}. Using Equation 6 for the given design parameters, the maximum value for R_{SHUNT} is calculated to be 8.192mΩ. The closest standard resistor value that is smaller than the maximum calculated value is 8.0mΩ. Smaller resistors can be used to minimize power loss at the expense of reduced accuracy. The shunt resistor selected must have sufficient wattage to handle the power dissipation at maximum load at the desired operating temperature.

$$R_{SHUNT} < \frac{V_{SENSE\_MAX}}{I_{MAX}} \quad (6)$$

8.2.2.2 Configure the Device

The first step to program the INA2227 is to properly set the device configuration registers, CONFIG1 and CONFIG2. On initial power up, the configuration registers are set to the reset values (see Table 7-3 and Table 7-4). In the default power on state the device is set to measured on the ±81.92mV range with the ADC continuously converting the shunt and bus voltages for all channels. If the default power up conditions do not meet the design requirements, these registers need to be set properly after each disable or V_S power cycle event.

8.2.2.3 Program the Shunt Calibration Registers

There are two shunt calibration registers for each channel that need to be correctly programmed after each power up for the device to properly report any result based on current. The first step to calculate the value for the calibration register is to calculate the minimum LSB value for the current by using Equation 2. Applying this equation with the maximum expected current of 10A results in an minimum LSB size of 305.17578µA. The INA2227 allows selection of the CURRENT_LSB to be up to 8 times larger than the minimum LSB size. For this example a value of 500µA is used. Applying Equation 1 to the Current_LSB and selected value for the shunt resistor results in a shunt calibration register setting of 1280d (500h). Failure to set the value of the shunt calibration registers results in a zero value for any result based on current for that channel. Programming these registers is not required for reading shunt voltage, bus voltage or setting corresponding alert limits.

8.2.2.4 Set Desired Fault Thresholds

The INA2227 has the ability to assert the alert pin on several different fault conditions as described in Alert Configuration Registers. The desired fault condition to assert the alert pin needs to be selected by appropriately programming the ALERT MASK field in the Alert Configuration Register. Fault thresholds are set by programming the desired trip threshold into the Alert Limit Registers.

For example, channel 1 can be configured to alert on an over current condition by setting the ALERT1 register CHANNEL field to channel 1(00b) with the ALERT MASK field set to shunt over voltage (001b). The desired threshold for the over current condition has to be programmed in the Limit1 Register. In this example, the over current threshold is 9.0A and the value of the current sense resistor is 8.0mΩ, which give a shunt voltage limit of 72mV. Once the shunt voltage limit is known, the value for the shunt over voltage limit register is calculated by dividing the shunt voltage limit by the shunt voltage LSB size.

For this case, the calculated value of the alert limit register is 72mV / 2.5µV = 28800d (7080h).

Values stored in the LIMIT1 and LIMIT2 registers are set to the default values when the device is disabled or V_S is power cycled.

Fault limits programmed into the LIMIT registers can be applied to a single channel or distributed to each of the 2 measurement channels. For example, if monitoring of the bus voltage is also required on channel 1, the CHANNEL field of the ALERT2 register can be also set to channel 1(00b) with the ALERT MASK field set to monitor over bus conditions (011b). The value for the over voltage fault can be set as desired in the LIMIT2 register.

8.2.2.5 Calculate Returned Values

Parametric values are calculated by multiplying the returned value by the LSB value. Table 8-4 shows the returned values for this application example, assuming the design requirements shown in Table 8-3.

Table 8-4. Register Values

Register	Contents	LSB Value	Calculated Value
Shunt_Voltage_CH1 (00h)	19200d (4B00h)	2.5µV	19200 × 2.5µV = 0.048V

Table 8-4. Register Values (continued)

Register	Contents	LSB Value	Calculated Value
Bus_Voltage_CH1 (01h)	7500d (1D4Ch)	1.6mV	7500 × 1.6mV = 12V
Current_CH1 (02h)	12000d (2EE0h)	Current LSB = 500µA	12000 × 500µA = 6A
Power_CH1 (03h)	4500d (1194h)	Current LSB x 32 = 16mW	4500 × 16mW = 72W
Energy_CH1 (04h)	16200000d (00F7 3140h)	Current LSB x 32 = 16mJ	16200000 × 16mJ = 259.2kJ

Shunt Voltage and Current return values in two's complement format. In two's complement format a negative value in binary is represented by having a 1 in the most significant bit of the returned value. These values can be converted to decimal by first inverting all the bits and adding 1 to obtain the unsigned binary value. This value must then be converted to decimal with the negative sign applied.

8.2.3 Application Curves

Figure 8-4 and Figure 8-5 show the ALERT pin response to a BUS over voltage fault with a conversion time of 140µs for the bus voltage measurements with averaging set to 1. For these scope shots, persistence is enabled on the ALERT channel to show the variation in the alert response for many sequential fault events. The alert response time can change depending on the value of the current before fault occurs as well as the how much the fault condition exceeds the programmed fault threshold. Figure 8-4 shows the response time for an overcurrent fault when the fault condition greatly exceeds the programmed threshold. While Figure 8-5 shows the over voltage response time when the fault slightly exceeds the programmed threshold. Variation in the alert response exists because the external fault event is not synchronized to the internal ADC conversion start. Also the ADC is constantly sampling to get a result, so the response time for fault events starting from zero are slower than fault events starting from values near the set fault threshold. In applications where the alert timing is critical, the worst-case alert response is equal to 2 × (t_{conv_shunt} + $t_{conv\_voltage}$) × number of channels enabled. When alerting on over power conditions, an additional 60µs needed to allow for background math calculations.

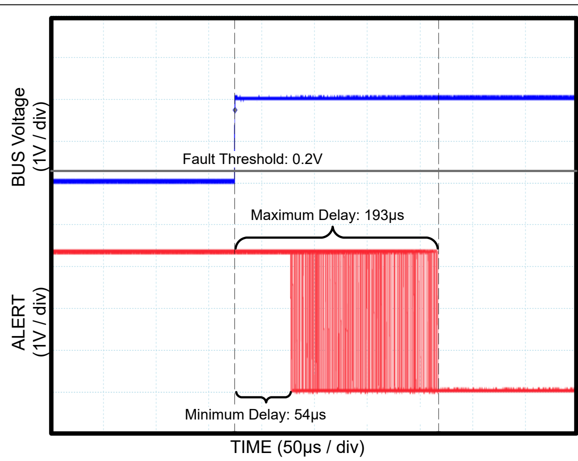


Figure 8-4. Alert Response Time (Sampled Values Significantly Above Threshold)

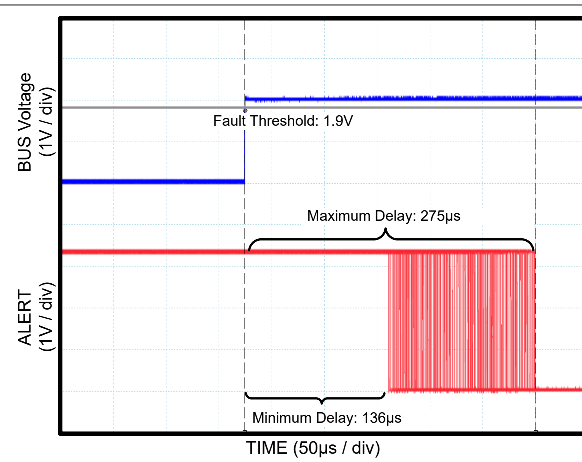


Figure 8-5. Alert Response Time (Sampled Values Slightly Above Threshold)

8.3 Power Supply Recommendations

Figure 8-3 shows that the device input circuitry can accurately measure signals on common-mode voltages beyond the power-supply voltage, V_S. For example, the voltage applied to the VS power supply pin can be 5V, whereas the bus power-supply voltage being monitored (the common-mode voltage) can be as high as 48V. The device can also withstand the full -0.3V to 48V range at the input pins, regardless of whether the device has power applied or not.

Place the required power-supply bypass capacitors as close as possible to the supply and ground pins of the device to provide stability. A typical value for this supply bypass capacitor is 0.1µF. Applications with noisy or high-impedance power supplies can require additional decoupling capacitors to reject power-supply noise.

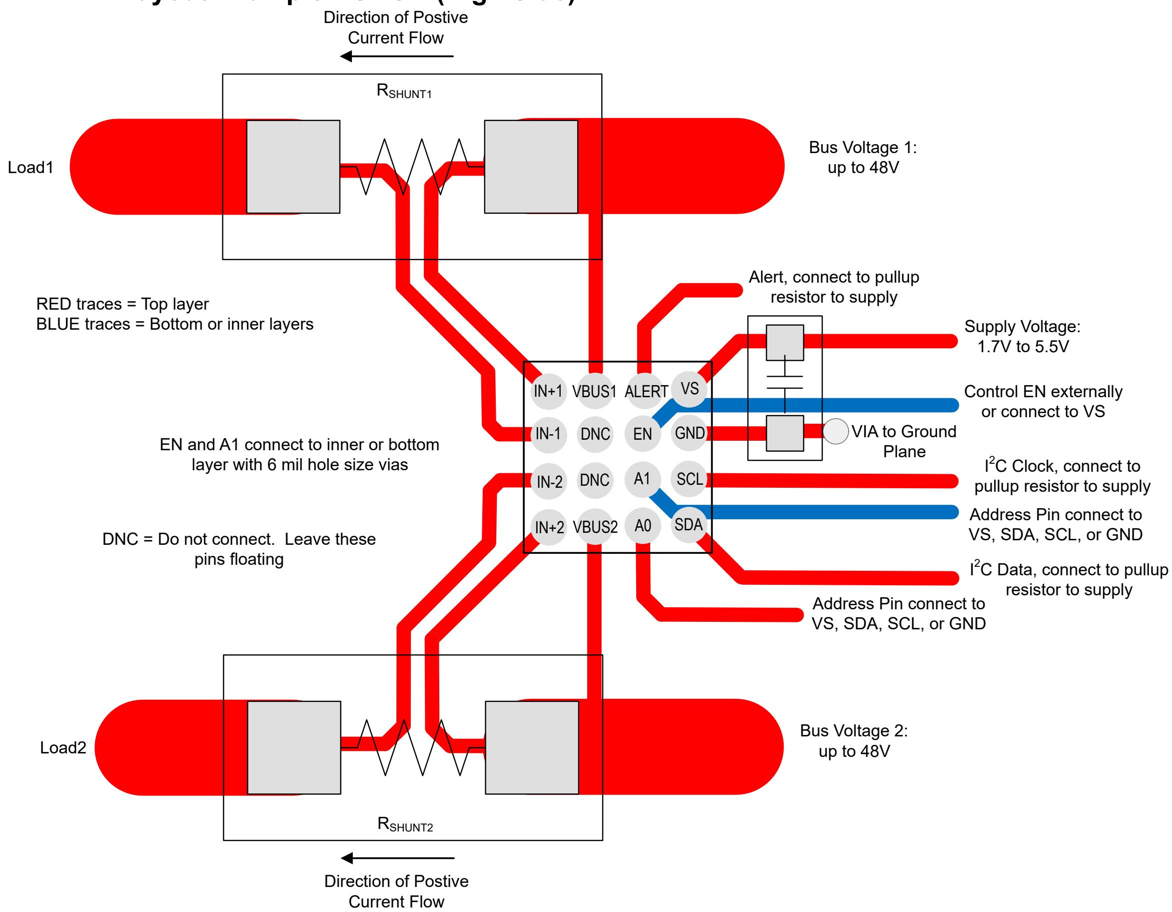
8.4 Layout

8.4.1 Layout Guidelines

Connect all input pins (IN+X and IN–X) to the sensing resistor using a Kelvin connection or a 4-wire connection for each channel. These connection techniques verify that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current-sensing resistor, any additional high-current carrying impedance causes significant measurement errors. Place the power-supply bypass capacitor as close as possible to the supply and ground pins.

8.4.2 Layout Example

INA2227 Layout Example DSBGA (High Side)



9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

For development support see the following:

INA2227EVM User's Guide

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Current Shunt Monitor with Transient Robustness Reference Design*, Design guide
- Texas Instruments, *INA2227EVM User's Guide*

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

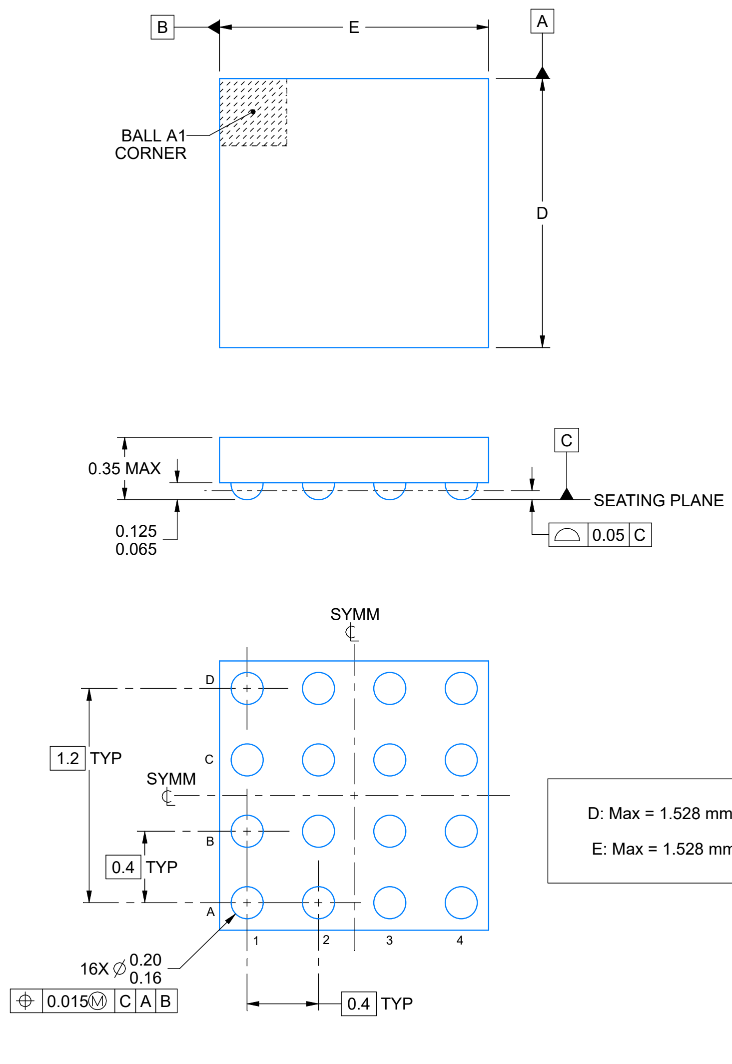
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

YBJ0016-C01

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.528 mm, Min = 1.488 mm
E: Max = 1.528 mm, Min = 1.488 mm

NOTES:

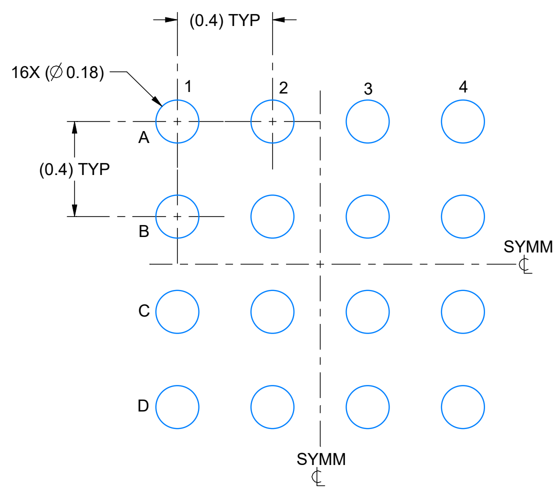
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

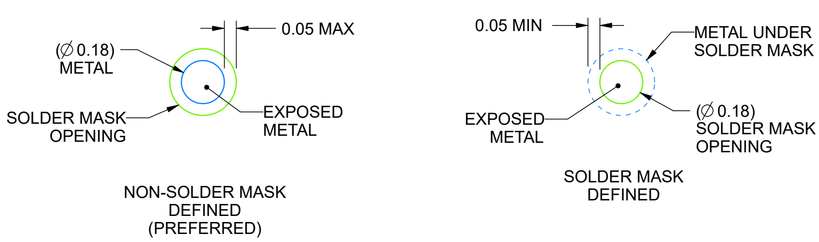
YBJ0016-C01

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

4228994/B 04/2023

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

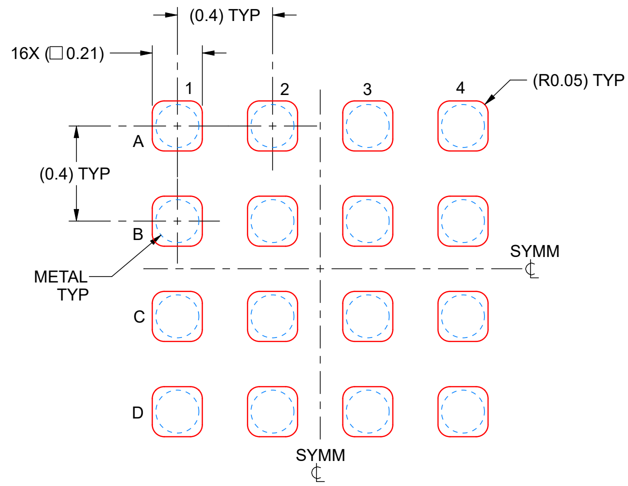
TEXAS INSTRUMENTS
www.ti.com

EXAMPLE STENCIL DESIGN

YBJ0016-C01

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 40X

4228994/B 04/2023

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA2227AIYBJR	Active	Production	DSBGA (YBJ) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	I27

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

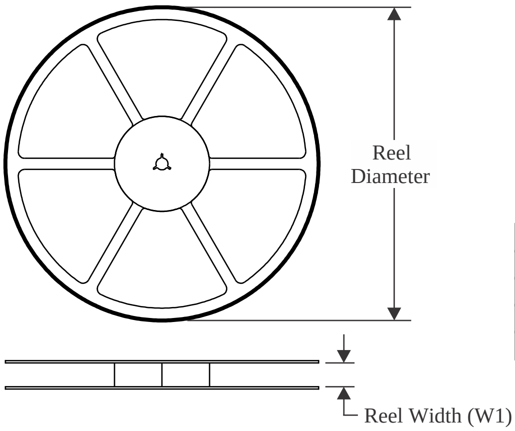
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

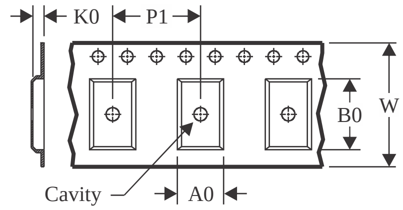
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

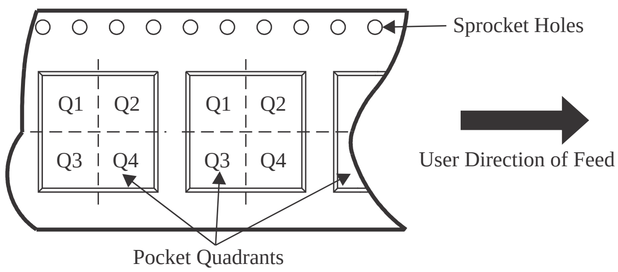


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

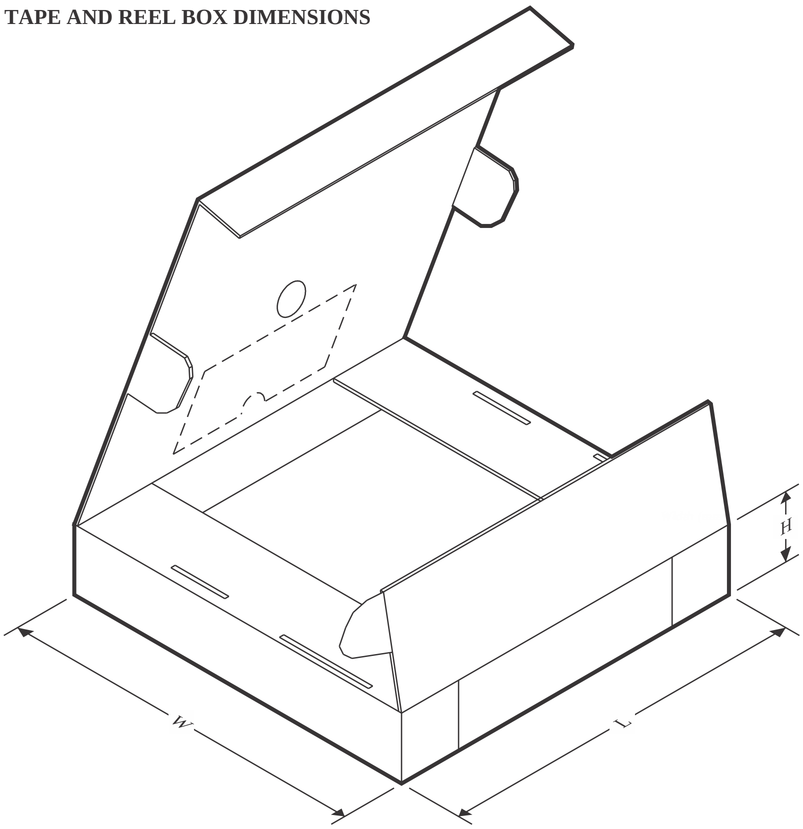
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA2227AIYBJR	DSBGA	YBJ	16	3000	180.0	8.4	1.68	1.68	0.39	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA2227AIYBJR	DSBGA	YBJ	16	3000	182.0	182.0	20.0