Burr-Brown Products
from Texas Instruments

INA163

Low-Noise, Low-Distortion INSTRUMENTATION AMPLIFIER

FEATURES

- LOW NOISE: 1nV/√Hz at 1kHz
- LOW THD+N: 0.002% at 1kHz, G = 100
- WIDE BANDWIDTH: 800kHz at G = 100
- WIDE SUPPLY RANGE: ±4.5V to ±18V
- HIGH CMR: > 100dB
- GAIN SET WITH EXTERNAL RESISTOR
- SO-14 SURFACE-MOUNT PACKAGE

APPLICATIONS

- PROFESSIONAL MICROPHONE PREAMPS
- MOVING-COIL TRANSDUCER AMPLIFIERS
- DIFFERENTIAL RECEIVERS
- BRIDGE TRANSDUCER AMPLIFIERS

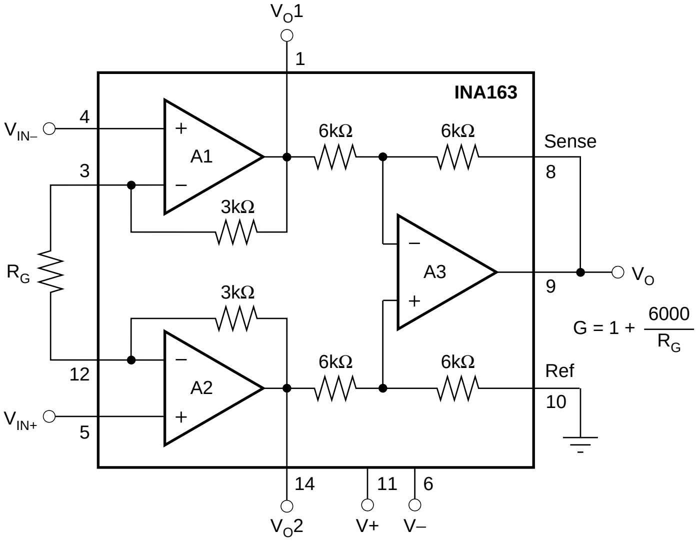
DESCRIPTION

The INA163 is a very low-noise, low-distortion, monolithic instrumentation amplifier. Its current-feedback circuitry achieves very wide bandwidth and excellent dynamic response over a wide range of gain. It is ideal for low-level audio signals such as balanced low-impedance microphones. Many industrial, instrumentation, and medical applications also benefit from its low noise and wide bandwidth.

Unique distortion cancellation circuitry reduces distortion to extremely low levels, even in high gain. The INA163 provides near-theoretical noise performance for 200Ω source impedance. Its differential input, low noise, and low distortion provide superior performance in professional microphone amplifier applications.

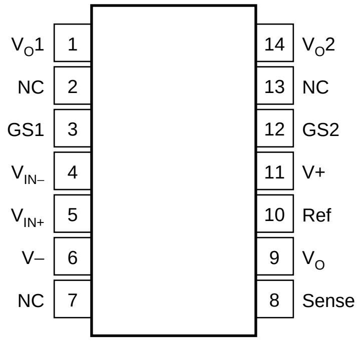
The INA163's wide supply voltage, excellent output voltage swing, and high output current drive allow its use in high-level audio stages as well.

The INA163 is available in a space-saving SO-14 surface-mount package, specified for operation over the –40°C to +85°C temperature range.



PIN CONFIGURATION

Top View



NC = No Internal Connection

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

Power Supply Voltage	±18V
Signal Input Terminals, Voltage(2)	(V–) – 0.5V to (V+) + 0.5V
Current(2)	10mA
Output Short-Circuit to Ground	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	DESIGNATOR	MARKING
INA163UA	SO-14 Surface Mount	D	INA163UA

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this document, or see the TI web site at www.ti.com.

ELECTRICAL CHARACTERISTICS: $V_S = \pm15V$

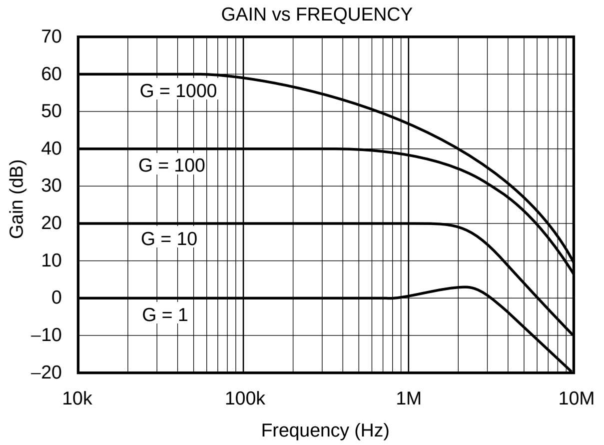
T_A = +25°C and at rated supplies, V_S = ±15V, R_L = 2kΩ connected to ground, unless otherwise noted.

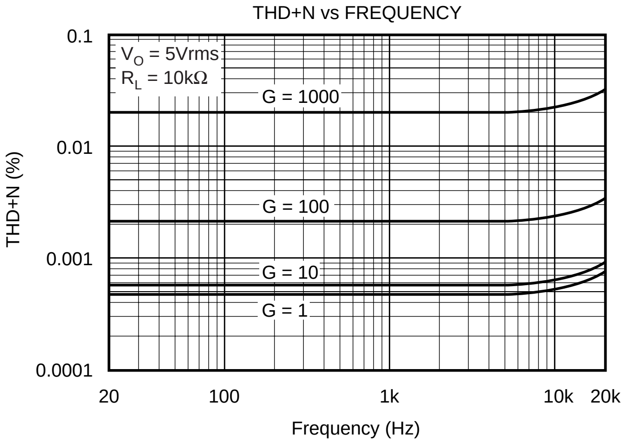
		INA163UA			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
GAIN					
Range			1 to 10000		V/V
Gain Equation(1)			$G = 1 + 6k/R_G$		
Gain Error, G = 1			±0.1	±0.25	%
G = 10			±0.2	±0.7	%
G = 100			±0.2		%
G = 1000			±0.5		%
Gain Temp Drift Coefficient, G = 1			±1	±10	ppm/°C
G > 10			±25	±100	ppm/°C
Nonlinearity, G = 1			±0.0003		% of FS
G = 100			±0.0006		% of FS
INPUT STAGE NOISE					
Voltage Noise	$R_{SOURCE} = 0\Omega$				
f_O = 1kHz			1		nV/$\sqrt{Hz}$
f_O = 100Hz			1.2		nV/$\sqrt{Hz}$
f_O = 10Hz			2		nV/$\sqrt{Hz}$
Current Noise					
f_O = 1kHz			0.8		pA/$\sqrt{Hz}$
OUTPUT STAGE NOISE					
Voltage Noise, f_O = 1kHz			60		nV/$\sqrt{Hz}$
INPUT OFFSET VOLTAGE					
Input Offset Voltage	$V_{CM} = V_{OUT} = 0V$		50 + 2000/G	250 + 5000/G	µV
vs Temperature	$T_A = T_{MIN}$ to T_{MAX}		1 + 20/G		µV/°C
vs Power Supply	V_S = ±4.5V to ±18V		1 + 50/G	3 + 200/G	µV/V
INPUT VOLTAGE RANGE					
Common-Mode Voltage Range	$V_{IN+} - V_{IN-} = 0V$	(V+) – 4	(V+) – 3		V
	$V_{IN+} - V_{IN-} = 0V$	(V–) + 4	(V–) + 3		V
Common-Mode Rejection, G = 1	V_{CM} = ±11V, $R_{SRC} = 0\Omega$	70	80		dB
G = 100		100	116		dB
INPUT BIAS CURRENT					
Initial Bias Current			2	12	µA
vs Temperature			10		nA/°C
Initial Offset Current			0.1	1	µA
vs Temperature			0.5		nA/°C
INPUT IMPEDANCE					
	Differential		60 ‖ 2		MΩ ‖ pF
	Common-Mode		60 ‖ 2		MΩ ‖ pF
DYNAMIC RESPONSE					
Bandwidth, Small Signal, –3dB, G = 1			3.4		
G = 100			800		kHz
Slew Rate			15		V/µs
THD+Noise, f = 1kHz	G = 100		0.002		%
Settling Time, 0.1%	G = 100, 10V Step		2		µs
0.01%	G = 100, 10V Step		3.5		µs
Overload Recovery	50% Overdrive		1		µs
OUTPUT					
Voltage	R_L = 2kΩ to Gnd	(V+) – 2	(V+) – 1.8		V
		(V–) + 2	(V–) + 1.8		V
Load Capacitance Stability			1000		pF
Short-Circuit Current	Continuous-to-Common		±60		mA
POWER SUPPLY					
Rated Voltage			±15		V
Voltage Range		±4.5		±18	V
Current, Quiescent	I_O = 0mA		±10	±12	mA
TEMPERATURE RANGE					
Specification		–40		+85	°C
Operating		–40		+125	°C
θ_{JA}			100		°C/W

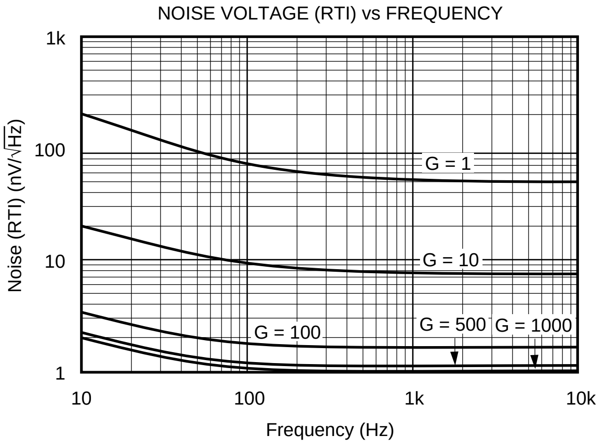
NOTE: (1) Gain accuracy is a function of external R_G.

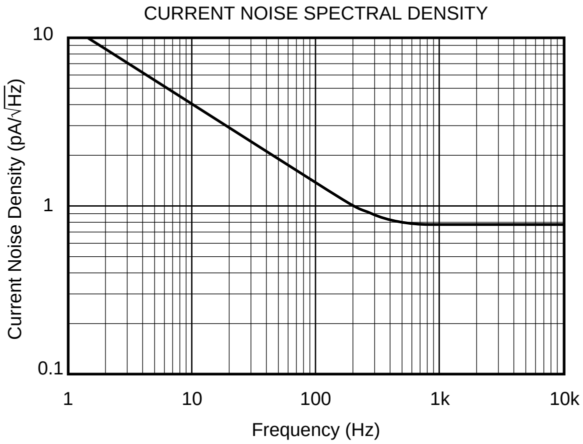
TYPICAL CHARACTERISTICS

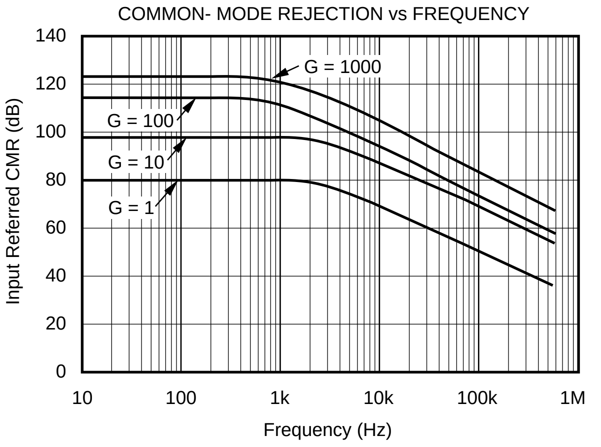
At $T_A = +25°C$, $V_S = 5V$, $V_{CM} = 1/2V_S$, $R_L = 25k\Omega$, CL = 50pF, unless otherwise noted.

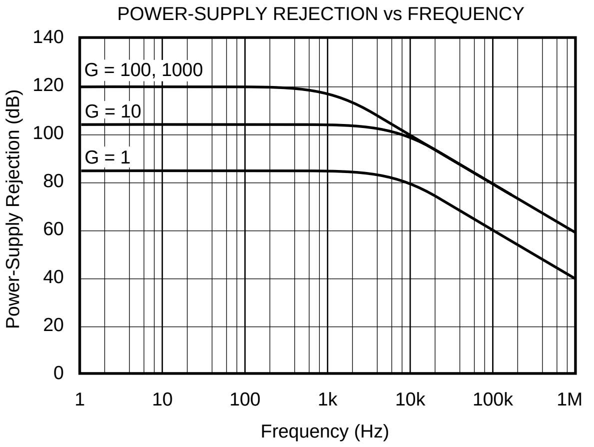








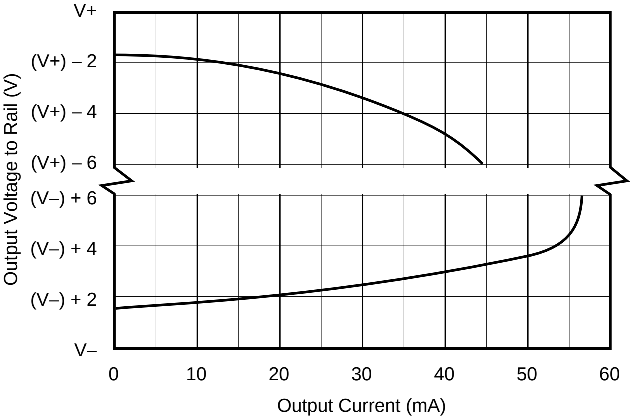




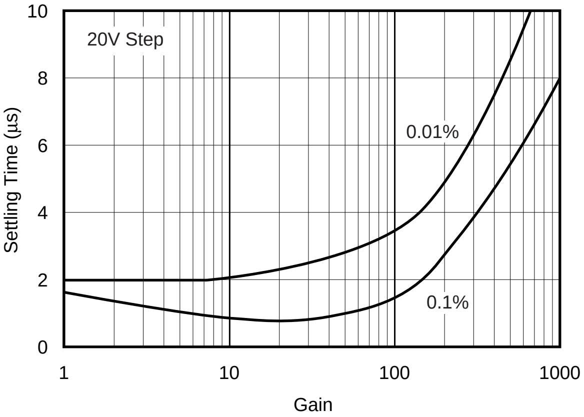
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = 5V, V_{CM} = 1/2V_S, R_L = 25kΩ, CL = 50pF, unless otherwise noted.

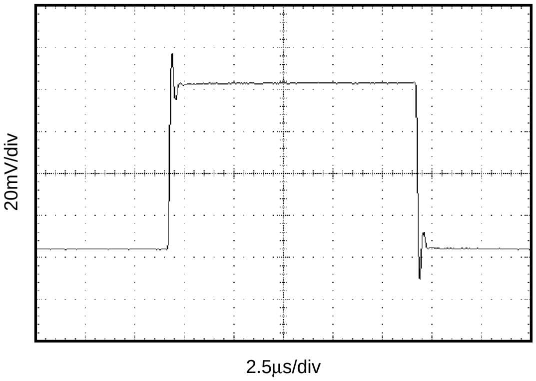
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



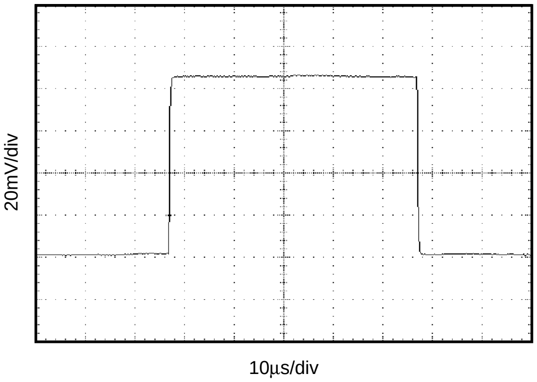
SETTLING TIME vs GAIN



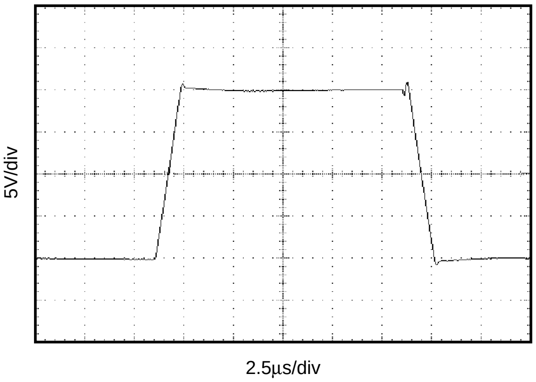
SMALL-SIGNAL TRANSIENT RESPONSE (G = 1)



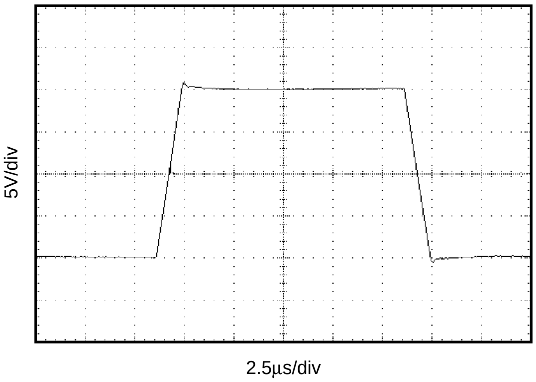
SMALL-SIGNAL TRANSIENT RESPONSE (G = 100)



LARGE-SIGNAL TRANSIENT RESPONSE (G = 1)



LARGE-SIGNAL TRANSIENT RESPONSE (G = 100)



APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for operation. Power supplies should be bypassed with 0.1µF tantalum capacitors near the device pins. The output Sense (pin 8) and output Reference (pin 10) should be low-impedance connections. Resistance of a few ohms in series with these connections will degrade the common-mode rejection of the INA163.

GAIN-SET RESISTOR

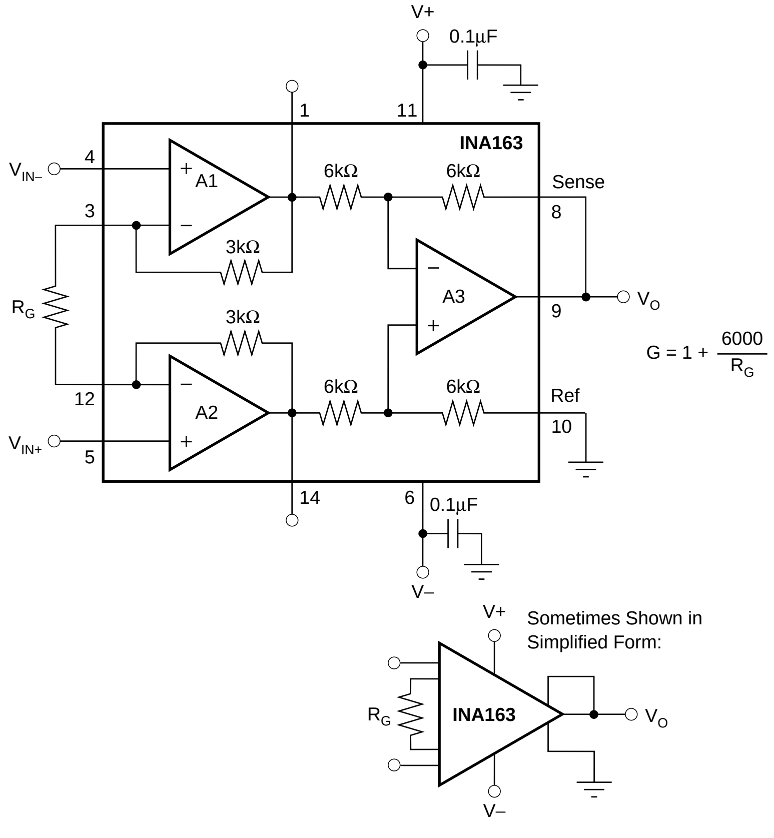
Gain is set with an external resistor, R_G, as shown in Figure 1. The two internal 3kΩ feedback resistors are laser-trimmed to 3kΩ within approximately ±0.2%. Gain is:

$$G = 1 + \frac{6000}{R_G}$$

The temperature coefficient of the internal 3kΩ resistors is approximately ±25ppm/°C. Accuracy and TCR of the external R_G will also contribute to gain error and temperature drift. These effects can be inferred from the gain equation. Make a short, direct connection to the gain set resistor, R_G. Avoid running output signals near these sensitive input nodes.

NOISE PERFORMANCE

The INA163 provides very low-noise with low-source impedance. Its $1nV/\sqrt{Hz}$ voltage noise delivers near-theoretical noise performance with a source impedance of 200Ω. The input stage design used to achieve this low noise, results in relatively high input bias current and input bias current noise. As a result, the INA163 may not provide the best noise performance with a source impedance greater than 10kΩ. For source impedance greater than 10kΩ, other instrumentation amplifiers may provide improved noise performance.



GAIN (V/V)	GAIN (dB)	R_G (Ω)
1	0	NC[1]
2	6	6000
5	14	1500
10	20	667
20	26	316
50	34	122
100	40	61
200	46	30
500	54	12
1000	60	6
2000	66	3

NOTE: (1) NC = No Connection.

FIGURE 1. Basic Circuit Connections.

INPUT CONSIDERATIONS

Very low source impedance (less than 10Ω) can cause the INA163 to oscillate. This depends on circuit layout, signal source, and input cable characteristics. An input network consisting of a small inductor and resistor, as shown in Figure 2, can greatly reduce any tendency to oscillate. This is especially useful if a variety of input sources are to be connected to the INA163. Although not shown in other figures, this network can be used as needed with all applications shown.

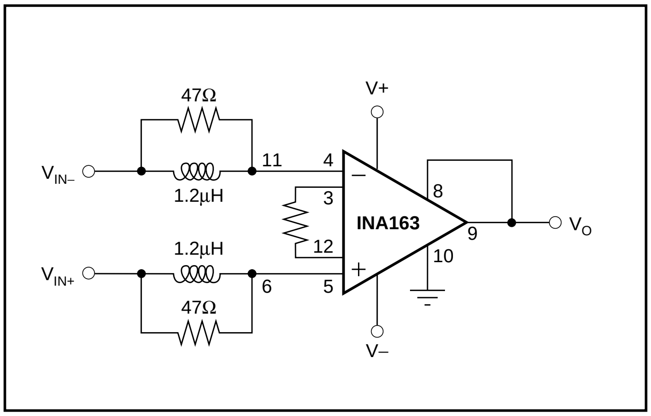


FIGURE 2. Input Stabilization Network.

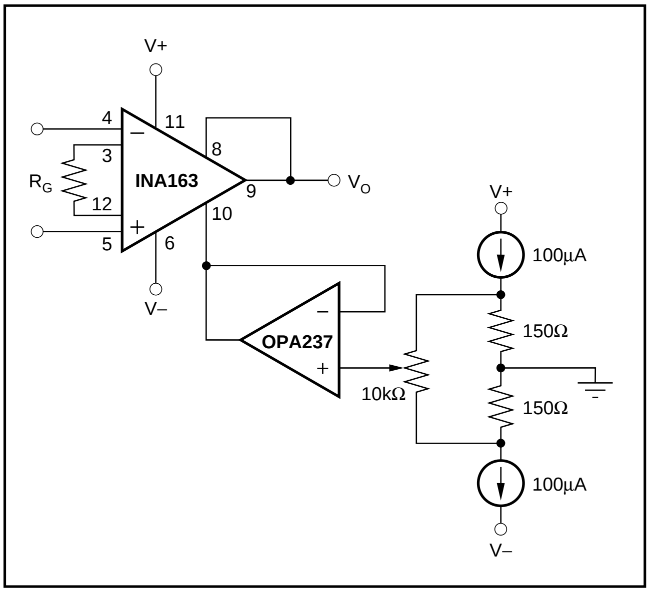


FIGURE 3. Offset Voltage Adjustment Circuit.

OFFSET VOLTAGE TRIM

A variable voltage applied to pin 10, as shown in Figure 3, can be used to adjust the output offset voltage. A voltage applied to pin 10 is summed with the output signal. An op amp connected as a buffer is used to provide a low impedance at pin 10 to assure good common-mode rejection.

OUTPUT SENSE

An output sense terminal allows greater gain accuracy in driving the load. By connecting the sense connection at the load, I • R voltage loss to the load is included inside the feedback loop. Current drive can be increased by connecting a buffer amp inside the feedback loop, as shown in Figure 4.

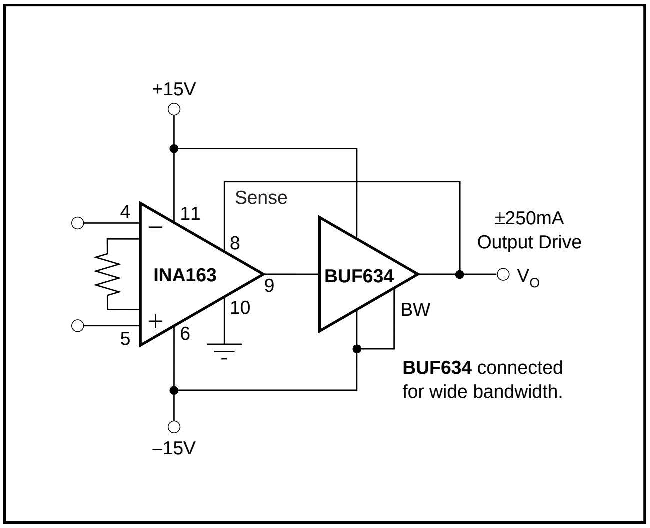


FIGURE 4. Buffer for Increase Output Current.

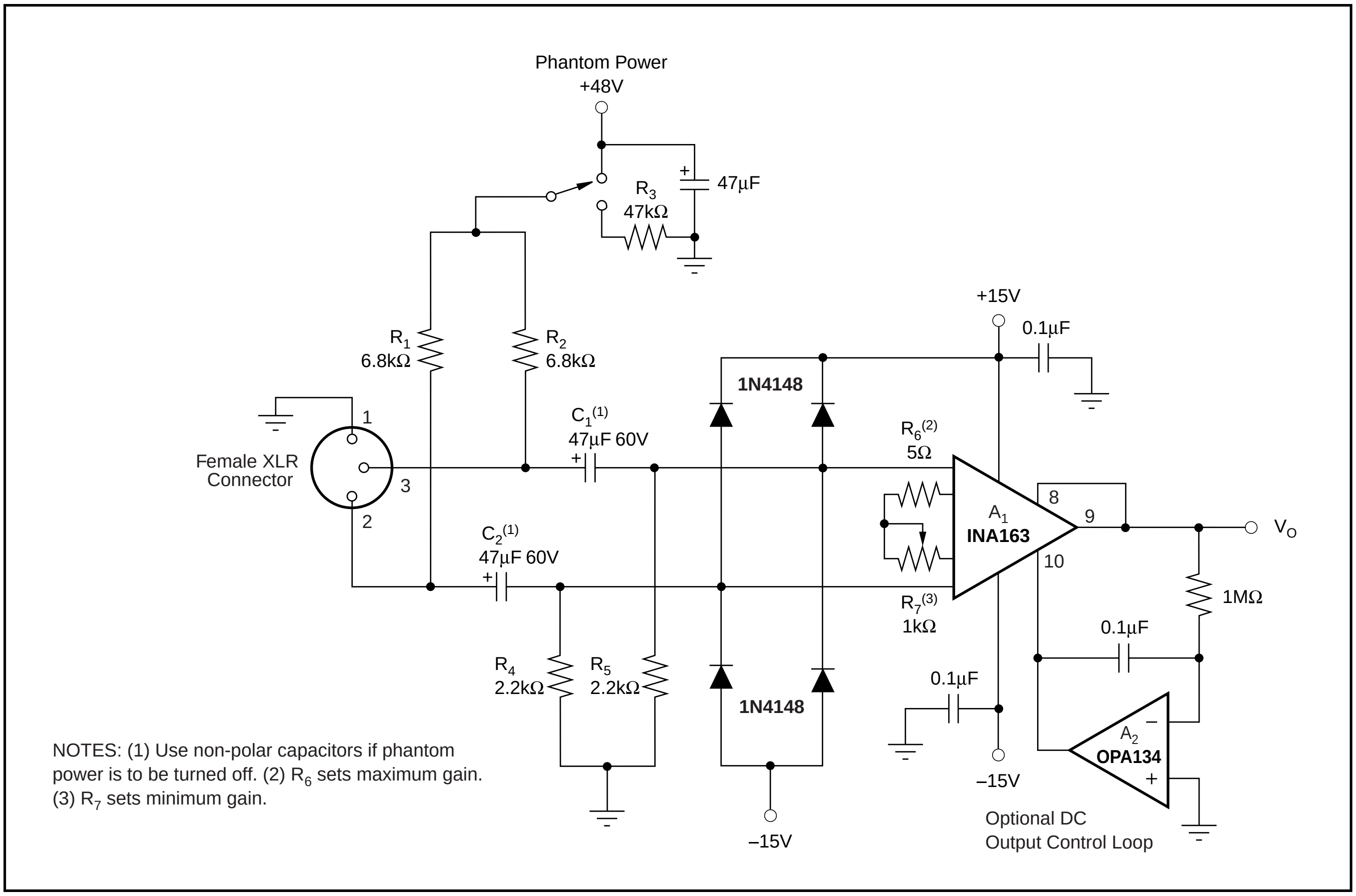


FIGURE 5. Phantom-Powered Microphone Preamplifier.

MICROPHONE AMPLIFIER

Figure 5 shows a typical circuit for a professional microphone input amplifier. R_1 and R_2 provide a current path for conventional 48V phantom power source for a remotely located microphone. An optional switch allows phantom power to be disabled. C_1 and C_2 block the phantom power voltage from the INA163 input circuitry. Non-polarized capacitors should be used for C_1 and C_2 if phantom power is to be disabled. For additional input protection against ESD and hot-plugging, four INA4148 diodes may be connected from the input to supply lines.

R_4 and R_5 provide a path for input bias current of the INA163. Input offset current (typically 100nA) creates a DC differential input voltage that will produce an output offset voltage. This is generally the dominant source of output offset voltage in this application. With a maximum gain of 1000 (60dB), the output offset voltage can be several volts. This may be entirely acceptable if the output is AC-coupled into the subsequent stage. An alternate technique is shown in Figure 5. An inexpensive FET-input op amp in a feedback loop drives the DC output voltage to 0V. A_2 is not in the audio signal path and does not affect signal quality.

Gain is set with a variable resistor, R_7, in series with R_6. R_6 determines the maximum gain. The total resistance, $R_6 + R_7$, determines the lowest gain. A special reverse-log taper potentiometer for R_7 can be used to create a linear change (in dB) with rotation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA163UA	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA163UA
INA163UA.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA163UA
INA163UA/2K5	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA163UA
INA163UA/2K5.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA163UA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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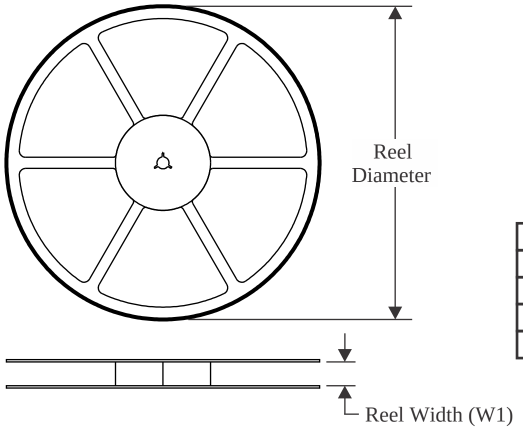
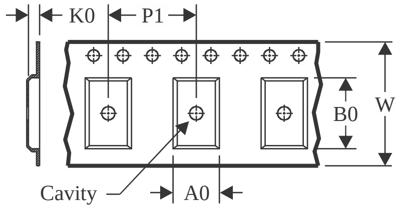
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

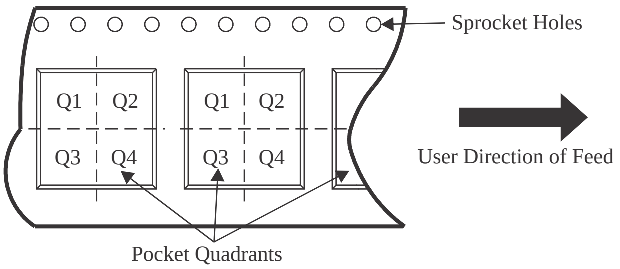


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

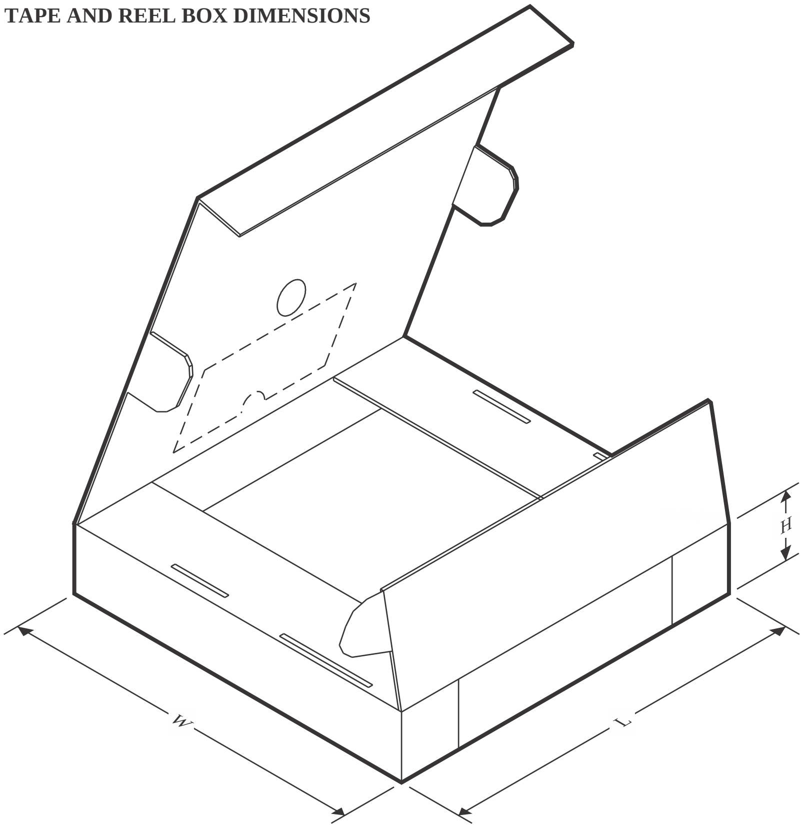
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA163UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

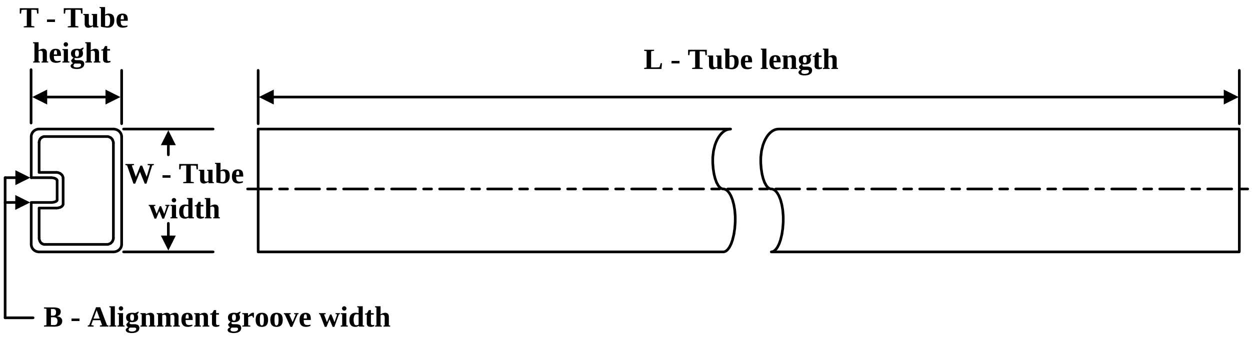
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

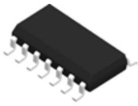
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA163UA/2K5	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA163UA	D	SOIC	14	50	506.6	8	3940	4.32
INA163UA.A	D	SOIC	14	50	506.6	8	3940	4.32

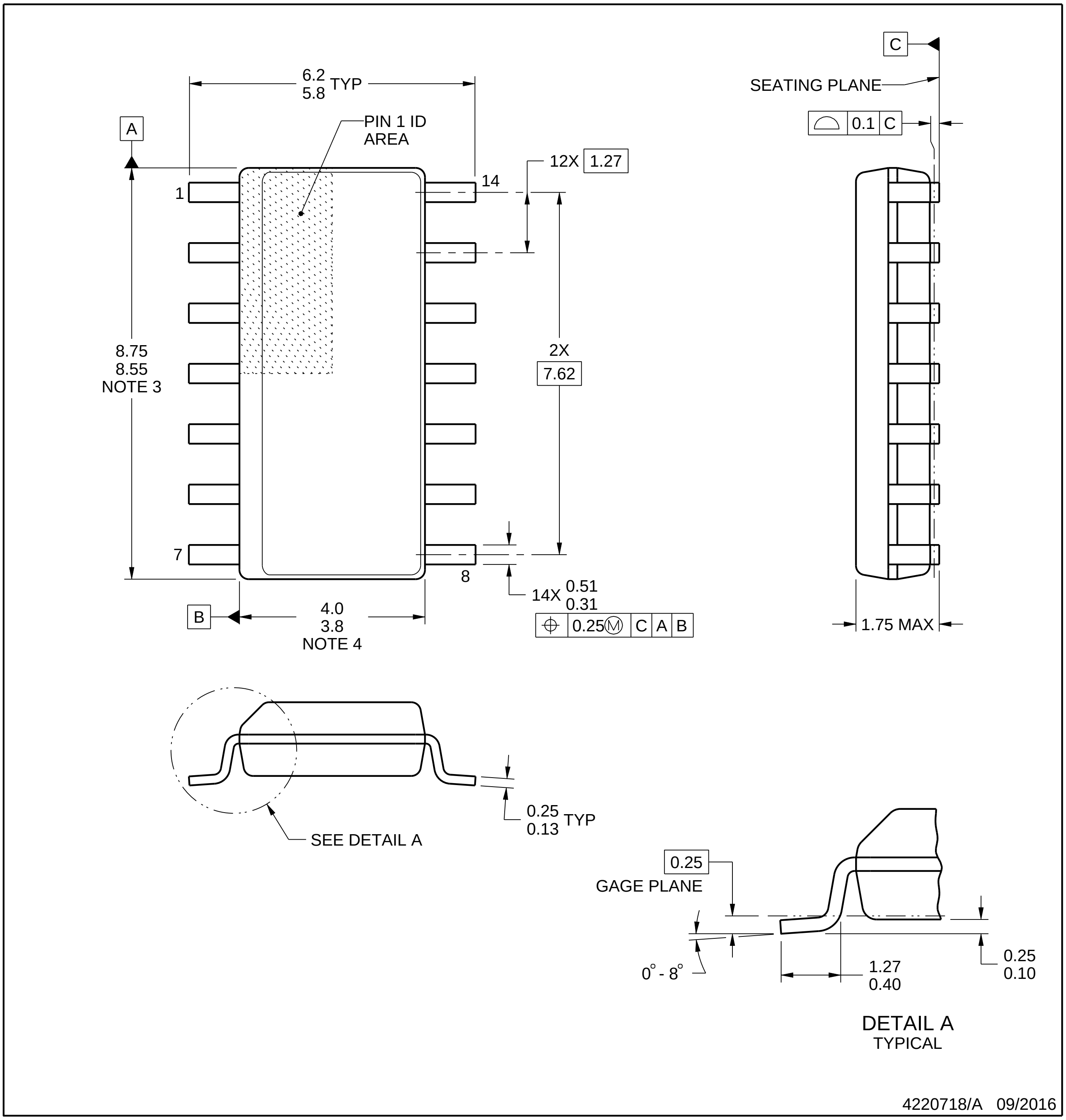


PACKAGE OUTLINE

D0014A

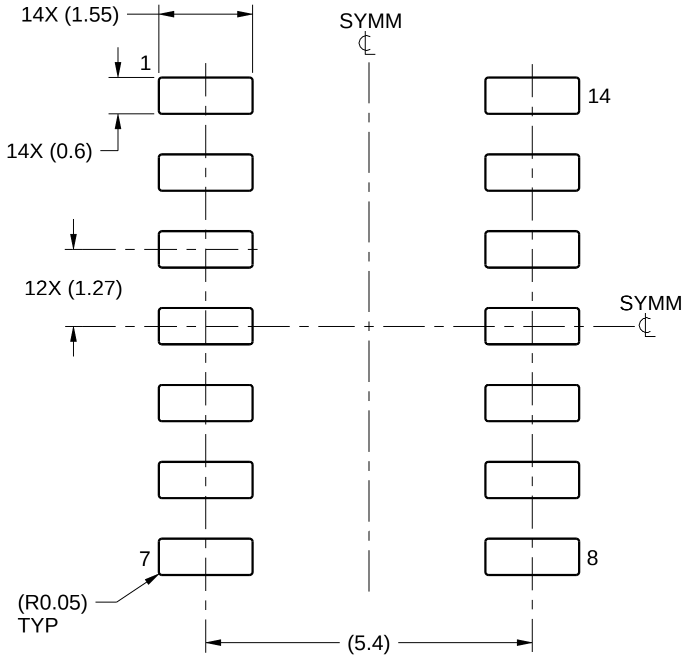
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

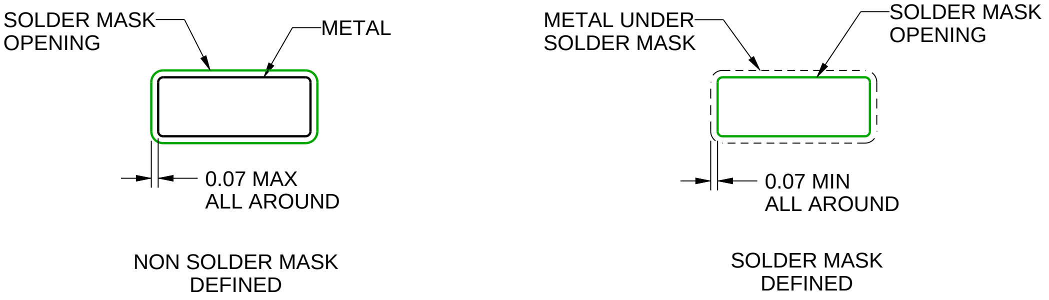


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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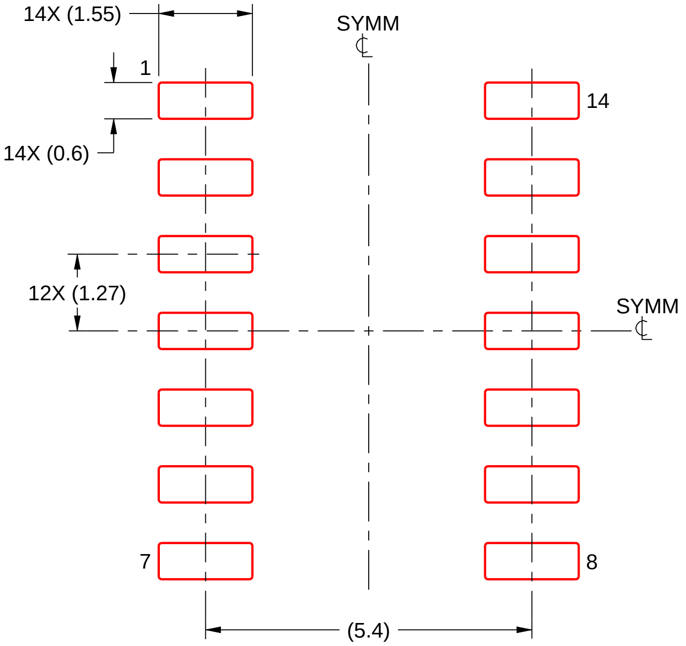
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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