



## Precision, Gain of 0.2 Level Translation DIFFERENCE AMPLIFIER

### FEATURES

- GAIN OF 0.2 TO INTERFACE  $\pm 10\text{V}$  SIGNALS TO SINGLE-SUPPLY ADCs
- GAIN ACCURACY:  $\pm 0.024\%$  (max)
- WIDE BANDWIDTH: 1.5MHz
- HIGH SLEW RATE:  $15\text{V}/\mu\text{s}$
- LOW OFFSET VOLTAGE:  $\pm 100\mu\text{V}$
- LOW OFFSET DRIFT:  $\pm 1.5\mu\text{V}/^\circ\text{C}$
- SINGLE-SUPPLY OPERATION DOWN TO 1.8V

### APPLICATIONS

- INDUSTRIAL PROCESS CONTROLS
- INSTRUMENTATION
- DIFFERENTIAL TO SINGLE-ENDED CONVERSION
- AUDIO LINE RECEIVERS

### DESCRIPTION

The INA159 is a high slew rate,  $G = 1/5$  difference amplifier consisting of a precision op amp with a precision resistor network. The gain of  $1/5$  makes the INA159 useful to couple  $\pm 10\text{V}$  signals to single-supply analog-to-digital converters (ADCs), particularly those operating on a single  $+5\text{V}$  supply. The on-chip resistors are laser-trimmed for accurate gain and high common-mode rejection. Excellent temperature coefficient of resistance (TCR) tracking of the resistors maintains gain accuracy and common-mode rejection over temperature. The input common-mode voltage range extends beyond the positive and negative supply rails. It operates on a total of  $+1.8\text{V}$  to  $+5.5\text{V}$  single or split supplies. The INA159 reference input uses two resistors for easy mid-supply or reference biasing.

The difference amplifier is the foundation of many commonly-used circuits. The INA159 provides this circuit function without using an expensive external precision resistor network. The INA159 is available in an MSOP-8 surface-mount package and is specified for operation over the extended industrial temperature range,  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

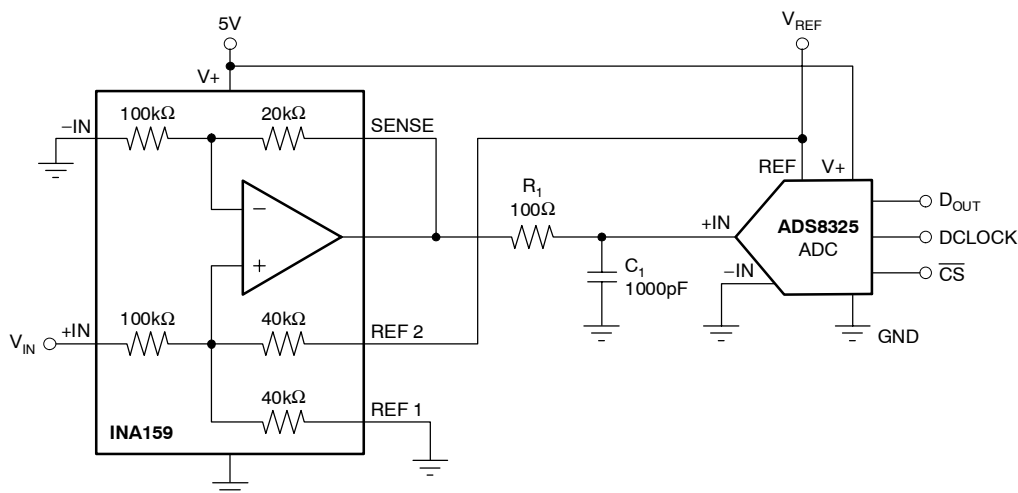


Figure 1. Typical Application



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

|                                                     |                            |
|-----------------------------------------------------|----------------------------|
| Supply Voltage .....                                | +5.5V                      |
| Signal Input Terminals (–IN and +IN), Voltage ..... | ±30V                       |
| Reference (REF 1 and REF2) and Sense Pins           |                            |
| Current .....                                       | ±10mA                      |
| Voltage .....                                       | (V–) – 0.5V to (V+) + 0.5V |
| Output Short Circuit .....                          | Continuous                 |
| Operating Temperature .....                         | –40°C to +150°C            |
| Storage Temperature .....                           | –65°C to +150°C            |
| Junction Temperature .....                          | +150°C                     |
| ESD Rating                                          |                            |
| Human Body Model .....                              | 4000V                      |
| Charged Device Model .....                          | 1000V                      |

<sup>(1)</sup> Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

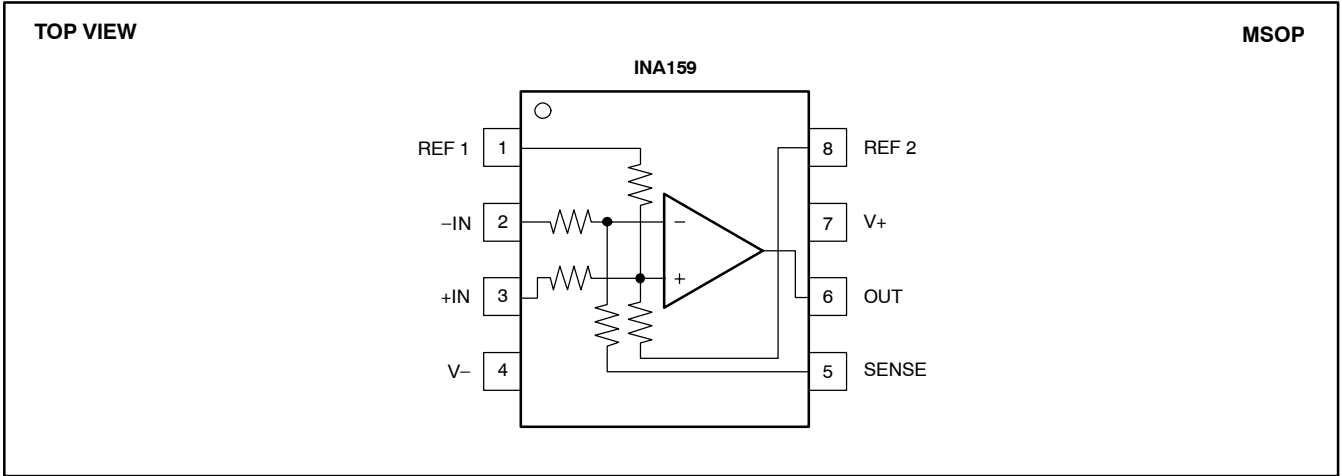
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**ORDERING INFORMATION<sup>(1)</sup>**

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | PACKAGE MARKING |
|---------|--------------|--------------------|-----------------|
| INA159  | MSOP-8       | DGK                | CJB             |

<sup>(1)</sup> For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

**PIN CONFIGURATIONS**



**ELECTRICAL CHARACTERISTICS:  $V_S = +5V$** 
**Boldface** limits apply over the specified temperature range,  $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

At  $T_A = +25^{\circ}\text{C}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , REF pin 1 connected to ground, and REF pin 2 connected to  $V_{REF} = 5V$ , unless otherwise noted.

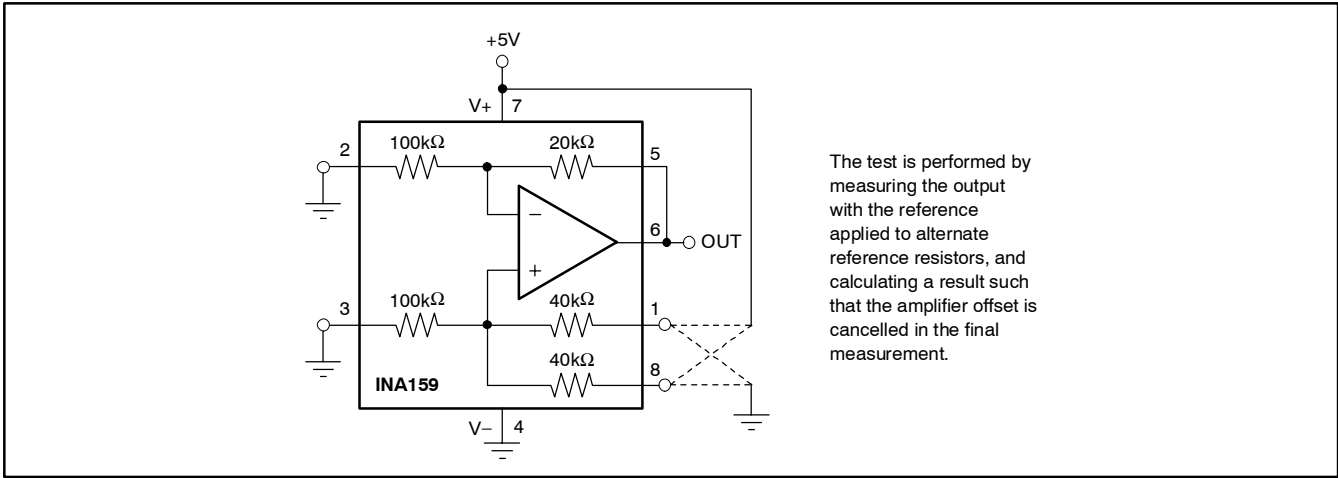
| PARAMETER                                                                                                                                                                                       | CONDITIONS                                                                                                                        | INA159                                                           |                                                                                                      |                                           | UNIT                                                                                          |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|-------------------------------------------|-----------------------------------------------------------------------------------------------|
|                                                                                                                                                                                                 |                                                                                                                                   | MIN                                                              | TYP                                                                                                  | MAX                                       |                                                                                               |
| <b>OFFSET VOLTAGE<sup>(1)</sup></b><br>Initial <sup>(1)</sup> $V_{OS}$<br><b>vs Temperature</b><br>vs Power Supply PSRR<br>Reference Divider Accuracy <sup>(2)</sup><br><b>over Temperature</b> | RTO<br>$V_S = \pm 2.5V$ , Reference and Input Pins Grounded<br><br>$V_S = \pm 0.9V$ to $\pm 2.75V$                                |                                                                  | $\pm 100$<br><b><math>\pm 1.5</math></b><br>$\pm 20$<br>$\pm 0.002$<br><b><math>\pm 0.002</math></b> | $\pm 500$<br><br>$\pm 100$<br>$\pm 0.024$ | $\mu V$<br>$\mu V/^{\circ}\text{C}$<br>$\mu V/V$<br>%<br>%                                    |
| <b>INPUT IMPEDANCE<sup>(3)</sup></b><br>Differential<br>Common-Mode                                                                                                                             |                                                                                                                                   |                                                                  | 240<br>60                                                                                            |                                           | $\text{k}\Omega$<br>$\text{k}\Omega$                                                          |
| <b>INPUT VOLTAGE RANGE</b><br>Common-Mode Voltage Range<br>Positive<br>Negative<br>Common-Mode Rejection Ratio<br><b>over Temperature</b>                                                       | RTI<br><br><br><br>$V_{CM} = -10V$ to $+10V$ , $R_S = 0\Omega$                                                                    | 80                                                               | 17.5<br>-12.5<br>96<br><b>94</b>                                                                     |                                           | V<br>V<br>dB<br><b>dB</b>                                                                     |
| <b>OUTPUT VOLTAGE NOISE<sup>(4)</sup></b><br>$f = 0.1\text{Hz}$ to $10\text{Hz}$<br>$f = 10\text{kHz}$                                                                                          | RTO                                                                                                                               |                                                                  | 10<br>30                                                                                             |                                           | $\mu V_{PP}$<br>$\text{nV}/\sqrt{\text{Hz}}$                                                  |
| <b>GAIN</b><br>Initial Error<br><b>vs Temperature</b><br>Nonlinearity                                                                                                                           | $V_{REF2} = 4.096V$ , $R_L$ Connected to GND,<br>$(V_{IN+}) - (V_{IN-}) = -10V$ to $+10V$ , $V_{CM} = 0V$<br><br>G                |                                                                  | 0.2<br>$\pm 0.005$<br><b><math>\pm 1</math></b><br>$\pm 0.0002$                                      | $\pm 0.024$                               | V/V<br>%<br><b><math>\text{ppm}/^{\circ}\text{C}</math></b><br>% of FS                        |
| <b>OUTPUT</b><br>Voltage, Positive<br>Voltage, Negative<br>Current Limit, Continuous to Common<br>Capacitive Load<br>Open-Loop Output Impedance                                                 | $V_{REF2} = 4.096V$ , $R_L$ Connected to GND<br>$V_{REF2} = 4.096V$ , $R_L$ Connected to GND<br><br>$f = 1\text{MHz}$ , $I_O = 0$ | $(V+) - 0.1$<br>$(V-) + 0.048$<br><br>See Typical Characteristic | $(V+) - 0.02$<br>$(V-) + 0.01$<br>$\pm 60$<br>110                                                    |                                           | V<br>V<br>mA<br>pF<br>$\Omega$                                                                |
| <b>FREQUENCY RESPONSE</b><br>Small-Signal Bandwidth<br>Slew Rate<br>Settling Time, 0.01%<br>Overload Recovery Time                                                                              | -3dB<br><br>4V Output Step, $C_L = 100\text{pF}$<br>50% Overdrive                                                                 |                                                                  | 1.5<br>15<br>1<br>250                                                                                |                                           | MHz<br>$V/\mu s$<br>$\mu s$<br>ns                                                             |
| <b>POWER SUPPLY</b><br>Specified Voltage Range<br>Operating Voltage Range<br>Quiescent Current                                                                                                  | $V_S$<br><br>$I_Q = 0\text{mA}$ , $V_S = \pm 2.5V$ ,<br>Reference and Input Pins Grounded<br><br>$I_Q$                            | +1.8                                                             | +5<br><br>1.1                                                                                        | +5.5<br><br>1.5                           | V<br>V<br>mA                                                                                  |
| <b>TEMPERATURE RANGE</b><br>Specified Range<br>Operating Range<br>Storage Range<br>Thermal Resistance<br>MSOP-8                                                                                 | <br><br><br>$\theta_{JA}$<br><br>Surface-Mount                                                                                    | -40<br>-40<br>-65                                                |                                                                                                      | +125<br>+150<br>+150                      | $^{\circ}\text{C}$<br>$^{\circ}\text{C}$<br>$^{\circ}\text{C}$<br>$^{\circ}\text{C}/\text{W}$ |

(1) Includes effects of amplifier input bias and offset currents.

(2) Reference divider accuracy specifies the match between the reference divider resistors using the configuration in Figure 2.

(3) Internal resistors are ratio matched but have  $\pm 20\%$  absolute value.

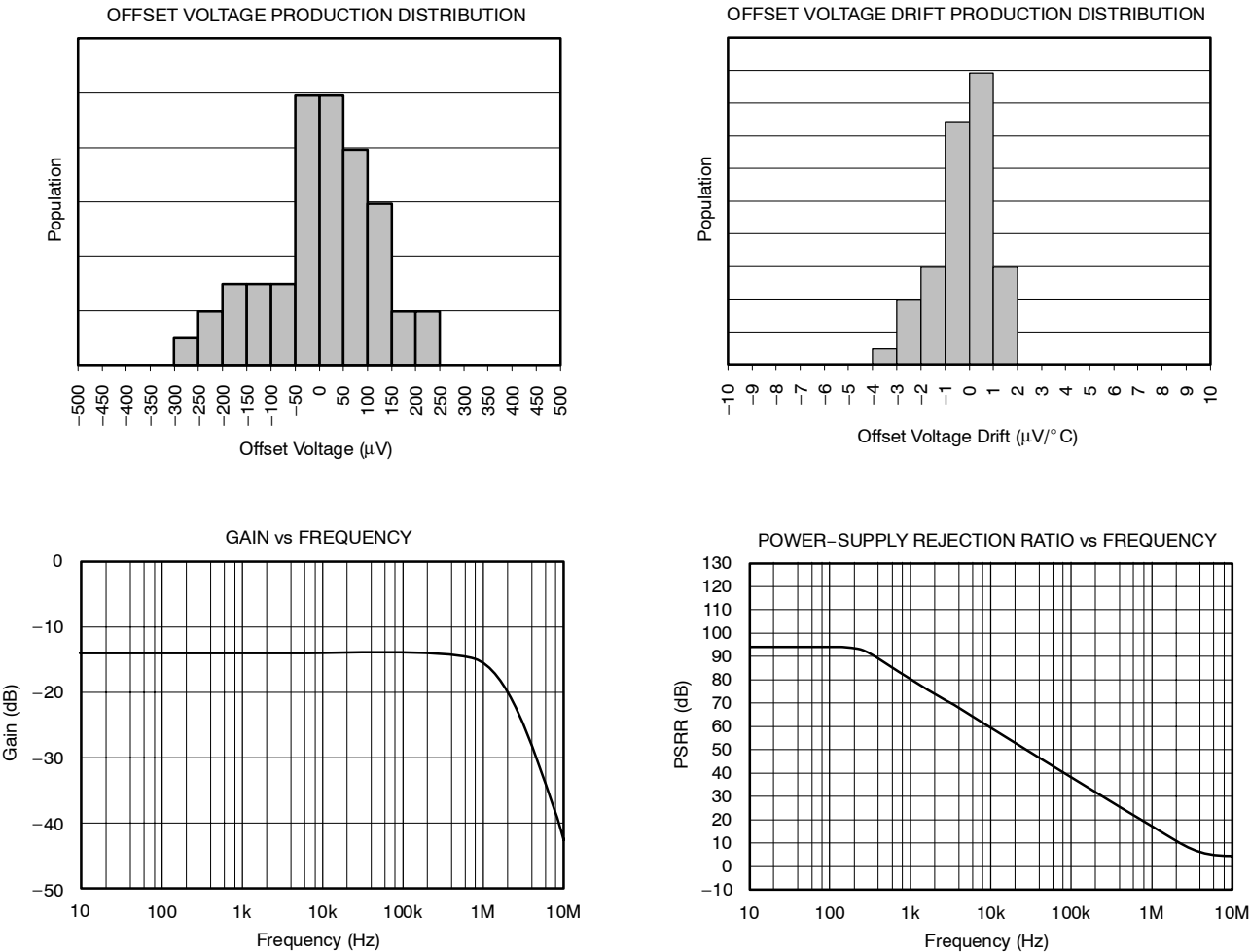
(4) Includes effects of amplifier input current noise and thermal noise contribution of resistor network.



**Figure 2. Test Circuit for Reference Divider Accuracy**

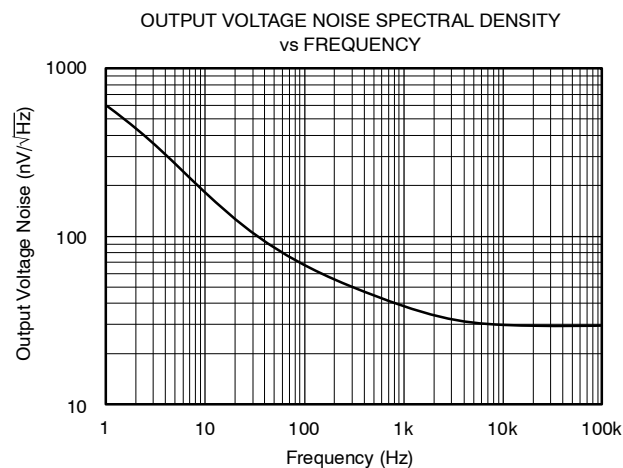
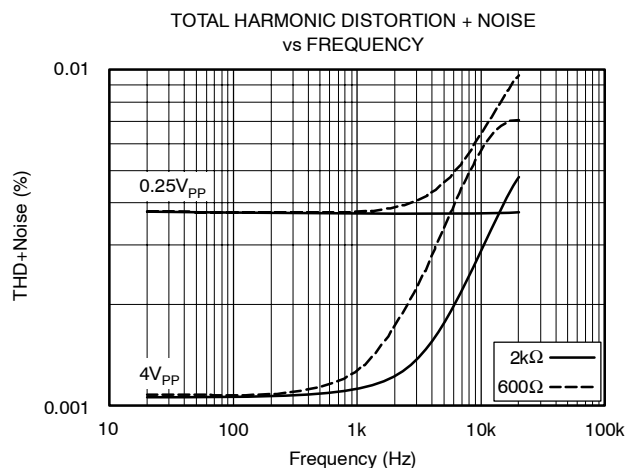
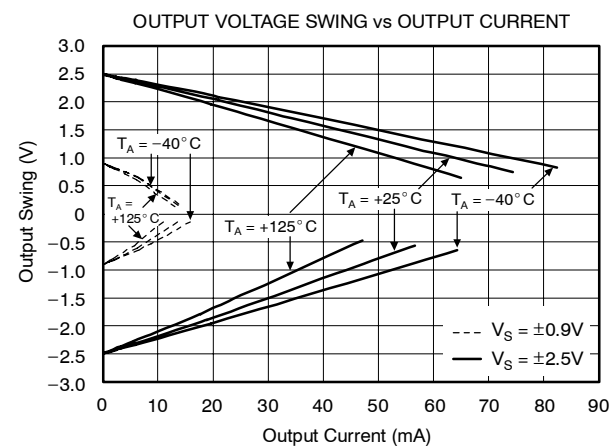
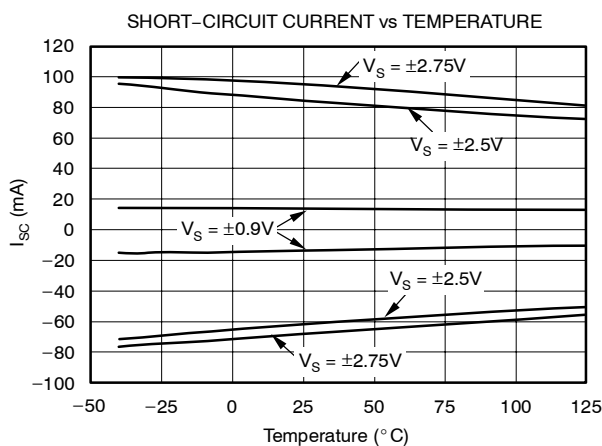
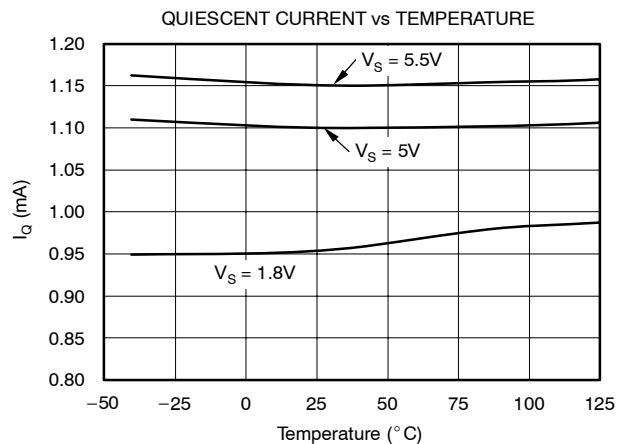
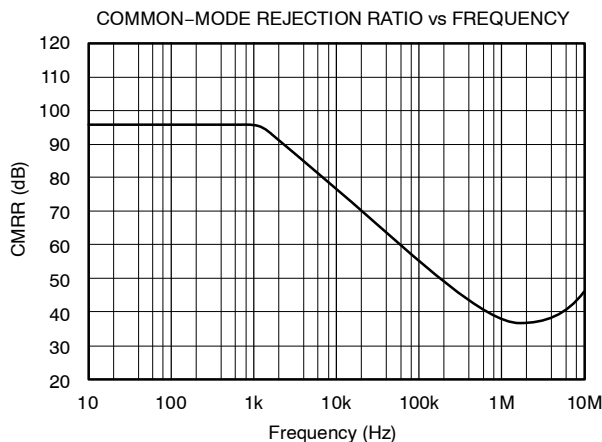
**TYPICAL CHARACTERISTICS**

At  $T_A = +25^\circ\text{C}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , REF pin 1 connected to ground, and REF pin 2 connected to  $V_{\text{REF}} = 5\text{V}$ , unless otherwise noted.



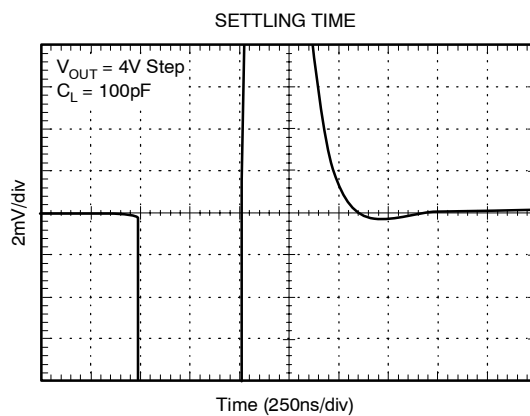
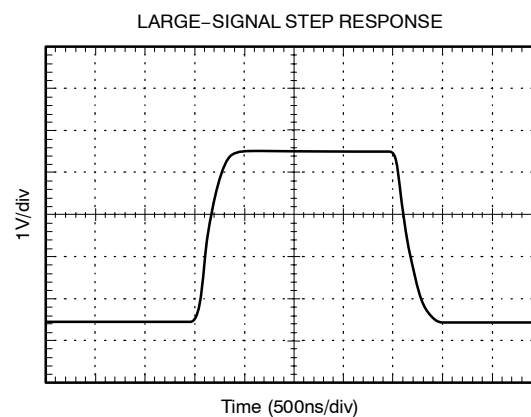
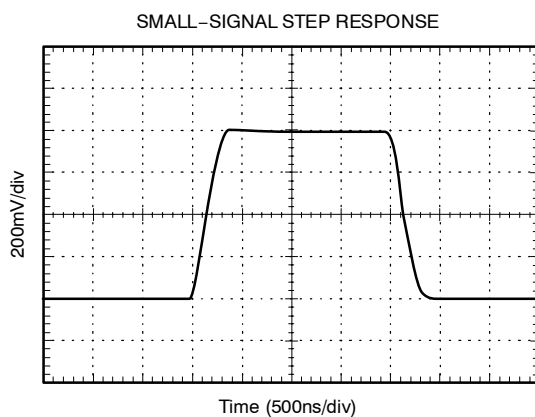
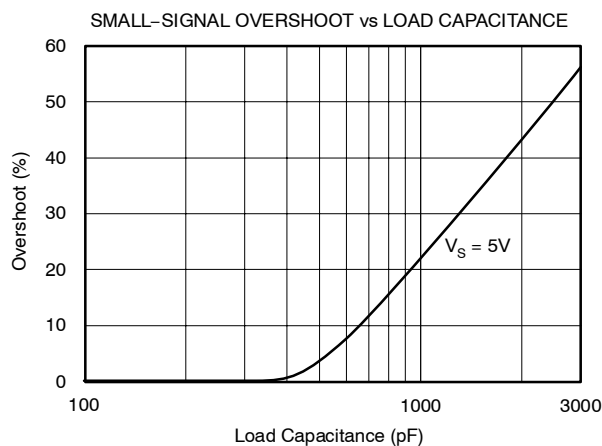
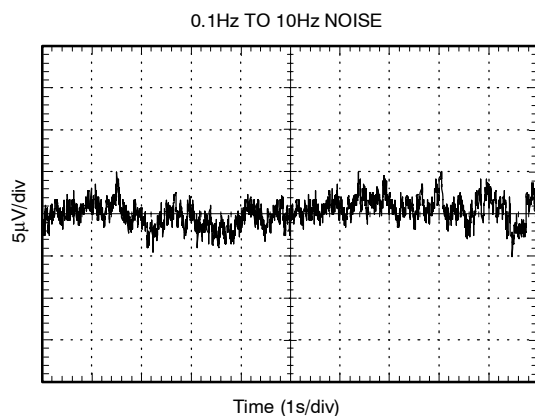
## TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , REF pin 1 connected to ground, and REF pin 2 connected to  $V_{\text{REF}} = 5\text{V}$ , unless otherwise noted.



## TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ , REF pin 1 connected to ground, and REF pin 2 connected to  $V_{\text{REF}} = 5\text{V}$ , unless otherwise noted.



## APPLICATION INFORMATION

The internal op amp of the INA159 has a rail-to-rail common-mode voltage capability at its inputs. A rail-to-rail op amp allows the use of  $\pm 10\text{V}$  inputs into a circuit biased to 1/2 of a 5V reference (2.5V quiescent output). The inputs to the op amp will swing from approximately 400mV to 3.75V in this application.

The unique input topology of the INA159 eliminates the input offset transition region typical of most rail-to-rail complementary stage operational amplifiers. This allows the INA159 to provide superior glitch- and transition-free performance over the entire common-mode range.

Good layout practice includes the use of a 0.1 $\mu\text{F}$  bypass capacitor placed closely across the supply pins.

### COMMON-MODE RANGE

The common-mode range of the INA159 is a function of supply voltage and reference. Where both pins, REF1 and REF2, are connected together:

$$V_{\text{CM}+} = (V+) + 5[(V+) - V_{\text{REF}}] \quad (1)$$

$$V_{\text{CM}-} = (V-) - 5[V_{\text{REF}} - (V-)] \quad (2)$$

Where one REF pin is connected to the reference, and the other pin grounded (1/2 reference connection):

$$V_{\text{CM}+} = (V+) + 5[(V+) - (0.5V_{\text{REF}})] \quad (3)$$

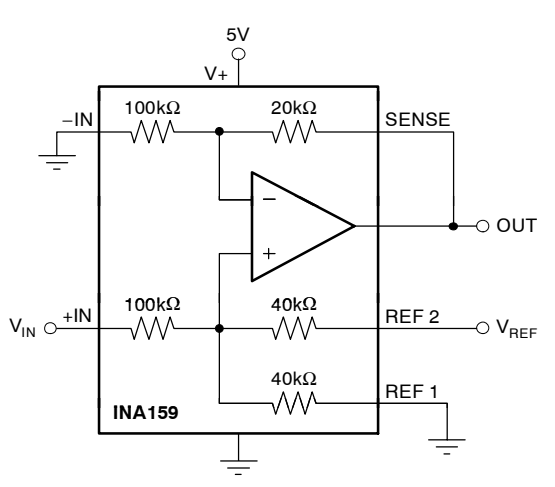
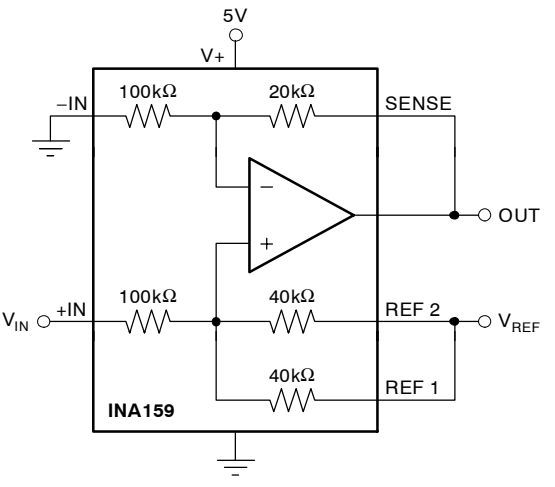
$$V_{\text{CM}-} = (V-) - 5[(0.5V_{\text{REF}}) - (V-)] \quad (4)$$

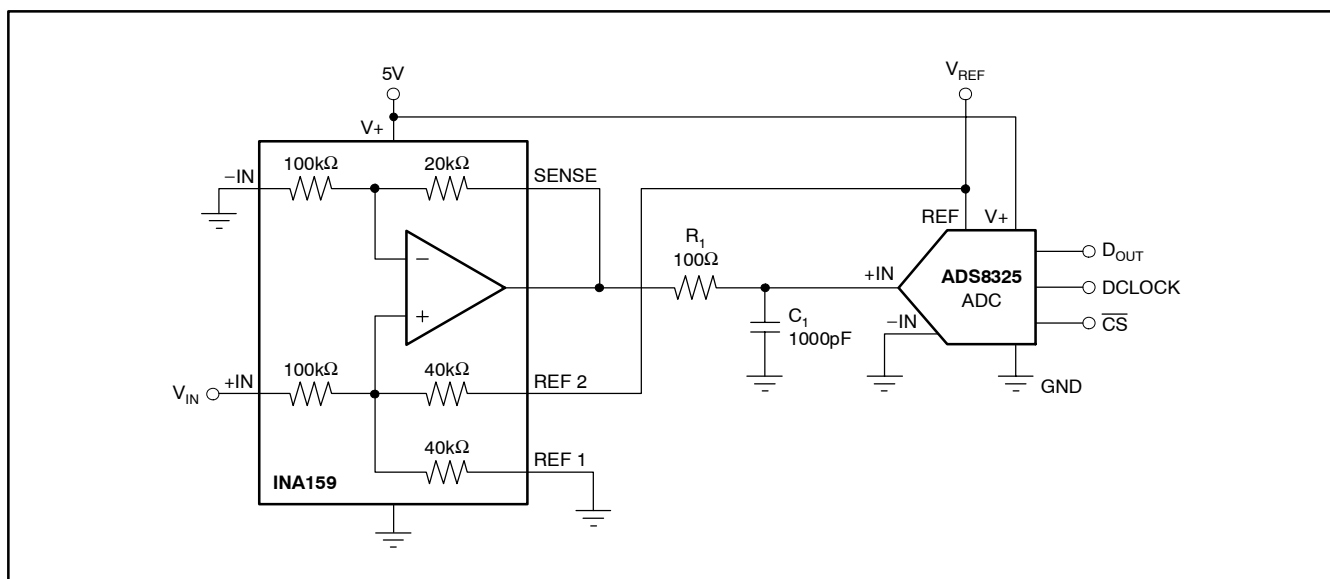
Some typical values are shown in Table 1.

**Table 1. Common-Mode Range For Various Supply and Reference Voltages**

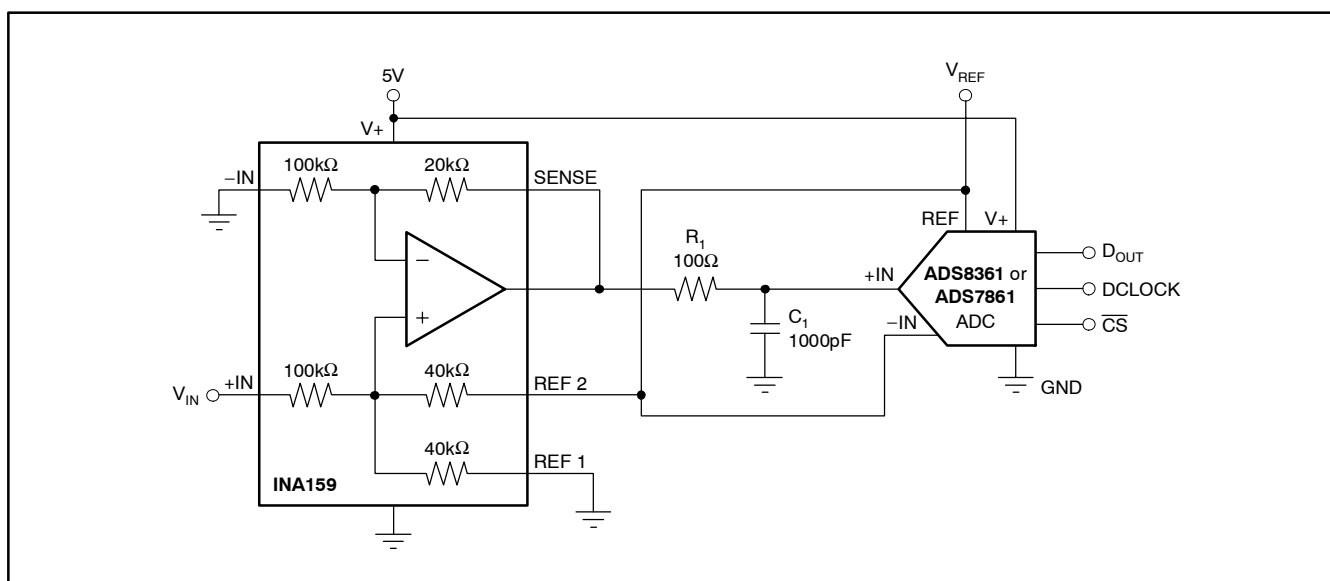
| REF 1 and REF 2 Connected Together |    |                  |                  |                  |
|------------------------------------|----|------------------|------------------|------------------|
| V+                                 | V- | V <sub>REF</sub> | V <sub>CM+</sub> | V <sub>CM-</sub> |
| 5                                  | 0  | 3                | 15               | -15              |
| 5                                  | 0  | 2.5              | 17.5             | -12.5            |
| 5                                  | 0  | 1.25             | 23.75            | -6.25            |
| 1/2 Reference Connection           |    |                  |                  |                  |
| V+                                 | V- | V <sub>REF</sub> | V <sub>CM+</sub> | V <sub>CM-</sub> |
| 5                                  | 0  | 5                | 17.5             | -12.5            |
| 5                                  | 0  | 4.096            | 19.76            | -10.24           |
| 5                                  | 0  | 2.5              | 23.75            | -6.25            |
| 3.3                                | 0  | 3.3              | 11.55            | -8.25            |
| 3.3                                | 0  | 2.5              | 13.55            | -6.25            |
| 3.3                                | 0  | 1.25             | 16.675           | -3.125           |

**Table 2. Input and Output Relationships for Various Reference and Connection Combinations**

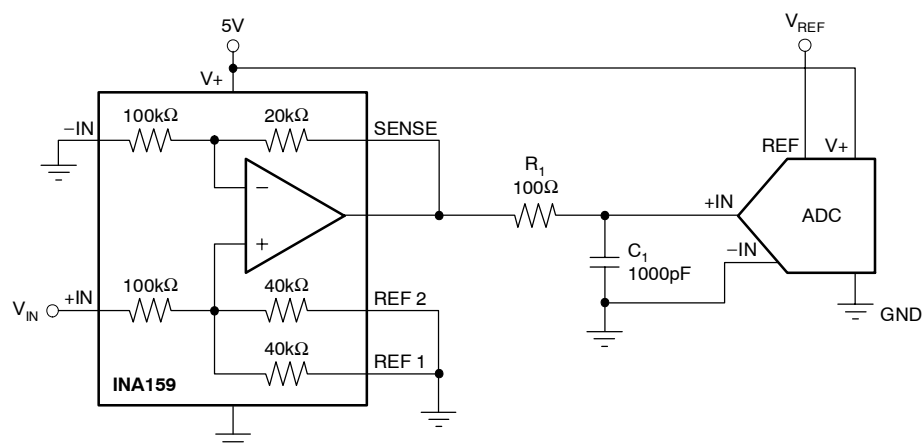
| $V_{REF}$<br>(V) | REF CONNECTION                                                                     | $V_{OUT}$ for $V_{IN} = 0$<br>(V) | LINEAR $V_{IN}$ RANGE<br>(V)       | USEFUL $V_{OUT}$ SWING<br>(V)         |
|------------------|------------------------------------------------------------------------------------|-----------------------------------|------------------------------------|---------------------------------------|
| 5                |   | 2.5                               | +10<br>0<br>-10                    | 4.5<br>( $\pm 2V$ swing)<br>0.5       |
| 4.096            |                                                                                    | 2.048                             | +10<br>0<br>-10                    | 4.048<br>( $\pm 2V$ swing)<br>0.048   |
| 3.3              |                                                                                    | 1.65                              | +10<br>0<br>-7.885                 | 3.65<br>(-1.577V, +2V swing)<br>0.048 |
| 2.5              |                                                                                    | 1.25                              | +10 (also +5)<br>0<br>-6 (also -5) | 3.25<br>(-1.2V, +2V swing)<br>0.048   |
| 1.8              |                                                                                    | 0.9                               | +10<br>0<br>-4.26                  | 2.9<br>(-0.852V, +2V swing)<br>0.048  |
| 2.5              |  | 2.5                               | +10<br>0<br>-10                    | 4.5<br>( $\pm 2V$ swing)<br>0.5       |
| 1.8              |                                                                                    | 1.8                               | +10<br>0<br>-8.76                  | 3.8<br>(-1.752V, +2V swing)<br>0.048  |
| 1.2              |                                                                                    | 1.2                               | +10<br>0<br>-5.76                  | 3.2<br>(-1.15V, +2V swing)<br>0.048   |



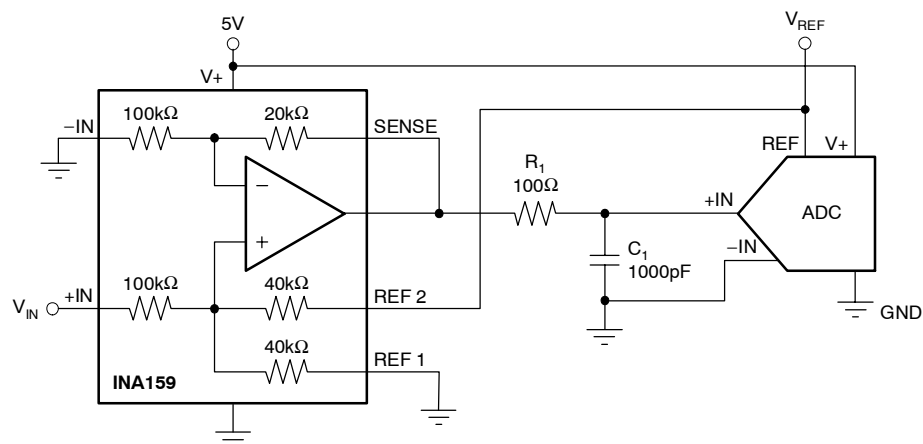
**Figure 3. Typical Application Circuit Interfacing to Medium-Speed, Single-Supply ADCs**



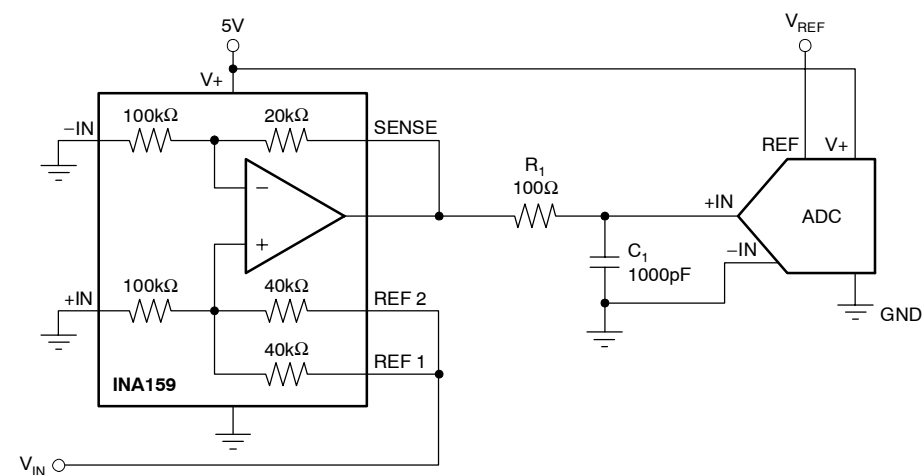
**Figure 4. Typical Application Circuit Interfacing to Medium-Speed, Single-Supply ADCs with Pseudo-Differential Inputs (such as the ADS7861 and ADS8361)**



a) Unipolar, Noninverting,  $G = 0.2$

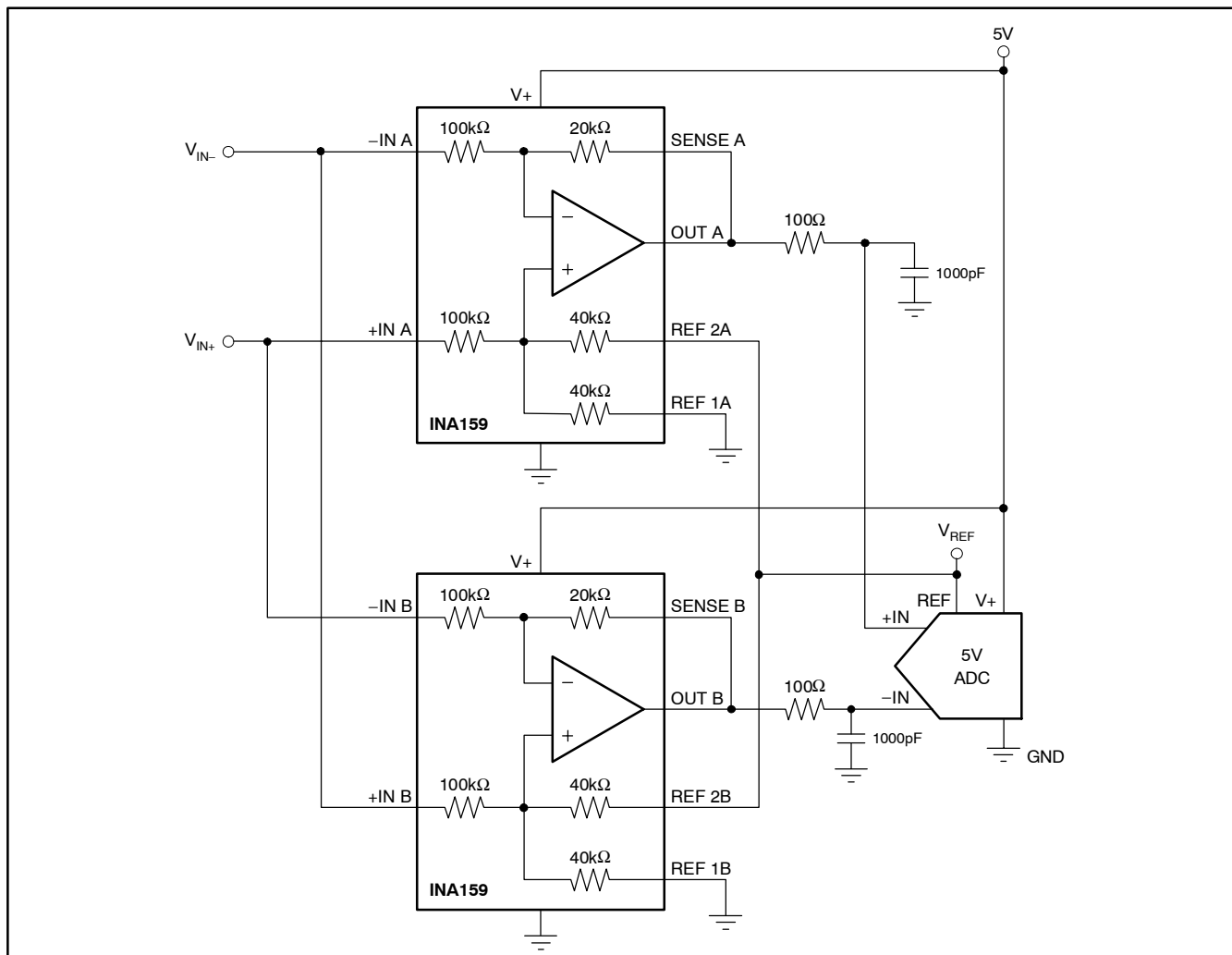


b) Bipolar, Noninverting,  $G = 0.2$



c) Unipolar, Unity Gain

**Figure 5. Basic INA159 Configurations**



**Figure 6. Differential ADC Drive**

## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">INA159AIDGKR</a> | Active        | Production           | VSSOP (DGK)   8 | 2500   LARGE T&R      | Yes         | Call TI   Nipdauag<br>  Nipdau       | Level-1-260C-UNLIM                | -40 to 125   | CJB                 |
| INA159AIDGKR.A               | Active        | Production           | VSSOP (DGK)   8 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | CJB                 |
| INA159AIDGKRG4               | Active        | Production           | VSSOP (DGK)   8 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | CJB                 |
| <a href="#">INA159AIDGKT</a> | Active        | Production           | VSSOP (DGK)   8 | 250   SMALL T&R       | Yes         | Call TI   Nipdauag<br>  Nipdau       | Level-1-260C-UNLIM                | -40 to 125   | CJB                 |
| INA159AIDGKT.A               | Active        | Production           | VSSOP (DGK)   8 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | CJB                 |
| INA159AIDGKTG4               | Active        | Production           | VSSOP (DGK)   8 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | CJB                 |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF INA159 :**

- Enhanced Product : [INA159-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| INA159AIDGKR | VSSOP        | DGK             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| INA159AIDGKT | VSSOP        | DGK             | 8    | 250  | 180.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |

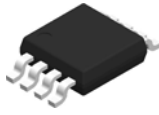
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| INA159AIDGKR | VSSOP        | DGK             | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| INA159AIDGKT | VSSOP        | DGK             | 8    | 250  | 213.0       | 191.0      | 35.0        |

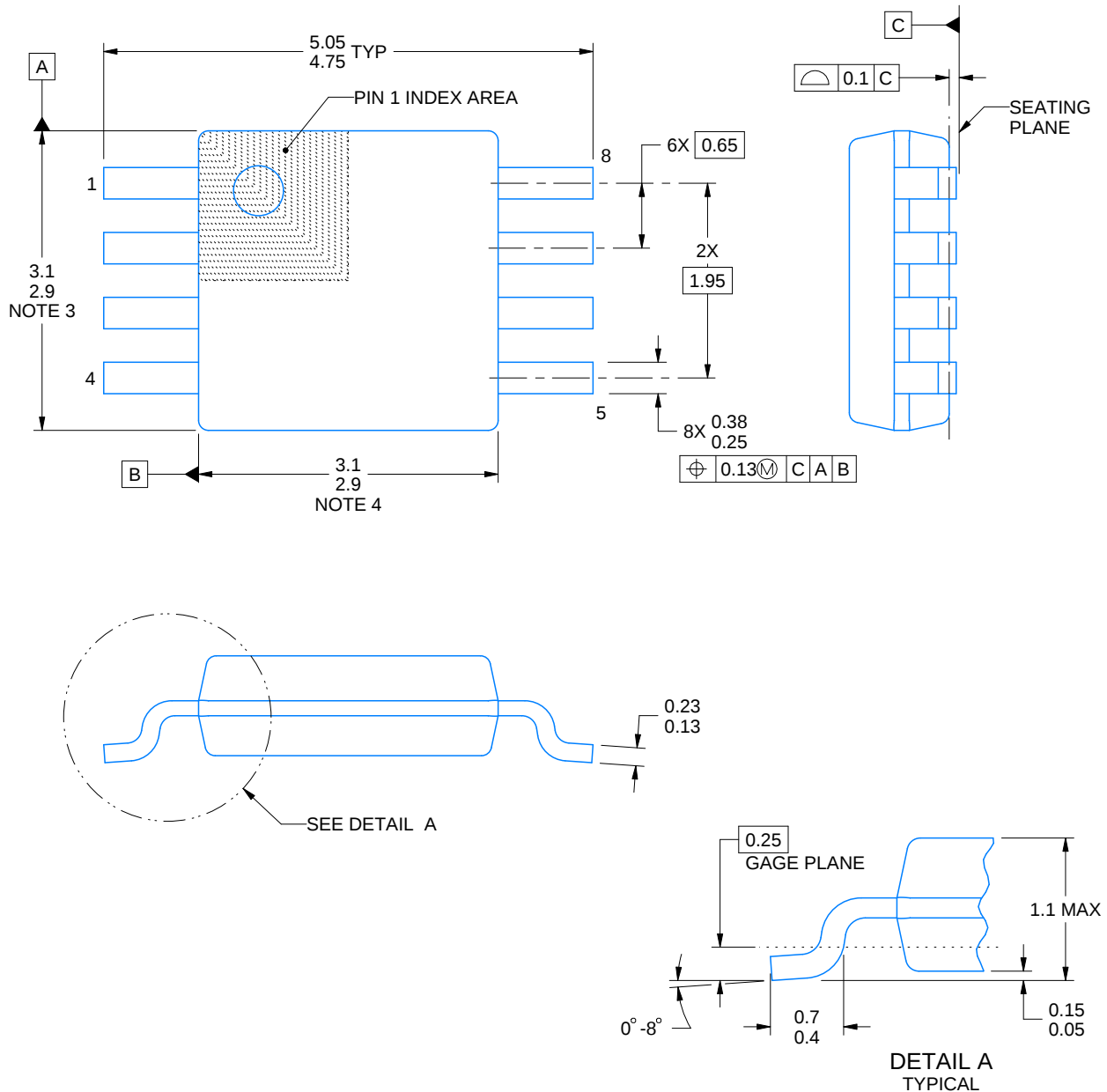
DGK0008A



# PACKAGE OUTLINE

## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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### NOTES:

PowerPAD is a trademark of Texas Instruments.

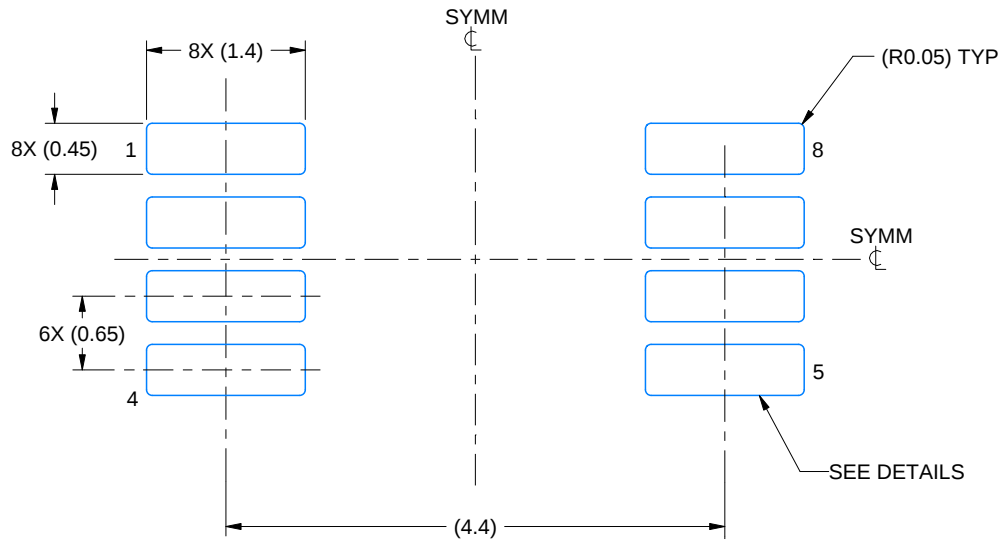
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

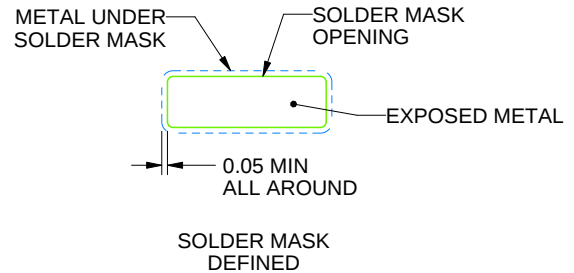
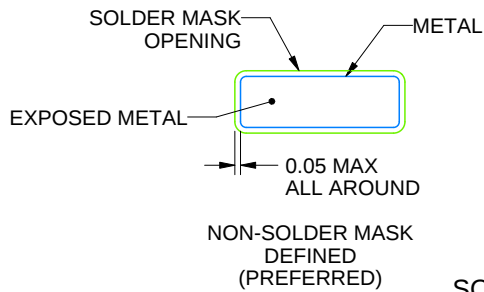
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™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

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NOTES: (continued)

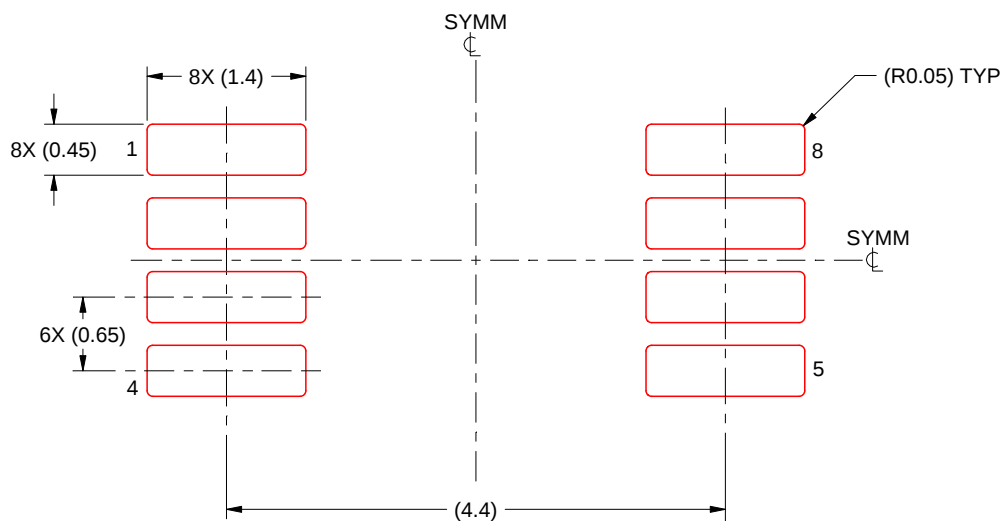
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

## EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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