







INA128, INA129 SBOS051F - OCTOBER 1995 - REVISED MAY 2022

INA12x Precision, Low-Power Instrumentation Amplifiers

1 Features

Low offset voltage: 50 µV, maximum

Low drift: 0.5 µV/°C, maximum

Low input bias current: 5 nA, maximum

Low noise: 8 nV/√Hz, 0.2 µVpp High CMR: 120 dB, minimum

Bandwidth: 1.3 MHz (G = 1)

Inputs protected to ±40 V

Wide supply range: ±2.25 V to ±18 V

Low quiescent current: 700 µA Packages: 8-pin plastic DIP, SO-8

2 Applications

Pressure transmitter

Temperature transmitter

Weigh scale

Electrocardiogram (ECG)

Analog input module

Data acquisition (DAQ)

3 Description

The INA128 and INA129 (INA12x) are low-power, general-purpose instrumentation amplifiers that offer excellent accuracy. The versatile three op amp design and small size make these amplifiers an excellent choice for a wide range of applications. Currentfeedback input circuitry provides wide bandwidth even at high gain (200 kHz at G = 100).

A single external resistor sets any gain from 1 to 10,000. The INA128 provides an industry-standard gain equation with a 50-k Ω resistor. The INA129 gain equation uses a 49.4-kΩ resistor to allow for drop-in replacements of comparable devices.

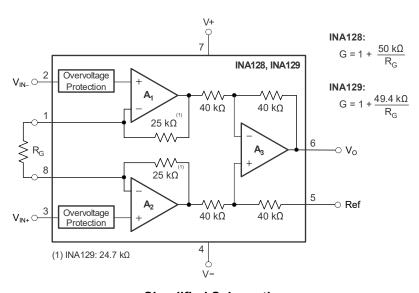
The INA12x are available in plastic DIP and surfacemount packages, specified for the -40°C to +85°C temperature range. The INA128 is also available in a dual configuration, the INA2128.

The upgraded INA828 offers a lower input bias current (0.6 nA, max) and lower noise (7 nV/ $\sqrt{\text{Hz}}$) at the same quiescent current. See the Device Comparison Table for a selection of precision instrumentation amplifiers from Texas Instruments.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
INA128,	SOIC (8)	3.91 mm × 4.90 mm
INA129	PDIP (8)	6.35 mm × 9.81 mm

For all available packages, see the package option addendum at the end of the data sheet.



Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

C	hanges from Revision E (April 2019) to Revision F (May 2022)	Page
•	Updated the numbering format for tables, figures, and cross-references throughout the document	1
•	Added bandwidth and noise specifications in Features	
•	Changed Applications to link to latest end-equipment solutions on ti.com	1
•	Changed reference from INA819 to INA818 in Device Comparison Table	4
•	Added single supply specification to Absolute Maximum Ratings	
•	Added note clarifying output short-circuit "to ground" in Absolute Maximum Ratings refers to short-circuit	it to
	V _S / 2	_
•	Added single supply specification to Recommended Operating Conditions	<mark>5</mark>
•	Changed input common-mode voltage range specification from V – 2 to (V–) + 2 in <i>Recommended Ope Conditions</i>	erating 5
•	Deleted INA128-HT and INA129-HT operating temperature specifications from Recommended Operating	• • • • • • • • • • • • • • • • • • • •
	Conditions	
•	Added specified temperature range to Recommended Operating Conditions	<mark>5</mark>
•	Added $V_{REF} = 0 \text{ V}$, $V_{CM} = V_S / 2$, and $G = 1 to "unless otherwise noted" conditions in Electrical$	
	Characteristics and Typical Characteristics for clarity	6
•	Changed test condition for offset voltage drift specification in <i>Electrical Characteristics</i> from " $T_A = T_{MIN}$ to T_{MAX} " to " $T_A = -40$ °C to +85°C" for clarity	6
•	Changed typical long-term stability specification from ±0.1±3/G µV/mo to ±0.2±3/G µV/mo in <i>Electrical</i>	
	Characteristics	6
•	Changed common-mode voltage specification from (V-) + 2 V minimum and (V+) - 2 V minimum acros	s two
	rows to (V-) + 2 V minimum and (V+) - 2 V maximum across one row in Electrical Characteristics	6
•	Deleted typical common-mode voltage specifications in Electrical Characteristics	
•	Added test condition of " $R_S = 0 \Omega$ " to safe input voltage specification in <i>Electrical Characteristics</i> for claim	rity6
•	Added test condition of " $T_A = -40$ °C to +85°C" to input bias current drift specification in <i>Electrical</i>	
	Characteristics for clarity	6
•	Added test condition of ${}^{"}T_{A} = -40$ °C to +85 °C" to input offset current drift specification in <i>Electrical</i>	
	Characteristics for clarity	6
•	Changed maximum gain error specification for INA128PA/UA and INA129PA/UA with G = 1 from ±0.019	%
	to ±0.1% in Electrical Characteristics	6

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•	Added test condition of " $T_A = -40$ °C to +85°C" for gain drift in <i>Electrical Characteristics</i> for clarity	
•	Changed parameter names from "Voltage - Positive" to "Positive output voltage swing" and from "Voltage	age -
	Negative" to "Negative output voltage swing" in Electrical Characteristics	<mark>6</mark>
•	Deleted typical positive and negative output voltage swing specifications in Electrical Characteristics	<mark>6</mark>
•	Added test condition of "Continuous to V _S / 2" to short-circuit current specification in Electrical Charact	
	for clarity	
•	Changed typical bandwidth specification for G = 10 from 700 kHz to 640 kHz in <i>Electrical Characterist</i> .	ics6
•	Changed typical slew rate specification from 4 V/µs to 1.2 V/µs in <i>Electrical Characteristics</i>	
	Changed typical settling time specification for $G = 1$, $G = 10$, and $G = 100$ from 7 μ s, 7 μ s, and	•
	9 μs respectively to 12 μs, 12 μs, and 12 μs, in <i>Electrical Characteristics</i>	6
	Deleted redundant voltage range, operating temperature range, and specification temperature range	
	specifications from <i>Electrical Characteristics</i>	6
	Changed Figures 7-1, 7-3, 7-4, 7-9, 7-10, 7-11, 7-16, 7-17, 7-20, 7-21	
	Changed values discussed in <i>Input Common-Mode Range</i> from typical input common-mode voltage range from typical input common-mode voltage range.	
	values to maximum and minimum values	
	Changed Figure 9-1 to fix missing text and include reference voltage	
	Added more detailed guidance concerning REF pin in <i>Design Requirements</i>	
	Changed Figures 9-6, 9-7	10
	Changed Figures 9-0, 9-7 Changed Figures 9-10 and 9-11 to fix missing text	
	Added Related Documentation links to Device and Documentation Support	
_	Added Related Documentation links to Device and Documentation Support	
Cł	hanges from Revision D (January 2018) to Revision E (April 2019)	Page
•	Added information about the newer, upgraded INA828	1
•	Added Device Comparison Table	
Cł	hanges from Revision C (October 2015) to Revision D (January 2018)	Page
•	Added top navigator icon for TI Reference Design	
	Changed "±0.5±0/G" to "±0.5±20/G" in MAX column of Offset voltage RTI vs temperature row of <i>Electi</i>	
	Characteristics	
CI	hanges from Revision B (February 2005) to Revision C (April 2015)	Page
	Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and	- i age
•	Implementation section, Power Supply Recommendations section, Layout section, Device and	
		4
	Documentation Support section, and Mechanical, Packaging, and Orderable Information section	

5 Device Comparison Table

DEVICE	DESCRIPTION	GAIN EQUATION	RG PINS AT PIN
INA818	35-µV offset, 0.4-µV/°C V _{OS} drift, 8-nV/√Hz noise, low-power, precision instrumentation amplifier	G = 1 + 50 kΩ / RG	1, 8
INA821	35-μV offset, 0.4-μV/°C V _{OS} drift, 7-nV/ $\sqrt{\text{Hz}}$ noise, high-bandwidth, precision instrumentation amplifier	G = 1 + 49.4 kΩ / RG	2, 3
INA828	50-μV offset, 0.5-μV/°C V _{OS} drift, 7-nV/√Hz noise, low-power, precision instrumentation amplifier	G = 1 + 50 kΩ / RG	1, 8
INA333	25-μV V_{OS} , 0.1-μV/°C V_{OS} drift, 1.8-V to 5-V, RRO, 50-μA I_{Q} , chopper-stabilized INA	G = 1 + 100 kΩ / RG	1, 8
PGA280	20-mV to ±10-V programmable gain IA with 3-V or 5-V differential output; analog supply up to ±18 V	Digital programmable	N/A
INA159	G = 0.2 V differential amplifier for ±10-V to 3-V and 5-V conversion	G = 0.2 V/V	N/A
PGA112	Precision programmable gain op amp with SPI	Digital programmable	N/A

6 Pin Configuration and Functions

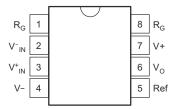


Figure 6-1. D (8-Pin SOIC) and P (8-Pin PDIP) Packages, Top View

Table 6-1. Pin Functions

PIN		TYPE	DESCRIPTION		
NAME	NO.	ITPE	DESCRIPTION		
REF	5	Input	Reference input. This pin must be driven by low impedance or connected to ground.		
R _G	1,8	_	Gain setting pin. For gains greater than 1, place a gain resistor between pin 1 and pin 8.		
V-	4	Power	Negative supply		
V+	7	Power	Positive supply		
V _{IN} _	2	Input	Negative input		
V _{IN+}	3	Input	Positive input		
Vo	6	Output	Output		

Product Folder Links: INA128 INA129



7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V	Supply voltage	Dual supply, $V_S = (V+) - (V-)$		±18	V
Vs	Supply voltage	Single supply, $V_S = (V+) - 0 V$		36	V
	Analog input voltage			±40	V
	Output short-circuit ⁽²⁾		Continuous		
T _A	Operating temperature	;	-40	125	°C
	Junction temperature			150	°C
	Lead temperature (sol	dering, 10 s)		300	°C
T _{stg}	Storage temperature		-55	125	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
V	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾		V
V _(ESD)	Liectrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±50	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	<u> </u>	,				
			MIN	TYP	MAX	UNIT
V _S Supply voltage	Single-supply	4.5	30	36		
	Supply voltage	Dual-supply	±2.25	±15	±18	v
	Input common-mode voltage range for V _O = 0 V		(V-) + 2		(V+) – 2	V
T _A	Specified temperature		-40		85	°C

7.4 Thermal Information

		INA		
	THERMAL METRIC ⁽¹⁾	D (SOIC)	P (PDIP)	UNIT
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110	46.1	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	57	34.1	°C/W
R _{0JB}	Junction-to-board thermal resistance	54	23.4	°C/W
ΨЈТ	Junction-to-top characterization parameter	11	11.3	°C/W
ΨЈВ	Junction-to-board characterization parameter	53	23.2	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

⁽²⁾ Short-circuit to V_S / 2.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



7.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 k Ω , V_{REF} = 0 V, V_{CM} = V_S / 2, and G = 1 (unless otherwise noted)

	PARAMETER	TES	T CONDITI	ONS	MIN	TYP	MAX	UNIT	
INPUT									
.,	05 1 1 (DTI)	4 . 0 . 40000	INA12xP, I	NA12xU		±10 ±100 / G	±50 ±500 / G	.,	
V _{OS}	Offset voltage (RTI)	1 ≤ G ≤ 10000	INA12xPA	, INA12xUA		±25 ±100 / G	±125 ±1000 / G	μV	
	05 1 1 15 (DT)	T 4000 4 0500	INA12xP, I	NA12xU		±0.2 ±2 / G	±0.5 ±20 / G		
	Offset voltage drift (RTI)	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	INA12xPA	, INA12xUA		±0.2 ±5 / G	±1 ±20 / G	μV/°C	
DODD	Power-supply rejection	V .0.05.V/ .40.V/	INA12xP, I	NA12xU		±0.2 ±20 / G	±1 ±100 / G		
PSRR	ratio (RTI)	$V_S = \pm 2.25 \text{ V to } \pm 18 \text{ V}$	INA12xPA	, INA12xUA			±2 ±200 / G	μV/V	
	Long-term stability		'			±0.2 ±3 / G		μV/mo	
	I	Differential				10 2		00 11 5	
	Input impedance	Common-mode				100 9		GΩ pF	
V _{CM}	Common-mode voltage ⁽²⁾	V _O = 0 V			(V-) + 2		(V+) – 2	V	
	Safe input voltage	R _S = 0 Ω					±40	V	
	Common-mode rejection ratio			0 - 1	INA12xP, INA12xU	80	86	86	
		mon-mode rejection $\Delta R_{S} = 1 \text{ k}\Omega, \text{ V}_{CM} = \pm 13 \text{ V}$	G = 1	INA12xPA, INA12xUA	73			dB	
			G = 10	INA12xP, INA12xU	100	106			
OMBB				INA12xPA, INA12xUA	93				
CMRR			G = 100	INA12xP, INA12xU	120	125			
				INA12xPA, INA12xUA	110				
			G = 1000	INA12xP, INA12xU	120	130			
			0 - 1000	INA12xPA, INA12xUA	110				
INPUT E	BIAS CURRENT								
I_	Input bias current	INA12xP, INA12xU				±2	±5	nA	
l _Β	input bias current	INA12xPA, INA12xUA					±10	IIA	
	Input bias current drift	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$				±30		pA/°C	
Ios	Input offset current	INA12xP, INA12xU				±1	±5	nA	
108	input onset current	INA12xPA, INA12xUA					±10	nA	
	Input offset current drift	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$				±30		pA/°C	
NOISE									
			f = 10 Hz			10			
e _N	Voltage noise (RTI)	G = 1000, R _S = 0 Ω	f = 100 Hz	f = 100 Hz		8		nV/√ Hz	
ON.	voltage Holse (KTI)	G = 1000, NS = 0 12	f = 1 kHz			8			
			f _B = 0.1 Hz	z to 10 Hz		0.2		μV _{PP}	
		f = 10 Hz				0.9		pA/√ Hz	
In	Current noise	f = 1 kHz				0.3		P. 4 11 12	
		f _B = 0.1 Hz to 10 Hz				30		pA _{PP}	

Product Folder Links: INA128 INA129

7.5 Electrical Characteristics (continued)

at $T_A = 25^{\circ}$ C, $V_S = \pm 15$ V, $R_L = 10$ k Ω , $V_{REF} = 0$ V, $V_{CM} = V_S / 2$, and G = 1 (unless otherwise noted)

	PARAMETER	Т	EST CONDITIONS	MIN	TYP	MAX	UNIT	
Gain equation NA128								
	Cain a suretian	INA128		1	+ (50 kΩ / R _G)		1/0/	
	Gain equation	INA129		1 +	+ (49.4 kΩ / R _G)		0/0	
G	Gain			1		10000	V/V	
		0 4	INA12xP, INA12xU		±0.01	±0.024		
		G = 1	INA12xPA, INA12xUA			±0.1		
		0 - 40	INA12xP, INA12xU		±0.02	±0.4		
С Г	Cain arrar	G = 10	INA12xPA, INA12xUA			±0.5	0/	
GE	Gain end	0 - 100	INA12xP, INA12xU		±0.05	±0.5	70	
		G = 100	INA12xPA, INA12xUA			±0.7		
		0 - 4000	INA12xP, INA12xU		±0.5	±1		
		G = 1000	INA12xPA, INA12xUA			±2		
	O - i i i	T - 40°C t- 105°C			±1	±10	/00	
	Gain drift(4)	$I_A = -40^{\circ} \text{C to } +85^{\circ} \text{C}$	50-kΩ or 49.4-kΩ resistance ⁽³⁾		±25	±100	ppm/°C	
		0 4 1/4 140 0 1/4	INA12xP, INA12xU		±0.0001	±0.001		
		$G = 1, V_0 = \pm 13.6 \text{ V}$	INA12xPA, INA12xUA			±0.002		
		0 10	INA12xP, INA12xU		±0.0003	±0.002		
	Gain nonlinearity ⁽¹⁾	G = 10	INA12xPA, INA12xUA			±0.004	% of FSF	
		0 100	INA12xP, INA12xU		±0.0005	±0.002		
		G = 100	INA12xPA, INA12xUA			±0.004		
		G = 1000	'		±0.001			
OUTP	UT			<u> </u>				
				(V+) – 1.4			V	
				(V-) + 1.4			V	
C _L	Load capacitance	Stable operation			1000		pF	
I _{sc}	Short-circuit current	Continuous to V _S / 2			+6/–15		mA	
FREQ	UENCY RESPONSE	•						
		G = 1			1.3		MHz	
BW	Pandwidth 2 dP	G = 10			640			
DVV	Bandwidth, –3 dB	G = 100			200		kHz	
		G = 1000			20			
SR	Slew rate	G = 5, V _O = ±10 V			1.2		V/µs	
			G = 1		12			
	Cattling time	To 0.040/	G = 10		12			
t _S	Settling time	To 0.01%	G = 100		12		μs	
			G = 1000		80		1	
	Overload recovery	50% input overload			4		μs	
POWE	R SUPPLY	•						
ΙQ	Quiescent current	V _{IN} = 0 V			±700	±750	μΑ	

⁽¹⁾ (2) Nonlinearity measurements in G = 1000 are dominated by noise. Typical nonlinearity is $\pm 0.001\%$

Input common-mode voltage varies with output voltage; see Typical Characteristics.

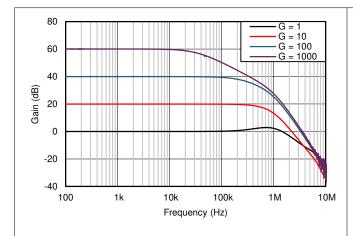
⁽³⁾ Temperature coefficient of the 50-k $\!\Omega$ or 49.4-k $\!\Omega$ term in the gain equation.

Specified by wafer test.



7.6 Typical Characteristics

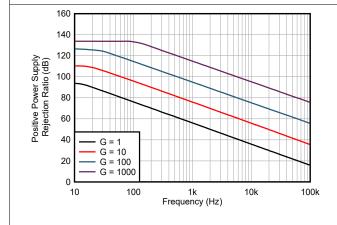
at $T_A = 25$ °C, $V_S = \pm 15$ V, $R_L = 10$ k Ω , $V_{REF} = 0$ V, $V_{CM} = V_S / 2$, and G = 1 (unless otherwise noted)



G = 1000V/V 120 Common-Mode Rejection (dB) 100 80 60 40 20 0 10 100 10k 100k 1M 1k Frequency (Hz)

Figure 7-1. Gain vs Frequency

Figure 7-2. Common-Mode Rejection vs Frequency



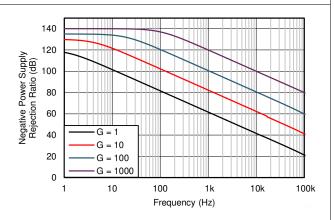
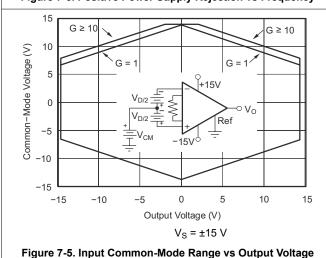


Figure 7-3. Positive Power Supply Rejection vs Frequency

Figure 7-4. Negative Power Supply Rejection vs Frequency



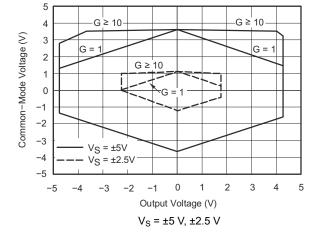
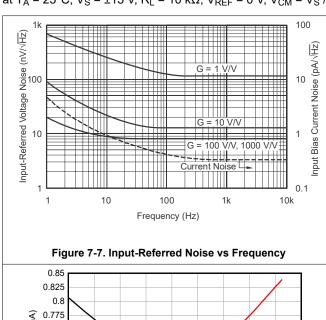


Figure 7-6. Input Common-Mode Range vs Output Voltage



7.6 Typical Characteristics (continued)

at $T_A = 25$ °C, $V_S = \pm 15$ V, $R_L = 10$ k Ω , $V_{REF} = 0$ V, $V_{CM} = V_S / 2$, and G = 1 (unless otherwise noted)



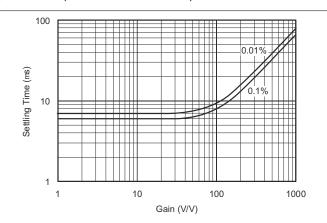
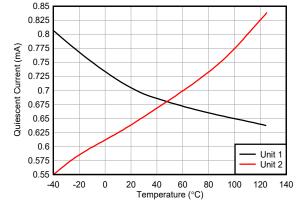


Figure 7-8. Settling Time vs Gain



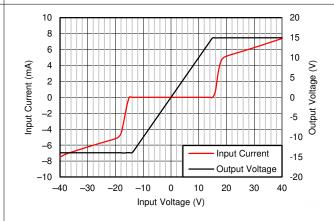
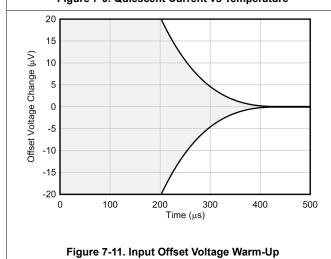


Figure 7-9. Quiescent Current vs Temperature

Figure 7-10. Input Overvoltage V/I Characteristics



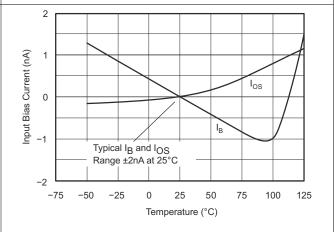
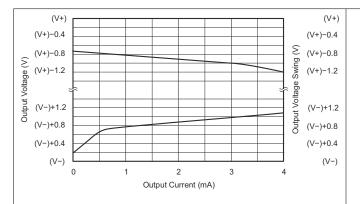


Figure 7-12. Input Bias Current vs Temperature



7.6 Typical Characteristics (continued)

at $T_A = 25$ °C, $V_S = \pm 15$ V, $R_L = 10$ k Ω , $V_{REF} = 0$ V, $V_{CM} = V_S / 2$, and G = 1 (unless otherwise noted)



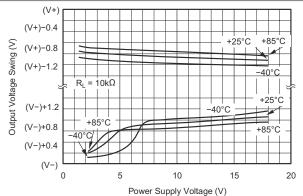
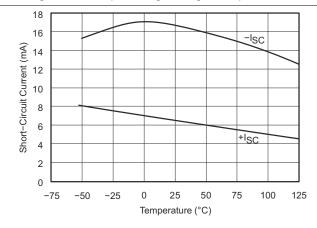


Figure 7-13. Output Voltage Swing vs Output Current

Figure 7-14. Output Voltage Swing vs Power Supply Voltage



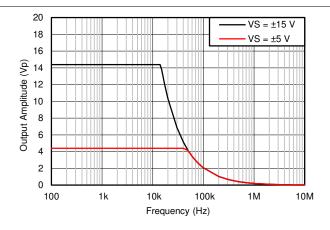
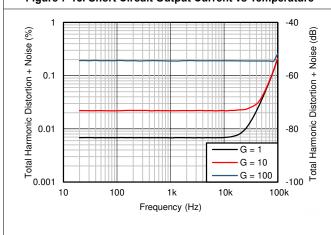


Figure 7-15. Short Circuit Output Current vs Temperature

Figure 7-16. Maximum Output Voltage vs Frequency



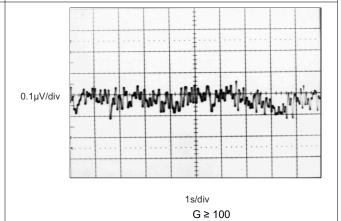


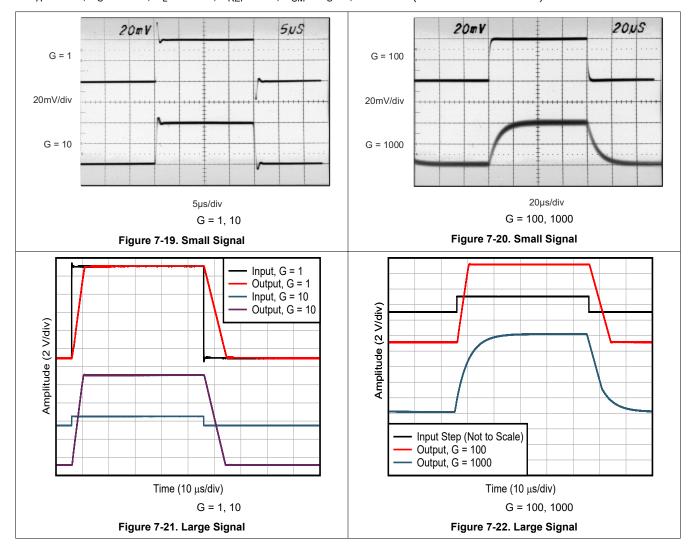
Figure 7-17. Total Harmonic Distortion + Noise vs Frequency

Figure 7-18. 0.1 to 10-Hz Input-Referred Voltage Noise



7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 k Ω , V_{REF} = 0 V, V_{CM} = V_S / 2, and G = 1 (unless otherwise noted)

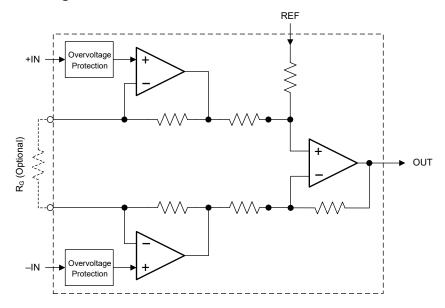


8 Detailed Description

8.1 Overview

The INA128 and INA129 (INA12x) instrumentation amplifiers are outfitted with an input protection circuit and input buffer amplifiers. These features eliminate the need for input impedance matching and make the amplifier an excellent choice for use in measurement and test equipment. Additional characteristics of the INA12x include a very-low dc offset, low drift, low noise, very-high open-loop gain, very-high common-mode rejection ratio, and very-high input impedances. The INA12x is used where great accuracy and stability of the circuit, both short and long term, are required.

8.2 Functional Block Diagram





8.3 Feature Description

The INA12x are low power, general-purpose instrumentation amplifiers offering excellent accuracy. The versatile three-op-amp design and small size make the amplifiers an excellent choice for a wide range of applications. Current-feedback input circuitry provides wide bandwidth, even at high gain. A single external resistor sets any gain from 1 to 10,000. The INA12x are laser trimmed for very low offset voltage (25 μ V typical) and high common-mode rejection (93 dB at G \geq 100). These devices operate with power supplies as low as ± 2.25 V, and a quiescent current of 2 mA, typically. The internal input protection can withstand up to ± 40 V without damage, as shown in Figure 7-10.

8.3.1 Noise Performance

The INA12x provide very low noise in most applications. Low-frequency noise is approximately 0.2 μ V_{PP} measured from 0.1 to 10 Hz (G \geq 100). This feature provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.

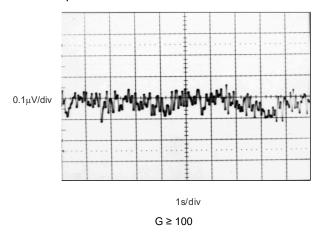


Figure 8-1. 0.1-Hz to 10-Hz Input-Referred Voltage Noise

8.4 Device Functional Modes

The INA12x have a single functional mode and operate when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power-supply voltage for the INA12x is 36 V (±18 V).

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The INA12x measure a small differential voltage with a high common-mode voltage developed between the noninverting and inverting input. The high input-voltage protection circuit in conjunction with high input impedance make the INA12x an excellent choice for a wide range of applications. The ability to set the reference pin to adjust the functionality of the output signal offers additional flexibility that is practical for multiple configurations.

9.1.1 Input Common-Mode Range

The linear input voltage range of the INA12x input circuitry ranges from approximately 2 V less than the positive supply voltage to 2 V greater than the negative supply. A differential input voltage causes the output voltage to increase; however, the linear input range is limited by the output voltage swing of amplifiers A_1 and A_2 . Thus, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on the supply voltage (see Figure 7-6).

Input overload can produce an output voltage that appears normal. For example, if an input-overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier is near zero. The output of A₃ is near 0 V even though both inputs are overloaded.

Product Folder Links: INA128 INA129

9.2 Typical Application

Figure 9-1 shows the basic connections required for operation of the INA12x. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown. The output is referred to the output reference (REF) pin, which is normally grounded. This connection must be low-impedance to provide good common-mode rejection. A resistance of 8 Ω in series with the REF pin causes a typical device to degrade to approximately 80 dB CMR (G = 1).

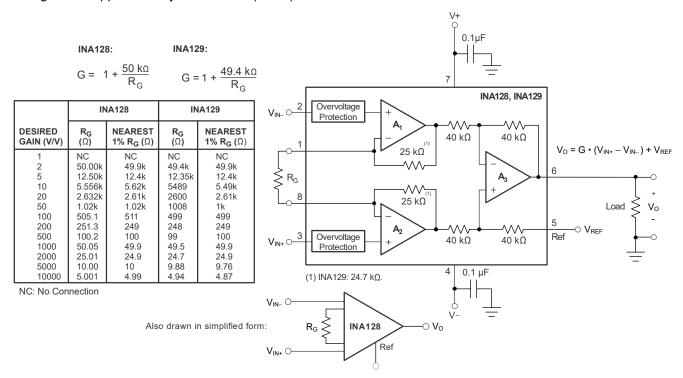


Figure 9-1. Basic Connections

9.2.1 Design Requirements

The devices are configured to monitor the input differential voltage when the input signal gain is set by the external resistor, R_G . The output signal is developed with respect to the voltage on the reference pin, REF. The most common application is where the output is referenced to ground when no input signal is present by connecting the REF pin to ground, as Figure 9-1 shows. In single-supply operation, offsetting the output signal to a precise midsupply level is useful (for example, 2.5 V in a 5-V supply environment). To accomplish this level shift, a voltage source must be connected to the REF pin to level shift the output so that the device can drive a single-supply ADC.

Voltage reference devices are an excellent option for providing a low-impedance voltage source for the reference pin. However, if a resistor voltage divider is used to generate a reference voltage, the voltage must be buffered by an op amp to avoid CMRR degradation.

9.2.2 Detailed Design Procedure

9.2.2.1 Setting the Gain

The gain (G) is set by connecting a single external resistor, R_G, between pins 1 and 8:

INA128:
$$G = 1 + 50 k\Omega / R_G$$
 (1)

INA129:
$$G = 1 + 49.4 \text{ k}\Omega / R_G$$
 (2)

Commonly used gains and resistor values are shown in Figure 9-1.

The 50-k Ω term in Equation 1 and the 49.4-k Ω term in Equation 2 come from the sum of the two internal feedback resistors of A₁ and A₂. These on-chip metal film resistors are laser trimmed to accurate, absolute values. The accuracy and temperature coefficient of these internal resistors are included in the gain accuracy and drift specifications in the *Electrical Characteristics* table.

The stability and temperature drift of the external gain setting resistor, R_G , also affects gain. The contribution of R_G to gain accuracy and drift can be directly inferred from Equation 1 and Equation 2. Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance, which contributes additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

9.2.2.2 Dynamic Performance

The typical performance curve in Figure 7-1 shows that despite low quiescent current, the INA12x achieve wide bandwidth even at high gain. This performance is due to the current-feedback topology of the input stage circuitry. Settling time also remains excellent at high gain.

9.2.2.3 Offset Trimming

The INA12x is laser trimmed for low-offset voltage and low offset voltage drift. Most applications require no external offset adjustment. Figure 9-2 shows an optional circuit for trimming the output offset voltage. The voltage applied to the REF pin is summed with the output. The op-amp buffer provides low impedance at the REF pin to preserve good common-mode rejection.

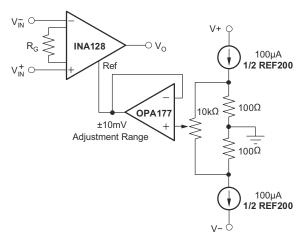


Figure 9-2. Optional Trimming of Output Offset Voltage



9.2.2.4 Input Bias Current Return Path

The input impedance of the INA12x is extremely high: approximately 10 G Ω . However, a path must be provided for the input bias current of both inputs. This input bias current is approximately ± 2 nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 9-3 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range, and the input amplifiers saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 9-3). With higher source impedance, use two equal resistors to provide a balanced input, with possible advantages of lower input offset voltage due to bias current, and better high-frequency common-mode rejection.

For more details about why a valid input bias current return path is necessary, see the *Importance of Input Bias Current Return Paths in Instrumentation Amplifier Applications* application note.

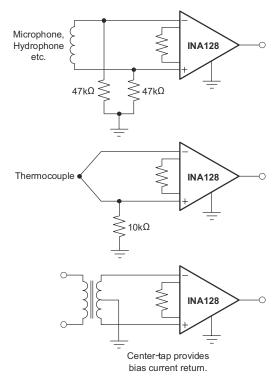
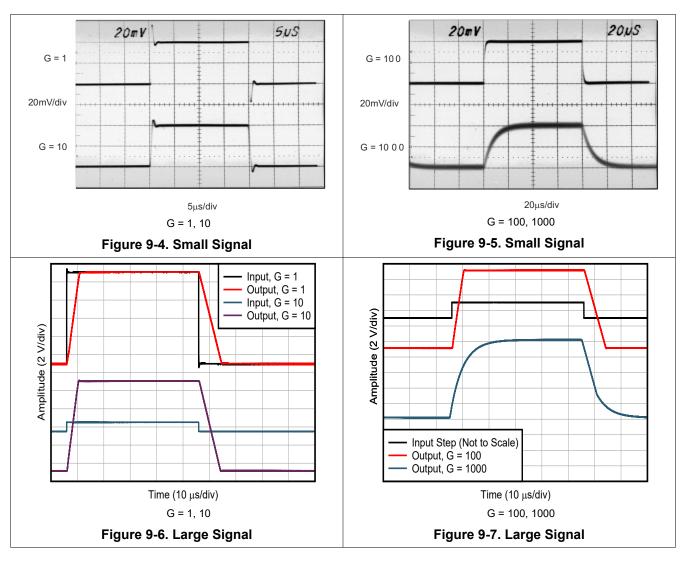


Figure 9-3. Providing an Input Common-Mode Current Path



9.2.3 Application Curves





9.3 System Examples

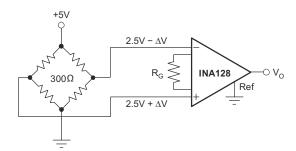


Figure 9-8. Bridge Amplifier

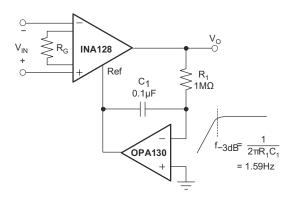
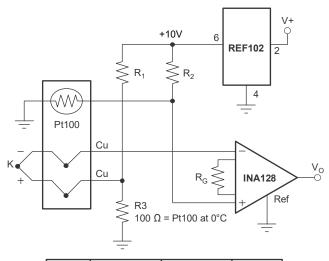


Figure 9-9. AC-Coupled Instrumentation Amplifier



ISA TYPE	MATERIAL	SEEBECK COEFICIENT (µV/°C)	R1, R2
E	+ Chromel - Constantan	58.5	66.5 kΩ
J	+ Iron - Constantan	50.2	76.8 kΩ
K	+ Chromel - Alumel	39.4	97.6 kΩ
Т	+ Copper - Constantan	38.0	102 kΩ

Figure 9-10. Thermocouple Amplifier With RTD Cold-Junction Compensation



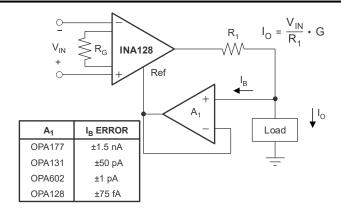


Figure 9-11. Differential Voltage to Current Converter

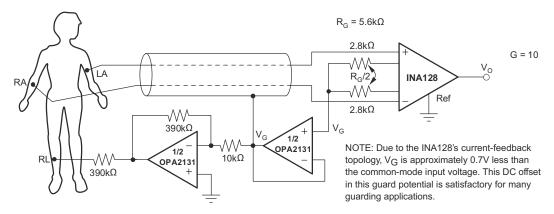


Figure 9-12. ECG Amplifier With Right-Leg Drive



10 Power Supply Recommendations

The minimum power supply voltage for INA12x is ± 2.25 V and the maximum power supply voltage is ± 18 V. This minimum and maximum range covers a wide range of power supplies; but for optimum performance, ± 15 V is recommended. Add a bypass capacitor at the input to compensate for the layout and power supply source impedance.

10.1 Low-Voltage Operation

The INA12x operate on power supplies as low as ±2.25 V. Performance remains excellent with power supplies ranging from ±2.25 V to ±18 V. Most parameters vary only slightly throughout this supply voltage range; see Section 7.6.

Operation at very-low supply voltages requires careful attention to make sure that the input voltages remain within the linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power-supply voltage. Figure 7-6 shows the range of linear operation for ±15-V, ±5-V, and ±2.5-V supplies.

11 Layout

11.1 Layout Guidelines

Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is $0.1~\mu F$ to $1~\mu F$. If necessary, add more decoupling capacitance to compensate for noisy or high-impedance power supplies. These decoupling capacitors must be placed between the power supply and INA12x devices.

The gain resistor must be placed close to pin 1 and pin 8. This placement limits the layout loop and minimizes any noise coupling into the devices.

11.2 Layout Example

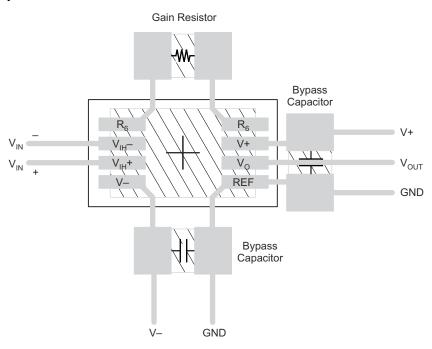


Figure 11-1. Recommended Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

12.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TITM software folder.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- · Texas Instruments, Comprehensive Error Calculation for Instrumentation Amplifiers application note
- Texas Instruments, Importance of Input Bias Current Return Paths in Instrumentation Amplifier Applications application note

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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PSpice® is a registered trademark of Cadence Design Systems. Inc.

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12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
INA128P	Active	Production	PDIP (P) 8	50 TUBE	-	Call TI	N/A for Pkg Type	-	INA128P
INA128P.A	Active	Production	PDIP (P) 8	50 TUBE	-	Call TI	N/A for Pkg Type	-40 to 125	INA128P
INA128PA	Active	Production	PDIP (P) 8	50 TUBE	-	Call TI	N/A for Pkg Type	-	INA128P A
INA128PA.A	Active	Production	PDIP (P) 8	50 TUBE	-	Call TI	N/A for Pkg Type	-40 to 125	INA128P A
INA128PG4	Active	Production	PDIP (P) 8	50 TUBE	-	Call TI	N/A for Pkg Type	See INA128P	INA128P
INA128U	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI Nipdau	Level-2-260C-1 YEAR	-	INA 128U
INA128U.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA 128U
INA128U/2K5	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	Call TI Nipdau	Level-3-260C-168 HR	-	INA 128U
INA128U/2K5.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 125	INA 128U
INA128U/2K51G4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	Call TI Nipdau	Level-3-260C-168 HR	-40 to 125	INA 128U
INA128U/2K51G4.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 125	INA 128U
INA128U/2K5G4	Active	Production	SOIC (D) 8	2500 LARGE T&R	-	Call TI	Call TI	See INA128U/2K5	
INA128UA	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 128U A
INA128UA.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 128U A
INA128UA/2K5	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	Call TI Nipdau	Level-3-260C-168 HR	-40 to 125	INA 128U A
INA128UA/2K5.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 128U A
INA128UA/2K5G4	Active	Production	SOIC (D) 8	2500 LARGE T&R	-	Call TI	Call TI	-40 to 125	





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Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
INA128UAG4	Active	Production	SOIC (D) 8	75 TUBE	-	Call TI	Call TI	-40 to 125	
INA129P	Active	Production	PDIP (P) 8	50 TUBE	Yes	Call TI	N/A for Pkg Type	-	INA129P
INA129P.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	Call TI	N/A for Pkg Type	-40 to 125	INA129P
INA129PA	Active	Production	PDIP (P) 8	50 TUBE	Yes	Call TI	N/A for Pkg Type	-	INA129P A
INA129PA.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	Call TI	N/A for Pkg Type	-40 to 125	INA129P A
INA129U	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI Nipdau	Level-3-260C-168 HR	-	INA 129U S
INA129U.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 125	INA 129U S
INA129U/2K5	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	Call TI Nipdau	Level-3-260C-168 HR	-	INA 129U S
INA129U/2K5.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 125	INA 129U S
INA129U/2K5G4	Active	Production	SOIC (D) 8	2500 LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA 129U S
INA129U/2K5G4.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA 129U S
INA129UA	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 129U A
INA129UA.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 129U A
INA129UA/2K5	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 129U A

PACKAGE OPTION ADDENDUM

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Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
INA129UA/2K5.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 129U A

⁽¹⁾ Status: For more details on status, see our product life cycle.

- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA128, INA129:

■ Enhanced Product : INA129-EP

NOTE: Qualified Version Definitions:

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

PACKAGE OPTION ADDENDUM

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• Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA128U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA128U/2K51G4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA128UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA129U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA129U/2K5G4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA129UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA128U/2K5	SOIC	D	8	2500	353.0	353.0	32.0
INA128U/2K51G4	SOIC	D	8	2500	353.0	353.0	32.0
INA128UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
INA129U/2K5	SOIC	D	8	2500	353.0	353.0	32.0
INA129U/2K5G4	SOIC	D	8	2500	353.0	353.0	32.0
INA129UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0



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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA128P	Р	PDIP	8	50	506	13.97	11230	4.32
INA128P	Р	PDIP	8	50	506	13.97	11230	4.32
INA128P.A	Р	PDIP	8	50	506	13.97	11230	4.32
INA128P.A	Р	PDIP	8	50	506	13.97	11230	4.32
INA128PA	Р	PDIP	8	50	506	13.97	11230	4.32
INA128PA	Р	PDIP	8	50	506	13.97	11230	4.32
INA128PA.A	Р	PDIP	8	50	506	13.97	11230	4.32
INA128PA.A	Р	PDIP	8	50	506	13.97	11230	4.32
INA128PG4	Р	PDIP	8	50	506	13.97	11230	4.32
INA128PG4	Р	PDIP	8	50	506	13.97	11230	4.32
INA128U	D	SOIC	8	75	506.6	8	3940	4.32
INA128U.B	D	SOIC	8	75	506.6	8	3940	4.32
INA128UA	D	SOIC	8	75	506.6	8	3940	4.32
INA128UA.B	D	SOIC	8	75	506.6	8	3940	4.32
INA129P	Р	PDIP	8	50	506	13.97	11230	4.32
INA129P.A	Р	PDIP	8	50	506	13.97	11230	4.32
INA129PA	Р	PDIP	8	50	506	13.97	11230	4.32
INA129PA.A	Р	PDIP	8	50	506	13.97	11230	4.32
INA129U	D	SOIC	8	75	506.6	8	3940	4.32
INA129U.B	D	SOIC	8	75	506.6	8	3940	4.32
INA129UA	D	SOIC	8	75	506.6	8	3940	4.32
INA129UA.B	D	SOIC	8	75	506.6	8	3940	4.32



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.



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