

# ESD8x2 2-Channel, 36V ESD Protection Diode

#### 1 Features

- Working voltage 36V
- Low leakage current 50nA (maximum)
- IEC 61000-4-2 ESD protection:
  - ±25kV contact and ±25kV air (ESD852)
  - ±18kV contact and ±18kV air (ESD862)
- Robust surge protection:
  - IEC 61000-4-5 (8/20µs): 4.3A (ESD852)
  - IEC 61000-4-5 (8/20µs): 3.1A (ESD862)
- Bidirectional ESD protection
- I/O capacitance = 2.8pF typical (ESD852)
- I/O capacitance = 2.6pF typical (ESD862)
- Leaded packages used for automatic optical inspection (AOI)

# 2 Applications

- Factory automation
- Communication equipments
- USB power delivery (USB-PD):
  - VBUS protection
  - IO protection (withstand short to VBUS)
- Industrial communications:
  - CAN / CAN-FD

# 3 Description

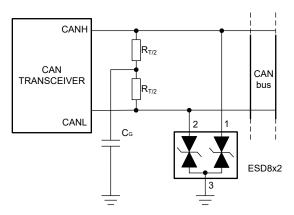
The ESD8x2 devices are bidirectional ESD protection diodes for USB power delivery (USB-PD) and industrial interfaces. The devices are rated to dissipate ESD that meets or exceeds the maximum level specified in the IEC 61000-4-2 standard (±25kV contact and airgap, or ±18kV contact and airgap). The low dynamic resistance and low clamping voltage enables system level protection against transient events. This protection is key because industrial systems require a high level of robustness and reliability.

These devices feature a low IO capacitance per channel and a pin-out to suit two IO lines from damage caused by electrostatic discharge (ESD) and other transients. The  $I_{PP}$  = 4.3A (8/20µs surge waveform) capability of the ESD852 makes it an excellent choice for protecting USB VBUS against transient surge events as well as industrial I/O lines. Additionally, the 2.8pF or 2.6pF line capacitance of the ESD8x2 are an excellent choice for protecting the slower speed signals for USB power delivery and IO signals for industrial applications.

### **Package Information**

PART NUMBER	CHANNEL	PACKAGE <sup>(1)</sup>		
ESD852	2 Channels	DBZ (SOT-23, 3)		
ESD862	2 Grianneis	DCK (SOT-SC70, 3)		

For more information, see Section 9.



ESD8x2 Typical Application



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# **4 Pin Configuration and Functions**

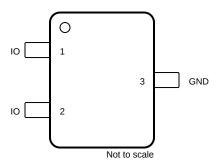


Figure 4-1. DBZ or DCK Package, SOT-23 (Top View)

**Table 4-1. Pin Functions** 

PIN		TYPE <sup>(1)</sup>	DESCRIPTION			
NAME	NO.	ITPE\/	DESCRIPTION			
Ю	1, 2	I/O	ESD protected IO			
GND	3	G	Connect to ground.			

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power



# **5 Specifications**

# 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	PARAMETER	DEVICE	MIN	MAX	UNIT
Dan	IEC 61000-4-5 Power (t <sub>p</sub> – 8/20μs) at 25°C	ESD852		233	W
Ppp	IEC 61000-4-5 Power (t <sub>p</sub> – 8/20μs) at 25°C	ESD862		175	W
	IEC 61000-4-5 current (t <sub>p</sub> - 8/20µs) at 25°C	ESD852		4.3	Α
I <sup>pp</sup>	IEC 61000-4-5 current (t <sub>p</sub> - 8/20µs) at 25°C	ESD862		3.1	Α
T <sub>A</sub>	Operating free-air temperature		-55	150	°C
TJ	Junction temperature		-55	150	°C
T <sub>stg</sub>	Storage temperature		-65	155	°C

<sup>(1)</sup> Operation outside the Section 5.1 may cause permanent device damage. Section 5.1 do not imply functional operation of the device at these or any other conditions beyond those listed under Section 5.4. If used outside the Section 5.4 but within the Section 5.1, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

## 5.2 ESD Ratings—JEDEC Specification

PARAMETER		TEST CONDITION	VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	± 2500	V	
	Charged device model (CDM), per JEDEC specification JS-002 <sup>(2)</sup>	± 1000	'	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

# 5.3 ESD Ratings—IEC Specification

over TA = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	DEVICE	VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic dischar		IEC 61000-4-2 Contact Discharge, all pins	ESD852	±25000	V
	Electrostatic discharge	TEC 61000-4-2 Contact Discharge, all pins	ESD862	±18000	V
		IFC 61000 4 2 Air Discharge all pins	ESD852	±25000	V
		IEC 61000-4-2 Air Discharge, all pins	ESD862	±18000	V

## **5.4 Recommended Operating Conditions**

	PARAMETER	MIN	NOM MAX	UNIT
V <sub>IN</sub>	Input voltage	-36	36	V
T <sub>A</sub>	Operating free-air temperature	-55	150	°C

Product Folder Links: ESD852 ESD862

### 5.5 Thermal Information

		ESC	852	ESC		
	THERMAL METRIC(1)	DBZ (SOT-23)	DCK (SC-70)	DBZ (SOT-23)	DCK (SC-70)	UNIT
		3 PINS	3 PINS	3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	293.4	258.1	313.5	265.4	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	148.9	134.8	162.8	142.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	133.0	75.1	151.8	82.4	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	32.9	31.1	43.5	38.2	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	132.0	74.3	150.8	81.5	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

# **5.6 Electrical Characteristics**

over  $T_A = 25$ °C (unless otherwise noted)<sup>(1)</sup>

	PARAMETER	TEST CONDITIONS	DEVICE	MIN	TYP	MAX	UNIT
$V_{RWM}$	Reverse stand-off voltage			-36		36	V
V <sub>BRF</sub>	Forward breakdown voltage <sup>(1)</sup> (2)	I <sub>IO</sub> = 10mA, IO to GND		37.8	40	44.2	V
V <sub>BRR</sub>	Reverse breakdown voltage (1) (2)	I <sub>IO</sub> = -10mA, IO to GND		-44.2	-40	-37.8	V
		$I_{PP}$ = 1A, $t_p$ = 8/20 $\mu$ s, IO to GND	ESD852		43	50	V
.,	Clamping valtage(3)	$I_{PP}$ = 4. A, $t_p$ = 8/20 $\mu$ s, from IO to GND	_ E9D092		61	66	V
V <sub>CLAMP</sub> CI	Clamping voltage <sup>(3)</sup>	$I_{PP}$ = 1A, $t_p$ = 8/20µs, from IO to GND	ESD862		47		V
		$I_{PP}$ = 3.1A, $t_p$ = 8/20 $\mu$ s, from IO to GND			61		V
V	Clamping voltage <sup>(4)</sup>	I <sub>PP</sub> = 16A, TLP, IO to GND or GND to IO	ESD852		63		V
V CLAMP	Clamping voltage(*)		ESD862		64		V
I <sub>LEAK</sub>	Leakage current	V <sub>IO</sub> = ±36V, IO to GND			5	50	nA
В	Dynamia raciatanaa(4)	(4)	ESD852		0.49		Ω
R <sub>DYN</sub> Dyna	Dynamic resistance <sup>(4)</sup>	IO to GND and GND to IO	ESD862		0.49		Ω
C	Line capacitance <sup>(1)</sup>	V <sub>IO</sub> = 0V, f = 1MHz, V <sub>pp</sub> = 30mV	ESD852		2.8	3.5	pF
CL	при сараснансе	V <sub>IO</sub> = 0V, I = 11VIFIZ, V <sub>pp</sub> = 30111V	ESD862		2.6	2.9	pF

<sup>(1)</sup> Measured from IO to GND on each channel.

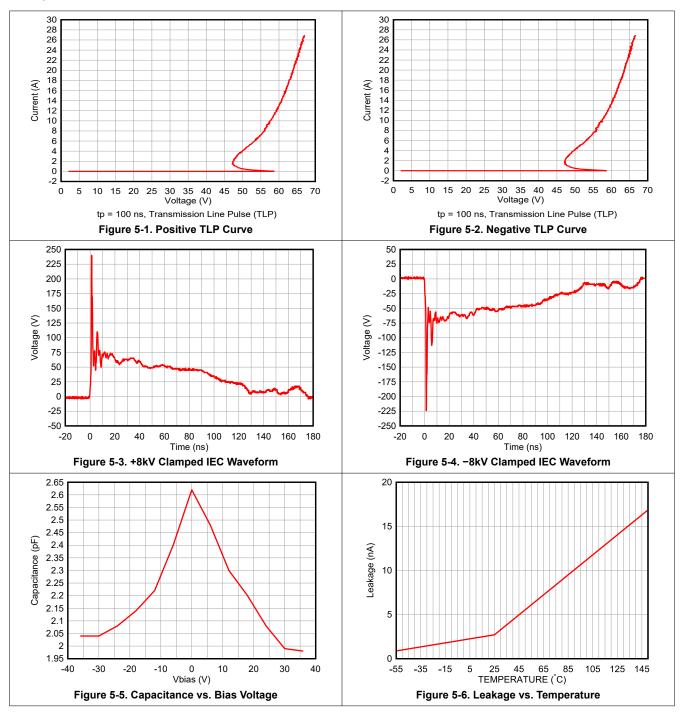
<sup>(2)</sup> V<sub>BRF</sub> and V<sub>BRR</sub> are defined as the voltage when ± 10mA is applied in the positive or negative direction respectively.

<sup>(3)</sup> Device stressed with 8/20µs exponential decay waveform according to IEC 61000-4-5.

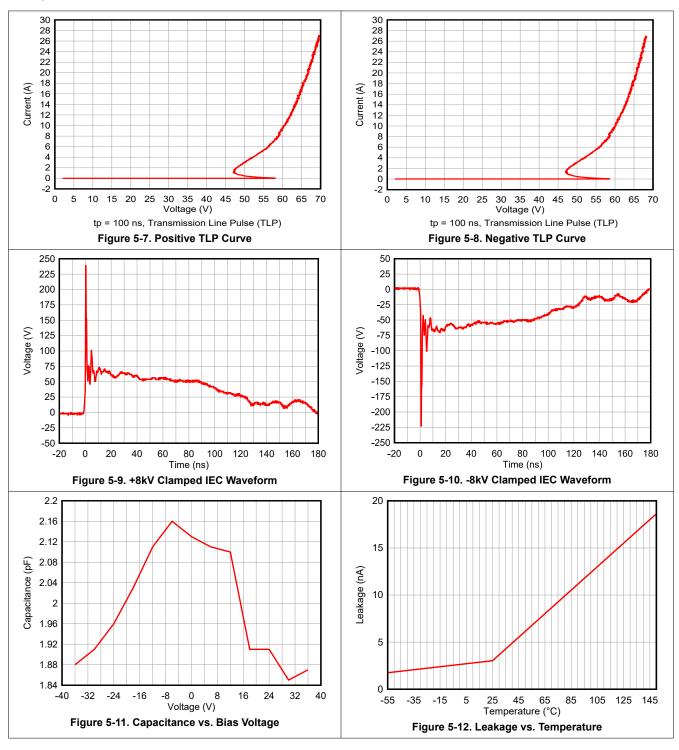
<sup>(4)</sup> Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008



# 5.7 Typical Characteristics - ESD852



# 5.8 Typical Characteristics – ESD862





# 6 Application and Implementation

#### **Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

# **6.1 Application Information**

The ESD8x2 devices are ESD diodes which provide a path to ground for dissipating transient voltage spikes, such as ESD or surge on signal lines and power lines. Connect the devices in parallel to the down stream circuitry they are protecting. As the current from the transient passes through the ESD device, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low  $R_{DYN}$  of the triggered ESD device holds this voltage ( $V_{CLAMP}$ ) to a safe level for the protected IC. For more information on how to properly use this device, refer to the *ESD Packaging and Layout Guide*.

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# 7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 7.1 Documentation Support

#### 7.1.1 Related Documentation

For related documentation, see the following:

- · Texas Instruments, ESD Layout Guide user's guide
- Texas Instruments, ESD and Surge Protection for USB Interfaces application note
- Texas Instruments, ESD Protection Diodes EVM user's guide
- Texas Instruments, Generic ESD Evaluation Module user's guide
- Texas Instruments, Reading and Understanding an ESD Protection data sheet

### 7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 7.3 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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#### 7.4 Trademarks

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#### 7.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 7.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

### 8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision *	(November 2023) to Revision A	(June 2025)
Changes Hom Kevision	(Novellibel 2023) to Kevision F	(Julie 2023)

Page

Added DCK package.....1

DATE	REVISION	NOTES		
November 2023	*	Initial Release		



# 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
ESD852DBZR	Active	Production	SOT-23 (DBZ)   3	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2Z38
ESD852DBZR.B	Active	Production	SOT-23 (DBZ)   3	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2Z38
ESD862DBZR	Active	Production	SOT-23 (DBZ)   3	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2Z78
ESD862DBZR.B	Active	Production	SOT-23 (DBZ)   3	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2Z78

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

# **PACKAGE MATERIALS INFORMATION**

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## TAPE AND REEL INFORMATION





	•
A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD852DBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
ESD862DBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3

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### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD852DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
ESD862DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0



SMALL OUTLINE TRANSISTOR



## NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
   This drawing is subject to change without notice.
   Reference JEDEC registration TO-236, except minimum foot length.

- 4. Support pin may differ or may not be present.
- 5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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