

ESD501 Low Capacitance ESD Diode for RF and ADAS Signal Protection

1 Features

- IEC 61000-4-2 ESD Protection:
 - ±15kV contact discharge
 - ±15kV air gap discharge
- IEC 61000-4-5 surge protection:
 - 3A (8/20µs)
- I/O capacitance: 0.3pF (typical)
- Ultra low leakage current: 1nA (typical)
- Industry standard 0402 package

2 Applications

- Automotive Antenna ESD Protection
- RF Signal ESD Protection
- Near Field Communications (NFC)
- Automotive SerDes w/Power over Coax
- USB Type-C (short-to-Vbus tolerant)

3 Description

The ESD501 is a bidirectional ESD protection diode. The ESD501 is offered in the industry standard 0402 (DFN1006) package, and offers an IEC 61000-4-2 protection level of 15kV. The device can clamp 8/20µs surges with peak pulse currents up to 3A in accordance with the IEC 61000-4-5 standard.

The low capacitance and low leakage current help to ensure protection against transient events in a variety of systems and applications. This protection is key for many applications, such as smaller form factors and faster data speeds, which are becoming more popular over time.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
ESD501	DPY (DFN1006, 2)	1mm × 0.6mm

- For more information, see Section 8.
- The package size (length × width) is a nominal value and includes pins, where applicable.

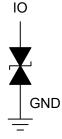


Figure 3-1. Functional Block Diagram



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4 Pin Configuration and Functions

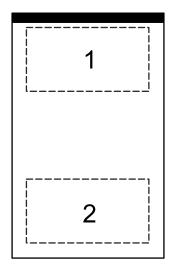


Figure 4-1. DPY Package, 2-Pin DFN1006 (Top View)

Table 4-1. Pin Functions

PIN TYPE(1)		TVDE(1)	DESCRIPTION	
NAME	NO.	I I PE\ /	DESCRIPTION	
Ю	1	I/O ESD Protected Channel. If used as ESD I/O, connect pin 2 to ground		
Ю	2	I/O	ESD Protected Channel. If used as ESD I/O, connect pin 1 to ground	

(1) I = input, O = output



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	Parameter	MIN	MAX	UNIT
I _{PPM}	IEC 61000-4-5 Surge (t_p = 8/20 μ s) Peak Pulse Current at 25 °C $^{(2)}$		3	Α
T _A	Operating free-air temperature	-40	125	°C
T _{stg}	Storage temperature	-65	155	°C

- (1) Stresses beyond those listed under Absolute Maximum Rating may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability
- (2) Voltages are with respect to GND unless otherwise noted.

5.2 ESD Ratings -JEDEC Specifications

Parameter		Test Conditions	VALUE	UNIT
	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	±2500	V	
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JS-002, all pins ⁽²⁾	±1000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings - IEC Specifications

Parameter		Test Conditions	VALUE	UNIT
V	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±15000	\/
V _(ESD)	Electrostatic discharge	IEC 61000-4-2 Air Discharge, all pins	±15000	V

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM MAX	UNIT
V _{IN}	Input voltage	-12	12	V
T _A	Operating Free Air Temperature	-40	125	°C

Product Folder Links: ESD501



5.5 Thermal Information

		ESD501	
	THERMAL METRIC ⁽¹⁾	DPY (DFN1006)	UNIT
		2 PINS	
R _{0JA}	Junction-to-ambient thermal resistance	284.4	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	153.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	100.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	99.9	°C/W
R ₀ JC(bot)	Junction-to-case (bottom) thermal resistance	N/A	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.6 Electrical Characteristics

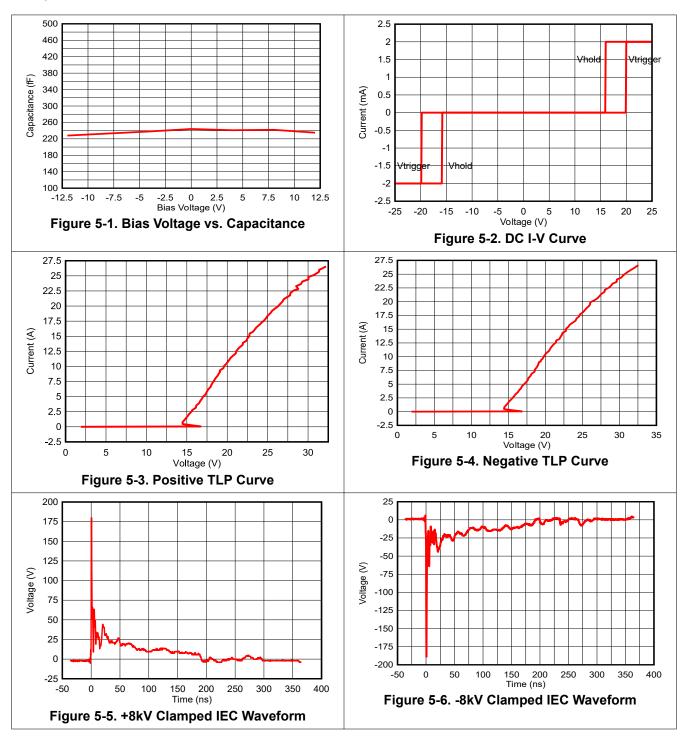
At TA = 25°C unless otherwise noted

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{RWM} Reverse stand-off voltage		I _{IO} < 10 nA	-12		12	V
I _{LEAK}	Leakage current at V _{RWM}	VIO = ±12 V, I/O to GND		1	10	nA
V_{BR}	Breakdown voltage, I/O to GND (1)	I _{IO} = ±1 mA	13.2	15	18	V
Surge clamping voltage, t _p = 8/20 µs		I _{PP} = 3 A, I/O to GND		23		V
.,	(2)	I _{PP} = 3 A, GND to I/O		23		V
V _{CLAMP}	TID elemping veltage t = 100 mg (3)	I _{PP} = ±4 A (100 ns TLP), I/O to GND		19.4		V
TLP clamping voltage, $t_p = 100 \text{ ns}^{(3)}$		I _{PP} = ±16 A (100 ns TLP), I/O to GND		27		V
Б	Dynamic resistance (4)	I/O to GND		0.6		Ω
R _{DYN}	Dynamic resistance (*/	GND to I/O		0.6		12
C _{LINE}	Line capacitance, IO to GND	V _{IO} = 0 V, f = 1 MHz		0.3	0.5	pF

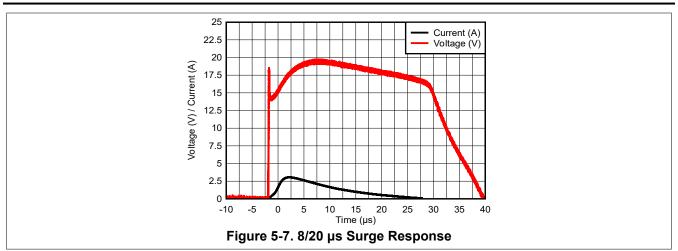
- V_{BR} is defined as the voltage obtained at 1 mA when sweeping the voltage up, before the device enters the snapback state
- Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5 (2)
- Non-repetitive square wave current pulse, Transmission Line Pulse (TLP); ANSI / ESD STM5.5.1-2008 Extraction of R_{DYN} using least squares fit of TLP characteristics between I = 10 A and I = 20 A



5.7 Typical Characteristics









6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6.3 Trademarks

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6.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2024	*	Initial Release

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: ESD501

www.ti.com 8-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
ESD501DPYR	Active	Production	X1SON (DPY) 2	10000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-55 to 150	Q3
ESD501DPYR.B	Active	Production	X1SON (DPY) 2	10000 LARGE T&R	-	Call TI	Call TI	-55 to 150	

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF ESD501:

Automotive : ESD501-Q1

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD501DPYR	X1SON	DPY	2	10000	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 23-Nov-2024



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD501DPYR	X1SON	DPY	2	10000	205.0	200.0	33.0

1 x 0.6 mm

PLASTIC SMALL OUTLINE - NO LEAD

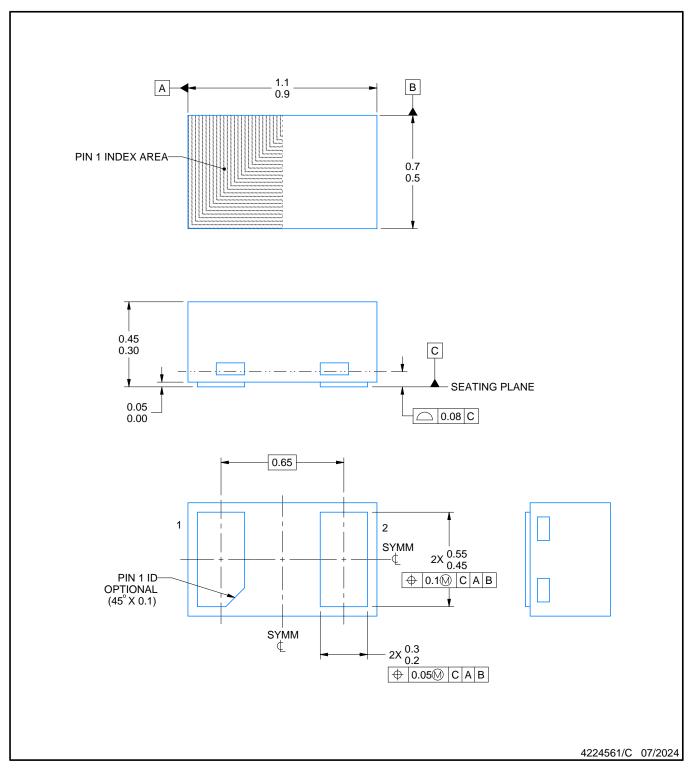
This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC SMALL OUTLINE - NO LEAD

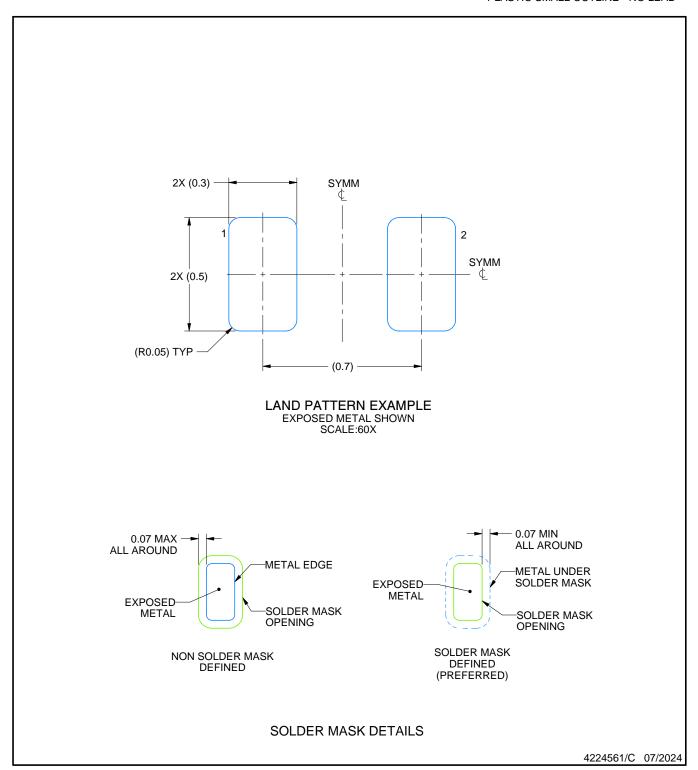


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
- per ASME Y14.5M
 2. This drawing is subject to change without notice.



PLASTIC SMALL OUTLINE - NO LEAD

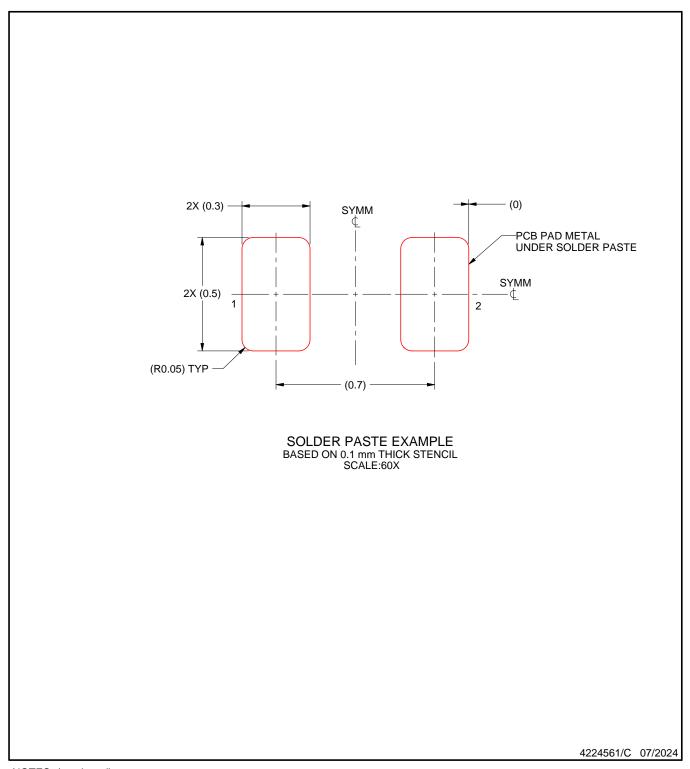


NOTES: (continued)

- 3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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