ESD321 1-Channel 30kV ESD Protection Diode with Low Capacitance (< 1pF) in 0402 and SOD-523 Packages

1 Features

- IEC 61000-4-2 Level 4 ESD protection:
  - ±30kV contact discharge
  - ±30kV air gap discharge
- IEC 61000-4-4 EFT protection:
  - 80A (5/50ns)
- IEC 61000-4-5 surge protection:
  - 6A (8/20µs)
- IO capacitance: 0.9pF (typical)
- DC breakdown voltage: 4.5V (minimum)
- Low leakage current: 0.1nA (typical)
- Extremely Low ESD clamping voltage:
  - 6.8V at 16A TLP (I/O to GND)
  - R_{DYN}: 0.13Ω (I/O to GND)
- Industrial temperature range: –40°C to +125°C
- Industry standard 0402 (DFN1006P2) and SOD-523 packages

2 Applications

- End equipment:
  - Wearables
  - Industrial and service robots
  - Laptops and desktops
  - Mobile and tablets
  - Set-top boxes
  - DVR and NVR
  - TV and monitors
  - EPOS (electronic point of sale)
- Interfaces:
  - USB 2.0/1.1
  - GPIO
  - Ethernet 10/100/1000 Mbps
  - Pushbuttons
  - Audio

3 Description

The ESD321 is a uni-directional TVS ESD protection diode featuring low dynamic resistance and low clamping voltage. The ESD321 is rated to dissipate ESD strikes up to ±30kV per the IEC 61000-4-2 international standard (greater than Level 4).

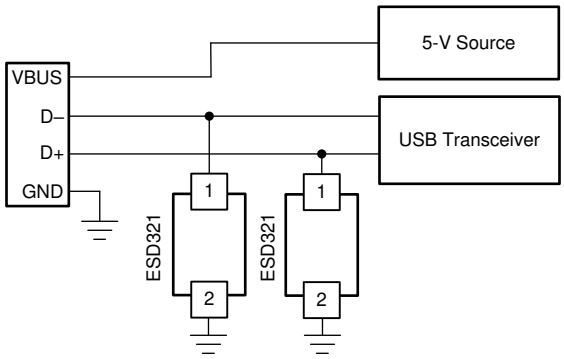
The ultra-low dynamic resistance (0.13Ω) and extremely low clamping voltage (6.8V at 16A TLP) ensure system level protection against transient events. This device has a low capacitance of 0.9pF IO capacitance making it suitable for protecting interfaces such as USB 2.0 and Ethernet 10/100/1000Mbps.

The ESD321 is offered in the industry standard 0402 (DPY/DFN1006P2) and SOD-523 (DYA) packages.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ESD321	DPY (X1SON, 2)	1mm × 0.6mm
	DYA (SOD-523, 2)	1.6mm × 0.8mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical USB 2.0 Application Schematic

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4 Pin Configuration and Functions

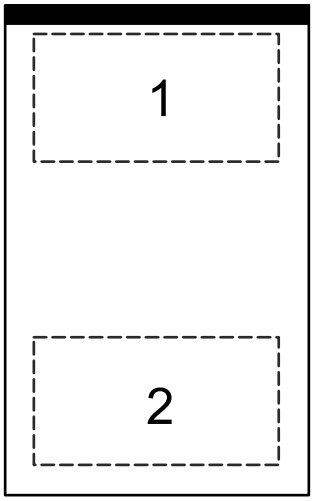

Figure 4-1. DPY Package, 2-Pin X1SON (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	DPY		
IO	1	I/O	ESD Protected Channel. Connect to the line being protected.
GND	2	GND	Connect to ground.

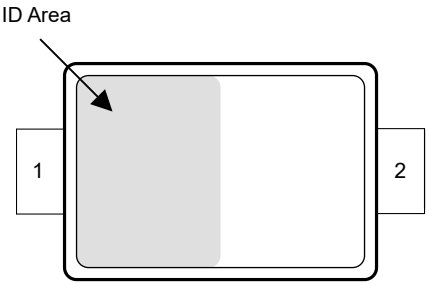

Figure 4-2. DYA Package, 2-Pin SOD-523 (Top View)

Table 4-2. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	DYA		
IO	2	I/O	ESD Protected Channel. Connect to the line being protected.
GND	1	GND	Connect to ground.

(1) I = input, O = output, GND = ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Electrical Fast Transient	IEC 61000-4-4 Peak Current at 25 °C		80	A
Surge Pulse	IEC 61000-4-5 Surge (tp 8/20µs) Peak Power at 25 °C		40	W
	IEC 61000-4-5 Surge (tp 8/20µs) Peak Current at 25 °C		6	A
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Section 5.1* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Section 5.4*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings – JEDEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings – IEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000	V
		IEC 61000-4-2 Air Discharge, all pins	±30000	

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	0		3.6	V
T_A	Operating Free Air Temperature	–40		125	°C

5.5 Thermal Information

THERMAL METRIC (1)		ESD321		UNIT
		DYA (SOD-523)	DPY (X1SON)	
		2 Pins	2 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	774.7	437.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	462.3	249.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	541.1	169.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	164.4	99.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	534.6	168.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.6 Electrical Characteristics

At TA = 25°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 50nA, across operating temperature range			3.6	V
$I_{LEAKAGE}$	Leakage current at 3.6V	V_{IO} = 3.6V, I/O to GND		0.1	10	nA
V_{BRF}	Breakdown voltage, I/O to GND (1)	I_{IO} = 1mA	4.5		7.5	V
V_{FWD}	Forward Voltage, GND to I/O (1)	I_{IO} = 1mA		0.8		V
V_{HOLD}	Holding voltage, I/O to GND (2)	I_{IO} = 1mA		5.1		V
V_{CLAMP}	Clamping voltage	I_{PP} = 6A (8/20µs Surge), I/O to GND		6.3		V
		I_{PP} = 16A (100ns TLP), I/O to GND		6.8		V
		I_{PP} = 16A (100ns TLP), GND to I/O		4.7		V
R_{DYN}	Dynamic resistance	I/O to GND, 100ns TLP, between 10 to 20A I_{PP}		0.13		Ω
		GND to I/O , 100ns TLP, between 10 to 20A I_{PP}		0.2		Ω
C_{LINE}	Line capacitance, IO to GND	V_{IO} = 0V, V_{p-p} = 30mV, f = 1MHz		0.9	1.1	pF

(1) V_{BRF} and V_{BRR} are defined as the voltage obtained at 1mA when sweeping the voltage up, before the device latches into the snapback state

(2) V_{HOLD} is defined as the voltage when 1mA is applied, after the device has successfully latched into the snapback state.

5.7 Typical Characteristics

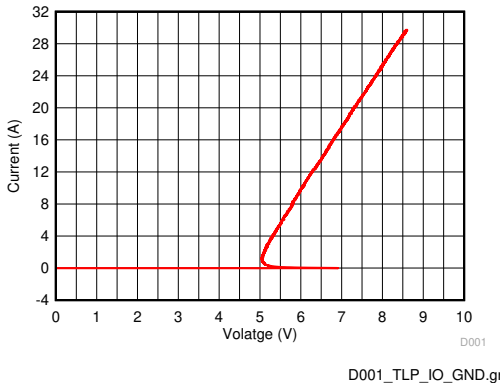

Figure 5-1. TLP I-V Curve, I/O Pin to GND (t_p = 100ns)

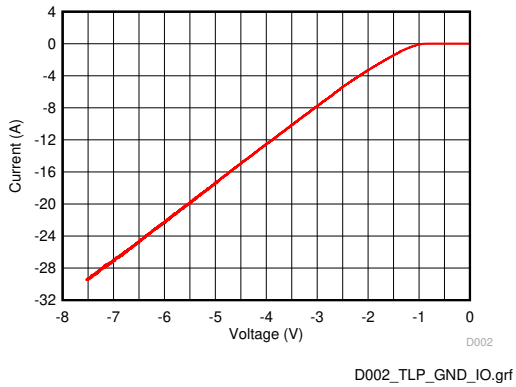

Figure 5-2. TLP I-V Curve, GND to I/O Pin (t_p = 100ns)

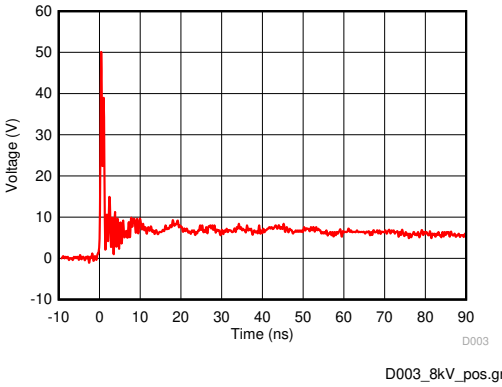

Figure 5-3. 8kV IEC 61000-4-2 Clamping Voltage Waveform, I/O Pin to GND

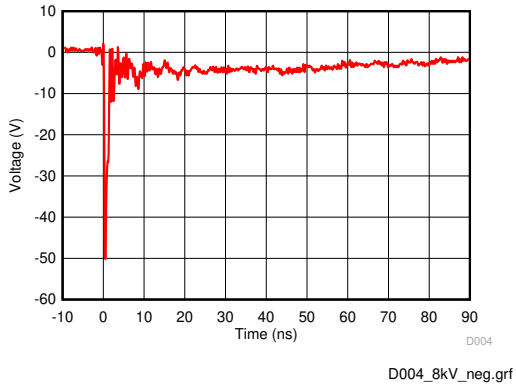

Figure 5-4. 8kV IEC 61000-4-2 Clamping Voltage Waveform, GND to I/O Pin

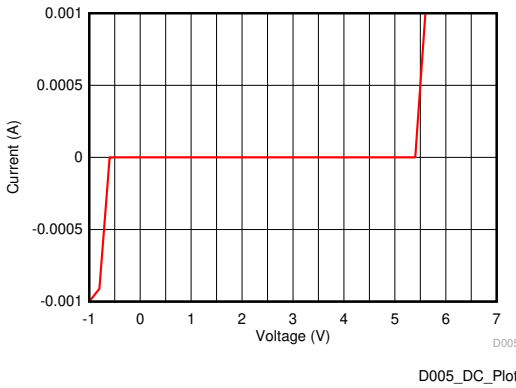

Figure 5-5. DC Voltage Sweep I-V Curve, I/O Pin to GND

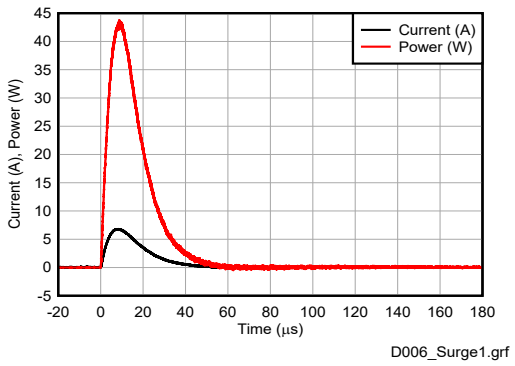

Figure 5-6. Surge Curve (IEC 61000-4-5, t_p=8/20µs), I/O Pin to GND

5.7 Typical Characteristics (continued)

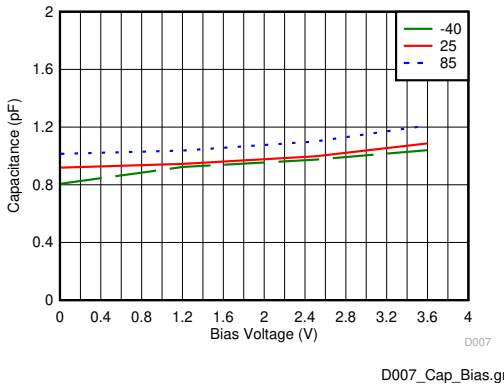

Figure 5-7. Capacitance vs. Bias Voltage For Different Temperatures (°C)

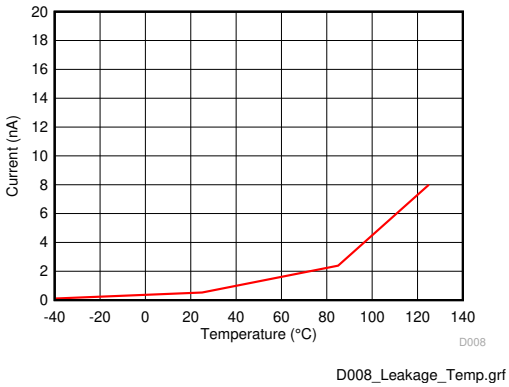

Figure 5-8. Leakage Current (at 3.6V Bias) Across Temperature, I/O Pin to GND

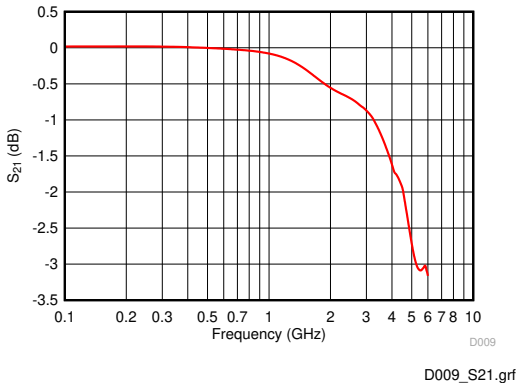

Figure 5-9. Insertion Loss vs. Frequency

6 Detailed Description

6.1 Overview

The ESD321 is a low capacitance uni-directional ESD Protection Diode with a low clamping voltage. This device can dissipate ESD strikes up to ±30kV (Contact and Air) per the IEC 61000-4-2 Standard. The low clamping makes this device suitable for protecting any ESD sensitive devices.

6.2 Functional Block Diagram

6.3 Feature Description

ESD321 provides ESD protection up to ±30kV contact and ±30kV air gap per IEC 61000-4-2 standard. During an ESD event, ESD diode connected to the I/O pin turns on and diverts the current to ground. Additionally, ESD321 also provides protection against IEC 61000-4-5 Surge currents up to 6A (8/20µs waveform) and up to 80A per IEC 61000-4-4 (5/50ns waveform, 4kV with 50Ω impedance) electrical fast transient (EFT) standard. The capacitance between the I/O pin and ground is 0.9pF (typical) and 1.1pF (maximum). The device features a low leakage current of 0.1nA (typical) and 50nA (maximum, across operating temperature range) with a bias of 3.6V. The ESD diode at the I/O pin protects the ESD-sensitive devices by clamping the voltage to a low value of 6.8V (I_{PP} = 16A 100ns TLP). The layout makes adding protection to an existing layout simple. The package offers flow-through routing, requiring minimal modification to an existing layout.

6.4 Device Functional Modes

The ESD321 is a passive integrated circuit that triggers when voltages exceed V_{BRF} or fall below V_{FWD}. During ESD events, voltages as high as ±30kV (contact or air) can be directed to ground through the internal diode network. When the voltages on the protected line fall below the trigger levels of ESD321 (typically within 10ns) the device returns to passive.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The ESD321 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

7.2 Typical Application

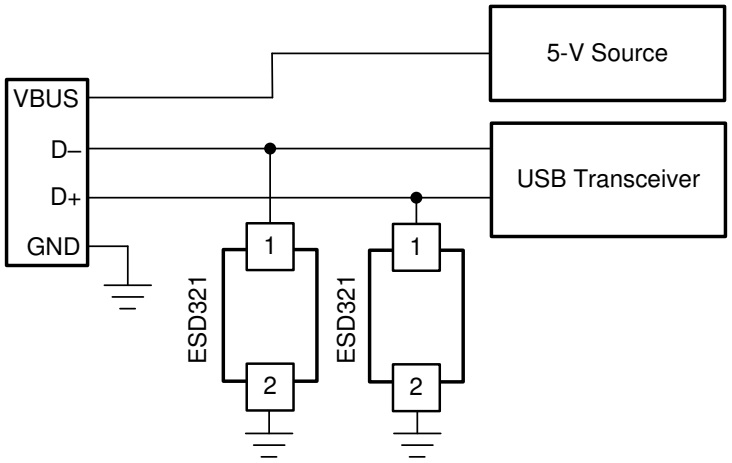

Figure 7-1. USB 2.0 ESD Schematic

7.2.1 Design Requirements

For this design example, two ESD321 devices are being used in a USB 2.0 application. This provides a complete ESD protection scheme.

Given the USB 2.0 application, the parameters listed in Table 7-1 are known.

Table 7-1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on DP-DM lines	0V to 3.6V
Operating frequency on DP-DM lines	up to 240MHz

7.2.2 Detailed Design Procedure

7.2.2.1 Signal Range

The ESD321 supports signal ranges between 0V and 3.6V, which supports the USB 2.0 signal pair on the USB 2.0 application.

7.2.2.2 Operating Frequency

The ESD321 has a 0.9pF (typical) capacitance, which supports the USB 2.0 data rates of 480Mbps.

7.2.3 Application Curve

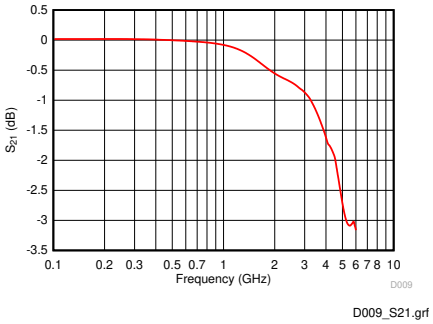

Figure 7-2. Insertion Loss Vs. Frequency

7.3 Power Supply Recommendations

Because the ESD321 is a passive ESD device, there is no need to power it. To help ensure the device functions properly, do not violate the recommended I/O specification (0V to 3.6V).

7.4 Layout

7.4.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, which increases EMI coupling.

7.4.2 Layout Example

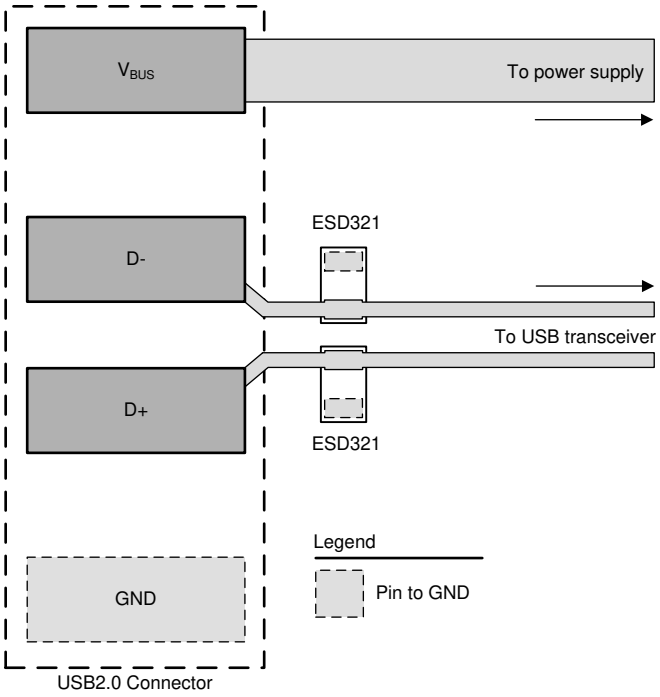

Figure 7-3. USB 2.0 ESD Layout

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Generic ESD Device Evaluation Module*

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2023) to Revision C (June 2025)	Page
• Separated pinout information into two tables	3

Changes from Revision A (December 2022) to Revision B (October 2023)	Page
• Updated the *Package Information* table to include package size	1
• Changed voltage to power in the *Surge Curve (IEC 61000-4-5, t_p=8/20µs), I/O Pin to GND* figure	6

Changes from Revision * (July 2018) to Revision A (December 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added the *DYA* package to the data sheet	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESD321DPYR	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DD
ESD321DPYR.B	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DD
ESD321DPYRG4	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	DD
ESD321DPYRG4.B	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	DD
ESD321DYAR	Active	Production	SOT-5X3 (DYA) | 2	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-55 to 150	1L8
ESD321DYAR.B	Active	Production	SOT-5X3 (DYA) | 2	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-55 to 150	1L8

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

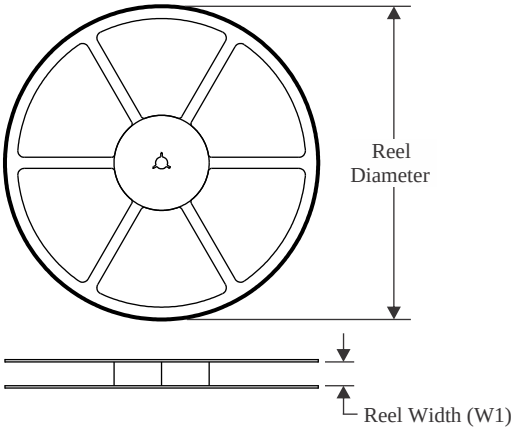
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

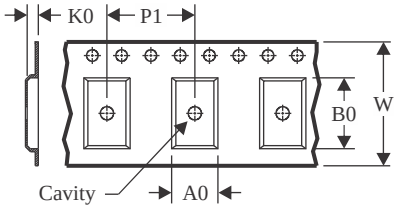
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

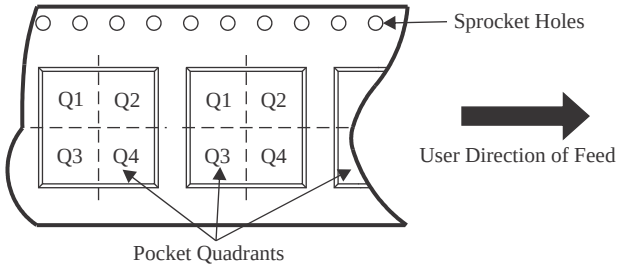


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

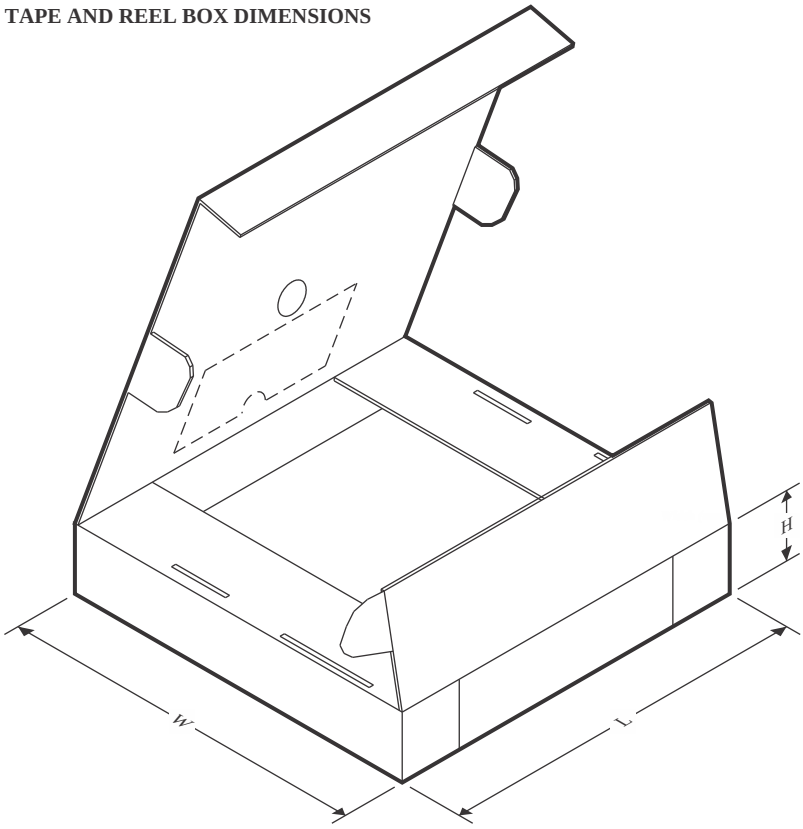
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD321DPYR	X1SON	DPY	2	10000	180.0	8.4	0.67	1.15	0.46	2.0	8.0	Q2
ESD321DPYRG4	X1SON	DPY	2	10000	180.0	8.4	0.67	1.15	0.46	2.0	8.0	Q2
ESD321DYAR	SOT-5X3	DYA	2	3000	178.0	9.5	0.5	1.94	0.73	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD321DPYR	X1SON	DPY	2	10000	210.0	185.0	35.0
ESD321DPYRG4	X1SON	DPY	2	10000	210.0	185.0	35.0
ESD321DYAR	SOT-5X3	DYA	2	3000	210.0	200.0	42.0

GENERIC PACKAGE VIEW

DPY 2

X1SON - 0.45 mm max height

1 x 0.6 mm

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

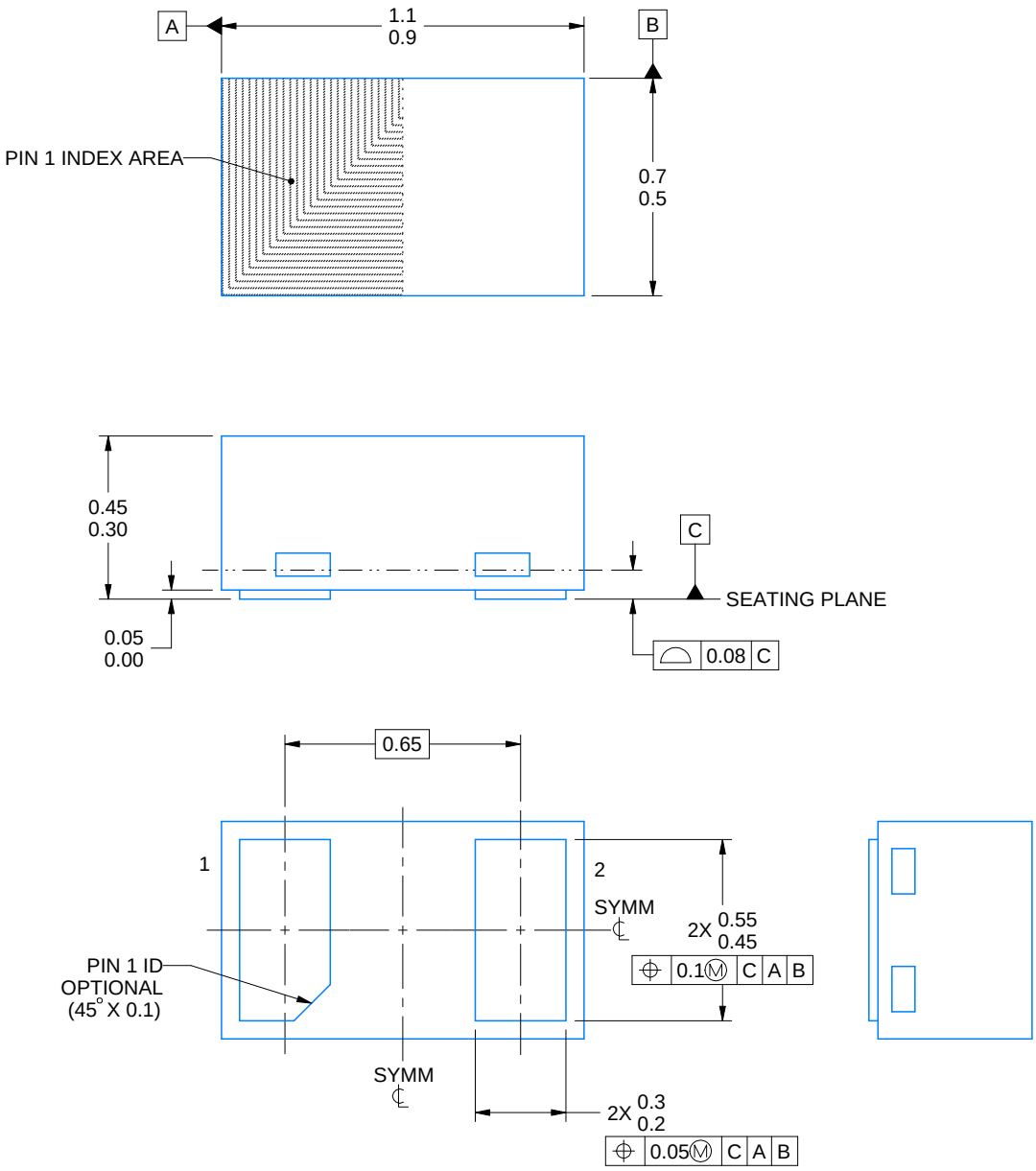
4231484/A

PACKAGE OUTLINE

DPY0002A

X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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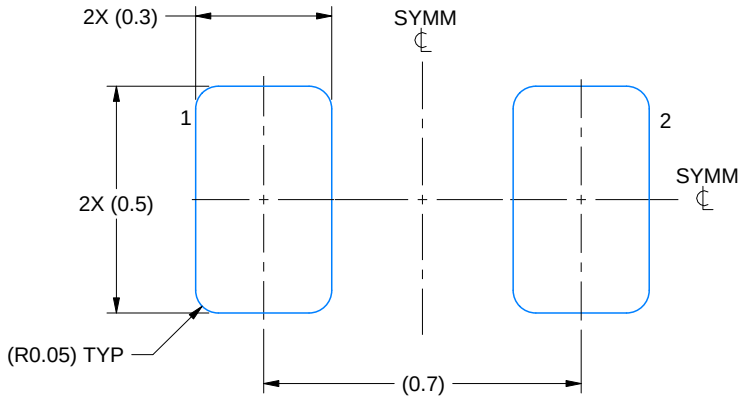
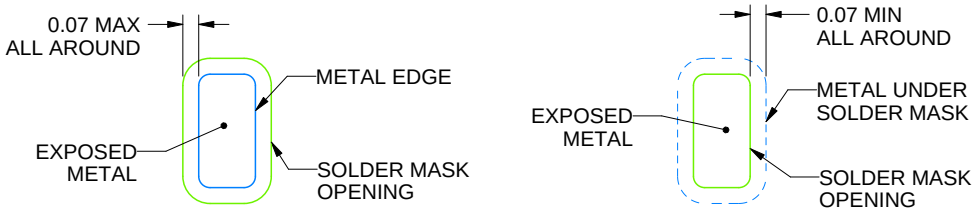
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



SOLDER MASK DETAILS

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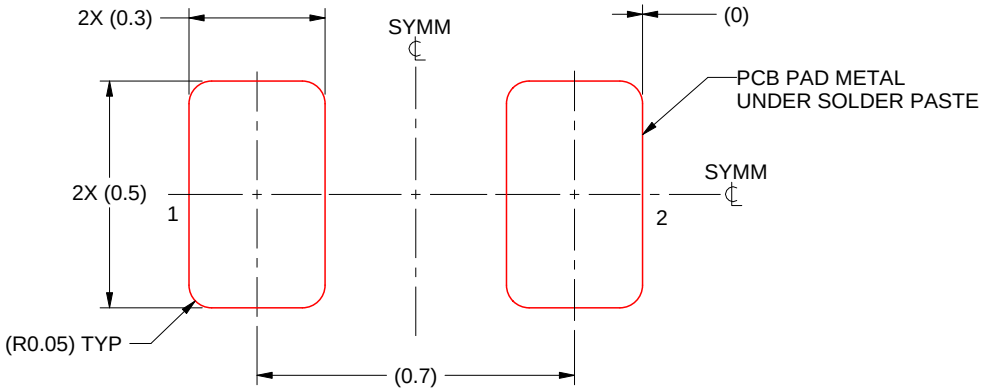
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

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NOTES: (continued)

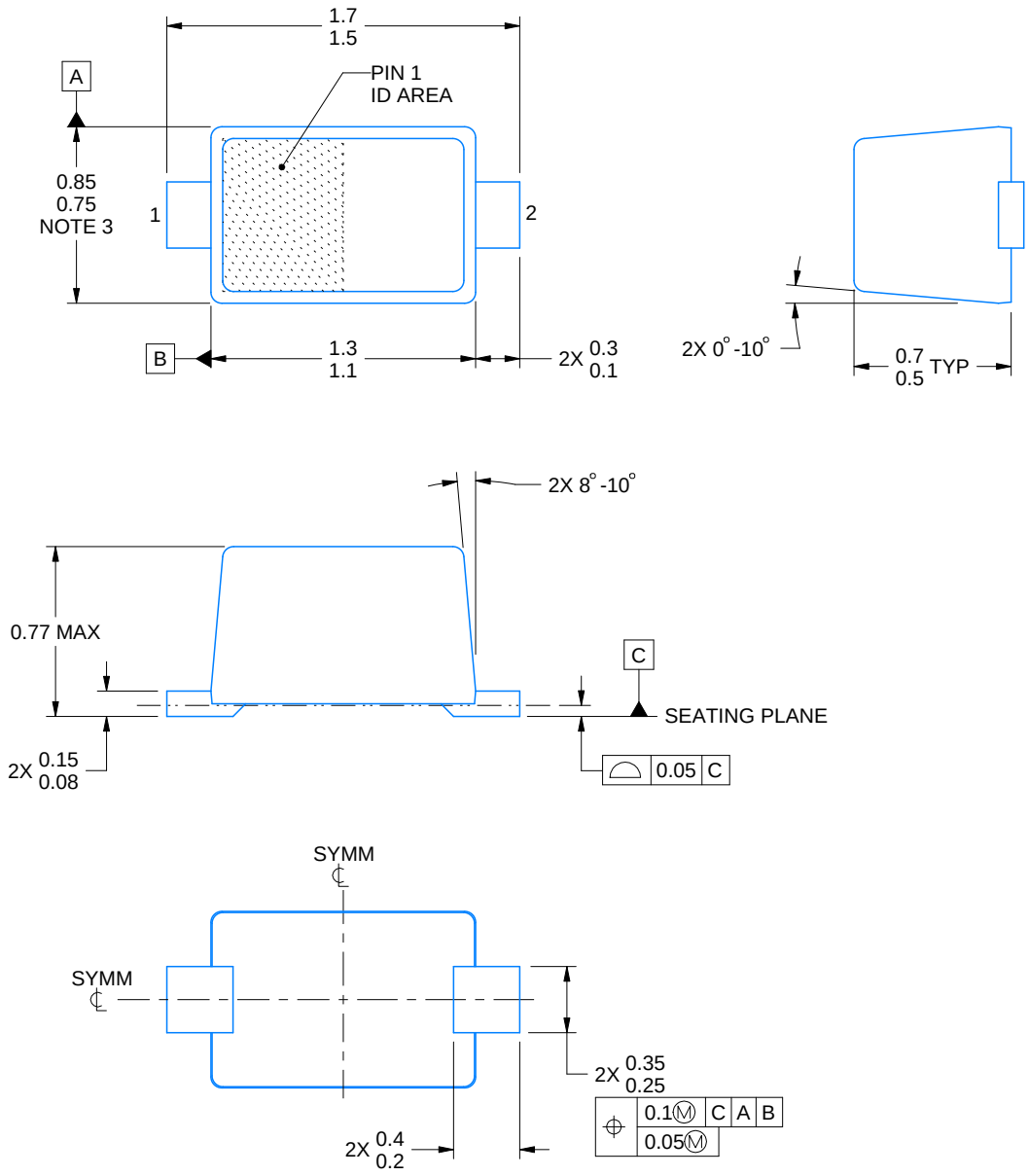
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DYA0002A

SOT (SOD-523) - 0.77 mm max height

PLASTIC SMALL OUTLINE



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NOTES:

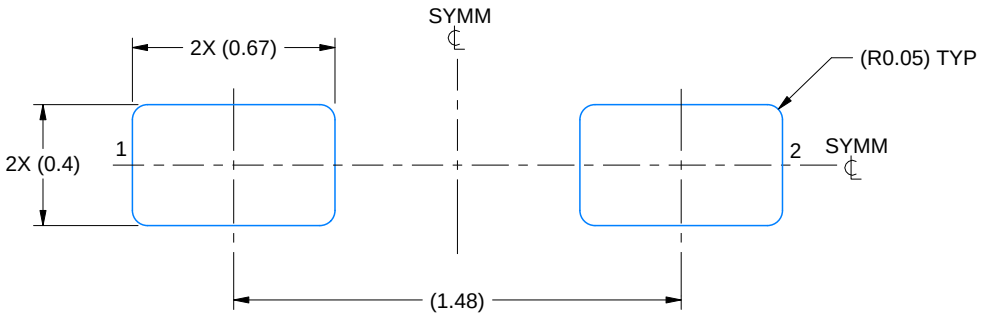
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEITA SC-79 registration except for package height

EXAMPLE BOARD LAYOUT

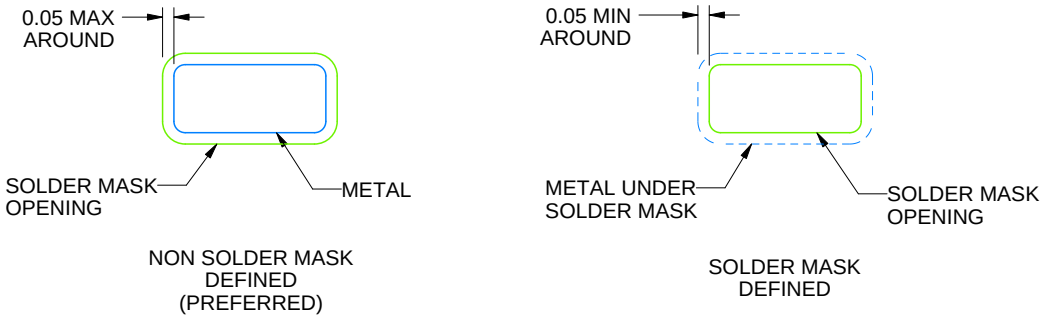
DYA0002A

SOT (SOD-523) - 0.77 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:40X



SOLDERMASK DETAILS

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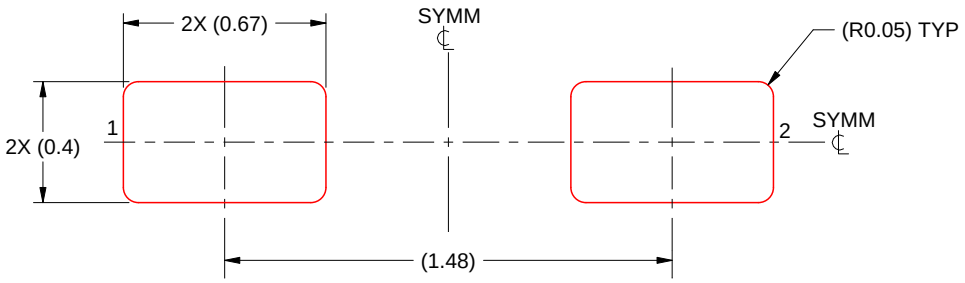
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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