











DS90LV027A

SNLS026D -MARCH 2000-REVISED JUNE 2016

DS90LV027A LVDS Dual High Speed Differential Driver

1 Features

- >600-Mbps (300 MHz) Switching Rates
- 0.3-ns Typical Differential Skew
- 0.7-ns Maximum Differential Skew
- 1.5-ns Maximum Propagation Delay
- 3.3-V Power Supply Design
- ±360-mV Differential Signaling
- Low Power Dissipation (46 mW at 3.3-V Static)
- · Flow-Through Design Simplifies PCB Layout
- Interoperable With Existing 5-V LVDS Devices
- Power-Off Protection (Outputs in High Impedance)
- Conforms to TIA/EIA-644 Standard
- 8-Pin SOIC Package Saves Space
- Industrial Temperature Operating Range: -40°C to 85°C

2 Applications

- Multi-Function Printers
- LVCMOS-to-LVDS Translation
- Building and Factory Automation
- Grid Infrastructure

3 Description

The DS90LV027A is a dual LVDS driver device optimized for high data rate and low-power applications. The device is designed to support data rates in excess of 600 Mbps (300 MHz) using Low Voltage Differential Signaling (LVDS) technology. The DS90LV027A is a current mode driver allowing power dissipation to remain low even at high frequency. In addition, the short circuit fault current is also minimized.

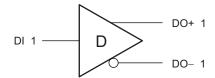
The device is in a 8-pin SOIC package. The DS90LV027A has a flow-through design for easy printed-circuit board (PCB) layout. The differential driver outputs provides low EMI with its typical low output swing of 360 mV. It is perfect for high-speed transfer of clock and data. The DS90LV027A can be paired with its companion dual line receiver, the DS90LV028A, or with any of TI's LVDS receivers, to provide a high-speed point-to-point LVDS interface.

Device Information⁽¹⁾

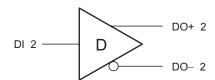
PART NUMBER	PACKAGE	BODY SIZE (NOM)		
DS90LV027A	SOIC (8)	4.90 mm × 3.91 mm		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Diagrams



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Table of Contents

1	Features 1		8.3 Feature Description	. 1
2	Applications 1		8.4 Device Functional Modes	. 1
3	Description 1	9	Application and Implementation	. 12
4	Revision History2		9.1 Application Information	
5	Pin Configuration and Functions 3		9.2 Typical Application	. 12
6	Specifications4	10	Power Supply Recommendations	. 13
•	6.1 Absolute Maximum Ratings	11	Layout	. 14
	6.2 ESD Ratings 4		11.1 Layout Guidelines	. 14
	6.3 Recommended Operating Conditions 4		11.2 Layout Example	. 14
	6.4 Thermal Information	12	Device and Documentation Support	. 18
	6.5 Electrical Characteristics 5		12.1 Documentation Support	. 1
	6.6 Switching Characteristics 5		12.2 Receiving Notification of Documentation Updates	s 1
	6.7 Typical Characteristics		12.3 Community Resources	. 1
7	Parameter Measurement Information9		12.4 Trademarks	. 1
8	Detailed Description 10		12.5 Electrostatic Discharge Caution	. 1
•	8.1 Overview		12.6 Glossary	. 1
	8.2 Functional Block Diagrams	13	Mechanical, Packaging, and Orderable Information	. 1!

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2013) to Revision D

Page

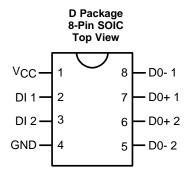
Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section

Changes from Revision B (April 2013) to Revision C

Page



5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION	
NAME	NO.	1/0	DESCRIPTION	
DI	2, 3	I	TL/CMOS driver input pins	
DO+	6, 7	0	Noninverting LVDS driver output pin	
DO-	5, 8	0	Inverting LVDS driver output pin	
GND	4	_	Ground pin	
V_{CC}	1	_	Positive power supply pin, 3.3 V ± 0.3 V	

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage, V _{CC}		-0.3	4	V
Input voltage, DI		-0.3	3.6	V
Output voltage, DO±		-0.3	3.9	V
	D package		1190	mW
Maximum package power dissipation at 25°C	Derate D package		9.5 mW/°C above 25°C	°C
Lead temperature range, soldering (4 s)			260	°C
Storage temperature, T _{stg}		-65	150	°C

⁽¹⁾ Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V Electrontation		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±8000	
	Flactroatatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	\/
V _(ESD)	Electrostatic discharge	EIAJ, 0 Ω, 200 pF	±1000	V
	IEC direct, 330 Ω, 150 pF	IEC direct, 330 Ω , 150 pF	±4000	

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
T _A	Operating free-air temperature	-40	25	85	°C

6.4 Thermal Information

			DS90LV027A	
	THERMAL METRIC ⁽¹⁾		D (SOIC)	UNIT
			8 PINS	
D		Low-K thermal resistance (2)	212	°C AA
$R_{\theta JA}$	Junction-to-ambient thermal resistance High-K thermal resistance ⁽²⁾		112	°C/W
R ₀ JC(top)	Junction-to-case (top) thermal resistance		69.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		47.7	°C/W
ΨЈТ	Junction-to-top characterization parameter	15.2	°C/W	
ΨЈВ	Junction-to-board characterization parameter	47.2	°C/W	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		_	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

⁽²⁾ Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface-mount packages.



6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) (1)(2)

	PARAMETER	TEST CONDI	TIONS	MIN	TYP ⁽³⁾	MAX	UNIT
V _{OD}	Output differential voltage	R_L = 100 Ω (see Figure 15), DC	R_L = 100 Ω (see Figure 15), DO+, DO- pins			450	mV
ΔV_{OD}	V _{OD} magnitude change	R_L = 100 Ω (see Figure 15), DC	D+, DO- pins		1	35	mV
V _{OH}	Output high voltage	R_L = 100 Ω (see Figure 15), DC	D+, DO- pins		1.4	1.6	V
V _{OL}	Output low voltage	$R_L = 100 \Omega$ (see Figure 15), DC	D+, DO- pins	0.9	1.1		V
Vos	Offset voltage	$R_L = 100 \Omega$ (see Figure 15), DC	D+, DO- pins	1.125	1.2	1.375	V
ΔV_{OS}	Offset magnitude change	$R_L = 100 \Omega$ (see Figure 15), DC	D+, DO- pins	0	3	25	mV
I _{OXD}	Power-off leakage	$V_{OUT} = V_{CC}$ or GND, $V_{CC} = 0$ V	$V_{OUT} = V_{CC}$ or GND, $V_{CC} = 0$ V, DO+, DO- pins			±10	μΑ
I _{OSD}	Output short-circuit current	DO+, DO- pins			-5.7	-8	mA
V _{IH}	Input high voltage	DI pin		2		V _{CC}	V
V _{IL}	Input low voltage	DI pin		GND		0.8	V
I _{IH}	Input high current	V _{IN} = 3.3 V or 2.4 V, DI pin			±2	±10	μΑ
I _{IL}	Input low current	V _{IN} = GND or 0.5 V, DI pin	V _{IN} = GND or 0.5 V, DI pin		±1	±10	μΑ
V_{CL}	Input clamp voltage	I _{CL} = −18 mA, DI pin	I _{CL} = −18 mA, DI pin		-0.6		V
	Davisa avanlı avansat	V V an CND V min	No load		8	14	^
I _{CC}	Power supply current	$V_{IN} = V_{CC}$ or GND, V_{CC} pin	$R_L = 100 \Omega$		14	20	mA

⁽¹⁾ Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD}.

6.6 Switching Characteristics

 R_L = 100 Ω and C_L = 15 pF, see Figure 16 and Figure 17 (unless otherwise noted) $^{(1)(2)(3)}$

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽⁴⁾	MAX	UNIT
t _{PHLD}	Differential propagation delay high to low		0.3	0.8	1.5	ns
t _{PLHD}	Differential propagation delay low to high		0.3	1.1	1.5	ns
t _{SKD1}	Differential pulse skew t _{PHLD} - t _{PLHD} (5)		0	0.3	0.7	ns
t _{SKD2}	Channel to channel skew ⁽⁶⁾		0	0.4	8.0	ns
t _{SKD3}	Differential part to part skew ⁽⁷⁾		0		1	ns
t _{SKD4}	Differential part to part skew ⁽⁸⁾		0		1.2	ns
t _{TLH}	Transition low to high time		0.2	0.5	1	ns
t _{THL}	Transition high to low time		0.2	0.5	1	ns
f_{MAX}	Maximum operating frequency (9)			350		MHz

⁽¹⁾ These parameters are ensured by design. The limits are based on statistical analysis of the device over PVT (process, voltage, temperature) ranges.

⁽²⁾ The DS90LV027A is a current mode device and only function with datasheet specification when a resistive load is applied to the drivers outputs.

⁽³⁾ All typicals are given for: $V_{CC} = 3.3 \text{ V}$ and $T_A = 25^{\circ}\text{C}$.

⁽²⁾ C_L includes probe and fixture capacitance.

⁽³⁾ Generator waveform for all tests unless otherwise specified: f = 1 MHz, $Z_0 = 50 \Omega$, $t_f \le 1$ ns, $t_f \le 1$ ns (10%-90%).

⁽⁴⁾ All typicals are given for: $V_{CC} = 3.3 \text{ V}$ and $T_A = 25^{\circ}\text{C}$.

⁽⁵⁾ t_{SKD1}, |t_{PHLD} - t_{PLHD}|, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

⁽⁶⁾ t_{SKD2} is the Differential Channel to Channel Skew of any event on the same device.

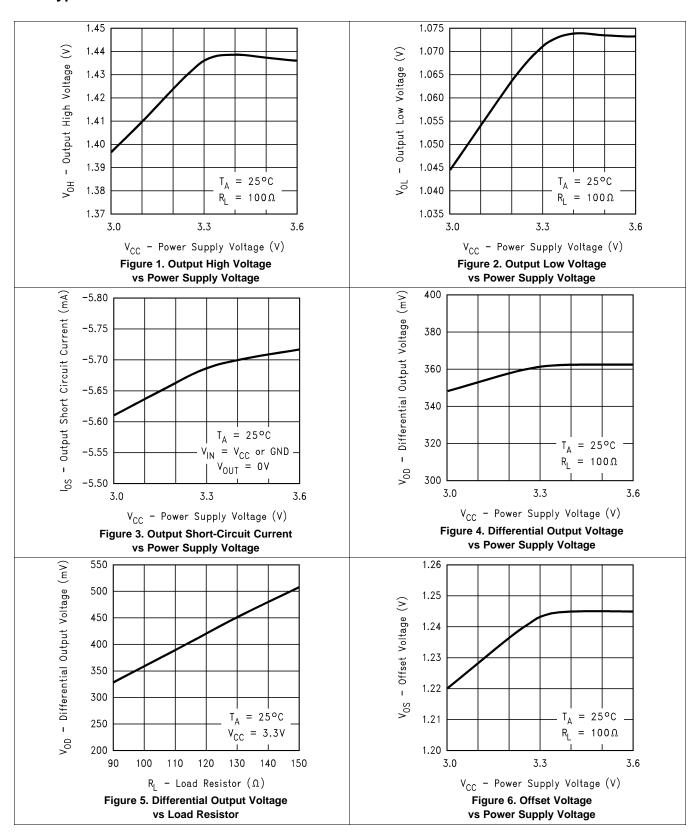
⁽⁷⁾ t_{SKD3}, Differential Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.

⁽⁸⁾ t_{SKD4}, part to part skew, is the differential channel to channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max - Min| differential propagation delay.

⁽⁹⁾ f_{MAX} generator input conditions: $t_r = t_f < 1$ ns (0% to 100%), 50% duty cycle, 0 V to 3 V. Output criteria: duty cycle = 45% / 55%, $V_{OD} > 250$ mV, all channels switching.

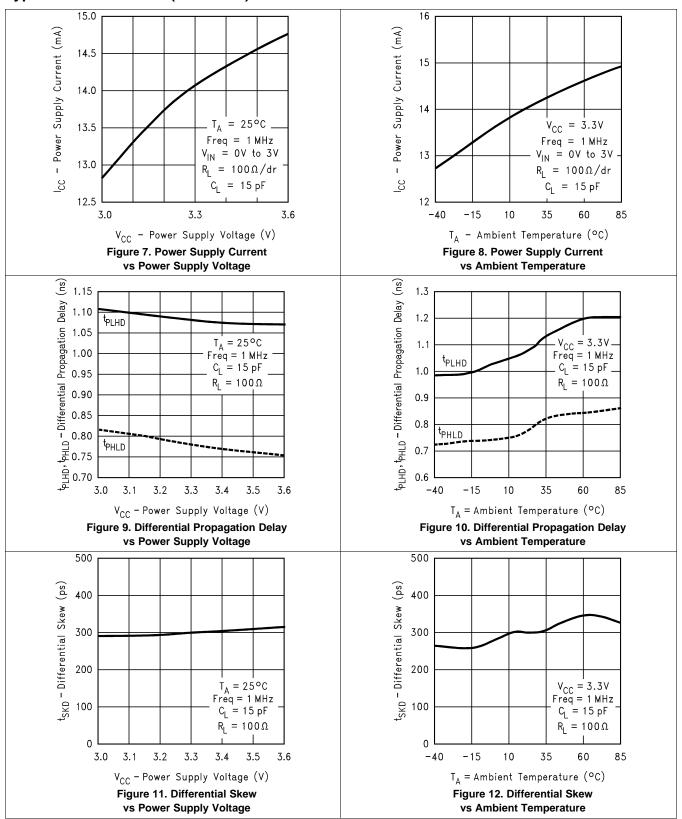


6.7 Typical Characteristics



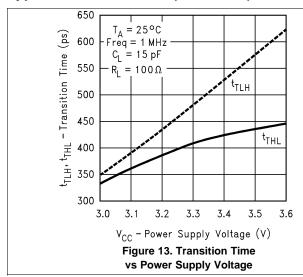


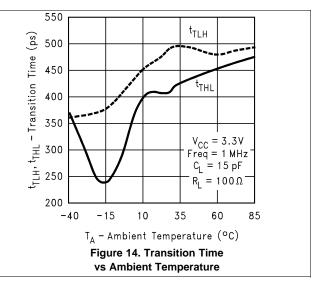
Typical Characteristics (continued)





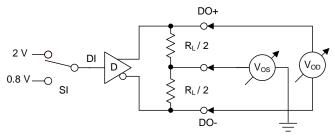
Typical Characteristics (continued)





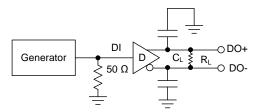


7 Parameter Measurement Information



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Figure 15. Differential Driver DC Test Circuit



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Figure 16. Differential Driver Propagation Delay and Transition Time Test Circuit

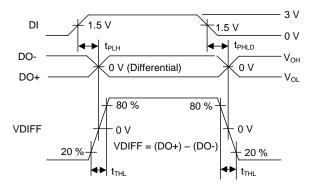


Figure 17. Differential Driver Propagation Delay and Transition Time Waveforms

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8 Detailed Description

8.1 Overview

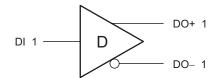
LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in Figure 19. This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic differential impedance of the media is in the range of 100 Ω . A termination resistor of 100 Ω (selected to match the media), and is placed as close to the receiver input pins as possible. The termination resistor converts the driver output current (current mode) into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be considered. The DS90LV027A differential line driver is a balanced current source design. A current mode driver, generally speaking has a high output impedance and supplies a constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). Current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The output current is typically 3.1 mA, a minimum of 2.5 mA, and a maximum of 4.5 mA. The current mode driver requires (as discussed above) that a resistive termination be employed to terminate the signal and to complete the loop as shown in Figure 19. AC or unterminated configurations are not allowed. The 3.1-mA loop current develops a differential voltage of 310 mV across the 100-Ω termination resistor which the receiver detects with a 250-mV minimum differential noise margin, (driven signal minus receiver threshold (250 mV - 100 mV = 150 mV). The signal is centered around 1.2 V (Driver Offset, VOS) with respect to ground as shown in Figure 18.

NOTE

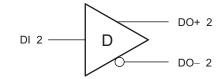
The steady-state voltage (VSS) peak-to-peak swing is twice the differential voltage (VOD) and is typically 620 mV.

The current mode driver provides substantial benefits over voltage mode drivers, such as an RS-422 driver. Its quiescent current remains relatively flat versus switching frequency. Whereas the RS-422 voltage mode driver increases exponentially in most case from 20 MHz to 50 MHz. This is due to the overlap current that flows between the rails of the device when the internal gates switch. Whereas the current mode driver switches a fixed current between its output without any substantial overlap current. This is similar to some ECL and PECL devices, but without the heavy static ICC requirements of the ECL/PECL designs. LVDS requires >80% less current than similar PECL devices. AC specifications for the driver are a tenfold improvement over other existing RS-422 drivers.

8.2 Functional Block Diagrams



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8.3 Feature Description

8.3.1 LVDS Fail-Safe

This section addresses the common concerns of fail-safe biasing of LVDS interconnects, specifically looking at the DS90LV027A driver outputs and the DS90LV028A receiver inputs.

The LVDS receiver is a high-gain, high-speed device that amplifies a small differential signal (20 mV) to CMOS logic levels. Due to the high gain and tight threshold of the receiver, take care to prevent noise from appearing as a valid signal.

The internal fail-safe circuitry of the receiver is designed to source or sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated, or shorted receiver inputs.

- Open Input Pins: The DS90LV028A is a dual receiver device, and if an application requires only 1 receiver, the unused channel inputs must be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pullup and pulldown resistors to set the output to a HIGH state. This internal circuitry ensures a HIGH, stable output state for open inputs.
- 2. Terminated Input: If the DS90LV027A driver is disconnected (cable unplugged), or if the DS90LV027A driver is in a TRI-STATE or power-off condition, the receiver output is in a HIGH state again, even with the end of cable 100-Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10 mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect must be used. Twisted pair cable offers better balance than flat ribbon cable.
- 3. Shorted Inputs: If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0-V differential input voltage, the receiver output remains in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (GND to 2.4 V). It is only supported with inputs shorted and no external common-mode voltage applied.

External lower value pullup and pulldown resistors (for a stronger bias) may be used to boost fail-safe in the presence of higher noise levels. The pullup and pulldown resistors must be in the $5-k\Omega$ to $15-k\Omega$ range to minimize loading and waveform distortion to the driver. The common-mode bias point must be set to approximately 1.2 V (less than 1.75 V) to be compatible with the internal circuitry.

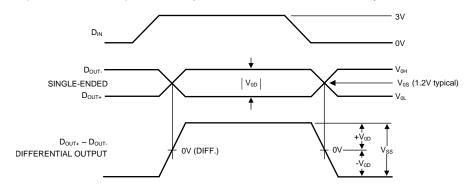


Figure 18. Driver Output Levels

8.4 Device Functional Modes

Table 1 lists the functional modes of the DS90LV027A.

Table 1. Truth Table

INPUT	OUTPUTS				
DI	DO+	DO-			
L	L	Н			
Н	Н	L			



9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

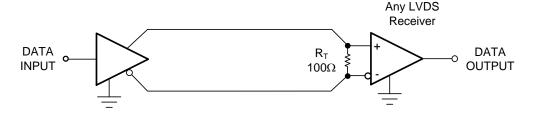
9.1 Application Information

The DS90LV027A has a flow-through pinout that allows for easy PCB layout. The LVDS signals on one side of the device easily allows for matching electrical lengths of the differential pair trace lines between the driver and the receiver as well as allowing the trace lines to be close together to couple noise as common-mode. Noise isolation is achieved with the LVDS signals on one side of the device and the TTL signals on the other side.

General application guidelines and hints for LVDS drivers and receivers may be found in the following application notes:

- LVDS Owner's Manual
- AN-808 Long Transmission Lines and Data Signal Quality
- AN-977 LVDS Signal Quality: Jitter Measurements Using Eye Patterns Test Report
- AN-971 An Overview of LVDS Technology
- AN-916 A Practical Guide To Cable Selection
- AN-805 Calculating Power Dissipation for Differential Line Drivers
- AN-903 A Comparison of Differential Termination Techniques

9.2 Typical Application



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Figure 19. LVDS Application Schematic

9.2.1 Design Requirements

When using LVDS devices, it is important to remember to specify controlled impedance PCB traces, cable assemblies, and connectors. All components of the transmission media must have a matched differential impedance of about 100 Ω . They must not introduce major impedance discontinuities. Balanced cables (for example, twisted pair) are usually better than unbalanced cables (ribbon cable) for noise reduction and signal quality.

Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode (not differential mode) noise which is rejected by the LVDS receiver.

For cable distances < 0.5 M, most cables can be made to work effectively. For distances 0.5 M \leq d \leq 10 M, CAT5 (Category 5) twisted pair cable works well, is readily available, and relatively inexpensive.



Typical Application (continued)

9.2.2 Detailed Design Procedure

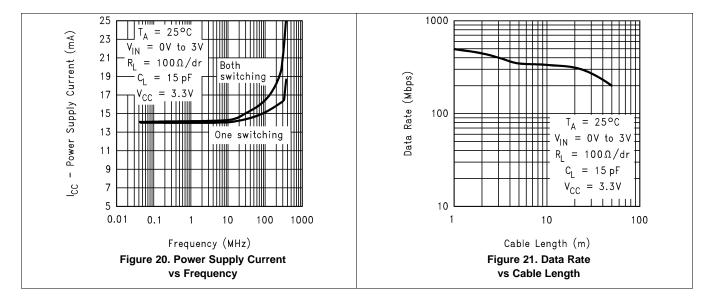
9.2.2.1 Probing LVDS Transmission Lines

Always use high impedance (>100 k Ω), low capacitance (<2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing gives deceiving results.

A pseudo-random bit sequence (PRBS) of 2^9 –1 bits was programmed into a function generator (Tektronix HFS9009) and connected to the driver inputs through 50- Ω cables and SMB connectors. An oscilloscope (Tektronix 11801B) was used to probe the resulting eye pattern, measured differentially at the input to the receiver. A 100- Ω resistor was used to terminate the pair at the far end of the cable. The measurements were taken at the far end of the cable, at the input of the receiver, and used for the jitter analysis for Figure 21. The frequency of the input signal was increased until the measured jitter (ttcs) equaled 20% with respect to the unit interval (ttui) for the particular cable length under test. Twenty percent jitter is a reasonable place to start with many system designs. The data used was NRZ. Jitter was measured at the 0-V differential voltage of the differential eye pattern.

The DS90LV027A and DS90LV028A can be evaluated using the new DS90LV047-048AEVM.

9.2.3 Application Curves



10 Power Supply Recommendations

Although the DS90LV027A draws very little power while at rest, at higher switching frequencies there is a dynamic current component which increases the overall power consumption. The DS90LV027A power supply connection must take this additional current consumption into consideration for maximum power requirements.

Product Folder Links: DS90LV027A

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11 Layout

11.1 Layout Guidelines

- Use at least 4 PCB layers (top to bottom); LVDS signals, ground, power, and TTL signals.
- Isolate TTL signals from LVDS signals, otherwise the TTL may couple onto the LVDS lines. Best practice is to place TTL and LVDS signals on different layers which are isolated by power or ground plane(s).
- Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

11.2 Layout Example

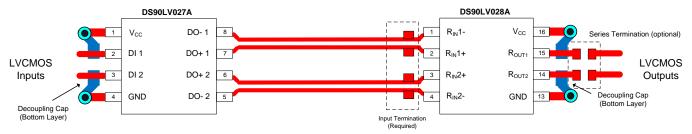


Figure 22. Simplified DS90LV027A and DS90LV028A Layout

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- LVDS Owner's Manual
- AN-808 Long Transmission Lines and Data Signal Quality
- AN-977 LVDS Signal Quality: Jitter Measurements Using Eye Patterns Test Report
- AN-971 An Overview of LVDS Technology
- AN-916 A Practical Guide To Cable Selection
- AN-805 Calculating Power Dissipation for Differential Line Drivers
- AN-903 A Comparison of Differential Termination Techniques

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community T's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
DS90LV027ATM/NOPB	Active	Production	SOIC (D) 8	95 TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LV27A TM
DS90LV027ATM/NOPB.A	Active	Production	SOIC (D) 8	95 TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LV27A TM
DS90LV027ATMX/NOPB	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LV27A TM
DS90LV027ATMX/NOPB.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LV27A TM

⁽¹⁾ Status: For more details on status, see our product life cycle.

- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.



PACKAGE OPTION ADDENDUM

www.ti.com 10-Nov-2025

PACKAGE MATERIALS INFORMATION

www.ti.com 23-May-2025

TAPE AND REEL INFORMATION



TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

A0	Dimension designed to accommodate the component width					
В0	Dimension designed to accommodate the component length					
K0	Dimension designed to accommodate the component thickness					
W	Overall width of the carrier tape					
P1	Pitch between successive cavity centers					

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	U	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90LV027ATMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

www.ti.com 23-May-2025



*All dimensions are nominal

Device	Device Package Type		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
DS90LV027ATMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0	

PACKAGE MATERIALS INFORMATION

www.ti.com 23-May-2025

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DS90LV027ATM/NOPB	D	SOIC	8	95	495	8	4064	3.05
DS90LV027ATM/NOPB.A	D	SOIC	8	95	495	8	4064	3.05



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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