

DS90LV018A 3V LVDS Single CMOS Differential Line Receiver

Check for Samples: DS90LV018A

FEATURES

- >400 Mbps (200 MHz) Switching Rates
- 50 ps Differential Skew (Typical)
- 2.5 ns Maximum Propagation Delay
- 3.3V Power Supply Design
- **Flow-Through Pinout**
- Power Down High Impedance on LVDS Inputs
- Low Power Design (18mW @ 3.3V Static)
- Interoperable with Existing 5V LVDS Networks
- Accepts Small Swing (350 mV Typical) **Differential Signal Levels**
- **Supports Open, Short and Terminated Input**
- Conforms to ANSI/TIA/EIA-644 Standard
- **Industrial Temperature Operating Range**
 - (-40°C to +85°C)
- Available in SOIC Package

DESCRIPTION

The DS90LV018A is a single CMOS differential line receiver designed for applications requiring ultra low power dissipation, low noise and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90LV018A accepts low voltage (350 mV typical) differential input signals and translates them to 3V CMOS output levels. The receiver also supports open, shorted and terminated (100 Ω) input fail-safe. The receiver output will be HIGH for all failsafe conditions. The DS90LV018A has a flow-through design for easy PCB layout.

The DS90LV018A and companion LVDS line driver provide a new alternative to high power PECL/ECL devices for high speed point-to-point interface applications.

Connection Diagram

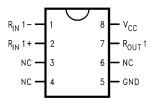
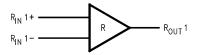


Figure 1. SOIC See Package Number D (R-PDSO-G8)

Functional Diagram



Truth Table

INPUTS	OUTPUT
[R _{IN} +] - [R _{IN} -]	R _{OUT}
V _{ID} ≥ 0.1V	Н
V _{ID} ≤ −0.1V	L
Full Fail-safe OPEN/SHORT or Terminated	Н

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

-0.3V to +4V
-0.3V to +3.9V
$-0.3V$ to $(V_{CC} + 0.3V)$
1025 mW
8.2 mW/°C above +25°C
−65°C to +150°C
+260°C
+150°C
≥ 7 kV
≥ 500 V

^{(1) &}quot;Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be specified. They are not meant to imply that the devices should be operated at these limits. Electrical Characteristics specifies conditions of device operation.

Recommended Operating Conditions

	Min	Тур	Max	Units
Supply Voltage (V _{CC})	+3.0	+3.3	+3.6	V
Receiver Input Voltage	GND		3.0	V
Operating Free Air				
Temperature (T _A)	-40	25	+85	°C



Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (1)(2)

Symbol	Parameter		Conditions	Pin	Min	Тур	Max	Units
V_{TH}	Differential Input High Threshold	V _{CM} = +1.2V,	0V, 3V ⁽³⁾	R _{IN} +,			+100	mV
V_{TL}	Differential Input Low Threshold			R _{IN} -	-100			mV
I _{IN}	Input Current	V _{IN} = +2.8V	V _{CC} = 3.6V or 0V		-10	±1	+10	μΑ
		$V_{IN} = 0V$			-10	±1	+10	μΑ
		$V_{IN} = +3.6V$	V _{CC} = 0V		-20		+20	μΑ
V_{OH}	Output High Voltage	I _{OH} = −0.4 mA	, V _{ID} = +200 mV	R _{OUT}	2.7	3.1		V
		$I_{OH} = -0.4 \text{ mA}$, Inputs terminated		2.7	3.1		V
		$I_{OH} = -0.4 \text{ mA}$, Inputs shorted		2.7	3.1		V
V _{OL}	Output Low Voltage	$I_{OL} = 2 \text{ mA}, V_{I}$	_D = −200 mV			0.3	0.5	V
Ios	Output Short Circuit Current	$V_{OUT} = 0V^{(4)}$			-15	-50	-100	mA
V_{CL}	Input Clamp Voltage	I _{CL} = −18 mA			-1.5	-0.8		V
I _{CC}	No Load Supply Current	Inputs Open		V _{CC}		5.4	9	mA

- (1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified (such as V_{ID}).
- All typicals are given for: $V_{CC} = +3.3V$ and $T_A = +25^{\circ}C$. V_{CC} is always higher than R_{IN} + and R_{IN} voltage. R_{IN} + and R_{IN} are allowed to have voltage range -0.05V to +3.05V. V_{ID} is not allowed to be greater than 100 mV when $V_{CM} = 0V$ or 3V.
- Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.

Switching Characteristics

 $V_{CC} = +3.3V \pm 10\%$, $T_A = -40$ °C to +85°C (1)(2)

Symbol	Parameter	Conditions	Min	Тур	Max	Units
t _{PHLD}	Differential Propagation Delay High to Low	C _L = 15 pF	1.0	1.6	2.5	ns
t _{PLHD}	Differential Propagation Delay Low to High	V _{ID} = 200 mV	1.0	1.7	2.5	ns
t _{SKD1}	Differential Pulse Skew t _{PHLD} - t _{PLHD} (3)	(Figure 2 and Figure 3)	0	50	400	ps
t _{SKD3}	Differential Part to Part Skew ⁽⁴⁾		0		1.0	ns
t _{SKD4}	Differential Part to Part Skew ⁽⁵⁾		0		1.5	ns
t _{TLH}	Rise Time			325	800	ps
t _{THL}	Fall Time			225	800	ps
f _{MAX}	Maximum Operating Frequency (6)		200	250		MHz

- (1) C_L includes probe and jig capacitance.
- Generator waveform for all tests unless otherwise specified: f = 1 MHz, $Z_O = 50\Omega$, t_r and t_f (0% to 100%) ≤ 3 ns for R_{IN} .
- t_{SKD1} is the magnitude difference in differential propagation delay time between the positive-going-edge and the negative-going-edge of
- t_{SKD3}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
- t_{SKD4}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over the recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max - Min| differential propagation delay.
- f_{MAX} generator input conditions: $t_r = t_f < 1$ ns (0% to 100%), 50% duty cycle, differential (1.05V to 1.35V peak to peak). Output criteria: 60%/40% duty cycle, V_{OL} (max 0.4V), V_{OH} (min 2.7V), load = 15 pF (stray plus probes).



PARAMETER MEASUREMENT INFORMATION

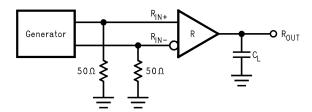


Figure 2. Receiver Propagation Delay and Transition Time Test Circuit

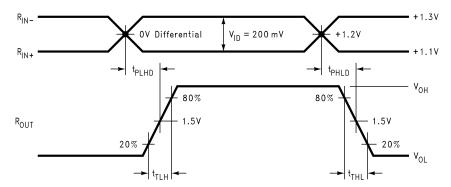


Figure 3. Receiver Propagation Delay and Transition Time Waveforms

TYPICAL APPLICATION

Balanced System

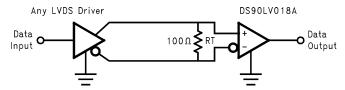


Figure 4. Point-to-Point Application

Submit Documentation Feedback



APPLICATION INFORMATION

General application guidelines and hints for LVDS drivers and receivers may be found in the following application notes: LVDS Owner's Manual (lit #550062-001), AN-808 (SNLA028), AN-1035 (SNOA355), AN-977 (SNLA166), AN-971 (SNLA165), AN-916 (SNLA219), AN-805 (SNOA233), AN-903 (SNLA034).

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in Figure 4. This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically the characteristic impedance of the media is in the range of 100Ω . A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the driver output (current mode) into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90LV018A differential line receiver is capable of detecting signals as low as 100 mV, over a ± 1 V common-mode range centered around +1.2V. This is related to the driver offset voltage which is typically +1.2V. The driven signal is centered around this voltage and may shift ± 1 V around this center point. The ± 1 V shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise, or a combination of the two. The AC parameters of both receiver input pins are optimized for a recommended operating input voltage range of 0V to +2.4V (measured from each pin to ground). The device will still operate for receivers input voltages up to V_{CC} , but exceeding V_{CC} will turn on the ESD protection circuitry which will clamp the bus voltages.

POWER DECOUPLING RECOMMENDATIONS

Bypass capacitors must be used on power pins. Use high frequency ceramic (surface mount is recommended) $0.1\mu\text{F}$ and $0.001\mu\text{F}$ capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed circuit board will improve decoupling. Multiple vias should be used to connect the decoupling capacitors to the power planes. A $10\mu\text{F}$ (35V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board between the supply and ground.

PC BOARD CONSIDERATIONS

Use at least 4 PCB board layers (top to bottom): LVDS signals, ground, power, TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL signals may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s).

Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

DIFFERENTIAL TRACES

Use controlled impedance traces which match the differential impedance of your transmission medium (ie. cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be < 10mm long). This will help eliminate reflections and ensure noise is coupled as commo-mode. In fact, we have seen that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result! (Note that the velocity of propagation, $v = c/E_r$ where c (the speed of light) = 0.2997mm/ps or 0.0118 in/ps). Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Copyright © 1998–2013, Texas Instruments Incorporated



Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

TERMINATION

Use a termination resistor which best matches the differential impedance or your transmission line. The resistor should be between 90Ω and 130Ω . Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work without resistor termination. Typically, connecting a single resistor across the pair at the receiver end will suffice.

Surface mount 1% - 2% resistors are the best. PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be < 10mm (12mm MAX).

FAIL-SAFE FEATURE

The LVDS receiver is a high gain, high speed device that amplifies a small differential signal (20mV) to CMOS logic levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal.

The receiver's internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated or shorted receiver inputs.

- 1. **Open Input Pins.** The DS90LV018A is a single receiver device. Do not tie the receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will ensure a HIGH, stable output state for open inputs.
- 2. Terminated Input. If the driver is disconnected (cable unplugged), or if the driver is in a power-off condition, the receiver output will again be in a HIGH state, even with the end of cable 100Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. Twisted pair cable will offer better balance than flat ribbon cable.
- 3. **Shorted Inputs.** If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0V differential input voltage, the receiver output will remain in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (GND to 2.4V). It is only supported with inputs shorted and no external common-mode voltage applied.

External lower value pull up and pull down resistors (for a stronger bias) may be used to boost fail-safe in the presence of higher noise levels. The pull up and pull down resistors should be in the $5k\Omega$ to $15k\Omega$ range to minimize loading and waveform distortion to the driver. The common-mode bias point should be set to approximately 1.2V (less than 1.75V) to be compatible with the internal circuitry.

PROBING LVDS TRANSMISSION LINES

Always use high impedance (> $100k\Omega$), low capacitance (< 2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing will give deceiving results.

CABLES AND CONNECTORS, GENERAL COMMENTS

When choosing cable and connectors for LVDS it is important to remember:

Use controlled impedance media. The cables and connectors you use should have a matched differential impedance of about 100Ω . They should not introduce major impedance discontinuities.

Balanced cables (e.g. twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation a common-mode (not differential mode) noise which is rejected by the receiver.

For cable distances < 0.5M, most cables can be made to work effectively. For distances $0.5M \le d \le 10M$, CAT 3 (category 3) twisted pair cable works well, is readily available and relatively inexpensive.

www.ti.com

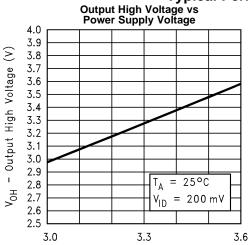
Pin Descriptions

Pin No.	Name	Description				
1	R _{IN} -	nverting receiver input pin				
2	R _{IN} +	lon-inverting receiver input pin				
7	R _{OUT}	Receiver output pin				
8	V _{CC}	Power supply pin, +3.3V ± 0.3V				
5	GND	Ground pin				
3, 4, 6	NC	No connection				

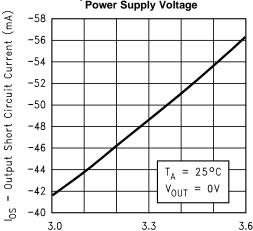
3.6



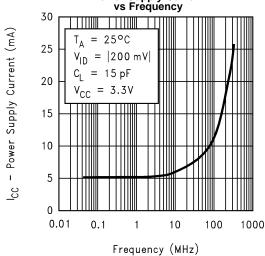


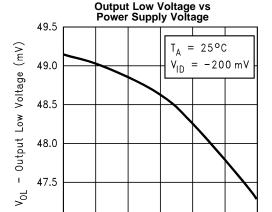






V_{CC} - Power Supply Voltage (V) Power Supply Current



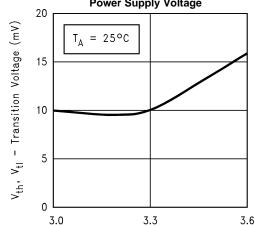


47.0

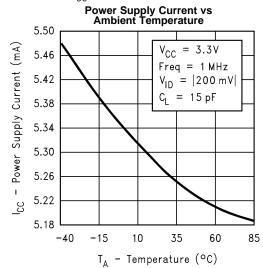
3.0

V_{CC} - Power Supply Voltage (V) Differential Transition Voltage vs Power Supply Voltage

3.3



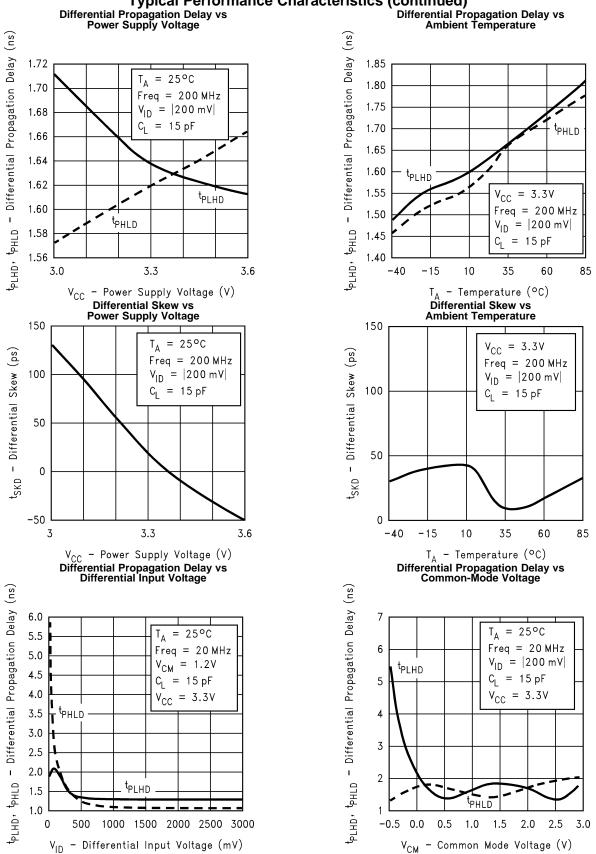
V_{CC} - Power Supply Voltage (V)



Submit Documentation Feedback

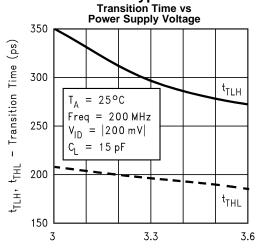


Typical Performance Characteristics (continued)

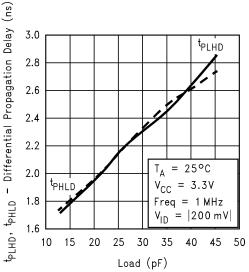




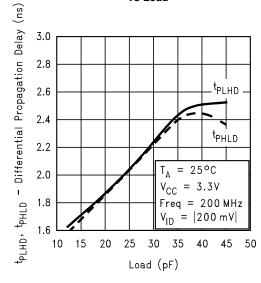


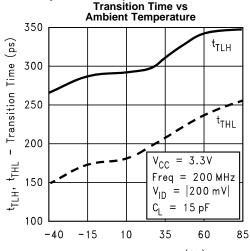


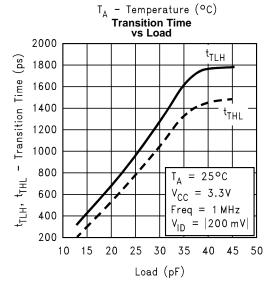
V_{CC} - Power Supply Voltage (V) **Differential Propagation Delay**vs Load

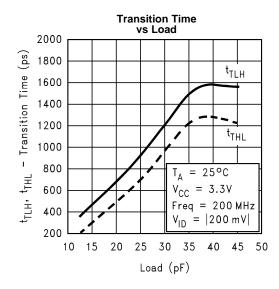


Differential Propagation Delay vs Load













REVISION HISTORY

Cł	hanges from Revision C (April 2013) to Revision D	Pa	ge
•	Changed layout of National Data Sheet to TI format		10

www.ti.com 11-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
DS90LV018ATM/NOPB	Active	Production	SOIC (D) 8	95 TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	90LV0 18ATM
DS90LV018ATM/NOPB.B	Active	Production	SOIC (D) 8	95 TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	90LV0 18ATM
DS90LV018ATMX/NOPB	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	90LV0 18ATM
DS90LV018ATMX/NOPB.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	90LV0 18ATM

⁽¹⁾ Status: For more details on status, see our product life cycle.

- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.



PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2025

PACKAGE MATERIALS INFORMATION

www.ti.com 23-May-2025

TAPE AND REEL INFORMATION



TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	U	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90LV018ATMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 23-May-2025



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90LV018ATMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

PACKAGE MATERIALS INFORMATION

www.ti.com 23-May-2025

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DS90LV018ATM/NOPB	D	SOIC	8	95	495	8	4064	3.05
DS90LV018ATM/NOPB.B	D	SOIC	8	95	495	8	4064	3.05



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025