

DS90LV017A LVDS Single High Speed Differential Driver

Check for Samples: DS90LV017A

FEATURES

- >600 Mbps (300 MHz) Switching Rates
- 0.3 ns Typical Differential Skew
- 0.7 ns Maximum Differential Skew
- 1.5 ns Maximum Propagation Delay
- 3.3V Power Supply Design
- ±355 mV Differential Signaling
- Low Power Dissipation (23 mW @ 3.3V Static)
- Flow-Through Design Simplifies PCB Layout
- Interoperable with Existing 5V LVDS Devices
- Power Off Protection (Outputs in High Impedance)
- Conforms to TIA/EIA-644 Standard
- 8-Lead SOIC Package Saves Space
- Industrial Temperature Operating Range
 - (-40°C to +85°C)

DESCRIPTION

The DS90LV017A is a single LVDS driver device optimized for high data rate and low power applications. The DS90LV017A is a current mode driver allowing power dissipation to remain low even at high frequency. In addition, the short circuit fault current is also minimized. The device is designed to support data rates in excess of 600Mbps (300MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The device is in a 8-lead SOIC package. The DS90LV017A has a flow-through design for easy PCB layout. The differential driver outputs provides low EMI with its typical low output swing of 355 mV. The DS90LV017A can be paired with its companion single line receiver, the DS90LV018A, or with any of TI's LVDS receivers, to provide a high-speed point-to-point LVDS interface.

Connection Diagram

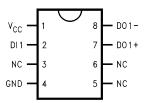
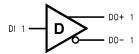


Figure 1. Dual-In-Line See Package Number D (R-PDSO-G8)

Functional Diagram





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AA.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



Absolute Maximum Ratings(1)

| Supply Voltage (V _{CC}) | -0.3V to +4V | |
|---|----------------------------|-----------------------|
| Input Voltage (DI) | -0.3V to +3.6V | |
| Output Voltage (DO±) | | -0.3V to +3.9V |
| Mariana Barlana Barra Biarinatian @ 10500 | D Package | 1190 mW |
| Maximum Package Power Dissipation @ +25°C | Derate D Package | 9.5 mW/°C above +25°C |
| Storage Temperature Range | | −65°C to +150°C |
| Lead Temperature Range Soldering (4 sec.) | | +260°C |
| | (HBM 1.5 kΩ, 100 pF) | ≥ 8kV |
| FCD Deticate | (EIAJ 0 Ω, 200 pF) | ≥ 1000V |
| ESD Ratings | (CDM) | ≥ 1000V |
| | (IEC direct 330 Ω, 150 pF) | ≥ 4kV |

[&]quot;Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. Electrical Characteristics specifies conditions of device operation.

Recommended Operating Conditions

| | Min | Тур | Max | Units |
|-----------------------------------|-----|-----|-----|-------|
| Supply Voltage (V _{CC}) | 3.0 | 3.3 | 3.6 | V |
| Temperature (T _A) | -40 | 25 | +85 | °C |

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (1)(2)(3)

| Symbol | Parameter | | Conditions | Pin | Min | Тур | Max | Units |
|------------------|----------------------------------|---------------------------|--|-----------------|-------|--------------|----------|-------|
| DIFFEREN | ITIAL DRIVER CHARACTERISTIC | s | | | | | • | |
| V _{OD} | Output Differential Voltage | $R_L = 100\Omega$ | | DO+, | 250 | 355 | 450 | mV |
| ΔV_{OD} | V _{OD} Magnitude Change | (Figure 2) | | DO- | | 1 | 35 | mV |
| V _{OH} | Output High Voltage | | | | | 1.4 | 1.6 | V |
| V _{OL} | Output Low Voltage | | | | 0.9 | 1.1 | | V |
| Vos | Offset Voltage | | | | 1.125 | 1.2 | 1.375 | V |
| ΔV _{OS} | Offset Magnitude Change | | | | 0 | 3 | 25 | mV |
| I _{OXD} | Power-off Leakage | $V_{OUT} = V_{CC}$ o | $V_{OUT} = V_{CC}$ or GND, $V_{CC} = 0V$ | | | ±1 | ±10 | μΑ |
| I _{OSD} | Output Short Circuit Current | | | | | - 5.7 | -8 | mA |
| V _{IH} | Input High Voltage | | | DI | 2.0 | | V_{CC} | V |
| V_{IL} | Input Low Voltage | | | | GND | | 0.8 | V |
| I _{IH} | Input High Current | V _{IN} = 3.3V or | 2.4V | | | ±2 | ±10 | μΑ |
| I _{IL} | Input Low Current | V _{IN} = GND or | 0.5V | | | ±1 | ±10 | μΑ |
| V_{CL} | Input Clamp Voltage | I _{CL} = −18 mA | I _{CL} = −18 mA | | -1.5 | -0.6 | | V |
| I _{CC} | Power Supply Current | No Load | $V_{IN} = V_{CC}$ or GND | V _{CC} | | 5 | 8 | mA |
| | | $R_L = 100\Omega$ | | | | 7 | 10 | mA |

⁽¹⁾ Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground

except V_{OD} . All typicals are given for: V_{CC} = +3.3V and T_A = +25°C. The DS90LV017A is a current mode device and only function with datasheet specification when a resistive load is applied to the drivers outputs.



Switching Characteristics

Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified (1)(2)(3)(4)

| Symbol | Parameter | Conditions | Min | Тур | Max | Units | | | | | | |
|-------------------|---|--------------------------------|-----|-----|-----|-------|--|--|--|--|--|--|
| DIFFEREN | FFERENTIAL DRIVER CHARACTERISTICS | | | | | | | | | | | |
| t _{PHLD} | Differential Propagation Delay High to Low | $R_L = 100\Omega, C_L = 15 pF$ | 0.3 | 0.8 | 1.5 | ns | | | | | | |
| t _{PLHD} | Differential Propagation Delay Low to High | (Figure 3 and Figure 4) | 0.3 | 1.1 | 1.5 | ns | | | | | | |
| t _{SKD1} | Differential Pulse Skew t _{PHLD} - t _{PLHD} ⁽⁵⁾ | | 0 | 0.3 | 0.7 | ns | | | | | | |
| t _{SKD3} | Differential Part to Part Skew ⁽⁶⁾ | | 0 | | 1.0 | ns | | | | | | |
| t _{SKD4} | Differential Part to Part Skew ⁽⁷⁾ | | 0 | | 1.2 | ns | | | | | | |
| t _{TLH} | Transition Low to High Time | | 0.2 | 0.5 | 1.0 | ns | | | | | | |
| t _{THL} | Transition High to Low Time | | 0.2 | 0.5 | 1.0 | ns | | | | | | |
| f _{MAX} | Maximum Operating Frequency ⁽⁸⁾ | | | 350 | | MHz | | | | | | |

- (1) All typicals are given for: $V_{CC} = +3.3V$ and $T_A = +25$ °C.
- (2) These parameters are ensured by design. The limits are based on statistical analysis of the device performance over PVT (process, voltage, temperature) ranges.
- C_L includes probe and fixture capacitance.
- (4) Generator waveform for all tests unless otherwise specified: f = 1 MHz, $Z_0 = 50\Omega$, $t_r \le 1$ ns, $t_f \le 1$ ns (10%-90%).
- (5) t_{SKD1}, |t_{PHLD} t_{PLHD}|, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
- (6) t_{SKD3}, Differential Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
- (7) t_{SKD4}, part to part skew, is the differential channel to channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max Min| differential propagation delay.
- (8) f_{MAX} generator input conditions: $t_r = t_f < 1$ ns (0% to 100%), 50% duty cycle, 0V to 3V. Output criteria: duty cycle = 45%/55%, $V_{OD} > 250 \text{mV}$

Parameter Measurement Information

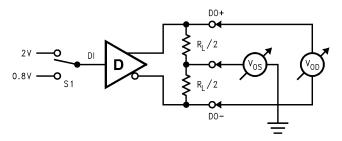


Figure 2. Differential Driver DC Test Circuit

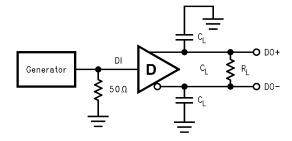


Figure 3. Differential Driver Propagation Delay and Transition Time Test Circuit

Product Folder Links: DS90LV017A

Parameter Measurement Information (continued)

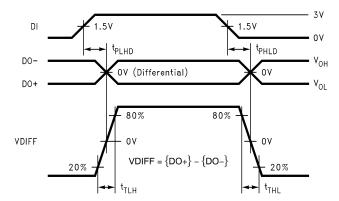


Figure 4. Differential Driver Propagation Delay and Transition Time Waveforms

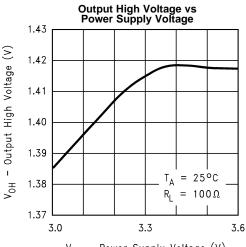
APPLICATION INFORMATION

Table 1. Device Pin Descriptions

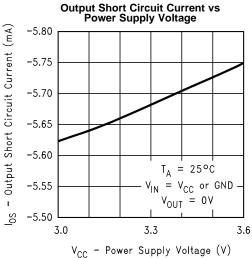
| | | · | | | | | |
|---------|-----------------|---|--|--|--|--|--|
| Pin# | Name | Description | | | | | |
| 2 | DI1 | TTL/CMOS driver input pins | | | | | |
| 7 | DO1+ | Non-inverting driver output pin | | | | | |
| 8 | DO1- | verting driver output pin | | | | | |
| 4 | GND | Ground pin | | | | | |
| 1 | V _{CC} | Positive power supply pin, +3.3V ± 0.3V | | | | | |
| 3, 5, 6 | NC | No connect | | | | | |



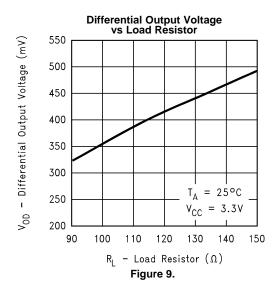
Typical Performance Curves

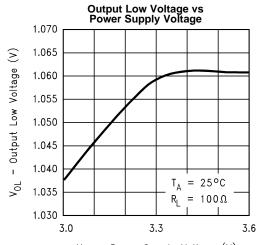


- Power Supply Voltage (V) Figure 5.

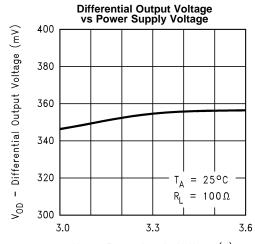


- Power Supply Voltage (V) Figure 7.

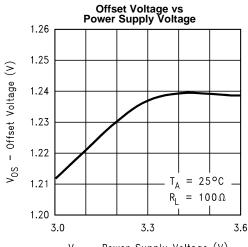




- Power Supply Voltage (V) Figure 6.



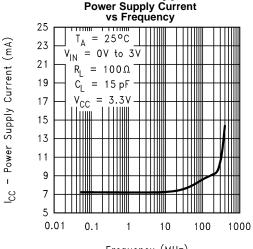
- Power Supply Voltage (V) Figure 8.



- Power Supply Voltage (V) v_{cc} Figure 10.



Typical Performance Curves (continued)



Frequency (MHz) Figure 11.

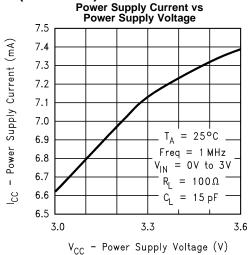


Figure 12.

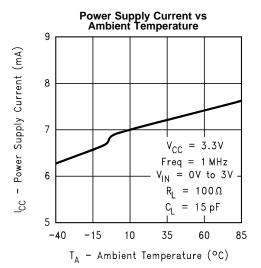
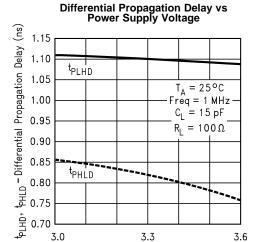
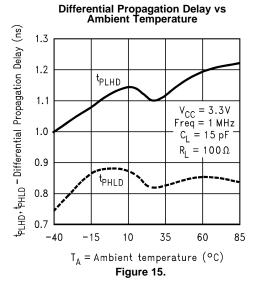


Figure 13.



 V_{CC} - Power Supply Voltage (V)

3.6



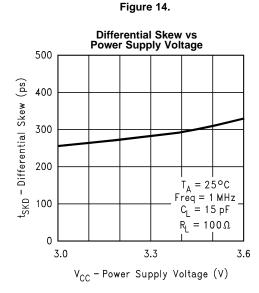
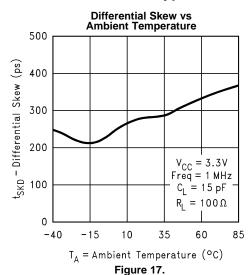
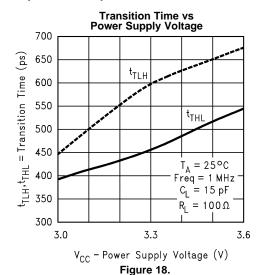


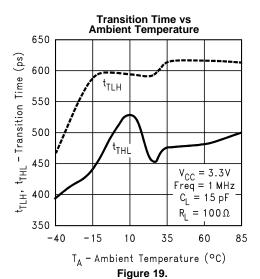
Figure 16.



Typical Performance Curves (continued)







SNLS022C - MARCH 2000-REVISED APRIL 2013



REVISION HISTORY

| Cł | hanges from Revision B (April 2013) to Revision C | Page |
|----|--|------|
| • | Changed layout of National Data Sheet to TI format | |

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PACKAGING INFORMATION

| Orderable part number | Status | Material type | Package Pins | Package qty Carrier | RoHS | Lead finish/ Ball material | MSL rating/ Peak reflow | Op temp (°C) | Part marking (6) |
|-----------------------|--------|---------------|----------------|-----------------------|------------|-------------------------------|----------------------------|--------------|------------------|
| | | | | | | (4) | (5) | | |
| DS90LV017ATM/NOPB | Active | Production | SOIC (D) 8 | 95 TUBE | JBE Yes SN | | Level-1-260C-UNLIM | -40 to 85 | LV17A TM |
| DS90LV017ATM/NOPB.A | Active | Production | SOIC (D) 8 | 95 TUBE | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | LV17A TM |
| DS90LV017ATM/NOPB.B | Active | Production | SOIC (D) 8 | 95 TUBE | - | Call TI | Call TI | -40 to 85 | |
| DS90LV017ATMX/NOPB | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | SN | SN Level-1-260C-UNLIM | | LV17A TM |
| DS90LV017ATMX/NOPB.A | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | LV17A TM |
| DS90LV017ATMX/NOPB.B | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | - | Call TI | Call TI | -40 to 85 | |

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





| A0 | Dimension designed to accommodate the component width |
|----|---|
| В0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Pack Typ | _ | Package Drawing | l . | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|-------------|---|--------------------|-----|------|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| DS90LV017ATMX/N | NOPB SO | С | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) | |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|--|
| DS90LV017ATMX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 | |

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| DS90LV017ATM/NOPB | D | SOIC | 8 | 95 | 495 | 8 | 4064 | 3.05 |
| DS90LV017ATM/NOPB.A | D | SOIC | 8 | 95 | 495 | 8 | 4064 | 3.05 |



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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