











DRV8837C

SLVSD61A - JULY 2016-REVISED JULY 2016

DRV8837C 1-A Low-Voltage H-Bridge Driver

1 Features

- H-Bridge Motor Driver
 - Drives a DC Motor or Other Loads
 - Low MOSFET On-Resistance: HS + LS 1 Ω
- 1-A Maximum Drive Current
- 0- to 11-V Operating Supply-Voltage Range
- Standard PWM Interface (IN1/IN2)
- Low-Power Sleep Mode With 120-nA Maximum Sleep Current
 - nSLEEP pin
- · Small Package and Footprint
 - 8 WSON (With Thermal Pad)
 - $-2.0 \times 2.0 \text{ mm}$
- Protection Features
 - VCC Undervoltage Lockout (UVLO)
 - Overcurrent Protection (OCP)
 - Thermal Shutdown (TSD)

2 Applications

- Cameras
- DSLR Lenses
- Consumer Products
- Toys
- Robotics
- Medical Devices

3 Description

The DRV8837C device provides an integrated motor driver solution for cameras, consumer products, toys, and other low-voltage or battery-powered motion control applications. The device can drive one DC motor or other devices like solenoids. The output driver block consists of N-channel power MOSFETs configured as an H-bridge to drive the motor winding. An internal charge pump generates needed gate drive voltages.

The DRV8837C device can supply up to 1 A of output current. The device operates on a motor power supply voltage from 0 to 11 V, and control logic can operate on 1.8-V to 5-V rails.

The DRV8837C device has a PWM (IN/IN) input interface.

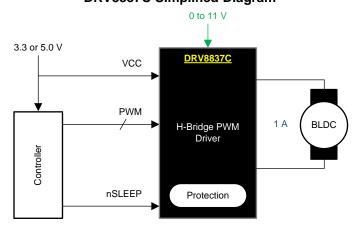
Internal shutdown functions are provided for overcurrent protection, short circuit protection, undervoltage lockout, and overtemperature.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8837C	WSON (8)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

DRV8837C Simplified Diagram



Copyright © 2016, Texas Instruments Incorporated



Table of Contents

1	Features 1	8 Application and Implementation 11
2	Applications 1	8.1 Application Information 11
3	Description 1	8.2 Typical Application 11
4	Revision History2	9 Power Supply Recommendations 12
5	Pin Configuration and Functions3	9.1 Bulk Capacitance 12
6	Specifications4	10 Layout 14
•	6.1 Absolute Maximum Ratings 4	10.1 Layout Guidelines 14
	6.2 ESD Ratings	10.2 Layout Example 14
	6.3 Recommended Operating Conditions	10.3 Power Dissipation
	6.4 Thermal Information	11 Device and Documentation Support 15
	6.5 Electrical Characteristics5	11.1 Documentation Support
	6.6 Timing Requirements	11.2 Receiving Notification of Documentation Updates 15
	6.7 Typical Characteristics	11.3 Community Resources
7	Detailed Description 8	11.4 Trademarks 15
	7.1 Overview 8	11.5 Electrostatic Discharge Caution 15
	7.2 Functional Block Diagram 8	11.6 Glossary 15
	7.3 Feature Description	12 Mechanical, Packaging, and Orderable
	7.4 Device Functional Modes	Information 15

4 Revision History

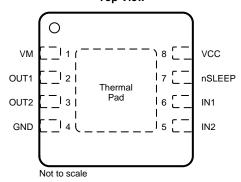
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2016) to Revision A			
•	Changed the device status from Product Preview to Production Data	1	



5 Pin Configuration and Functions

DSG Package 8-Pin WSON With Exposed Thermal Pad Top View



Pin Functions

	T III T GIICGOIIS					
F	PIN	TYPE	DESCRIPTION			
NAME NO.		IIFE	DESCRIPTION			
POWER AND	POWER AND GROUND					
GND	4	PWR	Device ground This pin must be connected to the PCB ground.			
VCC	8	PWR	Logic power supply Bypass this pin to the GND pin with a 0.1-µF ceramic capacitor rated for VCC.			
VM	1	PWR	Motor power supply Bypass this pin to the GND pin with a 0.1-μF ceramic capacitor rated for VM.			
CONTROL						
IN1	6	I	IN1 input			
IN2	5	I	IN2 input			
nSLEEP	Sleep mode input SLEEP 7 I When this pin is in logic low, the device enters low-power sleep mode. The device operates normally when this pin is logic high. The pin has an internal pulldown resistor to GND.		When this pin is in logic low, the device enters low-power sleep mode. The device operates			
OUTPUT						
OUT1	2	0	Motor output			
OUT2	3	0	Connect this pin to the motor winding.			



6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)(2)

		MIN	MAX	UNIT
Motor power-supply voltage	VM	-0.3	12	V
Logic power-supply voltage	V _{CC}	-0.3	7	V
Control pin voltage	IN1, IN2, nSLEEP	-0.5	7	V
Peak drive current OUT1, OUT2 Internally limited		y limited	Α	
Operating virtual junction temperature, T _J		-40	150	°C
Storage temperature, T _{stq}		-60	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V	Electrostatic	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
V _(ESD)	discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VM}	Motor power-supply voltage	0	11	V
V _{CC}	Logic power-supply voltage	1.8	7	V
I _{OUT}	Motor peak current	0	1	Α
f _{PWM}	Externally applied PWM frequency	0	250	kHz
V_{LOGIC}	Logic level input voltage	0	5.5	V
T _A	Operating ambient temperature	-40	85	°C

6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

		DRV8837C	
	THERMAL METRIC (1)	DSG (WSON)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.2	°C/W
ΨЈТ	Junction-to-top characterization parameter	1.6	°C/W
ΨЈВ	Junction-to-board characterization parameter	32.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.8	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

⁽²⁾ All voltage values are with respect to network ground pin.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



6.5 Electrical Characteristics

 $T_A = 25$ °C, over recommended operating conditions unless otherwise noted

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER	SUPPLIES (VM, V _{CC})	<u>'</u>	1			
V_{VM}	VM operating voltage		0		11	V
	VAA an audina a sunah asunah	V _{VM} = 5 V; V _{CC} = 3 V; No PWM		40	100	μА
I _{VM}	VM operating supply current	$V_{VM} = 5 \text{ V}; V_{CC} = 3 \text{ V};$ 50 kHz PWM		0.8	1.5	mA
I_{VMQ}	VM sleep mode supply current	V _{VM} = 5 V; V _{CC} = 3 V; nSLEEP = 0		30	95	nA
V _{CC}	V _{CC} operating voltage		1.8		7	V
	V apporating aupply aurrent	$V_{VM} = 5 \text{ V}; V_{CC} = 3 \text{ V};$ No PWM		300	500	μΑ
I _{vcc}	V _{CC} operating supply current	V _{VM} = 5 V; V _{CC} = 3 V; 50 kHz PWM		0.7	1.5	mA
I _{vccq}	V _{CC} sleep mode supply current	V _{VM} = 5 V; V _{CC} = 3 V; nSLEEP = 0		5	25	nA
CONTRO	OL INPUTS (IN1/PH, IN2/EN, nSLEE	EP)				
V _{IL}	Input logic-low voltage			0	.25 × V _{CC}	V
V _{IH}	Input logic-high voltage		0.5 × V _{CC}			V
V _{HYS}	Input logic hysteresis		0	.08 × V _{CC}		V
I _{IL}	Input logic-low current	$V_{INx} = 0 V$	-5		5	μΑ
I _{IH}	Input logic-high current	$V_{INx} = 3.3 \text{ V}$			50	μΑ
R _{PD}	Pulldown resistance			100		kΩ
MOTOR	DRIVER OUTPUTS (OUT1, OUT2)	·	•			
R _{DS(ON)}	HS + LS FET on-resistance	$V_{VM} = 5 \text{ V}; V_{CC} = 3.3 \text{ V};$ $I_{O} = 200 \text{ mA}; T_{J} = 25^{\circ}\text{C}$		1000		mΩ
I _{OFF}	Off-state leakage current	V _{OUTx} = 0 V	-200		200	nA
PROTEC	CTION CIRCUITS					
\/	V undervoltage la decut	V _{CC} falling			1.7	V
V_{UVLO}	V _{CC} undervoltage lockout	V _{CC} rising			1.8	V
ОСР	Overcurrent protection trip level		1.2			Α
DEG	Overcurrent deglitch time			1		μS
t _{RETRY}	Overcurrent retry time			1		ms
T _{TSD} (1)	Thermal shutdown temperature	Die temperature T _J	150	160	180	°C

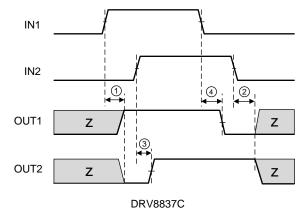
⁽¹⁾ Not tested in production; limits are based on characterization data



6.6 Timing Requirements

 T_{A} = 25°C, V_{VM} = 5 V, V_{CC} = 3 V, RL = 20 Ω

NO.				MIN	MAX	UNIT
1	t ₇	Output enable time			300	ns
2	t ₈	Output disable time			300	ns
3	t ₉	Delay time, INx high to OUTx high	Can Figure 4		160	ns
4	t ₁₀	Delay time, INx low to OUTx low	See Figure 1.		160	ns
5	t ₁₁	Output rise time		20	188	ns
6	t ₁₂	Output fall time		20	188	ns
_	t _{wake}	Wake time, nSLEEP rising edge to part active			30	μS



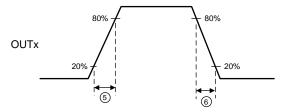
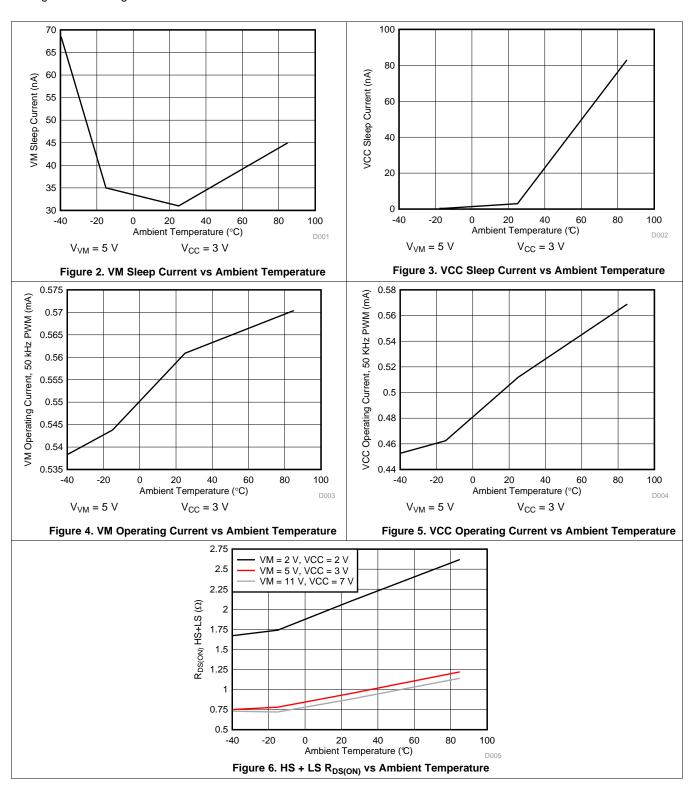


Figure 1. Input and Output Timing for DRV8837C



6.7 Typical Characteristics

Plots generated using characterization data.



Copyright © 2016, Texas Instruments Incorporated



7 Detailed Description

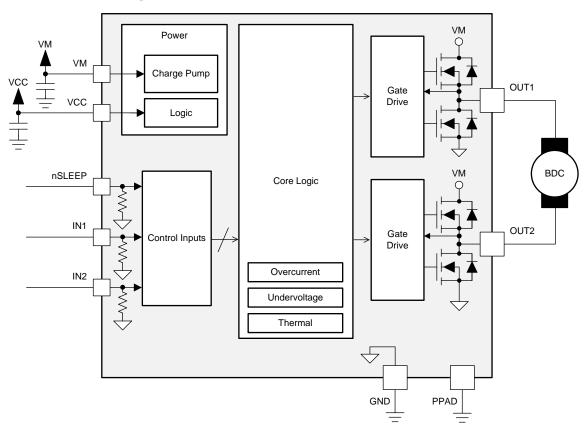
7.1 Overview

The DRV8837C device is an H-bridge driver that can drive one DC motor or other devices like solenoids. The outputs are controlled using a PWM interface (IN1/IN2).

A low-power sleep mode is included, which can be enabled using the nSLEEP pin.

This device greatly reduces the component count of motor driver systems by integrating the necessary driver FETs and FET control circuitry into a single device. In addition, the DRV8837C device adds protection features beyond traditional discrete implementations: undervoltage lockout, overcurrent protection, and thermal shutdown.

7.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated



7.3 Feature Description

7.3.1 Bridge Control

The DRV8837C device is controlled using a PWM input interface, also called an IN/IN interface. Each output is controlled by a corresponding input pin.

Table 1 shows the logic for the DRV8837C device.

nSLEEP IN2 OUT1 OUT2 **FUNCTION (DC MOTOR)** IN1 0 Χ Χ Ζ Ζ Coast Ζ 0 0 Ζ Coast 1 0 1 L Н Reverse L 1 1 0 Н Forward 1 1 1 L L **Brake**

Table 1. DRV8837C Device Logic

7.3.2 Sleep Mode

If the nSLEEP pin is brought to a logic-low state, the DRV8837C device enters a low-power sleep mode. In this state, all unnecessary internal circuitry is powered down.

7.3.3 Power Supplies and Input Pins

The input pins can be driven within the recommended operating conditions with or without the VCC, VM, or both power supplies present. No leakage current path exists to the supply. Each input pin has a weak pulldown resistor (approximately 100 $k\Omega$) to ground.

The VCC and VM supplies can be applied and removed in any order. When the VCC supply is removed, the device enters a low-power state and draws very little current from the VM supply. The VCC and VM pins can be connected together if the supply voltage is between 1.8 and 7 V.

The VM voltage supply does not have any undervoltage-lockout protection (UVLO). As long as $V_{CC} > 1.8 \text{ V}$, the internal device logic remains active which means that the VM pin voltage can drop to 0 V, however, the load may not be sufficiently driven at low VM voltages.

7.3.4 Protection Circuits

The DRV8837C is fully protected against VCC undervoltage, overcurrent, and overtemperature events.

VCC undervoltage lockout If at any time the voltage on the VCC pin falls below the undervoltage lockout threshold voltage, all FETs in the H-bridge are disabled. Operation resumes when the VCC pin voltage rises above the UVLO threshold.

Overcurrent protection (OCP) An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than t_{DEG}, all FETs in the H-bridge are disabled. Operation resumes automatically after t_{RETRY} has elapsed. Overcurrent conditions are detected on both the high-side and low-side devices. A short to the VM pin, GND, or from the OUT1 pin to theOUT2 pin results in an overcurrent condition.

Thermal shutdown (TSD) If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled. After the die temperature falls to a safe level, operation automatically resumes.

Table 2. Fault Behavior

FAULT	CONDITION	H-BRIDGE	RECOVERY
VCC undervoltage (UVLO)	VCC < 1.7 V	Disabled	VCC > 1.8 V
Overcurrent (OCP)	I _{OUT} > 1.2 A (MIN)	Disabled (retries automatically)	t _{RETRY} elapses
Thermal Shutdown (TSD)	$T_J > 150$ °C (MIN)	Disabled (retries automatically)	T _J < 150°C



7.4 Device Functional Modes

The DRV8837C device is active unless the nSLEEP pin is brought logic low. In sleep mode the H-bridge FETs are disabled Hi-Z. The DRV8837C device is brought out of sleep mode automatically if nSLEEP is brought logic high.

The H-bridge outputs are disabled during undervoltage lockout, overcurrent, and overtemperature fault conditions.

Table 3. Operation Modes

MODE	CONDITION	H-BRIDGE
Operating	nSLEEP pin = 1	Operating
Sleep mode	nSLEEP pin = 0	Disabled
Fault encountered	Any fault condition met	Disabled (retries automatically)



8 Application and Implementation

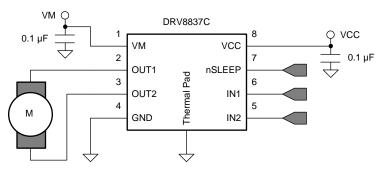
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8837C device is device is used to drive one DC motor or other devices like solenoids. The following design procedure can be used to configure the DRV8837C device.

8.2 Typical Application



Copyright © 2016, Texas Instruments Incorporated

Figure 7. Schematic of DRV8837C Application

8.2.1 Design Requirements

Table 4 lists the required parameters for a typical usage case.

Table 4. System Design Requirements

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor supply voltage	VM	9 V
Logic supply voltage	VCC	3.3 V
Target RMS current	I _{OUT}	0.8 A

8.2.2 Detailed Design Procedure

8.2.2.1 Motor Voltage

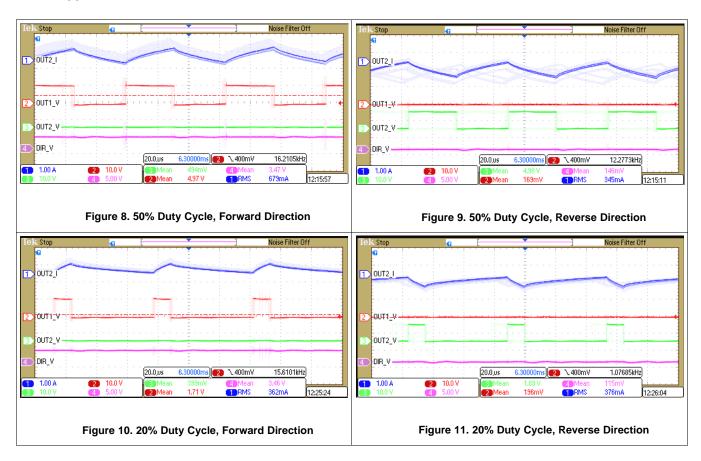
The appropriate motor voltage depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed dc motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

8.2.2.2 Low-Power Operation

When entering sleep mode, TI recommends setting all inputs as a logic low to minimize system power.



8.2.3 Application Curves



9 Power Supply Recommendations

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor-drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power-supply capacitance and ability to source current
- · The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed dc, brushless dc, stepper)
- · The motor braking method

The inductance between the power supply and motor drive system limits the rate at which current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate size of bulk capacitor.



Bulk Capacitance (continued)

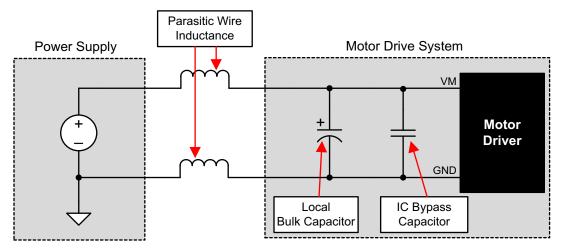


Figure 12. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply

Copyright © 2016, Texas Instruments Incorporated



10 Layout

10.1 Layout Guidelines

The VM and VCC pins should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1 µF rated for the VM and VCC supplies. These capacitors should be placed as close to the VM and VCC pins as possible with a thick trace or ground plane connection to the device GND pin. In addition bulk capacitance is required on the VM pin.

10.2 Layout Example

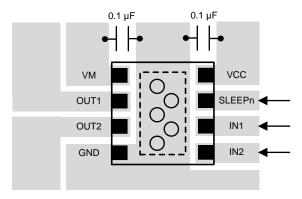


Figure 13. Simplified Layout Example

10.3 Power Dissipation

Power dissipation in the DRV8837C device is dominated by the power dissipated in the output FET resistance, or R_{DS(ON)}. Use Equation 1 to estimate the average power dissipation when running a brushed-DC motor.

$$P_{TOT} = R_{DS(ON)} \times (I_{OUT(RMS)})^2$$

where

- P_{TOT} is the total power dissipation
- R_{DS(ON)} is the resistance of the HS plus LS FETs
- I_{OUT(RMS)} is the RMS or DC output current being supplied to the load

(1)

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

NOTE

The value of R_{DS(ON)} increases with temperature, so as the device heats, the power dissipation increases.

The DRV8837C device has thermal shutdown protection. If the die temperature exceeds approximately 150°C, the device is disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.



11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Calculating Motor Driver Power Dissipation (SLVA504)
- DRV8837C Evaluation Module User's Guide (SLVUAS3)
- Understanding Motor Driver Current Ratings (SLVA505)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — TI Glossarv.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com 10-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
DRV8837CDSGR	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	837C
DRV8837CDSGR.B	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	837C
DRV8837CDSGRG4	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	837C
DRV8837CDSGRG4.B	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	837C
DRV8837CDSGT	Obsolete	Production	WSON (DSG) 8	-	-	Call TI	Call TI	-40 to 85	837C

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE MATERIALS INFORMATION

www.ti.com 15-Aug-2025

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8837CDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
DRV8837CDSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

www.ti.com 15-Aug-2025



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8837CDSGR	WSON	DSG	8	3000	182.0	182.0	20.0
DRV8837CDSGRG4	WSON	DSG	8	3000	210.0	185.0	35.0

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025