

DRV8351-SEP: 40V Three-Phase BLDC Gate Driver

1 Features

- 40V Three Phase Half-Bridge Gate driver
 - Drives N-Channel MOSFETs (NMOS)
 - Gate Driver Supply (GVDD): 5-15V
 - MOSFET supply (SHx) supports up to 40V
- Radiation Performance
 - SEL, SEB, and SET resistant up to LET = 43 MeV-cm2 /mg
 - SET and SEFI characterized up to LET = 43 MeV-cm2 /mg
 - TID assured for every wafer lot up to 30 krad(Si)
 - TID characterized up to 30 krad(Si)
 - Cross conduction event is observed during SEE and SEB. Refer to SEE report for more details.
- Space-enhanced plastic (space EP):
 - Controlled Baseline
 - One Assembly/Test Site
 - One Fabrication site
 - Extended Product Life Cycle
 - Product Traceability
- Integrated Bootstrap Diodes
- Supports Inverting and Non-Inverting INLx inputs
- Bootstrap gate drive architecture
 - 750mA source current
 - 1.5- sink current
- Low leakage current on SHx pins (<55µA)
- Absolute maximum BSTx voltage up to 57.5V
- Supports negative transients up to -22V on SHx
- Fixed deadtime insertion of 200nS
- Supports 3.3V and 5V logic inputs with 20V Abs
- 4nS typical propagation delay matching
- Compact TSSOP package
- Efficient system design with Power Blocks
- Integrated protection features
 - BST undervoltage lockout (BSTUV)
 - GVDD undervoltage (GVDDUV)

2 Applications

Supports Defense, Aerospace and Medical **Applications**

- Thruster Gimbal Mechanism
- Antenna Pointing Mechanism
- Reaction Wheel
- **Propellant Control Valve**

3 Description

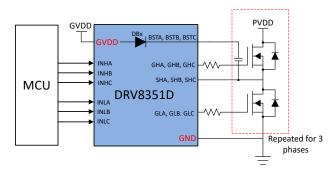
DRV8351-SEP is a three phase half-bridge gate driver, capable of driving high-side and low-side N-channel power MOSFETs. The DRV8351-SEPD generates the correct gate drive voltages using an integrated bootstrap diode and external capacitor for the high-side MOSFETs. GVDD is used to generate gate drive voltage for the low-side MOSFETs. The Gate Drive architecture supports peak up to 750mA source and 1.5A sink currents.

The phase pins SHx are able to tolerate significant negative voltage transients; while high side gate driver supply BSTx and GHx can support higher positive voltage transients (57.5V) abs max voltage which improve the robustness of the system. Small propagation delay and delay matching specifications minimize the dead-time requirement which further improves efficiency. Undervoltage protection is provided for both low and high sides through GVDD and BST undervoltage lockout.

Device Information (1)

PART	PACKAGE	PACKAGE	BODY SIZE
NUMBER		SIZE ⁽²⁾	(NOM)
DRV8351DMP	TSSOP (20)	6.50mm ×	6.40mm ×
WTSEP		6.40mm	4.40mm
DRV8351DIMP	TSSOP (20)	6.50mm ×	6.40mm ×
WTSEP		6.40mm	4.40mm

- For all available packages, see the orderable addendum at the end of the data sheet.
- The package size (length × width) is a nominal value and (2) includes pins, where applicable.



Simplified Schematic for DRV8351-SEPD



Table of Contents

1 Features	7.3 Feature Description	12
2 Applications1	7.4 Device Functional Modes	14
3 Description	8 Application and Implementation	. 15
4 Device Comparison Table3	8.1 Application Information	. 15
5 Pin Configuration and Functions4	8.2 Typical Application	
6 Specifications6	8.3 Power Supply Recommendations	
6.1 Absolute Maximum Ratings6	8.4 Layout	. 18
6.2 ESD Ratings Comm6	9 Device and Documentation Support	
6.3 Recommended Operating Conditions6	9.1 Receiving Notification of Documentation Updates	
6.4 Thermal Information7	9.2 Support Resources	. 20
6.5 Electrical Characteristics7	9.3 Trademarks	.20
6.6 Timing Diagrams8	9.4 Electrostatic Discharge Caution	. 20
6.7 Typical Characteristics9	9.5 Glossary	
7 Detailed Description10	10 Revision History	
7.1 Overview10	11 Mechanical, Packaging, and Orderable	
7.2 Functional Block Diagram11	Information	. 20



4 Device Comparison Table

Device Variants	Package	Integrated Bootstrap Diode	GLx polarity with respect to INLx Input	Deadtime
DRV8351-SEPDI	20-Pin TSSOP	Yes	Inverted	Fixed
DRV8351-SEPD	20-FIII 1330F	Yes	Non-Inverted	Fixed



5 Pin Configuration and Functions

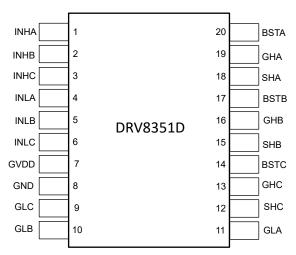


Figure 5-1. DRV8351-SEPD, DRV8351-SEPDI Package 20-Pin TSSOP Top View

Table 5-1. Pin Functions—20-Pin DRV8351-SEP Devices

PIN	ı	TVDE4	DESCRIPTION		
NAME	NO.	TYPE1	DESCRIPTION		
BSTA	20	0	Bootstrap output pin. Connect capacitor between BSTA and SHA		
BSTB	17	0	Bootstrap output pin. Connect capacitor between BSTB and SHB		
BSTC	14	0	Bootstrap output pin. Connect capacitor between BSTC and SHC		
GHA	19	0	High-side gate driver output. Connect to the gate of the high-side power MOSFET.		
GHB	16	0	High-side gate driver output. Connect to the gate of the high-side power MOSFET.		
GHC	13	0	High-side gate driver output. Connect to the gate of the high-side power MOSFET.		
GLA	11	0	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.		
GLB	10	0	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.		
GLC	9	0	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.		
INHA	1	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.		
INHB	2	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.		
INHC	3	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.		
INLA	4	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.		
INLB	5	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.		
INLC	6	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.		
GND	8	PWR	Device ground.		
SHA	18	I	High-side source sense input. Connect to the high-side power MOSFET source.		

Table 5-1. Pin Functions—20-Pin DRV8351-SEP Devices (continued)

PI	IN	TVDE4	PECCULATION
NAME	NO.	TYPE1	DESCRIPTION
SHB	15	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHC	12	I	High-side source sense input. Connect to the high-side power MOSFET source.
GVDD	7	PWR	Gate driver power supply input. Connect a X5R or X7R, GVDD-rated ceramic and greater then or equal to 10-uF local capacitance between the GVDD and GND pins.

1. PWR = power, I = input, O = output, NC = no connection



6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Gate driver regulator pin voltage	GVDD	-0.3	15	V
Bootstrap pin voltage	BSTx	-0.3	57.5	V
Bootstrap pin voltage	BSTx with respect to SHx	-0.3	15	V
Logic pin voltage	INHx, INLx	-0.3	V _{GVDD} +0.3	V
High-side gate drive pin voltage	GHx	-22	55	V
High-side gate drive pin voltage	GHx with respect to SHx	-0.3	15	V
Transient 500-ns high-side gate drive pin voltage	GHx with respect to SHx	-5	15	V
Low-side gate drive pin voltage	GLx	-0.3	V _{GVDD} +0.3	V
Transient 500-ns low-side gate drive pin voltage	GLx	-5	V _{GVDD} +0.3	V
High-side source pin voltage	SHx	-22	42.5	V
Ambient temperature, T _A		-55	125	°C
Junction temperature, T _J		-55	150	°C
Storage temperature, T _{stg}		-65	150	°C

⁽¹⁾ Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

6.2 ESD Ratings Comm

			VALUE	UNIT
V	Electrostatic	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000	\/
V _(ESD)	discharge	Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±250	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM MAX	UNIT
V_{GVDD}	Power supply voltage	GVDD	5	15	V
V _{SHx}	High-side source pin voltage	SHx	-2	40	V
V _{SHx}	Transient 2µs high-side source pin voltage	SHx	-22	40	V
V _{BST}	Bootstrap pin voltage	BSTx	5	55	V
V _{BST}	Bootstrap pin voltage	BSTx with respect to SHx	5	15	V
V _{IN}	Logic input voltage	INHx, INLx	0	GVDD	V
f _{PWM}	PWM frequency	INHx, INLx	0	100	kHz
V _{SHSL}	Slew rate on SHx pin			2	V/ns
C _{BOOT} (1)	Capacitor between BSTx and SHx			1	μF
T _A	Operating ambient temperature	•	-55	125	°C
TJ	Operating junction temperature		-55	150	°C

(1) Current flowing through boot diode (D_{BOOT}) needs to be limited for $C_{BOOT} > 1\mu F$

Product Folder Links: DRV8351-SEP



6.4 Thermal Information

		DRV8351-SEP	
	THERMAL METRIC ⁽¹⁾	PW (TSSOP)	UNIT
		20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97.4	°C/W
R ₀ JC(top)	Junction-to-case (top) thermal resistance	38.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	48.4	°C/W
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

 $4.8~V \le V_{GVDD} \le 20~V, -55^{\circ}C \le T_{J} \le 150^{\circ}C$ (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SU	PPLIES (GVDD, BSTx)					
	GVDD standby mode current	INHx = INLX = 0; V _{BSTx} = V _{GVDD}	400	800	1500	μA
I _{GVDD}	GVDD active mode current	INHx = INLX = Switching @20kHz; V _{BSTx} = V _{GVDD} ; NO FETs connected	400	825	1500	μA
IL _{BSx}	Bootstrap pin leakage current	V _{BSTx} = V _{SHx} = 40V; V _{GVDD} = 0V	2	7	13	μA
IL _{BS_TRAN}	Bootstrap pin active mode transient leakage current	INHx = Switching@20kHz	30	105	220	μΑ
IL _{BS_DC}	Bootstrap pin active mode leakage static current	INHx = High	30	85	150	μΑ
IL _{SHx}	High-side source pin leakage current	INHx = INLX = 0; V _{BSTx} - V _{SHx} = 12V; V _{SHx} = 0 to 40V	30	55	90	μΑ
LOGIC-LEV	EL INPUTS (INHx, INLx, MODE)					
V _{IL}	Input logic low voltage	INLx, INHx pins			8.0	V
V _{HYS}	Input hysteresis	INLx, INHx pins	40	100	260	mV
I _{IL_INLx}	INLx Input logic low current	V _{PIN} (Pin Voltage) = 0 V; INLx in non-inverting mode	-1	0	1	μΑ
I _{IH_INLx}	INLx Input logic high current	V _{PIN} (Pin Voltage) = 5 V; INLx in non-inverting mode	5	20	30	μA
I _{IL}	INHx Input logic low current	V _{PIN} (Pin Voltage) = 0 V;	-1	0	1	μΑ
I _{IH}	INHx Input logic high current	V _{PIN} (Pin Voltage) = 5 V;	5	20	30	μA
R _{PD_INHx}	INHx Input pulldown resistance	To GND	120	200	280	kΩ
R _{PD_INLx}	INLx Input pulldown resistance	To GND, INLx in non-inverting mode	120	200	280	kΩ
R _{PD_MODE}	MODE Input pulldown resistance	To GND	120	200	280	kΩ
GATE DRIV	ERS (GHx, GLx, SHx, SLx)					
V _{GHx_LO}	High-side gate drive low level voltage	I _{GLx} = -100 mA; V _{GVDD} = 12V; No FETs connected	0	0.15	0.35	V
V _{GHx_HI}	High-side gate drive high level voltage (V _{BSTx} - V _{GHx})	I _{GHx} = 100 mA; V _{GVDD} = 12V; No FETs connected	0.3	0.6	1.2	V
V _{GLx_LO}	Low-side gate drive low level voltage	I _{GLx} = -100 mA; V _{GVDD} = 12V; No FETs connected	0	0.15	0.35	V
V _{GLx_HI}	Low-side gate drive high level voltage (V _{GVDD} - V _{GHx})	I _{GHx} = 100 mA; V _{GVDD} = 12V; No FETs connected	0.3	0.6	1.2	V
I _{DRIVEP_HS}	High-side peak source gate current	GHx-SHx = 12V	400	750	1200	mA
I _{DRIVEN_HS}	High-side peak sink gate current	GHx-SHx = 0V	850	1500	2100	mA

4.8 V \leq V_{GVDD} \leq 20 V, -55° C \leq T_J \leq 150°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{DRIVEP_LS}	Low-side peak source gate current	GLx = 12V	400	750	1200	mA
I _{DRIVEN_LS}	Low-side peak sink gate current	GLx = 0V	850	1500	2100	mA
t _{PD}	Input to output propagation delay	INHx, INLx to GHx, GLx; $V_{GVDD} = V_{BSTx} - V_{SHx} > 8V$; SHx = 0V, No load on GHx and GLx	70	125	180	ns
t _{PD_match}	Matching propagation delay per phase	GHx turning OFF to GLx turning ON, GLx turning OFF to GHx turning ON; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V, No load on GHx and GLx	-30	±4	30	ns
${ m t}_{ m PD_match}$	Matching propagation delay phase to phase	GHx/GLx turning ON to GHy/GLy turning ON, GHx/GLx turning OFF to GHy/GLy turning OFF; $V_{GVDD} = V_{BSTx} - V_{SHx} > 8V$; SHx = 0V, No load on GHx and GLx	-30	±4	30	ns
t _{R_GLx}	GLx rise time (10% to 90%)	C_{LOAD} = 1000 pF; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V	10	24	50	ns
t _{R_GHx}	GHx rise time (10% to 90%)	C_{LOAD} = 1000 pF; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V	10	24	50	ns
t _{F_GLx}	GLx fall time (90% to 10%)	C _{LOAD} = 1000 pF; V _{GVDD} = V _{BSTx} - V _{SHx} > 8V; SHx = 0V	5	12	30	ns
t _{F_GHx}	GHx fall time (90% to 10%)	C _{LOAD} = 1000 pF; V _{GVDD} = V _{BSTx} - V _{SHx} > 8V; SHx = 0V	5	12	30	ns
t _{DEAD}	Gate drive dead time		150	215	280	ns
t _{PW_MIN}	Minimum input pulse width on INHx, INLx that changes the output on GHx, GLx		40	70	150	ns
BOOTSTRAP	DIODES					
\/	Postatran diada farward valtaga	I _{BOOT} = 100 μA	0.45	0.7	0.85	V
V_{BOOTD}	Bootstrap diode forward voltage	I _{BOOT} = 100 mA	2	2.3	3.1	V
R _{BOOTD}	Bootstrap dynamic resistance $(\Delta V_{BOOTD}/\Delta I_{BOOT})$	I _{BOOT} = 100 mA and 80 mA	11	15	25	Ω
PROTECTION	CIRCUITS					
\/	Gate Driver Supply undervoltage	Supply rising	4.45	4.6	4.7	V
V_{GVDDUV}	lockout (GVDDUV)	Supply falling	4.2	4.35	4.4	V
V _{GVDDUV_HYS}	Gate Driver Supply UV hysteresis	Rising to falling threshold	250	280	310	mV
t _{GVDDUV}	Gate Driver Supply undervoltage deglitch time		5	10	13	μs
V	Boot Strap undervoltage lockout (V _{BSTx} - V _{SHx})	Supply rising	3.6	4.2	4.8	V
V _{BSTUV}	Boot Strap undervoltage lockout (V _{BSTx} - V _{SHx})	Supply falling	3.5	4	4.5	V
V _{BSTUV_HYS}	Bootstrap UV hysteresis	Rising to falling threshold		200		mV
t _{BSTUV}	Bootstrap undervoltage deglitch time		6	10	22	μs

6.6 Timing Diagrams

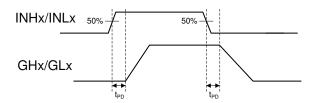


Figure 6-1. Propagation Delay(t_{PD})

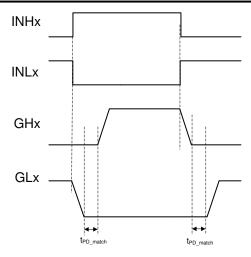
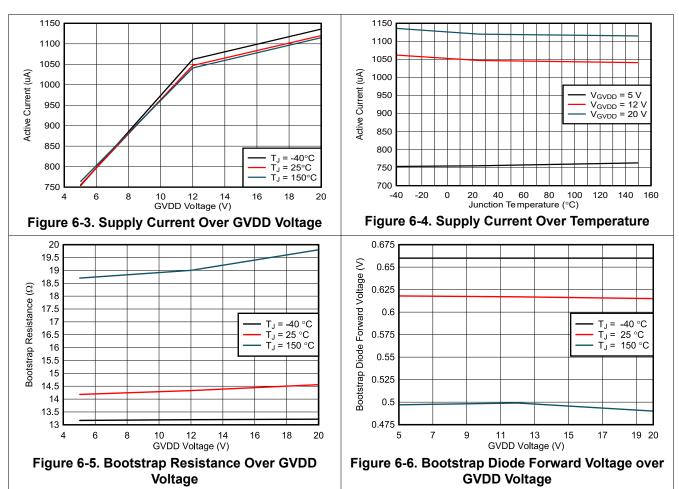


Figure 6-2. Propagation Delay Match (t_{PD_match})

6.7 Typical Characteristics





7 Detailed Description

7.1 Overview

The DRV8351-SEP family of devices are gate drivers for three-phase motor drive applications. These devices decrease system component count, saves PCB space and cost by integrating three independent half-bridge gate drivers and optional bootstrap diodes.

DRV8351-SEP supports external N-channel high-side and low-side power MOSFETs and can drive 750mA source, 1.5A sink peak currents with a total combined 30mA average output current. The DRV8351-SEP family of devices are available in 0.65mm pitch TSSOP surface-mount packages. The TSSOP body size is 6.5 × 4.4mm (0.65mm pin pitch) for the 20-pin package.

Submit Document Feedback



7.2 Functional Block Diagram

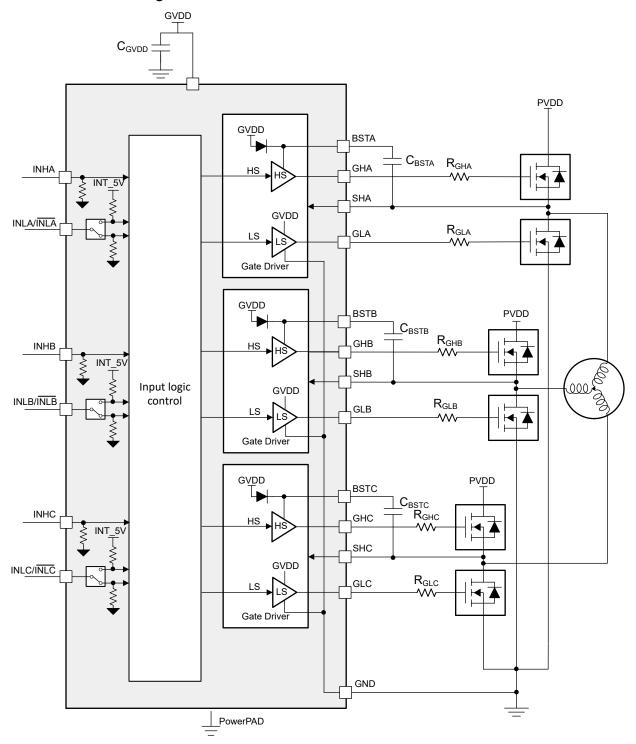


Figure 7-1. Block Diagram for DRV8351-SEPD

7.3 Feature Description

7.3.1 Three BLDC Gate Drivers

The DRV8351-SEP integrates three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. Input on GVDD provides the gate bias voltage for the low-side MOSFETs. The high voltage is generated using bootstrap capacitors and GVDD supply. The half-bridge gate drivers can be used in combination to drive a three-phase motor or separately to drive other types of loads.

7.3.1.1 Gate Driver Timings

7.3.1.1.1 Propagation Delay

The propagation delay time (t_{nd}) is measured as the time between an input logic edge to a detected output change. This time has two parts consisting of the input deglitcher delay and the delay through the analog gate drivers.

The input deglitcher prevents high-frequency noise on the input pins from affecting the output state of the gate drivers. The analog gate drivers have a small delay that contributes to the overall propagation delay of the device.

7.3.1.1.2 Dead Time and Cross-Conduction Prevention

In the DRV8351-SEP, high-side and low-side inputs operate independently, with an exception to prevent cross conduction when high and low side are turned ON at the same time. During normal operation, the DRV8351-SEP turns OFF high-side and low-side output to prevent shoot through when both high-side and low-side inputs are at logic HIGH at the same time.

In DRV8351D-SEP, fixed dead-time of 200ns (typical value) is inserted to prevent high and low side gate output turning ON at same time.

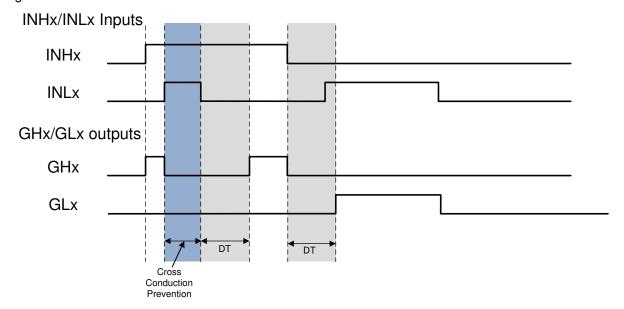


Figure 7-2. Cross Conduction Prevention and Dead Time Insertion

Note

DRV8351-SEP exhibited cross conduction during characterization of single-event effects (SEE) and single-even burnouts (SEB). Please refer to Single-Event Effects (SEE) report for more details.

7.3.1.2 Mode (Inverting and non inverting INLx)

The DRV8351-SEP has flexibility of accepting different kind of inputs on INLx. In DRV8351-SEP, there are different device options available for inverting and non inverting inputs (see Section 4).

Product Folder Links: DRV8351-SEP

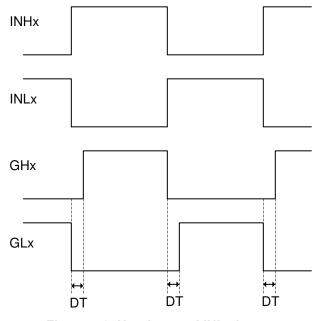


Figure 7-3. Non-Inverted INLx inputs

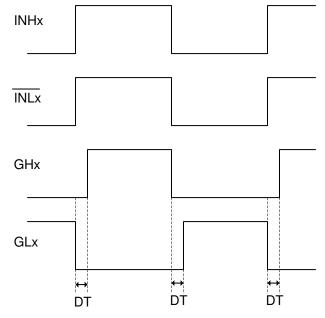
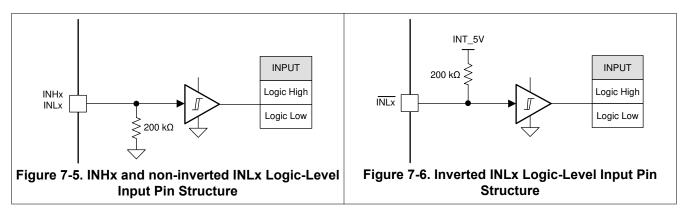


Figure 7-4. Inverted INLx inputs



7.3.2 Pin Diagrams

Figure 7-5 shows the input structure for the logic level pins INHx, INLx. INHx and non-inverted INLx has passive pull down, so when inputs are floating the output the gate driver is pulled low. Figure 7-6 shows the input structure for the inverted INLx pins. The inverted INLx has passive pull up, so when inputs are floating the output of the low-side gate driver is pulled low.



7.3.3 Gate Driver Protective Circuits

The DRV8351-SEP is protected against BSTx undervoltage and GVDD undervoltage events.

FAULT CONDITION **GATE DRIVER RECOVERY** Automatic: V_{BSTx} undervoltage $V_{BSTx} < V_{BSTUV}$ GHx - Hi-Z $V_{BSTx} > V_{BSTUV}$ and low to high (BSTUV) PWM edge detected on INHx pin GVDD undervoltage Automatic: Hi-Z $V_{GVDD} < V_{GVDDUV}$ (GVDDUV) $V_{GVDD} > V_{GVDDUV}$

Table 7-1. Fault Action and Response

7.3.3.1 V_{BSTx} Undervoltage Lockout (BSTUV)

The DRV8351-SEP has separate voltage comparator to detect undervoltage condition for each phases. If at any time the voltage on the BSTx pin falls lower than the V_{BSTUV} threshold, high side external MOSFETs of that particular phase is disabled by disabling (Hi-Z) GHx pin. Normal operation starts again when the BSTUV condition clears and low to high PWM edge is detected on INHx input of the same phase that BSTUV condition was detected. BSTUV protection ensures that high-side MOSFETs are not driven when the BSTx pins has lower value.

7.3.3.2 GVDD Undervoltage Lockout (GVDDUV)

If at any time the voltage on the GVDD pin falls lower than the V_{GVDDUV} threshold voltage, all of the external MOSFETs are disabled. Normal operation starts again when the GVDDUV condition clears. GVDDUV protection ensures that external MOSFETs are not driven when the GVDD input is at lower value.

7.4 Device Functional Modes

The DRV8351-SEP is in operating (active) mode, whenever the GVDD and BST pins are higher than the UV threshold (GVDD > V_{GVDDUV} and V_{BSTX} > V_{BSTUV}). In active mode, the gate driver output GHx and GLX will follow respective inputs INHx and INLx.

Product Folder Links: DRV8351-SEP



8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8351-SEP family of devices is primarily used in applications for three-phase brushless DC motor control. The design procedures in the Section 8.2 section highlight how to use and configure the DRV8351-SEP.



8.2 Typical Application

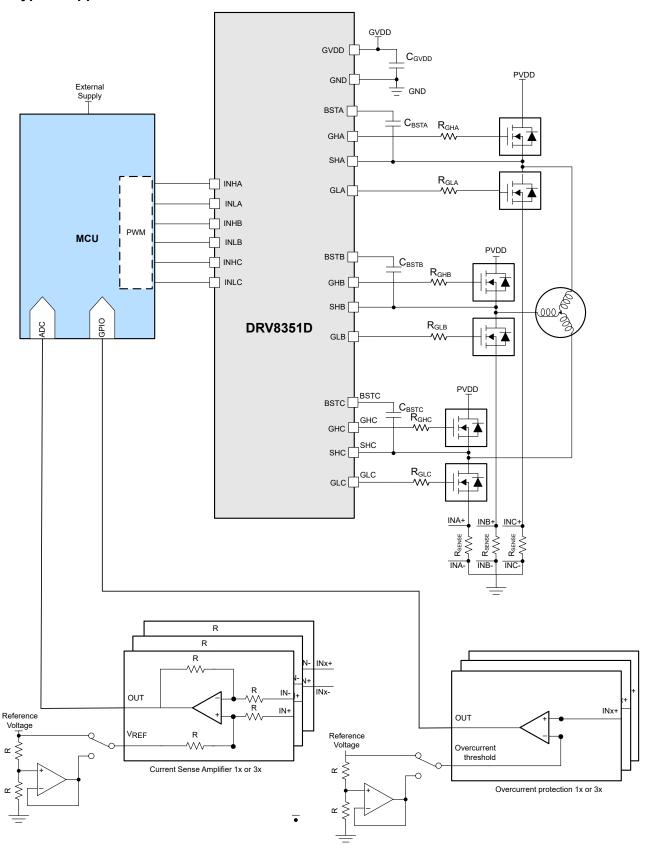


Figure 8-1. Application Schematic

Product Folder Links: DRV8351-SEP

Note

DRV8351-SEP exhibited cross conduction during characterization of single-event effects (SEE) and single-even burnouts (SEB). To detect overcurrent or short-circuit conditions on the external power MOSFETs, TI recommends to have overcurrent protection circuits such as voltage monitoring across drain and source of FETs or R_{sense}.

8.2.1 Design Requirements

Table 8-1 lists the example design input parameters for system design.

Table 8-1. Design Parameters

EXAMPLE DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
MOSFET	-	CSD19532Q5B
Gate Supply Voltage	V_{GVDD}	12V
Gate Charge	Q_{G}	48nC

8.2.2 Bootstrap Capacitor and GVDD Capacitor Selection

The bootstrap capacitor must be sized to maintain the bootstrap voltage above the undervoltage lockout for normal operation. Equation 1 calculates the maximum allowable voltage drop across the bootstrap capacitor:

$$\Delta V_{BSTX} = V_{GVDD} - V_{BOOTD} - V_{BSTUV} \tag{1}$$

$$=12V - 0.85V - 4.5V = 6.65V$$

where

- V_{GVDD} is the supply voltage of the gate drive
- V_{BOOTD} is the forward voltage drop of the bootstrap diode
- V_{BSTUV} is the threshold of the bootstrap undervoltage lockout

In this example the allowed voltage drop across bootstrap capacitor is 6.65V. TI recommends to minimize ripple voltage on both the bootstrap capacitor and GVDD capacitor as much as possible. Many commercial, industrial, and automotive applications use ripple values between 0.5V to 1V.

The total charge needed per switching cycle can be estimated with Equation 2:

$$Q_{TOT} = Q_G + \frac{IL_{BS_TRANS}}{f_{SW}} \tag{2}$$

 $=48nC + 220\mu A/20kHz = 50nC + 11nC = 59nC$

where

- Q_G is the total MOSFET gate charge
- I_{LBS TRAN} is the bootstrap pin leakage current
- f_{SW} is the is the PWM frequency

The minimum bootstrap capacitor an then be estimated as below assuming 1V ΔV_{BSTx}:

$$C_{BST_MIN} = \frac{Q_{TOT}}{\Delta V_{BSTX}} \tag{3}$$

= 59nC / 1V = 59nF

The calculated value of the minimum bootstrap capacitor is 59nF. Note that this value of capacitance is needed at full bias voltage. In practice, the value of the bootstrap capacitor must be greater than the calculated value to allow for situations where the power stage can skip pulse due to various transient conditions. TI recommends to

Copyright © 2025 Texas Instruments Incorporated

Submit Document Feedback



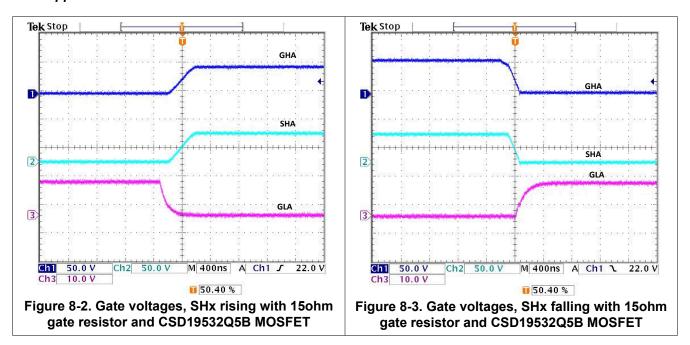
use a 100nF bootstrap capacitor in this example. TI also recommends to include enough margin and place the bootstrap capacitor as close to the BSTx and SHx pins as possible.

$$C_{GVDD} \ge 10 \times C_{BSTX}$$
 (4)

 $= 10*100 nF = 1 \mu F$

For this example application choose $1\mu F$ C_{GVDD} capacitor. Choose a capacitor with a voltage rating at least twice the maximum voltage that the capacitor is exposed to because most ceramic capacitors lose significant capacitance when biased. This value also improves the long term reliability of the system.

8.2.3 Application Curves



8.3 Power Supply Recommendations

The DRV8351-SEP is designed to operate from an input voltage supply (GVDD) range from 4.8V to 15V. A local bypass capacitor should be placed between the GVDD and GND pins. This capacitor should be located as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. It is recommended to use two capacitors across GVDD and GND: a low capacitance ceramic surface-mount capacitor for high frequency filtering placed very close to GVDD and GND pin, and another high capacitance value surface mount capacitor for device bias requirements. Similarly, the current pulses delivered by the GHx pins are sourced from the BSTx pins. Therefore, a capacitor across the BSTx to SHx is recommended, it should be a high enough capacitance value capacitor to deliver GHx pulses.

8.4 Layout

8.4.1 Layout Guidelines

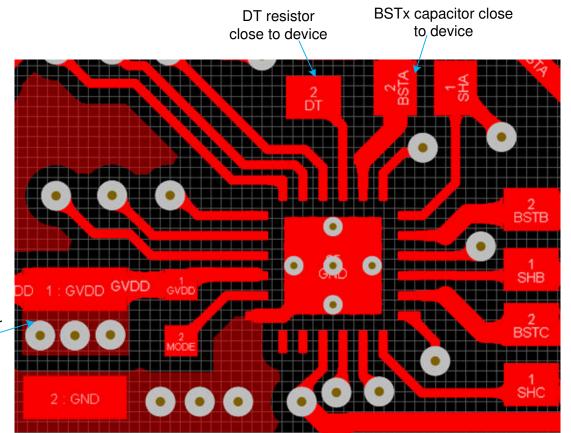
- Low ESR/ESL capacitors must be connected close to the device between GVDD and GND and between BSTx and SHx pins to support high peak currents drawn from GVDD and BSTx pins during the turn-on of the external MOSFETs.
- To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor and a good quality ceramic capacitor must be connected between the high side MOSFET drain and ground.
- To avoid large negative transients on the switch node (SHx) pin, the parasitic inductances between the source of the high-side MOSFET and the source of the low-side MOSFET must be minimized.

Submit Document Feedback

Copyright © 2025 Texas Instruments Incorporated

- www.ti.com
- To avoid unexpected transients, the parasitic inductance of the GHx, SHx, and GLx connections must be minimized. Minimize the trace length and number of vias wherever possible. Minimum 10mil and typical 15mil trace width is recommended.
- Place the gate driver as close to the MOSFETs as possible. Confine the high peak currents that charge and discharge the MOSFET gates to a minimal physical area by reducing trace length. This confinement decreases the loop inductance and minimize noise issues on the gate terminals of the MOSFETs.
- Refer to sections General Routing Techniques and MOSFET Placement and Power Stage Routing in **Application Report**

8.4.2 Layout Example



GVDD capacitor close to device



9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on Notifications to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

C	hanges from Revision * (December 2024) to Revision A (April 2025)	Page
•	In Section 1 removed the word "Target" from second bullet point. Under the same section replaced "imr with "restraint."	
•	In Section 1 added a new line "Cross conduction event is observed during SEE and SEB. Refer to SEE for more details."	
•	In Section 1 removed the line "Built-in cross conduction prevention."	
	In Section 7.3.1.1.2 added note about cross conduction during characterization of single-event effects ((SEE)
•	and single-event burnouts (SEB)	

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: DRV8351-SEP

www.ti.com 7-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8351DIMPWTSEP	Active	Production	TSSOP (PW) 20	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8351DIM
DRV8351DIMPWTSEP.A	Active	Production	TSSOP (PW) 20	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8351DIM
V62/24612-01XE	Active	Production	TSSOP (PW) 20	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8351DIM

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE MATERIALS INFORMATION

www.ti.com 18-Jul-2025

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8351DIMPWTSEP	TSSOP	PW	20	250	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 18-Jul-2025



*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
I	DRV8351DIMPWTSEP	TSSOP	PW	20	250	353.0	353.0	32.0	



SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025