

DRV8263-Q1 Automotive 65V H-Bridge Driver with Integrated Current Sense and Diagnostics

1 Features

- AEC-Q100 qualified for automotive applications:
 - Temperature grade 1: -40°C to $+125^{\circ}\text{C}$, T_A
- [Functional Safety-Compliant Targeted](#)
 - Documentation available to aid functional safety system design
- **4.5V to 65V (70V abs. max)** operating range
- DRV8263-Q1 MOSFET ON resistance (HS + LS): **85mΩ**
- DRV8263A-Q1 MOSFET ON resistance (HS + LS): **65mΩ**
- DRV8163A-Q1 MOSFET ON resistance (HS + LS): **33mΩ**
- Maximum output current = **28A**
- Configurable control modes
 - Single full-bridge, **PH/EN**, or **PWM** interface
 - Two half-bridges using **Independent mode**
 - Parallel Half-bridge mode (DRV8263A-Q1)
- 2 Interface options - **HW or SPI**
- PWM frequency operation up to 100kHz with automatic dead time assertion
- Configurable slew rate and spread spectrum clocking for low electromagnetic interference (EMI)
- Integrated current sense (eliminates shunt resistor)
- Proportional load current output on **IPROPI**
- Die temperature monitoring on IPROPI (SPI only)
- Configurable current regulation
- Protection and diagnostic features with configurable fault reaction (latched or retry)
 - Load diagnostics in both the off-state and on-state to detect open load and short circuit
 - Voltage monitoring on supply (VM)
 - Over current protection
 - Over temperature warning (SPI only)
 - Over temperature protection
 - **Powered off Braking**
 - Fault indication on nFAULT pin
- Supports 1.8V, 3.3V, 5V logic inputs
- Low sleep current - 7μA typical at 25°C
- [Device family comparison table](#)

2 Applications

- [24V and 48V Automotive Body Systems](#)
- [Automotive brushed DC motors, Solenoids](#)
- [Door modules](#) , [mirror modules](#), [wiper modules](#) and [seat modules](#)
- [Trunk lift](#), [Window lift](#)

- [Steering column](#), [Sunroof shade](#)
- [Electric Vehicles](#), [Truck](#), [Bus](#) and other [Commercial Vehicles](#)

3 Description

The DRV8263-Q1 is a wide-voltage, high-power fully integrated H-bridge driver for 24V and 48V automotive applications. Designed in a BiCMOS high-power process technology node, this device in a power package offers excellent power handling and thermal capability while providing compact package size, ease of layout, EMI control, accurate current sense, robustness, and diagnostic capability.

The device integrates a N-channel H-bridge, charge pump, high-side current sensing with regulation, current proportional output, and protection circuitry. The integrated sensing uses a current mirror, removing the need for shunt resistors, saving board area, and reducing system cost. A low-power sleep mode is provided to achieve low quiescent current.

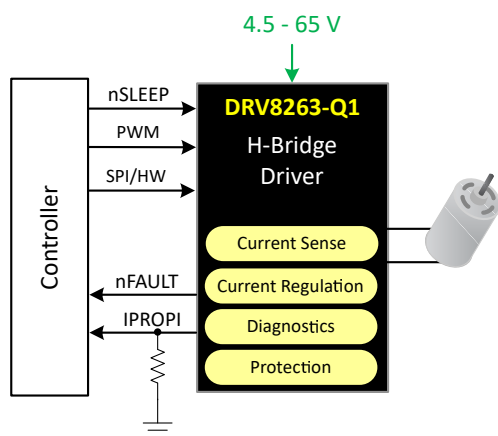
The device offers voltage monitoring and load diagnostics, as well as protection features against overcurrent and overtemperature. Fault conditions are indicated on the nFAULT pin. The device is available in two variants: HW interface and SPI. The SPI variant offers more flexibility in device configuration and fault observability.

Device Information ¹

PART NUMBER	INTERFACE	PACKAGE SIZE ²
DRV8263HQVAKRQ1	HW	VQFN-HR (15) (3.5mm x 6mm)
DRV8263SQVAKRQ1	SPI	VQFN-HR (15) (3.5mm x 6mm)

- (1) See the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.





Simplified Schematic

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4 Device Comparison

Table 4-1 summarizes the R_{ON} and package differences between devices in the DRV8X6X-Q1 family of 48V capable integrated motor drivers.

Table 4-1. Device Comparison

PART NUMBER ⁽¹⁾	Configuration	(LS + HS) R_{ON}	$I_{OUT\ MAX}$	PACKAGE	BODY SIZE	Interface
DRV8262-Q1	1 or 2 H-bridge	50m Ω or 100m Ω	16A or 8A	HTSSOP (44)	14mm × 6.1mm	HW
DRV8962-Q1	4 Half-bridge	100m Ω	8A	HTSSOP (44)	14mm × 6.1mm	HW
DRV8263-Q1	1 H-bridge	85m Ω	28A	VQFN-HR (15)	3.5mm × 6mm	HW, SPI
DRV8163-Q1	1 Half-bridge	43m Ω	40A	VQFN-HR (15)	3.5mm × 6mm	HW, SPI

(1) This is the product data sheet for the DRV8263-Q1. Please reference other device variant data sheets for additional information.

Table 4-2 summarizes the feature differences between the SPI and HW interface variants in the DRV8263-Q1. In general, the SPI variant offers more configurability, bridge control options, diagnostic feedback, and additional features.

Table 4-2. SPI Variant vs HW Variant Comparison

FUNCTION	HW Variant	SPI Variant
Bridge control	Pin only	Individual pin "and/or" register bit with pin status indication (Refer Register Pin control)
Clear fault command	Reset pulse on nSLEEP pin	SPI CLR_FAULT command
Over current protection (OCP)	Fixed at the highest setting	4 choices for thresholds, 2 choices for filter time
ITRIP regulation	5 levels with disable & fixed TOFF time	7 levels with disable & indication, with programmable TOFF time
Individual fault reaction configuration between retry or latched behavior	Not supported, either all latched or all retry	Supported
Detailed fault logging and device status feedback	Not supported, nFAULT pin monitoring necessary	Supported, nFAULT pin monitoring optional
VM over voltage	Not supported	Supported
On-state (Active) diagnostics	Not supported	Supported for high-side loads
Spread spectrum clocking (SSC)	Not supported	Supported
Additional driver states in PWM mode	Not supported	Supported
Hi-Z for individual half-bridge in Independent mode	Not supported	Supported (SPI register only)
Overttemperature warning	Not supported	Supported
Die Temperature monitor	Not supported	Supported

Table 4-3. Differentiating between devices in the family

Device	Package Symbolization	DEVICE_ID Register
DRV8262-Q1	8262	Not applicable
DRV8962-Q1	8962	Not applicable
DRV8263H-Q1	8263H	Not applicable
DRV8163H-Q1	8163H	Not applicable
DRV8263S-Q1	8263S	0 x 25
DRV8163S-Q1	8163S	0 x 2D

5 Pin Configuration and Functions

5.1 HW Variant

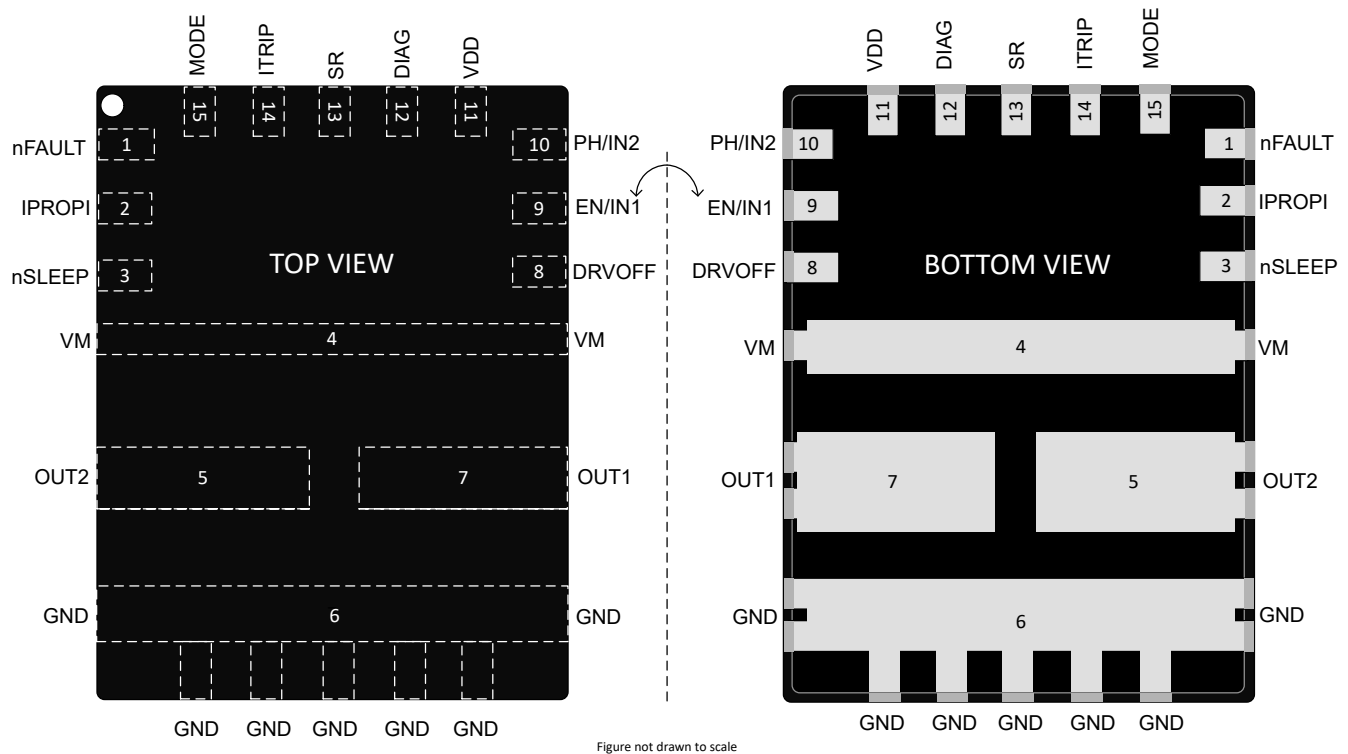


Figure 5-1. DRV8263H-Q1 in VQFN-HR(15) Package

Figure 5-2.

Table 5-1. Pin Functions

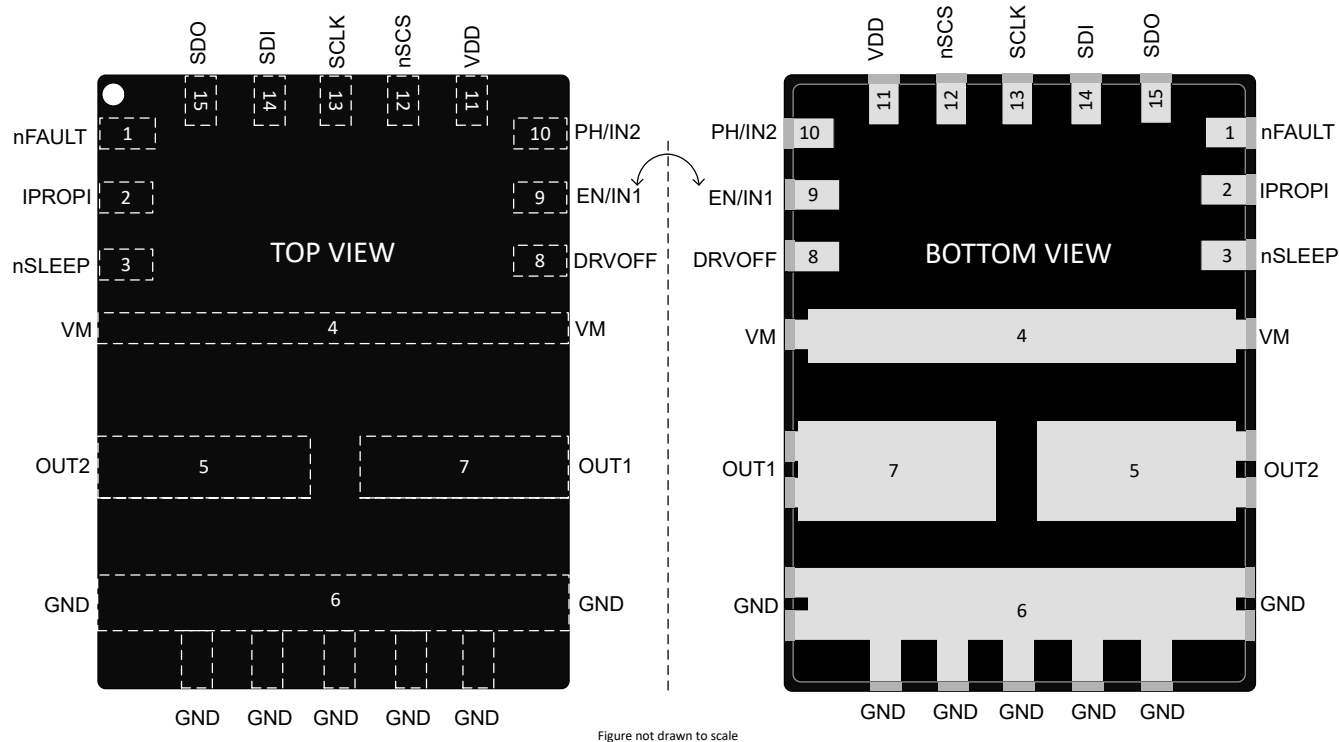
PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	nFAULT	OD	Fault indication to the controller.
2	IPROPI	I/O	Load current analog feedback. For details, refer to IPROPI in the Device Configuration section .
3	nSLEEP	I	Controller input pin for SLEEP . For details, see the Bridge Control section .
4	VM	P	Power supply. This pin is the motor supply voltage. Bypass this pin to GND with a 0.1µF ceramic capacitor and a bulk capacitor.
5	OUT2	P	Half-bridge output 2. Connect these pins together to the motor or load.
6	GND	G	Ground pin
7	OUT1	P	Half-bridge output 1. Connect these pins together to the motor or load.
8	DRVOFF	I	Controller input pin for bridge Hi-Z. For details, see the Bridge Control section .
9	EN/IN1	I	Controller input pin for bridge operation. For details, see the Bridge Control section .
10	PH/IN2	I	Controller input pin for bridge operation. For details, see the Bridge Control section .
11	VDD	P	Logic power supply to the device.
12	DIAG	I	Device configuration pin for load type indication and fault reaction configuration. For details, refer to DIAG in the Device Configuration section .
13	SR	I	Device configuration pin for Slew Rate control . For details, refer to Slew Rate in the Device Configuration section .

Table 5-1. Pin Functions (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
14	ITRIP	I	Device configuration pin for ITRIP level for high-side current limiting. For details, refer to ITRIP in the Device Configuration section.
15	MODE	I	Device configuration pin for MODE. For details, refer to the Bridge Control section.

(1) I = input, O = output, I/O = input/output, G = ground, P = power, OD = open-drain output, PP = push-pull output

5.2 SPI Variant

**Figure 5-3. DRV8263S-Q1 in VQFN-HR (15) Package****Figure 5-4.****Table 5-2. Pin Functions**

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	nFAULT	OD	Fault indication to the controller.
2	IPROPI	I/O	Multi-purpose pin. Provides load current analog feedback or analog current proportional to die temperature. For details, refer to IPROPI in the Device Configuration section.
3	nSLEEP	I	Controller input pin for SLEEP . For details, see the Bridge Control section.
4	VM	P	Power supply. This pin is the motor supply voltage. Bypass this pin to GND with a 0.1µF ceramic capacitor and a bulk capacitor.
5	OUT2	P	Half-bridge output 2. Connect these pins together to the motor or load.
6	GND	G	Ground pin
7	OUT1	P	Half-bridge output 1. Connect these pins together to the motor or load.
8	DRVOFF	I	Controller input pin for bridge Hi-Z. For details, see the Bridge Control section.
9	EN/IN1	I	Controller input pin for bridge operation. For details, see the Bridge Control section.

Table 5-2. Pin Functions (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
10	PH/IN2	I	Controller input pin for bridge operation. For details, see the Bridge Control section .
11	VDD	P	Logic power supply to the device.
12	nSCS	I	SPI - Chip Select. An active low on this pin enables the serial interface communication.
13	SCLK	I	SPI - Serial Clock input.
14	SDI	I	SPI - Serial Data Input. Data is captured at the falling edge of SCLK.
15	SDO	PP	SPI - Serial Data Output. Data is updated at the rising edge of SCLK.

(1) I = input, O = output, I/O = input/output, G = ground, P = power, OD = open-drain output, PP = push-pull output

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Power supply pin voltage	VM	−0.3	70	V
Power supply transient voltage ramp	VM		2	V/μs
Logic supply voltage	VDD	−0.3	5.75	V
Logic supply transient voltage ramp	VDD		5	V/μs
Continuous OUTx pin voltage	OUTx	−1	VM+1	V
Transient 100ns OUTx pin voltage	OUTx		71	V
Transient 100ns OUTx pin voltage	OUTx	−3	VM+3	V
Controller pins voltage, adjacent to VM	nSLEEP, DRVOFF	−0.3	70	V
Controller pins voltage	EN/IN1, PH/EN2, nFAULT	−0.3	5.75	V
Analog feedback pin voltage	IPROPI	−0.3	5.75	V
SPI variant - SPI pin voltage	SDI, SDO, nSCS, SCLK	−0.3	5.75	V
HW variant - Configuration pin voltage	MODE, ITRIP, SR, DIAG	−0.3	5.75	V
Logic & configuration pins voltage	EN/IN1, PH/EN2, nFAULT, IPROPI, SDI, SDO, nSCS, SCLK, MODE, ITRIP, SR, DIAG	−0.3	DVDD+0.3	V
Ambient temperature, T _A		−40	125	°C
Junction temperature, T _J		−40	150	°C
Storage temperature, T _{stg}		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	VM, OUT1, OUT2, GND	V
		HBM ESD Classification Level 2	All other pins	
		Charged device model (CDM), per AEC Q100-011	Corner pins	
		CDM ESD Classification Level C4B	Other pins	
			±4000	
			±2000	
			±750	
			±500	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _{VM}	Power supply voltage	VM	4.5	48	65	V
V _{VDD}	Logic supply voltage	VDD	3		5.5	V
V _{LOGIC}	Controller pins voltage	EN/IN1, PH/EN2, nSLEEP, DRVOFF, IPROPI, nFAULT	0		5.5	V
V _{CONFIG}	HW variant - Configuration pin voltage	MODE, ITRIP, SR, DIAG	0		5.5	V
V _{SPI_IOS}	SPI variant - SPI pin voltage	SDI, SDO, nSCS, SCLK	0		VDD + 0.5	V
f _{PWM}	PWM frequency	EN/IN1, PH/EN2			100	kHz
T _A	Operating ambient temperature		−40		125	°C
T _J	Operating junction temperature		−40		150	°C

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
R _{DRVOFF}	Series resistance connected from DRVOFF to controller	DRVOFF	0		45	kΩ

6.4 Electrical Characteristics

4.5 V ≤ V_{VM} ≤ 65 V, -40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, VDD)					
I _{VDD}	VDD current in ACTIVE state Die temperature readout disabled		2	3.5	mA
I _{VMS}	VM current in STANDBY state V _{VM} = 48 V, Drivers Hi-Z, Die temperature readout disabled		1	1.8	mA
I _{VMQ}	VM current in SLEEP state V _{VM} = 48 V, POB disabled, V _{nSLEEP} = 0 V or V _{VDD} < POR _{VDD_FALL}		7	30	μA
I _{VMQ_POB}	VM current in SLEEP state with POB V _{VM} = 48 V, POB enabled, V _{nSLEEP} = 0 V		8	35	μA
I _{VDDQ_POB}	VDD current in SLEEP state with POB V _{VM} = 48 V, POB enabled, V _{nSLEEP} = 0 V		7.5	35	μA
t _{RESET}	RESET pulse filter time Reset signal on nSLEEP, HW variant	5		35	μs
t _{SLEEP}	Sleep command filter time Sleep signal on nSLEEP, HW variant	40		120	μs
t _{SLEEP_SPI}	Sleep command filter time Sleep signal on nSLEEP, SPI variant	5		20	μs
t _{COM}	Time for communication to be available after wake-up or power-up through VM or VDD pin Wake-up signal on nSLEEP pin or power cycle (V _{VM} > VM _{POR_RISE} or V _{VDD} > VDD _{POR_RISE})			0.2	ms
t _{READY}	Time for driver ready to be driven after wake-up through nSLEEP or power-up through VM or VDD Wake-up signal on nSLEEP pin or power cycle (V _{VM} > VM _{POR_RISE} or V _{VDD} > VDD _{POR_RISE})			1.2	ms
CONTROLLER (nSLEEP, DRVOFF, EN/IN1, PH/IN2, IN) and SPI INPUTS (SDI, nSCS, SCLK)					
V _{IL}	Input logic low voltage All pins	0		0.6	V
V _{IH}	Input logic high voltage All pins	1.5		5.5	V
V _{HYS}	Input hysteresis All pins except nSLEEP		0.1		V
V _{HYS_nSLEEP}	Input hysteresis on nSLEEP pin		0.15		V
R _{PU}	Internal pull-up resistance on DRVOFF and nSCS Measured at min V _{IH} level	150		450	kΩ
R _{PD}	Input pull-down resistance on EN/IN1, PH/IN2, SDI, SCLK Measured at max V _{IL} level	150		450	kΩ
R _{PD_nSLEEP}	Input pull-down resistance on nSLEEP to GND Measured at max V _{IL} level	160		400	kΩ
TRI-LEVEL INPUT (MODE)					
R _{LVL1}	Level 1 Connect to GND			10	Ω
R _{LVL2}	Level 2 +/- 10% resistor to GND	8	16	24	kΩ
R _{LVL3}	Level 3 Hi-Z (no connect)	249			kΩ
Quad-level Input (SR)					
R _{LVL1}	Level 1 Connect to GND			10	Ω
R _{LVL2}	Level 2 +/-10% resistor GND	8	16	24	kΩ
R _{LVL3}	Level 3 +/-10% resistor GND	45	75	110	kΩ
R _{LVL4}	Level 4 Hi-Z (no connect)	249			kΩ
6 LEVEL INPUT (ITRIP, DIAG, EXT_SR)					
R _{LVL1}	Level 1 Connect to GND			10	Ω
R _{LVL2}	Level 2 +/- 10% resistors	8	9	10	kΩ
R _{LVL3}	Level 3 +/- 10% resistors	22	24	26	kΩ
R _{LVL4}	Level 4 +/- 10% resistors	45	48	51	kΩ

DRV8263-Q1

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 $4.5\text{ V} \leq V_{VM} \leq 65\text{ V}$, $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R _{LVL5}	Level 5	+/- 10% resistors	90	100	110	kΩ
R _{LVL6}	Level 6	Hi-Z (no connect)	249			kΩ
PUSH-PULL and Control Outputs (SDO, nFAULT)						
V _{OL_SDO}	SDO Output logic-low voltage	0.5 mA sink		0.1	0.2	V
V _{OH_SDO}	SDO Output logic-high voltage	0.5 mA source, V _{VDD} = 5 V	4.7	4.9		V
I _{SDO}	SDO Leakage Current	V _{VM} > 6 V	-2		2	μA
V _{OL}	nFAULT Output logic-low voltage	I _O = 5 mA			0.3	V
I _{OH}	nFAULT Output logic-high leakage		-1		1	μA
DRIVER OUTPUT (OUTx)						
R _{HS_DS(on)}	High-side MOSFET on resistance, DRV8263	I _O = -4 A, T _J = 25°C		42	50	mΩ
R _{HS_DS(on)}	High-side MOSFET on resistance, DRV8263	I _O = -4 A, T _J = 150°C		70	84	mΩ
R _{LS_DS(on)}	Low-side MOSFET on resistance, DRV8263	I _O = 4 A, T _J = 25°C		43	52	mΩ
R _{LS_DS(on)}	Low-side MOSFET on resistance, DRV8263	I _O = 4 A, T _J = 150°C		72	86	mΩ
V _{SD}	Body diode forward voltage	I _O = -4 A (8263), -6A (8163)	0.4	0.8	1.2	V
I _{HIZ_SLP_POB}	OUTx leakage current to GND in SLEEP state, POB enabled	V(OUTx) = V _M = 48 V, per OUT pin			10.5	mA
I _{HIZ_STBY_POB}	OUTx leakage current to GND in Standby state, POB enabled	V(OUTx) = V _M = 48 V, per OUT pin	1		21	mA
I _{HIZ_SLP}	OUTx leakage current to GND in SLEEP state, POB disabled	V(OUTx) = V _M = 48 V, per OUT pin			140	μA
I _{HIZ_STBY}	OUTx leakage current to GND in Standby state, POB disabled	V(OUTx) = V _M = 48 V, per OUT pin	1		21	mA
SR _{LS}	Output voltage rise slew rate, 10% - 90%, V _{VM} = 48 V	SR = 00b or LVL1, high-side recirculation	146	192	237	V/μs
SR _{LS}	Output voltage fall slew rate, 90% - 10%, V _{VM} = 48 V	SR = 00b or LVL1, high-side recirculation	130	160	204	V/μs
SR _{LS}	Output voltage rise slew rate, 10% - 90%, V _{VM} = 48 V	SR = 01b or LVL2, high-side recirculation	73	99	124	V/μs
SR _{LS}	Output voltage fall slew rate, 90% - 10%, V _{VM} = 48 V	SR = 01b or LVL2, high-side recirculation	67	83	107	V/μs
SR _{LS}	Output voltage rise slew rate, 10% - 90%, V _{VM} = 48 V	SR = 10b or LVL3, high-side recirculation	32	46	60	V/μs
SR _{LS}	Output voltage fall slew rate, 90% - 10%, V _{VM} = 48 V	SR = 10b or LVL3, high-side recirculation	26	38	52	V/μs
SR _{LS}	Output voltage rise slew rate, 10% - 90%, V _{VM} = 48 V	SR = 11b or LVL4, high-side recirculation	11	18	25	V/μs
SR _{LS}	Output voltage fall slew rate, 90% - 10%, V _{VM} = 48 V	SR = 11b or LVL4, high-side recirculation	8	14.5	21.5	V/μs
t _{PD_LSOFF}	Propagation delay during output voltage rise	SR = 00b or 01b or LVL1 or LVL2, high-side recirculation		0.3		μs
t _{PD_LSOFF}	Propagation delay during output voltage rise	SR = 10b or 11b or LVL3 or LVL4, high-side recirculation		0.5		μs
t _{PD_LSON}	Propagation delay during output voltage fall	SR = 00b or 01b or LVL1 or LVL2, high-side recirculation		0.26		μs
t _{PD_LSON}	Propagation delay during output voltage fall	SR = 10b or 11b or LVL3 or LVL4, high-side recirculation		0.33		μs
t _{DEAD_LSOFF}	Dead time during output voltage rise	SR = 00b or 01b or LVL1 or LVL2, high-side recirculation		0.95		μs

4.5 V ≤ V_{VM} ≤ 65 V, -40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{DEAD_LSOFF}	Dead time during output voltage rise	SR = 10b or LVL3, high-side recirculation		0.83		μs
t _{DEAD_LSOFF}	Dead time during output voltage rise	SR = 11b or LVL4, high-side recirculation		1.06		μs
t _{DEAD_LSON}	Dead time during output voltage fall	SR = 00b or 01b or LVL1 or LVL2, high-side recirculation		0.5		μs
t _{DEAD_LSON}	Dead time during output voltage fall	SR = 10b or LVL3, high-side recirculation		0.53		μs
t _{DEAD_LSON}	Dead time during output voltage fall	SR = 11b or LVL4, high-side recirculation		0.62		μs
SR _{HS}	Output voltage rise slew rate, 10% - 90%, V _{VM} = 48 V	SR = 00b or LVL1, low-side recirculation	89	130	185	V/μs
SR _{HS}	Output voltage fall slew rate, 90% - 10%, V _{VM} = 48 V	SR = 00b or LVL1, low-side recirculation	140	180	230	V/μs
SR _{HS}	Output voltage rise slew rate, 10% - 90%, V _{VM} = 48 V	SR = 01b or LVL2, low-side recirculation	50	71	98	V/μs
SR _{HS}	Output voltage fall slew rate, 90% - 10%, V _{VM} = 48 V	SR = 01b or LVL2, low-side recirculation	70	94	122	V/μs
SR _{HS}	Output voltage rise slew rate, 10% - 90%, V _{VM} = 48 V	SR = 10b or LVL3, low-side recirculation	23	33	47	V/μs
SR _{HS}	Output voltage fall slew rate, 90% - 10%, V _{VM} = 48 V	SR = 10b or LVL3, low-side recirculation	31	45	59	V/μs
SR _{HS}	Output voltage rise slew rate, 10% - 90%, V _{VM} = 48 V	SR = 11b (SPI only), low-side recirculation	7	13	21	V/μs
SR _{HS}	Output voltage fall slew rate, 90% - 10%, V _{VM} = 48 V	SR = 11b (SPI only), low-side recirculation	13	19	26	V/μs
t _{PD_HSON}	Propagation delay during output voltage rise	SR = 00b or 01b or LVL1 or LVL2, low-side recirculation		0.35		μs
t _{PD_HSON}	Propagation delay during output voltage rise	SR = 10b or 11b or LVL3 or LVL4, low-side recirculation		0.68		μs
t _{PD_HSOFF}	Propagation delay during output voltage fall	SR = 00b or 01b or LVL1 or LVL2, low-side recirculation		0.27		μs
t _{PD_HSOFF}	Propagation delay during output voltage fall	SR = 10b or LVL3, low-side recirculation		0.33		μs
t _{PD_HSOFF}	Propagation delay during output voltage fall	SR = 11b or LVL4, low-side recirculation		0.38		μs
t _{DEAD_HSON}	Dead time during output voltage rise	SR = 00b or LVL1, low-side recirculation		0.46		μs
t _{DEAD_HSON}	Dead time during output voltage rise	SR = 01b or LVL2, low-side recirculation		0.52		μs
t _{DEAD_HSON}	Dead time during output voltage rise	SR = 10b or LVL3, low-side recirculation		0.60		μs
t _{DEAD_HSON}	Dead time during output voltage rise	SR = 11b or LVL4, low-side recirculation		0.60		μs
t _{DEAD_HSOFF}	Dead time during output voltage fall	All SRs, low-side recirculation		0.1		μs
t _{BLANK}	Current regulation blanking time (Valid for only for LS recirculation)	TBLK = 0b. Only choice for HW.		2.4		μs
t _{BLANK}	Current regulation blanking time (Valid for only for LS recirculation)	TBLK = 1b		3.4		μs
EXTENDED SLEW RATE (DRV8263A-Q1)						
SR _{LS}	Output voltage rise slew rate, 10% - 90%, V _{VM} = 48 V	EXT_SR = 11b or LVL7, high-side recirculation		400		V/μs
SR _{LS}	Output voltage fall slew rate, 90% - 10%, V _{VM} = 48 V	EXT_SR = 11b or LVL7, high-side recirculation		400		V/μs
SR _{LS}	Output voltage rise slew rate, 10% - 90%, V _{VM} = 48 V	EXT_SR = 10b or LVL6, high-side recirculation		330		V/μs
SR _{LS}	Output voltage fall slew rate, 90% - 10%, V _{VM} = 48 V	EXT_SR = 10b or LVL6, high-side recirculation		330		V/μs
SR _{LS}	Output voltage rise slew rate, 10% - 90%, V _{VM} = 48 V	EXT_SR = 01b or LVL5, high-side recirculation		270		V/μs

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 $4.5\text{ V} \leq V_{VM} \leq 65\text{ V}$, $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR _{LS}	Output voltage fall slew rate, 90% - 10%, $V_{VM} = 48\text{ V}$	EXT_SR = 01b or LVL5, high-side recirculation		270		V/ μ s
t _{PD_LSOFF}	Propagation delay during output voltage rise	EXT_SR = 01b, 10b, 11b or LVL5, LVL6, LVL7 high-side recirculation		0.3		μ s
t _{PD_LSON}	Propagation delay during output voltage fall	EXT_SR = 01b, 10b, 11b or LVL5, LVL6, LVL7 high-side recirculation		0.26		μ s
t _{DEAD_LSOFF}	Dead time during output voltage rise	EXT_SR = 01b, 10b, 11b or LVL5, LVL6, LVL7 high-side recirculation		0.95		μ s
t _{DEAD_LSON}	Dead time during output voltage fall	EXT_SR = 01b, 10b, 11b or LVL5, LVL6, LVL7 high-side recirculation		0.5		μ s
SR _{HS}	Output voltage rise slew rate, 10% - 90%, $V_{VM} = 48\text{ V}$	EXT_SR = 11b or LVL7, low-side recirculation		400		V/ μ s
SR _{HS}	Output voltage fall slew rate, 90% - 10%, $V_{VM} = 48\text{ V}$	EXT_SR = 11b or LVL7, low-side recirculation		400		V/ μ s
SR _{HS}	Output voltage rise slew rate, 10% - 90%, $V_{VM} = 48\text{ V}$	EXT_SR = 10b or LVL6, low-side recirculation		330		V/ μ s
SR _{HS}	Output voltage fall slew rate, 90% - 10%, $V_{VM} = 48\text{ V}$	EXT_SR = 10b or LVL6, low-side recirculation		330		V/ μ s
SR _{HS}	Output voltage rise slew rate, 10% - 90%, $V_{VM} = 48\text{ V}$	EXT_SR = 01b or LVL5, low-side recirculation		270		V/ μ s
SR _{HS}	Output voltage fall slew rate, 90% - 10%, $V_{VM} = 48\text{ V}$	EXT_SR = 01b or LVL5, low-side recirculation		270		V/ μ s
t _{PD_HSON}	Propagation delay during output voltage rise	EXT_SR = 01b, 10b, 11b or LVL5, LVL6, LVL7 low-side recirculation		0.35		μ s
t _{PD_HSOFF}	Propagation delay during output voltage fall	EXT_SR = 01b, 10b, 11b or LVL5, LVL6, LVL7 low-side recirculation		0.27		μ s
t _{DEAD_HSON}	Dead time during output voltage rise	EXT_SR = 01b, 10b, 11b or LVL5, LVL6, LVL7 low-side recirculation		0.46		μ s
I _{PD_OLA}	Internal sink current on OUTx to GND during dead-time in high-side recirculation, 400 V/ μ s slew rate		18		44	mA
I _{PD_OLA}	Internal sink current on OUTx to GND during dead-time in high-side recirculation, 330 V/ μ s slew rate		15		36	mA
I _{PD_OLA}	Internal sink current on OUTx to GND during dead-time in high-side recirculation, 270 V/ μ s slew rate		12		29	mA
CURRENT SENSE AND REGULATION (IPROPI, VREF)						
A _{IPROPI}	Current mirror gain			202		μ A/A
A _{ERR}	Current mirror scaling error	I _{OUT} > 2 A	-4		4	%
A _{ERR}	Current mirror scaling error	0.5 A < I _{OUT} ≤ 2 A	-10		10	%
A _{ERR}	Current mirror scaling error	0.2 A < I _{OUT} ≤ 0.5 A	-25		25	%
A _{ERR_M}	Current matching between the two half-bridges	I _{OUT} > 2 A	-3		3	%
V _{IPROPI_LIM}	Internal clamping voltage on IPROPI		3.4		5.5	V
V _{ITRIP_LVL}	Voltage limit on V _{IPROPI} to trigger TOFF cycle for ITRIP regulation	S_ITRIP = 001b or LVL2	1.08	1.2	1.3	V
V _{ITRIP_LVL}	Voltage limit on V _{IPROPI} to trigger TOFF cycle for ITRIP regulation	S_ITRIP = 010b (SPI only)	1.31	1.44	1.55	V
V _{ITRIP_LVL}	Voltage limit on V _{IPROPI} to trigger TOFF cycle for ITRIP regulation	S_ITRIP = 011b (SPI only)	1.53	1.67	1.81	V
V _{ITRIP_LVL}	Voltage limit on V _{IPROPI} to trigger TOFF cycle for ITRIP regulation	S_ITRIP = 100b or LVL3	1.83	2	2.16	V

4.5 V ≤ V_{VM} ≤ 65 V, -40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{ITRIP_LVL}	Voltage limit on V _{IPROPI} to trigger TOFF cycle for ITRIP regulation	S_ITRIP = 101b or LVL4	2.14	2.34	2.52	V
V _{ITRIP_LVL}	Voltage limit on V _{IPROPI} to trigger TOFF cycle for ITRIP regulation	S_ITRIP = 110b or LVL5	2.44	2.67	2.88	V
V _{ITRIP_LVL}	Voltage limit on V _{IPROPI} to trigger TOFF cycle for ITRIP regulation	S_ITRIP = 111b or LVL6	2.74	3	3.24	V
t _{OFF}	ITRIP regulation off-time	TOFF = 00b	9	20	35	µs
t _{OFF}	ITRIP regulation off-time	TOFF = 01b. Only choice for HW.	15	30	45	µs
t _{OFF}	ITRIP regulation off-time	TOFF = 10b	20	40	60	µs
t _{OFF}	ITRIP regulation off-time	TOFF = 11b	25	50	70	µs
PROTECTION CIRCUITS						
V _{VMOV_POB}	VM over voltage threshold while rising during POB		60		69	V
V _{VMOV}	VM over voltage threshold while rising	OVSEL = 0b (SPI only)	59.5		64.5	V
V _{VMOV}	VM over voltage threshold while rising	VMOV_SEL = 01b (DRV8263A-Q1SPI only)	21		23	V
V _{VMOV}	VM over voltage threshold while rising	VMOV_SEL = 10b (DRV8263A-Q1SPI only)	27		28	V
V _{VMOV_HYS}	VM over voltage hysteresis			0.7		V
t _{VMOV}	VM over voltage deglitch time		4	12	19	µs
V _{VMUV}	VM Under Voltage	VM falling	4.1	4.25	4.4	V
V _{VMUV}	VM Under Voltage	VM rising	4.15	4.3	4.45	V
V _{VMUV_HYS}	VM UV hysteresis	Rising to falling threshold		0.065		V
t _{VMUV}	VM UV deglitch time		3	12	20	µs
V _{POR_FALL}	VDD voltage at which device goes into POR				2.7	V
V _{POR_RISE}	VDD voltage at which device comes out of POR				2.8	V
I _{OCP}	Overcurrent protection threshold, DRV8263	OCP_SEL = 11b, only choice for HW	28		47	A
I _{OCP}	Overcurrent protection threshold, DRV8263	OCP_SEL = 10b	22		37.5	A
I _{OCP}	Overcurrent protection threshold, DRV8263	OCP_SEL = 01b	14.5		26	A
I _{OCP}	Overcurrent protection threshold, DRV8263	OCP_SEL = 00b	5.5		16	A
t _{OCP}	Overcurrent protection deglitch time	TOCP = 0b	0.5	1	1.65	µs
t _{OCP}	Overcurrent protection deglitch time	TOCP = 1b, only choice for HW	0.6	2	3.5	µs
t _{RETRY}	Overcurrent protection retry time	Fault reaction set to RETRY	2.6	5	6.7	ms
t _{CLEAR}	Fault free operation time to auto-clear from over current event	Fault reaction set to RETRY	70		140	µs
T _{TSD}	Thermal shutdown temperature	Die temperature T _J	155	170	185	°C
T _{HYS}	Thermal shutdown hysteresis	Die temperature T _J		20		°C
t _{TSD}	Thermal shutdown deglitch time		7	12	18	µs
t _{CLEAR_TSD}	Fault free operation time to auto-clear from over temperature event	Fault reaction set to RETRY	3.6	5	6.4	ms
T _{OTW}	Over temperature warning threshold	Die temperature T _J , OTW_SEL = 0b	125	140	155	°C
T _{OTW}	Over temperature warning threshold	Die temperature T _J , OTW_SEL = 1b	105	120	135	°C

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 $4.5\text{ V} \leq V_{VM} \leq 65\text{ V}$, $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{HYS_OTW}	Over temperature warning hysteresis	Die temperature T_J		20		$^{\circ}\text{C}$
t_{OTW}	Over temperature warning deglitch time		7	12	18	μs
T_{DIE}	Die temperature measurement range	Die temperature T_J	-40		185	$^{\circ}\text{C}$
I_{IPROPI_DIE}	IPROPI current range for die temperature measurement		0.5		1.5	mA
T_{DIE_ACC}	Die temperature measurement accuracy	Error relative to ideal IPROPI current	-10		10	%
V_{POB_TH}	Powered off braking threshold			580		mV
I_{OCP_POB}	Overcurrent protection threshold in POB			29		A
t_{OCP_POB}	Overcurrent protection deglitch time in POB			8		μs
t_{POB_ON}	Powered off braking turn-on time			20		μs
t_{POB_RETRY}	Powered off braking retry time			180		μs
$R_{S_GND_High}$	Output resistance range detected as normal	OUTx-GND resistance, full-bridge load	13		∞	k Ω
$R_{S_GND_X}$	Output resistance range with indeterminate detection (may be detected as either state)	OUTx-GND resistance, full-bridge load	1.5		13	k Ω
$R_{S_GND_Low}$	Output resistance range detected as short circuit	OUTx-GND resistance, full-bridge load	0		1.5	k Ω
$R_{S_VM_High}$	Output resistance range detected as normal	OUTx-VM resistance, $V_M=48\text{V}$, full-bridge load	150		∞	k Ω
$R_{S_VM_X}$	Output resistance range with indeterminate detection (may be detected as either state)	OUTx-VM resistance, $V_M=48\text{V}$, full-bridge load	3		150	k Ω
$R_{S_VM_Low}$	Output resistance range detected as short circuit	OUTx-VM resistance, $V_M=48\text{V}$, full-bridge load	0		3	k Ω
$R_{OPEN_FB_High}$	Output resistance range detected as open	OUT1-OUT2 resistance, full-bridge load	0.55		∞	k Ω
$R_{OPEN_FB_X}$	Output resistance range with indeterminate detection (may be detected as either state)	OUT1-OUT2 resistance, full-bridge load	0.03		0.55	k Ω
$R_{OPEN_FB_Low}$	Output resistance range detected as normal	OUT1-OUT2 resistance, full-bridge load	0		0.03	k Ω
$R_{OPEN_LS_High}$	Output resistance range detected as open	OUTx-GND resistance, low side load	1.5		∞	k Ω
$R_{OPEN_LS_X}$	Output resistance range with indeterminate detection (may be detected as either state)	OUTx-GND resistance, low side load	0.9		1.5	k Ω
$R_{OPEN_LS_Low}$	Output resistance range detected as normal	OUTx-GND resistance, low side load	0		0.9	k Ω
$R_{OPEN_HS_High}$	Output resistance range detected as open	OUTx-VM resistance, high side load, $V_{VM} = 48\text{ V}$	30		∞	k Ω
$R_{OPEN_HS_X}$	Output resistance range with indeterminate detection (may be detected as either state)	OUTx-VM resistance, high side load, $V_{VM} = 48\text{ V}$	16		30	k Ω
$R_{OPEN_HS_Low}$	Output resistance range detected as normal	OUTx-VM resistance, high side load, $V_{VM} = 48\text{ V}$	0		16	k Ω
V_{OLP_REFH}	OLP Comparator Reference High			2.7		V
V_{OLP_REFL}	OLP Comparator Reference Low			2.2		V
R_{OLP_PU}	Internal pull-up resistance on OUT to internal 5V during OLP	$V_{OUTx} = V_{OLP_REFH} + 0.1\text{ V}$		1		k Ω
R_{OLP_PD}	Internal pull-down resistance on OUT to GND during OLP	$V_{OUTx} = V_{OLP_REFL} - 0.1\text{ V}$		1		k Ω

4.5 V ≤ V_{VM} ≤ 65 V, -40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{PD_OLA}	Internal sink current on OUTx to GND during dead-time in high-side recirculation, 220 V/us slew rate		10		24	mA
I _{PD_OLA}	Internal sink current on OUTx to GND during dead-time in high-side recirculation, 110V/us slew rate		5		12	mA
I _{PD_OLA}	Internal sink current on OUTx to GND during dead-time in high-side recirculation, 50V/us slew rate		2.3		6	mA
I _{PD_OLA}	Internal sink current on OUTx to GND during dead-time in high-side recirculation, 20V/us slew rate		0.8		2.6	mA
V _{OLA_REF}	Comparator Reference with respect to VM used for OLA			0.28		V

6.5 Timing Requirements

		MIN	NOM	MAX	UNIT
t _{SCLK}	SCLK minimum period	150			ns
t _{SCLKH}	SCLK minimum high time	70			ns
t _{SCLKL}	SCLK minimum low time	70			ns
t _{HI_nSCS}	SDO minimum high time	600			ns
t _{SU_nSCS}	nSCS input setup time	25			ns
t _{H_nSCS}	nSCS input hold time	25			ns
t _{SU_SDI}	SDI input data setup time	25			ns
t _{H_SDI}	SDI input data hold time	25			ns
t _{EN_nSCS}	Enable delay time, nSCS low to SDO active			45	ns
t _{DIS_nSCS}	Disable delay time, nSCS high to SDO HI-Z			425	ns

6.6 Timing Diagrams

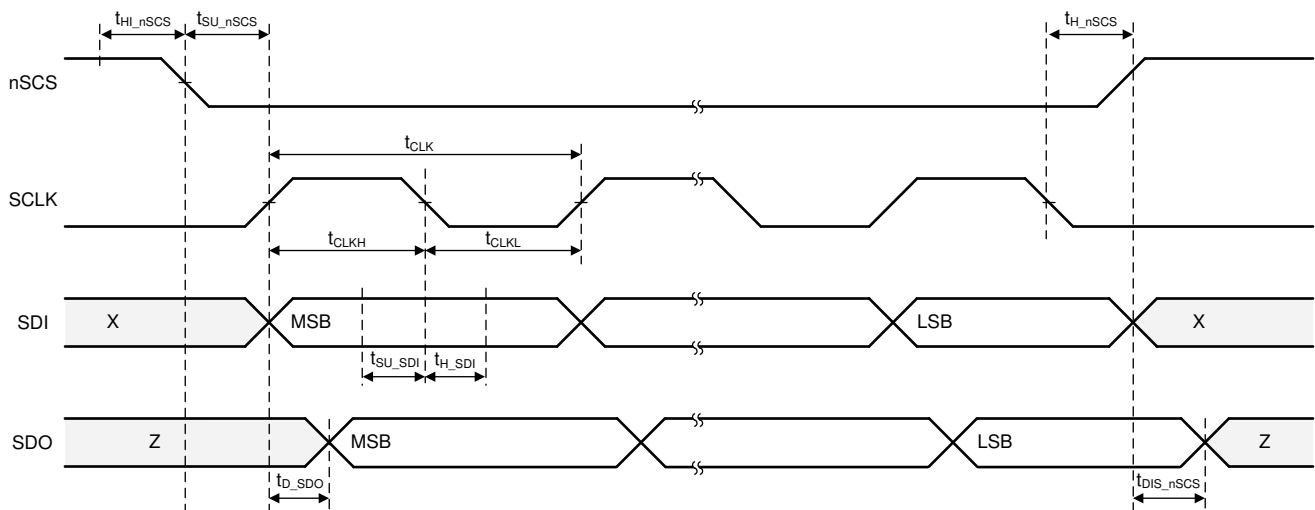


Figure 6-1. SPI Timing Diagram

6.7 Thermal Information

Refer [Transient thermal impedance](#) table for application related use case.

THERMAL METRIC ⁽¹⁾		VQFN-HR package	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	18.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	6.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.7.1 Transient Thermal Impedance & Current Capability

Information based on thermal simulations

Table 6-1. Transient Thermal Impedance ($R_{\theta JA}$) and Current Capability

PART NUMBER	$R_{\theta JA}$ [°C/W] ⁽¹⁾			Current [A] ⁽²⁾				
				without PWM ⁽³⁾			with PWM ⁽⁴⁾	
	0.1sec	1sec	DC	0.1sec	1sec	DC	1sec	DC
DRV8263-Q1	4.4	13.9	35.1	9.0	5.1	3.2	4.4	2.5

- (1) Based on thermal simulations using 40mm x 40mm x 1.6mm 4-layer PCB – 2oz Cu on top and bottom layers, 1oz Cu on internal planes with 0.3 mm thermal via drill diameter, 0.025mm Cu plating, 1 minimum mm via pitch.
 (2) Estimated transient current capability at 85 °C ambient temperature for junction temperature rise to 150°C
 (3) Only conduction losses (I^2R) are considered
 (4) Switching loss roughly estimated by the following equation:

$$P_{SW} = V_{VM} \times I_{Load} \times f_{PWM} \times V_{VM}/SR, \text{ where } V_{VM} = 48V, f_{PWM} = 20KHz, SR = 175V/\mu s \quad (1)$$

6.8 Switching Waveforms

6.8.1 Output switching transients

This section illustrates the switching transients for an inductive load due to external PWM or internal ITRIP regulation.

6.8.1.1 High-Side Recirculation

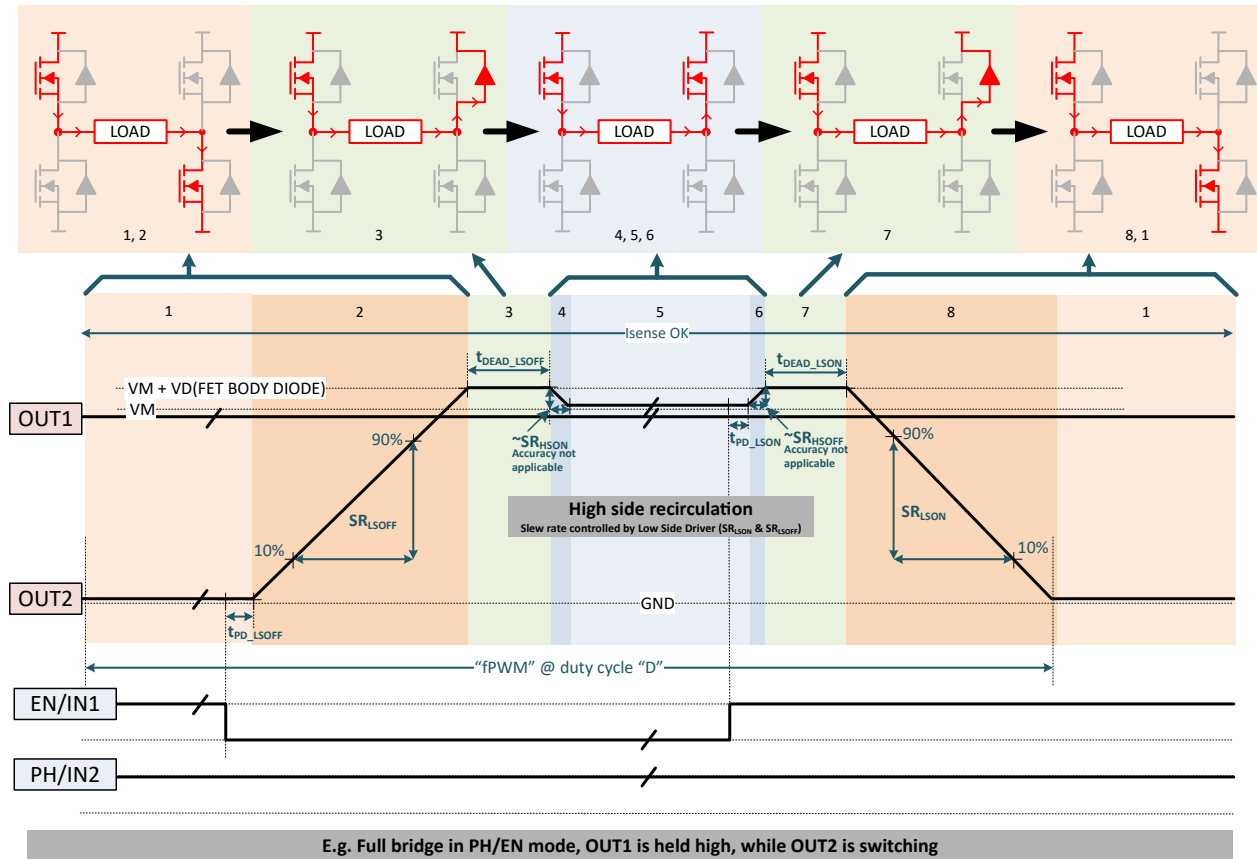


Figure 6-2. Output Switching Transients for a H-Bridge with High-Side Recirculation

6.8.2 Wake-up Transients

6.8.2.1 HW Variant

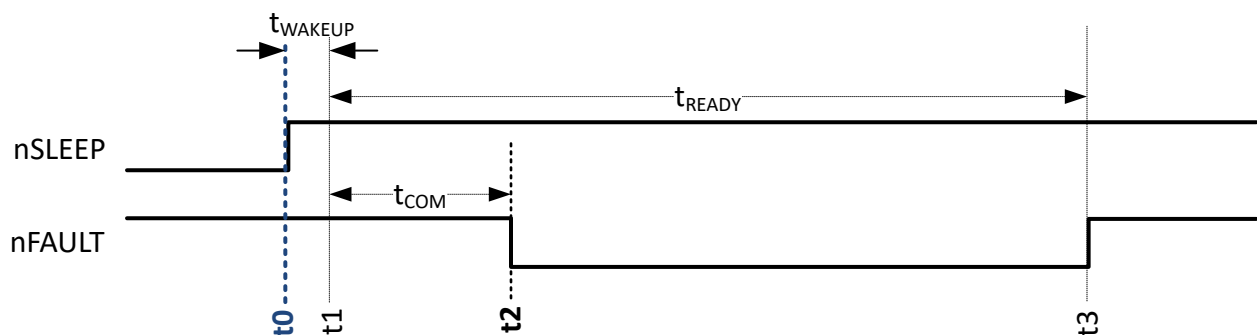


Figure 6-3. Wake-up from SLEEP State to STANDBY State without ACK Pulse

Hand shake between controller and device during wake-up as follows:

- t0: Controller - nSLEEP asserted high to initiate device wake-up
- t1: Device internal state - Wake-up command registered by device (end of Sleep state)
- t2: Device - nFAULT asserted low to acknowledge wake-up and indicate device ready for communication
- t3: Device internal state - Initialization complete. nFAULT de-asserted. Device in STANDBY state.

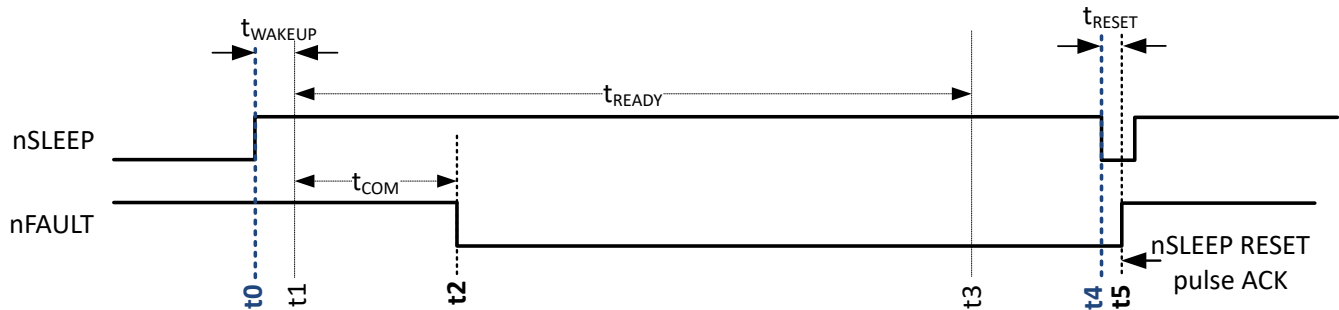


Figure 6-4. Wake-up from SLEEP State to STANDBY State with ACK pulse

Hand shake between controller and device during wake-up as follows:

- t0: Controller - nSLEEP asserted high to initiate device wake-up
- t1: Device internal state - Wake-up command registered by device (end of Sleep state)
- t2: Device – nFAULT asserted low to acknowledge wake-up and indicate device ready for communication
- t3: Device internal state - Initialization complete
- t4 (any time after t3): **Controller – Issue nSLEEP reset pulse** to acknowledge device wake-up
- t5: Device - nFAULT de-asserted as an acknowledgment of nSLEEP reset pulse. Device in STANDBY state.

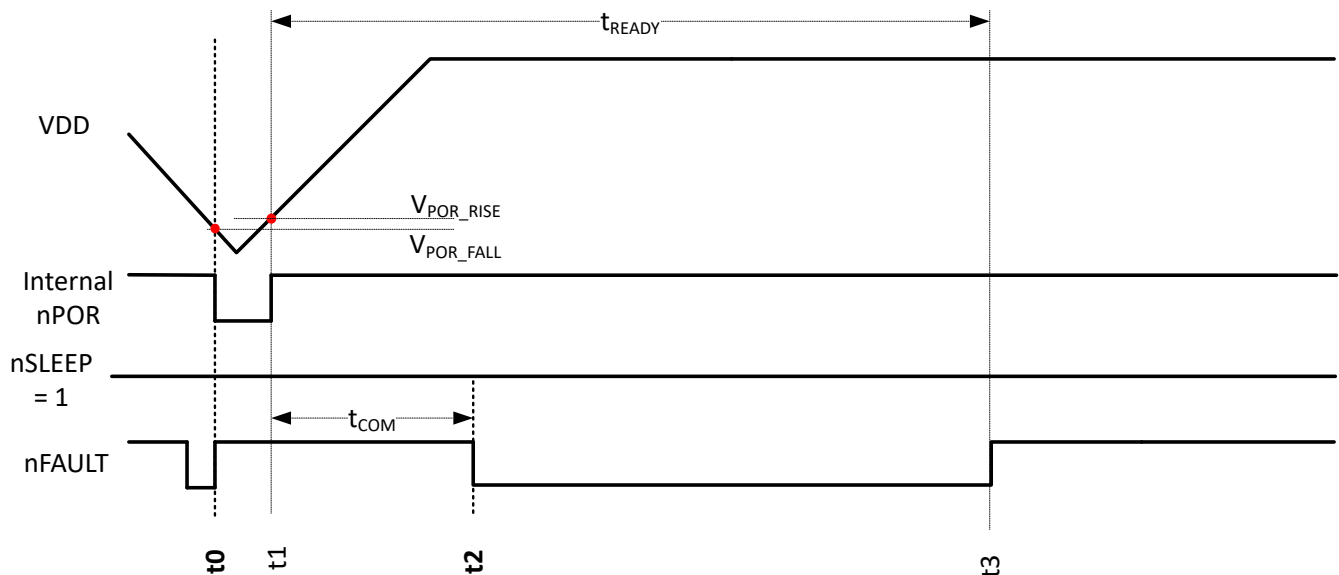


Figure 6-5. Power-up Via VDD to STANDBY State Without ACK Pulse

Hand shake between controller and device during power-up as follows:

- t0: Device internal state - POR asserted based on under voltage on VDD (external supply)
- t1: Device internal state – POR de-asserted based on recovery of voltage on VDD (external supply)
- t2: Device – nFAULT asserted low to acknowledge wake-up and indicate device ready for communication
- t3: Device internal state - Initialization complete. nFAULT de-asserted. Device in STANDBY state.

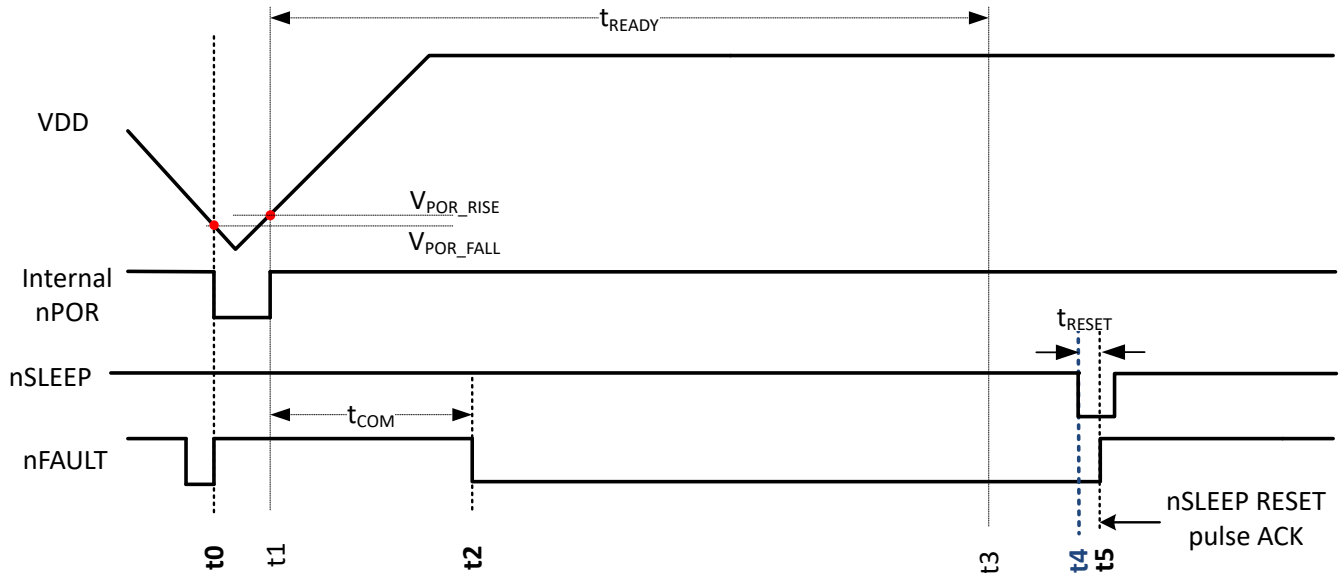


Figure 6-6. Power-up via VDD to STANDBY State with ACK pulse

Hand shake between controller and device during power-up as follows:

- t0: Device internal state - POR asserted based on under voltage on VDD (external supply)
- t1: Device internal state – POR de-asserted based on recovery of voltage on VDD (external supply)
- t2: Device – nFAULT asserted low to acknowledge wake-up and indicate device ready for communication
- t3: Device internal state - Initialization complete
- t4 (any time after t3): **Controller – Issue nSLEEP reset pulse** to acknowledge device power-up
- t5: Device - nFAULT de-asserted as an acknowledgment of nSLEEP reset pulse. Device in STANDBY state.

6.8.2.2 SPI Variant

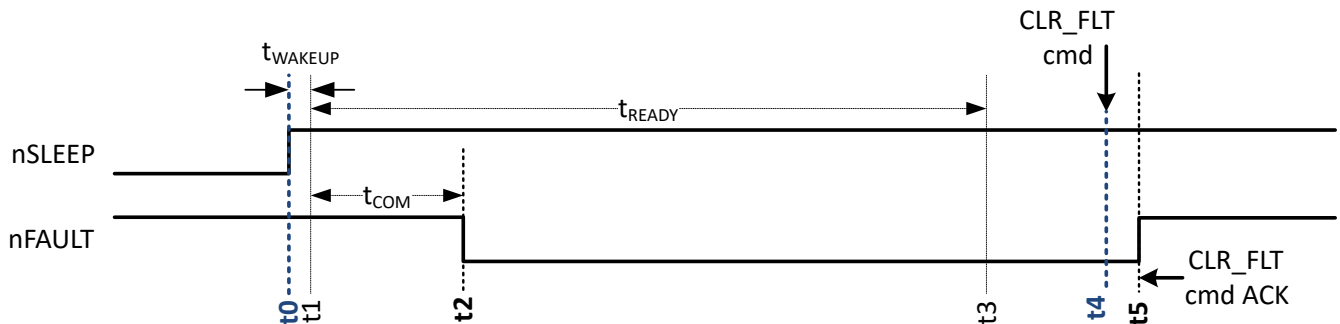


Figure 6-7. Wake-up from SLEEP State to STANDBY State

Hand shake between controller and device during a wake-up transient as follows:

- t0: Controller - nSLEEP asserted high to initiate device wake-up
- t1: Device internal state - Wake-up command registered by device (end of Sleep state)
- t2: Device – nFAULT asserted low to acknowledge wake-up and indicate device ready for communication
- t3: Device internal state - Initialization complete
- t4 (Any time after t3): **Controller – Issue CLR_FLT command** through SPI to acknowledge device wake-up
- t5: Device - nFAULT de-asserted as an acknowledgment of CLR_FLT command. Device in STANDBY state

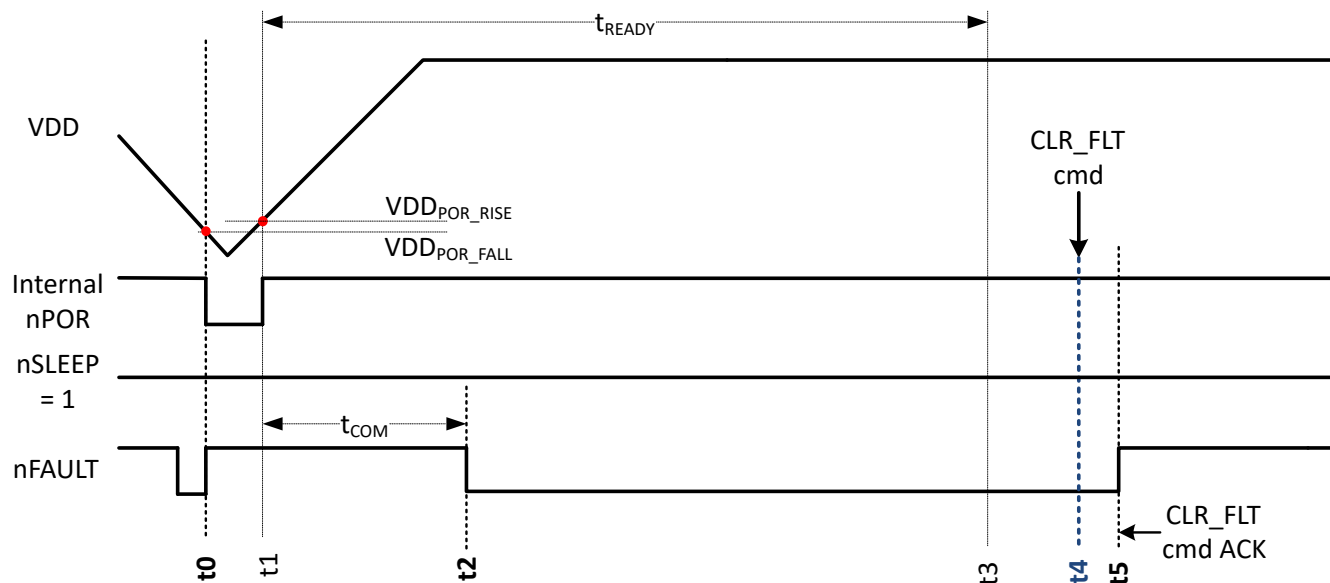


Figure 6-8. Power-up via VDD to STANDBY State Transition

Hand shake between controller and device during power-up as follows:

- t0: Device internal state - POR asserted based on under voltage on VDD (external supply)
- t1: Device internal state – POR de-asserted based on recovery of voltage on VDD (external supply)
- t2: Device – nFAULT asserted low to acknowledge wake-up and indicate device ready for communication
- t3: Device internal state - Initialization complete
- t4 (Any time after t3): **Controller – Issue CLR_FLT command** through SPI to acknowledge device power-up
- t5: Device - nFAULT de-asserted as an acknowledgment of CLR_FLT command. Device in STANDBY state

6.8.3 Fault Reaction Transients

6.8.3.1 Retry setting

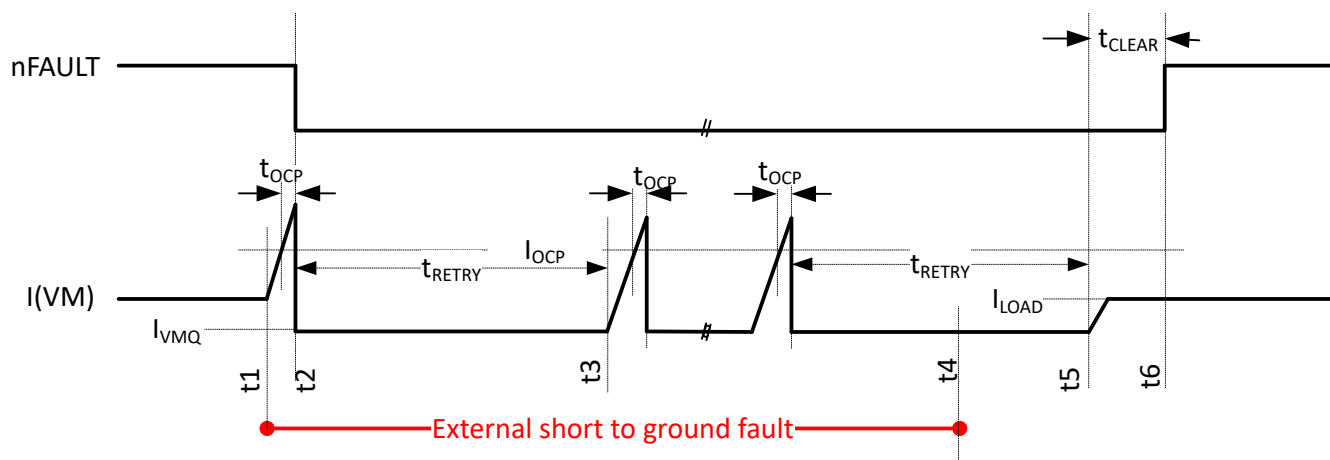


Figure 6-9. Fault reaction with RETRY setting (shown for OCP occurrence on high-side when OUT is shorted to ground)

Short occurrence and recovery scenario with RETRY setting:

- t1: An external short occurs.
- t2: OCP (Over Current Protection) fault confirmed after t_{OCP} , output disabled, nFAULT asserted low to indicate fault.

- t3: Device automatically attempts retry (auto retry) after t_{RETRY} . Each time output is briefly turned on to confirm short occurrence and then immediately disabled after t_{OCP} . nFAULT remains asserted low through out. Cycle repeats till driver is disabled by the user or external short is removed, as illustrated further. Note that, in case of a TSD (Thermal Shut Down) event, automatic retry time depends on the cool off based on thermal hysteresis.
- t4: The external short is removed.
- t5: Device attempts auto retry. But this time, no fault occurs and device continues to keep the output enabled.
- t6: After a fault free operation for a period of t_{CLEAR} is confirmed, nFAULT is de-asserted.
- SPI variant only – Fault status remains latched until a CLR_FLT command is issued.

Note that, in the event of an output short to ground causing the high-side OCP fault detection, IPROPI pin will continue to be pulled up to V_{IPROPI_LIM} voltage to indicate this type of short, while the output is disabled. This is especially useful for the HW variant to differentiate the indication of a short to ground fault from the other faults.

6.8.3.2 Latch setting

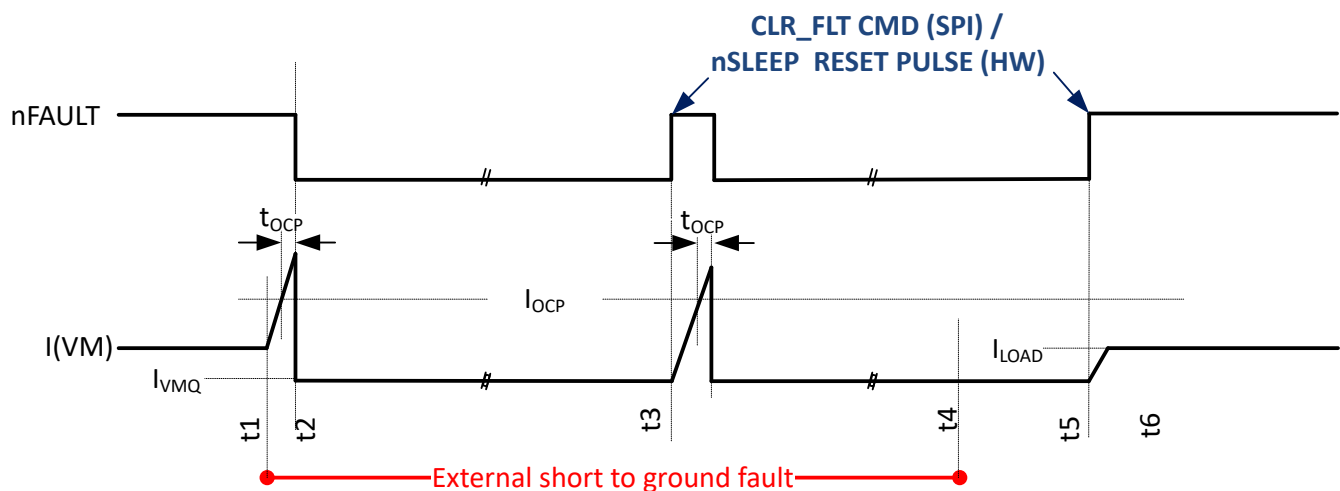


Figure 6-10. Fault reaction with Latch setting (shown for OCP occurrence on high-side when OUT is shorted to ground)

Short occurrence and recovery scenario with LATCH setting:

- t1: An external short occurs.
- t2: OCP (Over Current Protection) fault confirmed after t_{OCP} , output disabled, nFAULT asserted low to indicate fault.
- t3: A CLR_FLT command (SPI variant) or nSLEEP RESET Pulse (HW variant) issued by controller. nFAULT is de-asserted and output is enabled. OCP fault is detected again and output is disabled with nFAULT asserted low.
- t4: The external short is removed.
- t5: A CLR_FLT command (SPI variant) or nSLEEP RESET Pulse (HW variant) issued by controller. nFAULT is de-asserted and output is enabled. Normal operation resumes.
- SPI variant only – Fault status remains latched until a CLR_FLT command is issued.

Note that, in the event of an output short to ground causing the high-side OCP fault detection, IPROPI pin will continue to be pulled up to V_{IPROPI_LIM} voltage to indicate this type of short, while the output is disabled. This is especially useful for the HW variant to differentiate the indication of a short to ground fault from the other faults.

6.9 Typical Characteristics

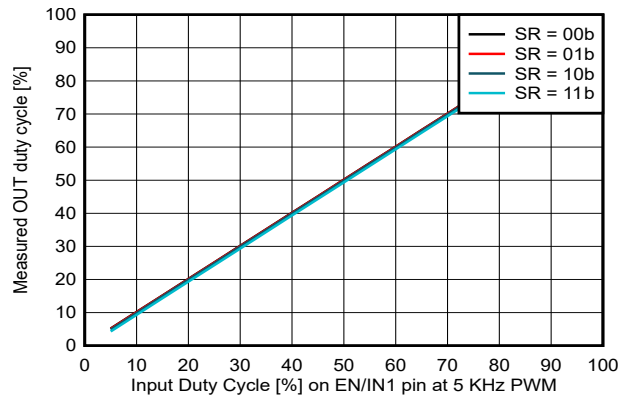


Figure 6-11. Measured Duty Cycle vs Input Duty Cycle at PWM Frequency of 5KHz at $V_M = 48V$ for HS Recirculation

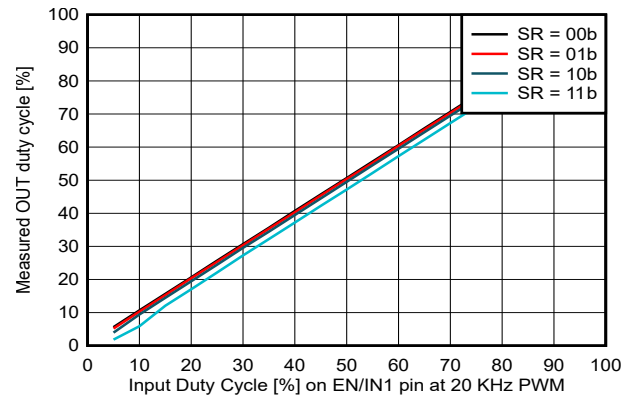


Figure 6-12. Measured Duty Cycle vs Input Duty Cycle at PWM Frequency of 20KHz at $V_M = 48V$ for HS Recirculation

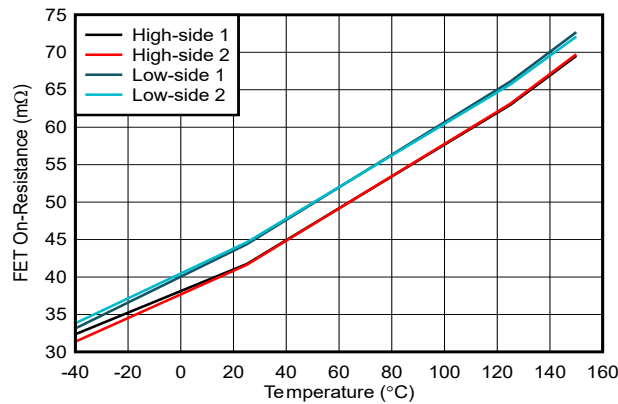


Figure 6-13. R_{HS_ON} & R_{LS_ON} vs Temperature at $V_M = 48V$

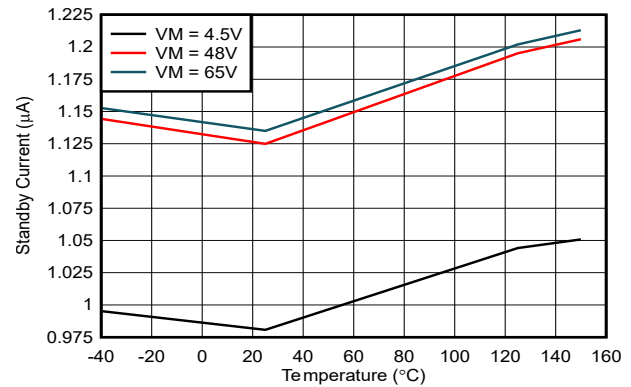


Figure 6-14. Current on VM in STANDBY state vs Temperature

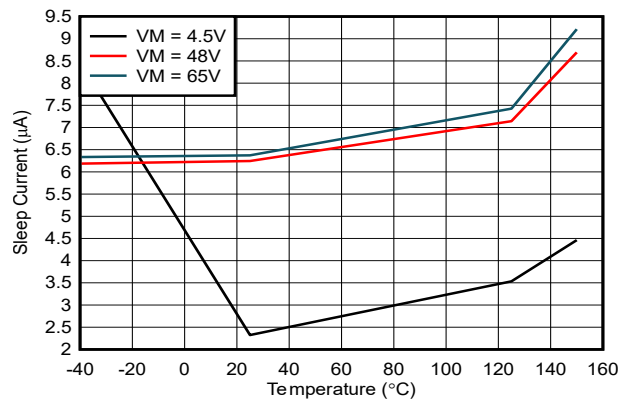


Figure 6-15. Current on VM in SLEEP state vs Temperature

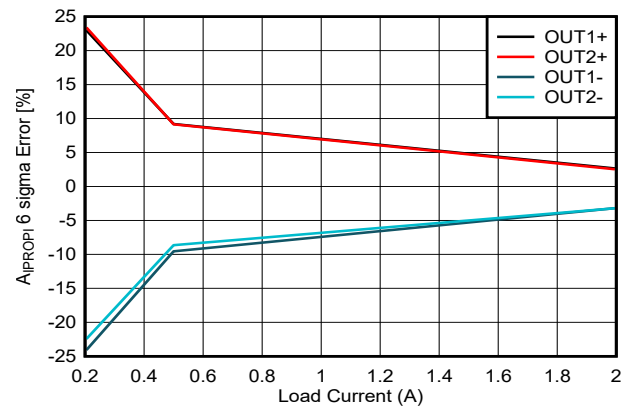


Figure 6-16. A_{IPROPI} Gain Error vs Load Current at $V_M = 48 V$

7 Detailed Description

7.1 Overview

The DRV8263-Q1 is a brushed DC motor driver that operates from 4.5 to 65V supporting a wide range of output load currents for various types of motors and loads. The device integrates an H-bridge output power stage that can be operated in three different control modes set by the MODE function. The device integrates a charge pump regulator to support efficient high-side N-channel MOSFETs with 100% duty cycle operation. The device operates from a power supply input (VM) which can be directly connected to a battery or DC voltage supply. The device also provides a low-power mode to minimize current draw during system inactivity. The digital block of the device is powered by an external supply input through the VDD pin. Both VM & VDD are required for operation.

The device is available in two interface variants -

1. HW variant - The hardwired interface variant is available for easy device configuration. Due to the limited number of available pins in the device, this variant offers fewer configuration and fault reporting capabilities compared to the SPI variant.
2. SPI variant - A standard 4-wire serial peripheral interface (SPI) with daisy chain capability allows flexible device configuration and detailed fault reporting to an external controller. The feature differences of the SPI and HW variants can be found in the [device comparison](#) section.

The DRV8263-Q1 device provides a load current sense output using current mirrors on the high-side power MOSFETs. The IPROPI pin sources a small current that is proportional to the current in the high-side MOSFETs (current sourced out of the OUTx pin). This current can be converted to a proportional voltage using an external resistor (R_{IPROPI}). Additionally, for the SPI variant, the IPROPI pin can be programmed to output a current proportional to the die temperature. The device also supports a fixed off-time PWM chopping scheme for limiting current to the load. The current regulation level can be configured through the ITRIP function.

A variety of protection features and diagnostic functions are integrated into the device. These include supply voltage monitor (VMUV and VMOV), off-state (Passive) diagnostics (OLP), on-state (Active) diagnostics (OLA), overcurrent protection (OCP) for each power FET, powered-off braking (POB), over-temperature warning (OTW) and die temperature monitor, and over-temperature shutdown (TSD). Fault conditions are indicated on the nFAULT pin. The SPI variant has additional communication protection features such as frame errors and lock features for configuration register bits and driver control bits.

7.2 Functional Block Diagram

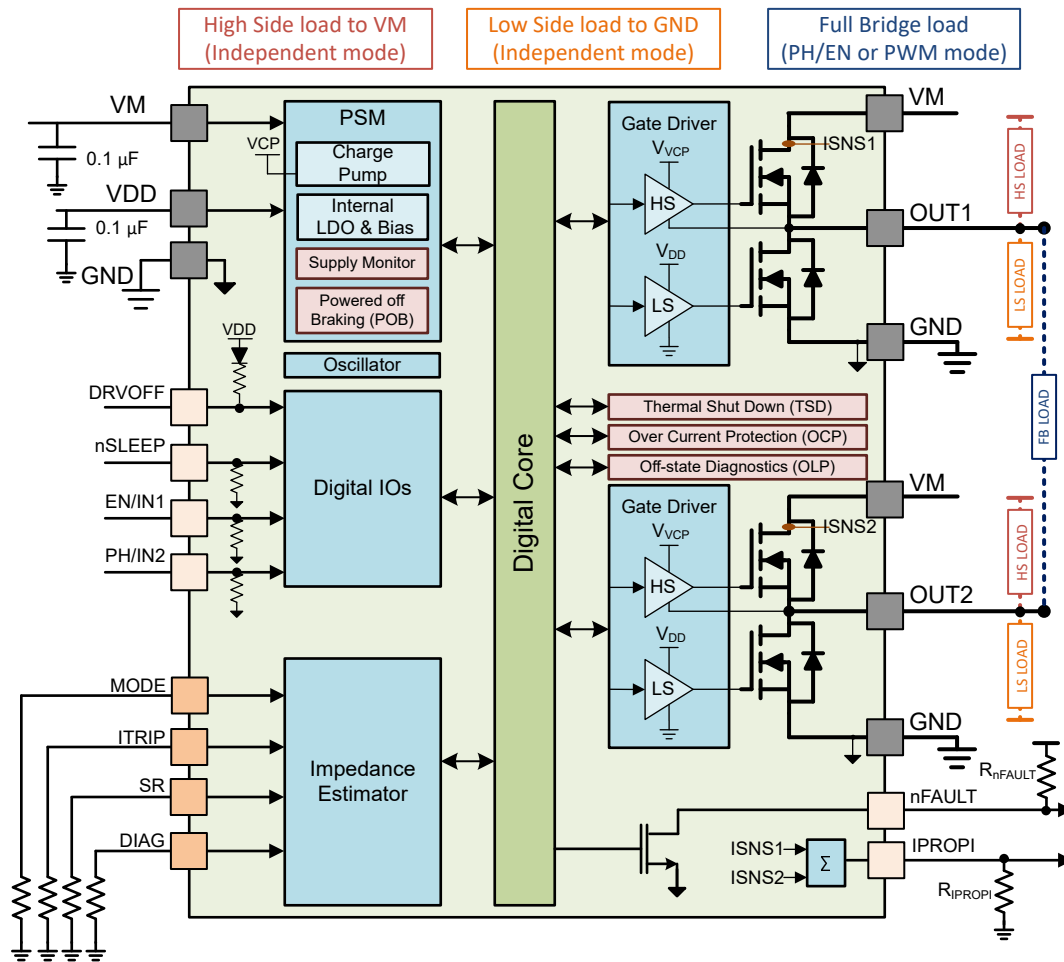


Figure 7-1. Functional Block Diagram - HW Variant

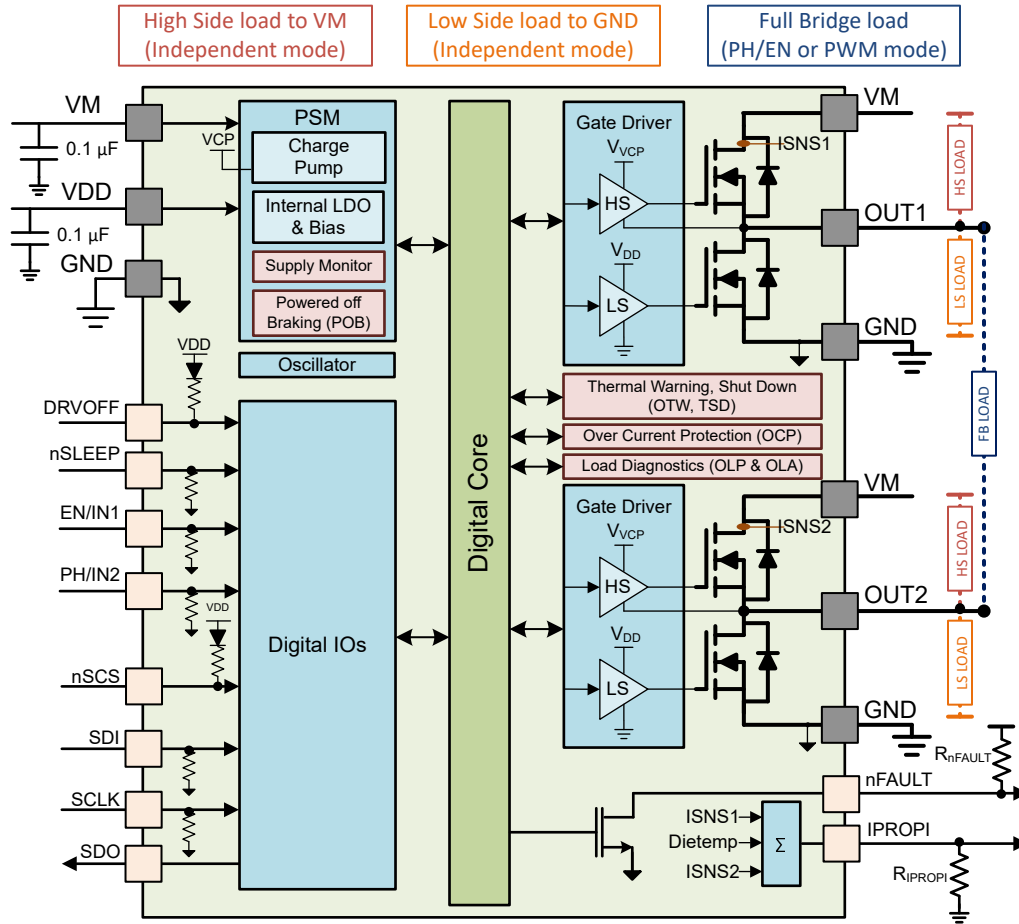


Figure 7-2. Functional Block Diagram - SPI Variant

7.3 Feature Description

7.3.1 External Components

Table 7-1 and Table 7-2 contain the recommended external components for the device.

7.3.1.1 HW Variant

Table 7-1. External Components Table for HW Variant

Component	PIN	Recommendation
C_{VM1}	VM	0.1μF, low ESR ceramic capacitor to GND rated for VM
C_{VM2}	VM	Local bulk capacitor to GND, 10μF or higher, rated for VM to handle load transients. Refer to the section on bulk capacitor sizing.
C_{VDD}	VDD	0.1μF, 6.3V, low ESR ceramic capacitor to GND.
R_{IPROPI}	IPROPI	Typically 500 - 5000Ω 0.063 W resistor to GND, depending on the controller ADC dynamic range. The pin can be shorted to GND if ITRIP and IPROPI function is not needed.
C_{IPROPI}	IPROPI	Optional 10 - 100nF, 6.3V capacitor to GND to slow down the ITRIP regulation loop. Refer Over Current Protection (OCP) section .
R_{nFAULT}	nFAULT	Typically 1KΩ - 10KΩ, 0.063W pull-up resistor to controller supply.
R_{SR}	SR	Open or short to GND or 0.063W 10% resistor to GND depending on the setting. Refer SR section .
R_{ITRIP}	ITRIP	Open or short to GND or 0.063W 10% resistor to GND depending on the setting. Refer ITRIP table .

Table 7-1. External Components Table for HW Variant (continued)

Component	PIN	Recommendation
R _{DIAG}	DIAG	Open or short to GND or 0.063W 10% resistor to GND depending on the setting. Refer DIAG section .

7.3.1.2 SPI Variant**Table 7-2. External Components Table for SPI Variant**

Component	PIN	Recommendation
C _{VM1}	VM	0.1μF, low ESR ceramic capacitor to GND rated for VM
C _{VM2}	VM	Local bulk capacitor to GND, 10μF or higher, rated for VM to handle load transients. Refer to the section on bulk capacitor sizing.
C _{VDD}	VDD	0.1μF, 6.3V, low ESR ceramic capacitor to GND.
R _{IPROPI}	IPROPI	Typically 500 - 5000 Ω 0.063W resistor to GND, depending on the controller ADC dynamic range. The pin can be shorted to GND if ITRIP and IPROPI function is not needed.
C _{IPROPI}	IPROPI	Optional 10 - 100nF, 6.3V capacitor to GND to slow down the ITRIP regulation loop. Refer Over Current Protection (OCP) section .
R _{nFAULT}	nFAULT	Typically 1KΩ - 10KΩ, 0.063W pull-up resistor to controller supply. If nFAULT signaling is not used, this pin can be short to GND or left open.

7.3.2 Bridge Control

The DRV8263-Q1 device provides three separate modes to support different control schemes with the EN/IN1 and PH/IN2 pins. The control mode is selected through the MODE setting. MODE is a 3-level setting based on the MODE pin for the HW variant or S_MODE bits in the [CONFIG3](#) register for the SPI variant as summarized in [Table 7-3](#):

Table 7-3. Mode table

MODE pin	S_MODE bits	Device Mode	Description
R _{LVL1}	00b	PH/EN mode	full-bridge mode where EN/IN1 is the PWM input, PH/IN2 is the direction input
R _{LVL2}	01b	Independent mode	Independent control for 2 half-bridges
R _{LVL3}	10b, 11b	PWM mode	full-bridge mode where EN/IN1 and PH/IN2 control the PWM respectively depending on the direction
R _{LVL4} (DRV8263A-Q1)	P_EN = 1b	Parallel mode	parallel Half-bridge mode where input is synchronized for OUT1 and OUT2, outputs can be tied together

In the HW variant, MODE pin is latched during device initialization following power-up or wake-up from sleep. Update during operation is blocked.

In the SPI variant of the device, the mode setting can be changed anytime the SPI communication is available by writing to the S_MODE bits and P_EN bit. This change is immediately reflected.

The inputs can accept static or pulse-width modulated (PWM) voltage signals for either 100% or PWM drive modes. The device input pins can be powered before VM is applied. By default, the nSLEEP and DRVOFF pins have an internal pull-down and pull-up resistor respectively, to maintain the outputs are Hi-Z if no inputs are present. Both the EN/IN1 and PH/IN2 pins also have internal pull down resistors. The sections below show the truth table for each control mode.

The device automatically generates the desired dead-time needed during transitioning between the high-side and low-side FET on the switching half-bridge. This timing is based on internal FET gate-source voltage feedback. No external timing is required. This scheme provides for minimum dead time, while guaranteeing no shoot-through current.

Note

1. The SPI variant also provides additional control through the SPI_IN register bits. Refer to - [Register - Pin control](#).

7.3.2.1 PH/EN mode

In this mode, the two half-bridges are configured to operate as a full-bridge. EN/IN1 is the PWM input and PH/IN2 is the direction input.

Table 7-4. Control table - PH/EN mode

nSLEEP	DRVOFF	EN/IN1	PH/IN2	OUT1	OUT2	Device State
0	X	X	X	Hi-Z	Hi-Z	SLEEP
1	1	0	0	Hi-Z	Hi-Z	STANDBY
1	1	1	0	Refer Off-state diagnostics table		STANDBY
1	1	0	1			
1	1	1	1			
1	0	0	X	H	H	ACTIVE
1	0	1	0	L ⁽¹⁾	H	ACTIVE
1	0	1	1	H	L ⁽¹⁾	ACTIVE

(1) If internal ITRIP regulation is enabled and ITRIP level is reached, then OUTx is forced "H" for a fixed time

7.3.2.2 PWM mode

In this mode, the two half-bridges are configured to operate as a full-bridge. EN/IN1 provides the PWM input in one direction, while PH/IN2 provides the PWM in the other direction.

Table 7-5. Control table - PWM mode

nSLEEP	DRVOFF	EN/IN1	PH/IN2	OUT1	OUT2	Device State
0	X	X	X	Hi-Z	Hi-Z	SLEEP
1	1	0	0	Hi-Z	Hi-Z	STANDBY
1	1	1	0	Refer Off-state diagnostics table		STANDBY
1	1	0	1			STANDBY
1	1	1	1			STANDBY
1	0	0	0	H	H	ACTIVE
1	0	0	1	L ⁽¹⁾	H	ACTIVE
1	0	1	0	H	L ⁽¹⁾	ACTIVE
1	0	1	1	Hi-Z	Hi-Z	STANDBY

(1) If internal ITRIP regulation is enabled and ITRIP level is reached, then OUTx is forced "H" for a fixed time

For the SPI variant, by setting the EXTEND bit in the [CONFIG2](#) register, there are additional Hi-Z states that are possible, when a forward ([EN/IN1 PH/IN2] = [1 0]) or reverse ([EN/IN1 PH/IN2] = [0 1]) command is followed by a Hi-Z command ([EN/IN1 PH/IN2] = [1 1]). In this condition of Hi-Z (coasting), only the half-bridge involved with the PWM is Hi-Z, while the HS FET on the other half-bridge is kept ON. The determination on which half-bridge to Hi-Z is made based on the previous cycle. This is summarized in [Table 7-6](#).

Table 7-6. PWM EXTEND table (EXTEND bit = 1b)

PREVIOUS STATE		CURRENT STATE			Device State Transition
OUT1	OUT2	OUT1	OUT2	IPOPI	
Hi-Z	Hi-Z	Hi-Z	Hi-Z	No current	Remains in STANDBY, no change
H	H	Hi-Z	Hi-Z	No current	ACTIVE to STANDBY
L	H	Hi-Z	H	ISNS2	ACTIVE to STANDBY

Table 7-6. PWM EXTEND table (EXTEND bit = 1b) (continued)

PREVIOUS STATE		CURRENT STATE			Device State Transition
OUT1	OUT2	OUT1	OUT2	IPOPI	
H	L	H	Hi-Z	ISNS1	ACTIVE to STANDBY

7.3.2.3 Independent mode

In this mode, the two half-bridges are configured to be used as two independent half-bridges. The [Table 7-7](#) shows the logic table for bridge control.

Table 7-7. Control table - Independent mode

nSLEEP	DRVOFF	EN/IN1	PH/IN2	OUT1	OUT2	Device State
0	X	X	X	Hi-Z	Hi-Z	SLEEP
1	1	0	0	Hi-Z	Hi-Z	STANDBY
1	1	1	0	Refer Off-state diagnostics table		STANDBY
1	1	0	1			STANDBY
1	1	1	1			STANDBY
1	0	0	0	L	L	ACTIVE
1	0	0	1	L	H ⁽¹⁾	ACTIVE
1	0	1	0	H ⁽¹⁾	L	ACTIVE
1	0	1	1	H ⁽¹⁾	H ⁽¹⁾	ACTIVE

For the SPI variant, it is possible to have independent Hi-Z control of both half-bridges through equivalent bits, S_DRVOFF & S_DRVOFF2 in the [SPI_IN](#) register, when the **SPI_IN register has been unlocked**. [Table 7-8](#) shows the logic table for bridge control using the pin & register combined inputs. Refer to - [Register - Pin control](#) for details on the combined inputs shown in [Table 7-8](#).

Table 7-8. Control table - Independent mode for SPI variant, when SPI_IN is unlocked

nSLEEP	DRVOFF1 combined	DRVOFF2 combined	EN_IN1 combined	PH_IN2 combined	OUT1	OUT2	Device State
0	X	X	X	X	Hi-Z	Hi-Z	SLEEP
1	1	1	0	0	Hi-Z	Hi-Z	STANDBY
1	1	1	1	0	Refer Off-state diagnostics table		STANDBY
1	1	1	0	1			STANDBY
1	1	1	1	1			STANDBY
1	1	0	X	0	Hi-Z	L	ACTIVE
1	1	0	X	1	Hi-Z	H ⁽¹⁾	ACTIVE
1	0	1	0	X	L	Hi-Z	ACTIVE
1	0	1	1	X	H ⁽¹⁾	Hi-Z	ACTIVE
1	0	0	0	0	L	L	ACTIVE
1	0	0	0	1	L	H ⁽¹⁾	ACTIVE
1	0	0	1	0	H ⁽¹⁾	L	ACTIVE
1	0	0	1	1	H ⁽¹⁾	H ⁽¹⁾	ACTIVE

(1) If internal ITRIP regulation is enabled and ITRIP level is reached, then OUTx is forced "L" for a fixed time

In this mode, the device behavior is as listed below:

- Load current can be sensed only for current from VM → OUTx → Load. So current sense is not possible for high-side loads.
- For the SPI variant, the current on IPOPI pin can be configured to be the current of either half-bridge or the sum of the high-side sense current from both the half-bridges, as per the ISEL bits.

- For the HW variant, the current on IPROPI pin is the sum of the high-side sense current from both the half-bridges. This limits the ITRIP current regulation feature as a combined current regulation, rather than as truly independent.
- Slew rate configurability is limited for low-side recirculation (low-side loads)
- Active state open load diagnostics (OLA) is possible only for high-side loads
- For the HW variant, it is NOT possible to have independent Hi-Z control of each half-bridge. Asserting DRVOFF pin high will Hi-Z both the half-bridges.

7.3.2.4 Register - Pin Control - SPI Variant Only

The SPI variant allows control of the bridge through the specific register bits, S_DRVOFF, S_DRVOFF2, S_ENIN1, S_PHIN2 in the [SPI_IN](#) register, provided the **SPI_IN register has been unlocked**. The user can unlock this register by writing the right combination to the SPI_IN_LOCK bits in the [COMMAND](#) register.

Additionally, the user can configure between an AND / OR logic combination of each of external input pin with their equivalent register bit in the SPI_IN register. This logical configuration is done through the equivalent selects bits in the [CONFIG4](#) register:

- DRV_SEL, ENIN1_SEL and PHIN2_SEL

The control of the output is similar to the truth tables described in the section before, but with these logically combined inputs. These combined inputs are listed as follows:

- Combined input = Pin input **OR** equivalent SPI_IN register bit, if equivalent CONFIG4 select bit = 0b
- Combined input = Pin input **AND** equivalent SPI_IN register bit, if equivalent CONFIG4 select bit = 1b
- In Independent mode:
 - DRVOFF2 combined = DRVOFF pin **OR** S_DRVOFF2 bit, if DRV_SEL bit = 0b
 - DRVOFF2 combined = DRVOFF pin **AND** S_DRVOFF2 bit, if DRV_SEL bit = 1b

Note that external nSLEEP pin is still needed for sleep function.

This logical combination offers more configurability to the user as shown in the table below.

Table 7-9. Register - Pin Control Examples

Example	CONFIG4: xxx_SEL Bit	PIN status	SPI_IN Bit Status	Comment
DRVOFF as redundant shutoff	DRV_SEL = 0b	DRVOFF active	S_DRVOFF active	Either DRVOFF pin = 1 or S_DRVOFF bit = 1 will shutoff the output
Pin only control	DRV_SEL = 1b	DRVOFF active	S_DRVOFF = 1b	Only DRVOFF pin function is available
Register only control	PHIN2_SEL bit = 0b	PH/IN2 - short to GND or float	S_PHIN2 active	PH (direction) will be controlled by the register bit alone

7.3.3 Device Configuration

This section describes the various device configurations to enable the user to configure the device to suit their use case.

7.3.3.1 Slew Rate (SR)

The SR pin (HW variant) or SR bit in the [CONFIG3](#) and EXT_SR bits in [CONFIG5](#) register (SPI variant) determines the voltage slew rate of the driver output. This enables the user to optimize the PWM switching losses while meeting the EM conformance requirements. The device supports four slew rate settings and two additional extended slew rate options. Depending on the use case, refer to the switching parameters table for either high-side recirculation or low-side recirculation in the [Section 6.4](#) section for the slew rate range and values.

Note

The SPI variant also offers an **optional** spread spectrum clocking (SSC) feature that spreads the internal oscillator frequency +/- 12% around the mean with a period triangular function of approximately 1.3MHz to reduce emissions at higher frequencies. There is **no** spread spectrum clocking (SSC) feature in the HW variant.

In the HW variant, the SR pin is **latched** during device initialization following power-up or wake-up from sleep. Update during operation is blocked.

In the SPI variant, the slew rate setting can be changed at any time when SPI communication is available by writing to the SR bit. This change is immediately reflected.

7.3.3.2 IPROPI

The device features an output (IPROPI pin) for current sensing and die temperature measurement. This information can be used for status or regulation of loads (on OUTx), or to check die temperature. These integrated features eliminate the need for multiple external sense resistors or sense circuitry, reducing system size, cost and complexity.

The device senses the load current by using a shunt-less high-side current mirror topology. This way the device can only sense an uni-directional high-side current from VM → OUTx → Load through the high-side FET when it is fully turned ON (linear mode).

The IPROPI pin must be connected to an external resistor (R_{IPROPI}) to ground in order to generate a proportional voltage V_{IPROPI} . This allows for the load current to be measured as a voltage-drop across the R_{IPROPI} resistor with an analog to digital converter (ADC). The R_{IPROPI} resistor can be sized based on the expected load current in the application so that the full range of the controller ADC is utilized.

Depending on the ISEL bits setting or the EXT_ISEL bits for DRV8263A-Q1, the IPROPI pin can also output analog current representation of the die temperature. This is intended for use in testing and evaluation, but not during device run-time.

Table 7-10. ISEL settings for DRV8263-Q1

Interface	S_MODE	MODE	ISEL	IPROPI
SPI	00b, 10b, 11b	PH/EN or PWM, full-bridge mode	11b	$(I_{HS1} + I_{HS2}) \times A_{IPROPI}$
			EXT_ISEL = 10b	$I_{HS2} \times A_{IPROPI}$ (DRV8263A-Q1)
			EXT_ISEL = 01b	$I_{HS1} \times A_{IPROPI}$ (DRV8263A-Q1)
			00b	Die Temperature Readout
	01b	Independent half-bridge mode	11b	$(I_{HS1} + I_{HS2}) \times A_{IPROPI}$
			10b	$I_{HS2} \times A_{IPROPI}$
			01b	$I_{HS1} \times A_{IPROPI}$
			00b	Die Temperature Readout
	P_EN = 1b	Parallel half-bridge mode (DRV8263A-Q1)	11b	Reserved
			10b	Reserved
			01b	$(I_{HS1} + I_{HS2}) \times A_{IPROPI}$
			00b	Die Temperature Readout
HW	NA	PH/EN or PWM (full-bridge mode) or Independent half-bridge mode	NA	$(I_{HS1} + I_{HS2}) \times A_{IPROPI}$

Note

ISEL = 01b or 10b are not recommended in full-bridge mode, use EXT_ISEL for DRV8263A-Q1 as applicable

When the IPROPI output is configured for die temperature readout, the device outputs a current as per the following formula -

$$\text{Current } (\mu\text{A}) = 3.00 * (\text{Temperature in } ^\circ\text{C}) + 863$$

This equation is valid for temperatures between -40 °C and 185 °C. For example, when the die temperature is 85° C and ISEL is selected for the die temperature readout, current out of the IPROPI pin will be 1.118mA.

7.3.3.3 ITRIP Regulation

The device offers an optional internal load current regulation feature using fixed TOFF time method. This is done by comparing the voltage on the IPROPI pin against a reference voltage determined by ITRIP setting. TOFF time is fixed at 30μsec for HW variant, while TOFF time is configurable between 20 to 50μsec for the SPI variant using TOFF bits in the [CONFIG3](#) register.

The ITRIP regulation, when enabled, comes into action only when the HS FET is enabled and current sensing is possible. In this scenario, when the voltage on the IPROPI pin exceeds the reference voltage set by the ITRIP setting, the internal current regulation loop forces the following action:

- In PH/EN or PWM mode, OUT1 = H, OUT2 = H (high-side recirculation) for the fixed TOFF time
 - Cycle skipping: Due to minimum duty cycle limitations (especially at low slew rate settings and high VM), load current continues to increase even with ITRIP regulation. To prevent this current walk away, a cycle skipping scheme is implemented, where, if IOUT sensed is still greater than ITRIP at the end of TOFF time, then the recirculation time is extended by an additional TOFF period. This recirculation time addition continues till IOUT sensed is less than ITRIP at the end of the TOFF period.
- In Independent mode, If OUTx = H, then toggle OUTx = L for the fixed TOFF time, else no action on OUTx

Note

The user inputs always takes **precedence** over the internal control. That means that if the inputs change during the TOFF time, the remainder of the TOFF time is ignored and the outputs follows the inputs as commanded.

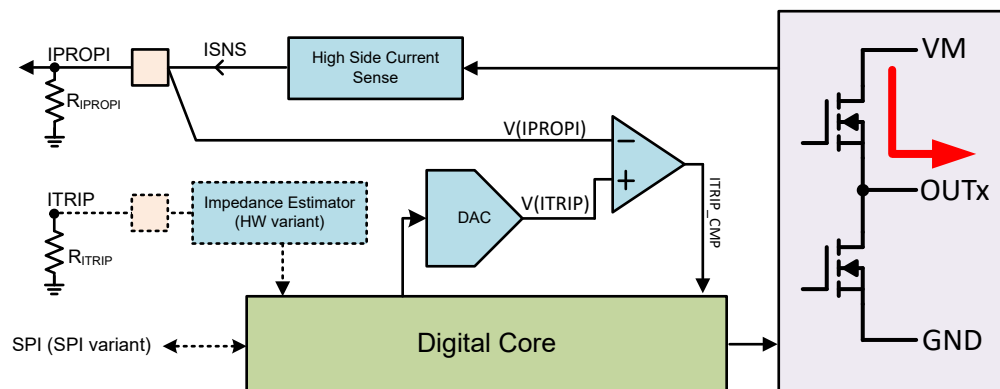


Figure 7-3. ITRIP Implementation

The current limit is set by the following equation:

$$\text{ITRIP regulation level} = V_{ITRIP} / (R_{IPROPI} \times A_{IPROPI}) \quad (2)$$

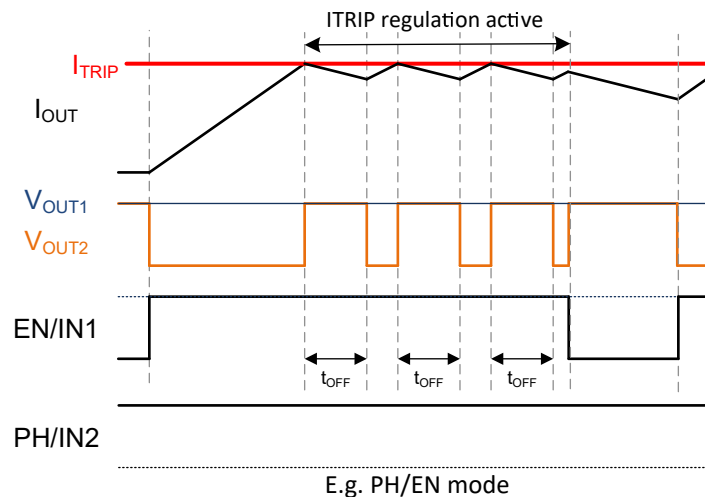


Figure 7-4. Fixed TOFF ITRIP Current Regulation

In Independent mode, the ITRIP function is not independent. If either bridge reaches ITRIP, any half-bridge with OUTx pin high is toggled low for TOFF duration.

The ITRIP comparator output (ITRIP_CMP) is ignored during output slewing to avoid false triggering of the comparator output due to current spikes from the load capacitance. Additionally, in the event of transition from low-side recirculation, an additional blanking time t_{BLANK} is needed for the sense loop to stabilize before the ITRIP comparator output is valid.

ITRIP is a 6-level setting for the HW variant. The SPI variant offers two more settings. This is summarized in the table below:

Table 7-11. ITRIP Table

ITRIP Pin	S_ITRIP Register Bits	V _{ITRIP} [V]
R _{LVL1}	000b	Regulation Disabled
R _{LVL2}	001b	1.2
Not available	010b	1.44
Not available	011b	1.67
R _{LVL3}	100b	2.00
R _{LVL4}	101b	2.34
R _{LVL5}	110b	2.67
R _{LVL6}	111b	3.00

In the HW variant of the device, the ITRIP pin changes are **transparent** and changes are reflected immediately.

In the SPI variant of the device, the ITRIP setting can be changed at any time when SPI communication is available by writing to the S_ITRIP bits. This change is immediately reflected in the device behavior.

SPI variant only - If the ITRIP regulation levels are reached, the ITRIP_CMP bit in the [STATUS1](#) register is set. There is no nFAULT pin indication. This bit can be cleared with a CLR_FLT command.

Note

If the application requires a linear ITRIP control with multiple steps beyond the choices provided by the device, an external DAC can be used to force the voltage on the bottom side of the IPROPI resistor, instead of terminating the voltage to GND. With this modification, the ITRIP current can be controlled by the external DAC setting as follows:

$$\text{ITRIP regulation level} = (V_{\text{ITRIP}} - V_{\text{DAC}}) / (R_{\text{IPROPI}} \times A_{\text{IPROPI}}) \quad (3)$$

7.3.3.4 DIAG

The DIAG is a pin (HW variant) or register (SPI variant) setting that is used in both ACTIVE and STANDBY operation of the device, as follows:

- STANDBY state
 - In PH/EN or PWM modes: Enable or disable [Off-state diagnostics \(OLP\)](#), as well as enable or disable POB.
 - In Independent mode: Enable or disable [Off-state diagnostics \(OLP\)](#), as well as select the OLP combinations when enabled. Refer to the tables in the [Off-state diagnostics \(OLP\)](#) section for details on this.
- ACTIVE state
 - In Independent mode: Mask ITRIP regulation function if the load type is indicated as high-side load.
 - SPI variant only - In Independent mode: Mask active open load detection (OLA) if the load type is indicated as low-side load.
 - HW variant only - configure device wake-up and fault reaction between retry and latch settings

7.3.3.4.1 HW variant

For the HW variant, the DIAG pin is a 6-level setting. Depending on the mode, the configurations are summarized in the table below.

Table 7-12. DIAG table for the HW variant, PH/EN or PWM mode

DIAG pin	Off-state diagnostics	nSLEEP Wakeup Pulse	POB	Fault reaction
R _{LVL1}	Disabled	Not Required	Disabled	Retry
R _{LVL2}	Disabled	Not Required	Disabled	Latch
R _{LVL3}	Disabled	Not Required	Enabled	Latch
R _{LVL4}	Enabled	Not Required	Disabled	Latch
R _{LVL5}	Disabled	Required	Disabled	Latch
R _{LVL6}	Enabled	Not Required	Enabled (only in sleep mode)	Latch

Table 7-13. DIAG table for the HW variant, Independent mode

DIAG pin	STANDBY state		ACTIVE state		
	Off-state diagnostics	nSLEEP wake pulse	Load Configuration	Fault reaction	IPROPI / ITRIP
R _{LVL1}	Disabled	Not required	Low-side load	Retry	Available
R _{LVL2}	Enabled	Required	Low-side load	Latch	Available
R _{LVL3}	Enabled	Required	High-side load	Latch	Disabled
R _{LVL4}	Enabled	Not required	High-side load	Retry	Disabled
R _{LVL5}	Disabled	Required	Low-side load	Latch	Available
R _{LVL6}	Enabled	Not required	Low-side load	Retry	Available

Note

HW variant only - In Independent mode: Option to disable off-state diagnostics for a high-side load use case is not supported. In this case, setting DRVOFF pin high and IN pin low is only way to disable off-state diagnostics.

In the HW variant, the DIAG pin is **latched** during device initialization following power-up or wake-up from sleep. Update during operation is blocked.

7.3.3.4.2 SPI variant

For the SPI variant, S_DIAG is a 2-bit setting in the [CONFIG2](#) register. Depending on the mode, its configurations are summarized in the table below.

Table 7-14. DIAG table for the SPI variant, PH/EN or PWM mode

S_DIAG bits	STANDBY state	ACTIVE state
	Off-state diagnostics	On-state diagnostics
00b	Disabled	Available
01b, 10b, 11b	Enabled	Available

Table 7-15. DIAG table for the SPI variant, Independent mode

S_DIAG bits	STANDBY state	ACTIVE state		
	Off-state diagnostics	Load Configuration	On-state diagnostics	IPROPI / ITRIP
00b	Disabled	Low-side load	Disabled	Available
01b	Enabled ⁽¹⁾	Low-side load	Disabled	Available
10b	Disabled	High-side load	Available	Disabled
11b	Enabled ⁽¹⁾	High-side load	Available	Disabled

In the SPI variant of the device, the settings can be changed anytime when SPI communication is available by writing to the S_DIAG bits. This change is immediately reflected.

7.3.4 Protection and Diagnostics

The driver is protected against over-current and over-temperature events to maintain device robustness. Additionally, the device also offers load monitoring (on-state and off-state) and over / under voltage monitoring on VM pin to signal any unexpected conditions. Fault signaling is done through a low-side open drain nFAULT pin which gets pulled to GND on detection of a fault condition. Transition to SLEEP state automatically de-asserts nFAULT.

Note

In the SPI variant, nFAULT pin logic level is the inverted copy of the FAULT bit in the FAULT register. Only exception is when off-state diagnostics are enabled and SPI_IN register is locked (Refer [OLP section](#)).

For the SPI variant, whenever nFAULT is asserted low, the device logs the fault into the FAULT and STATUS registers. These registers can be cleared only by CLR_FLT command.

Getting all the useful diagnostic information for periodic software monitoring in a single 16 bit SPI frame is possible by:

- Reading the STATUS1 register during ACTIVE state
- Reading the STATUS2 register during STANDBY state

All the diagnosable fault events can be uniquely identified by reading the STATUS registers.

7.3.4.1 Over Current Protection (OCP)

- Device state: ACTIVE
- Mechanism & thresholds: An analog current limit circuit on each MOSFET limits the peak current out of the device even in hard short circuit events. If the output current exceeds the overcurrent threshold, I_{OCP} , for longer than t_{OCP} , then an over current fault is detected.
- Action:
 - nFAULT pin is asserted low
 - Reaction is based on mode selection:

- PH/EN or PWM mode - Both OUTx is Hi-Z
- Independent mode - the affected half-bridge OUTx is Hi-Z
- For a short to GND fault (over current detected on the high-side FET), the IPROPI pin continues to be pulled up to V_{IPROPI_LIM} even if the FET has been disabled. For the HW variant, this helps differentiate a short to GND fault during ACTIVE state from other fault types, as the IPROPI pin is pulled high while the nFAULT pin is asserted low.
- Reaction configurable between latch setting and retry setting based on t_{RETRY} and t_{CLEAR}
- User can add a capacitor in the range of 10nF to 100nF on the IPROPI pin to ensure OCP detection in case of a load short condition when internal ITRIP regulation is enabled. This is especially true where there is enough inductance in the short that causes ITRIP regulation to trigger ahead of the OCP detection, resulting in the device missing the short detection. To ensure that OCP detection wins this race condition, a small capacitance added on the IPROPI pin slows down the ITRIP regulation loop enough to allow the OCP detection circuit to work as intended.

The SPI variant offers configurable I_{OCP} levels and t_{OCP} filter times. Refer [CONFIG4](#) register for these settings.

7.3.4.2 Over Temperature Warning (OTW) - SPI Variant Only

- Device state: STANDBY, ACTIVE
- Mechanism & thresholds: if the die temperature exceeds T_{OTW} for a time greater than t_{OTW} , then an over temperature warning is detected.
- The OTW_SEL bit programs the T_{OTW} levels. Refer [CONFIG1](#) register for these settings.
- Action:
 - OTW bit is made 1b
 - The device performs no additional action and continues to function
 - If OTW_REP bit is 1b -
 - nFAULT output is pulled low
 - FAULT bit is made 1b
- When the die temperature falls below the hysteresis point (T_{HYS_OTW}) of the overtemperature warning, the OTW bit clears automatically.

7.3.4.3 Over Temperature Protection (TSD)

- Device state: STANDBY, ACTIVE
- Mechanism & thresholds: If the device detects an over temperature event, set by T_{TSD} for a time greater than t_{TSD} , then an over temperature fault is detected.
- Action:
 - nFAULT pin is asserted low
 - Both OUTx is Hi-Z
 - IPROPI pin is Hi-Z
- Reaction configurable between latch setting and retry setting based on T_{HYS} and t_{CLEAR_TSD}

7.3.4.4 Off-State Diagnostics (OLP)

The user can determine the impedance on the OUTx node using off-state diagnostics in the STANDBY state when the power FETs are off. With this diagnostics, it is possible to detect the following fault conditions passively in the STANDBY state:

- Output short to VM or GND
- Open load for full-bridge load or low-side load
- Open load for high-side load

Note

It is NOT possible to detect a **load short** with this diagnostic. However, the user can deduce this logically if an over-current fault (OCP) occurs during ACTIVE operation, but OLP diagnostics do not report any fault in the STANDBY state. The occurrence of both OCP in the ACTIVE state and OLP in the STANDBY state would imply a terminal short (short on OUT node).

- The user can configure the following combinations
 - Internal pull up resistor (R_{OLP_PU}) on OUTx
 - Internal pull down resistor (R_{OLP_PD}) on OUTx
 - Comparator reference level
 - Comparator input selection (OUT1 or OUT2)
- This combination is determined by the controller inputs (pins only for the HW variant) or equivalent bits in the [SPI_IN](#) register for the SPI variant if the SPI_IN register has been unlocked.
- HW variant - When off-state diagnostics are enabled, comparator output (OLP_CMP) is available on nFAULT pin.
- SPI variant - The off-state diagnostics comparator output (OLP_CMP) is available on OLP_CMP bit in [STATUS2](#) register. Additionally, if the SPI_IN register has been locked, this comparator output is also available on the nFAULT pin when off-state diagnostics are enabled.
- The user is expected to toggle through all the combinations and record the comparator output after its output is settled.
- Based on the input combinations and comparator output, the user can determine if there is a fault on the output.

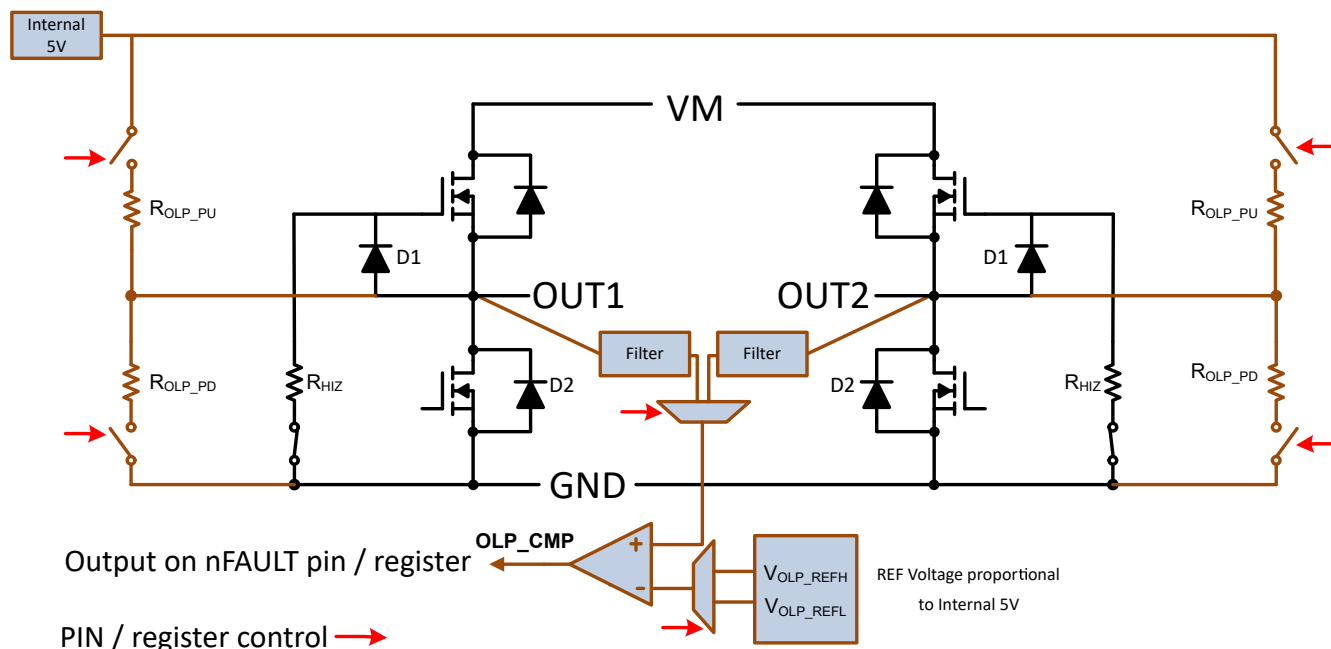


Figure 7-5. Off-State Diagnostics for full-bridge Load (PH/EN or PWM Mode)

The OLP combinations and truth table for a no fault scenario vs. fault scenario for a full-bridge load in [PH/EN](#) or [PWM](#) modes is shown in [Table 7-16](#).

Table 7-16. Off-State Diagnostics Table - PH/EN or PWM Mode (full-bridge)

User Inputs				OLP Set-Up				OLP CMP Output			
nSLEEP	DRVOFF	EN/IN1	PH/IN2	OUT1	OUT2	CMP REF	Output selected	Normal	Open	GND Short	VM Short
1	1	1	0	R_{OLP_PU}	R_{OLP_PD}	V_{OLP_REFH}	OUT1	L	H	L	H
1	1	0	1	R_{OLP_PU}	R_{OLP_PD}	V_{OLP_REFL}	OUT2	H	L	L	H
1	1	1	1	R_{OLP_PD}	R_{OLP_PU}	V_{OLP_REFL}	OUT2	H	H	L	H

The OLP combinations and truth table for a no fault scenario vs. fault scenario for a low-side load in [Independent](#) mode is shown in [Table 7-17](#).

Table 7-17. Off-State Diagnostics Table for Low-Side Load - Independent Mode

User Inputs						OLP Set-Up				OLP_CMP Output		
DIAG pin	S_DIAG bits	nSLEEP	DRVOFF	EN/IN1	PH/IN2	OUT1	OUT2	CMP REF	Output selected	Normal	Open	Short to VM
LVL2, LVL6	01b	1	1	1	don't care	R _{OLP_PU}	Hi-Z	V _{OLP_REF_H}	OUT1	L	H	H
LVL3, LVL4	11b	1	1	1	don't care	R _{OLP_PD}	Hi-Z	V _{OLP_REF_L}	OUT1	L	L	H
LVL2, LVL6	01b	1	1	0	1	Hi-Z	R _{OLP_PU}	V _{OLP_REF_H}	OUT2	L	H	H
LVL3, LVL4	11b	1	1	0	1	Hi-Z	R _{OLP_PD}	V _{OLP_REF_L}	OUT2	L	L	H

The OLP combinations and truth table for a no fault scenario vs. fault scenario for a high-side load in [Independent](#) mode is shown in [Table 7-18](#).

Table 7-18. Off-State Diagnostics Table for High-Side Load - Independent Mode

User Inputs						OLP Set-Up				OLP_CMP Output		
DIAG pin	S_DIAG bits	nSLEEP	DRVOFF	EN/IN1	PH/IN2	OUT1	OUT2	CMP REF	Output selected	Normal	Open	Short to GND
LVL2, LVL6	01b	1	1	1	don't care	R _{OLP_PU}	Hi-Z	V _{OLP_REF_H}	OUT1	H	H	L
LVL3, LVL4	11b	1	1	1	don't care	R _{OLP_PD}	Hi-Z	V _{OLP_REF_L}	OUT1	H	L	L
LVL2, LVL6	01b	1	1	0	1	Hi-Z	R _{OLP_PU}	V _{OLP_REF_H}	OUT2	H	H	L
LVL3, LVL4	11b	1	1	0	1	Hi-Z	R _{OLP_PD}	V _{OLP_REF_L}	OUT2	H	L	L

7.3.4.5 On-State Diagnostics (OLA) - SPI Variant Only

- Device state: ACTIVE - high-side recirculation
- Mechanism and threshold: On-state diagnostics (OLA) can detect an open load detection in the ACTIVE state during high-side recirculation. This includes high-side load connected directly to VM or through a high-side FET on the other half-bridge. During a PWM switching transition, the inductive load current re-circulates into VM through the HS body diode when the LS FET is turned OFF. The device looks for a voltage spike on OUTx above VM during the brief dead time, before the HS FET is turned ON. To observe the voltage spike, this load current needs to be higher than the pull down current (I_{PD_OLA}) on the output asserted by the FET driver. Device has configurable bit OLA_FLTR ([CONFIG4](#)) for either "16" or "1024" consecutive re-circulation switching cycles with absence of this voltage spike to indicate a loss of load inductance or increase in load resistance and is detected as an OLA fault.
- Action:
 - nFAULT pin is asserted low
 - Output - normal function maintained
 - IPROPI pin - normal function maintained
- Reaction configurable between latch setting and retry setting. In retry setting, OLA fault is automatically cleared with the detection of either "16" or "1024" consecutive voltage spikes during re-circulation switching cycles.
- OLA Fault Behavior during direction change:
 - Retry mode - If an open load condition is detected on OUTx, OLAX bit is set if condition persists for longer than the filter time. OLAX filter is cleared on direction change.

- Latch mode - If an open load condition is detected on OUTx, OLAX is set if condition persists for longer than the filter time. OLAX remains latched until a CLR_FLT command is issued. OLAX filter is cleared on direction change.
- OLA Fault Behavior during CLR_FLT command:
 - Retry mode - CLR_FLT command is not used.
 - Latch mode - If an open load condition is detected on OUT1, OLA1 is set if condition persists for longer than the filter time. OLAX remains latched until a CLR_FLT command is issued, which is cleared regardless of open load condition. If the condition does exist, OLA fault is reported again after the filter time.

This monitoring is optional and can be disabled.

Note

OLA is not supported for low-side loads (low-side recirculation).

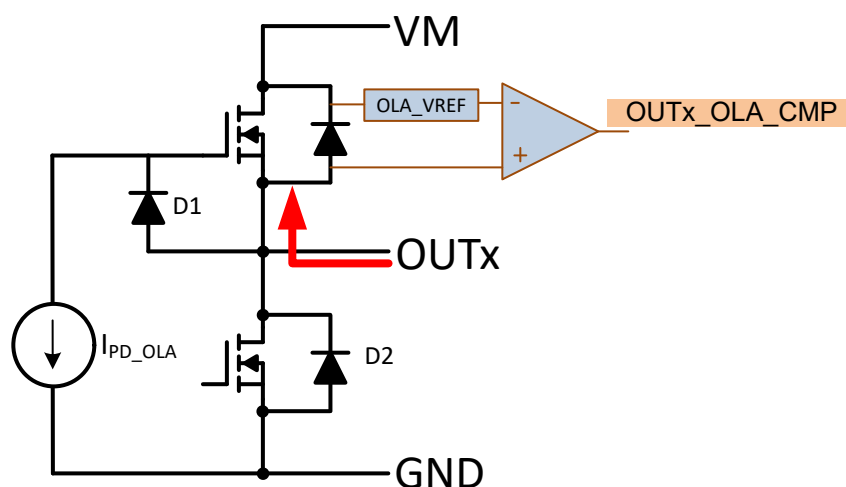


Figure 7-6. On-State Diagnostics

7.3.4.6 Manual Diagnostics - DRV8265-Q1 SPI Variant Only

The Manual Off-state diagnostics mode [M_OLP_EN](#) overrides the sequencing in off-state diagnostics allowing the user to fully configure the selected OUTx internal pullup, pulldown, Hi-Z resistors and monitor pin output on OLP_CMP status using [CONFIG5](#) and [CONFIG6](#) registers. The manual diagnostics comparator output (OLP_CMP) is available on OLP_CMP bit in [STATUS2](#) register. This combination is determined by the controller inputs or equivalent bits in the [SPI_IN](#) register for the SPI variant if the SPI_IN register has been unlocked.

The user can configure the Manual Diagnostics to determine the impedance on the OUTx node using off-state diagnostics in the STANDBY state when the power FETs are off or test for a FET fault in the ACTIVE state. With the Manual Diagnostics mode the user has full control of test circuit and it is possible to detect the following fault conditions as examples:

- Output short to VM or GND
- Open load for full-bridge load or low-side load
- Open load for high-side load
- FET stuck low
- FET output open
- The user can configure the following combinations for Manual Diagnostics in [CONFIG6](#)
 - Internal pull up resistor (R_{OLP_PU}) on OUTx with PUX bit
 - Internal pull down resistor (R_{OLP_PD}) on OUTx with PDx bit
 - Comparator reference level with CMP_REF_SEL

- Comparator input selection (OUTx)
- Internal Hi-Z resistor enable/disable for each output with RHIZx_DIS
- The user is expected to toggle through all the combinations and record the comparator output after its output is settled.
- Based on the input combinations and comparator output, the user can determine if there is a fault on the output or the FET.

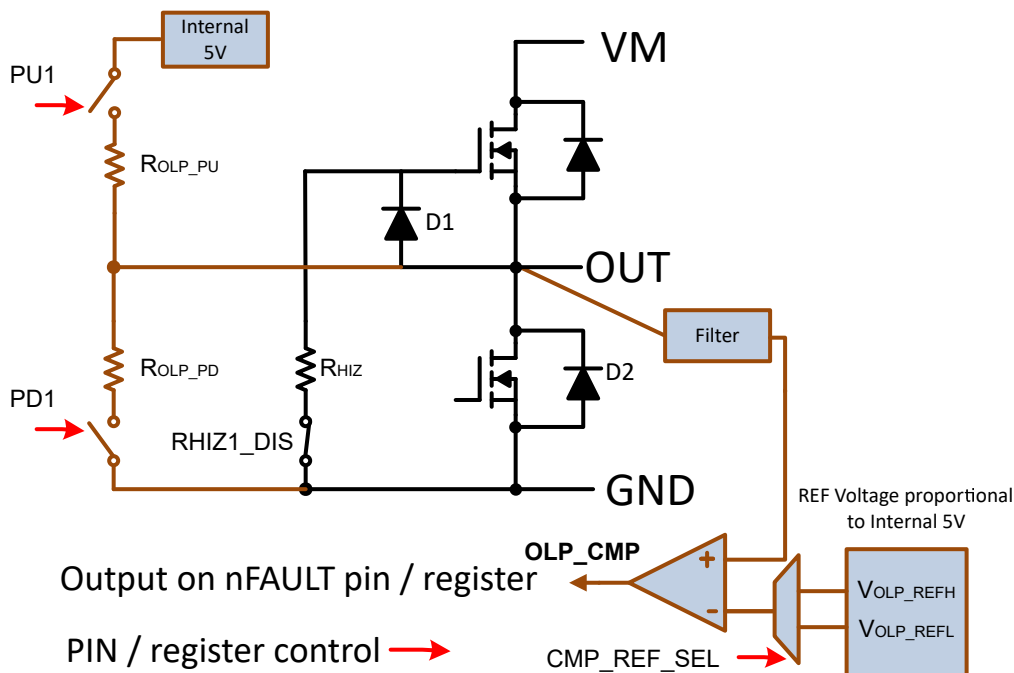


Figure 7-7. Manual Off-State (Passive) Diagnostics

The Manual Off-state diagnostics OLP combinations and truth table for a no fault scenario vs. fault scenario for a low-side load is shown in .

Note

Pullup (PUx) and Pulldown (PDx) should not be enabled at the same time.

Table 7-19. Manual Off-State Diagnostics Table for a Low-Side Load

User Inputs OLP Set-Up						OLP_CMP Output		
M_OLP_EN	OLP_CMP_SEL	S_DRVFFx	RHIZx_DIS	OUTx PU/PD	CMP_REF_SEL	Normal	Open	Short
1b	OUTx	1b	1b	PU1 = 1b (R _{OLP_PU})	1b (V _{OLP_REFH})	L	H	H
1b	OUTx	1b	1b	PD1 = 1b (R _{OLP_PD})	0b (V _{OLP_REFL})	L	L	H

The Manual Off-state diagnostics OLP combinations and truth table for a no fault scenario vs. fault scenario for a high-side load is shown in .

Table 7-20. Manual Off-State Diagnostics Table for a High-Side Load

User Inputs OLP Set-Up						OLP_CMP Output		
M_OLP_EN	OLP_CMP_SEL	S_DRVOFFx	RHIZx_DIS	OUTx PU/PD	CMP_REF_SEL	Normal	Open	Short
1b	OUTx	1b	1b	PU1 = 1b (R _{OLP_PU})	1b (V _{OLP_REFH})	H	H	L
1b	OUTx	1b	1b	PD1 = 1b (R _{OLP_PD})	0b (V _{OLP_REFL})	H	L	L

The Manual Off-state diagnostics OLP combinations and truth table for a no fault scenario vs. fault scenario for an H-bridge load is shown in .

Table 7-21. Manual Off-State Diagnostics Table for an H-bridge Load (assumes other side of H-bridge is Hi-Z)

User Inputs OLP Set-Up						OLP_CMP Output		
M_OLP_EN	OLP_CMP_SEL	S_DRVOFFx	RHIZx_DIS	OUTx PU/PD	CMP_REF_SEL	Normal	Short to VM	Short to GND
1b	OUTx	1b	1b	PU1 = 1b (R _{OLP_PU})	1b (V _{OLP_REFH})	H	H	L
1b	OUTx	1b	1b	PD1 = 1b (R _{OLP_PD})	0b (V _{OLP_REFL})	L	H	L

7.3.4.7 VM Over Voltage Monitor - SPI Variant Only

- Device state: STANDBY, ACTIVE
- Mechanism & thresholds: If the supply voltage on the VM pin exceeds the threshold, set by V_{VMOV} for a time greater than t_{VMOV}, then an VM over voltage fault is detected.
- Action:
 - nFAULT pin is asserted low
 - Output - normal function maintained
 - IPROPI pin - normal function maintained
- Reaction configurable between retry and latch setting

This monitoring is optional and can be disabled by making the OVSEL bit 1b. The V_{VMOV} can be configured for lower thresholds based on VMOV_SEL bits.

7.3.4.8 VM Under Voltage Monitor

- Device state: STANDBY, ACTIVE
- Mechanism & thresholds: If the supply voltage on the VM pin drops below the threshold, set by V_{VMUV} for a time greater than t_{VMUV}, then an VM under voltage fault is detected.
- Action:
 - nFAULT pin is asserted low
 - Both OUTx is Hi-Z
 - IPROPI pin is Hi-Z
- HW variant: Reaction configurable between retry and latch as per DIAG setting
- SPI variant: Reaction configurable between retry and latch setting
- Note that retry time is only dependent on recovery of VM under voltage condition and is independent of t_{RETRY} / t_{CLEAR} times

7.3.4.9 Power On Reset (POR)

- Device state: ALL

- Mechanism & thresholds: If VDD drops below V_{POR_FALL} for a time greater than t_{POR} , then a power on reset will occur that will hard reset the device.
- Action:
 - nFAULT pin is de-asserted
 - Both OUTx is Hi-Z
 - IPROPI pin is Hi-Z.
 - When VDD recovers above the V_{POR_RISE} level, the device will go through a wake-up initialization and nFAULT pin will be asserted low to notify the user on this reset (Refer [Wake-up transients](#)).
- Fault reaction: Always retry, retry time depends on the external supply condition to initiate a device wake-up
- POR fault is cleared only if VM voltage is above the under voltage threshold level

7.3.4.10 Powered off Braking (POB)

When the motor is driven by external force, it acts as a generator and pumps back current to the supply voltage rail. This can potentially damage other circuits connected to the supply rail. The powered off braking (POB) feature is implemented to prevent the increase in the supply voltage. POB should only be used with H-bridge loads.

In low-power sleep mode or when the bridge is disabled (Hi-Z), if the supply voltage is more than V_{VMOV_POB} and if the voltage of the output nodes rise above the supply voltage by more than V_{POB_TH} , the device turns on the two low-side MOSFETs. This allows the device to actively brake a motor connected to the outputs by shorting the back emf across the motor terminals.

For the SPI variant -

- Powered off braking (POB) is enabled by default.
- After power-up, the EN_POB bit in [CONFIG3](#) register can be made 0b to disable this feature.
- The EN_POB logic state is latched, so that in sleep mode the device behaves as per the EN_POB bit setting, even though the internal digital logic is reset.
 - The VDD supply must be present to latch the EN_POB state.
 - If VDD is cycled, the EN_POB state is reset, and POB is enabled again during the next power-up. If POB was disabled before VDD was cycled, user has to disable POB again after VDD goes above UVLO level.
 - VM cycling will not have any effect on the EN_POB state.

For the HW variant in full-bridge mode, POB can be enabled or disabled by the DIAG pin setting.

In sleep mode, in case of a short circuit to power supply fault present on the power stage, a simple overcurrent detector circuit with analog RC deglitch filter is provided to disable the low-side MOSFET if a high current event is detected while braking. This is needed since the normal overcurrent protection circuits are disabled during the device low-power sleep mode. The overcurrent comparator and RC deglitch filter values are fixed and cannot be adjusted. If this limit is reached seven times, POB_EN is automatically set low & the POB function is disabled. POB disable is latched until a full power cycle ($VDD = 0V$ & $VM = 0V$) occurs.

7.3.4.11 Event Priority

In the ACTIVE state, in a scenario where two or more events occur simultaneously, the device assigns control of the driver based on the following priority table.

Table 7-22. Event Priority Table

Event	Priority
User SLEEP command	1
User input: DRVOFF	2
Over temperature detection (TSD)	3
Over current detection (OCP) ⁽¹⁾	4
VM under voltage detection (VMUV)	5
User input: EN/IN1 and/or PH/IN2	6
Internal PWM control from ITRIP regulation	7

Table 7-22. Event Priority Table (continued)

Event	Priority
VM over voltage detection (VMOV)	8
On-state fault detection (OLA - SPI variant only) ⁽²⁾	9

- (1) If the device is waiting for an OCP event to be confirmed (waiting for t_{OCP}) when any of events with lower priority than OCP occur, then the device can delay servicing the other events up to a maximum time of t_{OCP} to enable detection of the OCP event.
- (2) Priority is "do not care" in this case as this fault event does not cause a change in OUTx

7.3.5 Device Functional Modes

The device has three functional states:

- SLEEP
- STANDBY
- ACTIVE

These states are described in the following section.

7.3.5.1 SLEEP State

This state occurs when nSLEEP pin is asserted low for a time $> t_{SLEEP}$ or voltage on the VDD pin is $< VDD_{POR_FALL}$.

This is the deep sleep low power (I_{SLEEP}) state of the device where all functions except a wake-up command are not serviced. The drivers are in Hi-Z. The internal power supply rails (5 V and others) are powered off. nFAULT pin is de-asserted in this state. The device can enter this state from either the STANDBY or the ACTIVE state.

7.3.5.2 STANDBY State

The device is in this state when nSLEEP pin is asserted high, the voltage on the VDD pin is $> VDD_{POR_RISE}$ and DRVOFF = logic-high for all modes and additionally, in PWM mode when both IN1/EN & IN2/PH are logic-high with DRVOFF = logic-low. In this state, the device is powered up ($I_{STANDBY}$), with the driver Hi-Z and nFAULT de-asserted. The device is ready to transition to ACTIVE state or SLEEP state when commanded so. Off-state diagnostics (OLP), if enabled, are done in this state.

7.3.5.3 Wake-up to STANDBY State

The device starts transition from SLEEP state to STANDBY state:

- If the nSLEEP pin goes high for a duration longer than t_{WAKE} , or
- If VDD supply $> VDD_{POR_RISE}$ such that internal POR is released to indicate a power-up.

The device goes through an initialization sequence to load the internal registers and wake-up all the blocks in the following sequence:

- At a certain time, t_{COM} from wake-up, the device is capable of communication. This is indicated by asserting the nFAULT pin low.
- This is followed by the time t_{READY} , when the device wake-up is complete.
- At this point, the HW variant device enters STANDBY mode for all DIAG options in PH/EN or PWM mode except RLVL5. For DIAG = RLVL5, an nSLEEP wake-up pulse is required for entry into STANDBY mode. For independent mode behavior, refer to [independent mode DIAG table](#). For SPI variant, once the device receives a **CLR FAULT** command through SPI as an acknowledgment of the wake-up from the controller, the device enters the STANDBY state. This is indicated by the de-assertion of the nFAULT pin. The driver is held in Hi-Z till this point.
- From here on, the device is ready to drive the bridge based on the truth tables for the specific mode configured.

Refer to the [wake-up transients waveforms](#) for the illustration.

7.3.5.4 ACTIVE State

The device is fully functional in this state with the drivers controlled by other inputs as described in prior sections. All protection features are fully functional with fault signaling on nFAULT pin. SPI communication is available. The device can transition into this state only from the STANDBY state.

7.3.5.5 nSLEEP Reset Pulse (HW Variant, LATCHED setting Only)

This is a special communication signal from the controller to the device through the nSLEEP pin available only for the HW variant. This is used to -

- Clear a latched fault when the fault reaction is configured to the LATCHED setting, without forcing the device into SLEEP or affecting any of the other functions (Equivalent to the CLR_FAULT command in the SPI variant)

This pulse on nSLEEP must be greater than the nSLEEP deglitch time of t_{RESET} time, but shorter than t_{SLEEP} time, as shown in case # 3, in Table 7-23 below.

Table 7-23. nSLEEP Timing (HW Variant Only)

Case #	Window Start Time	Window End Time	Command Interpretation	
			Clear Fault	Sleep
1	0	$t_{\text{RESET min}}$	No	No
2	$t_{\text{RESET min}}$	$t_{\text{RESET max}}$	Indeterminate	No
3	$t_{\text{RESET max}}$	$t_{\text{SLEEP min}}$	Yes	No
4	$t_{\text{SLEEP min}}$	$t_{\text{SLEEP max}}$	Yes	Indeterminate
5	$t_{\text{SLEEP max}}$	No limit	Yes	Yes

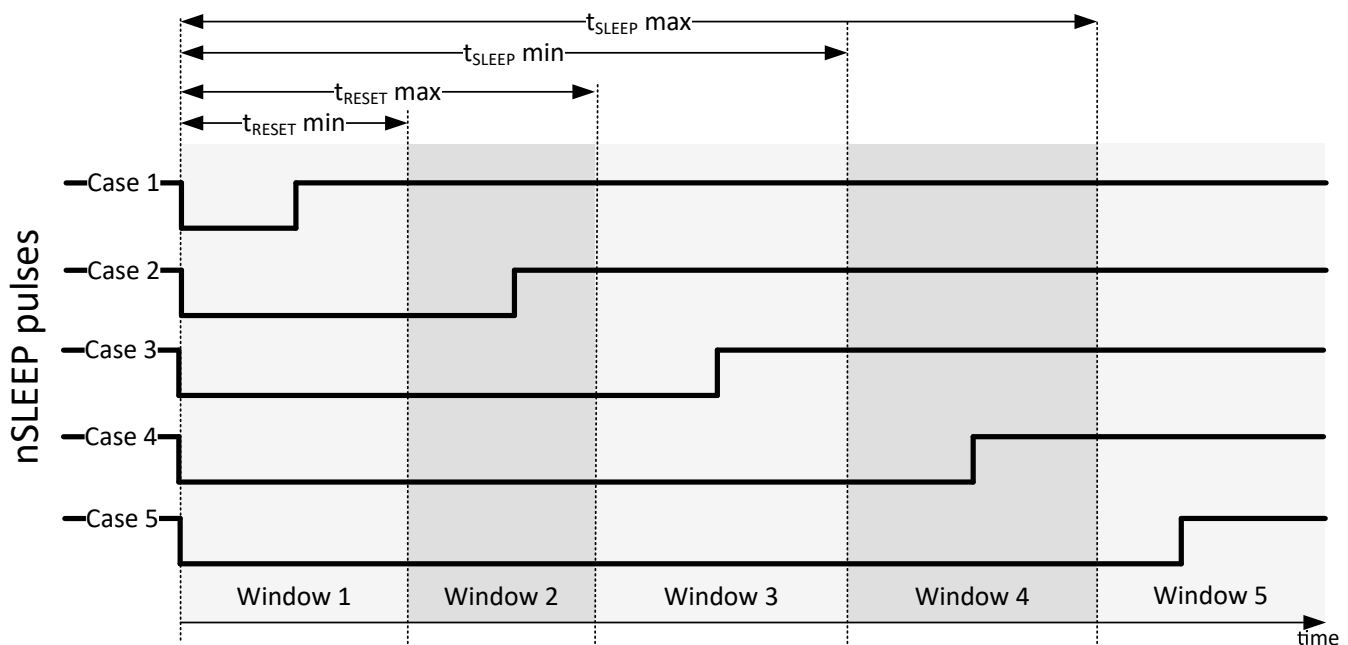


Figure 7-8. nSLEEP Pulse Scenarios

7.3.6 Programming - SPI Variant Only

7.3.6.1 Serial Peripheral Interface (SPI)

The SPI variant has full-duplex, 4-wire synchronous communication that is used to set device configurations, operating parameters, and read out diagnostic information from the device. The SPI operates in peripheral mode

and connects to a controller. The serial data input (SDI) word consists of a 16-bit word, with an 8-bit command (A1), followed by 8-bit data (D1). The serial data output (SDO) word consists of the FAULT byte (S1), followed by a report byte (R1). The report byte is either the register data being accessed by read command or null for a write command. The data sequence between the MCU and the SPI peripheral driver is shown in Figure 7-9.

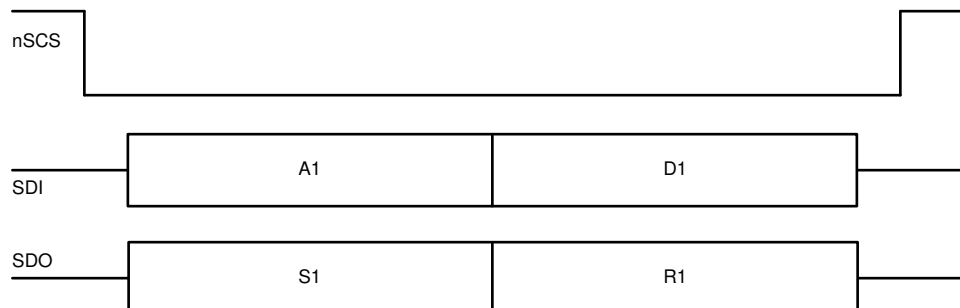


Figure 7-9. SPI Data - Standard "16-bit" Frame

A valid frame must meet the following conditions:

- SCLK pin is low when the nSCS pin transitions from high to low and from low to high.
- nSCS pin is pulled high between words.
- When nSCS pin is pulled high, any signals at the SCLK and SDI pins are ignored and the SDO pin is placed in the Hi-Z state.
- Data on SDO from the device is propagated on the rising edge of SCLK, while data on SDI is captured by the device on the subsequent falling edge of SCLK.
- The most significant bit (MSB) is shifted in and out first.
- A full 16 SCLK cycles must occur for a valid transaction for a standard frame, or alternately, for a daisy chain frame with "n" number of peripheral devices, $16 + (n \times 16)$ SCLK cycles must occur for a valid transaction. Else, a frame error (ERR) is reported and the data is ignored if valid frame is a WRITE operation.

7.3.6.2 Standard Frame

The SDI input data word is 2 bytes long and consists of the following format:

- Command byte (first byte)
 - MSB bit indicates frame type (bit B15 = 0 for standard frame).
 - Next to MSB bit, W0, indicates read or write operation (bit B14, write = 0, read = 1)
 - Followed by 6 address bits, A[5:0] (bits B13 through B8)
- Data byte (second byte)
 - Second byte indicates data, D[7:0] (bits B7 through B0). For a read operation, these bits are typically set to null values, while for a write operation, these bits have the data value for the addressed register.

Table 7-24. SDI - Standard Frame Format

	Command Byte								Data Byte							
Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data	0	W0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

The SDO output data word is 2 bytes long and consists of the following format:

- Status byte (first byte)
 - 2 MSB bits are forced high (B15, B14 = 1)
 - Following 6 bits are from the FAULT register (B13:B8)
- Report byte (second byte)
 - The second byte (B7:B0) is either the data currently in the register being read for a read operation (W0 = 1), or, existing data in the register being written to for a write command (W0 = 0)

Table 7-25. SDO - Standard Frame Format

Bit	Status Byte								Report Byte							
	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data	1	1	FAULT	VMOV	VMUV	OCF	TSD	ERR	D7	D6	D5	D4	D3	D2	D1	D0

7.3.6.3 SPI Interface for Multiple Peripherals

Multiple devices can be connected to the controller with and without the daisy chain. For connecting a 'n' number of devices to a controller without using a daisy chain, 'n' number of I/O resources from controller has to be utilized for nSCS pins as shown in [Figure 7-10](#). Whereas, if the daisy chain configuration is used, then a single nSCS line can be used for connecting multiple devices, as shown in [Figure 7-11](#).

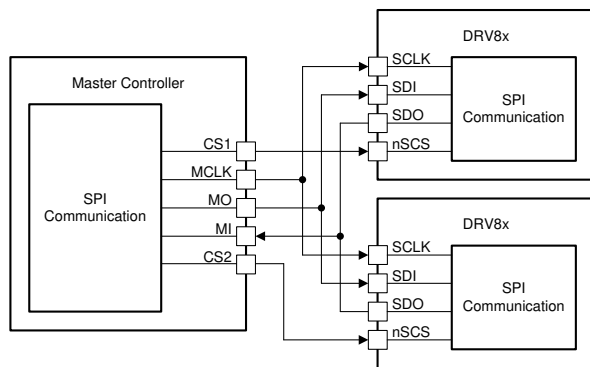


Figure 7-10. SPI Operation Without Daisy Chain

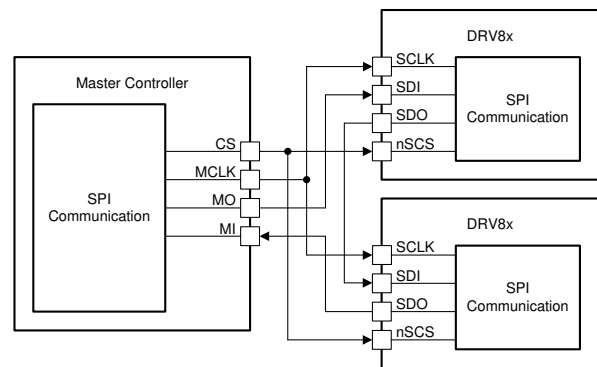


Figure 7-11. SPI Operation With Daisy Chain

7.3.6.3.1 Daisy Chain Frame for Multiple Peripherals

The device can be connected in a daisy chain configuration to save GPIO ports when multiple devices are communicating to the same MCU. [Figure 7-12](#) shows the topology with waveforms, where, number of peripherals connected in a daisy chain "n" is set to 3. A maximum of up to 63 devices can be connected in this manner.

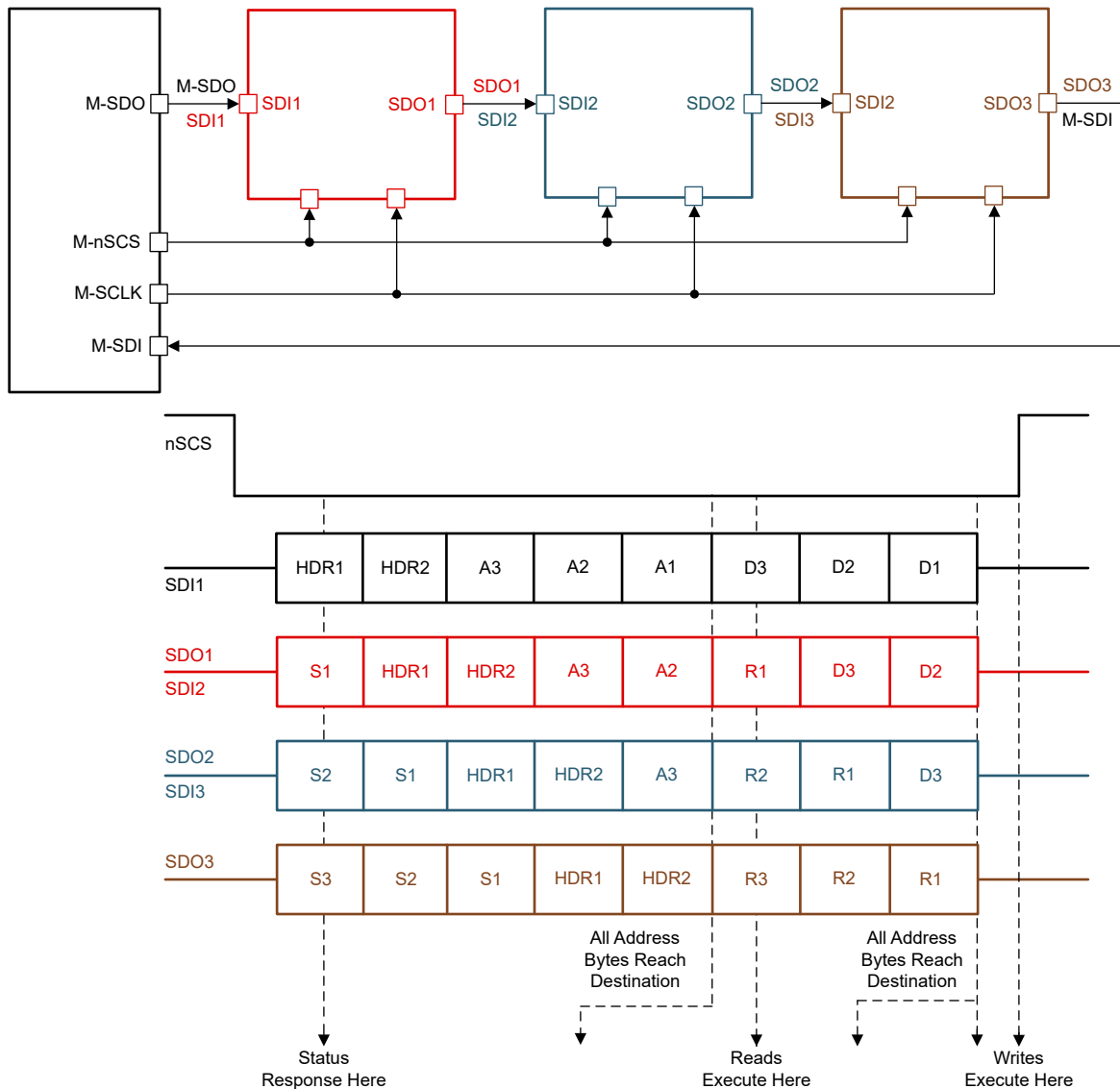


Figure 7-12. Daisy Chain SPI Operation

The SDI sent by the controller in this case is in the following format (see SDI1 in [Figure 7-12](#)):

- 2 bytes of header (HDR1, HDR2)
- "n" bytes of command byte starting with furthest peripheral in the chain (for this example, this is A3, A2, A1)
- "n" bytes of data byte starting with furthest peripheral in the chain (for this example, this is D3, D2, D1)
- Total of $2 \times "n" + 2$ bytes

While the data is being transmitted through the chain, the controller receives the data in the following format (see SDO3 in [Figure 7-12](#)):

- 3 bytes of status byte starting with furthest peripheral in the chain (for this example, this is S3, S2, S1)
- 2 bytes of header that are transmitted before (HDR1, HDR2)
- 3 bytes of report byte starting with furthest peripheral in the chain (for this example, this is R3, R2, R1)

The Header bytes are special bytes asserted at the beginning of a daisy chain SPI communication. **Header bytes must start with 1 and 0 for the two leading bits.**

The first header byte (HDR1) contains information of the total number of peripheral devices in the daisy chain. N5 through N0 are 6 bits dedicated to show the number of device in the chain as shown in [Figure 7-13](#). Up to

63 devices can be connected in series per daisy chain connection. Number of peripheral = 0 is not permitted and results in a ERR flag.

The second header byte (HDR2) contains a global **CLR FAULT** command that clears the fault registers of all the devices on the rising edge of the chip select (nSCS) signal. The 5 trailing bits of the HDR2 register are marked as SPARE (don't care bits). These can be used by the MCU to determine integrity of the daisy chain connection.

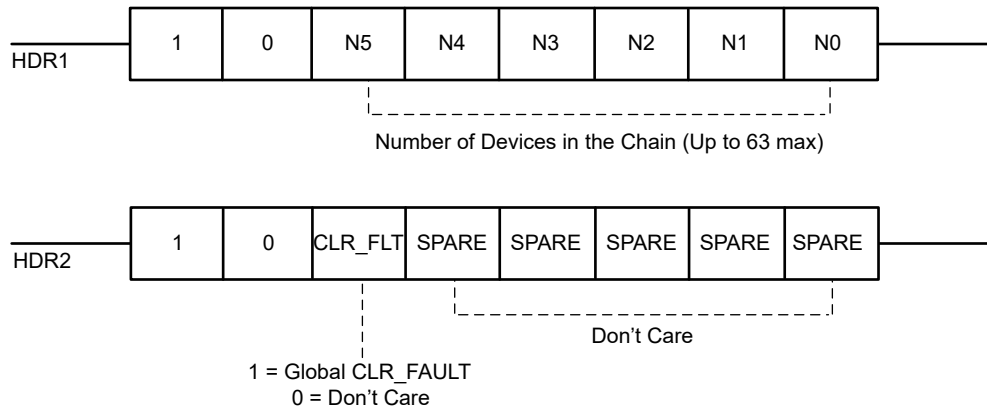


Figure 7-13. Header bytes

In addition, the device recognizes bytes that start with 1 and 1 for the two leading bits as a "pass" byte. These "pass" bytes are NOT processed by the device, but the "pass" bytes are simply transmitted out on SDO in the following byte.

When data passes through a device, the data determines the position of the data in the chain by counting the number of Status bytes the device receives following by the first Header byte. For example, in this 3 device configuration, device 2 in the chain receives one status byte before receiving the two header bytes.

From the one status byte the data knows that the position is second in the chain, and from HDR1 byte the data knows how many devices are connected in the chain. That way the header byte only loads the relevant address and data byte in the header bytes buffer and bypasses the other bits. This protocol allows for faster communication without adding latency to the system for up to 63 devices in the chain.

The command, data, status and report bytes remain the same as described in the standard frame format.

7.3.7 Register Map - SPI Variant Only

This section describes the user configurable registers in the device.

Note

While the device allows register writes at any time SPI communication is available, it is recommended to exercise caution while updating registers in the ACTIVE state while the load is being driven. This is especially important for settings such as S_MODE and S_DIAG which control the critical device configuration. In order to prevent accidental register writes, the device offers a locking mechanism through the REG_LOCK bits in the **COMMAND** register to lock the contents of all configurable registers. Best practice would be to write all the configurable registers during initialization and then lock these settings. Run-time register writes for output control are handled by the **SPI_IN** register, which offers its own separate locking mechanism through the SPI_IN_LOCK bits.

7.3.7.1 User Registers

The following table lists all the registers that can be accessed by the user. All register addresses NOT listed in this table should be considered as "reserved" locations and access is blocked to this space.

Table 7-26. User Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type ⁽¹⁾
DEVICE_ID	DEV_ID[5:0]						REV_ID[1:0]		R
FAULT	ERR ⁽²⁾	POR	FAULT	VMOV	VMUV	OCP	TSD	OLA ⁽²⁾	R
STATUS1	OLA1	OLA2	ITRIP_CMP	ACTIVE	OCP_H1	OCP_L1	OCP_H2	OCP_L2	R
STATUS2	DRV_STAT	RSVD	OTW	ACTIVE	RSVD			OLP_CMP	R
COMMAND	CLR_FLT	RSVD		SPI_IN_LOCK[1:0]		RSVD	REG_LOCK[1:0]		R/W
SPI_IN	RSVD				S_DRVOFF	S_DRVOFF2	S_ENIN1	S_PHIN2	R/W
CONFIG1	EN_OLA	OTW_SEL	OVSEL	SSC_DIS	OCP_RTRY	TSD_RTRY	OV_RTRY	OLA_RTRY	R/W
CONFIG2	EXTEND	S_DIAG[1:0]		ISEL[1:0]		S_ITRIP[2:0]			R/W
CONFIG3	TOFF[1:0]		EN_POB	TBLK	SR[1:0]		S_MODE [1:0]		R/W
CONFIG4	OTW_REP	TOCP	OLA_FLTR	OCP_SEL[1:0]		DRV_SEL	ENIN1_SEL	PHIN2_SEL	R/W

Table 7-27. Additional User Registers DRV8263A-Q1

CONFIG5	EXT_ISEL[1:0]		SR_MODE	OLP_CMP_SEL[1:0]		P_EN	EXT_SR[1:0]		R/W
CONFIG6	PU1_EN	PD1_EN	RHIZ1_DIS	PU2_EN	PD2_EN	RHIZ2_DIS	M_OLP_EN	CMP_REF_SEL	R/W
CONFIG7	RSVD						VMOV_SEL		R/W

(1) R = Read Only, R/W = Read/Write

(2) OLA replaced by ERR in the first SDO byte response, common to all SPI frames. Refer [SDO - Standard frame format](#).

7.3.7.1.1 DEVICE_ID register (Address = 00h)

Return to the [User Register table](#).

Device	DEVICE_ID value
DRV8263S-Q1	0 x 25

7.3.7.1.2 FAULT Register (Address = 01h) [reset = 40h]

Return to the [User Register table](#).

Bit	Field	Type	Reset	Description
7	ERR	R	0b	1b indicates that a SPI communication fault has occurred in the previous SPI frame.
6	POR	R	1b	1b indicates that a power-on-reset has been detected.
5	FAULT	R	0b	Logic OR of ERR, POR, VMUV, OCP & TSD
4	VMOV	R	0b	1b indicates that a VM over voltage has been detected.
3	VMUV	R	0b	1b indicates that a VM under voltage has been detected.
2	OCP	R	0b	1b indicates that an over current has been detected in either one or more power FETs. Refer OCP_SEL, TOCP to change thresholds & filter times. Refer OCP_RETRY to configure fault reaction.
1	TSD	R	0b	1b indicates that an over temperature has been detected. Refer TSD_RETRY to configure fault reaction.
0	OLA	R	0b	1b indicates that an open load condition has been detected in the ACTIVE state. Refer to EN_OLA to disable diagnostic, OLA_RETRY to configure fault reaction.

7.3.7.1.3 STATUS1 Register (Address = 02h) [reset = 00h]

Return to the [User Register table](#).

Bit	Field	Type	Reset	Description
7	OLA1	R	0b	1b indicates that an open load condition has been detected in the ACTIVE state on OUT1
6	OLA2	R	0b	1b indicates that an open load condition has been detected in the ACTIVE state on OUT2
5	ITRIP_CMP	R	0b	1b indicates that load current has reached the ITRIP regulation level.
4	ACTIVE	R	0b	1b indicates that the device is in the ACTIVE state
3	OCP_H1	R	0b	1b indicates that an over current has been detected on the high-side FET (short to GND) on OUT1
2	OCP_L1	R	0b	1b indicates that an over current has been detected on the low-side FET (short to VM) on OUT1
1	OCP_H2	R	0b	1b indicates that an over current has been detected on the high-side FET (short to GND) on OUT2
0	OCP_L2	R	0b	1b indicates that an over current has been detected on the low-side FET (short to VM) on OUT2

7.3.7.1.4 STATUS2 Register (Address = 03h) [reset = 0h]

Return to the [User Register table](#).

Bit	Field	Type	Reset	Description
7	DRV_STAT	R	-	This bit shows the status of the DRVOFF pin. 1b implies the pin status is high.

Bit	Field	Type	Reset	Description
6	RSVD	R	0b	Reserved
5	OTW	R	0b	1b indicates that a over temperature warning event has been detected.
4	ACTIVE	R	0b	1b indicates that the device is in the ACTIVE state (Copy of bit4 in STATUS1)
3-1	RSVD	R	000b	Reserved
0	OLP_CMP	R	0b	This bit is the output of the off-state diagnostics (OLP) comparator.

7.3.7.1.5 COMMAND Register (Address = 08h) [reset = 09h]

Return to the [User Register table](#).

Bit	Field	Type	Reset	Description
7	CLR_FLT	R/W	0b	Clear Fault command - Write 1b to clear all faults reported in the fault registers and de-assert the nFAULT pin
6-5	RSVD	R	00b	Reserved
4-3	SPI_IN_LOCK	R/W	01b	<ul style="list-style-type: none"> Write 10b to unlock the SPI_IN register Write 01b or 00b or 11b to lock the SPI_IN register SPI_IN register is locked by default.
2	RSVD	R	0b	Reserved
1-0	REG_LOCK	R/W	01b	<ul style="list-style-type: none"> Write 10b to lock the CONFIG registers Write 01b or 00b or 11b to unlock the CONFIG registers CONFIG registers are unlocked by default.

7.3.7.1.6 SPI_IN Register (Address = 09h) [reset = 0Ch]

Return to the [User Register table](#).

Bit	Field	Type	Reset	Description
7-4	RSVD	R	0000b	Reserved
3	S_DRVOFF	R/W	1b	Register bit equivalent of DRVOFF pin when SPI_IN is unlocked. Refer Register Pin control section. In Independent mode, this bit shuts off half-bridge 1.
2	S_DRVOFF2	R/W	1b	Register bit to shut off half-bridge 2 in Independent mode when SPI_IN is unlocked. Refer Register Pin control section
1	S_ENIN1	R/W	0b	Register bit equivalent of EN/IN1 pin when SPI_IN is unlocked. Refer Register Pin control section
0	S_PHIN2	R/W	0b	Register bit equivalent of PH/IN2 pin when SPI_IN is unlocked. Refer Register Pin control section

7.3.7.1.7 CONFIG1 Register (Address = 0Ah) [reset = 10h]

Return to the [User Register table](#).

Bit	Field	Type	Reset	Description
7	EN_OLA	R/W	0b	Write 1b to enable open load detection in the active state. In Independent mode, OLA is always disabled for low-side load. Refer DIAG section.

Bit	Field	Type	Reset	Description
6	OTW_SEL	R/W	0b	Over Temperature Warning threshold 0b = 140 °C 1b = 120 °C
5	OVSEL	R/W	0b	0b: VMOV enabled 1b: VMOV disabled
4	SSC_DIS	R/W	1b	0b: Enables the spread spectrum clocking feature
3	OCP_RTRY	R/W	0b	Write 1b to configure fault reaction to retry setting on the detection of over current, else the fault reaction is latched
2	TSD_RTRY	R/W	0b	Write 1b to configure fault reaction to retry setting on the detection of over temperature, else the fault reaction is latched
1	OV_RTRY	R/W	0b	Write 1b to configure fault reaction to retry setting on the detection of VMOV, else the fault reaction is latched. This bit also controls the fault reaction for a VM under voltage detection.
0	OLA_RTRY	R/W	0b	Write 1b to configure fault reaction to retry setting on the detection of open load during active, else the fault reaction is latched.

7.3.7.1.8 CONFIG2 Register (Address = 0Bh) [reset = 18h]

Return to the [User Register table](#).

Bit	Field	Type	Reset	Description
7	EXTEND	R/W	0b	Write 1b to access additional Hi-Z (coast) states in the PWM mode - refer PWM EXTEND table
6-5	S_DIAG	R/W	00b	Load type indication - refer to DIAG table
4-3	ISEL	R/W	11b	Selects between proportional current output and Die temperature readout voltage.
2-0	S_ITRIP	R/W	000b	ITRIP level configuration - refer ITRIP table

7.3.7.1.9 CONFIG3 Register (Address = 0Ch) [reset = 40h]

Return to the [User Register table](#).

Bit	Field	Type	Reset	Description
7-6	TOFF	R/W	01b	TOFF time used for ITRIP current regulation 00b = 20 µsec 01b = 30 µsec 10b = 40 µsec 11b = 50 µsec
5	EN_POB	R/W	0b	Write 1b to enable powered off braking in sleep mode or when the bridge is disabled (Hi-Z). Else powered off braking is disabled.
4	TBLK	R/W	0b	Blanking time configuration 0b = 2.4 µsec 1b = 3.4 µsec

Bit	Field	Type	Reset	Description
3-2	SR	R/W	00b	Slew Rate configuration 00b = 155 V/ μ s 01b = 83 V/ μ s 10b = 39 V/ μ s 11b = 16 V/ μ s
1-0	S_MODE	R/W	00b	Device mode configuration - refer MODE table

7.3.7.1.10 CONFIG4 Register (Address = 0Dh) [reset = 44h]

Return to the [User Register table](#).

Bit	Field	Type	Reset	Description
7	OTW_REP	R/W	0b	0b = Over temperature warning is not reported on nFAULT 1b = Over temperature warning is reported on nFAULT
6	TOCP	R/W	1b	Filter time for over current detection configuration 0b = 1 μ sec 1b = 2 μ sec
5	OLA_FLTR	R/W	0b	Selects OLA filter count. 0b = 16 count, 1b = 1024 count.
4-3	OCP_SEL	R/W	00b	Threshold for over current detection configuration
2	DRV_SEL	R/W	1b	DRVOFF pin - register logic combination , when SPI_IN is unlocked 0b = OR 1b = AND
1	ENIN1_SEL	R/W	0b	EN/IN1 pin - register logic combination , when SPI_IN is unlocked 0b = OR 1b = AND
0	PHIN2_SEL	R/W	0b	PH/IN2 pin - register logic combination , when SPI_IN is unlocked 0b = OR 1b = AND

7.3.7.1.11 CONFIG5 Register (Address = 0Eh) [reset = 00h]

DRV8263A-Q1 additional configuration options. Return to the [User Register table](#).

Bit	Field	Type	Reset	Description
7-6	EXT_ISEL	R/W	00b	Extended ISEL options for H-bridge configurations to monitor current individual High-side of a Half-bridge output. 00b = ISEL[1:0] settings apply 01b = IHS1 x AIPROPI 10b = IHS2 x AIPROPI 11b = Reserved

Bit	Field	Type	Reset	Description
5	SR_MODE	R/W	0b	Extended Slew Rate Mode Selection for High-side Low-side configuration. 0b = SR[1:0] and EXT_SR[1:0] slew rates apply to both High-side and Low-side FET 1b = EXT_SR[1:0] slew rates only apply to Low-side FET
4-3	OLP_CMP_SEL	R/W	00b	Manual Off-state diagnostics: output select, overrides pin controlled OLP selection and outputs result on OLP_CMP status bit. 00b = OUT1 01b = OUT2 10b = Reserved 11b = Reserved
2	P_EN	R/W	0b	Parallel Mode Enable. OUT1 and OUT2 outputs are connected and input to device matches independent Half-bridge mode for synchronization. 0b = Disabled 1b = Enabled
1-0	EXT_SR	R/W	00b	Extended Slew Rate configuration, overrides SR[1:0] slew rate options 00b = SR[1:0] settings applied 01b = 270 V/μs 10b = 330 V/μs 11b = 400 V/μs

7.3.7.1.12 CONFIG6 Register (Address = 10h) [reset = 00h]

DRV8263A-Q1 additional configuration options. Return to the [User Register table](#).

Bit	Field	Type	Reset	Description
7	PU1_EN	R/W	0b	Manual Off-state diagnostics: High-side ROLP_PU enable, overrides pin controlled OLP based on OLP_CMP_SEL = 00b configuration. Retains value until S_DRVOFFx for selected output is set to 0. 0b = Disable 1b = Enable
6	PD1_EN	R/W	0b	Manual Off-state diagnostics: Low-side ROLP_PD enable, overrides pin controlled OLP based on OLP_CMP_SEL = 00b configuration. Retains value until S_DRVOFFx for selected output is set to 0. 0b = Disable 1b = Enable
5	RHIZ1_DIS	R/W	0b	Manual Off-state diagnostics: RHIZ1 disable, overrides pin controlled OLP based on OLP_CMP_SEL = 00b configuration. 0b = Enable 1b = Disable

Bit	Field	Type	Reset	Description
4	PU2_EN	R/W	0b	Manual Off-sate diagnostics: High-side ROLP_PU enable, overrides pin controlled OLP based on OLP_CMP_SEL = 01b configuration. Retains value until S_DRVOFFx for selected output is set to 0. 0b = Disable 1b = Enable
3	PD2_EN	R/W	00b	Manual Off-sate diagnostics: Low-side ROLP_PD enable, overrides pin controlled OLP based on OLP_CMP_SEL = 01b configuration. Retains value until S_DRVOFFx for selected output is set to 0. 0b = Disable 1b = Enable
2	RHIZ2_DIS	R/W	0b	Manual Off-sate diagnostics: RHIZ2 disable, overrides pin controlled OLP based on OLP_CMP_SEL = 01b configuration. 0b = Enable 1b = Disable
1	M_OLP_EN	R/W	0b	Manual Off-sate diagnostics enable: overrides pin controlled OLP selection and is enabled for selected output on OLP_CMP_SEL. 0b = Disable 1b = Enable
0	CMP_REF_SEL	R/W	0b	Manual Off-sate diagnostics: comparator reference select, overrides pin controlled OLP_CMP_SEL selection and outputs result on OLP_CMP status bit. 0b = VOLP_REFL 1b = VOLP_REFH

7.3.7.1.13 CONFIG7 Register (Address = 11h) [reset = 00h]

DRV8263A-Q1 additional configuration options. Return to the [User Register table](#).

Bit	Field	Type	Reset	Description
7-2	RSVD	R	000000b	Reserved
1-0	VMOV_SEL	R/W	00b	Manual Off-sate diagnostics: comparator reference select, overrides pin controlled OLP_CMP_SEL selection and outputs result on OLP_CMP status bit. 00b = V _{MOV} set to 60V for 48V applications 01b = V _{MOV} set to 22V for 12V applications 10b = V _{MOV} set to 28V for 12V applications 11b = Reserved

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The DRV8263-Q1 can be used in a variety of applications that require either a half-bridge or H-bridge power stage configuration. Common application examples include brushed DC motors, solenoids, and actuators. The device can also be utilized to drive many common passive loads such as LEDs, resistive elements, relays, etc.

8.1.1 Load Summary

The following table summarizes the utility of the device features for different type of inductive loads.

Table 8-1. Load Summary Table

LOAD TYPE	Configuration		Device Feature	
	Device	Recirculation Path	Current sense	ITRIP regulation
Bi-directional motor or solenoid ⁽¹⁾	DRV8263 in PH/EN or PWM mode	High-side	Continuous	Useful
2 Uni-directional motors or low-side solenoids (one side connected to GND)	DRV8263 in Independent mode ⁽²⁾	Low-side	Discontinuous ⁽³⁾	Individual load regulation not possible
2 High-side solenoids (one side connected to VM)	DRV8263 in Independent mode ⁽²⁾	High-side	Not available, need external solution	

- (1) Solenoid - clamping or quick demagnetization possible, but clamping level is VM dependent
 (2) Independent Hi-Z only supported in the SPI variant
 (3) Not sensed during recirculation and during OUTx voltage slew times including t_{blank}

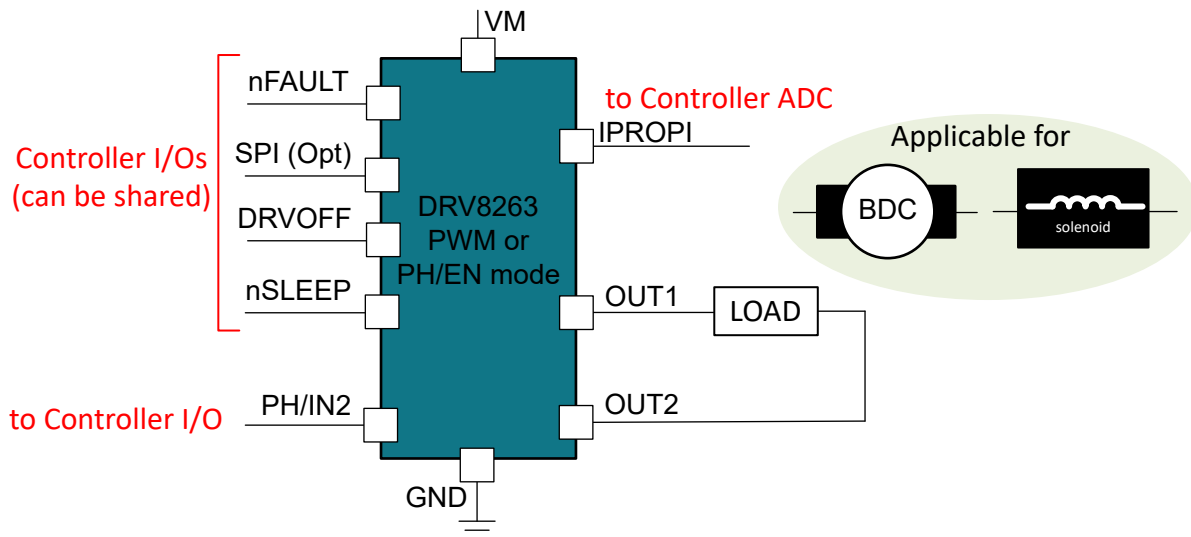


Figure 8-1. Illustration Showing a Full-Bridge Topology With DRV8263-Q1 in PWM or PH/EN Mode

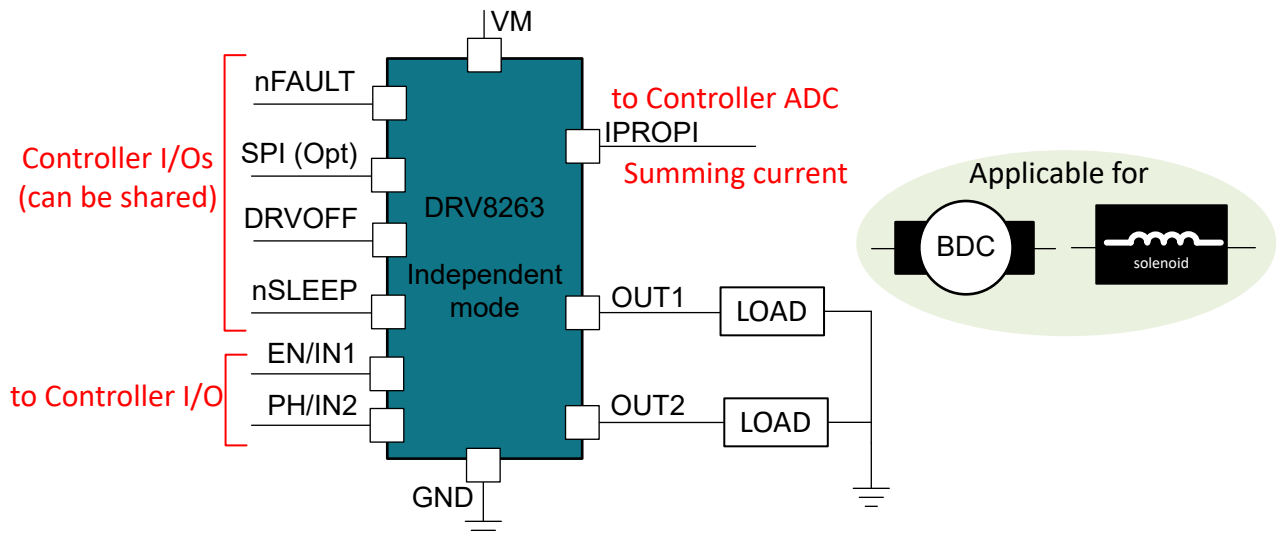


Figure 8-2. Illustration Showing Half-Bridge Topology to Drive Two Low-side Loads Independently With DRV8263-Q1 Device in INDEPENDENT Mode

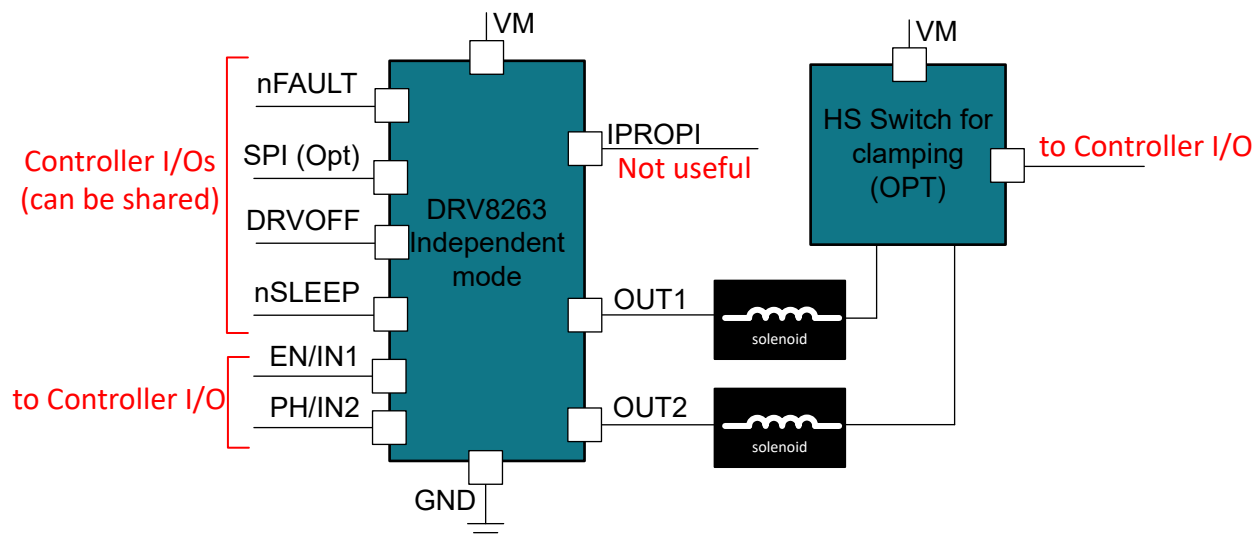


Figure 8-3. Illustration Showing a Half-Bridge Topology to Drive Two High-side Loads Independently With DRV8263-Q1 Device in INDEPENDENT Mode

8.2 Typical Application

The figures below show the typical application schematic for driving a brushed DC motor or any inductive load in various modes. There are several optional connections shown in these schematics, which are listed as follows:

- nSLEEP pin
 - SPI variant - This pin can be tied off high in the application if SLEEP function is not needed.
 - HW variant - Pin control is **mandatory** even if SLEEP function is not needed. The controller needs to issue a **reset pulse** during wake-up to acknowledge wake-up or power-up.
- DRVOFF pin
 - SPI variant - This pin can be tied off low in the application if shutoff through **pin** function is not needed. The equivalent register bit can be used.
- EN/IN1 pin
 - SPI variant - This pin can be tied off low or left floating if register only control is needed.

- PH/IN2 pin
 - SPI variant - This pin can be tied off low or left floating if register only control is needed.
- OUT1 & OUT2 pins
 - Recommend to add PCB footprints for capacitors from OUTx to GND as well as between OUTx close to the load for EMC purposes.
- IPROPI pin
 - All variants - Monitoring of this output is optional. Also IPROPI pin can be tied low if ITRIP feature & IPROPI function is not needed. Recommend to add a PCB footprint for a small capacitor (10nF to 100nF) if needed.
- nFAULT pin
 - SPI variant - Monitoring of this output is optional. All diagnostic information can be read from the STATUS registers.
- SPI input pins
 - SPI variant - Inputs (SDI, nSCS, SCLK) are compatible with 3.3V / 5V levels.
- SPI SDO pin
 - SDO tracks the VDD pin voltage. To interface with a 3.3V level controller input, a level shifter or a current limiting series resistor is recommended.
- CONFIG pins
 - HW variant - Resistor is not needed for short to GND and Hi-Z level selections

8.2.1 HW Variant

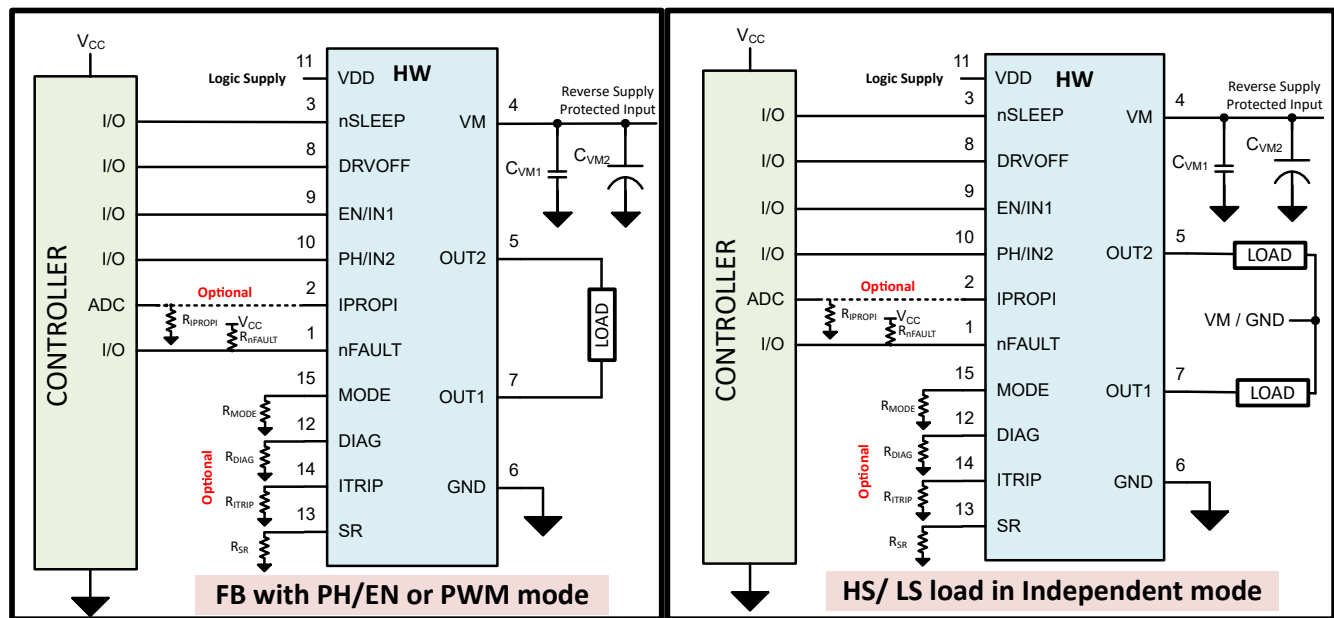


Figure 8-4. Typical Application Schematic - HW Variant

8.2.2 SPI Variant

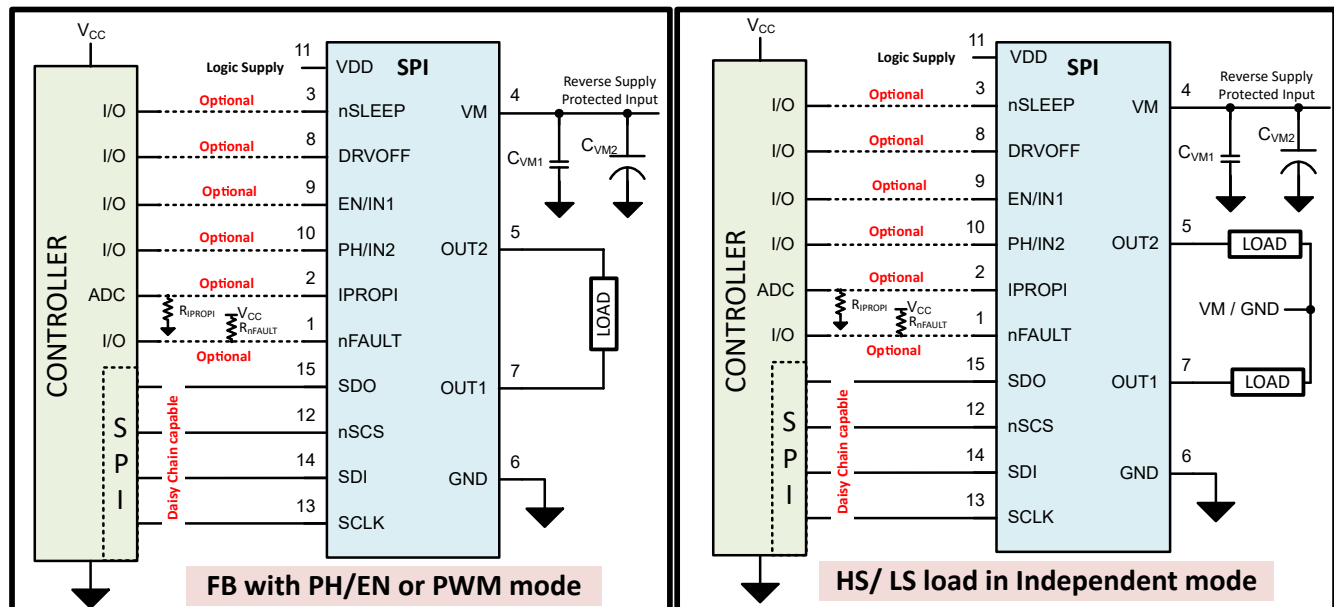


Figure 8-5. Typical Application Schematic - SPI Variant

8.3 Power Supply Recommendations

The device is design to operate with an input voltage supply (VM) range from 4.5 to 65V. A 0.1 μ F ceramic capacitor rated for VM must be placed as close to the device as possible. Also, an appropriately size bulk capacitor must be placed on the VM pin.

8.3.1 Bulk Capacitance Sizing

Bulk capacitance sizing is an important factor in motor drive system design. It is beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors including:

- The highest current required by the motor system.
- The capacitance of the power supply and the ability of the power supply to source current.
- The amount of parasitic inductance between the power supply and motor system.
- The acceptable voltage ripple.
- The type of motor used (brushed DC, brushless DC, and stepper).
- The motor braking method.

The inductance between the power supply and motor drive system limits the rate that current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When sufficient bulk capacitance is used, the motor voltage remains stable, and high current can be quickly supplied.

The data sheet provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

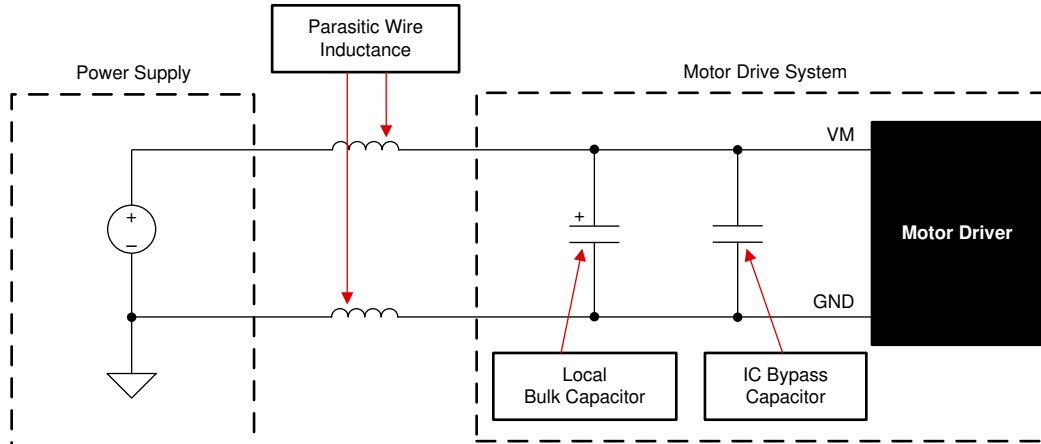


Figure 8-6. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage to provide a margin for cases when the motor transfers energy to the supply.

8.4 Layout

8.4.1 Layout Guidelines

Each VM pin must be bypassed to ground using low-ESR ceramic bypass capacitors with recommended values of 0.1µF rated for VM. These capacitors should be placed as close to the VM pins as possible with a thick trace or ground plane connection to the device GND pin.

Additional bulk capacitance is required to bypass the high current path. This bulk capacitance should be placed such that it minimizes the length of any high current paths. The connecting metal traces should be as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

VDD pin must be bypassed to ground using low-ESR ceramic 6.3V bypass capacitor with recommended values of 0.1µF.

8.4.2 Layout Example

For a layout example of DRV8x63-Q1, please see the EVMs for the following devices:

- [DRV8163S-Q1](#)
- [DRV8163H-Q1](#)
- [DRV8263S-Q1](#)
- [DRV8263H-Q1](#)

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop designs are listed below.

9.1 Device Support

9.2 Documentation Support

9.2.1 Related Documentation

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (January 2025) to Revision A (August 2025)	Page
• Updated device status to Production Data.....	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

[illegible]

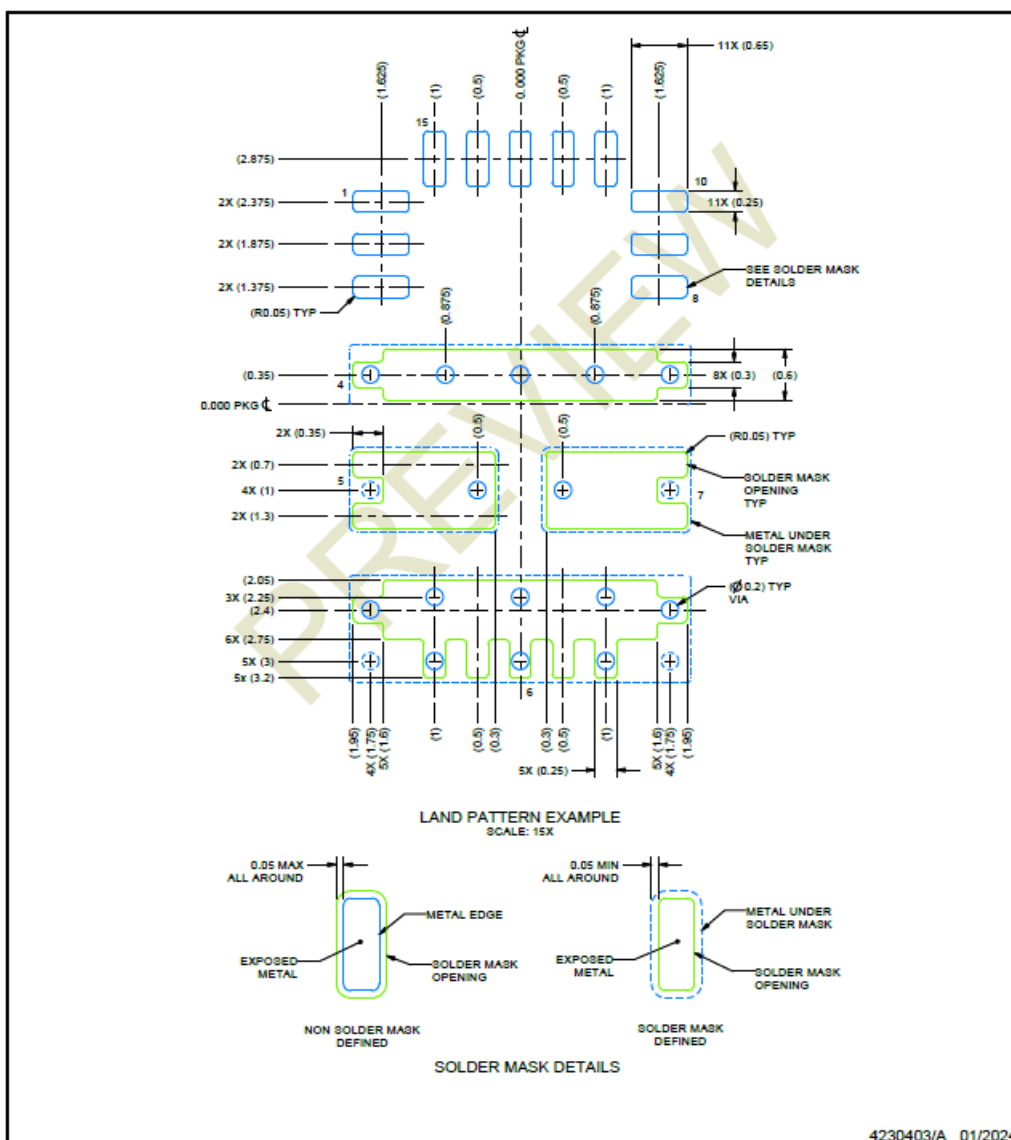
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

VAK0015A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

VQFN-HR - 1 mm max height

SOLDER PASTE EXAMPLE

BASED ON 0.125 mm THICK STENCIL
SCALE: 15X

PAD #	Coverage (%)
PADS 4, 5 & 7:	97%
PAD 6:	84%

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8263HQVAKRQ1	Active	Production	VQFN-HR (VAK) 15	3000 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	8263H

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8263HQAQRQ1	VQFN-HR	VAK	15	3000	330.0	12.4	3.8	6.3	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8263HQAQRQ1	VQFN-HR	VAK	15	3000	367.0	367.0	35.0



VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



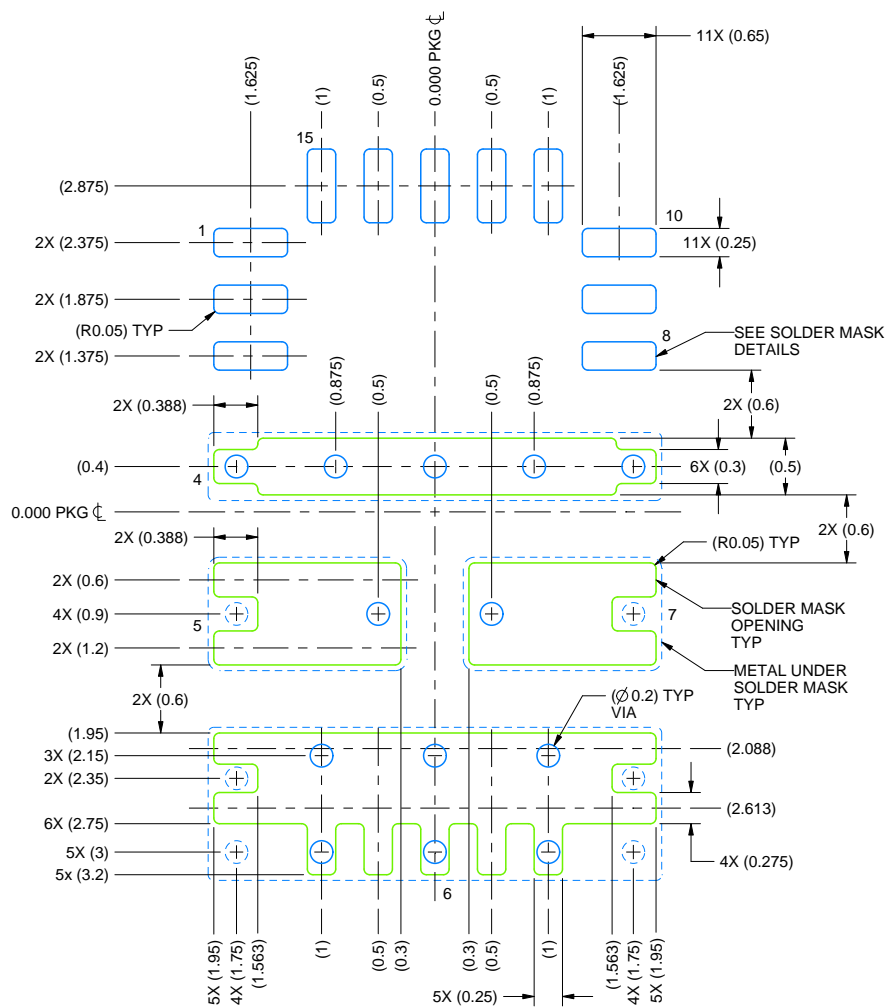
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.

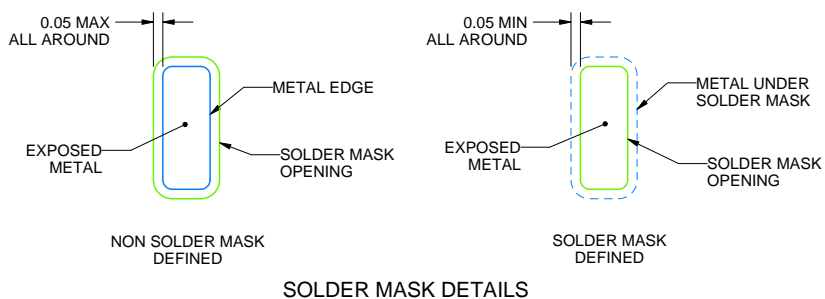
VAK0015A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE: 15X



4230403/C 02/2025

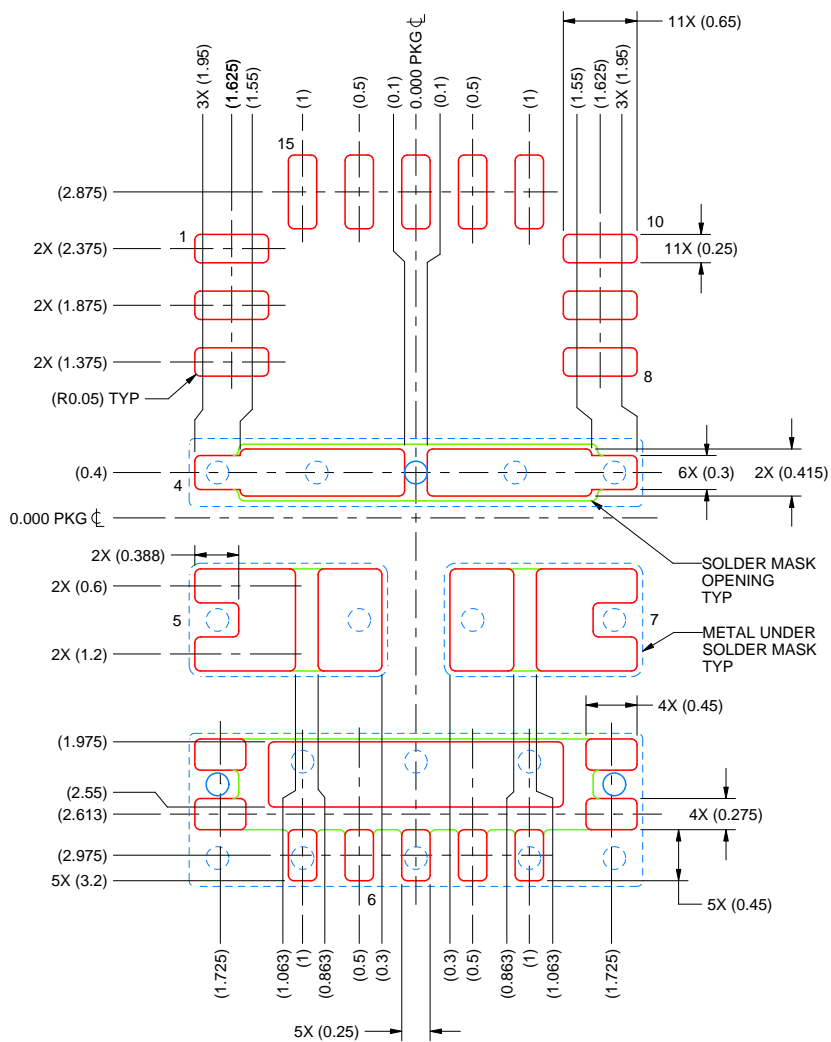
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

VAK0015A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 15X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

PAD 4: 87%
PADS 5 & 7: 89%
PAD 6: 77%

4230403/C 02/2025

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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