DRV8243-Q1 Automotive H-Bridge Driver with Integrated Current Sense and Diagnostics

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- 4.5-V to 35-V (40-V abs. max) operating range
- VQFN-HR package: R_{ON_LS} + R_{ON_HS}: 84 mΩ
- HVSSOP package: R_{ON_LS} + R_{ON_HS}: 98 mΩ
- I_{OUT} Max = 12 A
- PWM frequency operation up to 25 KHz with automatic dead time assertion
- Configurable slew rate and spread spectrum clocking for low electromagnetic interference (EMI)
- Integrated current sense (eliminates shunt resistor)
- Proportional load current output on IPROPI pin
- Configurable current regulation
- Protection and diagnostic features with configurable fault reaction (latched or retry)
  - Load diagnostics in both the off-state and on-state to detect open load and short circuit
  - Voltage monitoring on supply (VM)
  - Over current protection
  - Over temperature protection
  - Fault indication on nFAULT pin
- Supports 3.3-V, 5-V logic inputs
- Low sleep current - 1µA typical at 25°C
- 3 variants - HW (H), SPI (S) or SPI (P)
- Configurable control modes:
  - Single full bridge using PWM or PH/EN mode
  - Two half-bridges using Independent mode
- Device family comparison table

2 Applications

- Automotive brushed DC motors, Solenoids
- Door modules , mirror modules, and seat modules
- Body control module (BCM)
- E-Shifter
- Gas engine systems
- On board charger

3 Description

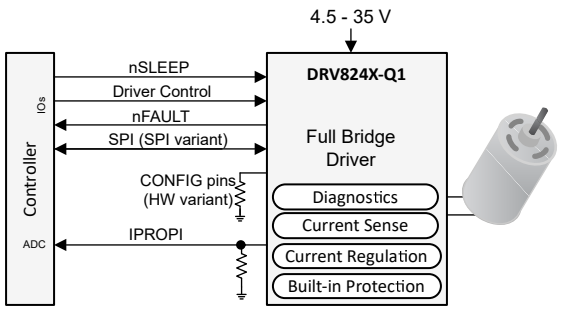
The DRV824x-Q1 family of devices is a fully integrated H-bridge driver intended for a wide range of automotive applications. The device can be configured as a single full-bridge driver or as two independent half-bridge drivers. Designed in a BiCMOS high power process technology node, this monolithic family of devices in a power package offer excellent power handling and thermal capability while providing compact package size, ease of layout, EMI control, accurate current sense, robustness, and diagnostic capability. This family provides an identical pin function with scalable R_{ON} (current capability) to support different loads.

The devices integrate a N-channel H-bridge, charge pump regulator, high-side current sensing with regulation, current proportional output, and protection circuitry. A low-power sleep mode is provided to achieve low quiescent current. The devices offer voltage monitoring and load diagnostics as well as protection features against over current and over temperature. Fault conditions are indicated on nFAULT pin. The devices are available in three variants - hardwired interface: HW (H) and two SPI interface variants: SPI(P) and SPI(S), with SPI (P) for externally supplied logic supply and SPI (S) for internally generated logic supply. The SPI interface variants offer more flexibility in device configuration and fault observability.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (nominal)
DRV8243-Q1	VQFN-HR (14)	3 mm X 4.5 mm
DRV8243-Q1	HVSSOP (28)	3 mm X 7.3 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2022) to Revision C (August 2022)	Page
• Added footer to allow Absolute Maximum Rating violation on VM pin during ISO 7637 transients	11
• Improved footer description on short protection	12
• EC table - HVSSOP package only - Lowered A_{IPROPI} accuracy from 5% to 6%, and A_{IPROPI} matching from 2% to 5%	17
• Typical characteristics - Added FET RON plot for leaded package	27

Changes from Revision A (January 2022) to Revision B (July 2022)	Page
• Device comparison - Removed pre-production information, slew rate and off-state diagnostics feature exceptions for DRV8245HRXZQ1 and DRV8244SRYJQ1	4
• Corrected pin name typo for PH/IN2	11
• EC table - $R_{LVL3of3}$ for MODE pin increased to 250 KΩ minimum	14
• EC table - Updated typical R_{ON} values	14
• Typical characteristics - Corrected FET RON plot, improved A_{IPROPI} plot	27
• Block diagram for P-variant - Corrected VDD pin typo	30
• Feature description for PWM mode - Removed pre-production information	34
• Feature description for Register - Pin control - Removed pre-production information	36
• Feature description for SR - Removed pre-production information and duplication of SR tables (Refer EC table instead)	37
• Feature description for ITRIP regulation - Removed pre-production information, added note on linear ITRIP levels using external DAC	37
• Feature description for DIAG pin (HW variant only) - Corrected behavior for LVL5 setting	39
• Feature description update for OLA - Added clarification on fault clearing when drive direction is reversed	44
• Functional states - Removed pre-production information	46
• SDO frame - Removed pre-production information	49
• User registers - Removed pre-production information	54
• Typical application - Added recommendations for EMC	61

Changes from Revision * (November 2021) to Revision A (January 2022)	Page
• Updated device status to Mixed Production	1

5 Device Comparison

Table 5-1 summarizes the R_{ON} and package differences between devices in the DRV824X-Q1 family.

Table 5-1. Device Comparison

PART NUMBER(1)	(LS + HS) R_{ON}	I_{OUT} MAX	PACKAGE	BODY SIZE (nominal)	Variants
DRV8243-Q1	84 mΩ	12 A	VQFN-HR (14)	3 mm X 4.5 mm	HW (H), SPI (S)
DRV8243-Q1	98 mΩ	12 A	HVSSOP (28)	3 mm X 7.3 mm	HW (H), SPI (S), SPI (P)
DRV8244-Q1	47 mΩ	21 A	VQFN-HR (16)	3 mm X 6 mm	HW (H), SPI (S)
DRV8244-Q1	60 mΩ	21 A	HVSSOP (28)	3 mm X 7.3 mm	HW (H), SPI (S), SPI (P)
DRV8245-Q1	32 mΩ	32 A	VQFN-HR (16)	3.5 mm X 5.5 mm	HW (H), SPI (S)
DRV8245-Q1	40 mΩ	32 A	HTSSOP (28)	4.4 mm X 9.7 mm	HW (H), SPI (S), SPI (P)

(1) This is the product datasheet for the DRV8243-Q1. Please reference other device variant data sheets for additional information.

Table 5-2 summarizes the feature differences between the SPI and HW interface variants in the DRV824X-Q1 family. In general, the SPI variant offers more configurability, bridge control options, diagnostic feedback, redundant driver shutoff, improved Pin FMEA and additional features.

In addition, the SPI variant has two options - **SPI (S) variant and SPI (P) variant**. The SPI (P) variant supports an external, low voltage 5 V supply to the device through the VDD pin for the device logic, whereas in the SPI (S) variant, this supply is internally derived from the VM pin. With this external logic supply, the SPI (P) variant avoids device brown out (reset of device) during VM under voltage transients.

Table 5-2. SPI Variant vs HW Variant Comparison

FUNCTION	HW (H) Variant	SPI (S) Variant	SPI (P) Variant
Bridge control	Pin only	Individual pin **"and/or"** register bit with pin status indication (Refer Register Pin control)	
Sleep function	Available through nSLEEP pin		Not available
External logic supply to the device	Not supported	Not supported	Supported through VDD pin
Clear fault command	Reset pulse on nSLEEP pin	SPI CLR_FAULT command	
Slew rate	6 levels	8 levels	
Over current protection (OCP)	Fixed at the highest setting	3 choices for thresholds, 4 choices for filter time	
ITRIP regulation	5 levels with disable & fixed TOFF time	7 levels with disable & indication, with programmable TOFF time	
Individual fault reaction configuration between retry or latched behavior	Not supported, either all latched or all retry	Supported	
Detailed fault logging and device status feedback	Not supported, nFAULT pin monitoring necessary	Supported, nFAULT pin monitoring optional	
VM over voltage	Fixed	4 threshold choices	
On-state (Active) diagnostics	Not supported	Supported for high-side loads	
Spread spectrum clocking (SSC)	Not supported	Supported	
Additional driver states in PWM mode	Not supported	Supported	
Hi-Z for individual half-bridge in Independent mode	Not supported	Supported (SPI register only)	

Table 5-3. Differentiating between devices in the family

Device	Package Symbolization	DEVICE_ID Register
DRV8243H-Q1	8243H	Not applicable
DRV8244H-Q1	8244H	Not applicable
DRV8245H-Q1	8245H	Not applicable
DRV8243S-Q1	8243S	0 x 32
DRV8244S-Q1	8244S	0 x 42

Table 5-3. Differentiating between devices in the family (continued)

Device	Package Symbolization	DEVICE_ID Register
DRV8245S-Q1	8245S	0 x 52
DRV8243P-Q1	8243P	0 x 36
DRV8244P-Q1	8244P	0 x 46
DRV8245P-Q1	8245P	0 x 56

6 Pin Configuration and Functions

6.1 HW Variant

6.1.1 HVSSOP (28) package

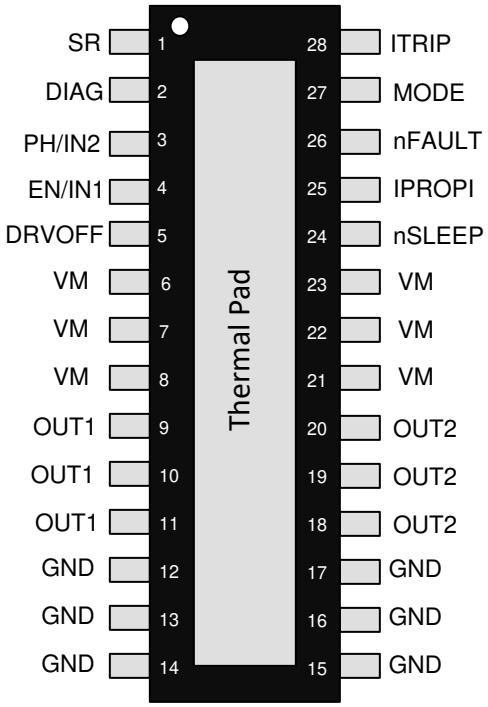

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Figure 6-1. DRV8243H-Q1 HW variant in HVSSOP (28) package

Table 6-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	SR	I	Device configuration pin for Slew Rate control . For details, refer to Slew Rate in the Device Configuration section.
2	DIAG	I	Device configuration pin for load type indication and fault reaction configuration. For details, refer to DIAG in the Device Configuration section.
3	PH/IN2	I	Controller input pin for bridge operation. For details, see the Bridge Control section.
4	EN/IN1	I	Controller input pin for bridge operation. For details, see the Bridge Control section.
5	DRVOFF	I	Controller input pin for bridge Hi-Z. For details, see the Bridge Control section.
6, 7, 8, 21, 22, 23	VM	P	Power supply. This pin is the motor supply voltage. Must combine with the rest of VM pins (6 total) to support device current capability. Bypass this pin to GND with a 0.1-µF ceramic capacitor and a bulk capacitor.
9, 10, 11	OUT1	P	Half-bridge output 1. Connect this pin to the motor or load. Must combine with the rest of OUT1 pins (3 total) to support device current capability.
12, 13, 14, 15, 16, 17	GND	G	Ground pin. Must combine with the rest of GND pins (6 total) to support device current capability.
18, 19, 20	OUT2	P	Half-bridge output 2. Connect this pin to the motor or load. Must combine with the rest of OUT2 pins (3 total) to support device current capability.
24	nSLEEP	I	Controller input pin for SLEEP. For details, see the Bridge Control section.
25	IPROPI	I/O	Driver load current analog feedback. For details, refer to IPROPI in the Device Configuration section.
26	nFAULT	OD	Fault indication to the controller. For details, refer to nFAULT in the Device Configuration section.

Table 6-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
27	MODE	I	Device configuration pin for MODE. For details, refer to the Device Configuration section.
28	ITRIP	I	Device configuration pin for ITRIP level for high-side current limiting. For details, refer to ITRIP in the Device Configuration section.

(1) I = input, O = output, I/O = input/output, G = ground, P = power, OD = open-drain output, PP = push-pull output

6.1.2 VQFN-HR (14) package

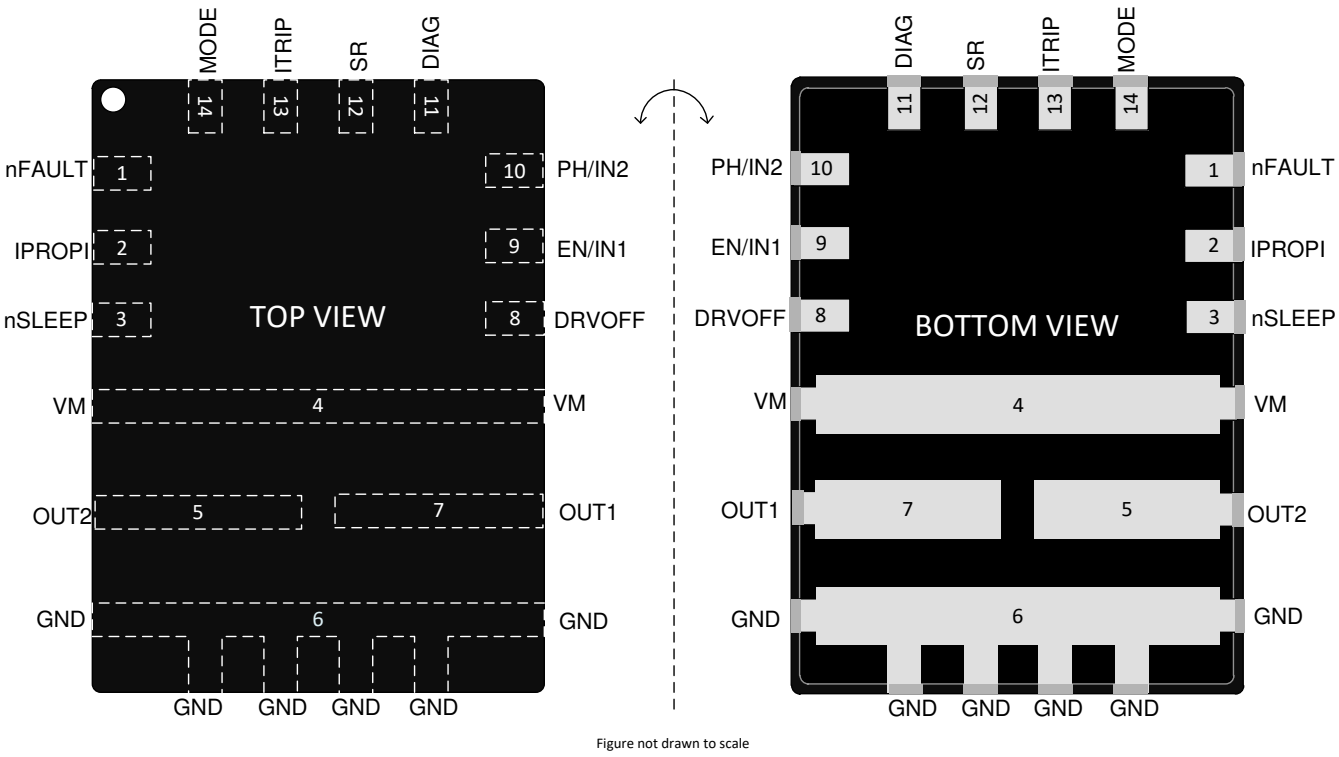

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Figure 6-2. DRV8243H-Q1 HW variant in VQFN-HR (14) package

Table 6-2. Pin Functions

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
1	nFAULT	OD	Fault indication to the controller. For details, refer to nFAULT in the Device Configuration section.
2	IPROPI	I/O	Driver load current analog feedback. For details, refer to IPROPI in the Device Configuration section.
3	nSLEEP	I	Controller input pin for SLEEP . For details, see the Bridge Control section.
4	VM	P	Power supply. This pin is the motor supply voltage. Bypass this pin to GND with a 0.1-µF ceramic capacitor and a bulk capacitor.
5	OUT2	P	Half-bridge output 2. Connect this pin to the motor or load.
6	GND	G	Ground pin
7	OUT1	P	Half-bridge output 1. Connect this pin to the motor or load.
8	DRVOFF	I	Controller input pin for bridge Hi-Z. For details, see the Bridge Control section.
9	EN/IN1	I	Controller input pin for bridge operation. For details, see the Bridge Control section.
10	PH/IN2	I	Controller input pin for bridge operation. For details, see the Bridge Control section.
11	DIAG	I	Device configuration pin for load type indication and fault reaction configuration. For details, refer to DIAG in the Device Configuration section.

Table 6-2. Pin Functions (continued)

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
12	SR	I	Device configuration pin for Slew Rate control . For details, refer to Slew Rate in the Device Configuration section.
13	ITRIP	I	Device configuration pin for ITRIP level for high-side current limiting. For details, refer to ITRIP in the Device Configuration section.
14	MODE	I	Device configuration pin for MODE. For details, refer to the Device Configuration section.

(1) I = input, O = output, I/O = input/output, G = ground, P = power, OD = open-drain output, PP = push-pull output

6.2 SPI Variant

6.2.1 HVSSOP (28) package

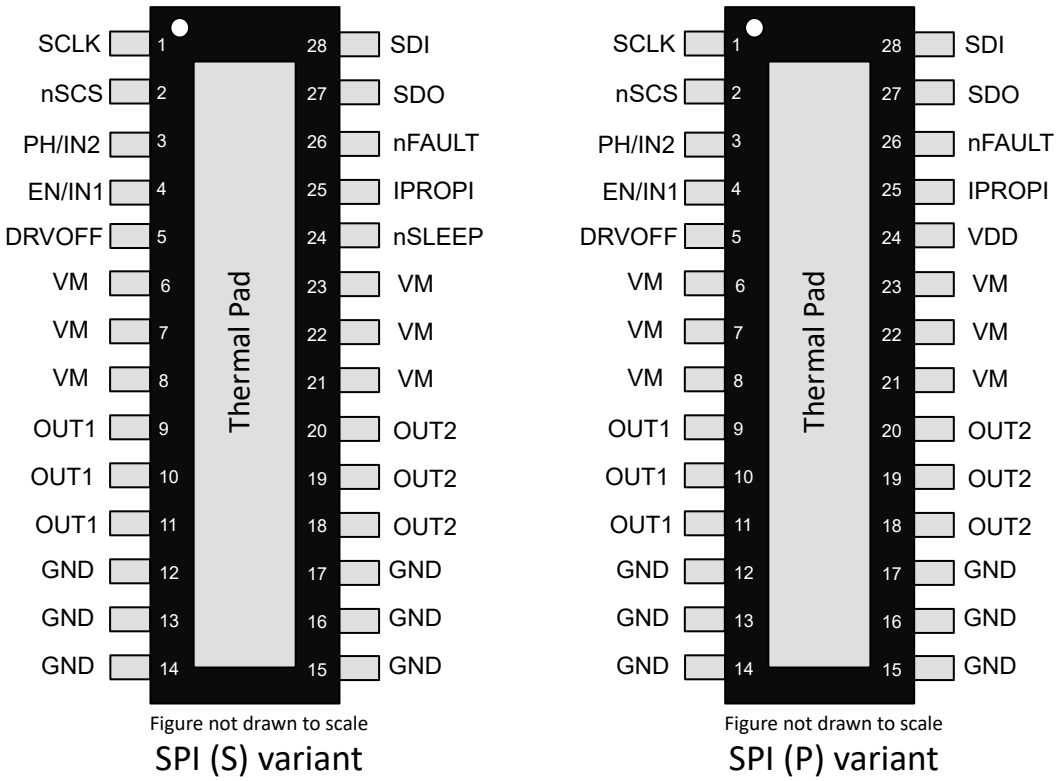

Figure 6-3. DRV8243S-Q1 SPI variant in HVSSOP (28) package

Table 6-3. Pin Functions

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
1	SCLK	I	SPI - Serial Clock input.
2	nSCS	I	SPI - Chip Select. An active low on this pin enables the serial interface communication.
3	PH/IN2	I	Controller input pin for bridge operation. For details, see the Bridge Control section.
4	EN/IN1	I	Controller input pin for bridge operation. For details, see the Bridge Control section.
5	DRVOFF	I	Controller input pin for bridge Hi-Z. For details, see the Bridge Control section.
6, 7, 8, 21, 22, 23	VM	P	Power supply. This pin is the motor supply voltage. Must combine with the rest of VM pins (6 total) to support device current capability. Bypass this pin to GND with a 0.1-µF ceramic capacitor and a bulk capacitor.
9, 10, 11	OUT1	P	Half-bridge output 1. Connect this pin to the motor or load. Must combine with the rest of OUT1 pins (3 total) to support device current capability.

Table 6-3. Pin Functions (continued)

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
12, 13, 14, 15, 16, 17	GND	G	Ground pin. Must combine with the rest of GND pins (6 total) to support device current capability.
18, 19, 20	OUT2	P	Half-bridge output 2. Connect this pin to the motor or load. Must combine with the rest of OUT2 pins (3 total) to support device current capability.
24	nSLEEP	I	SPI (S) variant: Controller input pin for SLEEP. For details, see the Bridge Control section. Also VIO logic level for SDO.
	VDD	P	SPI (P) variant: Logic power supply to the device.
25	IPROPI	I/O	Driver load current analog feedback. For details, refer to IPROPI in the Device Configuration section.
26	nFAULT	OD	Fault indication to the controller. For details, refer to nFAULT in the Device Configuration section.
27	SDO	PP	SPI - Serial Data Output. Data is updated at the rising edge of SCLK.
28	SDI	I	SPI - Serial Data Input. Data is captured at the falling edge of SCLK.

(1) I = input, O = output, I/O = input/output, G = ground, P = power, OD = open-drain output, PP = push-pull output

6.2.2 VQFN-HR (14) package

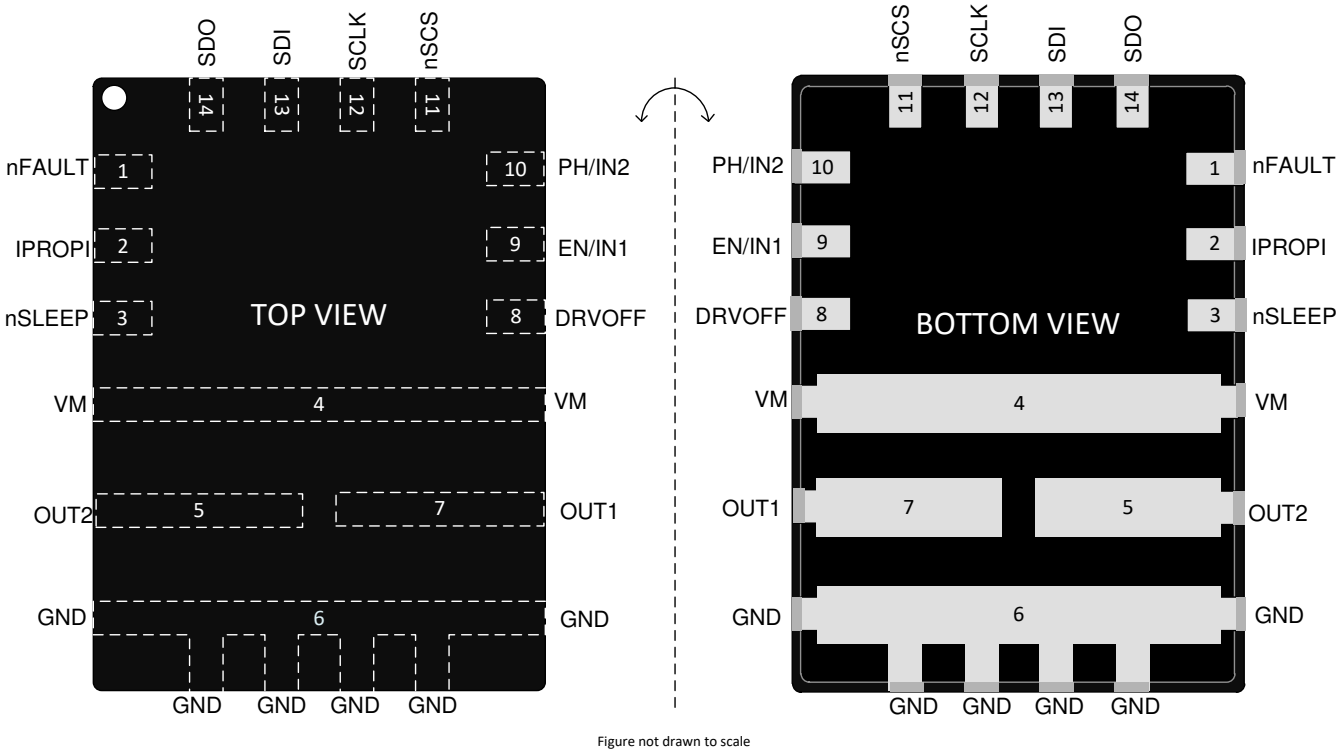

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Figure 6-4. DRV8243S-Q1 SPI variant in VQFN-HR (14) package

Table 6-4. Pin Functions

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
1	nFAULT	OD	Fault indication to the controller. For details, refer to nFAULT in the Device Configuration section.
2	IPROPI	O	Driver load current analog feedback. For details, refer to IPROPI in the Device Configuration section.
3	nSLEEP	I	Controller input pin for SLEEP. For details, see the Bridge Control section. Also VIO logic level for SDO.

Table 6-4. Pin Functions (continued)

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
4	VM	P	Power supply. This pin is the motor supply voltage. Bypass this pin to GND with a 0.1-µF ceramic capacitor and a bulk capacitor.
5	OUT2	P	Half-bridge output 2. Connect this pin to the motor or load.
6	GND	G	Ground pin
7	OUT1	P	Half-bridge output 1. Connect this pin to the motor or load.
8	DRVOFF	I	Controller input pin for bridge Hi-Z. For details, see the Bridge Control section.
9	EN/IN1	I	Controller input pin for bridge operation. For details, see the Bridge Control section.
10	PH/IN2	I	Controller input pin for bridge operation. For details, see the Bridge Control section.
11	nSCS	I	SPI - Chip Select. An active low on this pin enables the serial interface communication.
12	SCLK	I	SPI - Serial Clock input.
13	SDI	I	SPI - Serial Data Input. Data is captured at the falling edge of SCLK.
14	SDO	PP	SPI - Serial Data Output. Data is updated at the rising edge of SCLK.

(1) I = input, O = output, I/O = input/output, G = ground, P = power, OD = open-drain output, PP = push-pull output

7 Specifications

7.1 Absolute Maximum Ratings

Over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply pin voltage	VM	–0.3(3)	40	V
Power supply transient voltage ramp	VM		2	V/µs
Output pin voltage	OUT1, OUT2	-0.9	V_{VM} + 0.9	V
Output pin current	OUT1, OUT2	Internally limited(2)		A
Driver disable pin voltage	DRVOFF	–0.3	40	V
Logic I/O voltage	EN/IN1, PH/IN2, nFAULT	–0.3	5.75	V
HW variant - Configuration pins voltage	MODE, ITRIP, SR, DIAG	–0.3	5.75	V
Analog feedback pin voltage	IPROPI	–0.3	5.75	V
Sleep pin voltage (Not applicable for SPI (P) variant)	nSLEEP	–0.3	40	V
SPI I/O voltage - SPI variant	SDI, SDO, nSCS, SCLK	–0.3	5.75	V
SPI (P) variant - Logic supply	VDD	-0.3	5.75	V
SPI (P) variant - Logic supply transient voltage ramp	VDD		5	V/µs
Ambient temperature, T_A		–40	125	°C
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Limited by the over current and over temperature protection functions of the device
(3) With external component support, short duration violation of this limit can be tolerated during ISO 7637 transient pulse testing

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	VM, OUT1, OUT2, GND	±4000	V
			All other pins	±2000	
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	Corner pins	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{VM}	Power supply voltage	VM	4.5	35(1)	V
V_{VDD}	SPI (P) variant - Logic supply voltage	VDD	4.5	5.5	V
V_{LOGIC}	Logic pin voltage	EN/IN1, PH/IN2, nSLEEP, DRVOFF, nFAULT	0	5.5	V
f_{PWM}	PWM frequency	EN/IN1, PH/IN2	0	25	KHz
V_{CONFIG}	HW variant - Configuration pin voltage	MODE, ITRIP, SR, DIAG	0	5.5	V
V_{IPROPI}	Analog feedback voltage	IPROPI	0	5.5	V
V_{SPI_IOS}	SPI (S) variant - SPI pin voltage	SDI, SDO, nSCS, SCLK	0	V_{nSLEEP} + 0.5	V
	SPI (P) variant - SPI pin voltage	SDI, SDO, nSCS, SCLK	0	V_{VDD} + 0.5	V
T_A	Operating ambient temperature		–40	125	°C
T_J	Operating junction temperature		–40	150	°C

(1) The over current protection function does not support short on OUTx to VM or GND above 28 V for short inductance < 1 µH.

7.4 Thermal Information

Refer Transient thermal impedance table for application related use case.

THERMAL METRIC(1)		HVSSOP package	VQFN-HR package	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.0	48.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	29.1	22.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.3	8.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.4	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.3	7.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	1.3	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

4.5 V (falling) ≤ V_{VM} ≤ 35 V, -40°C ≤ T_J ≤ 150°C (unless otherwise noted)
For SPI (P) variant only: 4.5 V ≤ V_{VDD} ≤ 5.5 V (unless otherwise noted)

7.5.1 Power Supply & Initialization

Refer wake up transient waveforms

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VM_REV}	Supply pin voltage during reverse current	I_{VM} = - 5 A, device in unpowered state		1.4		V
I_{VMQ}	VM current in SLEEP state	V_{VM} = 13.5 V, V_{nSLEEP} = 0 V or V_{VDD} < POR_{VDD_FALL}, T_A = 25°C		1		µA
		V_{VM} = 13.5 V, V_{nSLEEP} = 0 V or V_{VDD} < POR_{VDD_FALL}, T_A = 125°C			5.8	µA
I_{VMS}	VM current in STANDBY state	V_{VM} = 13.5 V		3	5	mA
I_{VDD}	VDD current in ACTIVE state	SPI (P) variant			10	mA
t_{RESET}	RESET pulse filter time	Reset signal on nSLEEP pin for HW (H) variant	5		20	µs
t_{SLEEP}	SLEEP command filter time	Sleep signal on nSLEEP pin for HW (H) variant	40		120	µs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SLEEP_SPI}	SLEEP command filter time	Sleep signal on nSLEEP pin for SPI (S) variant	5		20	µs
t_{WAKEUP}	Wake-up command filter time	Wake-up signal on nSLEEP pin for HW (H) and SPI (S) variants		10		µs
t_{COM}	Time for communication to be available after wake-up or power-up through VM or VDD supply pin	Wake-up signal on nSLEEP pin or power cycle - V_{VM} > VM_{POR_RISE} or V_{VDD} > VDD_{POR_RISE}			400	µs
t_{READY}	Time for driver ready to be driven after wake-up through nSLEEP pin or power-up through VM or VDD supply pin	Wake-up signal on nSLEEP pin or power cycle - V_{VM} > VM_{POR_RISE} or V_{VDD} > VDD_{POR_RISE}			1	ms

7.5.2 Logic I/Os

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL_nSLEEP}	Input logic low voltage	nSLEEP pin			0.65	V
V_{IH_nSLEEP}	Input logic high voltage	nSLEEP pin	1.55			V
V_{IHYS_nSLEEP}	Input hysteresis	nSLEEP pin		200		mV
V_{IL}	Input logic low voltage	DRVOFF, EN/IN1, PH/IN2 pins			0.7	V
V_{IH}	Input logic high voltage	DRVOFF, EN/IN1, PH/IN2 pins	1.5			V
V_{IHYS}	Input hysteresis	DRVOFF, EN/IN1, PH/IN2 pins		100		mV
R_{PD_nSLEEP}	Internal pull-down resistance on nSLEEP to GND	Measured at min VIL level	100		400	KΩ
R_{PU}	Internal pull-up resistance to VDD (reverse current blocked) on DRVOFF	Measured at min VIH level	200		550	KΩ
R_{PD}	Internal pull-down resistance to GND on EN/IN1 and PH/IN2	Measured at max VIL level	200		500	KΩ
I_{nFAULT_PD}	Sink current to GND on nFAULT pin when asserted low	V_{nFAULT} = 0.3 V	5			mA

7.5.3 SPI I/Os

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PU_nSCS}	Internal pull-up resistance to VDD (reverse current blocked) on nSCS	Measured at min VIH level	200		500	KΩ
R_{PD_SPI}	Internal pull-down resistance to GND on SDI, SCLK	Measured at max VIL level	150		500	KΩ
V_{IL}	Input logic low voltage	SDI, SCLK, nSCS pins			0.7	V
V_{IH}	Input logic high voltage	SDI, SCLK, nSCS pins	1.5			V
V_{IHYS}	Input hysteresis	SDI, SCLK, nSCS pins		100		mV
V_{OL_SDO}	Output logic low voltage	0.5 mA sink into SDO			0.4	V
V_{OH_SDO}	Output logic high voltage for SPI (S) variant	0.5 mA source from SDO, V_{nSLEEP} = 5 V, V_{VM} > 7 V	4.1			V
		0.5 mA source from SDO, V_{nSLEEP} = 3.3 V, V_{VM} > 5 V	2.7			V
	Output logic high voltage for SPI (P) variant	0.5 mA source from SDO, V_{VDD} = 5 V	4.5			V
$V_{OH\_SDO\_NL}$	Output logic high voltage at no load on SDO, valid only for SPI (S) variant	No current from SDO, V_{nSLEEP} = 5 V, V_{VM} > 7 V			5.5	V
		No current from SDO, V_{nSLEEP} = 3.3 V, V_{VM} > 5 V			3.8	V

7.5.4 Configuration Pins - HW Variant Only

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
6 level setting for ITRIP, SR and DIAG						
$R_{LVL1OF6}$	Level 1 of 6	Connect to GND			10	Ω
$R_{LVL2OF6}$	Level 2 of 6	+/- 10% resistor to GND	7.4	8.2	9	KΩ
$R_{LVL3OF6}$	Level 3 of 6	+/- 10% resistor to GND	19.8	22	24.2	KΩ
$R_{LVL4OF6}$	Level 4 of 6	+/- 10% resistor to GND	42.3	47	51.7	KΩ
$R_{LVL5OF6}$	Level 5 of 6	+/- 10% resistor to GND	90	100	110	KΩ
$R_{LVL6OF6}$	Level 6 of 6	Hi-Z (no connect)	250			KΩ
3 level setting for MODE						
$R_{LVL1OF3}$	Level 1 of 3	Connect to GND			10	Ω
$R_{LVL2OF3}$	Level 2 of 3	+/- 10% resistor to GND	7.4	8.2	9	KΩ
$R_{LVL3OF3}$	Level 3 of 3	Hi-Z (no connect)	250			KΩ

7.5.5 Power FET Parameters

Measured at V_{VM} = 13.5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{HS_ON}	High-side FET on resistance, HVSSOP package	I_{OUT} = 3 A, T_J = 25°C		49		mΩ
		I_{OUT} = 3 A, T_J = 150°C			93.1	mΩ
	High-side FET on resistance, VQFN-HR package	I_{OUT} = 3 A, T_J = 25°C		41.7		mΩ
		I_{OUT} = 3 A, T_J = 150°C			79.8	mΩ
R_{LS_ON}	Low-side FET on resistance, HVSSOP package	I_{OUT} = 3 A, T_J = 25°C		49		mΩ
		I_{OUT} = 3 A, T_J = 150°C			93.1	mΩ
	Low-side FET on resistance, VQFN-HR package	I_{OUT} = 3 A, T_J = 25°C		42		mΩ
		I_{OUT} = 3 A, T_J = 150°C			79.8	mΩ
V_{SD}	Low-side & High-side FET source-drain voltage when body diode is forward biased	I_{OUT} = +/- 3 A (both directions)	0.4	0.9	1.5	V
R_{Hi-Z}	OUT resistance to GND in SLEEP or STANDBY state, V_{OUTx} = V_{VM} = 13.5 V	SR = 3'b000 or 3'b001 or 3'b010 or 3'b111 or LVL2 or LVL5	2		5	KΩ
		SR = 3'b011 or LVL3	7		14	KΩ
		SR = 3'b100 or LVL4	5		10.5	KΩ
		SR = 3'b101 or LVL1	4		8.5	KΩ
		SR = 3'b110 or LVL6	2.5		6	KΩ

7.5.6 Switching Parameters with High-Side Recirculation

Load = 1.5mH / 4.7 Ohm, V_{VM} = 13.5 V, refer high-side recirculation waveform

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR_{LSOFF}	Output voltage rise time, 10% - 90%	SR = 3'b000 or LVL2		1.6		V/µs
		SR = 3'b001 (SPI only)		5		V/µs
		SR = 3'b010 (SPI only)		8		V/µs
		SR = 3'b011 or LVL3		13.3		V/µs
		SR = 3'b100 or LVL4		19		V/µs
		SR = 3'b101 or LVL1		24.5		V/µs
		SR = 3'b110 or LVL6		36		V/µs
		SR = 3'b111 or LVL5		47		V/µs
t_{PD_LSOFF}	Propagation time during output voltage rise	SR = 3'b000 or LVL2		1		µs
		SR = 3'b001 (SPI only)		0.9		µs
		SR = 3'b010 (SPI only)		0.8		µs
		SR = 3'b011 or LVL3		0.7		µs
		SR = 3'b100 & 3'b101 or LVL4 & LVL1		0.6		µs
		SR = 3'b110 & 3'b111 or LVL6 & LVL5		0.5		µs
t_{DEAD_LSOFF}	Dead time during output voltage rise	All SRs		0.9		µs
SR_{LSON}	Output voltage fall time, 90% - 10%	SR = 3'b000 or LVL2		1.6		V/µs
		SR = 3'b001 (SPI only)		5		V/µs
		SR = 3'b010 (SPI only)		8		V/µs
		SR = 3'b011 or LVL3		13.3		V/µs
		SR = 3'b100 or LVL4		19		V/µs
		SR = 3'b101 or LVL1		24.5		V/µs
		SR = 3'b110 or LVL6		36		V/µs
		SR = 3'b111 or LVL5		47		V/µs
t_{PD_LSON}	Propagation time during output voltage fall	SR = 3'b000 or LVL2		0.2		µs
		SR = 3'b001 (SPI only)		0.2		µs
		SR = 3'b010 (SPI only)		0.2		µs
		SR = 3'b011 or LVL3		0.4		µs
		SR = 3'b100 or 3'b101 or LVL4 or LVL1		0.3		µs
		SR = 3'b110 & 3'b111 or LVL6 & LVL5		0.2		µs
t_{DEAD_LSON}	Dead time during output voltage fall	SR = 3'b000 or LVL2		1.5		µs
		SR = 3'b001 or 3'b010 (SPI only)		0.6		µs
		SR = 3'b011 or LVL3		0.7		µs
		All other SRs		0.6		µs
$Match_{SRLS}$	Output voltage rise and fall slew rate matching	All SRs	-20		+20	%

7.5.7 Switching Parameters with Low-Side Recirculation

Load = 1.5 mH / 4.7 Ohm, V_{VM} = 13.5 V, refer low-side recirculation waveform

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR_{HSON}	Output voltage rise time, 10% - 90%	All SRs		8		V/µs
t_{PD_HSON}	Propagation time during output voltage rise	SR = 3'b000 or LVL2		3.1		µs
		SR = 3'b001 (SPI only)		2		µs
		SR = 3'b010 (SPI only)		1.7		µs
		SR = 3'b011 or LVL3		1.2		µs
		All other SRs		0.9		µs
t_{DEAD_HSON}	Dead time during output voltage rise	SR = 3'b000 or LVL2		1.5		µs
		SR = 3'b001 (SPI only)		1		µs
		SR = 3'b010 (SPI only)		0.8		µs
		All other SRs		0.45		µs
SR_{HSOFF}	Output voltage fall time, 90% - 10%	SR = 3'b000 or 3'b001 or 3'b010 or LVL2		43		V/µs
		SR = 3'b011 or LVL3		14		V/µs
		SR = 3'b100 or LVL4		19		V/µs
		SR = 3'b101 or LVL1		24		V/µs
		SR = 3'b110 or LVL6		34		V/µs
		SR = 3'b111 or LVL5		43		V/µs
t_{PD_HSOFF}	Propagation time during output voltage fall	All SRs		0.25		µs
t_{DEAD_HSOFF}	Dead time during output voltage fall	All SRs		0.2		µs
t_{BLANK}	Current regulation blanking time after OUT slewing for current sense output to settle (Valid for only for LS recirculation)	All SRs		3.4		µs

7.5.8 IPROPI & ITRIP Regulation

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
A_{IPROPI}	Current scaling factor, HVSSOP package			3075		A/A
	Current scaling factor, VQFN-HR package			3070		A/A
A_{I_ERR}	Current scaling factor error, VQFN-HR package	0.8 A < I_{OUT} < 4.3 A	-5		+5	%
		0.2 A < I_{OUT} ≤ 0.8 A	-20		+20	%
		0.1 A < I_{OUT} ≤ 0.2 A	-50		+50	%
A_{I_ERR}	Current scaling factor error, HVSSOP package	0.8 A < I_{OUT} < 4.3 A	-6		+6	%
		0.2 A < I_{OUT} ≤ 0.8 A	-20		+20	%
		0.1 A < I_{OUT} ≤ 0.2 A	-50		+50	%
$A_{I\_ERR\_M}$	Current matching between the two half-bridges, VQFN-HR package	I_{OUT} > 0.8 A	-2		+2	%
$A_{I\_ERR\_M}$	Current matching between the two half-bridges, HVSSOP package	I_{OUT} > 0.8 A	-5		+5	%
$Offset_{IPROPI}$	Offset current on IPROPI at no load current	I_{OUT} = 0 A			15	µA
BW_{IPROPI}	Bandwidth of the IPROPI internal sense circuit	No external capacitor on IPROPI.	400			KHz
V_{IPROPI_LIM}	Internal clamping voltage on IPROPI		4.5		5.5	V
V_{ITRIP_LVL}	Voltage limit on V_{IPROPI} to trigger TOFF cycle for ITRIP regulation	ITRIP = 3'b001 or LVL2	1.06	1.18	1.3	V
		ITRIP = 3'b010 (SPI only)	1.27	1.41	1.55	V
		ITRIP = 3'b011 (SPI only)	1.49	1.65	1.82	V
		ITRIP = 3'b100 or LVL3	1.78	1.98	2.18	V
		ITRIP = 3'b101 or LVL4	2.08	2.31	2.54	V
		ITRIP = 3'b110 or LVL5	2.38	2.64	2.9	V
		ITRIP = 3'b111 or LVL6	2.67	2.97	3.27	V
t_{OFF}	ITRIP regulation - off time	TOFF = 2'b00 (SPI only)	16	20	25	µs
		TOFF = 2'b01 (SPI). Only choice for HW	24	30	36	µs
		TOFF = 2'b10 (SPI only)	33	40	48	µs
		TOFF = 2'b11 (SPI only)	41	50	61	µs

7.5.9 Over Current Protection (OCP)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OCP_HS}	Over current protection threshold on the high side	OCP_SEL = 2'b00 (SPI), Only choice for HW	12		24	A
		OCP_SEL = 2'b10 (SPI only)	9		18	A
		OCP_SEL = 2'b01 (SPI only)	6		14	A
I_{OCP_LS}	Over current protection threshold on the low side	OCP_SEL = 2'b00 (SPI), Only choice for HW	12		24	A
		OCP_SEL = 2'b10 (SPI only)	9		18	A
		OCP_SEL = 2'b01 (SPI only)	6		14	A
t_{OCP}	Over current protection deglitch time	TOCP_SEL = 2'b00 (SPI), Only choice for HW	4.5	6	7.3	µs
	Over current protection deglitch time	TOCP_SEL = 2'b01 (SPI only)	2.2	3	4.1	µs
	Over current protection deglitch time	TOCP_SEL = 2'b10 (SPI only)	1.1	1.5	2.3	µs
	Over current protection deglitch time	TOCP_SEL = 2'b11 (SPI only)	0.15	0.2	0.4	µs

7.5.10 Over Temperature Protection (TSD)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{TSD}	Thermal shutdown temperature		155	170	185	°C
T_{HYS}	Thermal shutdown hysteresis			30		°C
t_{TSD}	Thermal shutdown deglitch time		10	12	19	µs

7.5.11 Voltage Monitoring

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VMOV}	VM over voltage threshold while rising	VMOV_SEL = 2'b00 (SPI), Only choice in HW variant	33.6		37	V
		VMOV_SEL = 2'b01 (SPI only)	28		31	V
		VMOV_SEL = 2'b10 (SPI only)	18		21	V
V_{VMOV_HYS}	VM over voltage hysteresis			0.6		V
t_{VMOV}	VM over voltage deglitch time		10	12	19	µs
V_{VMUV}	VM under voltage threshold while falling		4.2		4.5	V
V_{VMUV_HYS}	VM under voltage hysteresis			200		mV
t_{VMUV}	VM under voltage deglitch time		8	12	19	µs
VM_{POR_FALL}	VM voltage at which device goes into POR	Applicable for HW & SPI (S) variant			3.6	V
VM_{POR_RISE}	VM voltage at which device comes out of POR	Applicable for HW & SPI (S) variant			3.9	V
VDD_{POR_FALL}	VDD voltage at which device goes into POR	Applicable for SPI (P) variant			3.5	V
VDD_{POR_RISE}	VDD voltage at which device comes out of POR	Applicable for SPI (P) variant			3.8	V

7.5.12 Load Monitoring

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Off-state diagnostics (OLP)						
R_{S_GND}	Resistance on OUT to GND that will be detected as short, All modes				1	KΩ
R_{S_VM}	Resistance on OUT to VM that will be detected as short , All modes				1	KΩ
R_{OPEN_FB}	Resistance between OUTx that will be detected as open, PH/EN or PWM mode		1.5			KΩ
R_{OPEN_LS}	Resistance on OUT to GND that will be detected as open , Independent mode	Valid for low-side load	2			KΩ
R_{OPEN_HS}	Resistance on OUT to VM that will be detected as open, Independent mode	Valid for high-side load, V_{VM} = 13.5 V	10			KΩ
V_{OLP_REFH}	OLP Comparator Reference High			2.65		V
V_{OLP_REFL}	OLP Comparator Reference Low			2		V
R_{OLP_PU}	Internal pull-up resistance on OUT to VDD during OLP	$V_{OUTx} = V_{OLP\_REFH} + 0.1V$		1		KΩ
R_{OLP_PD}	Internal pull-down resistance on OUT to GND during OLP	$V_{OUTx} = V_{OLP\_REFL} - 0.1V$		1		KΩ
SPI variant only - On-state diagnostics (OLA)						
I_{PD_OLA}	Internal sink current on OUTx to GND during dead-time in high-side recirculation	SR = 3'b000 or 3'b001 or 3'b010 or 3'b111 or LVL2 or LVL5	2.5		5	mA
		SR = 3'b011 or LVL3	0.8		2	mA
		SR = 3'b100 or LVL4	1.2		2.5	mA
		SR = 3'b101 or LVL1	1.5		3	mA
		SR = 3'b110 or LVL6	2.2		4	mA

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OLA_REF}	Comparator Reference with respect to VM used for OLA			0.25		V

7.5.13 Fault Retry Setting

Refer to retry setting waveform

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RETRY}	Automatic driver retry time	Fault reaction set to RETRY	4.1	5	6.1	ms
t_{CLEAR}	Fault free operation time to auto-clear from over current event	Fault reaction set to RETRY	85		200	µs
t_{CLEAR_TSD}	Fault free operation time to auto-clear from over temperature event	Fault reaction set to RETRY	4.2		6.7	ms

7.5.14 Transient Thermal Impedance & Current Capability

Information based on thermal simulations

Table 7-1. Transient Thermal Impedance ($R_{\theta JA}$) and Current Capability - full-bridge

PART NUMBER	PACKAGE	$R_{\theta JA}$ [°C/W](1)				Current [A](2)					
						without PWM(3)				with PWM(4)	
		0.1 sec	1 sec	10 sec	DC	0.1 sec	1 sec	10 sec	DC	10 sec	DC
DRV8243-Q1	VQFN-HR	7.3	13	17.5	34.2	7.5	5.6	4.8	3.5	4.4	3.0
DRV8243-Q1	HVSSOP	5.8	10.5	15.3	32.4	7.8	5.8	4.8	3.3	4.4	2.9

(1) Based on thermal simulations using 40 mm x 40 mm x 1.6 mm 4 layer PCB – 2 oz Cu on top and bottom layers, 1 oz Cu on internal planes with 0.3 mm thermal via drill diameter, 0.025 mm Cu plating, 1 minimum mm via pitch.
(2) Estimated transient current capability at 85 °C ambient temperature for junction temperature rise up to 150°C
(3) Only conduction losses (I^2R) considered
(4) Switching loss roughly estimated by the following equation:

$$P_{SW} = V_{VM} \times I_{Load} \times f_{PWM} \times V_{VM}/SR, \text{ where } V_{VM} = 13.5\ V,\ f_{PWM} = 20\ KHz,\ SR = 23\ V/\mu s \quad (1)$$

7.6 SPI Timing Requirements

		MIN	TYP	MAX	UNIT
t_{SCLK}	SCLK minimum period(1)	100			ns
t_{SCLKH}	SCLK minimum high time	50			ns
t_{SCLKL}	SCLK minimum low time	50			ns
t_{HI_nSCS}	nSCS minimum high time	300			ns
t_{SU_nSCS}	nSCS input setup time	25			ns
t_{H_nSCS}	nSCS input hold time	25			ns
t_{SU_SDI}	SDI input data setup time	25			ns
t_{H_SDI}	SDI input data hold time	25			ns
t_{EN_SDO}	SDO enable delay time(1)			35	ns
t_{DIS_SDO}	SDO disable delay time(1)			100	ns

(1) SPI (S) variant: SDO delay times are valid only with SDO external load of 5 pF. With a 20 pF load on SDO, there is an additional delay on SDO, which results in a 25% increase in SCLK minimum time, limiting the SCLK to a maximum of 8 MHz. There is NO such limitation for the SPI (P) variant.

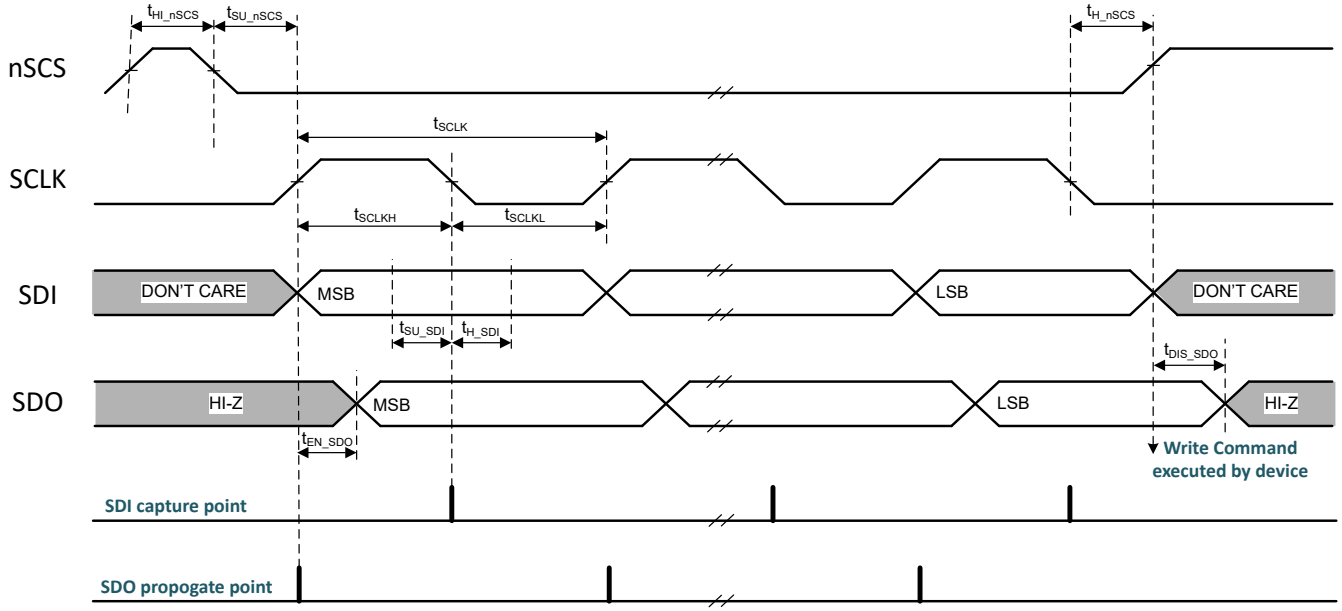

Figure 7-1. SPI Peripheral-Mode Timing Definition

7.7 Switching Waveforms

This section illustrates the switching transients for an inductive load due to external PWM or internal ITRIP regulation.

7.7.1.1 High-Side Recirculation

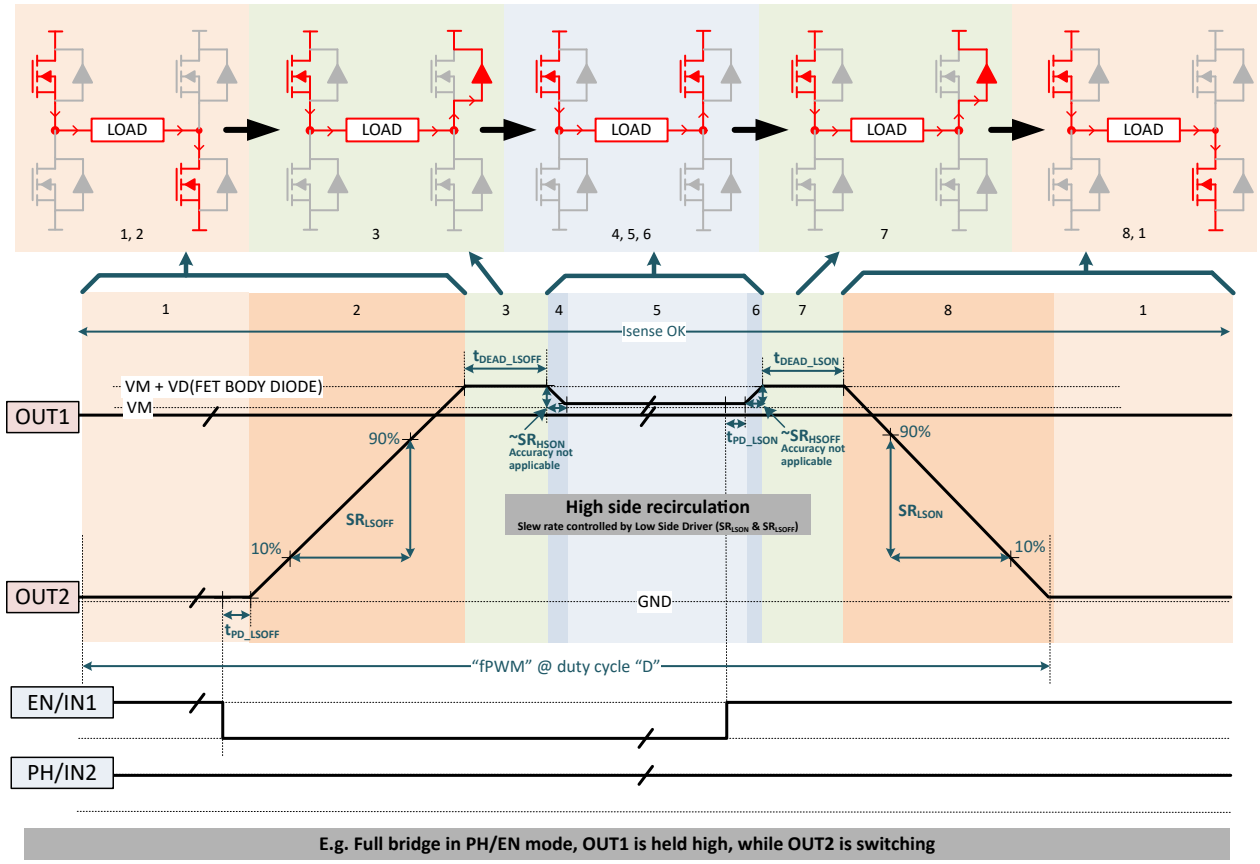

Figure 7-2. Output Switching Transients for a H-Bridge with High-Side Recirculation

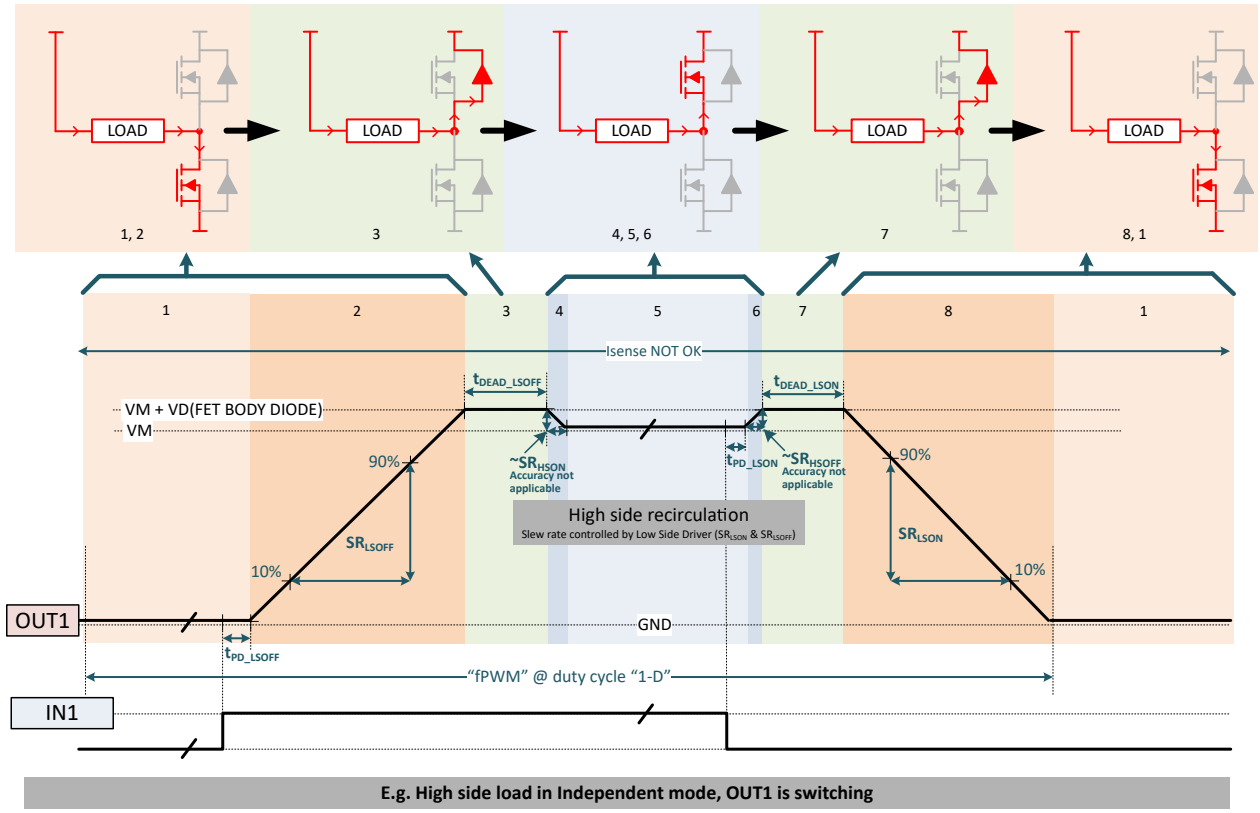

Figure 7-3. Output Switching Transients for a Half-Bridge with High-Side Recirculation

7.7.1.2 Low-Side Recirculation

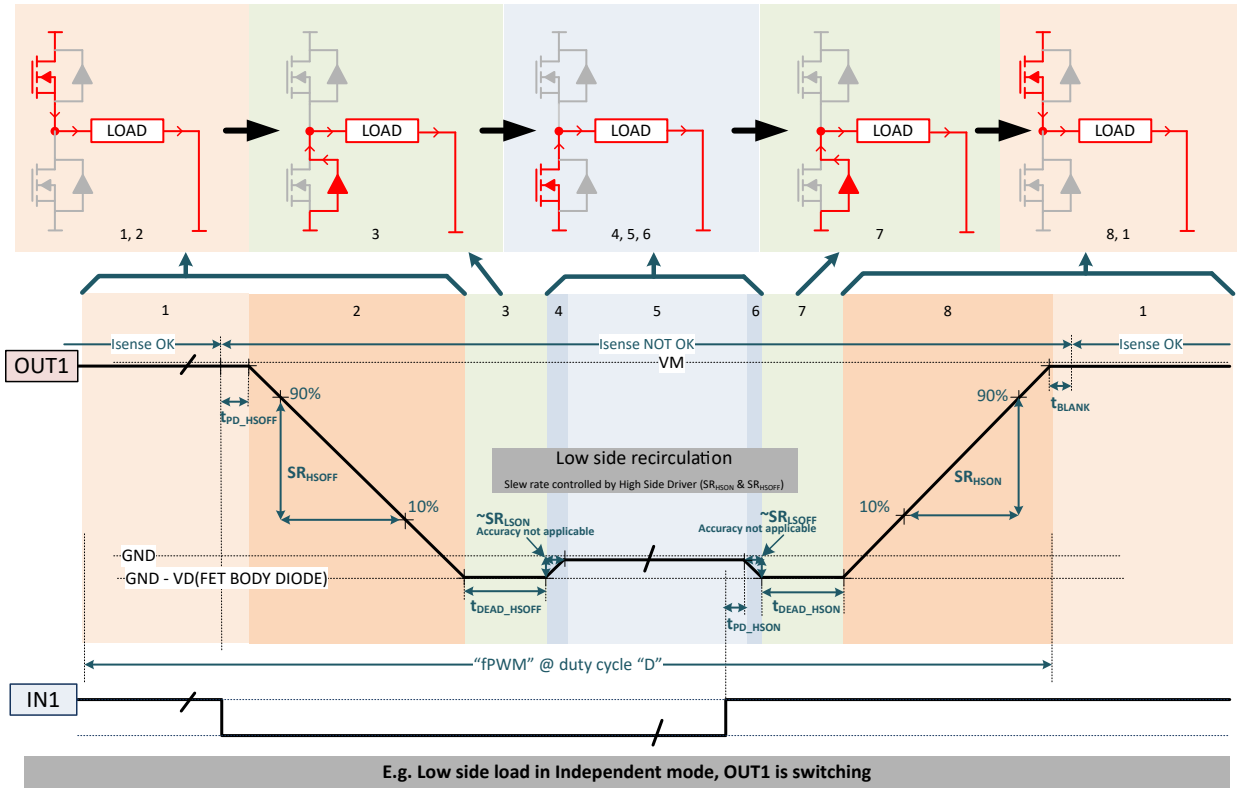

Figure 7-4. Output Switching Transients for a half-bridge with Low-Side Recirculation

7.7.2 Wake-up Transients

7.7.2.1 HW Variant

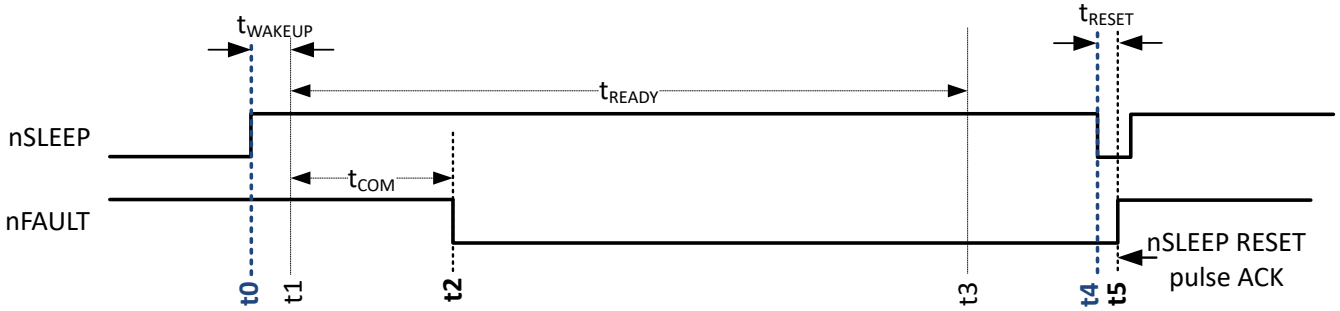

Figure 7-5. Wake-up from SLEEP State to STANDBY State Transition for HW Variant

Hand shake between controller and device during wake-up as follows:

- t0: Controller - nSLEEP asserted high to initiate device wake-up
- t1: Device internal state - Wake-up command registered by device (end of Sleep state)
- t2: Device – nFAULT asserted low to acknowledge wake-up and indicate device ready for communication
- t3: Device internal state - Initialization complete
- t4 (any time after t2): **Controller – Issue nSLEEP reset pulse** to acknowledge device wake-up
- t5: Device - nFAULT de-asserted as an acknowledgment of nSLEEP reset pulse. Device in STANDBY state

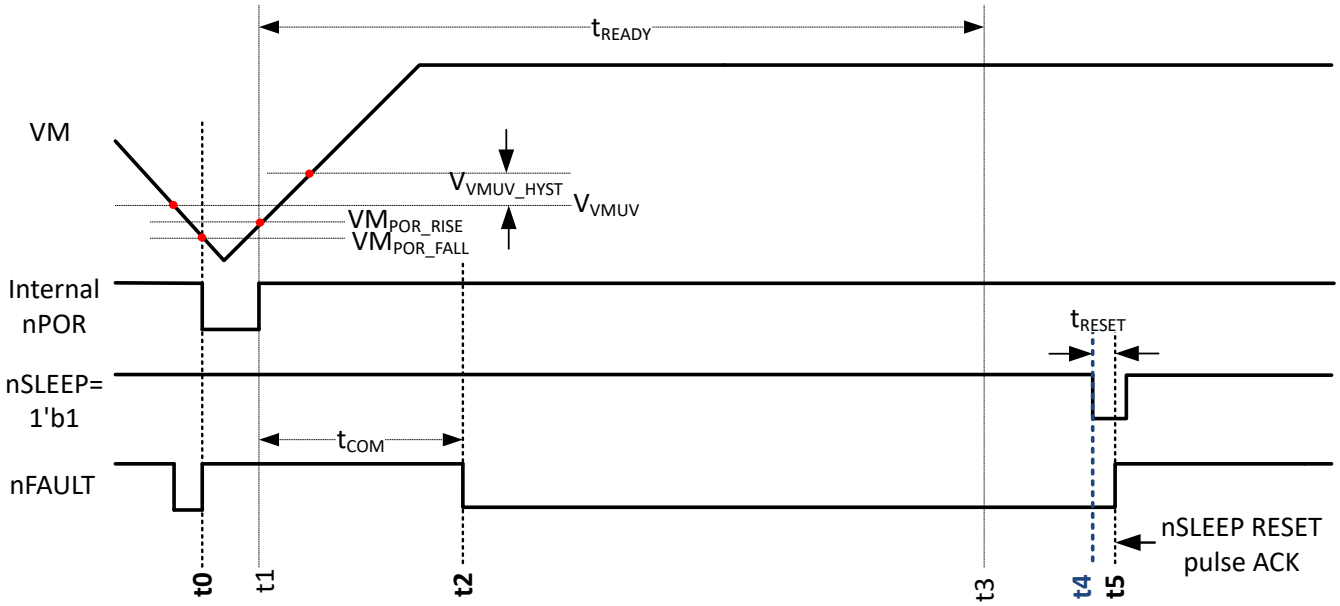

Figure 7-6. Power-up to STANDBY State Transition for HW Variant

Hand shake between controller and device during power-up as follows:

- t0: Device internal state - POR asserted based on under voltage of internal LDO (VM dependent)
- t1: Device internal state – POR de-asserted based on recovery of internal LDO voltage
- t2: Device – nFAULT asserted low to acknowledge wake-up and indicate device ready for communication
- t3: Device internal state - Initialization complete
- t4 (any time after t2): **Controller – Issue nSLEEP reset pulse** to acknowledge device power-up
- t5: Device - nFAULT de-asserted as an acknowledgment of nSLEEP reset pulse. Device in STANDBY state

7.7.2.2 SPI Variant

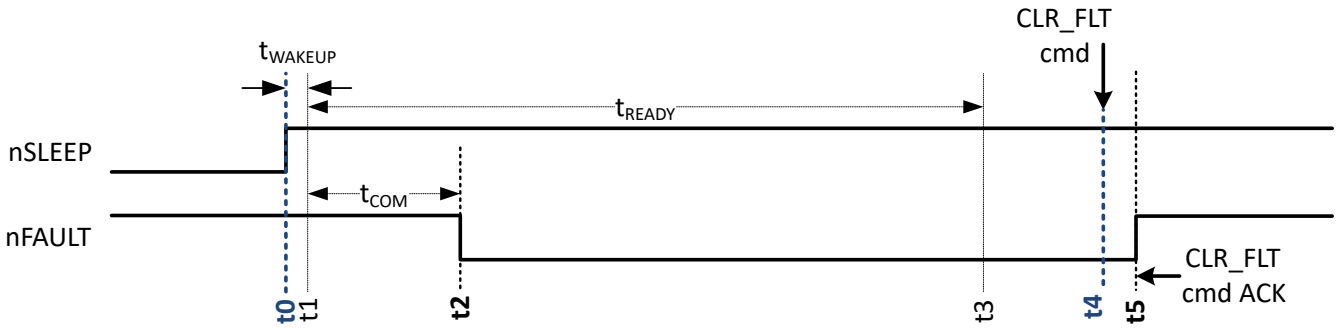

Figure 7-7. Wake-up from SLEEP State to STANDBY State Transition for SPI (S) Variant

Hand shake between controller and device during a wake-up transient as follows:

- t0: Controller - nSLEEP asserted high to initiate device wake-up
- t1: Device internal state - Wake-up command registered by device (end of Sleep state)
- t2: Device – nFAULT asserted low to acknowledge wake-up and indicate device ready for communication
- t3: Device internal state - Initialization complete
- t4 (Any time after t2): **Controller – Issue CLR_FLT command** through SPI to acknowledge device wake-up
- t5: Device - nFAULT de-asserted as an acknowledgment of nSLEEP reset pulse. Device in STANDBY state

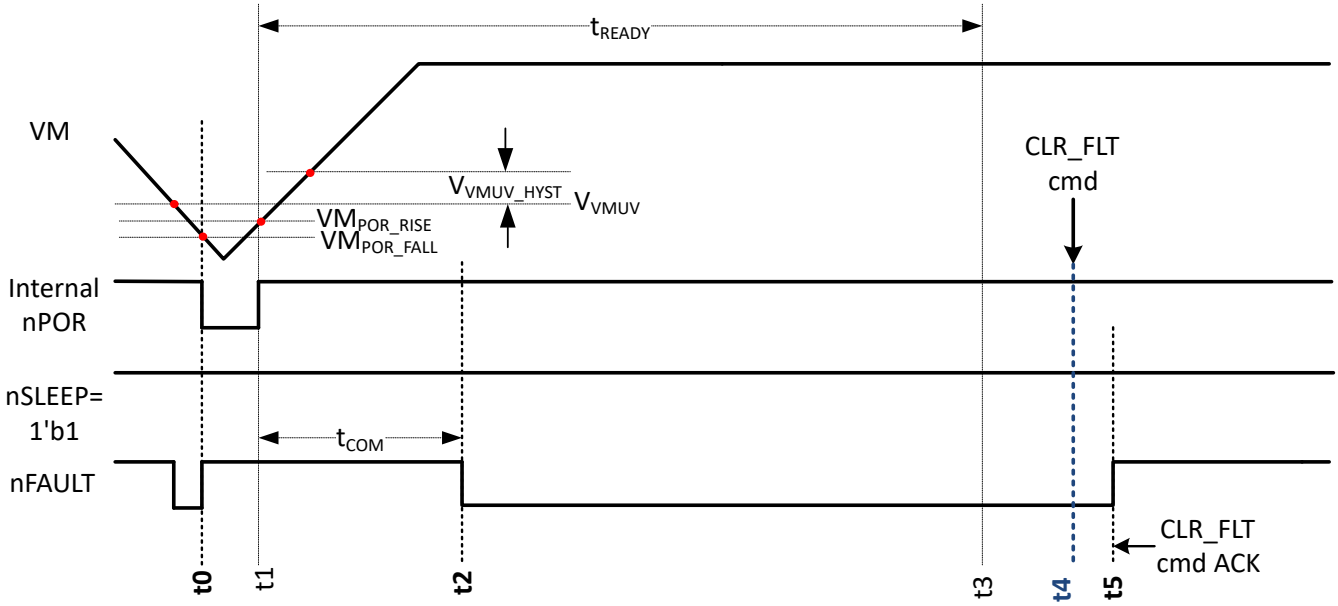

Figure 7-8. Power-up to STANDBY State Transition for SPI (S) Variant

Hand shake between controller and device during power-up as follows:

- t0: Device internal state - POR asserted based on under voltage of internal LDO (VM dependent)
- t1: Device internal state – POR de-asserted based on recovery of internal LDO voltage
- t2: Device – nFAULT asserted low to acknowledge wake-up and indicate device ready for communication
- t3: Device internal state - Initialization complete
- t4 (Any time after t2): **Controller – Issue CLR_FLT command** through SPI to acknowledge device power-up
- t5: Device - nFAULT de-asserted as an acknowledgment of nSLEEP reset pulse. Device in STANDBY state

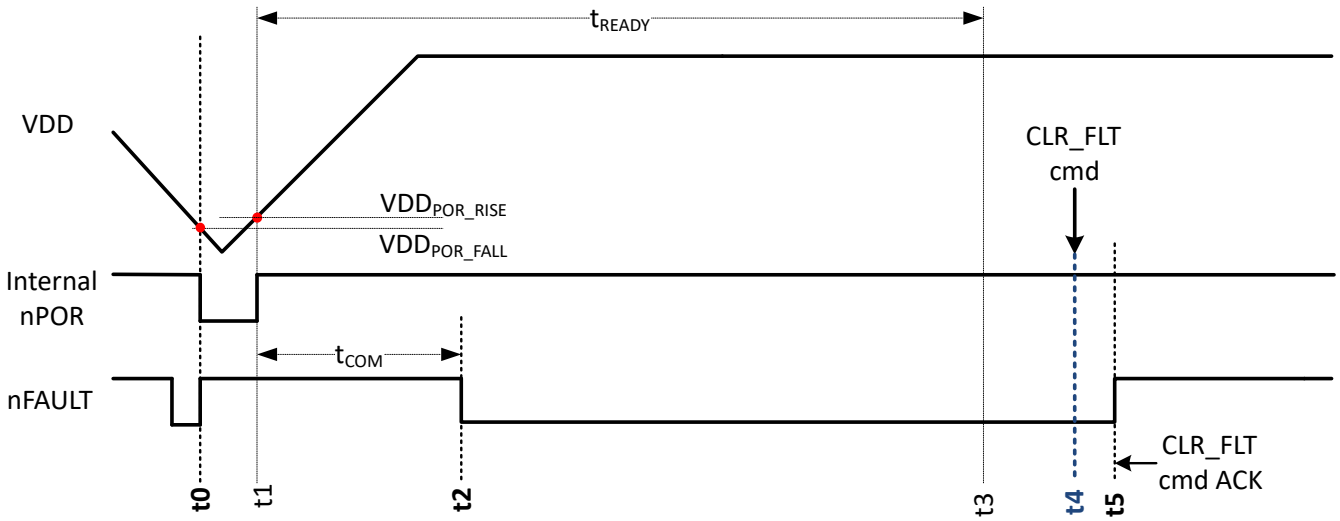

Figure 7-9. Power-up to STANDBY State Transition for SPI (P) Variant

Hand shake between controller and device during power-up as follows:

- t0: Device internal state - POR asserted based on under voltage on VDD (external supply)
- t1: Device internal state – POR de-asserted based on recovery of voltage on VDD (external supply)
- t2: Device – nFAULT asserted low to acknowledge wake-up and indicate device ready for communication
- t3: Device internal state - Initialization complete
- t4 (Any time after t2): **Controller – Issue CLR_FLT command** through SPI to acknowledge device power-up
- t5: Device - nFAULT de-asserted as an acknowledgment of nSLEEP reset pulse. Device in STANDBY state

7.7.3 Fault Reaction Transients

7.7.3.1 Retry setting

Valid for both SPI and HW variants

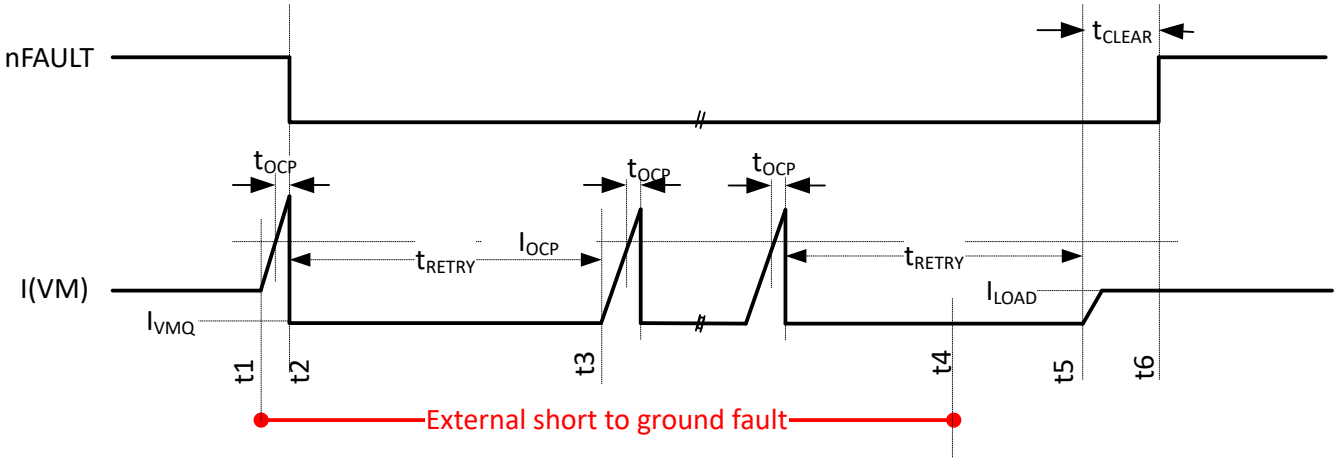

Figure 7-10. Fault reaction with RETRY setting (shown for OCP occurrence on high-side when OUT is shorted to ground)

Short occurrence and recovery scenario with RETRY setting:

- t1: An external short occurs.
- t2: OCP (Over Current Protection) fault confirmed after t_{OCP}, output disabled, nFAULT asserted low to indicate fault.
- t3: Device automatically attempts retry (auto retry) after t_{RETRY}. Each time output is briefly turned on to confirm short occurrence and then immediately disabled after t_{OCP}. nFAULT remains asserted low through out. Cycle repeats till driver is disabled by the user or external short is removed, as illustrated further. Note that, in case of a TSD (Thermal Shut Down) event, automatic retry time depends on the cool off based on thermal hysteresis.
- t4: The external short is removed.
- t5: Device attempts auto retry. But this time, no fault occurs and device continues to keep the output enabled.
- t6: After a fault free operation for a period of t_{CLEAR} is confirmed, nFAULT is de-asserted.
- SPI variant only – Fault status remains latched till a CLR_FLT command is issued.

Note that, in the event of an output short to ground causing the high-side OCP fault detection, IPROPI pin will continue to be pulled up to V_{IPROPI_LIM} voltage to indicate this type of short, while the output is disabled. This is especially useful for the HW (H) variant to differentiate the indication of a short to ground fault from the other faults.

7.7.3.2 Latch setting

Valid for both SPI and HW variants

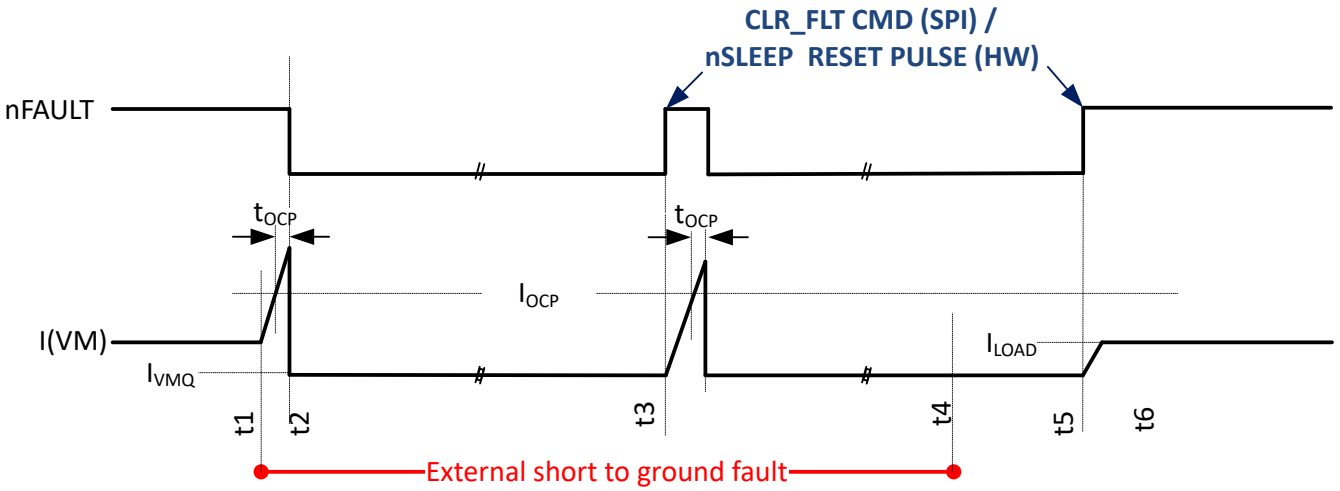

Figure 7-11. Fault reaction with Latch setting (shown for OCP occurrence on high-side when OUT is shorted to ground)

Short occurrence and recovery scenario with LATCH setting:

- t1: An external short occurs.
- t2: OCP (Over Current Protection) fault confirmed after t_{OCP}, output disabled, nFAULT asserted low to indicate fault.
- t3: A CLR_FLT command (SPI variant) or nSLEEP RESET Pulse (HW variant) issued by controller. nFAULT is de-asserted and output is enabled. OCP fault is detected again and output is disabled with nFAULT asserted low.
- t4: The external short is removed.
- t5: A CLR_FLT command (SPI variant) or nSLEEP RESET Pulse (HW variant) issued by controller. nFAULT is de-asserted and output is enabled. Normal operation resumes.
- SPI variant only – Fault status remains latched till a CLR_FLT command is issued.

Note that, in the event of an output short to ground causing the high-side OCP fault detection, IPROPI pin will continue to be pulled up to V_{IPROPI_LIM} voltage to indicate this type of short, while the output is disabled. This is especially useful for the HW (H) variant to differentiate the indication of a short to ground fault from the other faults.

7.8 Typical Characteristics

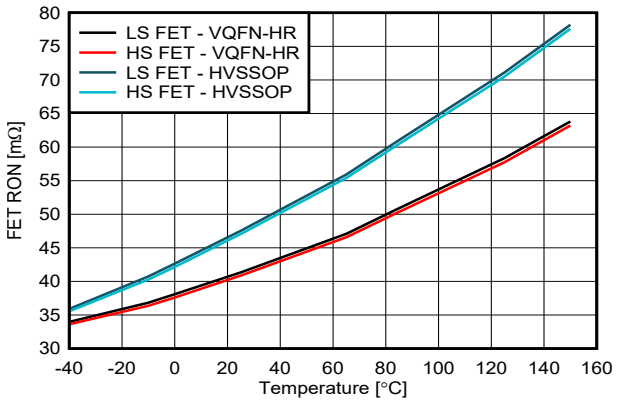

Figure 7-12. R_{HS_ON} & R_{LS_ON} vs Temperature at V_{VM} = 13.5 V

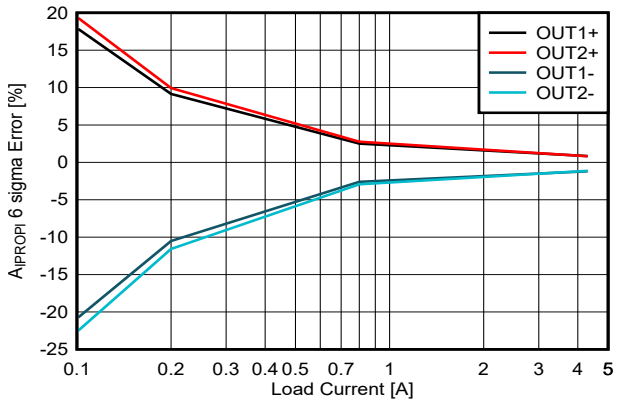

Figure 7-13. A_{IPROPI} Gain Error vs Load Current at V_{VM} = 13.5 V

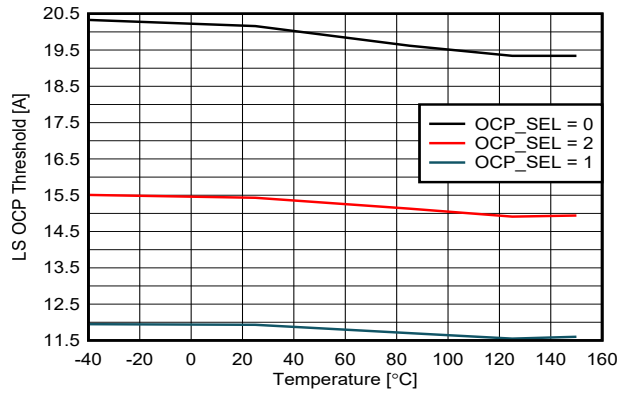

Figure 7-14. LS OCP Threshold vs Temperature at V_{VM} = 13.5 V

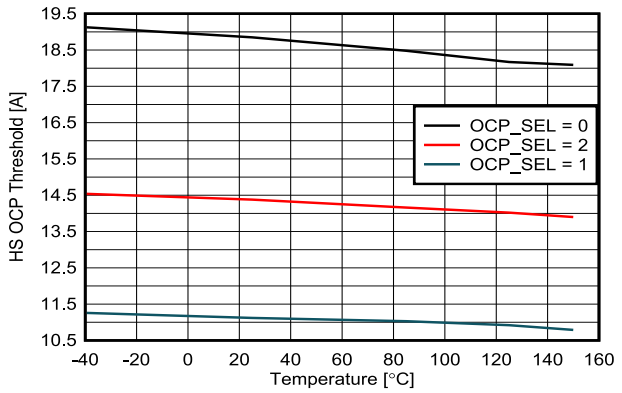

Figure 7-15. HS OCP Threshold vs Temperature at V_{VM} = 13.5 V

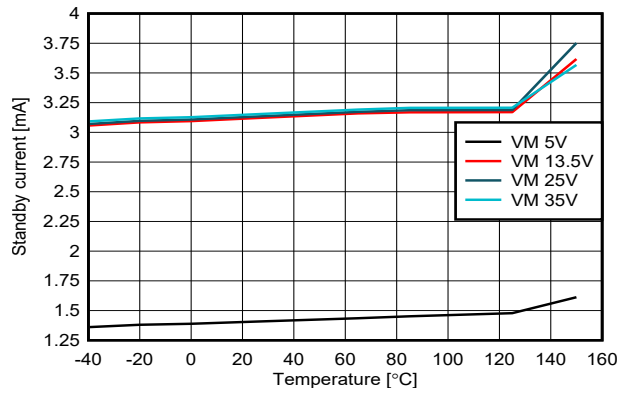

Figure 7-16. Current on VM in STANDBY state vs Temperature

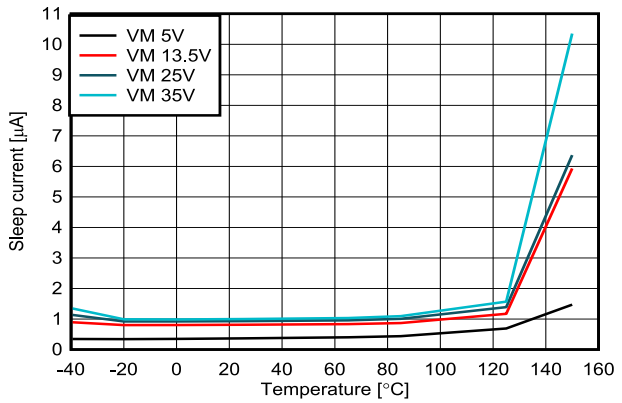

Figure 7-17. Current on VM in SLEEP state vs Temperature

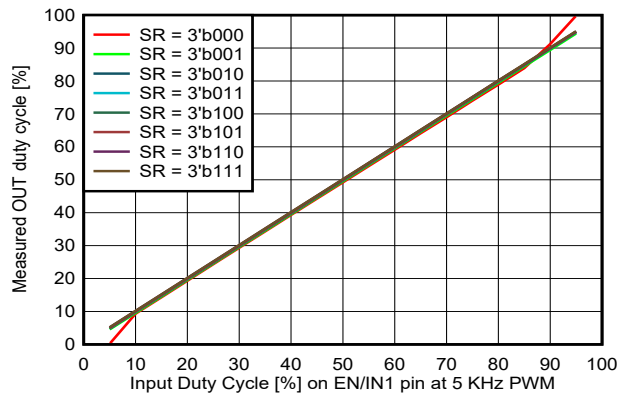

Figure 7-18. Measured Duty Cycle vs Input Duty Cycle at PWM frequency of 5 KHz at V_{VM} = 13.5 V for HS recirculation

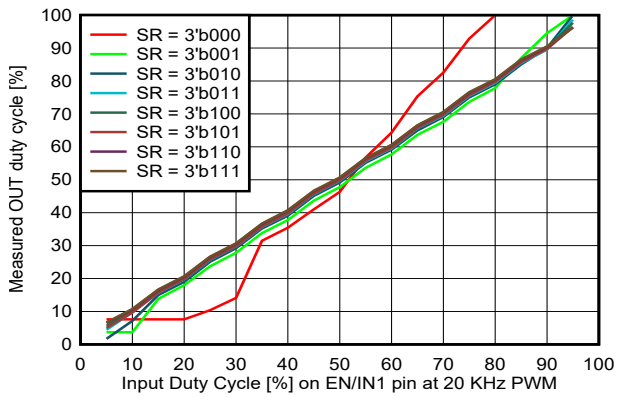

Figure 7-19. Measured Duty Cycle vs Input Duty Cycle at PWM frequency of 20 KHz at V_{VM} = 13.5 V for HS recirculation

8 Detailed Description

8.1 Overview

The DRV824x-Q1 family of devices are brushed DC motor drivers that operate from 4.5 to 35-V supporting a wide range of output load currents for various types of motors and loads. The devices integrate an H-bridge output power stage that can be operated in different control modes set by the MODE function. This allows for driving a single bidirectional brushed DC motor or two unidirectional brushed DC motors. The devices integrate a charge pump regulator to support efficient high-side N-channel MOSFETs with 100% duty cycle operation. The devices operate from a single power supply input (VM) which can be directly connected to a battery or DC voltage supply. The devices also provide a low power mode to minimize current draw during system inactivity.

The devices are available in two interface variants -

1. HW variant - Hardwired interface variant is available for easy device configuration. Due to the limited number of available pins in the device, this variant offers fewer configuration and fault reporting capability compared to the SPI variant.
2. SPI variant - A standard 4-wire serial peripheral interface (SPI) with daisy chain capability allows flexible device configuration and detailed fault reporting to an external controller. The feature differences of the SPI and HW variants can be found in the device comparison section. The SPI interface is available in two device variant choices, as stated below:
   a. SPI (S) variant - The power supply for the digital block is provided by an internal LDO regulator sourced from VM supply. The nSLEEP pin is a high impedance input pin.
   b. SPI (P) variant - This allows for an external supply input to the digital block of the device through a VDD pin. The nSLEEP pin is replaced by this VDD supply pin. This prevents device reset (brown out) during a VM under voltage condition.

The DRV824x family of devices provide a load current sense output using current mirrors on the high-side power MOSFETs. The IPROPI pin sources a small current that is proportional to the current in the high-side MOSFETs (current sourced out of the OUTx pin). This current can be converted to a proportional voltage using an external resistor (R_{IPROPI}). Additionally, the devices also support a fixed off-time PWM chopping scheme for limiting current to the load. The current regulation level can be configured through the ITRIP function.

A variety of protection features and diagnostic functions are integrated into the device. These include supply voltage monitors (VMOV & VMUV), , off-state (Passive) diagnostics (OLP), on-state (Active) diagnostics (OLA) - SPI variant only, overcurrent protection (OCP) for each power FET and over-temperature shutdown (TSD). Fault conditions are indicated on the nFAULT pin. The SPI variant has additional communication protection features such as frame errors and lock features for configuration register bits and driver control bits.

8.2 Functional Block Diagram

8.2.1 HW Variant

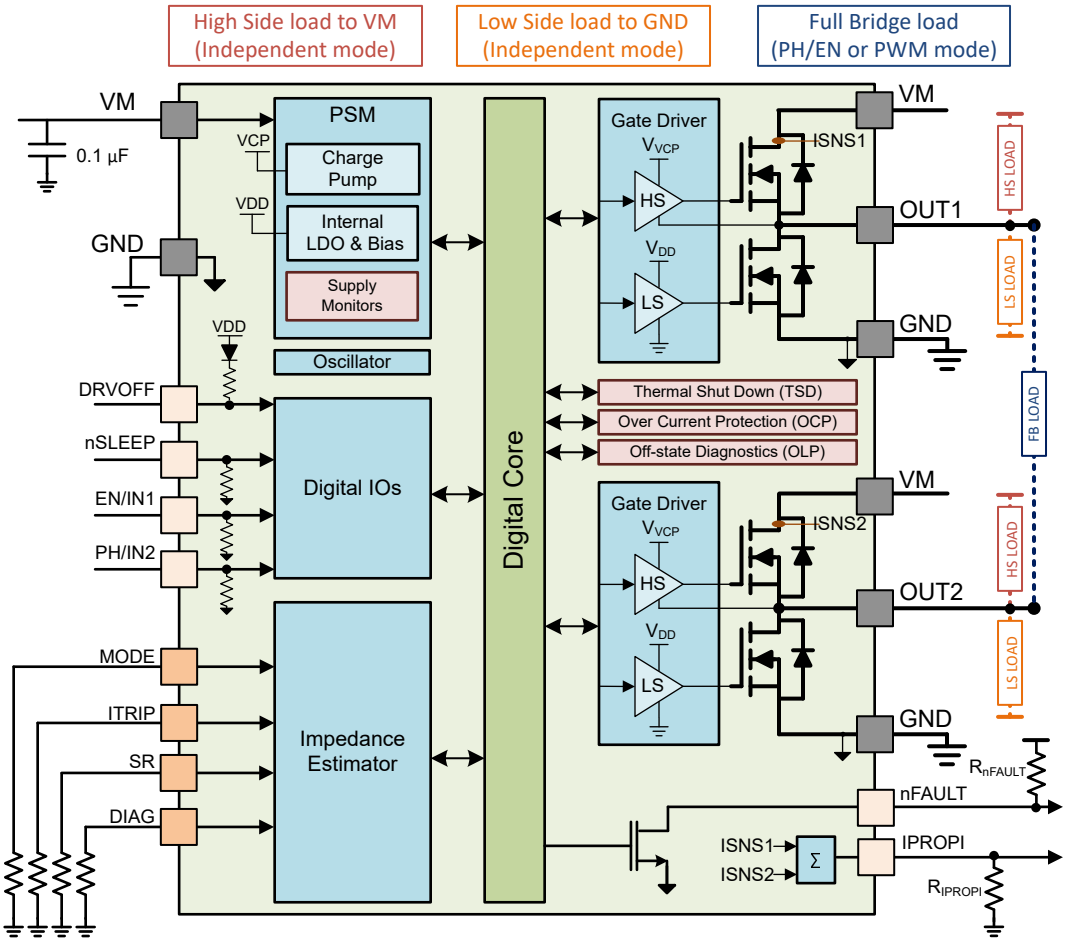

Figure 8-1. Functional Block Diagram - HW Variant

8.2.2 SPI Variant

There are two variants for the SPI interface - SPI (S) variant and SPI (P) variant as shown below.

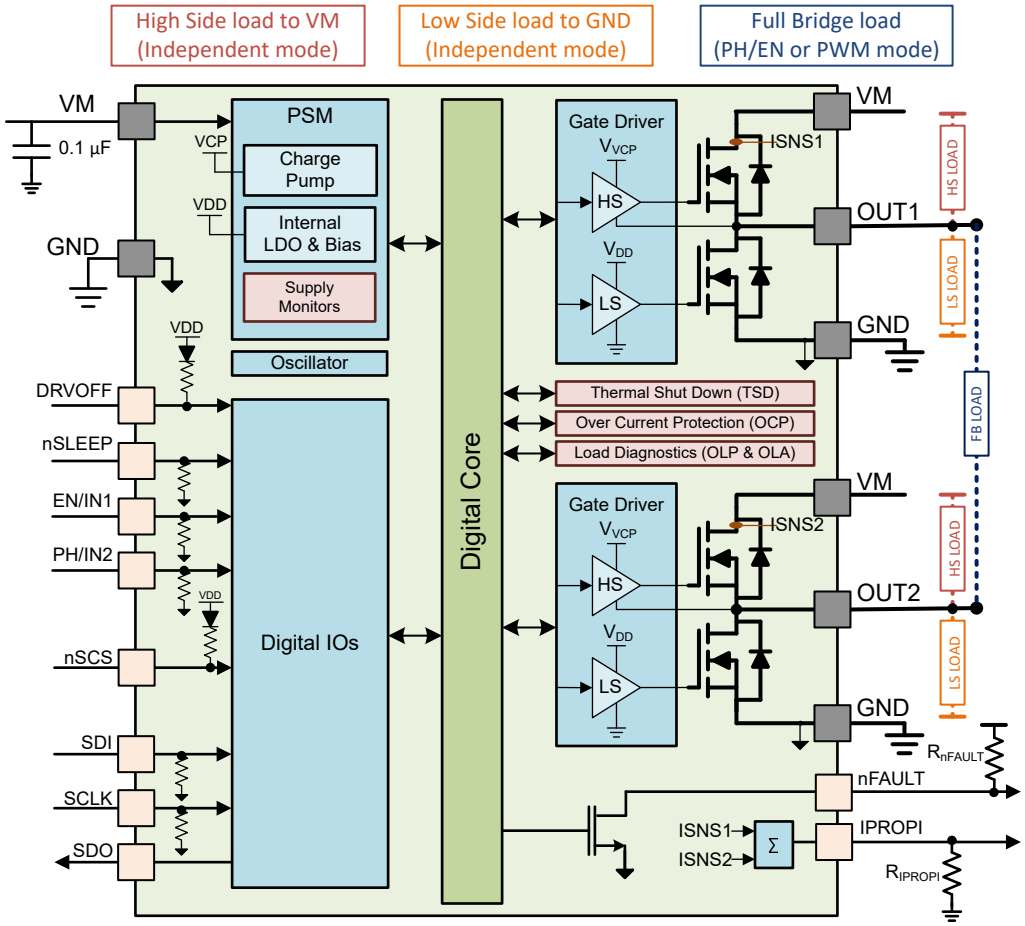

Figure 8-2. Functional Block Diagram - SPI (S) Variant

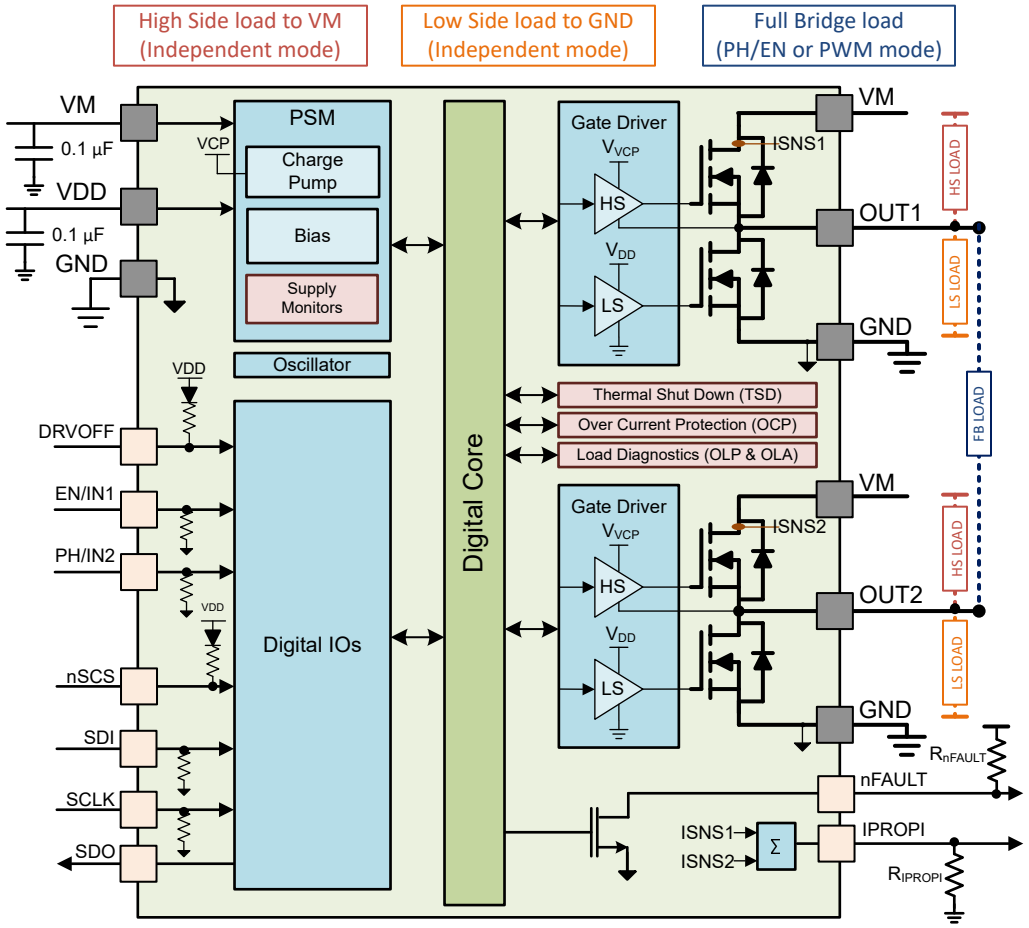

Figure 8-3. Functional Block Diagram - SPI (P) Variant

8.3 Feature Description

8.3.1 External Components

Section 8.3.1.1 and Section 8.3.1.2 contain the recommended external components for the device.

8.3.1.1 HW Variant

Table 8-1. External Components Table for HW Variant

Component	PIN	Recommendation
C_{VM1}	VM	0.1 µF, low ESR ceramic capacitor to GND rated for VM
C_{VM2}	VM	Local bulk capacitor to GND, 10 µF or higher, rated for VM to handle load transients. Refer the section on bulk capacitor sizing.
R_{IPROPI}	IPROPI	Typically 500 - 5000 Ω 0.063 W resistor to GND, depending on the controller ADC dynamic range. Pin can be shorted to GND if ITRIP and IPROPI function is not needed.
C_{IPROPI}	IPROPI	Optional 10 - 100nF, 6.3 V capacitor to GND to slow down the ITRIP regulation loop. Refer Over Current Protection (OCP) section.
R_{nFAULT}	nFAULT	Typically 1KΩ - 10 KΩ, 0.063 W pull-up resistor to controller supply.
R_{MODE}	MODE	Open or short to GND or 0.063 W 10% resistor to GND depending on setting. Refer MODE table.
R_{SR}	SR	Open or short to GND or 0.063 W 10% resistor to GND depending on setting. Refer SR section.
R_{ITRIP}	ITRIP	Open or short to GND or 0.063 W 10% resistor to GND depending on setting. Refer ITRIP table.
R_{DIAG}	DIAG	Open or short to GND or 0.063 W 10% resistor to GND depending on setting. Refer DIAG section.

8.3.1.2 SPI Variant

Table 8-2. External Components Table for SPI Variant

Component	PIN	Recommendation
C_{VM1}	VM	0.1 µF, low ESR ceramic capacitor to GND rated for VM
C_{VM2}	VM	Local bulk capacitor to GND, 10 µF or higher, rated for VM to handle load transients. Refer the section on bulk capacitor sizing.
R_{IPROPI}	IPROPI	Typically 500 - 5000 Ω 0.063 W resistor to GND, depending on the controller ADC dynamic range. Pin can be shorted to GND if ITRIP and IPROPI function is not needed.
C_{IPROPI}	IPROPI	Optional 10 - 100nF, 6.3 V capacitor to GND to slow down the ITRIP regulation loop. Refer Over Current Protection (OCP) section.
R_{nFAULT}	nFAULT	Typically 1KΩ - 10 KΩ, 0.063 W pull-up resistor to controller supply. If nFAULT signaling is not used, this pin can be short to GND or left open.
C_{VDD}	VDD	0.1 µF, 6.3 V, low ESR ceramic capacitor to GND. This is applicable for the SPI (P) variant only.

8.3.2 Bridge Control

The DRV824x-Q1 family of devices provides three separate modes to support different control schemes with the EN/IN1 and PH/IN2 pins. The control mode is selected through the MODE setting. MODE is a 3-level setting based on the MODE pin for the HW variant or S_MODE bits in the CONFIG3 register for the SPI variant as summarized in Table 8-3:

Table 8-3. Mode table

MODE pin	S_MODE bits	Device Mode	Description
$R_{LVL1OF3}$	2'b00	PH/EN mode	full-bridge mode where EN/IN1 is the PWM input, PH/IN2 is the direction input
$R_{LVL2OF3}$	2'b01	Independent mode	Independent control for 2 half-bridges
$R_{LVL3OF3}$	2'b10, 2b'11	PWM mode	full-bridge mode where EN/IN1 and PH/IN2 control the PWM respectively depending on the direction

In the HW variant, MODE pin is latched during device initialization following power-up or wake-up from sleep. Update during operation is blocked.

In the SPI variant of the device, the mode setting can be changed anytime the SPI communication is available by writing to the S_MODE bits. This change is immediately reflected.

The inputs can accept static or pulse-width modulated (PWM) voltage signals for either 100% or PWM drive modes. The device input pins can be powered before VM is applied. By default, the nSLEEP and DRVOFF pins have an internal pull-down and pull-up resistor respectively, to ensure the outputs are Hi-Z if no inputs are present. Both the EN/IN1 and PH/IN2 pins also have internal pull down resistors. The sections below show the truth table for each control mode.

The device automatically generates the optimal dead-time needed during transitioning between the high-side and low-side FET on the switching half-bridge. This timing is based on internal FET gate-source voltage feedback. No external timing is required. This scheme ensures minimum dead time, while guaranteeing no shoot-through current.

Note

1. The SPI variant also provides additional control through the SPI_IN register bits. Refer to - Register - Pin control.
2. For the SPI (P) variant, ignore the nSLEEP column in the control table as there is no nSLEEP pin. Internally, nSLEEP = 1, always. The control table is valid when VDD > VDD_{POR} level.

8.3.2.1 PH/EN mode

In this mode, the two half-bridges are configured to operate as a full-bridge. EN/IN1 is the PWM input and PH/IN2 is the direction input. For load illustration, refer the Load Summary section.

Table 8-4. Control table - PH/EN mode

nSLEEP	DRVOFF	EN/IN1	PH/IN2	OUT1	OUT2	IPROPI	Device State
0	X	X	X	Hi-Z	Hi-Z	No current	SLEEP
1	1	0	0	Hi-Z	Hi-Z	No current	STANDBY
1	1	1	0	Refer Off-state diagnostics table		No current	STANDBY
1	1	0	1				
1	1	1	1				
1	0	0	X	H	H	ISNS1 or ISNS2(1)	ACTIVE
1	0	1	0	L(2)	H	ISNS2	ACTIVE
1	0	1	1	H	L(2)	ISNS1	ACTIVE

(1) Current sourcing out of the device (VM → OUTx → Load)
(2) If internal ITRIP regulation is enabled and ITRIP level is reached, then OUTx is forced "H" for a fixed time

8.3.2.2 PWM mode

In this mode, the two half-bridges are configured to operate as a full-bridge. EN/IN1 provides the PWM input in one direction, while PH/IN2 provides the PWM in the other direction. For load illustration, refer the Load Summary section.

Table 8-5. Control table - PWM mode

nSLEEP	DRVOFF	EN/IN1	PH/IN2	OUT1	OUT2	IPROPI	Device State
0	X	X	X	Hi-Z	Hi-Z	No current	SLEEP
1	1	0	0	Hi-Z	Hi-Z	No current	STANDBY
1	1	1	0	Refer Off-state diagnostics table		No current	STANDBY
1	1	0	1			No current	STANDBY
1	1	1	1			No current	STANDBY
1	0	0	0	H	H	ISNS1 or ISNS2(1)	ACTIVE
1	0	0	1	L(2)	H	ISNS2	ACTIVE
1	0	1	0	H	L(2)	ISNS1	ACTIVE

Table 8-5. Control table - PWM mode (continued)

nSLEEP	DRVOFF	EN/IN1	PH/IN2	OUT1	OUT2	IPROPI	Device State
1	0	1	1	Hi-Z	Hi-Z	No current	STANDBY

(1) Current sourcing out of device (VM → OUTx → Load)
(2) If internal ITRIP regulation is enabled and ITRIP level is reached, then OUTx is forced "H" for a fixed time

For the SPI variant, by setting the PWM_EXTEND bit in the CONFIG2 register, there are additional Hi-Z states that are possible, when a forward ([EN/IN1 PH/IN2] = [1 0]) or reverse ([EN/IN1 PH/IN2] = [0 1]) command is followed by a Hi-Z command ([EN/IN1 PH/IN2] = [1 1]). In this condition of Hi-Z (coasting), only the half-bridge involved with the PWM is Hi-Z, while the HS FET on the other half-bridge is kept ON. The determination on which half-bridge to Hi-Z is made based on the previous cycle. This is summarized in Table 8-6.

Table 8-6. PWM EXTEND table (PWM_EXTEND bit = 1'b1)

PREVIOUS STATE		CURRENT STATE			Device State Transition
OUT1	OUT2	OUT1	OUT2	IPROPI	
Hi-Z	Hi-Z	Hi-Z	Hi-Z	No current	Remains in STANDBY, no change
H	H	Hi-Z	Hi-Z	No current	ACTIVE to STANDBY
L	H	Hi-Z	H	ISNS2	ACTIVE to STANDBY
H	L	H	Hi-Z	ISNS1	ACTIVE to STANDBY

8.3.2.3 Independent mode

In this mode, the two half-bridges are configured to be used as two independent half-bridges. The Table 8-7 shows the logic table for bridge control. For load illustration, refer the Load Summary section.

Table 8-7. Control table - Independent mode

nSLEEP	DRVOFF	EN/IN1	PH/IN2	OUT1	OUT2	IPROPI	Device State
0	X	X	X	Hi-Z	Hi-Z	No current	SLEEP
1	1	0	0	Hi-Z	Hi-Z	No current	STANDBY
1	1	1	0	Refer Off-state diagnostics table		No current	STANDBY
1	1	0	1			No current	STANDBY
1	1	1	1			No current	STANDBY
1	0	0	0	L	L	No current	ACTIVE
1	0	0	1	L	H(2)	ISNS2(1)	ACTIVE
1	0	1	0	H(2)	L	ISNS1(1)	ACTIVE
1	0	1	1	H(2)	H(2)	ISNS1 + ISNS2(1)	ACTIVE

For the SPI variant, it is possible to have independent Hi-Z control of both half-bridges through equivalent bits, S_DRVOFF & S_DRVOFF2 in the SPI_IN register, when the **SPI_IN register has been unlocked**. Table 8-8 shows the logic table for bridge control using the pin & register combined inputs. Refer to - Register - Pin control for details on the combined inputs shown in Table 8-8.

Table 8-8. Control table - Independent mode for SPI variant, when SPI_IN is unlocked

nSLEEP	DRVOFF1 *combined*	DRVOFF2 *combined*	EN_IN1 *combined*	PH_IN2 *combined*	OUT1	OUT2	IPROPI	Device State
0	X	X	X	X	Hi-Z	Hi-Z	No current	SLEEP
1	1	1	0	0	Hi-Z	Hi-Z	No current	STANDBY
1	1	1	1	0	Refer Off-state diagnostics table		No current	STANDBY
1	1	1	0	1			No current	STANDBY
1	1	1	1	1			No current	STANDBY
1	1	0	X	0	Hi-Z	L	No current	ACTIVE
1	1	0	X	1	Hi-Z	H(2)	ISNS2(1)	ACTIVE
1	0	1	0	X	L	Hi-Z	No current	ACTIVE

Table 8-8. Control table - Independent mode for SPI variant, when SPI_IN is unlocked (continued)

nSLEEP	DRVOFF1 *combined*	DRVOFF2 *combined*	EN_IN1 *combined*	PH_IN2 *combined*	OUT1	OUT2	IPROPI	Device State
1	0	1	1	X	H(2)	Hi-Z	ISNS1(1)	ACTIVE
1	0	0	0	0	L	L	No current	ACTIVE
1	0	0	0	1	L	H(2)	ISNS2(1)	ACTIVE
1	0	0	1	0	H(2)	L	ISNS1(1)	ACTIVE
1	0	0	1	1	H(2)	H(2)	ISNS1 + ISNS2(1)	ACTIVE

(1) Current sourcing out of device (VM → OUTx → Load)
(2) If internal ITRIP regulation is enabled and ITRIP level is reached, then OUTx is forced "L" for a fixed time

In this mode, the device behavior is as listed below:

- Load current can be sensed only for current from VM → OUTx → Load. So current sense is not possible for high-side loads
- The current on IPROPI pin is the sum of the high-side sense current from both the half-bridges. This limits the ITRIP current regulation feature as a combined current regulation, rather than as truly independent.
- Slew rate configurability is limited for low-side recirculation (low-side loads)
- Active state open load diagnostics (OLA) is possible only for high-side loads
- For the HW variant, it is NOT possible to have independent Hi-Z control of each half-bridge. Asserting DRVOFF pin high will Hi-Z both the half-bridges.

8.3.2.4 Register - Pin Control - SPI Variant Only

The SPI variant allows control of the bridge through the specific register bits, S_DRVOFF, S_DRVOFF2, S_EN_IN1, S_PH_IN2 in the SPI_IN register, provided the **SPI_IN register has been unlocked**. The user can unlock this register by writing the right combination to the SPI_IN_LOCK bits in the COMMAND register.

Additionally, the user can configure between an AND / OR logic combination of each of external input pin with their equivalent register bit in the SPI_IN register. This logical configuration is done through the equivalent selects bits in the CONFIG4 register:

- DRVOFF_SEL, EN_IN1_SEL and PH_IN2_SEL

The control of the output is similar to the truth tables described in the section before, but with these logically combined inputs. These combined inputs are listed as follows:

- Combined input = Pin input **OR** equivalent SPI_IN register bit, if equivalent CONFIG4 select bit = 1'b0
- Combined input = Pin input **AND** equivalent SPI_IN register bit, if equivalent CONFIG4 select bit = 1'b1
- In Independent mode:
  - DRVOFF2 combined = DRVOFF pin **OR** S_DRVOFF2 bit, if DRVOFF_SEL bit = 1'b0
  - DRVOFF2 combined = DRVOFF pin **AND** S_DRVOFF2 bit, if DRVOFF_SELbit = 1'b1

Note that external nSLEEP pin is still needed for sleep function.

This logical combination offers more configurability to the user as shown in the table below.

Table 8-9. Register - Pin Control Examples

Example	CONFIG4: xxx_SEL Bit	PIN status	SPI_IN Bit Status	Comment
DRVOFF as redundant shutoff	DRVOFF_SEL = 1'b0	DRVOFF active	S_DRVOFF active	Either DRVOFF pin = 1 or S_DRVOFF bit = 1 will shutoff the output
Pin only control	DRVOFF_SEL = 1'b1	DRVOFF active	S_DRVOFF = 1'b1	Only DRVOFF pin function is available
Register only control	PH_IN2_SEL bit = 1'b0	PH/IN2 - short to GND or float	S_PH_IN2 active	PH (direction) will be controlled by the register bit alone

8.3.3 Device Configuration

This section describes the various device configurations to enable the user to configure the device to suit their use case.

8.3.3.1 Slew Rate (SR)

The SR pin (HW variant) or S_SR bits in the CONFIG3 register (SPI variant) determines the voltage slew rate of the driver output. This enables the user to optimize the PWM switching losses while meeting the EM conformance requirements. For the HW variant, SR is a 6-level **setting**, while the SPI variant has 8 settings. For an inductive load, the slew rate control of the device depends on whether the recirculation path is through the high-side path to VM or through the low-side path to GND. Depending on the use-case, refer to the switching parameters table for either high-side recirculation or low-side recirculation in the Electrical Characteristics section for the slew rate range and values.

Note

The SPI variant also offers an **optional** spread spectrum clocking (SSC) feature that spreads the internal oscillator frequency +/- 12% around its mean with a period triangular function of ~1.3 MHz to reduce emissions at higher frequencies. There is **no** spread spectrum clocking (SSC) feature in the HW variant.

In the HW variant, the SR pin is **latched** during device initialization following power-up or wake-up from sleep. Update during operation is blocked.

In the SPI variant, the slew rate setting can be changed at any time when SPI communication is available by writing to the S_SR bits. This change is immediately reflected.

8.3.3.2 IPROPI

The device integrates a current sensing feature with a proportional analog current output on the IPROPI pin that can be used for load current regulation. This eliminates the need of an external sense resistor or sense circuitry reducing system size, cost, and complexity.

The device senses the load current by using a shunt-less high-side current mirror topology. This way the device can only sense an uni-directional high-side current from VM → OUTx → Load through the high-side FET when it is fully turned ON (linear mode). The IPROPI pin outputs an analog current proportional to this sensed current scaled by A_{IPROPI} as follows:

$$I_{IPROPI} = (I_{HS1} + I_{HS2}) / A_{IPROPI}$$

The IPROPI pin must be connected to an external resistor (R_{IPROPI}) to ground in order to generate a proportional voltage V_{IPROPI}. This allows for the load current to be measured as a voltage-drop across the R_{IPROPI} resistor with an analog to digital converter (ADC). The R_{IPROPI} resistor can be sized based on the expected load current in the application so that the full range of the controller ADC is utilized.

The current expressed on IPROPI is the sum of the currents flowing out of the OUTx pins from VM. This implies that:

- In full-bridge operation using PWM or PH/EN mode, the current expressed on IPROPI pin is always from one of the half-bridges that is sourcing the current from VM to the load.
- In independent mode, the current expressed on IPROPI pin could be from either half-bridges or both of them. It is **not** possible to observe only one half-bridge current independently.

8.3.3.3 ITRIP Regulation

The device offers an optional internal load current regulation feature using fixed TOFF time method. This is done by comparing the voltage on the IPROPI pin against a reference voltage determined by ITRIP setting. TOFF time is fixed at 30 µsec for HW variant, while it is configurable between or 20 to 50 µsec for the SPI variant using TOFF_SEL bits in the CONFIG3 register.

The ITRIP regulation, when enabled, comes into action only when the HS FET is enabled and current sensing is possible. In this scenario, when the voltage on the IPROPI pin exceeds the reference voltage set by the ITRIP setting, the internal current regulation loop forces the following action:

- In PH/EN or PWM mode, OUT1 = H, OUT2 = H (high-side recirculation) for the fixed TOFF time
  - Cycle skipping: Due to minimum duty cycle limitations (especially at low slew rate settings and high VM), load current will contiue to increase even with ITRIP regulation. In order to prevent this current walk away, a cycle skipping scheme is implemented, where, if IOUT sensed is still greater than ITRIP at the end of TOFF time, then the recirculation time is extended by an additional TOFF period. This recirculation time addition will continue till IOUT sensed is less than ITRIP at the end of the TOFF period.
- In Independent mode, If OUTx = H, then toggle OUTx = L for the fixed TOFF time, else no action on OUTx

Note

The user inputs always takes **precedence** over the internal control. That means that if the inputs change during the TOFF time, the remainder of the TOFF time is ignored and the outputs will follow the inputs as commanded.

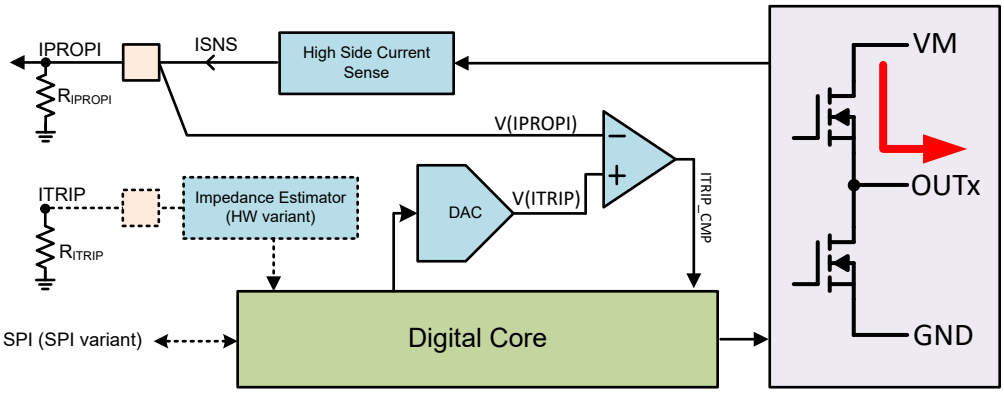

Figure 8-4. ITRIP Implementation

Current limit is set by the following equation:

$$\text{ITRIP regulation level} = (V_{ITRIP} / R_{IPROPI}) \times A_{IPROPI} \quad (2)$$

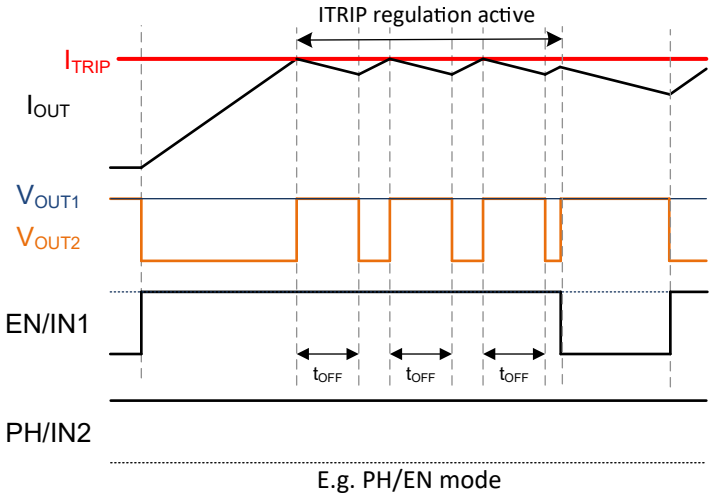

Figure 8-5. Fixed TOFF ITRIP Current Regulation

In Independent mode, since ITRIP regulation is based on summation of the two half-bridge currents on IPROPI pin, it is **not** possible to have completely independent current regulation for the two half-bridges simultaneously.

The ITRIP comparator output (ITRIP_CMP) is ignored during output slewing to avoid false triggering of the comparator output due to current spikes from the load capacitance. Additionally, in the event of transition from low-side recirculation, an additional blanking time t_{BLANK} is needed for the sense loop to stabilize before the ITRIP comparator output is valid.

ITRIP is a 6-level **setting** for the HW variant. The SPI variant offers two more settings. This is summarized in the table below:

Table 8-10. ITRIP Table

ITRIP Pin	S_ITRIP Register Bits	V_{ITRIP} [V]
$R_{LVL1OF6}$	3'b000	Regulation Disabled
$R_{LVL2OF6}$	3'b001	1.18
Not available	3'b010	1.41
Not available	3'b011	1.65
$R_{LVL3OF6}$	3'b100	1.98
$R_{LVL4OF6}$	3'b101	2.31
$R_{LVL5OF6}$	3'b110	2.64
$R_{LVL6OF6}$	3'b111	2.97

In the HW variant of the device, the ITRIP pin changes are **transparent** and changes are reflected immediately.

In the SPI variant of the device, the ITRIP setting can be changed at any time when SPI communication is available by writing to the S_ITRIP bits. This change is immediately reflected in the device behavior.

SPI variant only - If the ITRIP regulation levels are reached, the ITRIP_CMP bit in the STATUS1 register is set. There is no nFAULT pin indication. This bit can be cleared with a CLR_FLT command.

Note

If the application requires a linear ITRIP control with multiple steps beyond the choices provided by the device, an external DAC can be used to force the voltage on the bottom side of the IPROPI resistor, instead of terminating it to GND. With this modification, the ITRIP current can be controlled by the external DAC setting as follows:

$$\text{ITRIP regulation level} = [(V_{ITRIP} - V_{DAC}) / R_{IPROPI}] \text{ X } A_{IPROPI} \quad (3)$$

8.3.3.4 DIAG

The DIAG is a pin (HW variant) or register (SPI variant) setting that is used in both ACTIVE and STANDBY operation of the device, as follows:

- STANDBY state
  - In PH/EN or PWM modes: Enable or disable Off-state diagnostics (OLP).
  - Enable or disable Off-state diagnostics (OLP), as well as select the OLP combinations when enabled. Refer to the tables in the Off-state diagnostics (OLP) section for details on this.
- ACTIVE state
  - Mask ITRIP regulation function if the load type is indicated as high-side load.
  - SPI variant only - Mask active open load detection (OLA) if the load type is indicated as low-side. load
  - HW variant only - Configure fault reaction between retry and latch settings

8.3.3.4.1 HW variant

For the HW variant, the DIAG pin is a 6-level **setting**. Depending on the mode, its configurations are summarized in the table below.

Table 8-11. DIAG table for the HW variant, PH/EN or PWM mode

DIAG pin	STANDBY state	ACTIVE state
	Off-state diagnostics	Fault reaction
$R_{LVL1OF6}$	Disabled	Retry

Table 8-11. DIAG table for the HW variant, PH/EN or PWM mode (continued)

DIAG pin	STANDBY state	ACTIVE state
	Off-state diagnostics	Fault reaction
$R_{LVL5OF6}$	Disabled	Latch
All other levels	Enabled(1)	Latch

Table 8-12. DIAG table for the HW variant, Independent mode

DIAG pin	STANDBY state	ACTIVE state		
	Off-state diagnostics	Load Configuration	Fault reaction	IPROPI / ITRIP
$R_{LVL1OF6}$	Disabled	Low-side load	Retry	Available
$R_{LVL2OF6}$	Enabled(1)	Low-side load	Latch	Available
$R_{LVL3OF6}$	Enabled(1)	High-side load	Latch	Disabled
$R_{LVL4OF6}$	Enabled(1)	High-side load	Retry	Disabled
$R_{LVL5OF6}$	Disabled	Low-side load	Latch	Available
$R_{LVL6OF6}$	Enabled(1)	Low-side load	Retry	Available

(1) Refer to the tables in the Off-state diagnostics (OLP) section for combination details

Note

HW variant only - Option to disable off-state diagnostics for a high-side load use case is not supported. In this case, setting DRVOFF pin high and IN pin low is only way to disable off-state diagnostics.

In the HW variant, the DIAG pin is **latched** during device initialization following power-up or wake-up from sleep. Update during operation is blocked.

8.3.3.4.2 SPI variant

For the SPI variant, S_DIAG is a 2-bit setting in the CONFIG2 register. Depending on the mode, its configurations are summarized in the table below.

Table 8-13. DIAG table for the SPI variant, PH/EN or PWM mode

S_DIAG bits	STANDBY state	ACTIVE state
	Off-state diagnostics	On-state diagnostics
2'b00	Disabled	Available
2'b01, 2'b10, 2'b11	Enabled(1)	Available

Table 8-14. DIAG table for the SPI variant, Independent mode

S_DIAG bits	STANDBY state	ACTIVE state		
	Off-state diagnostics	Load Configuration	On-state diagnostics	IPROPI / ITRIP
2'b00	Disabled	Low-side load	Disabled	Available
2'b01	Enabled(1)	Low-side load	Disabled	Available
2'b10	Disabled	High-side load	Available	Disabled
2'b11	Enabled(1)	High-side load	Available	Disabled

(1) Refer to the tables in the Off-state diagnostics (OLP) section for combination details

In the SPI variant of the device, the settings can be changed anytime when SPI communication is available by writing to the S_DIAG bits. This change is immediately reflected.

8.3.4 Protection and Diagnostics

The driver is protected against over-current and over-temperature events to ensure device robustness. Additionally, the device also offers load monitoring (on-state and off-state), over/ under voltage monitoring on VM pin to signal any unexpected voltage conditions. Fault signaling is done through a low-side open drain nFAULT pin which gets pulled to GND by I_{nFAULT_PD} current on detection of a fault condition. Transition to SLEEP state automatically de-asserts nFAULT.

Note

In the SPI variant, nFAULT pin logic level is the inverted copy of the FAULT bit in the FAULT SUMMARY register. Only exception is when off-state diagnostics are enabled and SPI_IN register is locked (Refer OLP section) .

For the SPI variant, whenever nFAULT is asserted low, the device logs the fault into the FAULT SUMMARY and STATUS registers. These registers can be cleared only by

- CLR FLT command or
- SLEEP command through the nSLEEP pin

It is possible to get all the useful diagnostic information for periodic software monitoring in a single 16 bit SPI frame by:

- Reading the STATUS1 register during ACTIVE state
- Reading the STATUS2 register during STANDBY state

All the diagnosable fault events can be uniquely identified by reading the STATUS registers.

8.3.4.1 Over Current Protection (OCP)

- Device state: ACTIVE
- Mechanism & thresholds: An analog current limit circuit on each MOSFET limits the peak current out of the device even in hard short circuit events. If the output current exceeds the overcurrent threshold, I_{OCP}, for longer than t_{OCP}, then an over current fault is detected.
- Action:
  - nFAULT pin is asserted low
  - Reaction is based on mode selection:
    - PH/EN or PWM mode - Both OUTx is Hi-Z
    - Independent mode - The affected half-bridge OUTx is Hi-Z
  - For a short to GND fault (over current detected on the high-side FET), the IPROPI pin continues to be pulled up to V_{IPROPI_LIM} even if the FET has been disabled. For the HW variant, this helps differentiate a short to GND fault during ACTIVE state from other fault types, as the IPROPI pin is pulled high while the nFAULT pin is asserted low.
- Reaction configurable between latch setting and retry setting based on t_{RETRY} and t_{CLEAR}
- User can add a capacitor in the range of 10 nF to 100 nF on the IPROPI pin to ensure OCP detection in case of a load short condition when internal ITRIP regulation is enabled. This is especially true where there is enough inductance in the short that causes ITRIP regulation to trigger ahead of the OCP detection, resulting in the device missing the short detection. To ensure that OCP detection wins this race condition, a small capacitance added on the IPROPI pin slows down the ITRIP regulation loop enough to allow the OCP detection circuit to work as intended.

The SPI variant offers configurable I_{OCP} levels and t_{OCP} filter times. Refer CONFIG4 register for these settings.

8.3.4.2 Over Temperature Protection (TSD)

- Device state: STANDBY, ACTIVE
- Mechanism & thresholds: The device has several temperature sensors spread around the die. If any of the sensors detect an over temperature event, set by T_{TSD} for a time greater than t_{TSD}, then an over temperature fault is detected.
- Action:
  - nFAULT pin is asserted low

  - Both OUTx is Hi-Z
  - IPROPI pin is Hi-Z
- Reaction configurable between latch setting and retry setting based on T_{HYS} and t_{CLEAR_TSD}

8.3.4.3 Off-State Diagnostics (OLP)

The user can determine the impedance on the OUTx node using off-state diagnostics in the STANDBY state when the power FETs are off. With this diagnostics, it is possible to detect the following fault conditions passively in the STANDBY state:

- Output short to VM or GND < 100 Ω
- Open load > 1K Ω for full-bridge load or low-side load
- Open load > 10K Ω for high-side load, VM = 13.5 V

Note

It is NOT possible to detect a **load short** with this diagnostic. However, the user can deduce this logically if an over current fault (OCP) occurs during ACTIVE operation, but OLP diagnostics do not report any fault in the STANDBY state. Occurrence of both OCP in the ACTIVE state and OLP in the STANDBY state would imply a terminal short (short on OUT node).

- The user can configure the following combinations
  - Internal pull up resistor (R_{OLP_PU}) on OUTx
  - Internal pull down resistor (R_{OLP_PD}) on OUTx
  - Comparator reference level
  - Comparator input selection (OUT1 or OUT2)
- This combination is determined by the controller inputs (pins only for the HW variant) or equivalent bits in the SPI_IN register for the SPI variant if the SPI_IN register has been unlocked.
- HW variant - When off-state diagnostics are enabled, comparator output (OLP_CMP) is available on nFAULT pin.
- SPI variant - The off-state diagnostics comparator output (OLP_CMP) is available on OLP_CMP bit in STATUS2 register. Additionally, if the SPI_IN register has been locked, this comparator output is also available on the nFAULT pin when off-state diagnostics are enabled.
- The user is expected to toggle through all the combinations and record the comparator output after its output is settled.
- Based on the input combinations and comparator output, the user can determine if there is a fault on the output.

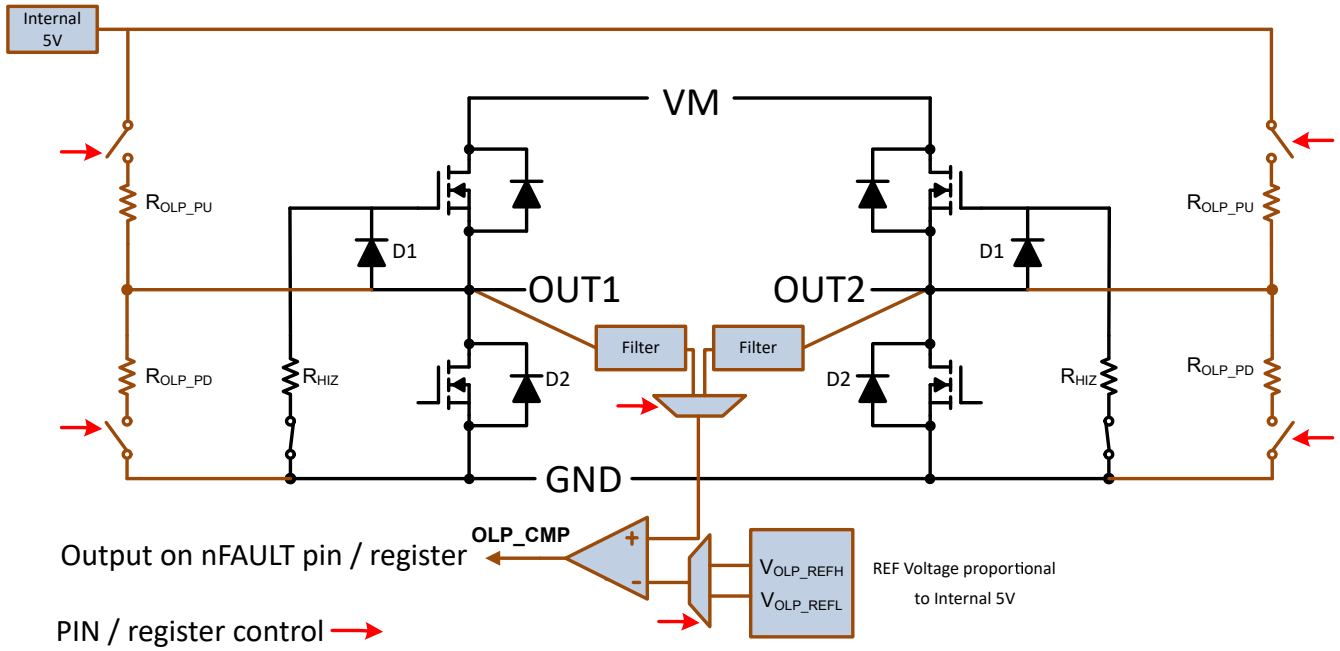

Figure 8-6. Off-State Diagnostics for full-bridge Load (PH/EN or PWM Mode)

The OLP combinations and truth table for a no fault scenario vs. fault scenario for a full-bridge load in PH/EN or PWM modes is shown in Table 8-15.

Table 8-15. Off-State Diagnostics Table - PH/EN or PWM Mode (full-bridge)

User Inputs				OLP Set-Up				OLP CMP Output			
nSLEEP	DRVOFF	EN/IN1	PH/IN2	OUT1	OUT2	CMP REF	Output selected	Normal	Open	GND Short	VM Short
1	1	1	0	R_{OLP_PU}	R_{OLP_PD}	V_{OLP_REFH}	OUT1	L	H	L	H
1	1	0	1	R_{OLP_PU}	R_{OLP_PD}	V_{OLP_REFL}	OUT2	H	L	L	H
1	1	1	1	R_{OLP_PD}	R_{OLP_PU}	V_{OLP_REFL}	OUT2	H	H	L	H

The OLP combinations and truth table for a no fault scenario vs. fault scenario for a low-side load in Independent mode is shown in Table 8-16.

Table 8-16. Off-State Diagnostics Table for Low-Side Load - Independent Mode

User Inputs						OLP Set-Up				OLP_CMP Output		
DIAG pin	S_DIAG bits	nSLEEP	DRVOFF	EN/IN1	PH/IN2	OUT1	OUT2	CMP REF	Output selected	Normal	Open	Short
LVL2, LVL6	2'b01	1	1	1	don't care	R_{OLP_PU}	Hi-Z	V_{OLP_REFH}	OUT1	L	H	H
LVL3, LVL4	2'b11	1	1	1	don't care	R_{OLP_PD}	Hi-Z	V_{OLP_REFL}	OUT1	L	L	H
LVL2, LVL6	2'b01	1	1	0	1	Hi-Z	R_{OLP_PU}	V_{OLP_REFH}	OUT2	L	H	H
LVL3, LVL4	2'b11	1	1	0	1	Hi-Z	R_{OLP_PD}	V_{OLP_REFL}	OUT2	L	L	H

The OLP combinations and truth table for a no fault scenario vs. fault scenario for a high-side load in Independent mode is shown in Table 8-17.

Table 8-17. Off-State Diagnostics Table for High-Side Load - Independent Mode

User Inputs						OLP Set-Up				OLP_CMP Output		
DIAG pin	S_DIAG bits	nSLEEP	DRVOFF	EN/IN1	PH/IN2	OUT1	OUT2	CMP REF	Output selected	Normal	Open	Short
LVL2, LVL6	2'b01	1	1	1	don't care	R_{OLP_PU}	Hi-Z	$V_{OLP\_REF\_H}$	OUT1	**H**	**H**	**L**
LVL3, LVL4	2'b11	1	1	1	don't care	R_{OLP_PD}	Hi-Z	$V_{OLP\_REF\_L}$	OUT1	**H**	**L**	**L**
LVL2, LVL6	2'b01	1	1	0	1	Hi-Z	R_{OLP_PU}	$V_{OLP\_REF\_H}$	OUT2	**H**	**H**	**L**
LVL3, LVL4	2'b11	1	1	0	1	Hi-Z	R_{OLP_PD}	$V_{OLP\_REF\_L}$	OUT2	**H**	**L**	**L**

8.3.4.4 On-State Diagnostics (OLA) - SPI Variant Only

- Device state: ACTIVE - high-side recirculation
- Mechanism and threshold: On-state diagnostics (OLA) can detect an open load detection in the ACTIVE state during high-side recirculation. This includes high-side load connected directly to VM or through a high-side FET on the other half-bridge. During a PWM switching transition, the inductive load current re-circulates into VM through the HS body diode when the LS FET is turned OFF. The device looks for a voltage spike on OUTx above VM during the brief dead time, before the HS FET is turned ON. To observe the voltage spike, this load current needs to be higher than the pull down current (I_{PD_OLA}) on the output asserted by the FET driver. Absence of this voltage spike for "3" consecutive re-circulation switching cycles indicates a loss of load inductance or increase in load resistance and is detected as an OLA fault.
- Action:
  - nFAULT pin is asserted low
  - Output - normal function maintained
  - IPROPI pin - normal function maintained
- Reaction configurable between latch setting and retry setting. In retry setting, OLA fault is automatically cleared with the detection of "3" consecutive voltage spikes during re-circulation switching cycles.

This monitoring is optional and can be disabled.

Note

1. OLA is not supported for low-side loads (low-side recirculation).
2. CLR_FAULT command can clear this fault (recorded in the STATUS1 register) only if the direction commanded is aligned with direction during which the fault was detected.

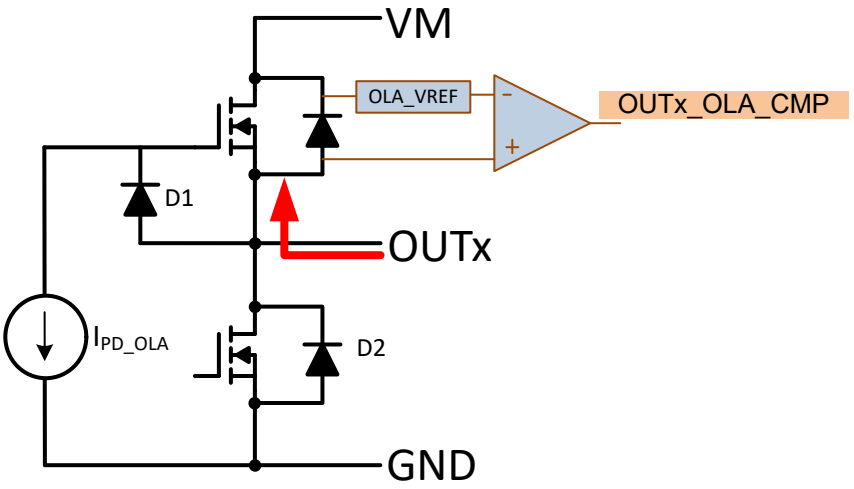

Figure 8-7. On-State Diagnostics

8.3.4.5 VM Over Voltage Monitor

- Device state: STANDBY, ACTIVE
- Mechanism & thresholds: If the supply voltage on the VM pin exceeds the threshold, set by V_{VMOV} for a time greater than t_{VMOV}, then an VM over voltage fault is detected.
- Action:
  - nFAULT pin is asserted low
  - Output - normal function maintained
  - IPROPI pin - normal function maintained
- Reaction configurable between retry and latch setting

In the SPI variant, this monitoring is optional and can be disabled. Also the thresholds are configurable. Refer CONFIG1 register.

8.3.4.6 VM Under Voltage Monitor

- Device state: STANDBY, ACTIVE
- Mechanism & thresholds: If the supply voltage on the VM pin drops below the threshold, set by V_{VMUV} for a time greater than t_{VMUV}, then an VM under voltage fault is detected.
- Action:
  - nFAULT pin is asserted low
  - Both OUTx is Hi-Z
  - IPROPI pin is Hi-Z
- HW and SPI (S) variant: Reaction fixed to retry setting
- Only for SPI (P) variant: Reaction configurable between retry and latch setting
- Note that retry time is only dependent on recovery of VM under voltage condition and is independent of t_{RETRY} / t_{CLEAR} times

8.3.4.7 Power On Reset (POR)

- Device state: ALL
- Mechanism & thresholds: If logic supply drops below VDD_{POR_FALL} for a time greater than t_{POR}, then a power on reset will occur that will hard reset the device.
- Action:
  - nFAULT pin is de-asserted
  - Both OUTx is Hi-Z
  - IPROPI pin is Hi-Z.
  - When this supply recovers above the VDD_{POR_RISE} level, the device will go through a wake-up initialization and nFAULT pin will be asserted low to notify the user on this reset (Refer Wake-up transients).

- HW and SPI (S) variant: These thresholds translate to VM_{POR_FALL} and VM_{POR_RISE} as the logic supply is internally derived from the VM supply
- Only for SPI (P) variant: These thresholds directly map to the VDD pin voltage (VDD_{POR_FALL} and VDD_{POR_RISE})
- Fault reaction: Always retry, retry time depends on the external supply condition to initiate a device wake-up

8.3.4.8 Event Priority

In the ACTIVE state, in a scenario where two or more events occur simultaneously, the device assigns control of the driver based on the following priority table.

Table 8-18. Event Priority Table

Event	Priority
User SLEEP command	1
User input: DRVOFF	2
Over temperature detection (TSD)	3
Over current detection (OCP)(1)	4
VM under voltage detection (VMUV)	5
User input: EN/IN1 and/or PH/IN2	6
Internal PWM control from ITRIP regulation	7
VM over voltage detection (VMOV)(2)	8
On-state fault detection (OLA - SPI variant only)(2)	9

(1) If the device is waiting for an OCP event to be confirmed (waiting for t_{OCP}) when any of events with lower priority than OCP occur, then the device may delay servicing the other events up to a maximum time of t_{OCP} to enable detection of the OCP event.
(2) Priority is "don't care" in this case as this fault event does not cause a change in OUTx

8.4 Device Functional States

The device has three functional states:

- SLEEP
- STANDBY
- ACTIVE

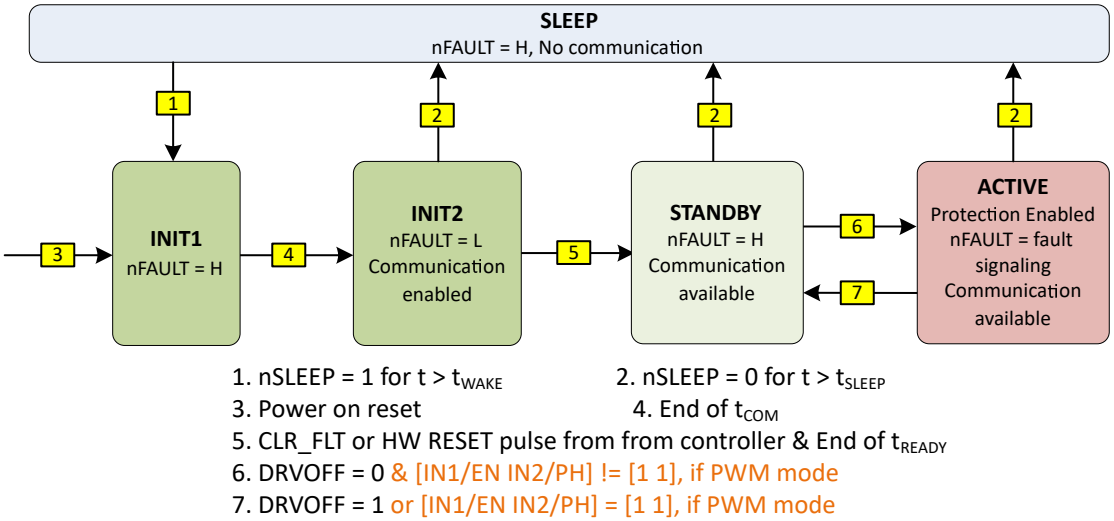

Figure 8-8. Illustrative State Diagram

These states are described in the following section.

8.4.1 SLEEP State

This state occurs when nSLEEP pin is asserted low for a time > t_{SLEEP} or voltage on the VDD pin is < VDD_{POR_FALL}.

This is the deep sleep low power (I_{SLEEP}) state of the device where all functions except a wake-up command are not serviced. The drivers are in Hi-Z. The internal power supply rails (5 V and others) are powered off. nFAULT pin is de-asserted in this state. The device can enter this state from either the STANDBY or the ACTIVE state, when the nSLEEP pin is asserted low for time longer than t_{SLEEP} (HW variant) or for t_{SLEEP_SPI} (SPI (S) variant).

8.4.2 STANDBY State

The device is in this state when nSLEEP pin is asserted high or the voltage on the VDD pin is > VDD_{POR_RISE} with DRVOFF = 1'b0 for all modes and additionally, in PWM mode when both IN1/EN & IN2/PH are 1'b1. In this state, the device is powered up ($I_{STANDBY}$), with the driver Hi-Z and nFAULT de-asserted. The device is ready to transition to ACTIVE state or SLEEP state when commanded so. Off-state diagnostics (OLP), if enabled, are done in this state.

8.4.3 Wake-up to STANDBY State

The device starts transition from SLEEP state to STANDBY state

- if the nSLEEP pin goes high for a duration longer than t_{WAKE}, or
- if VM supply > VM_{POR_RISE} or VDD supply > VDD_{POR_RISE} such that internal POR is released to indicate a power-up.

The device goes through an initialization sequence to load its internal registers and wake-up all the blocks in the following sequence:

- At a certain time, t_{COM} from wake-up, the device is capable of communication. This is indicated by asserting the nFAULT pin low.
- This is followed by the time t_{READY}, when the device wake-up is complete.
- At this point, once the device receives a nSLEEP reset pulse (HW variant) or a CLR FAULT command through SPI (SPI variant) as an acknowledgment of the wake-up from the controller, the device enters the STANDBY state. This is indicated by the de-assertion of the nFAULT pin. The driver is held in Hi-Z till this point.
- From here on, the device is ready to drive the bridge based on the truth tables for the specific mode configured.

Refer to the wake-up transients waveforms for the illustration.

8.4.4 ACTIVE State

The device is fully functional in this state with the drivers controlled by other inputs as described in prior sections. All protection features are fully functional with fault signaling on nFAULT pin. SPI communication is available.The device can transition into this state only from the STANDBY state.

8.4.5 nSLEEP Reset Pulse (HW Variant Only)

This is a special communication signal from the controller to the device through the nSLEEP pin available only for the HW variant. This is used to:

- Acknowledge the nFAULT asserted during the SLEEP/ Power up transition to STANDBY state
- Clear a latched fault when the fault reaction is configured to the LATCHED setting, without forcing the device into SLEEP or affecting any of the other functions (Equivalent to the CLR_FAULT command in the SPI variant)

This pulse on nSLEEP must be greater than the nSLEEP deglitch time of t_{RESET} time, but shorter than t_{SLEEP} time, as shown in case # 3, in Table 8-19 below.

Table 8-19. nSLEEP Timing (HW Variant Only)

Case #	Window Start Time	Window End Time	Command Interpretation	
			Clear Fault	Sleep
1	0	t_{RESET} min	No	No

Table 8-19. nSLEEP Timing (HW Variant Only) (continued)

Case #	Window Start Time	Window End Time	Command Interpretation	
			Clear Fault	Sleep
2	t_{RESET} min	t_{RESET} max	Indeterminate	No
3	t_{RESET} max	t_{SLEEP} min	Yes	No
4	t_{SLEEP} min	t_{SLEEP} max	Yes	Indeterminate
5	t_{SLEEP} max	No limit	Yes	Yes

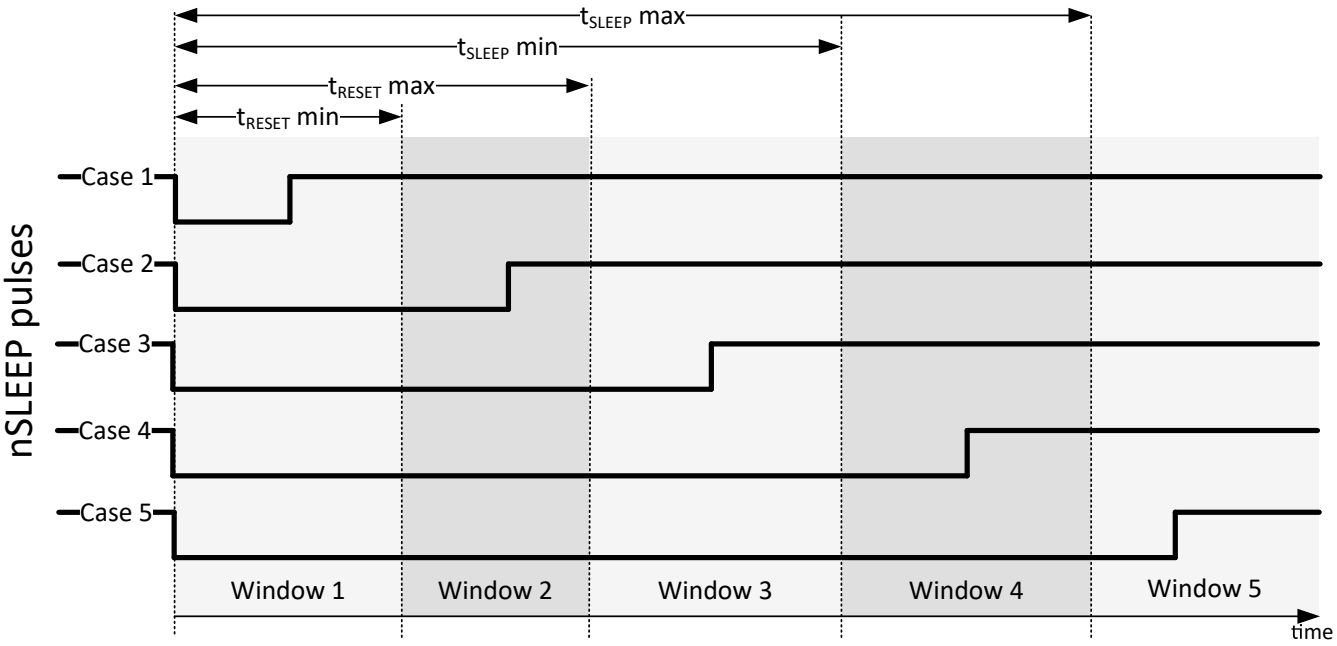

Figure 8-9. nSLEEP Pulse Scenarios

8.5 Programming - SPI Variant Only

8.5.1 SPI Interface

The SPI variant has full-duplex, 4-wire synchronous communication that is used to set device configurations, operating parameters, and read out diagnostic information from the device. The SPI operates in peripheral mode and connects to a controller. The serial data input (SDI) word consists of a 16-bit word, with an 8-bit command (A1), followed by 8-bit data (D1). The serial data output (SDO) word consists of the FAULT_SUMMARY byte (S1), followed by a report byte (R1). The report byte is either the register data being accessed by read command or null for a write command. The data sequence between the MCU and the SPI peripheral driver is shown in Figure 8-10.

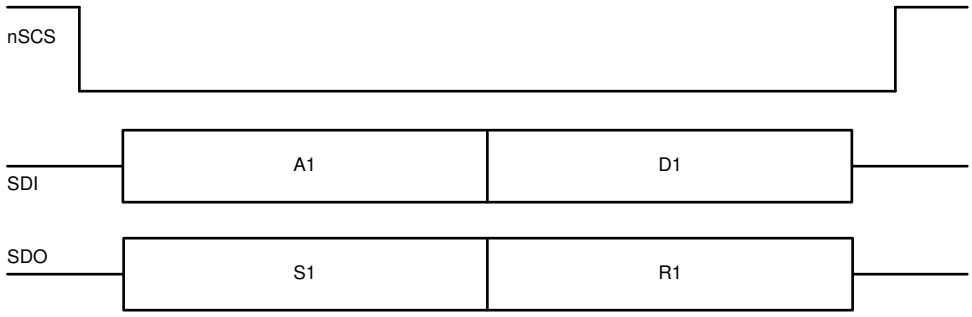

Figure 8-10. SPI Data - Standard "16-bit" Frame

A valid frame must meet the following conditions:

- SCLK pin should be low when the nSCS pin transitions from high to low and from low to high.
- nSCS pin should be pulled high between words.
- When nSCS pin is pulled high, any signals at the SCLK and SDI pins are ignored and the SDO pin is placed in the Hi-Z state.
- Data on SDO from the device is propagated on the rising edge of SCLK, while data on SDI is captured by the device on the subsequent falling edge of SCLK.
- The most significant bit (MSB) is shifted in and out first.
- A full 16 SCLK cycles must occur for a valid transaction for a standard frame, or alternately, for a daisy chain frame with "n" number of peripheral devices, 16 + (n x 16) SCLK cycles must occur for a valid transaction. Else, a frame error (SPI_ERR) is reported and the data is ignored if it is a WRITE operation.

8.5.2 Standard Frame

The SDI input data word is 2 bytes long and consists of the following format:

- Command byte (first byte)
  - MSB bit indicates frame type (bit B15 = 0 for standard frame).
  - Next to MSB bit, W0, indicates read or write operation (bit B14, write = 0, read = 1)
  - Followed by 6 address bits, A[5:0] (bits B13 through B8)
- Data byte (second byte)
  - Second byte indicates data, D[7:0] (bits B7 through B0). For a read operation, these bits are typically set to null values, while for a write operation, these bits have the data value for the addressed register.

Table 8-20. SDI - Standard Frame Format

	Command Byte								Data Byte							
Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data	0	W0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

The SDO output data word is 2 bytes long and consists of the following format:

- Status byte (first byte)
  - 2 MSB bits are forced high (B15, B14 = 1)
  - Following 6 bits are from the FAULT SUMMARY register (B13:B8)
- Report byte (second byte)
  - The second byte (B7:B0) is either the data currently in the register being read for a read operation (W0 = 1), or, existing data in the register being written to for a write command (W0 = 0)

Table 8-21. SDO - Standard Frame Format

	Status Byte								Report Byte							
Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

Table 8-21. SDO - Standard Frame Format (continued)

	Status Byte								Report Byte							
Data	1	1	FAULT	VMOV	VMUV	OCP	TSD	SPI_ERR	D7	D6	D5	D4	D3	D2	D1	D0

8.5.3 SPI Interface for Multiple Peripherals

Multiple devices can be connected to the controller with and without the daisy chain. For connecting a 'n' number of devices to a controller without using a daisy chain, 'n' number of I/O resources from controller has to utilized for nSCS pins as shown in Figure 8-11. Whereas, if the daisy chain configuration is used, then a single nSCS line can be used for connecting multiple devices. Figure 8-12

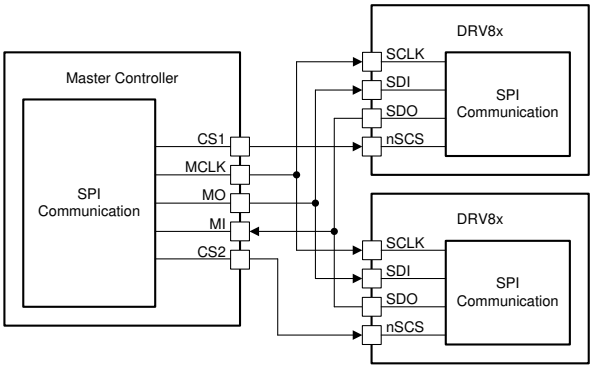

Figure 8-11. SPI Operation Without Daisy Chain

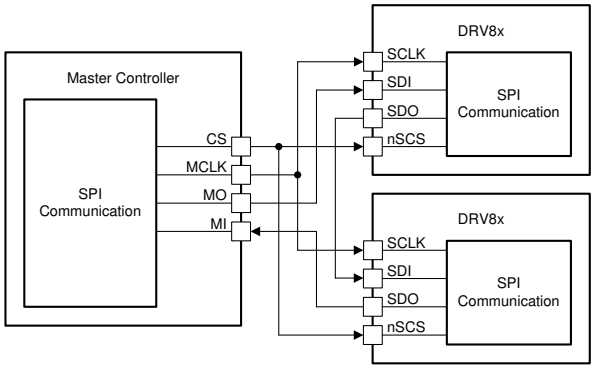

Figure 8-12. SPI Operation With Daisy Chain

8.5.3.1 Daisy Chain Frame for Multiple Peripherals

The device can be connected in a daisy chain configuration to save GPIO ports when multiple devices are communicating to the same MCU. Figure 8-13 shows the topology with waveforms, where, number of peripherals connected in a daisy chain "n" is set to 3. A maximum of up to 63 devices can be connected in this manner.

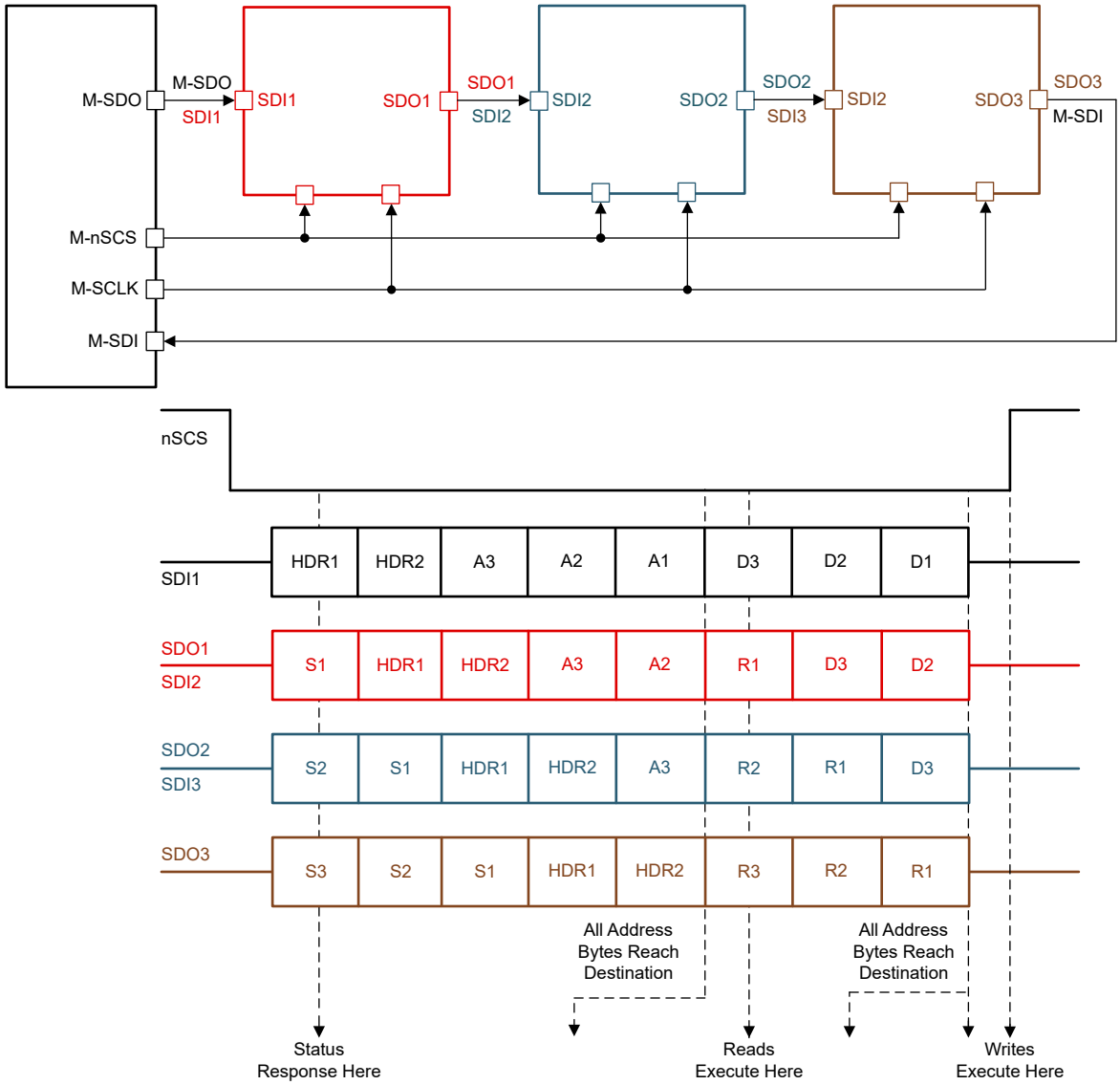

Figure 8-13. Daisy Chain SPI Operation

The SDI sent by the controller in this case would be in the following format (see SDI1 in Figure 8-13):

- 2 bytes of header (HDR1, HDR2)
- "n" bytes of command byte starting with furthest peripheral in the chain (for this example, this is A3, A2, A1)
- "n" bytes of data byte starting with furthest peripheral in the chain (for this example, this is D3, D2, D1)
- Total of 2 x "n" + 2 bytes

While the data is being transmitted through the chain, the controller receives it in the following format (see SDO3 in Figure 8-13):

- 3 bytes of status byte starting with furthest peripheral in the chain (for this example, this is S3, S2, S1)
- 2 bytes of header that were transmitted before (HDR1, HDR2)
- 3 bytes of report byte starting with furthest peripheral in the chain (for this example, this is R3, R2, R1)

The Header bytes are special bytes asserted at the beginning of a daisy chain SPI communication. **Header bytes must start with 1 and 0 for the two leading bits.**

The first header byte (HDR1) contains information of the total number of peripheral devices in the daisy chain. N5 through N0 are 6 bits dedicated to show the number of device in the chain as shown in Figure 8-14. Up to 63 devices can be connected in series per daisy chain connection. Number of peripheral = 0 is not permitted and will result in a SPI_ERR flag.

The second header byte (HDR2) contains a global CLR FAULT command that will clear the fault registers of all the devices on the rising edge of the chip select (nSCS) signal. The 5 trailing bits of the HDR2 register are marked as SPARE (don't care bits). These can be used by the MCU to determine integrity of the daisy chain connection.

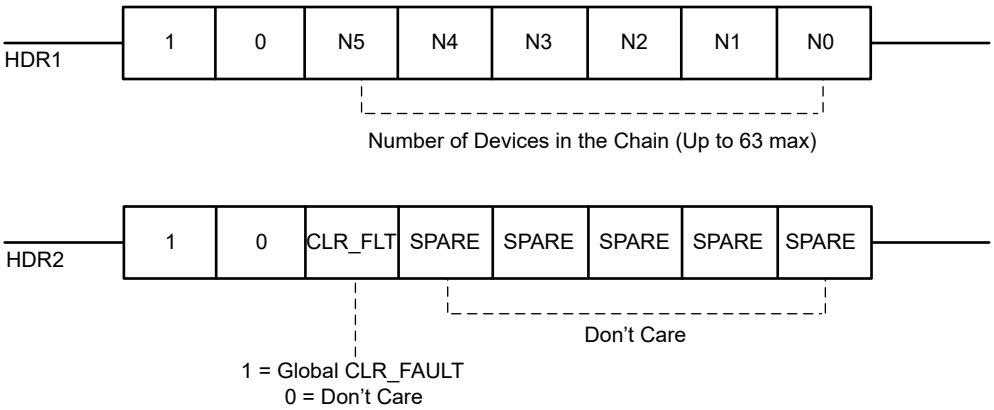

Figure 8-14. Header bytes

In addition, the device recognizes bytes that start with 1 and 1 for the two leading bits as a "pass" byte. These "pass" bytes are NOT processed by the device, but they are simply transmitted out on SDO in the following byte.

When data passes through a device, it determines the position of itself in the chain by counting the number of Status bytes it receives following by the first Header byte. For example, in this 3 device configuration, device 2 in the chain will receive two status bytes before receiving the two header bytes.

From the two status bytes it knows that its position is second in the chain, and from HDR2 byte it knows how many devices are connected in the chain. That way it only loads the relevant address and data byte in its buffer and bypasses the other bits. This protocol allows for faster communication without adding latency to the system for up to 63 devices in the chain.

The command, data, status and report bytes remain the same as described in the standard frame format.

8.6 Register Map - SPI Variant Only

This section describes the user configurable registers in the device.

Note

While the device allows register writes at any time SPI communication is available, it is recommended to exercise caution while updating registers in the ACTIVE state while the load is being driven. This is especially important for settings such as S_MODE and S_DIAG which control the critical device configuration. In order to prevent accidental register writes, the device offers a locking mechanism through the REG_LOCK bits in the COMMAND register to lock the contents of all configurable registers. Best practice would be to write all the configurable registers during initialization and then lock these settings. Run-time register writes for output control are handled by the SPI_IN register, which offers its own separate locking mechanism through the SPI_IN_LOCK bits.

8.6.1 User Registers

The following table lists all the registers that can be accessed by the user. All register addresses NOT listed in this table should be considered as "reserved" locations and access is blocked to this space. Accessing them will cause a SPI_ERR.

Table 8-22. User Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type (2)	Addr
DEVICE_ID	DEV_ID[5]	DEV_ID[4]	DEV_ID[3]	DEV_ID[2]	DEV_ID[1]	DEV_ID[0]	REV_ID[1]	REV_ID[0]	R	00h
FAULT_SUMMARY	SPI_ERR(3)	POR	FAULT	VMOV	VMUV	OCP	TSD	OLA (3)	R	01h
STATUS1	OLA1	OLA2	ITRIP_CMP	ACTIVE	OCP_H1	OCP_L1	OCP_H2	OCP_L2	R	02h
STATUS2	DRVOFF_STAT	N/A(4)	N/A(4)	ACTIVE	N/A(4)	N/A(4)	N/A(4)	OLP_CMP	R	03h
COMMAND	CLR_FLT	N/A(4)	N/A(4)	SPI_IN_LOCK[1]	SPI_IN_LOCK[0] (1)	N/A(4)	REG_LOCK[1]	REG_LOCK[0] (1)	R/W	08h
SPI_IN	N/A(4)	N/A(4)	N/A(4)	N/A(4)	S_DRVOFF (1)	S_DRVOFF2 (1)	S_EN_IN1	S_PH_IN2	R/W	09h
CONFIG1	EN_OLA	VMOV_SEL[1]	VMOV_SEL[0]	SSC_DIS(1)	OCP_RETRY	TSD_RETRY	VMOV_RETRY	OLA_RETRY	R/W	0Ah
CONFIG2	PWM_EXTEND	S_DIAG[1]	S_DIAG[0]	N/A(4)	N/A(4)	S_ITRIP[2]	S_ITRIP[1]	S_ITRIP[0]	R/W	0Bh
CONFIG3	TOFF[1]	TOFF[0] (1)	N/A(4)	S_SR[2]	S_SR[1]	S_SR[0]	S_MODE[1]	S_MODE[0]	R/W	0Ch
CONFIG4	TOCP_SEL[1]	TOCP_SEL[0]	N/A(4)	OCP_SEL[1]	OCP_SEL[0]	DRVOFF_SEL(1)	EN_IN1_SEL	PH_IN2_SEL	R/W	0Dh

(1) Defaulted to 1b on reset, others are defaulted to 0b on reset
(2) R = Read Only, R/W = Read/Write
(3) OLA replaced by SPI_ERR in the first SDO byte response, common to all SPI frames. Refer SDO - Standard frame format.
(4) N/A = Not available (read back of this bit will be 0b)

8.6.1.1 DEVICE_ID register (Address = 00h)

Return to the User Register table.

Device	DEVICE_ID value
DRV8243S-Q1	32h
DRV8244S-Q1	42h
DRV8245S-Q1	52h
DRV8243P-Q1	36h
DRV8244P-Q1	46h
DRV8245P-Q1	56h

8.6.1.2 FAULT_SUMMARY Register (Address = 01h) [reset = 40h]

Return to the User Register table.

Bit	Field	Type	Reset	Description
7	SPI_ERR	R	0b	1b indicates that a SPI communication fault has occurred in the previous SPI frame.
6	POR	R	1b	1b indicates that a power-on-reset has been detected.
5	FAULT	R	0b	Logic OR of SPI_ERR, POR, VMOV, VMUV, OCP, TSD & OLA
4	VMOV	R	0b	1b indicates that a VM over voltage has been detected. Refer VMOV_SEL to change thresholds or disable diagnostic, VMOV_RETRY to configure fault reaction.
3	VMUV	R	0b	1b indicates that a VM under voltage has been detected.
2	OCP	R	0b	1b indicates that an over current has been detected in either one or more power FETs. Refer OCP_SEL, TOCP_SEL to change thresholds & filter times. Refer OCP_RETRY to configure fault reaction.
1	TSD	R	0b	1b indicates that an over temperature has been detected. Refer TSD_RETRY to configure fault reaction.
0	OLA	R	0b	1b indicates that an open load condition has been detected in the ACTIVE state. Refer to EN_OLA to disable diagnostic, OLA_RETRY to configure fault reaction.

8.6.1.3 STATUS1 Register (Address = 02h) [reset = 00h]

Return to the User Register table.

Bit	Field	Type	Reset	Description
7	OLA1	R	0b	1b indicates that an open load condition has been detected in the ACTIVE state on OUT1
6	OLA2	R	0b	1b indicates that an open load condition has been detected in the ACTIVE state on OUT2
5	ITRIP_CMP	R	0b	1b indicates that load current has reached the ITRIP regulation level.

Bit	Field	Type	Reset	Description
4	ACTIVE	R	0b	1b indicates that the device is in the ACTIVE state
3	OCP_H1	R	0b	1b indicates that an over current has been detected on the high-side FET (short to GND) on OUT1
2	OCP_L1	R	0b	1b indicates that an over current has been detected on the low-side FET (short to VM) on OUT1
1	OCP_H2	R	0b	1b indicates that an over current has been detected on the high-side FET (short to GND) on OUT2
0	OCP_L2	R	0b	1b indicates that an over current has been detected on the low-side FET (short to VM) on OUT2

8.6.1.4 STATUS2 Register (Address = 03h) [reset = 80h]

Return to the User Register table.

Bit	Field	Type	Reset	Description
7	DRVOFF_STAT	R	1b	This bit shows the status of the DRVOFF pin. 1b implies the pin status is high.
6, 5	N/A	R	0b	Not available
4	ACTIVE	R	0b	1b indicates that the device is in the ACTIVE state (Copy of bit4 in STATUS1)
3, 2, 1	N/A	R	0b	Not available
0	OLP_CMP	R	0b	This bit is the output of the off-state diagnostics (OLP) comparator.

8.6.1.5 COMMAND Register (Address = 08h) [reset = 09h]

Return to the User Register table.

Bit	Field	Type	Reset	Description
7	CLR_FLT	R/W	0b	Clear Fault command - Write 1b to clear all faults reported in the fault registers and de-assert the nFAULT pin
6-5	N/A	R	0b	Not available
4-3	SPI_IN_LOCK	R/W	01b	Write 10b to **unlock** the SPI_IN register Write 01b or 00b or 11b to **lock** the SPI_IN register SPI_IN register is **locked** by default.
2	N/A	R	0b	Not available
1-0	REG_LOCK	R/W	01b	Write 10b to **lock** the CONFIG registers Write 01b or 00b or 11b to **unlock** the CONFIG registers CONFIG registers are **unlocked** by default.

8.6.1.6 SPI_IN Register (Address = 09h) [reset = 0Ch]

Return to the User Register table.

Bit	Field	Type	Reset	Description
7-4	N/A	R	0b	Not available
3	S_DRVOFF	R/W	1b	Register bit equivalent of DRVOFF pin when SPI_IN is unlocked. Refer Register Pin control section. In Independent mode, this bit shuts off half-bridge 1.
2	S_DRVOFF2	R/W	1b	Register bit to shut off half-bridge 2 in Independent mode when SPI_IN is unlocked. Refer Register Pin control section
1	S_EN_IN1	R/W	0b	Register bit equivalent of EN/IN1 pin when SPI_IN is unlocked. Refer Register Pin control section
0	S_PH_IN2	R/W	0b	Register bit equivalent of PH/IN2 pin when SPI_IN is unlocked. Refer Register Pin control section

8.6.1.7 CONFIG1 Register (Address = 0Ah) [reset = 10h]

Return to the User Register table.

Bit	Field	Type	Reset	Description
7	EN_OLA	R/W	0b	Write 1b to enable open load detection in the active state. In Independent mode, OLA is always disabled for low-side load. Refer DIAG section.
6-5	VMOV_SEL	R/W	0b	Determines the thresholds for the VM over voltage diagnostics 00b = VM > 35 V 01b = VM > 28 V 10b = VM > 18 V 11b = VMOV disabled
4	SSC_DIS	R/W	1b	0b: Enables the spread spectrum clocking feature
3	OCP_RETRY	R/W	0b	Write 1b to configure fault reaction to retry setting on the detection of over current, else the fault reaction is latched
2	TSD_RETRY	R/W	0b	Write 1b to configure fault reaction to retry setting on the detection of over temperature, else the fault reaction is latched
1	VMOV_RETRY	R/W	0b	Write 1b to configure fault reaction to retry setting on the detection of VMOV, else the fault reaction is latched. **Note** For the SPI (P) variant, this bit also controls the fault reaction for a VM under voltage detection.

Bit	Field	Type	Reset	Description
0	OLA_RETRY	R/W	0b	Write 1b to configure fault reaction to retry setting on the detection of open load during active, else the fault reaction is latched.

8.6.1.8 CONFIG2 Register (Address = 0Bh) [reset = 00h]

Return to the User Register table.

Bit	Field	Type	Reset	Description
7	PWM_EXTEND	R/W	0b	Write 1b to access additional Hi-Z (coast) states in the PWM mode - refer PWM EXTEND table
6-5	S_DIAG	R/W	0b	Load type indication - refer to DIAG table
4-3	N/A	R	0b	Not available
2-0	S_ITRIP	R/W	0b	ITRIP level configuration - refer ITRIP table

8.6.1.9 CONFIG3 Register (Address = 0Ch) [reset = 40h]

Return to the User Register table.

Bit	Field	Type	Reset	Description
7-6	TOFF	R/W	1b	TOFF time used for ITRIP current regulation 00b = 20 µsec 01b = 30 µsec 10b = 40 µsec 11b = 50 µsec
5	N/A	R	0b	Not available
4-2	S_SR	R/W	0b	Slew Rate configuration - refer to Section 8.3.3.1
1-0	S_MODE	R/W	0b	Device mode configuration - refer MODE table

8.6.1.10 CONFIG4 Register (Address = 0Dh) [reset = 04h]

Return to the User Register table.

Bit	Field	Type	Reset	Description
7-6	TOCP_SEL	R/W	0b	Filter time for over current detection configuration 00b = 6 µsec 01b = 3 µsec 10b = 1.5 µsec 11b = Minimum (~0.2 µsec)
5	N/A	R	0b	Not available
4-3	OCP_SEL	R/W	0b	Threshold for over current detection configuration 00b = 100% setting 01b, 11b = 50% setting 10b = 75% setting
2	DRVOFF_SEL	R/W	1b	DRVOFF pin - register logic combination, when SPI_IN is unlocked 0b = OR 1b = AND
1	EN_IN1_SEL	R/W	0b	EN/IN1 pin - register logic combination, when SPI_IN is unlocked 0b = OR 1b = AND
0	PH_IN2_SEL	R/W	0b	PH/IN2 pin - register logic combination, when SPI_IN is unlocked 0b = OR 1b = AND

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV824x-Q1 family of devices can be used in a variety of applications that require either a half-bridge or H-bridge power stage configuration. Common application examples include brushed DC motors, solenoids, and actuators. The device can also be utilized to drive many common passive loads such as LEDs, resistive elements, relays, etc. The application examples below will highlight how to use the device in bidirectional current control applications requiring an H-bridge driver and dual unidirectional current control applications requiring two half-bridge drivers.

9.1.1 Load Summary

Table 9-1 summarizes the utility of the device features for different type of inductive loads.

Table 9-1. Load Summary Table

LOAD TYPE	Configuration		Device Feature		
	Device	Recirculation Path	Slew Rate	Current sense	ITRIP regulation
Bi-directional motor or solenoid(1)	DRV824x in PH/EN or PWM mode	High-side	Full range	Continuous	Useful
2 Uni-directional motors or low-side solenoids (one side connected to GND)	DRV824x in Independent mode (2)	Low-side	Limited(4)	Discontinuous(3),	Individual load regulation not possible
2 High-side solenoids (one side connected to VM)	DRV824x in Independent mode (2)	High-side	Full range	Not available, need external solution	

(1) Solenoid - clamping or quick demagnetization possible, but clamping level will be VM dependent
(2) Independent Hi-Z only supported in the SPI variant
(3) Not sensed during recirculation and during OUTx voltage slew times including t_{blank}
(4) Rising edge slew rate capped at 8 V/µsec for higher settings

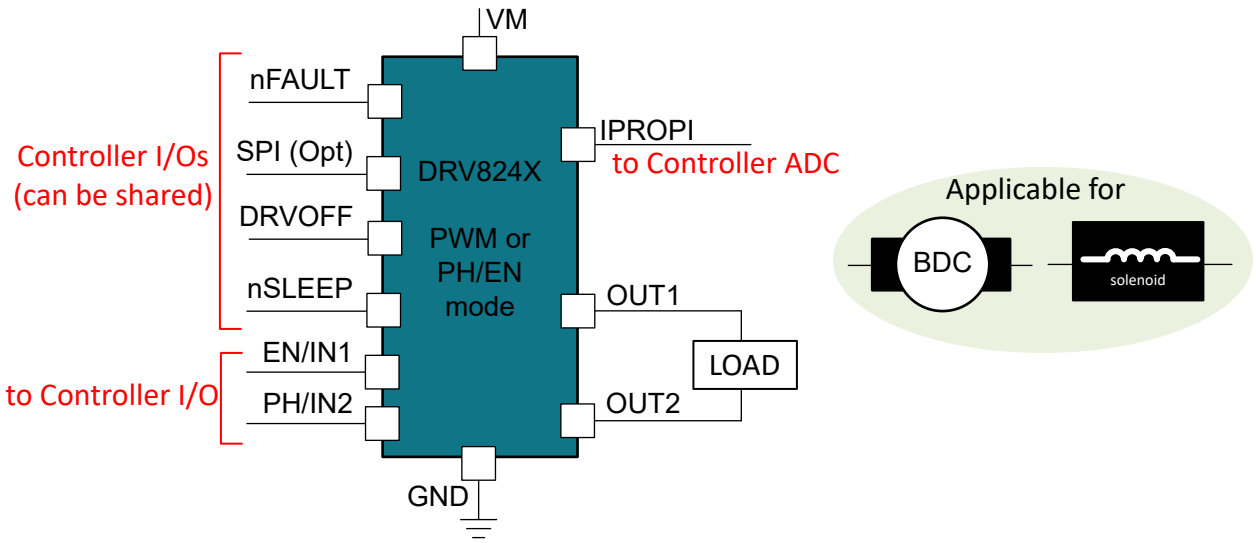

Figure 9-1. Illustration Showing a Full-Bridge Topology With DRV824X-Q1 in PWM or PH/EN Mode

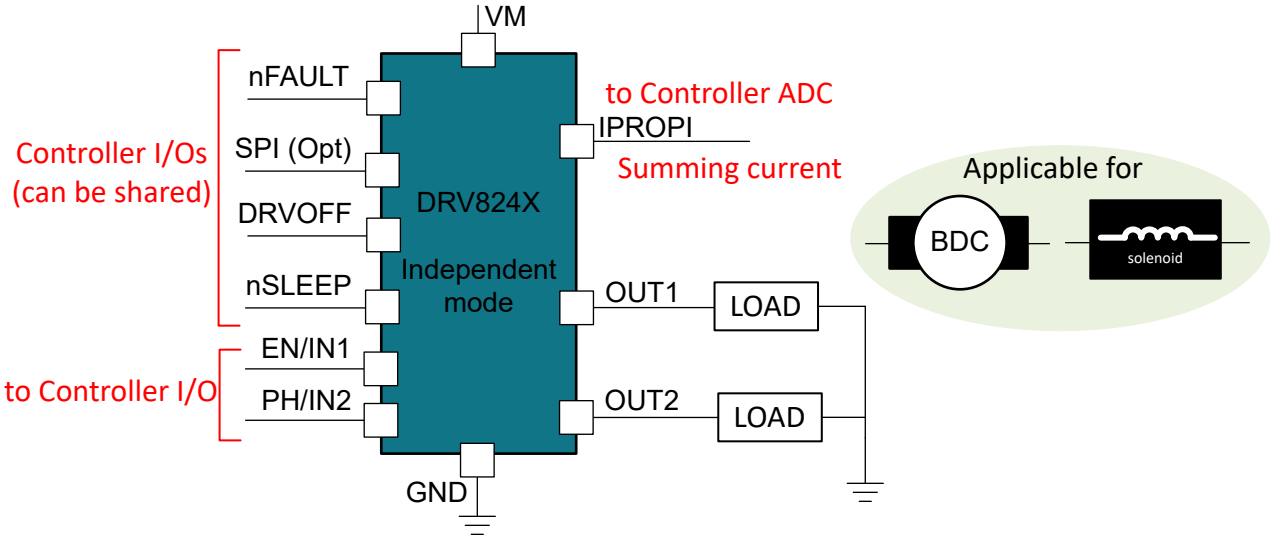

Figure 9-2. Illustration Showing Half-Bridge Topology to Drive Two Low-side Loads Independently With DRV824X-Q1 Device in INDEPENDENT Mode

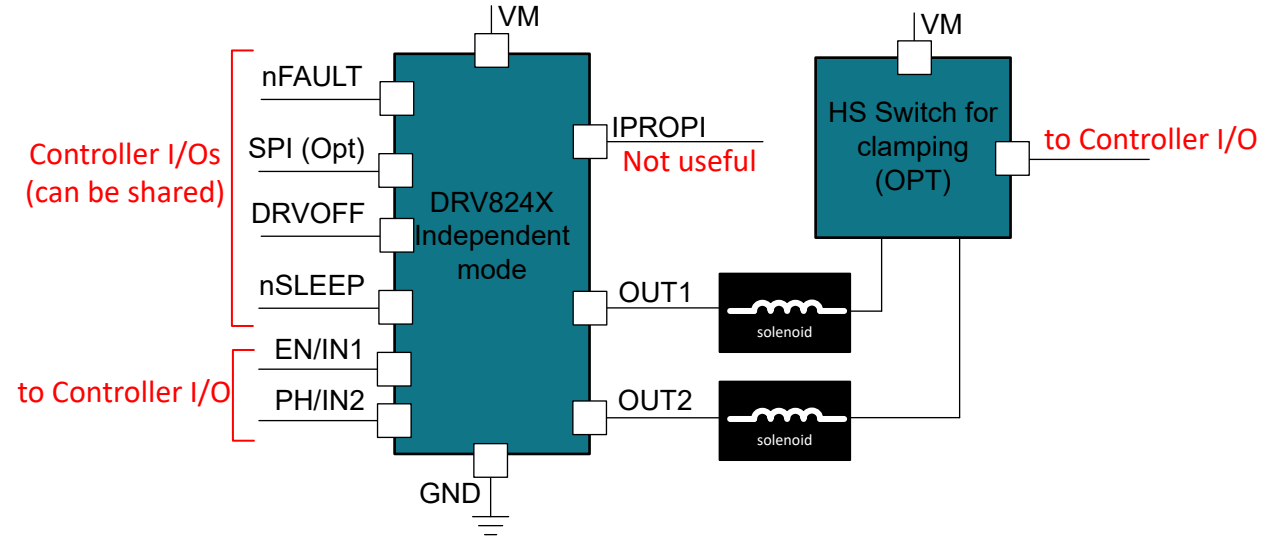

Figure 9-3. Illustration Showing a Half-Bridge Topology to Drive Two High-side Loads Independently With DRV824X-Q1 Device in INDEPENDENT Mode

9.2 Typical Application

The figures below show the typical application schematic for driving a brushed DC motor or any inductive load in various modes. There are several optional connections shown in these schematics, which are listed as follows:

- nSLEEP pin
  - SPI (S) variant - This pin can be tied off high in the application if SLEEP function is not needed.
  - SPI (P) variant - N/A
  - HW (H) variant - Pin control is **mandatory** even if SLEEP function is not needed. The controller needs to issue a reset pulse (typical: 30 µsec bounded between t_{reset} max and t_{sleep} min) during wake-up to acknowledge wake-up or power-up.
- DRVOFF pin
  - Both SPI (P) and SPI (S) variants - This pin can be tied off low in the application if shutoff through **pin** function is not needed. The equivalent register bit can be used.
- EN/IN1 pin

  - Both SPI (P) and SPI (S) variants - This pin can be tied off low or left floating if register only control is needed.
- PH/IN2 pin
  - Both SPI (P) and SPI (S) variants - This pin can be tied off low or left floating if register only control is needed.
- OUT1 & OUT2 pins
  - Recommend to add PCB footprints for capacitors from OUTx to GND as well as between OUTx close to the load for EMC purposes.
- IPROPI pin
  - All variants - Monitoring of this output is optional. Also IPROPI pin can be tied low if ITRIP feature & IPROPI function is not needed. Recommend to add a PCB footprint for a small capacitor (10 nF to 100 nF) if needed.
- nFAULT pin
  - Both SPI (P) and SPI (S) variants - Monitoring of this output is optional. All diagnostic information can be read from the STATUS registers.
- SPI input pins
  - Both SPI (S) and SPI (P) variants - Inputs (SDI, nSCS, SCLK) are compatible with 3.3 V / 5 V levels.
- SPI SDO pin
  - SPI (S) variant - SDO tracks the nSLEEP pin voltage.
  - SPI (P) variant - SDO tracks the VDD pin voltage. To interface with a 3.3 V level controller input, a level shifter or a current limiting series resistor is recommended.
- CONFIG pins
  - HW (H) variant - Resistor is not needed for short to GND and Hi-Z level selections
    - LVL1 and LVL3 for MODE pin
    - LVL1 and LVL6 for SR, ITRIP, DIAG pins

9.2.1 HW Variant

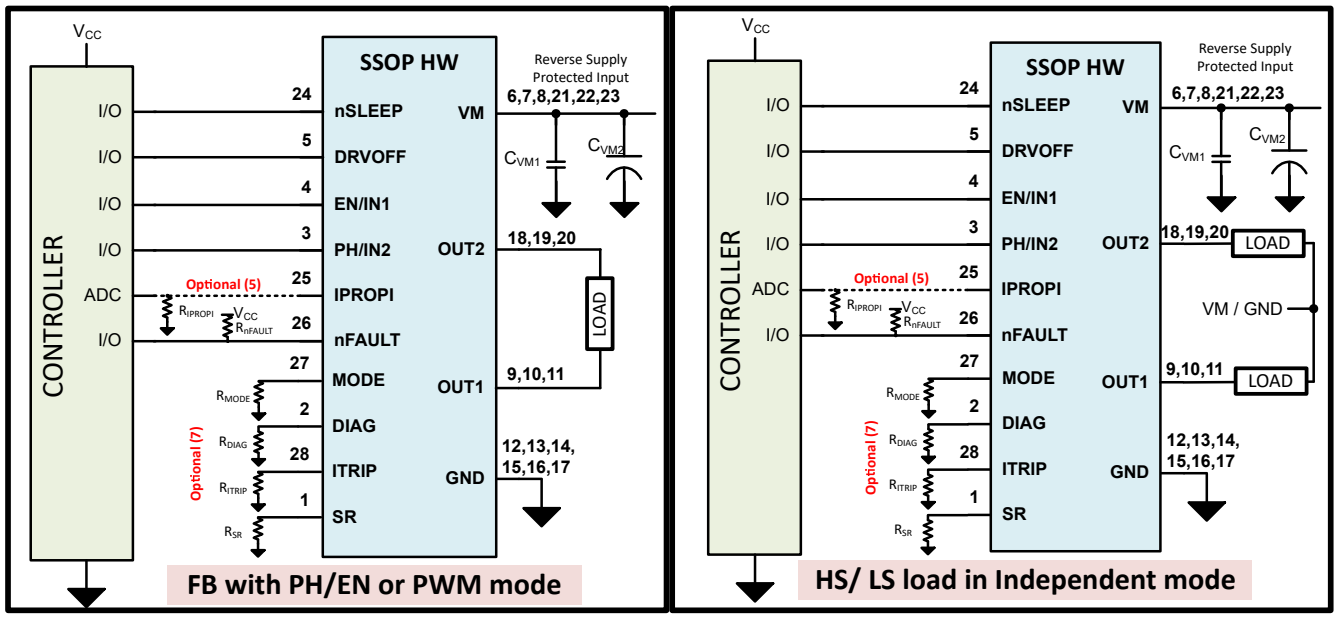

Figure 9-4. Typical Application Schematic - HW Variant in HVSSOP Package

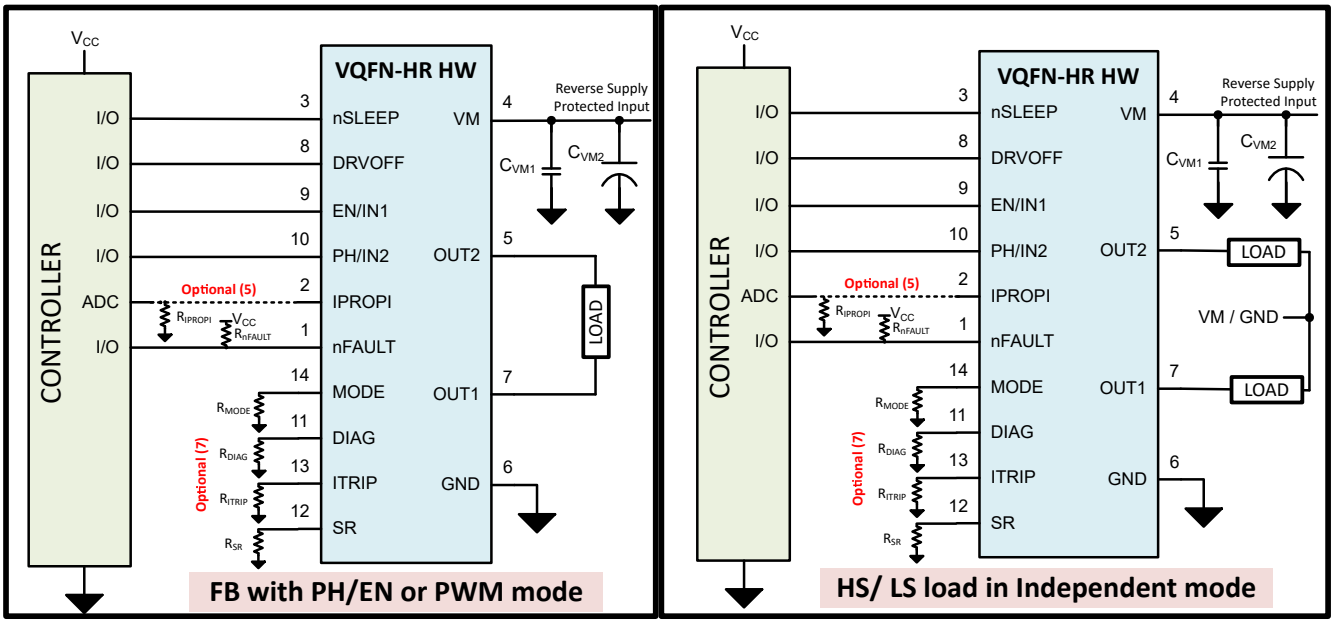

Figure 9-5. Typical Application Schematic - HW Variant in VQFN-HR Package

9.2.2 SPI Variant

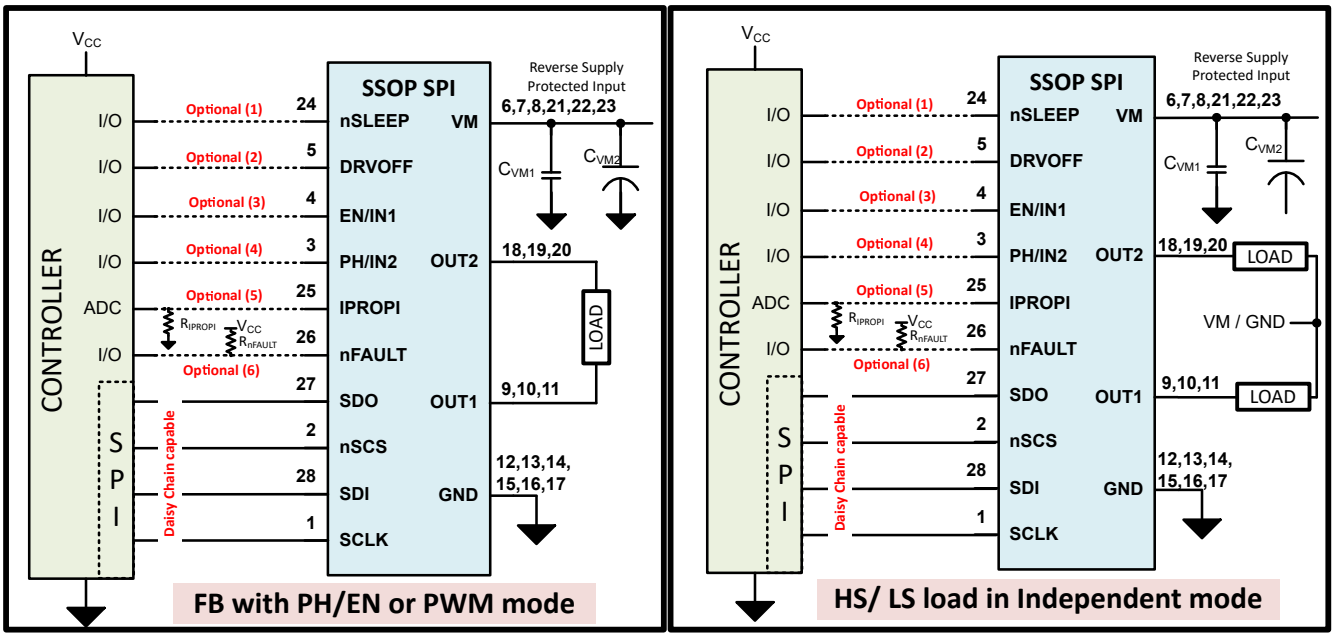

Figure 9-6. Typical Application Schematic - SPI (S) Variant in HVSSOP Package

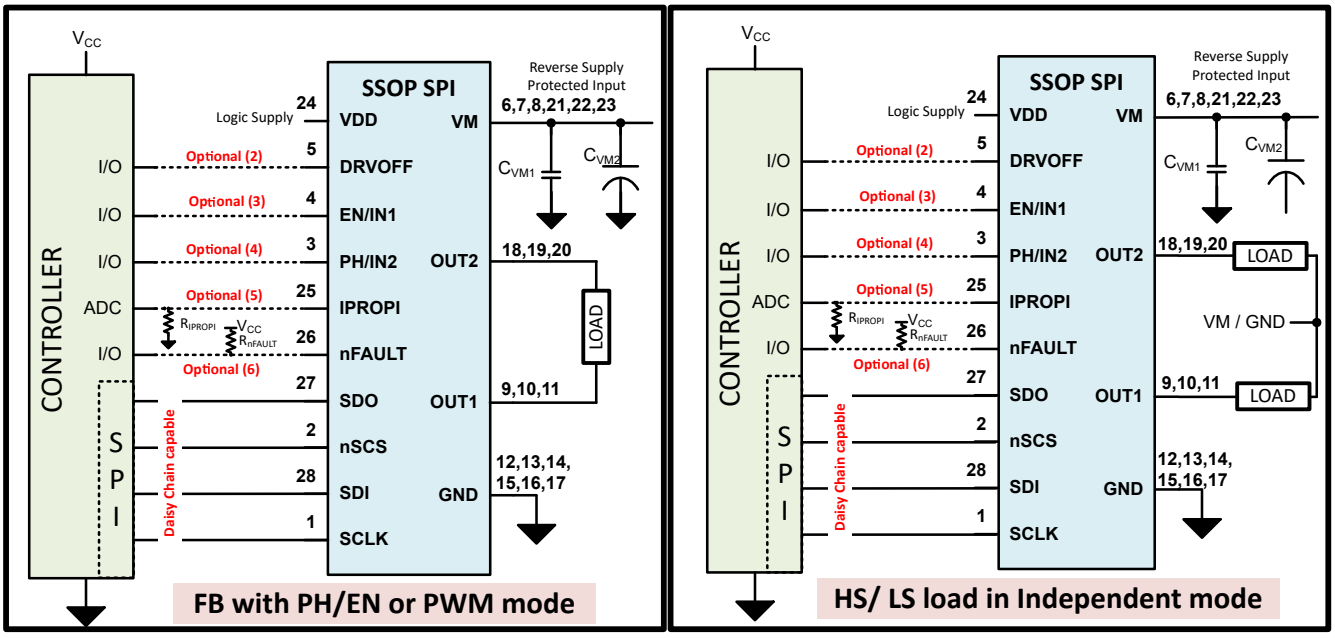

Figure 9-7. Typical Application Schematic - SPI (P) Variant in HVSSOP Package

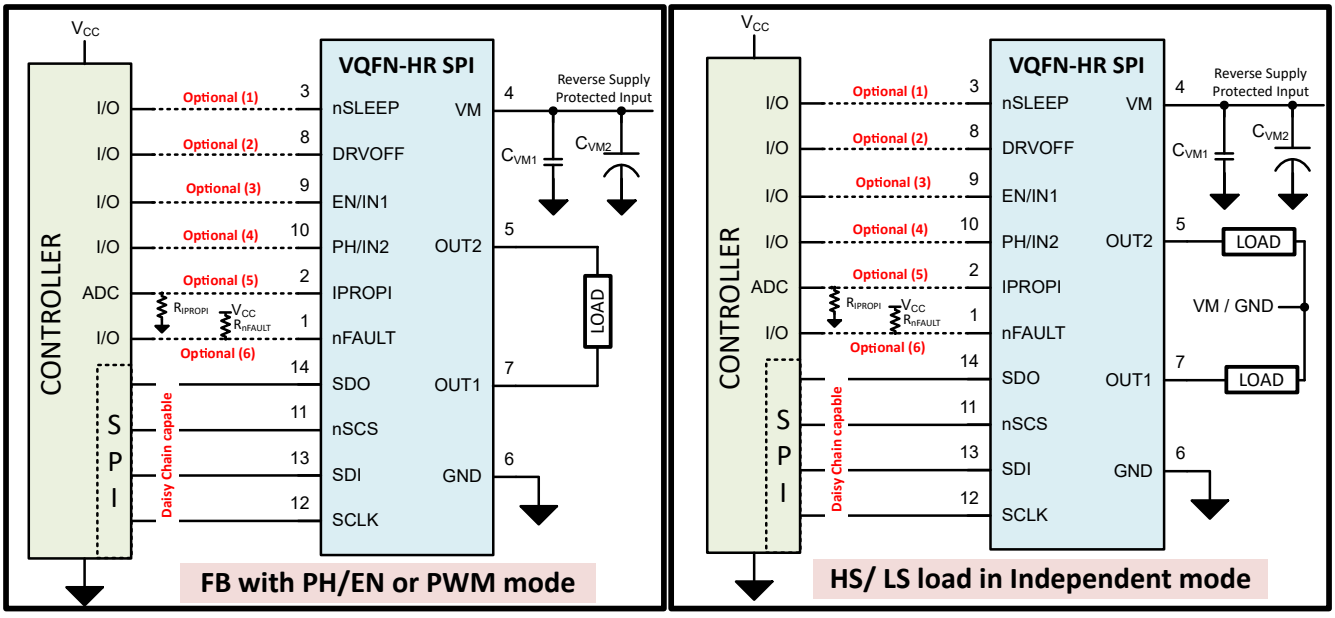

Figure 9-8. Typical Application Schematic - SPI (S) Variant in VQFN-HR Package

10 Power Supply Recommendations

The device is designed to operate with an input voltage supply (VM) range from 4.5 V to 40 V. A 0.1-µF ceramic capacitor rated for VM must be placed as close to the device as possible. Also, an appropriately sized bulk capacitor must be placed on the VM pin.

10.1 Bulk Capacitance Sizing

Bulk capacitance sizing is an important factor in motor drive system design. It is beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors including:

- The highest current required by the motor system.
- The capacitance of the power supply and the ability of the power supply to source current.
- The amount of parasitic inductance between the power supply and motor system.
- The acceptable voltage ripple.
- The type of motor used (brushed DC, brushless DC, and stepper).
- The motor braking method.

The inductance between the power supply and motor drive system limits the rate that current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When sufficient bulk capacitance is used, the motor voltage remains stable, and high current can be quickly supplied.

The data sheet provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

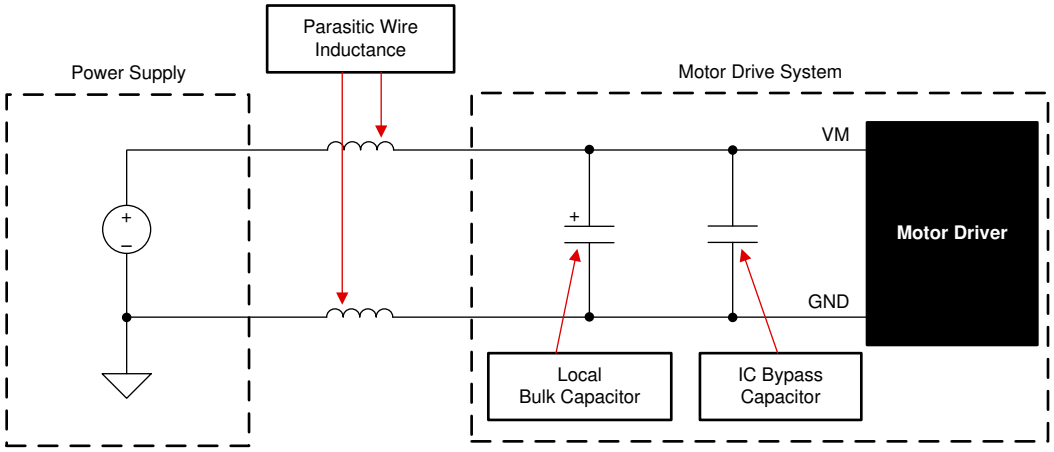

Figure 10-1. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage to provide a margin for cases when the motor transfers energy to the supply.

11 Layout

11.1 Layout Guidelines

Each VM pin must be bypassed to ground using low-ESR ceramic bypass capacitors with recommended values of 0.1 µF rated for VM. These capacitors should be placed as close to the VM pins as possible with a thick trace or ground plane connection to the device GND pin.

Additional bulk capacitance is required to bypass the high current path. This bulk capacitance should be placed such that it minimizes the length of any high current paths. The connecting metal traces should be as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

For the SPI (P) device variant, VDD pin may be bypassed to ground using low-ESR ceramic 6.3 V bypass capacitor with recommended values of 0.1 µF.

11.2 Layout Example

The following figure shows a layout example for a 4 cm X 4 cm x 1.6 mm, 4 layer PCB for a leaded package device. The 4 layers uses 2 oz copper on top/ bottom signal layers and 1 oz copper on internal supply layers, with 0.3 mm thermal via drill diameter, 0.025 mm Cu plating, 1 mm minimum via pitch. The same layout can be adopted for the non-leaded VQFN-HR package as well. The Section 7.5.14 for the 4 cm X 4 cm X 1.6 mm is based on a similar layout.

Note: The layout example shown is for a full bridge topology using DRV824xQ1 device in SSOP package.

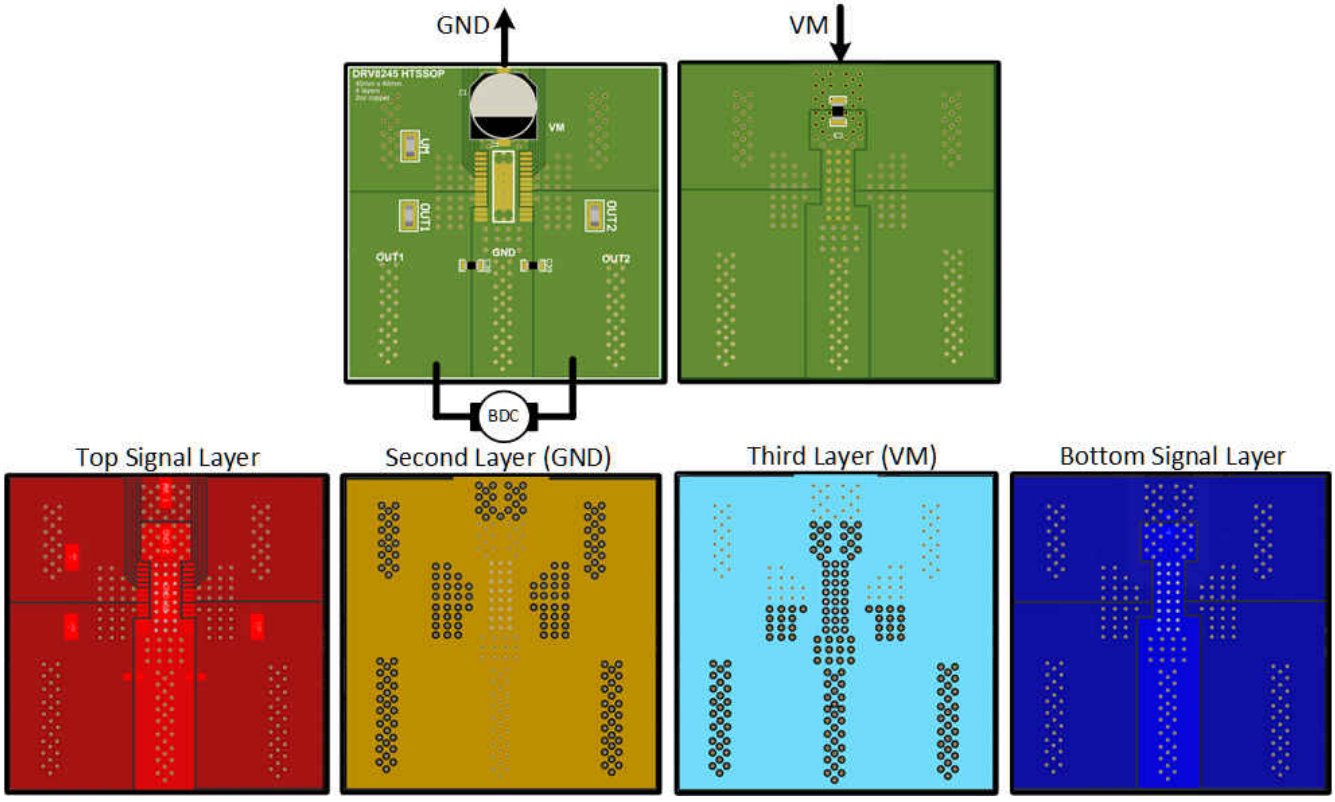

Figure 11-1. Layout example: 4cm x 4 cm x 1.6mm, 4 layer PCB

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Full Bridge Driver Junction Temperature Estimator (Excel-based worksheet)*
- Texas Instruments, *Calculating Motor Driver Power Dissipation* application report
- Texas Instruments, *Current Recirculation and Decay Modes* application report
- Texas Instruments, *PowerPAD™ Made Easy* application report
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application report
- Texas Instruments, *Understanding Motor Driver Current Ratings* application report
- Texas Instruments, *Best Practices for Board Layout of Motor Drivers* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

12.4 Trademarks

All trademarks are the property of their respective owners.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and order-able information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8243HQDGQRQ1	Active	Production	HVSSOP (DGQ) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	8243H
DRV8243HQDGQRQ1.A	Active	Production	HVSSOP (DGQ) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	8243H
DRV8243HQRXYRQ1	Active	Production	VQFN-HR (RXY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8243H
DRV8243HQRXYRQ1.A	Active	Production	VQFN-HR (RXY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8243H
DRV8243PQDGQRQ1	Active	Production	HVSSOP (DGQ) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	8243P
DRV8243PQDGQRQ1.A	Active	Production	HVSSOP (DGQ) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	8243P
DRV8243SQDGQRQ1	Active	Production	HVSSOP (DGQ) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	8243S
DRV8243SQDGQRQ1.A	Active	Production	HVSSOP (DGQ) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	8243S
DRV8243SQRXYRQ1	Active	Production	VQFN-HR (RXY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8243S
DRV8243SQRXYRQ1.A	Active	Production	VQFN-HR (RXY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8243S

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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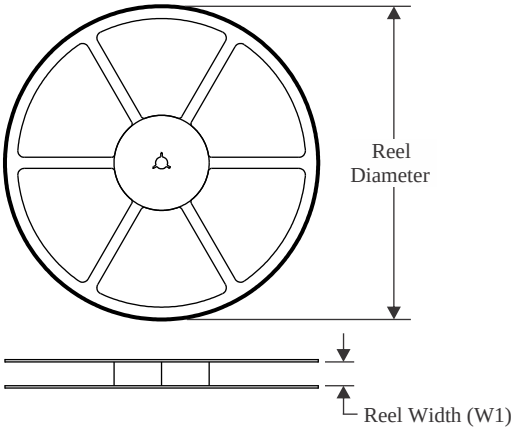
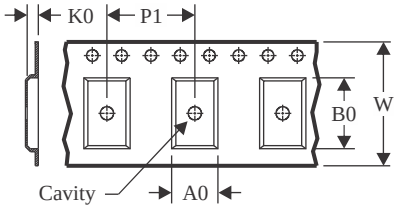
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

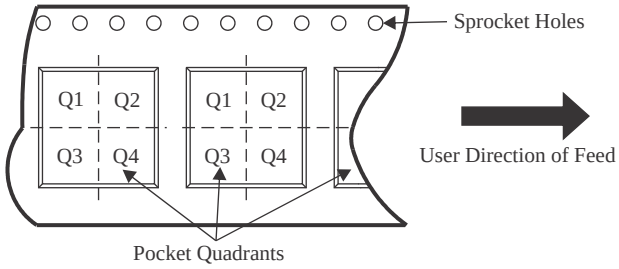


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

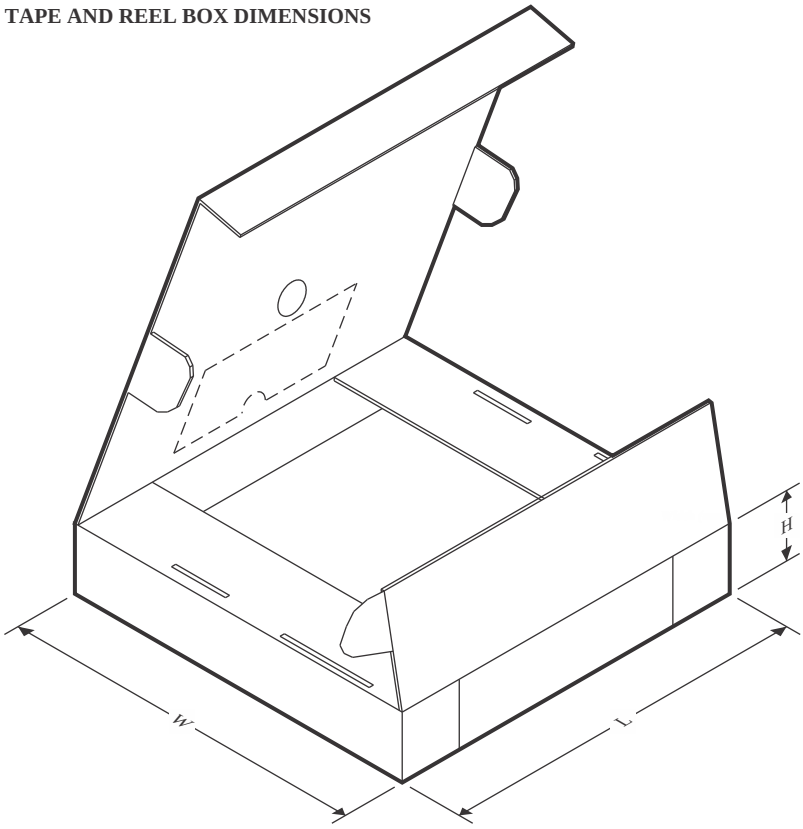
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8243HQDGQRQ1	HVSSOP	DGQ	28	2500	330.0	16.4	5.5	7.4	1.45	8.0	16.0	Q1
DRV8243HQRXYRQ1	VQFN-HR	RXY	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
DRV8243PQDGQRQ1	HVSSOP	DGQ	28	2500	330.0	16.4	5.5	7.4	1.45	8.0	16.0	Q1
DRV8243SQDGQRQ1	HVSSOP	DGQ	28	2500	330.0	16.4	5.5	7.4	1.45	8.0	16.0	Q1
DRV8243SQRXYRQ1	VQFN-HR	RXY	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8243HQDGQRQ1	HVSSOP	DGQ	28	2500	353.0	353.0	32.0
DRV8243HQRXYRQ1	VQFN-HR	RXY	14	3000	367.0	367.0	35.0
DRV8243PQDGQRQ1	HVSSOP	DGQ	28	2500	353.0	353.0	32.0
DRV8243SQDGQRQ1	HVSSOP	DGQ	28	2500	353.0	353.0	32.0
DRV8243SQRXYRQ1	VQFN-HR	RXY	14	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

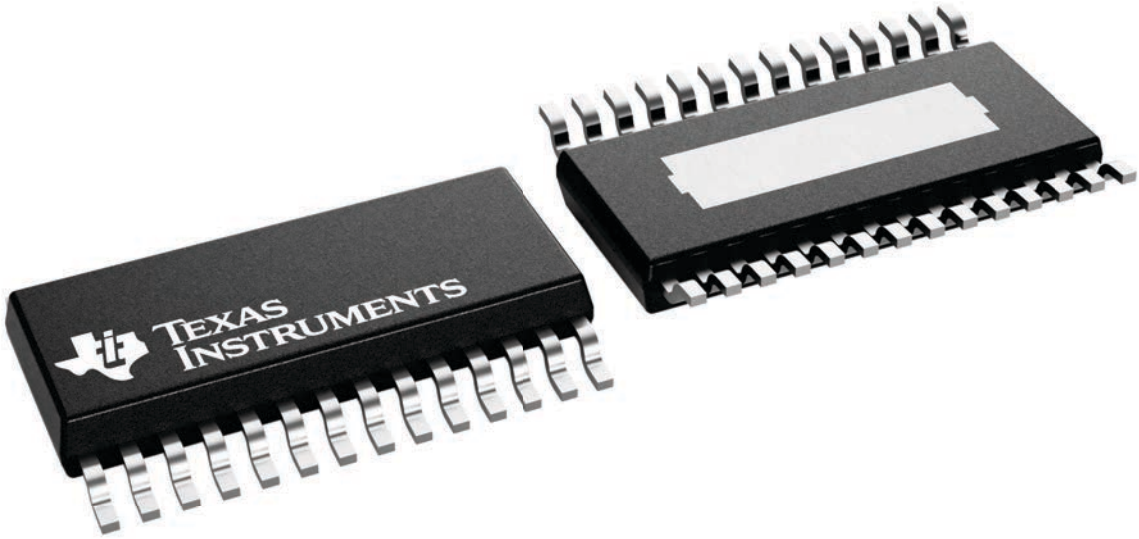
DGQ 28

HVSSOP - 1.1 mm max height

3 x 7.1, 0.5 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



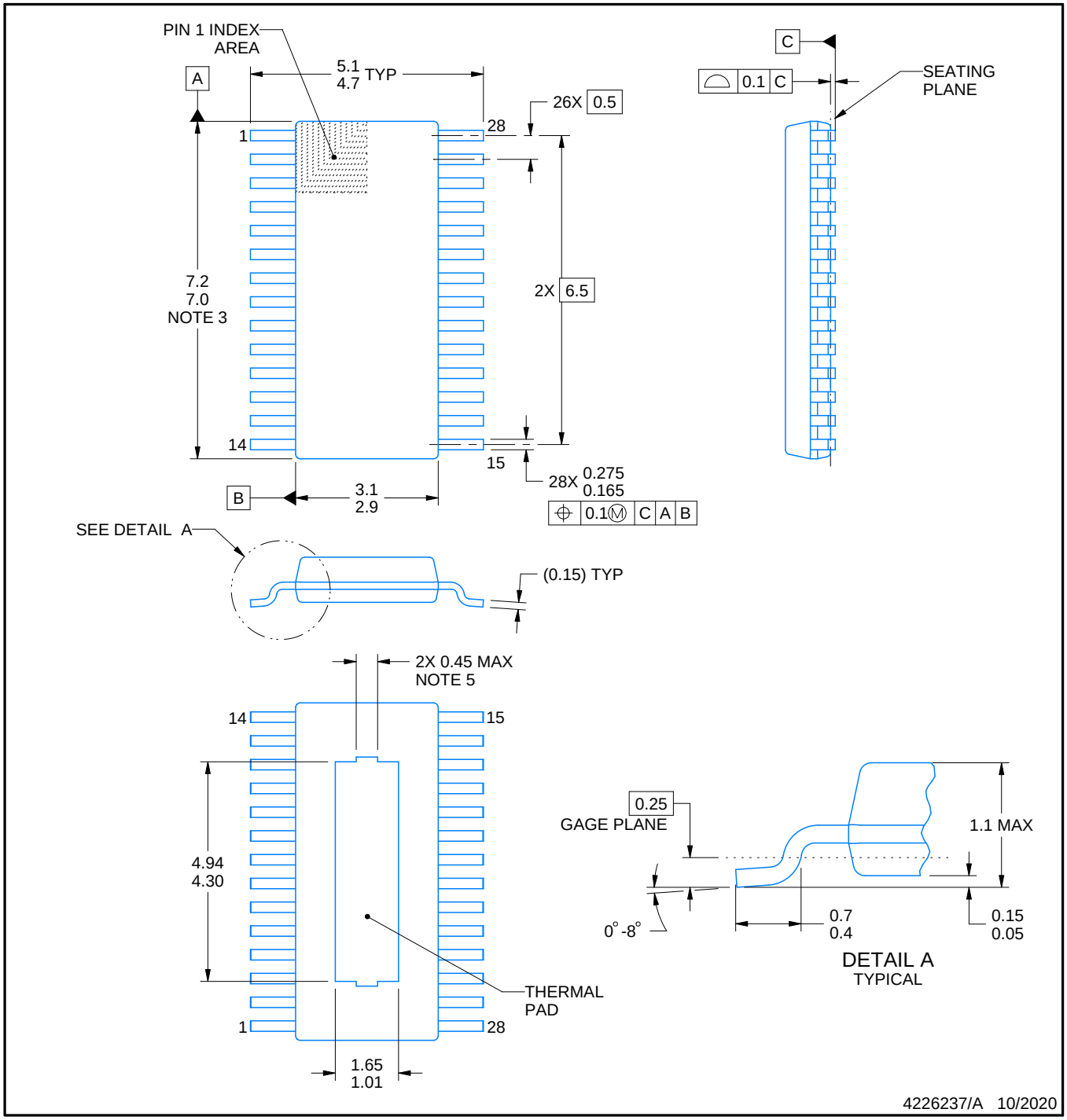
4226530/A

PACKAGE OUTLINE

DGQ0028A

PowerPAD™ VSSOP - 1.1 mm max height

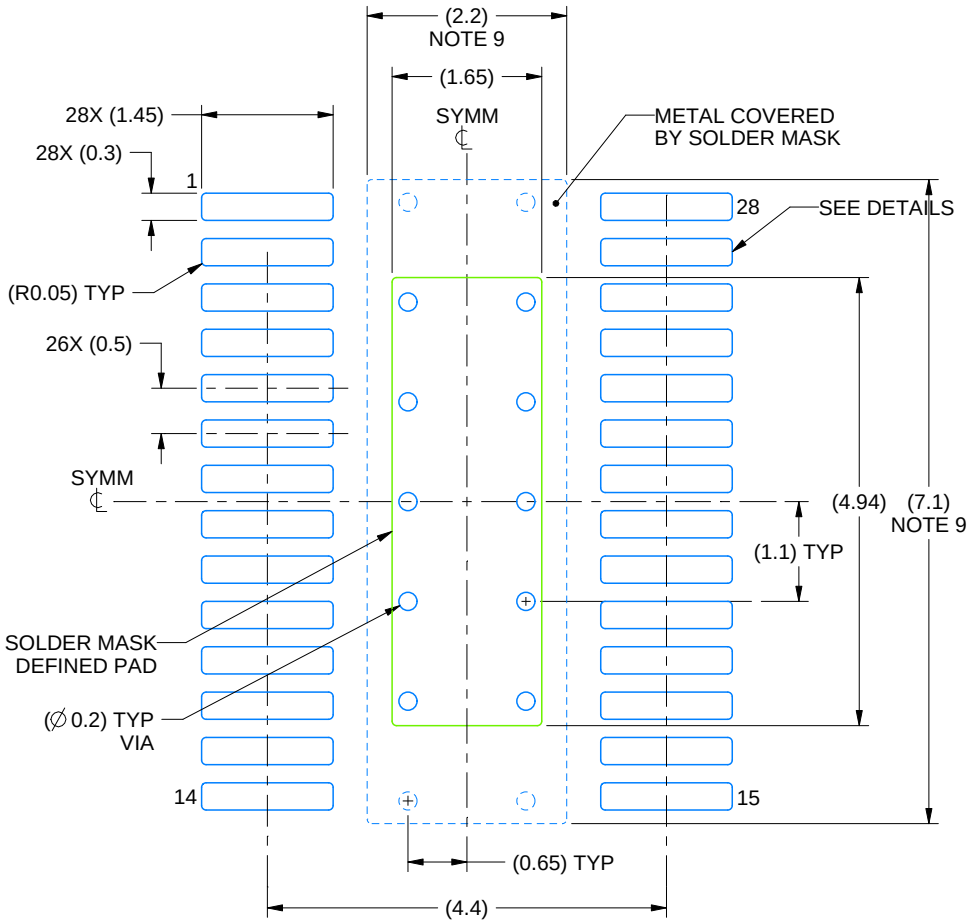
SMALL OUTLINE PACKAGE



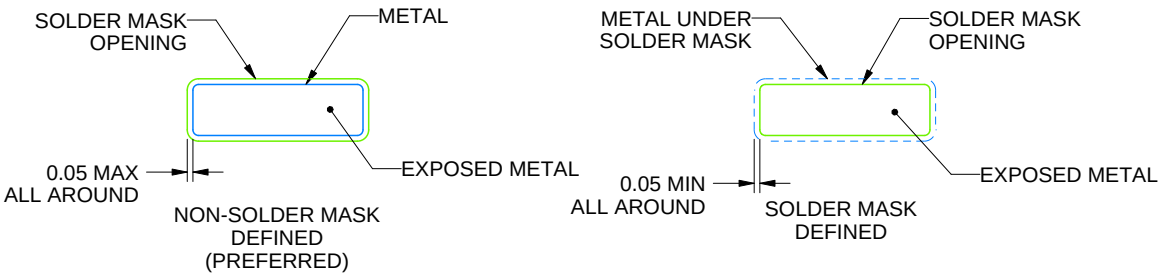
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

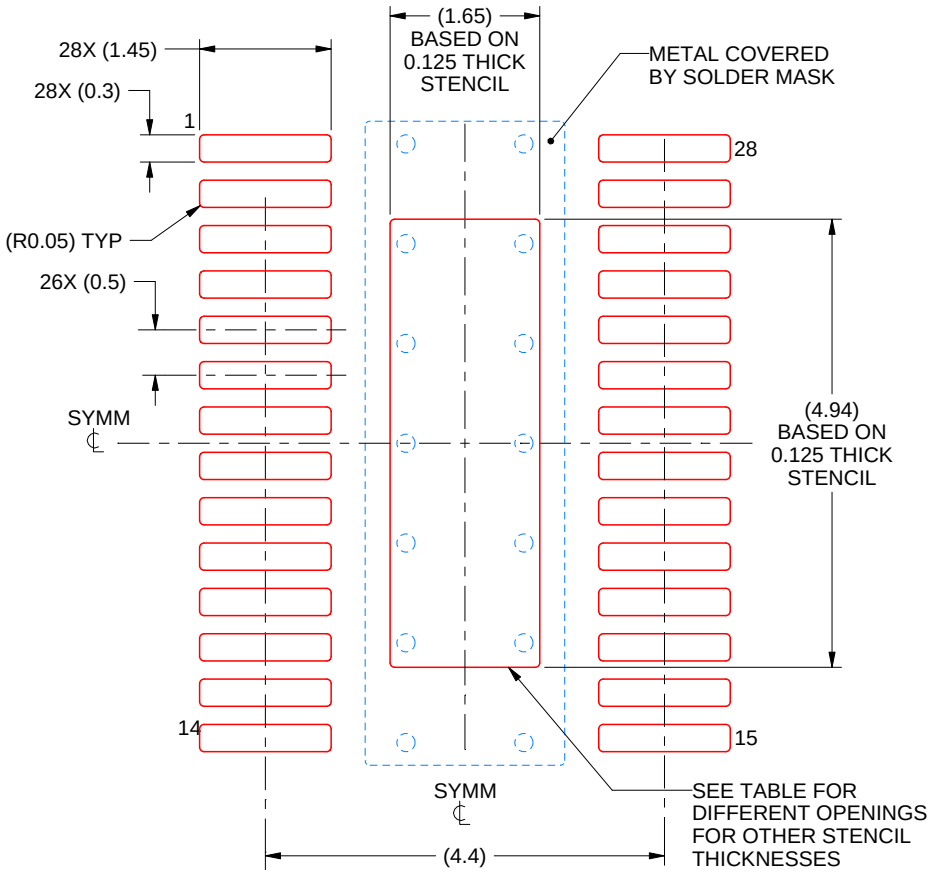


SOLDER MASK DETAILS

4226237/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.84 X 5.52
0.125	1.65 X 4.94 (SHOWN)
0.15	1.51 X 4.51
0.175	1.39 X 4.18

4226237/A 10/2020

NOTES: (continued)

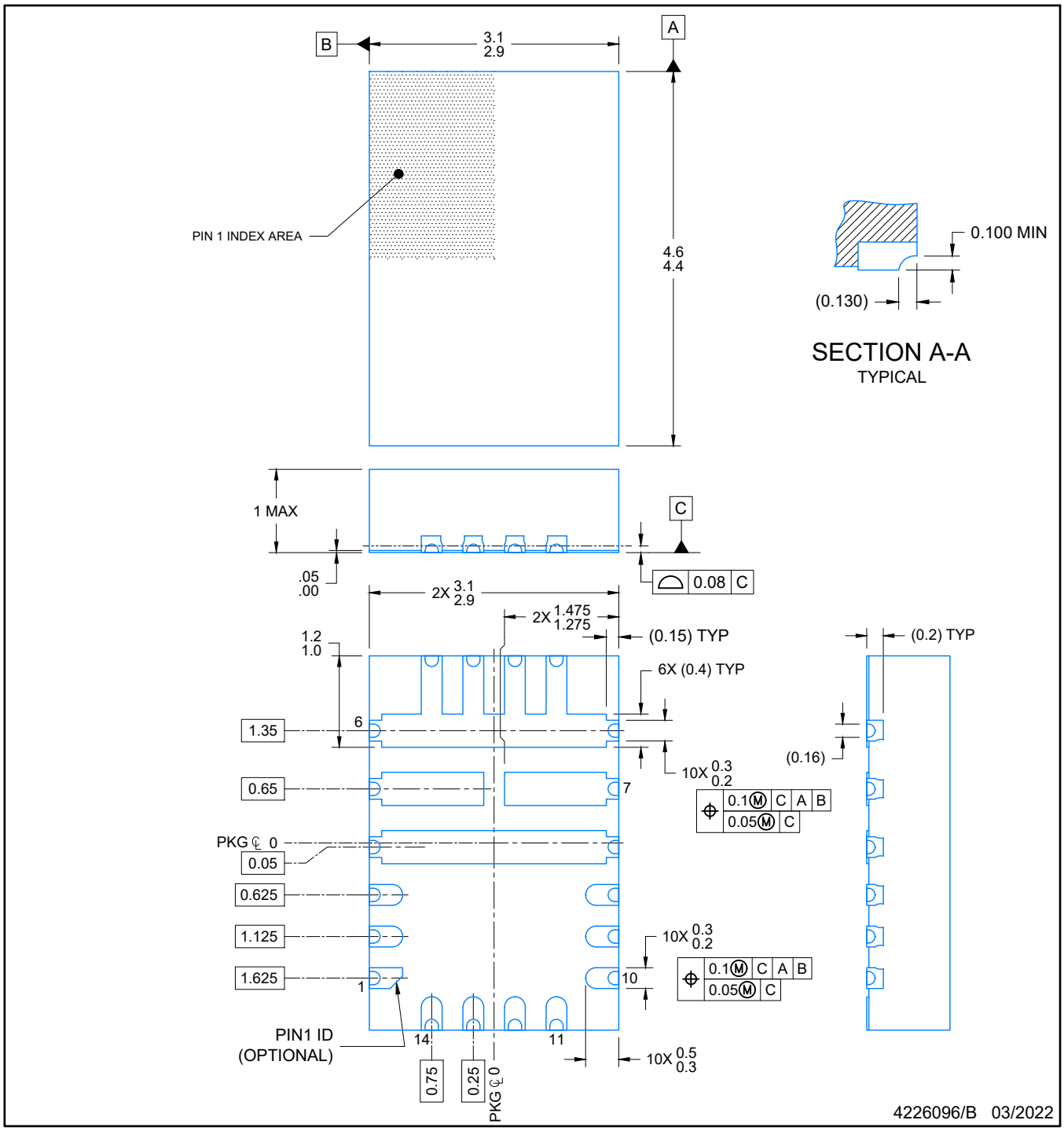
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

RXY0014A

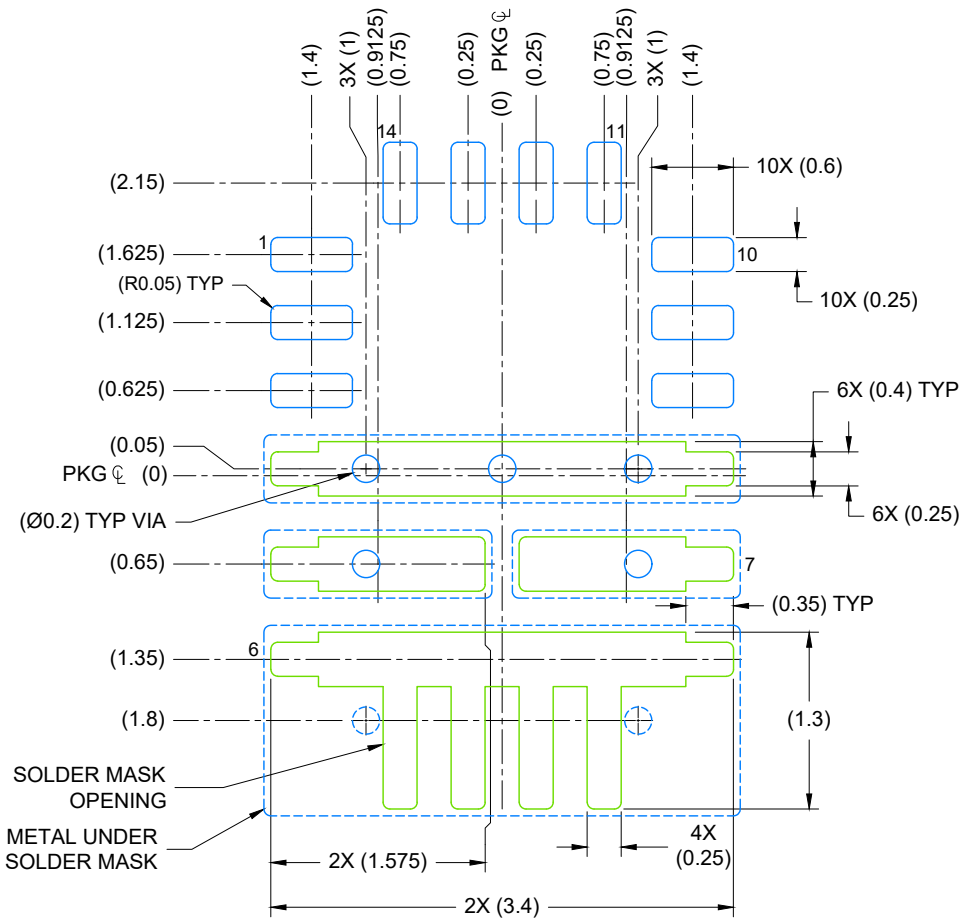
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

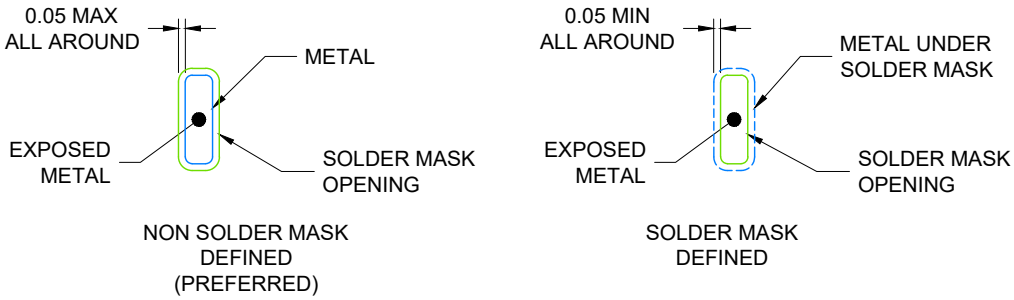
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 18X

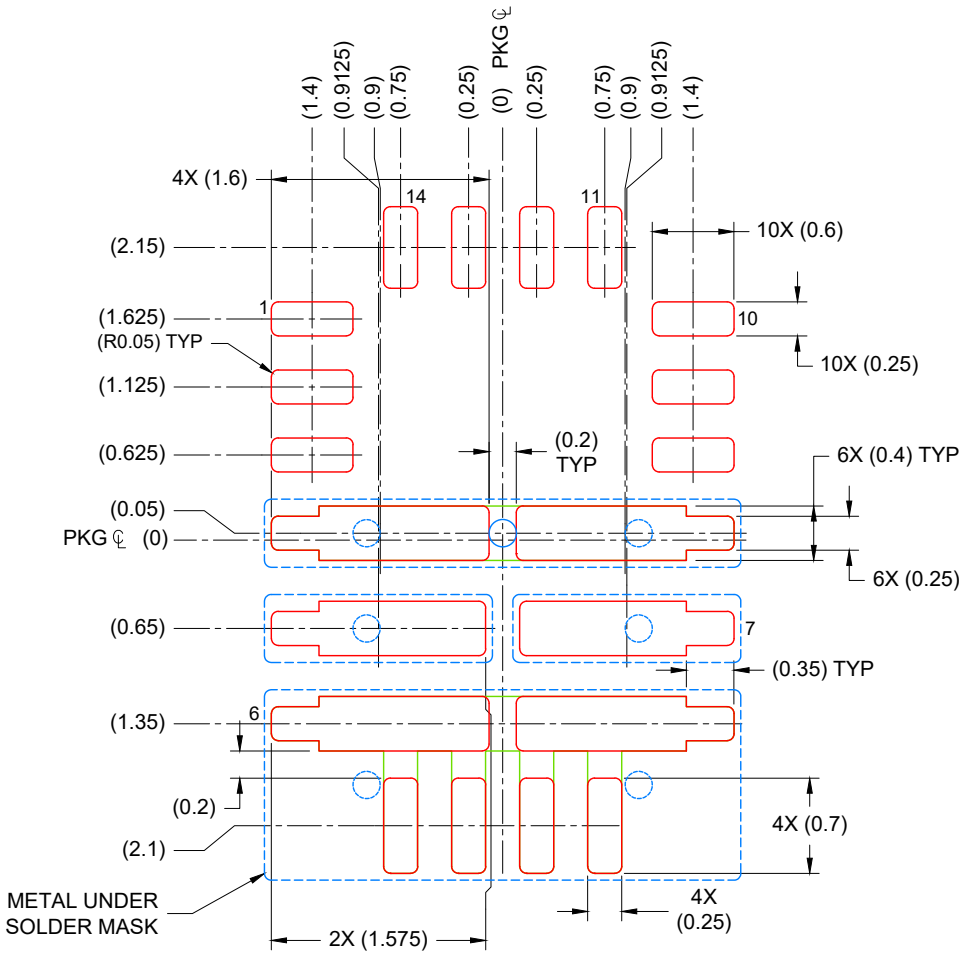


SOLDER MASK DETAILS

4226096/B 03/2022

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 18X

4226096/B 03/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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