DRV81545 Four-channel Low-side Driver with Integrated Protection Features

1 Features

- Four-channel integrated low-side switches
  - **235mΩ $R_{DS(ON)}$** at 25°C
  - Output Stage **55V operating max (60V abs max)**
  - **Integrated catch diodes** for flexible decay (external TVS/Zener) as alternate current path on switch turn-off
- Parallel interface for fast switching up to **250kHz**
- Fully protected
  - User settable **current limit**
  - **Independent overtemperature, overcurrent** protection for each switch
  - Configurable over-current **cut-off duration** (COD)
- Diagnostic feedback
  - MCU fault interrupt signal**(nFAULT)**
- **4.5V** to 55V operating supply voltage range
- Thermally enhanced surface mount package **(PWP20)**

2 Applications

- PLC
- Distributed I/O
- General relay and solenoid drive
- Textile machines

3 Description

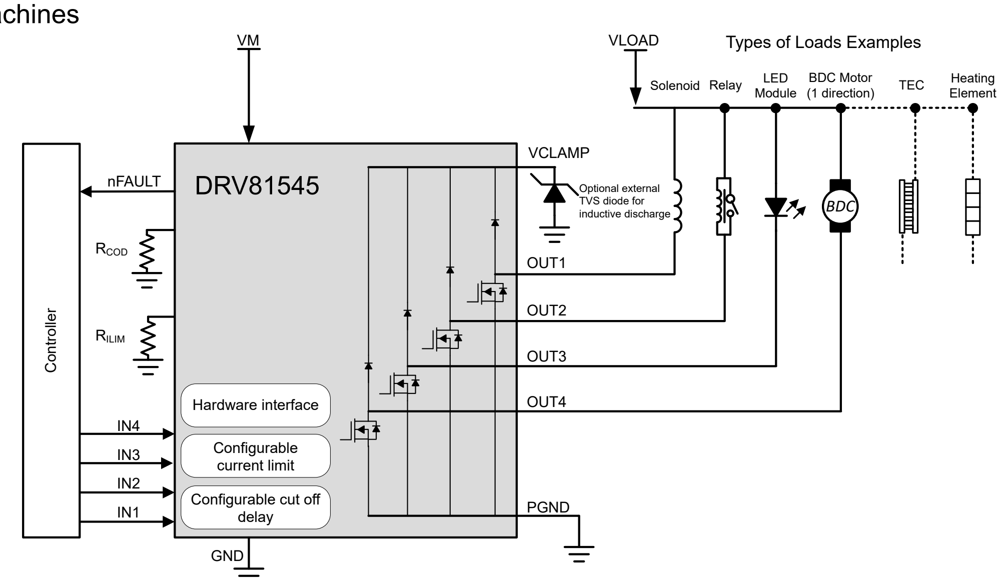
The DRV81545 is a four-channel low-side switch driver that operates from 4.5V to 55V and supports a wide range of load currents. The device integrates four low-side switches with a $R_{DS(on)}$ of 235mΩ, each with a freewheeling diode to the VCLAMP pin. This feature allows the user to either recirculate current or connect an external TVS for inductive load turn-off.

The device can be controlled through a hardware GPIO interface. Each channel features individual overtemperature protection, and an analog current limit adjustable with an external resistor on the ILIM pin. There is an optional cut-off duration (COD) configuration which limits the duration of a current-limiting condition on the respective channel, helping to prevent damage to the device or the load. Faults are indicated on a fault output pin (nFAULT).

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
DRV81545	PWP (HTSSOP, 20)	6.50mm × 6.40mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Pin Configuration and Functions

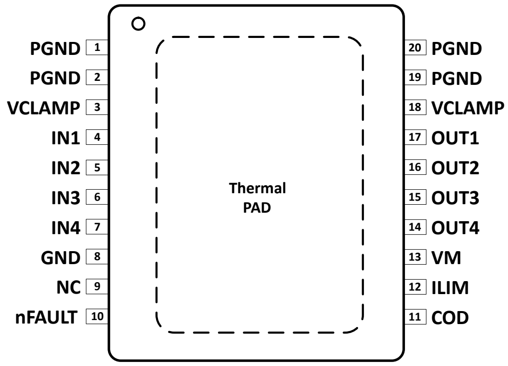

Figure 4-1. 20-Pin PWP Package, HTSSOP (Top View)

Table 4-1. Pin Functions

PIN			DESCRIPTION
NAME	PWP (20)	TYPE (1)	
POWER AND GROUND			
VM	13	PWR	Power supply. Bypass this pin to GND with a 0.1µF capacitor as well as sufficient bulk capacitance
VCLAMP	3, 18	PWR	Connect to VM supply, or zener diode to VM supply
GND	8	GND	Device ground. Connect to system ground.
PGND	1, 2, 19, 20	GND	Power ground. Connect to system ground.
THERMAL PAD	—	—	Thermal Pad. Connect to system ground. Connect to a continuous ground pour copper plane with direct-connect vias for the best thermal dissipation.
NC	9	—	Not connected
CONTROL			
ILIM	12	I	Current limit input. For details see Section 6.3.4.1. Connect a resistor between ILIM and GND to set the current limit threshold. Do not leave this pin unconnected. Connect directly to GND for the maximum current limit setting.
COD	11	I	Device configuration pin for Cutoff Delay. Connect to an appropriate resistor to GND to set the corresponding cut off delay. Connect directly to GND to disable this feature.
IN1	4	I	Controls the output of channel 1. For details, see the Hardware Interface section. Pin has internal pulldown resistor.
IN2	5	I	Controls the output of channel 2. For details, see the Hardware Interface section. Pin has internal pulldown resistor.
IN3	6	I	Controls the output of channel 3. For details, see the Hardware Interface section. Pin has internal pulldown resistor.
IN4	7	I	Controls the output of channel 4. For details, see the Hardware Interface section. Pin has internal pulldown resistor.
nFAULT	10	O	Open drain output. Pulled low when in fault condition. Connect pullup resistor to external logic supply.
OUTPUT			
OUT1	17	O	Connect to load 1
OUT2	16	O	Connect to load 2
OUT3	15	O	Connect to load 3

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Table 4-1. Pin Functions (continued)

PIN			DESCRIPTION
NAME	PWP (20)	TYPE (1)	
OUT4	14	O	Connect to load 4

(1) I = input, O = output, PWR = power, GND = ground

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5 Specification

5.1 Absolute Maximum Ratings

Over operating temperature range (unless otherwise noted)[1]

	PIN	MIN	MAX	UNIT
Power supply voltage	VM	–0.3	60	V
Output voltage	OUTx	–0.3	VCLAMP+0.3	V
Peak output current	OUTx		Internally limited	A
Clamp voltage	VCLAMP	–0.3	60	V
Continuous RMS current on VCLAMP (pins 3, 18 tied together)	VCLAMP		8	A
Transient current < 1ms on VCLAMP (pin 3, 18 tied together)	VCLAMP		20	A
OUTx FET recirculation diode current RMS or continuous	OUTx FET body diode		5	A
Digital input pin voltage	ILIM, INx	–0.5	5.5	V
Digital output current	nFAULT		10	mA
Digital output pin voltage	nFAULT	–0.5	7	V
Operating virtual junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–60	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

				MIN	NOM	MAX	UNIT
V_M	Power supply voltage			4.5		55	V
V_{CLAMP}	Output clamp voltage					55	V
I_{OUT}	Continuous output current (each channel)	PWP package, T_A = 25°C	1 channel on			2	A
	Continuous output current (each channel)		4 channels on			1	A
T_{AMB}	Operating Ambient temperature			-40		125	°C
T_J	Operating junction temperature			-40		150	°C

5.4 Thermal Information

THERMAL METRIC[1]		DRV81545 PWP (HTSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.2	°C/W

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THERMAL METRIC[(1)]		DRV81545 PWP (HTSSOP) 20 PINS	UNIT
Ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	13.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

4.5V ≤ V_{VM} ≤ 55V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted), Typical values at 24V, 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{VM}	VM operating supply current	V_M = 24V, No Switching			3	mA
		V_M = 24V, Output switching at 200kHz			5	mA
V_{UVLO}	VM undervoltage lockout voltage	V_M rising	4.1	4.25	4.45	V
		V_M falling	4.0	4.15	4.35	V
V_{UVLO_HYS}	VM undervoltage lockout hysteresis			100		mV
t_{UVLO}	VM undervoltage deglitch			10		µs
LOGIC-LEVEL INPUTS (INx)						
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage		2			V
V_{HYS}	Input hysteresis			0.4		V
I_{IL}	Input low current	V_{IN} = 0	–5		5	µA
I_{IH}	Input high current	V_{IN} = 3.3V		50	100	µA
OPEN-DRAIN OUTPUT (nFAULT)						
V_{OL}	Output low voltage for nFAULT	I_O = 5mA			0.1	V
I_{OH}	Output high leakage current for nFAULT	Pullup resistor to 5V			1	µA
SWITCHING						
t_R	Rise time OUTx rising from 10% to 90%	V_M = 24V, R_L = 48Ω, C_L = 0.1nF		200	300	ns
t_F	Fall time	V_M = 24 V; R_L = 48Ω C_L = 0.1nF , input fall time < 0.1 µs, Output falling 90% to 10% of final value		200	300	ns
t_{PD}	Input to output propagation delay	INx crossing 50% voltage to OUTx rising to 10% V_M = 24 V; R_L = 48Ω C_L = 0.1nF		300	500	ns
DRIVER OUTPUTS (OUTx)						
$R_{DS(ON)}$	FET on resistance	V_M = 24V, I_O = 500mA, T_J = 25°C		235		mΩ
		V_M = 24V, I_O = 500mA, T_J = 85°C			350	mΩ
I_{OFF}	Off-state leakage current	V_{OUT} = V_M = 24V		0.5		µA
I_{OFF}	Off-state leakage current	V_{OUT} = V_M = 55V			10	µA
V_F	Recirculation Diodes forward voltage	V_{OUT} = 24V, I_O = 500mA			1.2	V
I_{OFF}	Recirculation Diodes reverse leakage current	V_{OUT} = 0V, V_{CLAMP} = 55V			10	µA
PROTECTION CIRCUITS						

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5.5 Electrical Characteristics (continued)

$4.5V \le V_{VM} \le 55V$, $-40°C \le T_J \le 150°C$ (unless otherwise noted), Typical values at 24V, 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LIM}	Current limitation value Follows $60/R_{ILIM}[k\Omega]$ for $30k\Omega \le R_{ILIM} \le 120k\Omega$	R_{ILIM} short to GND or $R_{ILIM} < 20k\Omega$	3			A
		$R_{ILIM} = 30k\Omega$	1.4	2	2.6	A
		$R_{ILIM} = 60k\Omega$	0.7	1	1.3	A
		$R_{ILIM} = 90k\Omega$	0.4	0.66	0.8	A
		$R_{ILIM} = 120k\Omega$	0.3	0.5	0.7	A
$I_{LIM\_ACTIVATE}$	Current limit activation threshold	R_{ILIM} = Short to GND		3		A
		$R_{ILIM} = 30k\Omega$		3		A
		$R_{ILIM} = 60k\Omega$		1.5		A
		$R_{ILIM} = 90k\Omega$		1		A
		$R_{ILIM} = 120k\Omega$		0.75		A
t_{COD_DIS}	Cut off Delay disable threshold	Value of external resistor below which Cut off function is disabled			20	kΩ
t_{COD}	Cut off Delay Adjust with external resistor R_{COD} to GND Follows $R_{COD}[k\Omega]/120$ ±15% for $60k\Omega \le R_{COD} \le 240k\Omega$	$R_{COD} = 60k\Omega$	0.4	0.5	0.6	ms
		$R_{COD} = 120k\Omega$	0.8	1	1.2	ms
		$R_{COD} = 180k\Omega$	1.2	1.5	1.8	ms
		$R_{COD} = 240k\Omega$	1.6	2	2.4	ms
t_{RETRY}	Overcurrent protection retry time Adjust with external resistor R_{COD} to GND Follows $32*t_{COD}$ ±15% for $60k\Omega \le R_{COD} \le 240k\Omega$	$R_{COD} = 60k\Omega$		15.5		ms
		$R_{COD} = 120k\Omega$		31		ms
		$R_{COD} = 180k\Omega$		46.5		ms
		$R_{COD} = 240k\Omega$		62		ms
I_{VM_BREAK}	VM wire break power stage current	V_{INx} = VM =0V; V_{OUTx} = 24V, VCLAMP floating			10	µA
T_{TSD}	Thermal shutdown temperature	Die temperature	150	170	190	°C
T_{TSD_HYS}	Thermal shutdown temperature hysteresis			30		°C
t_{TSD_DG}	Thermal Shutdown deglitch			20		µs

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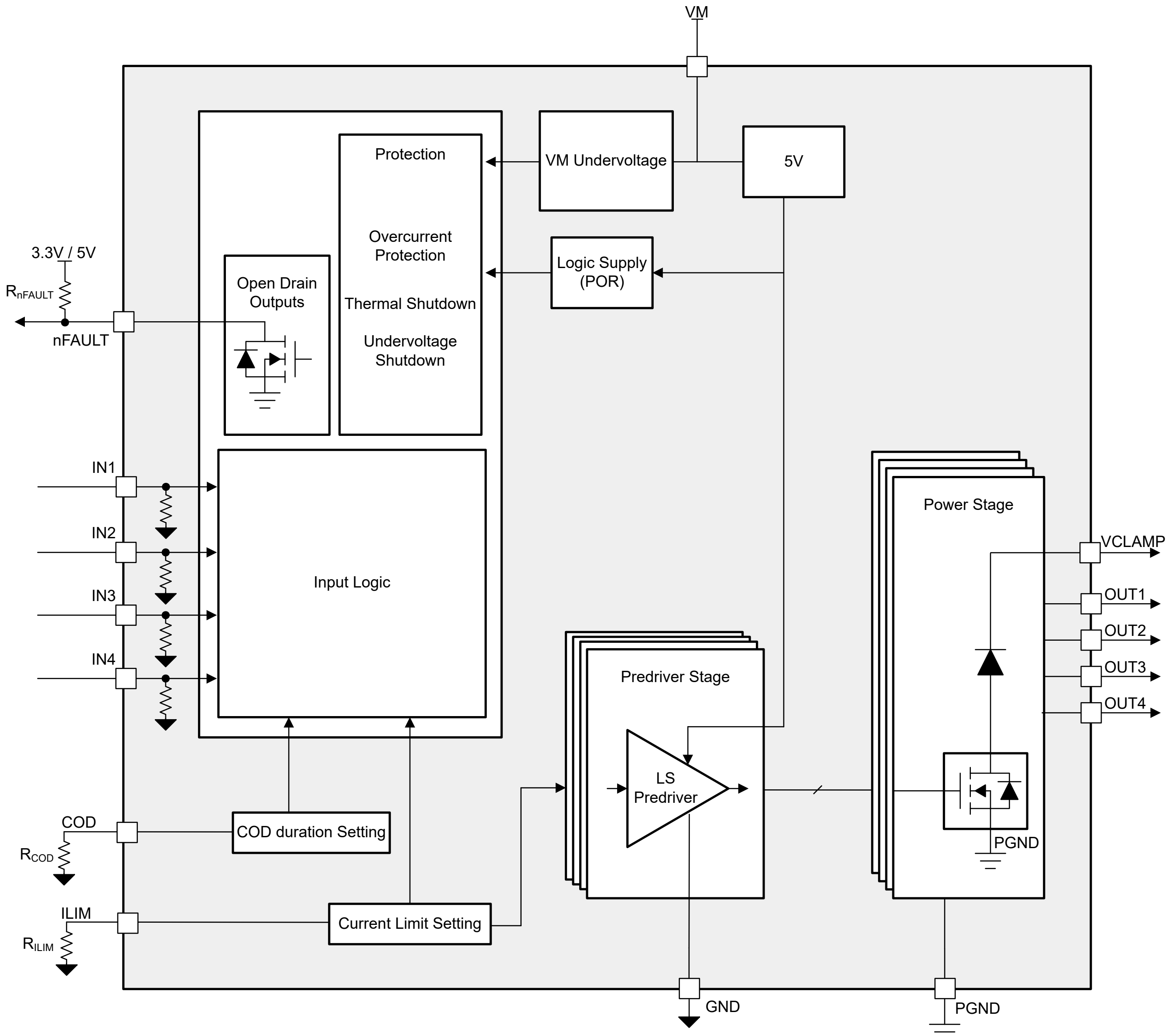
6 Detailed Description

6.1 Overview

The DRV81545 is a four-channel low-side switch driver that operates from 4.5V to 55V and supports a wide range of load currents. The device integrates four low-side switches with a $R_{DS(on)}$ of 235mΩ, each with a freewheeling diode to the VCLAMP pin. This feature allows the user to either recirculate current or connect an external TVS for inductive load turn-off.

The device can be controlled through a hardware GPIO interface. Each channel features individual overtemperature protection, and an analog current limit adjustable with an external resistor on the ILIM pin. There is an optional cut-off duration (COD) configuration which limits the duration of a current-limiting condition on the respective channel, helping to prevent damage to the device or the load. Faults are indicated on a fault output pin (nFAULT).

6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 Hardware Interface Operation

The DRV81545 can be controlled through a simple hardware interface where IN_X decides state of OUT_X. When the INx pin is driven high, internal logic switches on the corresponding output FET. Setting INx low switches off the corresponding OUTx FET. Table 6-1 illustrates this control scheme.

Table 6-1. Hardware Control Mode for Channel x

INx	OUTx	DESCRIPTION
0	Hi-Z	OUTx disabled (Hi-Z)
1	L	OUTx FET on

6.3.2 Integrated Clamp Diode, VCLAMP

The DRV81545 contains four protected low-side drivers. Each output has an integrated clamp diode connected to a common pin, VCLAMP.

VCLAMP can be connected to a Zener or TVS diode to VM or to GND, allowing the switch voltage to exceed the main supply voltage VM. This connection can be beneficial when driving loads that require very fast current decay. Because each output has a diode to the VCLAMP pin, the user can share a single external TVS diode for all 4 channels. Alternatively, VCLAMP can be connected directly to the main power supply voltage (VM).

In all cases, the voltage on the outputs must not be allowed to exceed the DRV81545 maximum output voltage specification. Below are some configurations which are supported by the DRV81545.

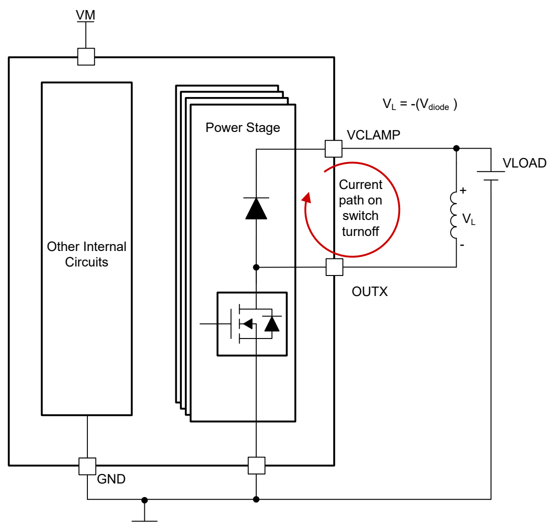

Figure 6-1. Slow Decay (VCLAMP Tied to VLOAD)

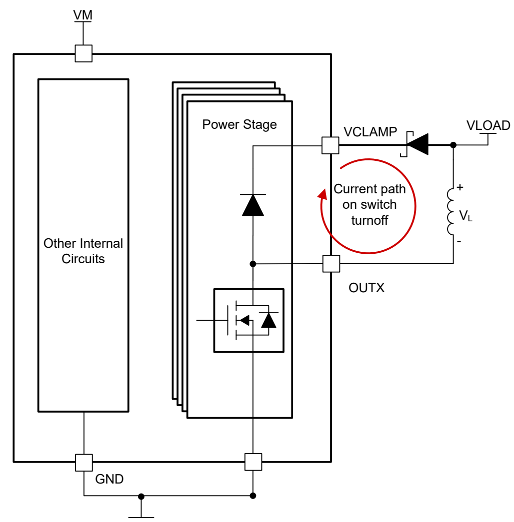

Figure 6-2. Fast Decay (TVS/Zener VCLAMP to VLOAD)

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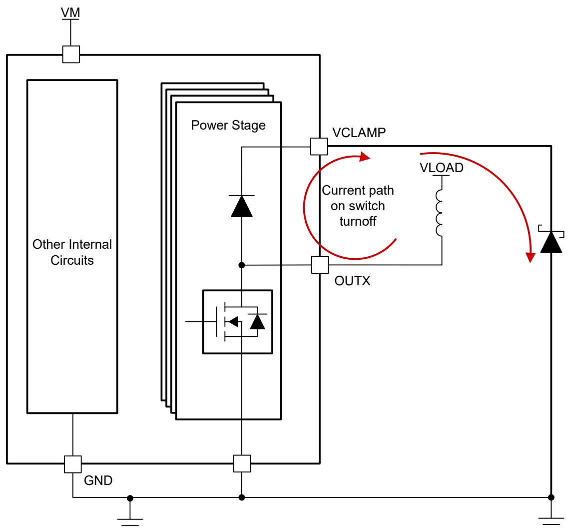

Figure 6-3. Fast Decay (TVS/Zener CLAMP to GND)

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Table 6-2. VCLAMP Decay Modes

VCLAMP CONNECTION	DECAY MODE	WHEN TO USE	V_L VOLTAGE
Directly to VLOAD	Slow Decay	Loads that do not need fast decay. Safe for the full VM operating range.	$V_L = -V_{diode}$
TVS or Zener to VLOAD	Fast Decay	Fastest current decay. Not recommended when VM or VLOAD > 28V due to chance of exceeding OUTx maximum voltage.	$V_L = -(V_{diode} + V_{zener})$
TVS or Zener to GND	Fast Decay	Lower clamping voltage than TVS to VLOAD, but slightly less fast current decay. TVS needs higher breakdown voltage than VLOAD to prevent leakage current.	$V_L = -(V_{diode} + V_{zener} - V_{LOAD})$

6.3.3 Parallel Outputs

Two outputs can be connected together in parallel for higher current. Figure 6-4 shows the schematic of DRV81545 driving two solenoid loads. The device also supports paralleling all four channels together.

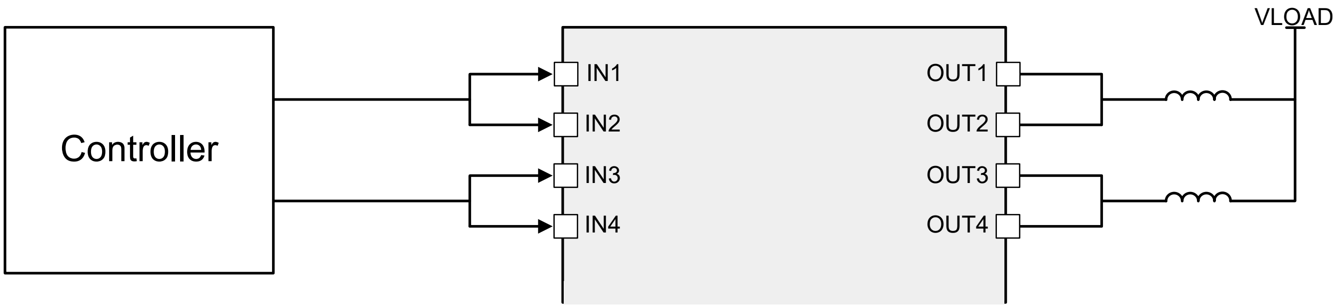

Figure 6-4. Drive Two Solenoids with Higher Current

Take care that the recirculation current on the VCLAMP pin does not exceed the absolute maximum ratings for continuous RMS current or transient current <1ms. PWM with a large inductive load can cause high current on VCLAMP.

6.3.4 Protection Circuits

The DRV81545 is protected from VM undervoltage, per-channel overtemperature, die overtemperature, and overcurrent events.

6.3.4.1 ILIM Analog Current Limit

The DRV81545 implements an analog current limit on each output as a protection against short circuits or capacitive loads with large inrush current. If the output stage sees a high-current condition $I > I_{LIM\_ACTIVATE}$, the FET gate drive voltage is reduced to regulate the output current at the I_{LIM} level. This gate drive adjustment operates the FET in the linear region, resulting in a much higher $R_{DS(ON)}$ and dissipating significant power. This current limiting feature (ILIM) is designed to be similar to overcurrent protection, but instead of completely shutting the FET off during an overcurrent event, the current is limited to a safe level until the device overheats.

Figures Figure 6-5 and Figure 6-6 show ILIM reducing the inrush current to a safe level before steady-state continuous current. This feature provides system-level benefits of reducing PCB trace width and reducing the system power supply capability requirements.

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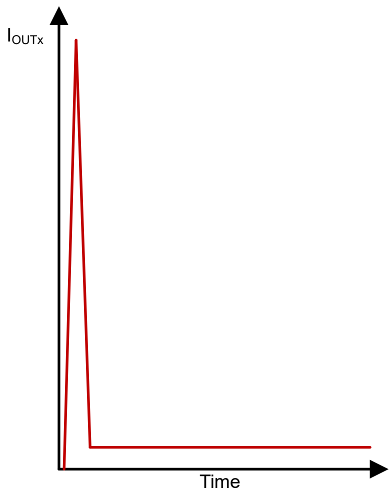

Figure 6-5. Inrush Current without ILIM

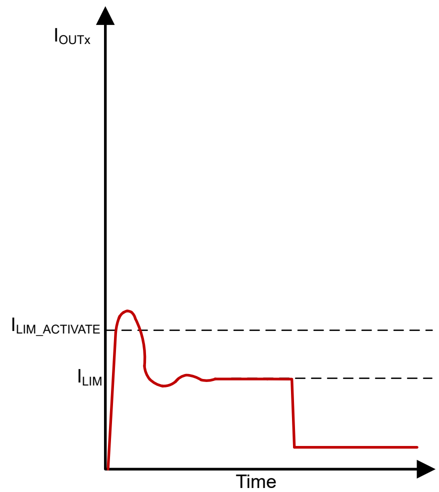

Figure 6-6. Inrush Current with ILIM Protection

The analog current limit level, I_{LIM}, can be configured with a pulldown resistor on the ILIM pin to GND as shown in Table 6-3. The same value of I_{LIM} is set for all four channels based on R_{ILIM}. The current limit condition on one channel does not affect other channels, unless there is an event such as a chip-wide over-temperature.

Table 6-3. Analog Current Limit Level Depending on ILIM Resistor

R_{ILIM} RESISTOR BETWEEN ILIM PIN AND GND	CURRENT LIMIT LEVEL, I_{LIM}
0 ≤ R_{LIM}< 20kΩ	3A
30kΩ ≤ R_{LIM} ≤ 120kΩ	I_{LIM}[A] = 60/R_{LIM}[kΩ]
R_{LIM}≥ 120kΩ	I_{LIM}[A] = 60/R_{LIM}[kΩ], can be non-linear

Figure 6-7 shows the active current limit during $t_{TIME\_TO\_TSD}$ during a short condition with cut-off delay disabled (0kΩ ≤ R_{COD} < 20kΩ). The cut-off delay feature is explained further in Section 6.3.4.2. After the channel shuts off, the channel retries only after the channel temperature returns to safe level (t_{TSD} – t_{TSD_HYS}). If the channel INx state changes during a I_{LIM} condition the controller responds to the input state change, such as shutting off the output. If the device has shut off due to TSD and the temperature is still above a safe level, the device does not respond to the input state change, meaning the devices does not turn the output back on if the device is still too hot, even if INx is toggled.

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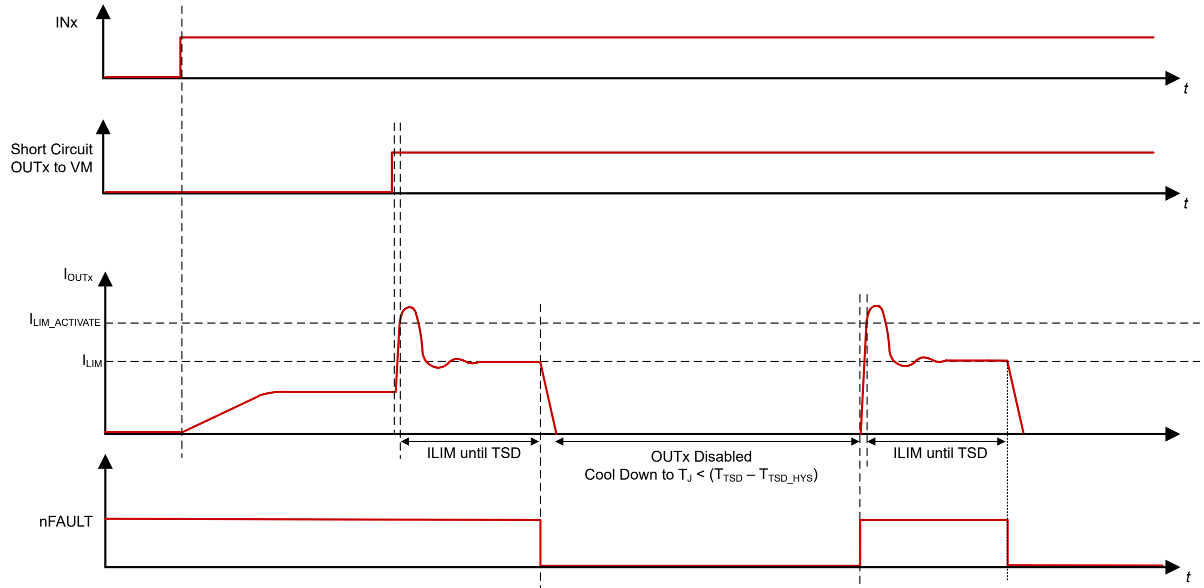

Figure 6-7. Current Limit Response to Short With Thermal Shutdown Based Retry (Cut-Off Delay Disabled)

Figure 6-8 shows a simplified schematic of the analog current limit circuit for each low-side FET.

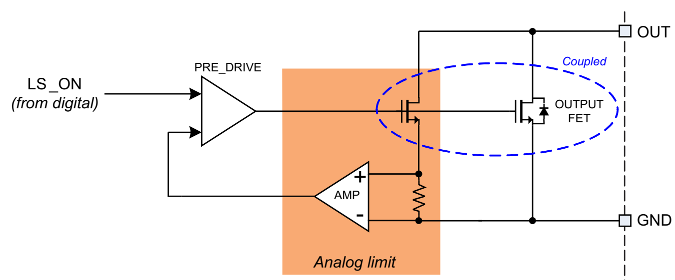

Figure 6-8. Analog Current Limit and Sensing Diagram

Effect of Load Resistance on Power Dissipation before TSD

The resistance of the load affects how long the channel can operate in the linear region before hitting thermal shutdown. The resistance functions similarly to a linear drop-out regulator (LDO), where a higher voltage drop requires the device to dissipate more power.

For example, take a 24V system with a 1A I_{LIM} setting for a 5Ω load versus an 11Ω load. Without current limiting these draw 4.8A and 2.2A respectively, but with the I_{LIM} feature, these regulate to 1A. Use the basic I = V / R to calculate the linear region resistance of the FET to achieve this 1A current limit:

$$I_{LIM} = V_{VM} / (R_{LOAD} + R_{DS(ON)}) \quad (1)$$

Rearrange Equation 1 to solve for $R_{DS(ON)}$, then plugging in our system values for loads 5Ω and 11Ω:

$$R_{DS(ON)} = (V_{VM} / I_{LIM}) - R_{LOAD} \quad (2)$$

$$R_{DS(ON)\_5\Omega} = (24V / 1A) - 5\Omega \rightarrow R_{DS(ON)\_5\Omega} = 19\Omega \quad (3)$$

$$R_{DS(ON)\_11\Omega} = (24V / 1A) - 11\Omega \rightarrow R_{DS(ON)\_11\Omega} = 13\Omega \quad (4)$$

Use this resistance to calculate the power dissipated inside the DRV81545 FET:

$$P_{FET\_5\Omega} = I^2 \times R = 1A^2 \times 19\Omega = 19W \tag{5}$$

$$P_{FET\_11\Omega} = I^2 \times R = 1A^2 \times 13\Omega = 13W \tag{6}$$

As you can see in the last equations above, even though both loads are limited to 1A, the DRV81545 has to dissipate more power for a 5Ω load than an 11Ω load. This power dissipation directly correlates with the temperature rise of the FET over time. More power dissipated means the channel hits thermal shutdown faster.

6.3.4.2 Cut-Off Delay (COD)

Since the analog current limit condition results in very high power dissipation, The DRV81545 offers a cut-off delay feature that controls the maximum length of an I_{LIM} or overcurrent condition. t_{COD} can be adjusted with a pull-down resistor on the COD pin as shown in Table 6-4.

Table 6-4. Cut-Off Delay (COD) Settings

R_{COD} RESISTOR BETWEEN COD PIN AND GND	FUNCTION BEHAVIOR	nFAULT PIN
$0 \le R_{COD} < 20k\Omega$	Cut-off delay function is disabled, Output stage and IC are protected by thermal shut down only	Pulled low when a channel hits thermal shutdown. Released when channel temperature returns to safe level
$60k\Omega \le R_{COD} \le 240k\Omega$	Current limit allowed to persist for $t_{COD} = R_{COD}(k\Omega)/120ms$ typical, before power stage shuts off	Pulled low when t_{COD} elapses. Released when t_{RETRY} elapses.
$R_{COD} \ge 240k\Omega$	$t_{COD} = R_{COD}(k\Omega)/120ms$, but linearity is not specified.	

For $60k\Omega \le R_{COD} \le 240k\Omega$, the device lasts in current limit condition for duration $t_{COD} = R_{COD}(k\Omega)/120$ ms. After the channel shuts off, the channel retries only after an interval of $t_{RETRY} = (t_{COD} \times 32)$ ms typical. If the user changes channel state during a current limit condition, the controller responds to the input state change. During t_{RETRY}, however, the controller does not respond to an input state change.

For $R_{COD} \ge 240k\Omega$ the same equation holds true, t_{COD} (ms) = $R_{COD}(k\Omega)/120$, but linearity is not specified.

If a thermal shutdown occurs during the COD interval, the channel turns off and retries once the temperature reaches safe level. The COD timer is paused for the duration the output turns off due to thermal shutdown.

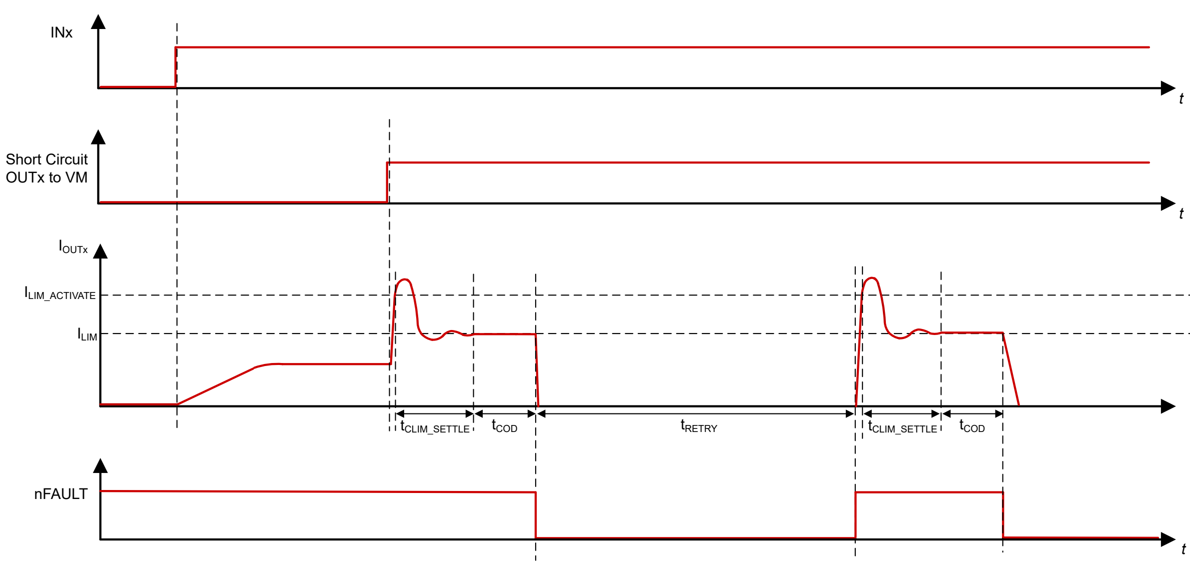

Figure 6-9. Current Limit Circuit Response to Short with COD Enabled

The cut-off delay-based timing of t_{COD} and t_{RETRY} feature reduces the average power dissipation compared to thermal-shutdown based retry. Without COD, the device recovers from thermal shutdown in 1-5ms at room temperature with one channel on. With COD, the device waits the full t_{RETRY} period before re-enabling the output. For example, let's calculate the average power dissipation per cycle with versus without COD for R_{ILIM}=100kΩ, V_{VM}=V_{LOAD} = 24V, R_{LOAD} = 1Ω

$$I_{LIM} = 60/R_{ILIM} = 60/100 = 0.6A \tag{7}$$

$$P_{OUTx\_ILIM} = V_{OUTx} \times I_{LIM} = (V_{LOAD} - I_{LIM} \times R_{LOAD}) \times I_{LIM} = (24V - 1\Omega \times 0.6A) \times 0.6A = 14.0W \tag{8}$$

With cut-off delay enabled (60kΩ ≤ R_{COD} ≤ 240kΩ) the average current depends on the t_{COD} and the t_{RETRY} = t_{COD} × 32ms. For R_{COD} = 120kΩ

$$t_{COD} = R_{COD}[k\Omega]/120 = 120/120 = 1ms \tag{9}$$

$$t_{RETRY} = t_{COD} * 32 = 1ms \times 32 = 32ms \tag{10}$$

$$P_{COD\_AVERAGE} = (P_{OUTx\_ILIM} \times t_{COD}) / (t_{COD} + t_{RETRY}) = (14.0W \times 1ms) / (1ms + 32ms) = 0.43W \tag{11}$$

Without cut-off delay (COD pin connected to GND, or R_{COD} < 20kΩ) the device automatically retries after thermal hysteresis (T_J < (t_{TSD} – t_{TSD_HYS}). Calculate the average power dissipation using a retry time of $t_{TSD\_HYS\_RETRY}$ = 2.5ms and the same 1ms on-time as if the device thermal shutdown after t_{TSD} = 1ms:

$$P_{ILIM\_AVERAGE} = (P_{OUTx\_ILIM} \times t_{TSD}) / (t_{TSD} + t_{TSD\_HYS\_RETRY}) = (14.0W \times 1ms) / (1ms + 2.5ms) = 4W \tag{12}$$

Cut-off delay results in a significantly lower average power dissipation (0.43W in this example) than thermal-shutdown based protection (4W in this example). This result leads to lower overall system heating and better performance on adjacent device channels.

6.3.4.3 Thermal Shutdown (TSD)

A dedicated thermal sensor is placed close to each power FET. When a channel encounters an overtemperature condition, the corresponding power FET is disabled and the NFAULT pin is asserted low. The thermal protection of the four output power stages is independent.

If the die temperature exceeds safe limits, all output FETs are disabled and the nFAULT pin is driven low. After the die temperature has fallen to a safe level, operation automatically resumes.

6.3.4.4 Undervoltage Lockout (UVLO)

Whenever the voltage on the VM pin falls below the UVLO falling threshold voltage, V_{UVLO}, all circuitry in the device is disabled, the output FETS are disabled, and all internal logic is reset. Operation continues when the V_{VM} voltage rises above the UVLO rising threshold, as shown in Figure 6-10

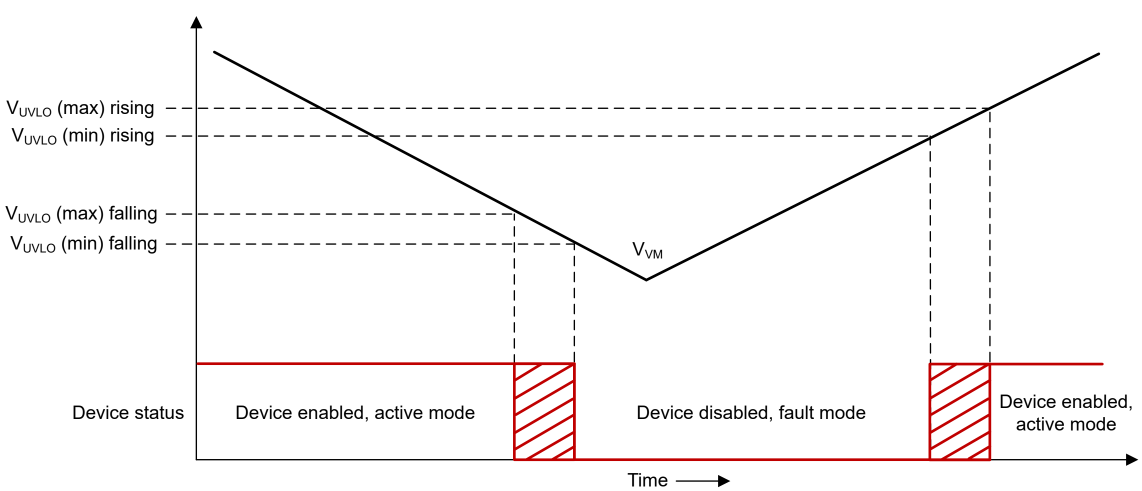

Figure 6-10. VM UVLO Operation

6.3.4.5 Fault Conditions Summary

FAULT	NFAULT PIN	RECOVERY
Channel Overtemperature, $T_{J\_CHx} > T_{TSD}$	High	$T_J < (T_{TSD} – T_{TSD\_HYS})$
	Pulled Low	
Global (Die) Overtemperature, $T_J > T_{TSD}$	Pulled Low	$T_J < (T_{TSD} – T_{TSD\_HYS})$
COD time expiry, when COD enabled	Pulled Low	t_{RETRY} elapses
VM Undervoltage (UVLO), $V_{VM} < V_{UVLO}$ VM falling	Internal circuits disabled	$V_{VM} > V_{UVLO}$ VM rising

ADVANCE INFORMATION

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The DRV81545 is a quad channel low side that can be used to drive loads to ground such as bulbs, coils, unipolar BDC motors, capacitive loads like LED modules. Channels can be paralleled to drive higher current. For inductive loads that need PWM type control, the DRV81545 also integrates catch diodes from OUT to VCLAMP that can be used to recirculate current for a slow decay. For fast turn-off the user can connect a breakdown Zener at the VCLAMP pin for a fast decay of current in an Inductive load.

7.2 Typical Application

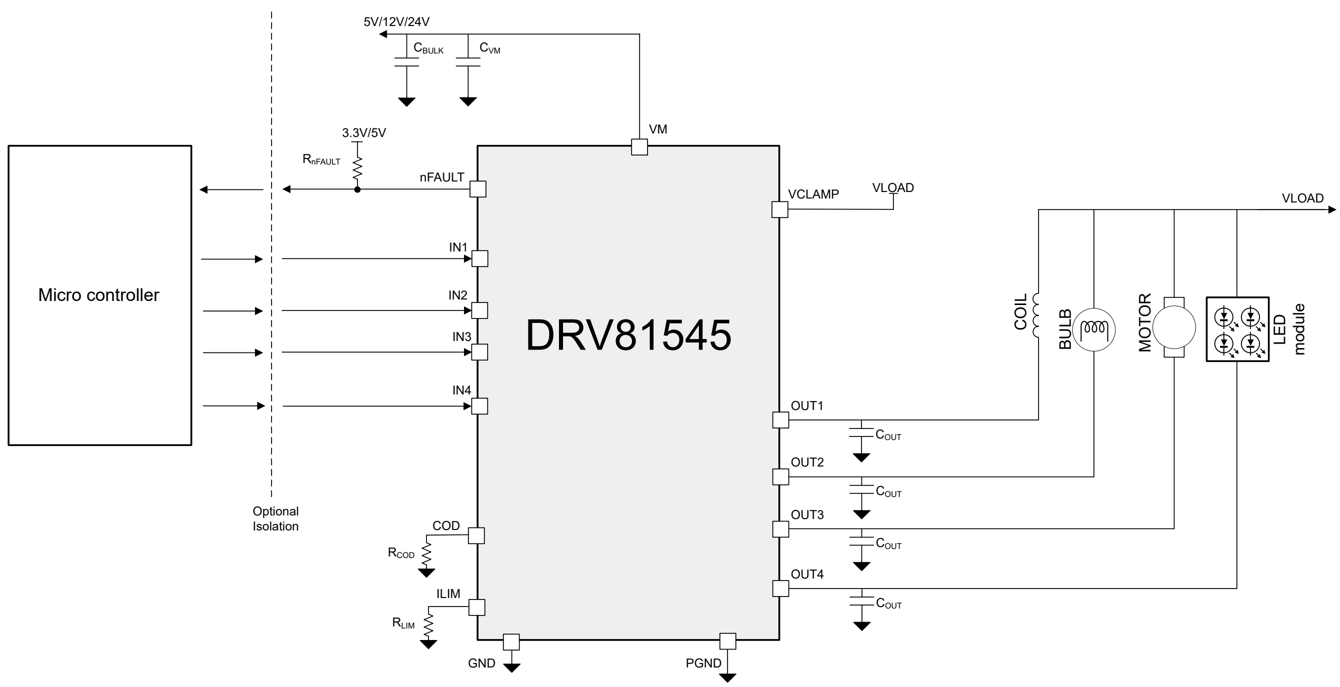

Figure 7-1. Typical Application Schematic

Figure 7-1 shows the application schematic of the DRV81545. VLOAD and VM can be tied together, or can be different voltages as long as the voltages do not exceed any pin absolute maximum ratings.

7.2.1 Suggested External Components

Table 7-1 lists the recommended external components for the DRV81545.

Table 7-1. Suggested External Components

SYMBOL	DESCRIPTION	VALUE	PURPOSE
C_{VM}	Capacitor on VM	1uF	Supply voltage filtering
C_{BULK}	Bulk capacitor on VM	47uF – 100uF	Supply voltage inrush and ripple smoothing
R_{COD}	Pulldown resistor on COD pin	Set a pulldown resistor based on desired cut-off delay	

Table 7-1. Suggested External Components (continued)

SYMBOL	DESCRIPTION	VALUE	PURPOSE
R_{ILIM}	Pulldown resistor on ILIM pin	Set a pulldown resistor based on current limit desired	
R_{nFAULT}	Pullup resistor to logic voltage on open-drain nFAULT pin	10kΩ	Bias the nFAULT voltage to high when the pin is not pulled low

Table 7-2. Optional External Components

SYMBOL	DESCRIPTION	VALUE	PURPOSE
C_{OUT}	Capacitor on each OUTx to GND	10nF	Filtering for system level ESD
TVS_{SURGE}	Surge diode on VCLAMP pin	TVS3300	Protection against system level voltage surge and for inductive demagnetization
$U_{ISOLATION}$	Quad-channel digital isolator for INx	INx control: ISO6440	Provide electrical isolation between rest of the circuit and the DRV81545

7.2.2 Detailed Design Procedure

7.2.3 Power Dissipation

Power dissipation in the DRV81545 device is dominated by the power dissipated in the output FET resistance, or $R_{DS(on)}$. Average power dissipation of each FET when running a static load can be roughly estimated by Equation 13:

$$P = R_{DS(ON)} \bullet (I_{OUT})^2 \tag{13}$$

where

- P is the power dissipation of one FET
- $R_{DS(ON)}$ is the resistance of each FET
- I_{OUT} is equal to the average current drawn by the load.

At start-up and fault conditions, this current is much higher than normal running current; consider these peak currents and duration. When driving more than one load simultaneously, the power in all active output stages must be summed.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases. Take this action into consideration when sizing the heatsink.

ADVANCE INFORMATION

7.3 Application Curves

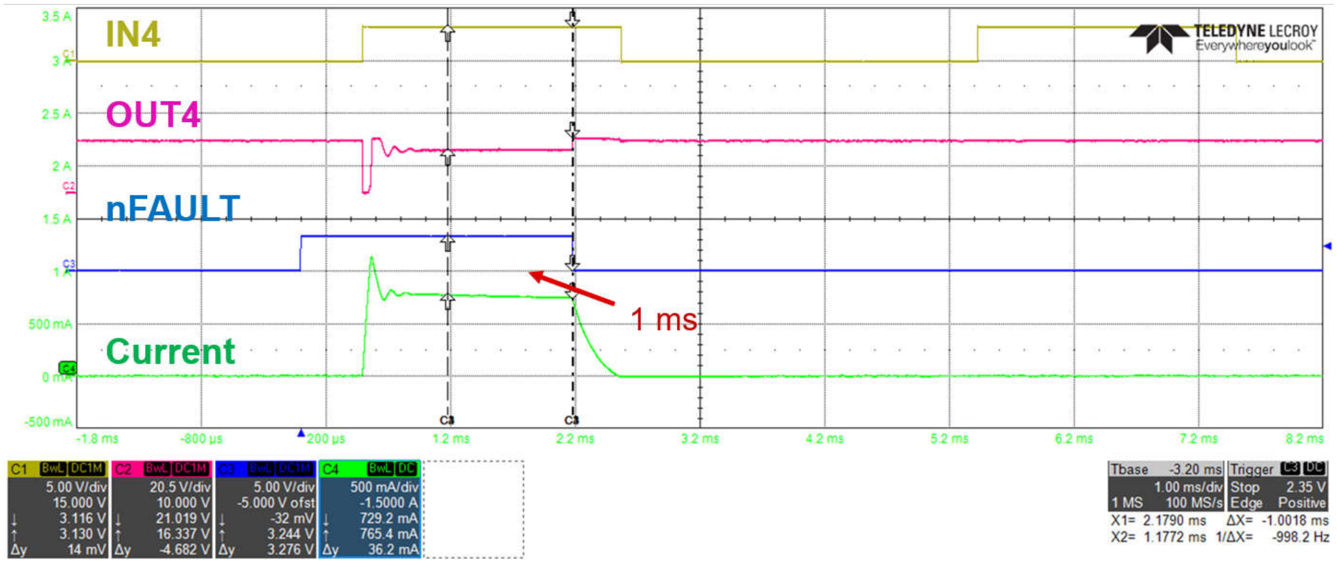

Figure 7-2. t_{COD} = 1ms with R_{COD} = 120kΩ, 12V, 12Ω Load, VCLAMP Shorted to VM

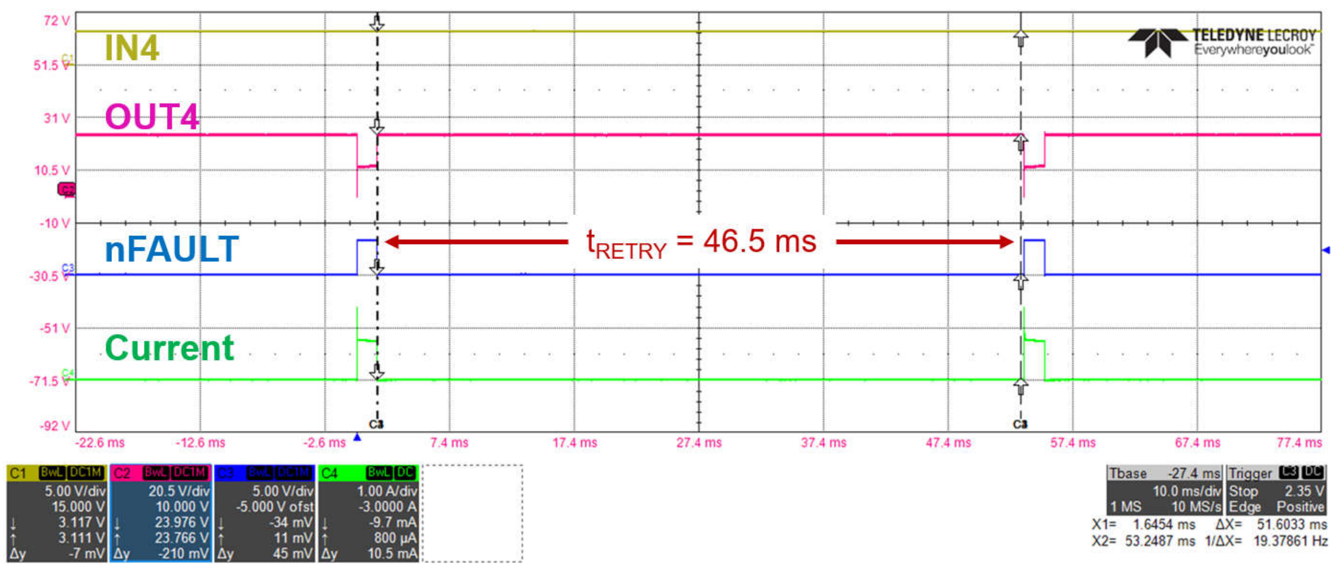

Figure 7-3. t_{RETRY} = 46.5ms with Cut-Off Delay (COD) Enabled, R_{COD} = 180kΩ, 12V, 12Ω 1mH Load, VCLAMP Shorted to VM

7.4 Power Supply Recommendations

7.4.1 Bulk Capacitance

Appropriate local bulk capacitance is an important factor in motor drive system design. Having more bulk capacitance is generally beneficial, although the disadvantages include increased cost and physical size. Bulk capacitors near the motor driver act as a local reservoir of electrical charge to smooth out the motor current variation.

Experienced engineers often use general guidelines about bulk capacitance to select the capacitor values. One such guideline says to use at least 1 to 4µF of capacitance for each Watt of motor power. For example, a solenoid which draws 4 Amps from a 24V supply has a power of 96 Watts, leading to bulk capacitance of 96 to 384µF, using this general guideline.

The voltage rating for bulk capacitors must be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

A large value of bulk capacitance is desired to provide a constant VM supply voltage during current transitions, such as solenoid start-up, changes in load torque, or PWM operation. A working estimate of the required capacitance for consistent supply is essential to reduce complexity, cost and size of board electronics. We can use a general guideline method to find an appropriate capacitor size based on the expected load current variation and allowable motor supply voltage variation:

$$C_{BULK} > k \times \Delta I_{MOTOR} \times T_{PWM} / \Delta V_{SUPPLY} \quad (14)$$

Where:

C_{BULK} is the bulk capacitance

k is a scale factor to account for the ESR for typical capacitors in this type of application; based on the lab measurements with DRV8718-Q1EVM, k ≈ 3 is practical for these cases.

ΔI_{MOTOR} is the expected variation in motor current, $i_{max} – i_{min}$

T_{PWM} is the PWM period which is the reciprocal of the PWM frequency

ΔV_{SUPPLY} is the allowable variation in the motor supply voltage.

Figure 7-4 plots several data points and applies this general guideline, showing relatively good agreement.

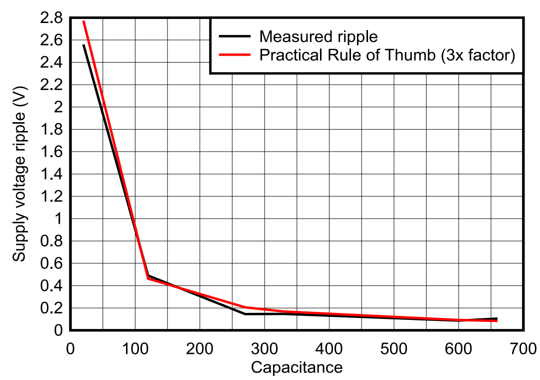

Figure 7-4. Measured Results and 3 × General Guideline, Accounting for Real-World Non-Zero ESR Values of Electrolytic Capacitors

See also the *Bulk Capacitor Sizing for DC Motor Drive Applications* application note.

7.5 Layout

7.5.1 Layout Guidelines

- Place the bulk capacitor to minimize the distance of the high-current path through the motor driver device. Make the connecting metal trace widths as wide as possible, and numerous vias must be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.
- Use wide metal traces for the high-current device outputs.
- The VM pins are bypassed to GND pins using low-ESR ceramic bypass capacitors with a recommended value rated for VM. The capacitors are placed as close to the VM pins as possible with a thick trace or ground plane connection to the device VNEG pins.
- In general, inductance between the power supply pins and decoupling capacitors must be avoided.
- The thermal PAD of the package must be connected to system ground.
  - Try to use a big unbroken single ground plane for the whole system / board. The ground plane can be made at bottom PCB layer. Figure 7-5 shows an example of temperature rise from constricted versus continuous ground pours underneath the driver.

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- To minimize the impedance and inductance, the traces from ground pins are as short and wide as possible, before connecting to bottom layer ground plane through vias.
- Use multiple vias to reduce the impedance.
- Try to clear the space around the device as much as possible especially at bottom PCB layer to improve the heat spreading.
- Single or multiple internal ground planes connected to the thermal PAD also help spread the heat and reduce the thermal resistance.

- For more layout guidelines and best practices see the *Best Practices for Board Layout of Motor Drivers* application note.

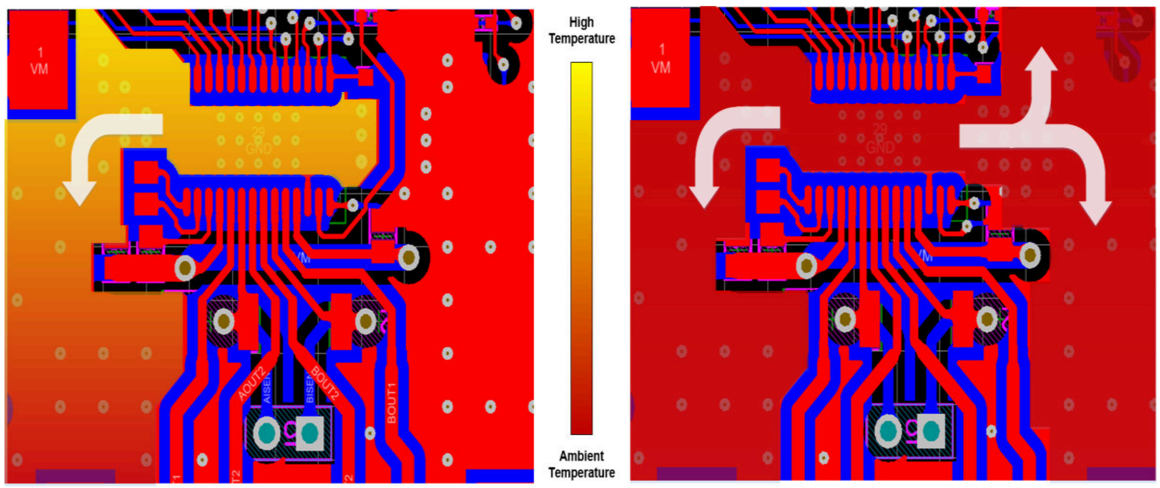

Figure 7-5. Broken Ground vs Continuous Ground Pour Heat Map

7.5.2 Layout Example

Follow the layout example see the evaluation module (EVM). The Altium design files can be downloaded from the DRV81545EVM product folder.

ADVANCE INFORMATION

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *PowerPAD Thermally Enhanced Package* application note
- Texas Instruments, *PowerPAD Made Easy* application note
- Texas Instruments, *Best Practices for Board Layout of Motor Drivers* application note
- Texas Instruments, *Bulk Capacitor Sizing for DC Motor Drive Applications* application note

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Trademarks

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2025	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

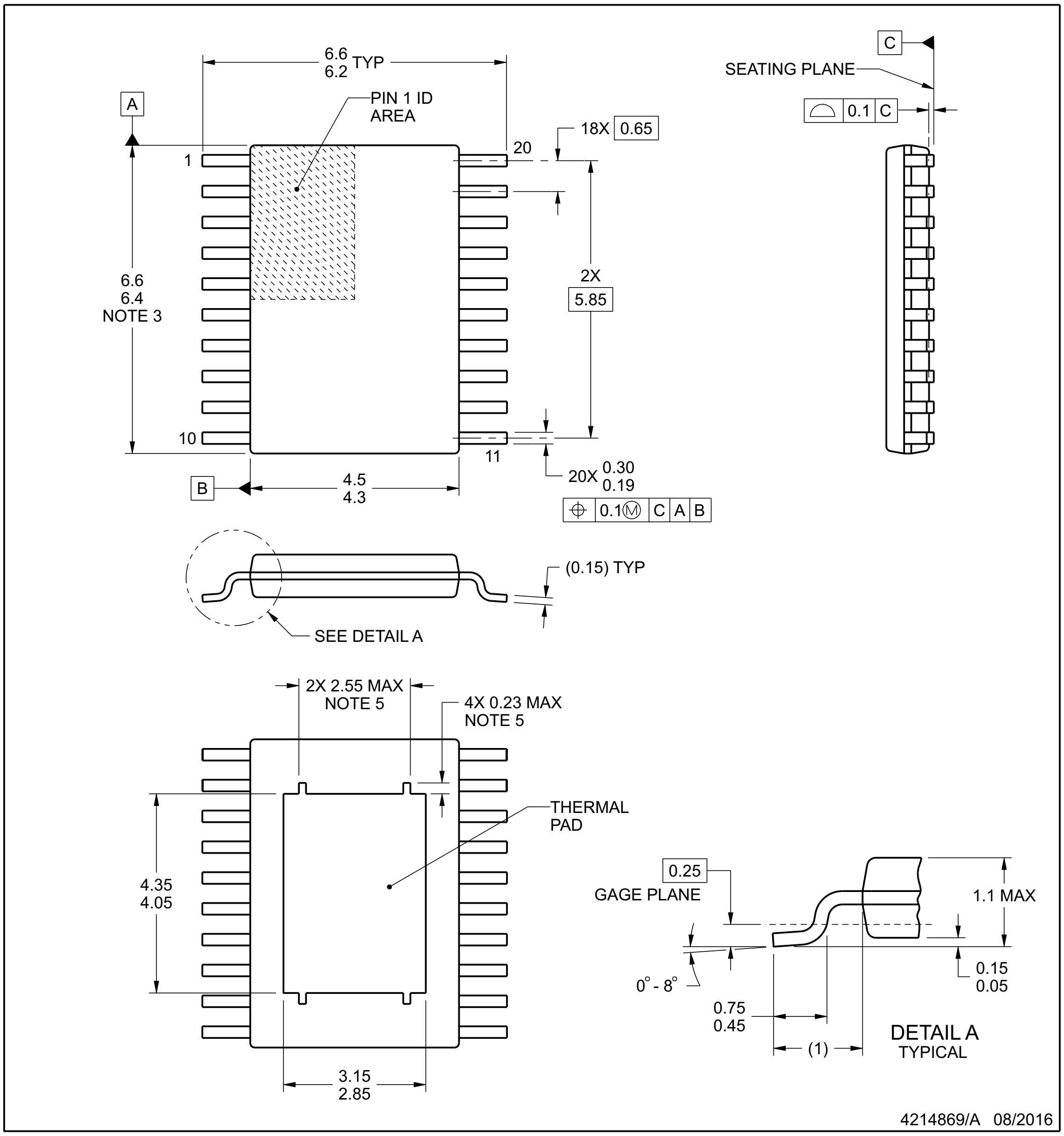
ADVANCE INFORMATION

PACKAGE OUTLINE

PWP0020A

PowerPAD™ TSSOP - 1.1 mm max height

PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

NOTES:

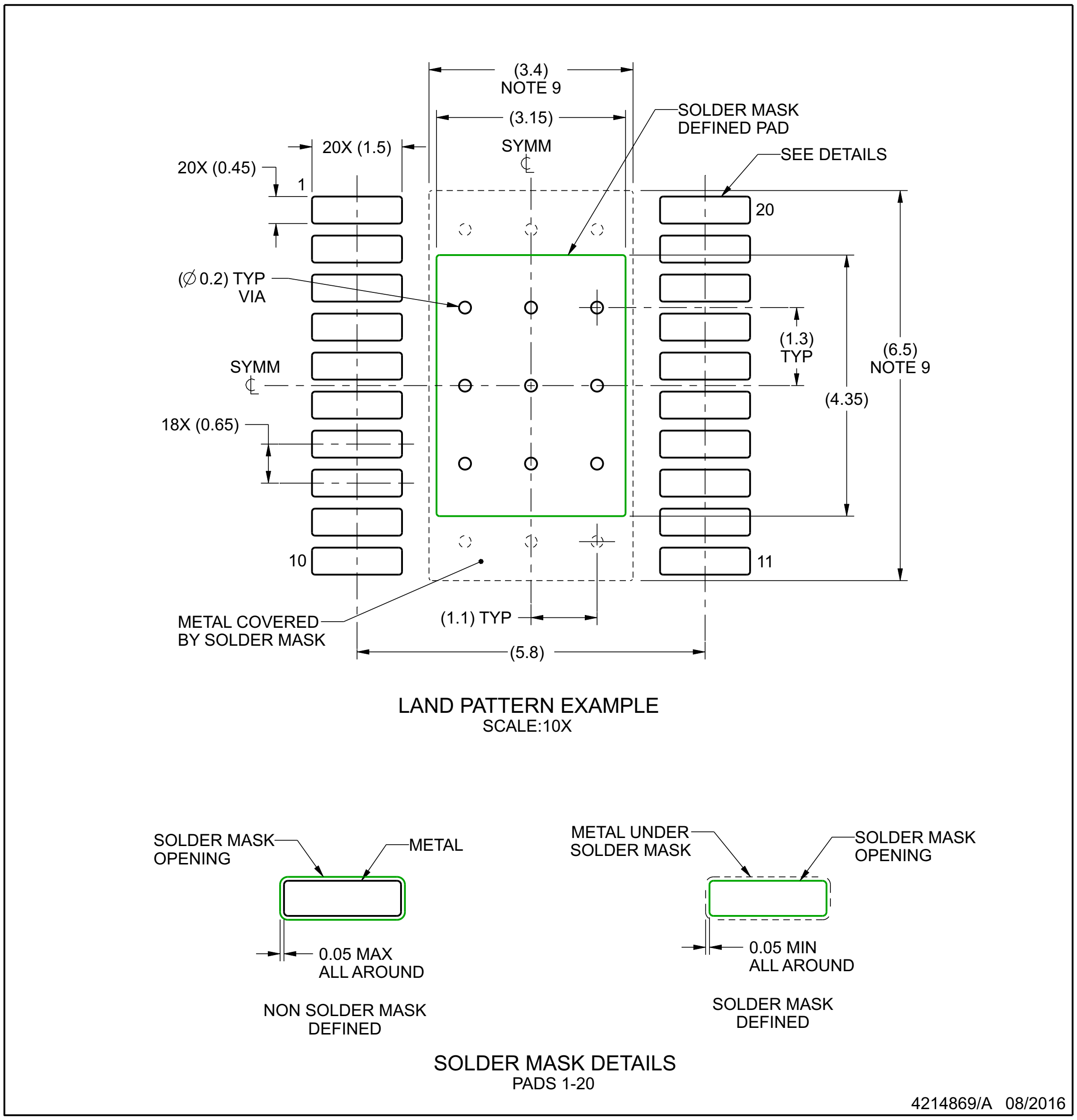
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

PWP0020A

PowerPAD™ TSSOP - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

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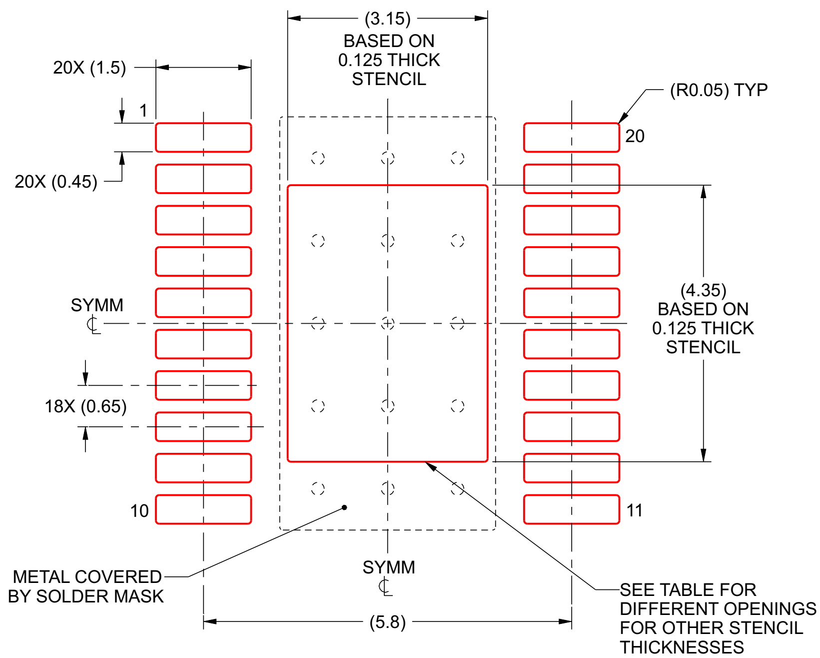
EXAMPLE STENCIL DESIGN

PWP0020A

PowerPAD™ TSSOP - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.52 X 4.86
0.125	3.15 X 4.35 (SHOWN)
0.15	2.88 X 3.97
0.175	2.66 X 3.68

4214869/A 08/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PDRV81545PWPR	Active	Preproduction	HTSSOP (PWP) | 20	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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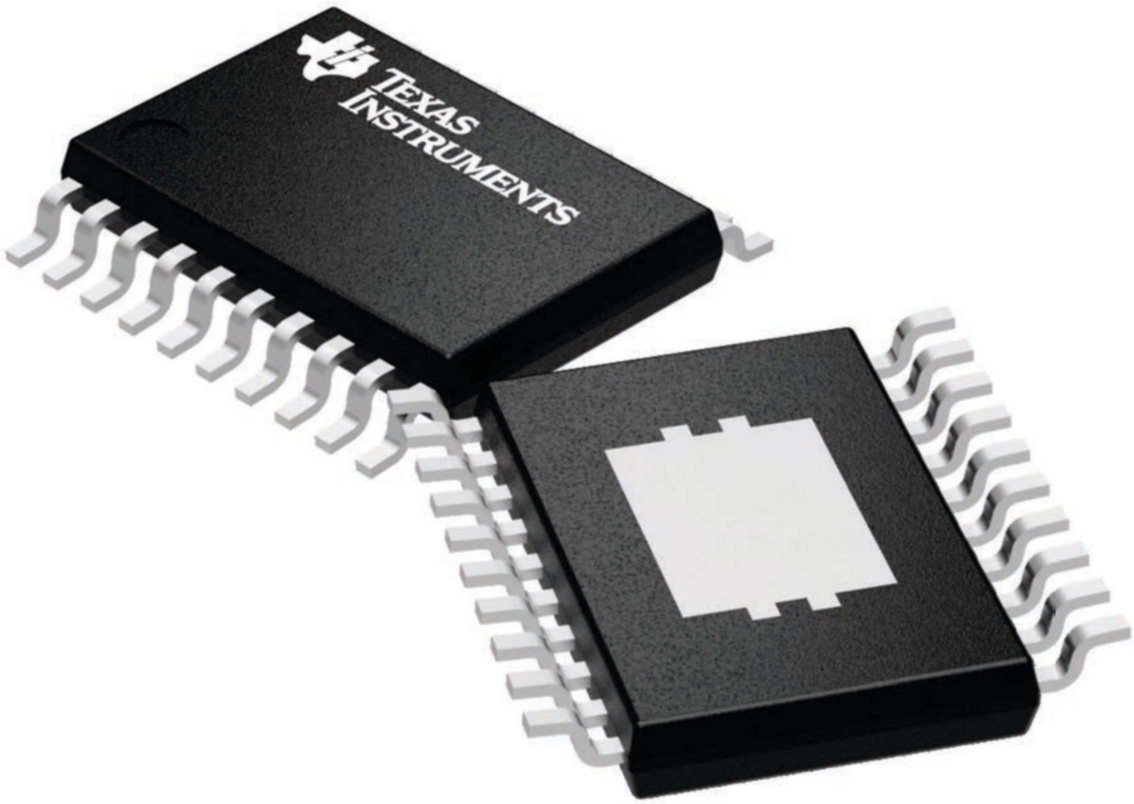
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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