DRV8106-Q1 Automotive Half-Bridge Smart Gate Driver With Wide Common Mode Inline Current Sense Amplifier

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Half-bridge smart gate driver
  - 4.9-V to 37-V (40-V abs. max) operating range
  - Doubler charge pump for 100% PWM
- Pin to pin gate driver variants
  - DRV8705-Q1: H-bridge with low-side amplifier
  - DRV8706-Q1: H-bridge with inline amplifier
- Smart gate drive architecture
  - Adjustable slew rate control
  - 0.5-mA to 62-mA peak source current output
  - 0.5-mA to 62-mA peak sink current output
  - Integrated dead-time handshaking
- Wide common mode current shunt amplifier
  - Supports inline, high-side, or low-side
  - Adjustable gain settings (10, 20, 40, 80 V/V)
  - Integrated feedback resistors
  - Adjustable PWM blanking scheme
- Multiple interface options available
  - SPI: Detailed configuration and diagnostics
  - H/W: Simplified control and less MCU pins
- Spread spectrum clocking for EMI reduction
- Compact VQFN package with wettable flanks
- Integrated protection features
  - Dedicated driver disable pin (DRVOFF)
  - Supply and regulator voltage monitors
  - MOSFET V_{DS} overcurrent monitors
  - MOSFET V_{GS} gate fault monitors
  - Charge pump for reverse polarity MOSFET
  - Offline open load and short circuit diagnostics
  - Device thermal warning and shutdown
  - Fault condition interrupt pin (nFAULT)

2 Applications

- Automotive brushed DC motors
- Solenoids and relays
- BDC fuel, water, oil pumps
- Windshield wipers
- Cordless vacuum cleaner

3 Descriptions

The DRV8106-Q1 is a highly integrated half-bridge gate driver, capable of driving high-side and low-side N-channel power MOSFETs. It generates the proper gate drive voltages using an integrated doubler charge pump for the high-side and a linear regulator for the low-side.

The device uses a smart gate drive architecture to reduce system cost and improve reliability. The gate driver optimizes dead time to avoid shoot-through conditions, provides control to decreasing electromagnetic interference (EMI) through adjustable gate drive current, and protects against drain to source and gate short conditions with V_{DS} and V_{GS} monitors.

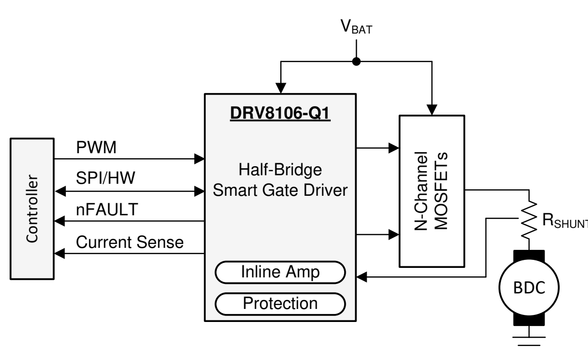
A wide common mode shunt amplifier provides inline current sensing to continuously measure motor current even during recirculating windows. The amplifier can be used in low-side or high-side sense configurations if inline sensing is not required.

The DRV8106-Q1 provide an array of protection features to ensure robust system operation. These include under and overvoltage monitors for the power supply and charge pump, V_{DS} overcurrent and V_{GS} gate fault monitors for the external MOSFETs, offline open load and short circuit diagnostics, and internal thermal warning and shutdown protection.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8106-Q1	VQFN (32)	5.00 mm x 5.00 mm

(1) For all avaiable packages, see orderable addendum at the end of the data sheet.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2021) to Revision B (June 2021) **Page**

- V_{OFF} specification improved to +/- 1.5mV........6
- CMRR specification MIN specification improved to 70 (125C) and 69 dB (150C)........6
- Improved EN_DRV register bit description........42

Changes from Revision * (July 2020) to Revision A (April 2021) **Page**

- Changed deviced status to Production Data........1

Device Comparison Table

DEVICE	HALF-BRIDGES	AMPLIFIERS	INTERFACE
DRV8106S-Q1	1	1	Serial (SPI)
DRV8106H-Q1	1		Hardware (H/W)

Table 5-1. SPI vs. H/W Feature Comparison

Feature	SPI (S) Interface	H/W (H) Interface
Gate Drive Output Current (I_{DRIVE})	16 Settings, HS & LS Independent	6 Settings, HS & LS Linked
Dead Time	Handshake + 7 Fixed Settings	Handshake Only
V_{DS} Comparator Threshold	16 Settings, HS & LS Independent	6 Settings, HS & LS Linked
V_{DS} and V_{GS} Blanking Time (t_{DRIVE})	4 Settings	Fixed, 4 µs
V_{DS} Deglitch Time	4 Settings	Fixed, 4 µs
V_{GS} Deglitch Time	Fixed, 2 µs	Fixed, 2 µs
V_{DS} Fault Response	4 Modes	Fixed, Cycle-By-Cycle
V_{GS} Fault Response	4 Modes	Fixed, Cycle-By-Cycle
Amplifier Gain	4 Settings	4 Settings
Amplifier Blanking Time	8 Settings	N/A
Amplifier Sample and Hold	Available	N/A
Amplifier Reference Voltage	2 Settings	Fixed, V_{AREF} / 2
V_{PVDD} Undervoltage Fault Response	2 Modes	Auto Retry
V_{PVDD} Overvoltage Fault Response	4 Modes	N/A
V_{VCP} Undervoltage Fault Response	2 Modes	Auto Retry
V_{VCP} Undervoltage Threshold	2 Settings	Fixed, 2.5 V
Offline Open Load Diagnostic	Available	N/A
Offline Short Circuit Diagnostic	Available	N/A

5 Pin Configuration

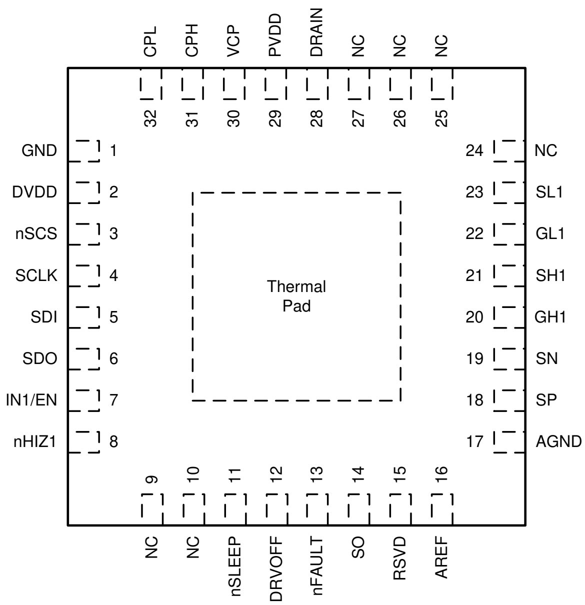


Figure 5-1. DRV8106S-Q1 RHB Package 32-Pin VQFN Top View

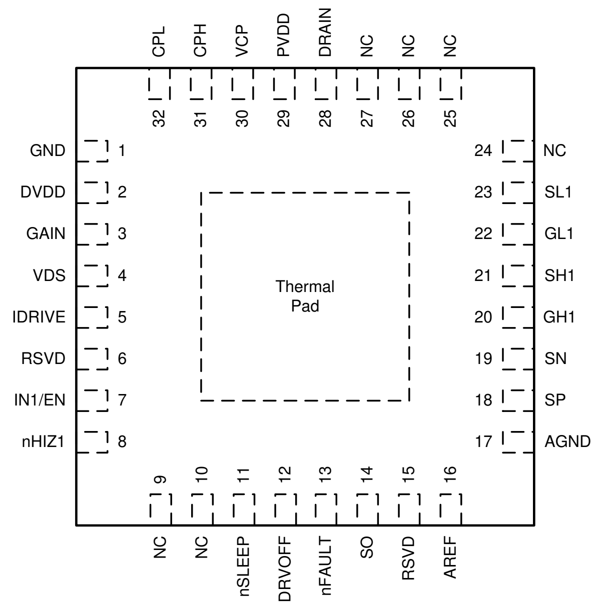


Figure 5-2. DRV8106H-Q1 RHB Package 32-Pin VQFN Top View

DRV8106-Q1_RHB Package (VQFN) Pin Functions

PIN			I/O	TYPE	DESCRIPTION
NO.	NAME DRV8106S-Q1	NAME DRV8106H-Q1			
1	GND		I/O	Ground	Device ground. Connect to system ground.
2	DVDD		I	Power	Device logic and digital output power supply input. Connect a 1.0-µF, 6.3-V ceramic capacitor between the DVDD and GND pins.
3	nSCS	—	I	Digital	Serial chip select. A logic low on this pin enables serial interface communication. Internal pullup resistor.
	—	GAIN	I	Analog	Amplifier gain setting. 4 level input pin set by an external resistor.
4	SCLK	—	I	Digital	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin. Internal pulldown resistor.
	—	VDS	I	Analog	VDS monitor threshold setting. 6 level input pin set by an external resistor.
5	SDI	—	I	Digital	Serial data input. Data is captured on the falling edge of the SCLK pin. Internal pulldown resistor.
	—	IDRIVE	I	Analog	Gate driver output current setting. 6 level input pin set by an external resistor.
6	SDO	—	O	Digital	Serial data output. Data is shifted out on the rising edge of the SCLK pin. Push-pull output.
	—	RSVD	—	—	Reserved. May be left floating or tied to GND.
7	IN1/EN		I	Digital	Half-bridge control input. See PWM modes for details. Internal pulldown.
8	nHIZ1		I	Digital	Half-bridge control input. See PWM modes for details. Internal pulldown.
9	NC		—	—	No connection.
10	NC		—	—	No connection.
11	nSLEEP		I	Digital	Device enable pin. Logic low to shutdown the device and enter sleep mode. Internal pulldown resistor.

PIN			I/O	TYPE	DESCRIPTION
NO.	NAME DRV8106S-Q1	NAME DRV8106H-Q1			
12	DRVOFF		I	Digital	Driver shutdown pin. Logic high to pull down both high-side and low-side gate driver output. Internal pulldown resistor.
13	nFAULT		O	Digital	Fault indicator output. This pin is pulled logic low to indicate a fault condition. Open-drain output. Requires external pullup resistor.
14	SO		O	Analog	Shunt amplifier output.
15	RSVD		—	—	Reserved. Connect to ground or leave disconnected.
16	AREF		I	Power	External voltage reference and power supply for current sense amplifiers. Connect a 0.1-µF, 6.3-V ceramic capacitor between the AREF and AGND pins.
17	AGND		I/O	Power	Device ground. Connect to system ground.
18	SP		I	Analog	Shunt amplifier positive input. Connect to the high-side of the current shunt resistor.
19	SN		I	Analog	Shunt amplifier negative input. Connect to the low-side of the current shunt resistor.
20	GH1		O	Analog	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
21	SH1		I	Analog	High-side source sense input. Connect to the high-side power MOSFET source.
22	GL1		O	Analog	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
23	SL1		I	Analog	Low-side MOSFET gate drive sense and power return. Connect to system ground with low impedance path to the low-side MOSFET ground return.
24	NC		—	—	No connection.
25	NC		—	—	No connection.
26	NC		—	—	No connection.
27	NC		—	—	No connection.
28	DRAIN		I	Analog	Bridge MOSFET drain voltage sense pin. Connect to common point of the high-side MOSFET drains.
29	PVDD		I	Power	Device driver power supply input. Connect to the bridge power supply. Connect a 0.1-µF, PVDD-rated ceramic capacitor and local bulk capacitance greater than or equal to 10-µF between PVDD and GND pins.
30	VCP		I/O	Power	Charge pump output. Connect a 1-µF, 16-V ceramic capacitor between the VCP and PVDD pins.
31	CPH		I/O	Power	Charge pump switching node. Connect a 100-nF, PVDD-rated ceramic capacitor between the CPH and CPL pins.
32	CPL		I/O	Power	Charge pump switching node. Connect a 100-nF, PVDD-rated ceramic capacitor between the CPH and CPL pins.

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Driver power supply pin voltage	PVDD	–0.3	40	V
MOSFET drain sense pin voltage	DRAIN	–0.3	40	V
Voltage difference between ground pins	AGND, GND	–0.3	0.3	V
Charge pump pin voltage	VCP	–0.3	55	V
Charge pump high-side pin voltage	CPH	V_{PVDD} – 0.3	V_{VCP} + 0.3	V
Charge pump low-side pin voltage	CPL	–0.3	V_{PVDD} + 0.3	V
Digital power supply pin voltage	DVDD	–0.3	5.75	V
Logic pin voltage	DRVOFF, GAIN, IDRIVE, IN1/EN, nHIZx, nSLEEP, nFAULT, nSCS, SCLK, SDI, VDS	–0.3	5.75	V
Output logic pin voltage	SDO	–0.3	V_{DVDD} + 0.3	V
High-side gate drive pin voltage	GHx[2]	–2	V_{VCP} + 0.3	V
Transient 1-µs high-side gate drive pin voltage		–5	V_{VCP} + 0.3	
High-side gate drive pin voltage with respect to SHx		–0.3	13.5	
High-side sense pin voltage	SHx[2]	–2	40	V
Transient 1-µs high-side sense pin voltage		–5	40	
Low-side gate drive pin voltage	GLx[2]	–2	13.5	V
Transient 1-µs low-side gate drive pin voltage		–3	13.5	
Low-side gate drive pin voltage with respect to SLx		–0.3	13.5	
Low-side sense pin voltage	SLx[2]	–2	2	V
Transient 1-µs low-side sense pin voltage		–3	3	
Peak gate drive current	GHx, GLx	Internally Limited	Internally Limited	mA
Amplfier power supply and reference pin voltage	AREF	–0.3	5.75	V
Amplifier input pin voltage	SN, SP	–2	V_{VCP} + 0.3	V
Transient 1-µs amplifier input pin voltage		–5	V_{VCP} + 0.3	
Amplifier input differential voltage	SN, SP	–5.75	5.75	V
Amplifier output pin voltage	SO	–0.3	V_{AREF} + 0.3	V
Ambient temperature, T_A		–40	125	°C
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) PVDD and DRAIN with respect to GHx, SHx, GLx, or SLx should not exceed 40-V. When PVDD or DRAIN are greater than 35-V, negative voltage on GHx, SHx, GLx, and SLx should be limited to ensure this rating is not exceeded. When PVDD and DRAIN are less than 35-V, the full negative voltage rating of GHx, SHx, GLx, and SLx is available.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[(1)] HBM ESD Classification Level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	Corner pins	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{PVDD}	Driver power supply voltage	PVDD	4.9		37	V
I_{HS} [(1)]	High-side average gate-drive current	GHx	0		15	mA
I_{LS} [(1)]	Low-side average gate-drive current	GLx	0		15	mA
V_{DVDD}	Digital power supply voltage	DVDD	3		5.5	V
V_{DIN}	Digital input voltage	DRVOFF, IN1/EN, nHIZx, nSLEEP, nSCS, SCLK, SDI	0		5.5	V
I_{DOUT}	Digital output current	SDO	0		5	mA
V_{OD}	Open drain pullup voltage	nFAULT	0		5.5	V
I_{OD}	Open drain output current	nFAULT	0		5	mA
V_{AREF}	Amplfier reference supply voltage	AREF	3		5.5	V
I_{SO}	Shunt amplifier output current	SO	0		5	mA
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

(1) Power dissipation and thermal limits must be observed

6.4 Thermal Information

THERMAL METRIC[(1)]		DRV8106-Q1 RHB (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	15.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

4.9 V ≤ V_{PVDD} ≤ 37 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (DRAIN, DVDD, PVDD, VCP)						
I_{PVDDQ}	PVDD sleep mode current	V_{PVDD}, V_{DRAIN} = 13.5 V, nSLEEP = 0 V –40 ≤ T_J ≤ 85°C		2.25	3	µA
I_{DRAINQ}	DRAIN sleep mode current	V_{PVDD}, V_{DRAIN} = 13.5 V, nSLEEP = 0 V –40 ≤ T_J ≤ 85°C		2	2.75	µA

4.9 V ≤ V_{PVDD} ≤ 37 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DVDDQ}	DVDD sleep mode current	V_{PVDD}, V_{DRAIN} = 13.5 V, nSLEEP = 0 V –40 ≤ T_J ≤ 85°C		2	3.5	µA
I_{PVDD}	PVDD active mode current	V_{PVDD}, V_{DRAIN} = 13.5 V, nSLEEP = 5 V		2	3	mA
I_{DRAIN}	DRAIN active mode current	V_{PVDD}, V_{DRAIN} = 13.5 V, nSLEEP = 5 V, V_{DS_LVL} ≤ 500 mV		250	325	µA
I_{DVDD}	DVDD active mode current	V_{DVDD} = 5 V, SDO = 0 V		3.5	5.5	mA
f_{DVDD}	Digital oscilator switching frequency	Primary frequency of spread spectrum.		14.25		MHz
t_{WAKE}	Turnon time	nSLEEP = 5 V to active mode			1	ms
t_{SLEEP}	Turnoff time	nSLEEP = 0 V to sleep mode			1	ms
V_{VCP}	Charge pump regulator voltage with respect to PVDD	V_{PVDD} ≥ 13 V, I_{VCP} ≤ 15 mA	9.5	10.5	11	V
		V_{PVDD} = 11 V, I_{VCP} ≤ 15 mA	8.4	10	11	
		V_{PVDD} = 9 V, I_{VCP} ≤ 11 mA	7	8	9	
		V_{PVDD} = 7 V, I_{VCP} ≤ 7.5 mA	5.5	6	7	
		V_{PVDD} = 5.5 V, I_{VCP} ≤ 5 mA	4.5	5	5.5	
f_{VCP}	Charge pump switching frequency	Primary frequency of spread spectrum.		400		kHz
LOGIC-LEVEL INPUTS (DRVOFF, IN1/EN, nHIZx, nSLEEP, nSCS, SCLK, SDI)						
V_{IL}	Input logic low voltage	DRVOFF, IN1/EN, nHIZx, nSLEEP, SCLK, SDI	0		V_{DVDD} x 0.3	V
V_{IH}	Input logic high voltage	DRVOFF, IN1/EN, nHIZx, nSLEEP, SCLK, SDI	V_{DVDD} x 0.7		5.5	V
V_{HYS}	Input hysteresis			V_{DVDD} x 0.1		V
I_{IL}	Input logic low current	V_{DIN} = 0 V, DRVOFF, IN1/EN, nHIZx, nSLEEP, SCLK, SDI	–5		5	µA
		V_{DIN} = 0 V, nSCS		50	100	
I_{IH}	Input logic high current	V_{DIN} = 5 V, DRVOFF, IN1/EN, nHIZx, nSLEEP, SCLK, SDI		50	100	µA
		V_{DIN} = 5 V, V_{DVDD} = 5 V, nSCS	–5		5	
R_{PD}	Input pulldown resistance	To GND, DRVOFF, IN1/EN, nHIZx, nSLEEP, SCLK, SDI	50	100	150	kΩ
R_{PU}	Input pullup resistance	To DVDD, nSCS	50	100	150	kΩ
MULTI-LEVEL INPUTS (GAIN, IDRIVE, VDS)						
V_{QI1}	Quad-level input 1	GAIN Voltage to set level 1	0		V_{DVDD} x 0.1	V
R_{QI2}	Quad-level input 2	GAIN Resistance to GND to set level 2	44.65	47	49.35	kΩ
R_{QI3}	Quad-level input 3	GAIN Resistance to GND to set level 3	500	Hi-Z		kΩ
V_{QI4}	Quad-level input 4	GAIN Voltage to set level 4	V_{DVDD} x 0.9		5.5	V
R_{QPD}	Quad-level pulldown resistane	GAIN, To GND		98		kΩ
R_{QPU}	Quad-level pullup resistane	GAIN, To DVDD		98		kΩ
V_{SI1}	Six-level input 1	IDRIVE, VDS Voltage to set level 1	0		V_{DVDD} x 0.1	V
R_{SI2}	Six-level input 2	IDRIVE, VDS Resistance to GND to set level 2	28.5	30	31.5	kΩ
R_{SI3}	Six-level input 3	IDRIVE, VDS Resistance to GND to set level 3	95	100	105	kΩ
R_{SI4}	Six-level input 4	IDRIVE, VDS Resistance to GND to set level 4	500	Hi-Z		kΩ

4.9 V ≤ V_{PVDD} ≤ 37 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{SI5}	Six-level input 5	IDRIVE, VDS Resistance to DVDD to set level 5	58.9	62	65.1	kΩ
R_{SI6}	Six-level input 6	IDRIVE, VDS Voltage to set level 6	V_{DVDD} x 0.9		5.5	V
R_{SPD}	Six-level pulldown resistane	IDRIVE, VDS, To GND		98		kΩ
R_{SPU}	Six-level pullup resistane	IDRIVE, VDS To DVDD		69		kΩ
LOGIC-LEVEL OUTPUTS (nFAULT, SDO)						
V_{OL}	Output logic low voltage	I_{DOUT} = 5 mA			0.5	V
V_{OH}	Output logic high voltage	I_{DOUT} = –5 mA, SDO	V_{DVDD} x 0.8			V
I_{ODZ}	Open-drain logic high current	V_{OD} = 5 V, nFAULT	–10		10	µA
GATE DRIVERS (GHx, GLx)						
V_{GHx_L}	GHx low level output voltage	I_{DRVN_HS} = I_{STRONG}, I_{GHx} = 1mA, GHx to SHx	0		0.25	V
V_{GLx_L}	GLx low level output voltage	I_{DRVN_LS} = I_{STRONG}, I_{GLx} = 1mA, GLx to SLx	0		0.25	V
V_{GHx_H}	GHx high level output voltage	I_{DRVP_HS} = I_{HOLD}, I_{GHx} = 1mA, VCP to GHx	0		0.25	V
V_{GLx_H}	GLx high level output voltage	I_{DRVP_LS} = I_{HOLD}, I_{GLx} = 1mA, 10.5 V ≤ V_{PVDD} ≤ 37 V, GLx to SLx	10.25	10.5	12.5	V
		I_{DRVP_LS} = I_{HOLD}, I_{GLx} = 1mA, 4.9 V ≤ V_{PVDD} ≤ 10.5 V, GLx to SLx	V_{PVDD} - 0.25	V_{PVDD}	V_{PVDD}	V
$I_{DRVP, SPI}$	Peak gate current (source) SPI Device	IDRVP = 0000b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	0.2	0.5	0.8	mA
		IDRVP = 0001b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	0.5	1	1.5	
		IDRVP = 0010b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	1.3	2	2.7	
		IDRVP = 0011b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	2.1	3	3.9	
		IDRVP = 0100b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	2.9	4	5.1	
		IDRVP = 0101b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	4.5	6	7.5	
		IDRVP = 0110b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	6	8	10	
		IDRVP = 0111b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	9	12	15	
		IDRVP = 1000b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	12	16	20	
		IDRVP = 1001b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	15	20	25	
		IDRVP = 1010b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	18	24	30	
		IDRVP = 1011b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	21	28	35	
		IDRVP = 1100b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	23.25	31	38.75	
		IDRVP = 1101b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	26.5	40	50	
		IDRVP = 1110b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	28	48	60	
		IDRVP = 1111b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	30	62	77.5	
$I_{DRVP, H/W}$	Peak gate current (source) H/W Device	IDRIVE level 1, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	0.5	1	1.5	mA
		IDRIVE level 2, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	2.9	4	5.1	
		IDRIVE level 3, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	6	8	10	
		IDRIVE level 4, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	12	16	20	
		IDRIVE level 5, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	23.25	31	38.75	
		IDRIVE level 6, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	30	62	77.5	

4.9 V ≤ V_{PVDD} ≤ 37 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DRVN, SPI}$	Peak gate current (sink) SPI Device	IDRVN = 0000b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	0.15	0.5	0.85	mA
		IDRVN = 0001b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	0.35	1	1.65	
		IDRVN = 0010b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	0.85	2	3.15	
		IDRVN = 0011b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	1.4	3	4.6	
		IDRVN = 0100b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	2.1	4	5.9	
		IDRVN = 0101b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	3.5	6	8.5	
		IDRVN = 0110b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	5	8	11	
		IDRVN = 0111b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	8	12	16	
		IDRVN = 1000b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	11.5	16	20	
		IDRVN = 1001b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	14.7	20	25	
		IDRVN = 1010b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	18	24	30	
		IDRVN = 1011b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	21	28	35	
		IDRVN = 1100b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	23.25	31	38.75	
		IDRVN = 1101b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	30	40	52	
		IDRVN = 1110b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	36	48	62	
		IDRVN = 1111b, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	46.5	62	80	
$I_{DRVN, H/W}$	Peak gate current (sink) H/W Device	IDRIVE level 1, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	0.35	1	1.65	mA
		IDRIVE level 2, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	2.1	4	5.9	
		IDRIVE level 3, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	5	8	11	
		IDRIVE level 4, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	11.5	16	20	
		IDRIVE level 5, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	23.25	31	38.75	
		IDRIVE level 6, V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	46.5	62	80	
I_{HOLD}	Gate pullup hold current	V_{GSx} = 3 V, V_{PVDD} ≥ 7 V	5	16	30	mA
I_{STRONG}	Gate pulldown strong current	V_{GSx} = 3 V, V_{PVDD} ≥ 7 V, 0.5 ≤ I_{DRVP} ≤ 12 mA	30	62	100	mA
		V_{GSx} = 3 V, V_{PVDD} ≥ 7 V, 16 ≤ I_{DRVP} ≤ 62 mA	45	128	205	mA
R_{PDSA_LS}	Low-side semi-active pulldown	GLx to SLx, V_{GSx} = 3 V		1.8		kΩ
		GLx to SLx, V_{GSx} = 1 V		5		kΩ
R_{PD_HS}	High-side passive pulldown resistor	GHx to SHx		150		kΩ
R_{PD_LS}	Low-side passive pulldown resistor	GLx to SLx		150		kΩ
I_{SHx}	Switch-node sense leakage current	Into SHx, SHx = DRAIN ≤ 37 V GHx – SHx = 0 V, nSLEEP = 0 V	–5	0	25	µA
		Into SHx, SHx = DRAIN ≤ 37 V GHx – SHx = 0 V, nSLEEP = 5 V	–150	–100	–40	µA
GATE DRIVER TIMINGS (GHx, GLx)						
t_{PDR_LS}	Low-side rising propagation delay	Input to GLx rising		300	850	ns
t_{PDF_LS}	Low-side falling propagation delay	Input to GLx falling		300	600	ns
t_{PDR_HS}	High-side rising propagation delay	Input to GHx rising		300	600	ns
t_{PDF_HS}	High-side falling propagation delay	Input to GHx falling		300	600	ns
t_{DEAD}	Internal handshake dead-time	V_{GSx_L}/V_{GSx_H} falling 10% to V_{GSx_H}/V_{GSx_L} rising 10%		350		ns

4.9 V ≤ V_{PVDD} ≤ 37 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{DEAD\_D, SPI}$	Insertable digital dead-time SPI Device	VGS_TDEAD = 000b, Handshake only		0		ns
		VGS_TDEAD = 001b	150	250	350	
		VGS_TDEAD = 010b	400	500	600	
		VGS_TDEAD = 011b	600	750	900	
		VGS_TDEAD = 100b	800	1000	1200	
		VGS_TDEAD = 101b	1600	2000	2400	
		VGS_TDEAD = 110b	3400	4000	4600	
		VGS_TDEAD = 111b	7200	8000	8800	
$t_{DEAD\_D, H/W}$	Insertable digital dead-time H/W Device	Handshake only		0		ns
CURRENT SHUNT AMPLIFIERS (AREF, SN, SO, SP)						
V_{COM}	Common mode input range		–2		V_{PVDD} + 2	V
$G_{CSA, SPI}$	Sense amplifier gain SPI device	CSA_GAIN = 00b	9.9	10.15	10.4	V/V
		CSA_GAIN = 01b	19.5	20	20.5	
		CSA_GAIN = 10b	39	40	41	
		CSA_GAIN = 11b	78	80	82	
$G_{CSA, H/W}$	Sense amplifier gain H/W device	GAIN quad-level 1	9.9	10.15	10.4	V/V
		GAIN quad-level 2	19.5	20	20.5	
		GAIN quad-level 3	39	40	41	
		GAIN quad-level 4	78	80	82	
t_{SET}	Sense amplifier settling time to ±1%	V_{SO_STEP} = 1.5 V, G_{CSA} = 10 V/V C_{SO} = 60 pF		2.2		µs
		V_{SO_STEP} = 1.5 V, G_{CSA} = 20 V/V C_{SO} = 60 pF		2.2		
		V_{SO_STEP} = 1.5 V, G_{CSA} = 40 V/V C_{SO} = 60 pF		2.2		
		V_{SO_STEP} = 1.5 V, G_{CSA} = 80 V/V C_{SO} = 60 pF		3		
$t_{BLK, SPI}$	Sense amplifier output blanking time SPI Device	CSA_BLK = 000b, % of t_{DRIVE} period		0		%
		CSA_BLK = 001b, % of t_{DRIVE} period		25		
		CSA_BLK = 010b, % of t_{DRIVE} period		37.5		
		CSA_BLK = 011b, % of t_{DRIVE} period		50		
		CSA_BLK = 100b, % of t_{DRIVE} period		62.5		
		CSA_BLK = 101b, % of t_{DRIVE} period		75		
		CSA_BLK = 110b, % of t_{DRIVE} period		87.5		
		CSA_BLK = 111b, % of t_{DRIVE} period		100		
$t_{BLK, H/W}$	Sense amplifier output blanking time H/W Device			0		ns
t_{SLEW}	Output slew rate	C_{SO} = 60 pF		2.5		V/µs
$V_{BIAS, SPI}$	Output voltage bias SPI Device	V_{SPx} = V_{SNx} = 0 V, CSA_DIV = 0b		V_{AREF} / 2		V
		V_{SPx} = V_{SNx} = 0 V, CSA_DIV = 1b		V_{AREF} / 8		
$V_{BIAS, H/W}$	Output voltage bias H/W Device			V_{AREF} / 2		V
V_{LINEAR}	Linear output voltage range	V_{AREF} = 3.3 V = 5 V	0.25		V_{AREF} – 0.25	V
V_{OFF}	Input offset voltage	V_{SPx} = V_{SNx} = 0 V, T_J = 25℃	–1.5		1.5	mV
V_{OFF_D}	Input offset voltage drift	V_{SPx} = V_{SNx} = 0 V		±10	±25	µV/℃

4.9 V ≤ V_{PVDD} ≤ 37 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{BIAS}	Input bias current	V_{SPx} = V_{SNx} = 0 V, into pin			100	µA
I_{BIAS_OFF}	Input bias current offset	I_{SPx} – I_{SNx}	–1		1	µA
I_{AREF}	AREF input current	V_{VREF} = 3.3 V = 5 V		1	1.8	mA
CMRR	Common mode rejection ratio	DC, –40 ≤ T_J ≤ 125°C	72	90		dB
		DC, –40 ≤ T_J ≤ 150°C	69	90		
		20kHz		80		
PSRR	Power supply rejection ratio	PVDD to SOx, DC		100		dB
		PVDD to SOx, 20kHz		90		
		PVDD to SOx, 400kHz		70		
PROTECTION CIRCUITS						
V_{PVDD_UV}	PVDD undervoltage threshold	V_{PVDD} rising	4.325	4.625	4.9	V
		V_{PVDD} falling	4.25	4.525	4.8	
$V_{PVDD\_UV\_HYS}$	PVDD undervoltage hysteresis	Rising to falling threshold		100		mV
$t_{PVDD\_UV\_DG}$	PVDD undervoltage deglitch time		8	10	12.75	µs
V_{PVDD_OV}	PVDD overvoltage threshold	V_{PVDD} rising, PVDD_OV_LVL = 0b	21	22.5	24	V
		V_{PVDD} falling, PVDD_OV_LVL = 0b	20	21.5	23	
		V_{PVDD} rising, PVDD_OV_LVL = 1b	27	28.5	30	
		V_{PVDD} falling, PVDD_OV_LVL = 1b	26	27.5	29	
$V_{PVDD\_OV\_HYS}$	PVDD overvoltage hysteresis	Rising to falling threshold		1		V
$t_{PVDD\_OV\_DG}$	PVDD overvoltage deglitch time	PVDD_OV_DG = 00b	0.75	1	1.5	µs
		PVDD_OV_DG = 01b	1.5	2	2.5	
		PVDD_OV_DG = 10b	3.25	4	4.75	
		PVDD_OV_DG = 11b	7	8	9	
V_{DVDD_POR}	DVDD supply POR threshold	DVDD falling	2.5	2.7	2.9	V
		DVDD rising	2.6	2.8	3	
$V_{DVDD\_POR\_HYS}$	DVDD POR hysteresis	Rising to falling threshold		100		mV
$t_{DVDD\_POR\_DG}$	DVDD POR deglitch time		5	8	12.75	µs
$V_{CP\_UV, SPI}$	Charge pump undervoltage threshold SPI Device	V_{VCP} - V_{PVDD}, falling, VCP_UV = 0b	2	2.5	3	V
		V_{VCP} - V_{PVDD}, falling, VCP_UV = 1b	4	5	6	
$V_{CP\_UV, H/W}$	Charge pump undervoltage threshold H/W Device		2	2.5	3	V
$t_{CP\_UV\_DG}$	Charge pump undervoltage deglitch time		8	10	12.75	µs
V_{GS_CLP}	High-side driver V_{GS} protection clamp		12.5	15	17	V
V_{GS_LVL}	Gate voltage monitor threshold	$V_{GH/Lx}$ – $V_{SH/Lx}$, VGS_LVL = 0b	1.1	1.4	1.75	V
		$V_{GH/Lx}$ – $V_{SH/Lx}$, VGS_LVL = 1b	0.8	1	1.2	V
$t_{GS\_FLT\_DG}$	V_{GS} fault monitor deglitch time		1.5	2	2.75	µs
$t_{GS\_HS\_DG}$	V_{GS} handshake monitor deglitch time			210		ns
$t_{DRIVE, SPI}$	V_{GS} and V_{DS} monitor blanking time SPI Device	VGS_TDRV = 00b	80	96	120	µs
		VGS_TDRV = 01b	1.5	2	2.5	
		VGS_TDRV = 10b	3.25	4	4.75	
		VGS_TDRV = 11b	7.5	8	9	
$t_{DRIVE, H/W}$	V_{GS} and V_{DS} monitor blanking time H/W Device		3.25	4	4.75	µs

4.9 V ≤ V_{PVDD} ≤ 37 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DS\_LVL, SPI}$	V_{DS} overcurrent protection threshold SPI Device	VDS_LVL = 0000b	0.04	0.06	0.08	V
		VDS_LVL = 0001b	0.06	0.08	0.10	
		VDS_LVL = 0010b	0.08	0.10	0.12	
		VDS_LVL = 0011b	0.10	0.12	0.14	
		VDS_LVL = 0100b	0.12	0.14	0.16	
		VDS_LVL = 0101b	0.14	0.16	0.18	
		VDS_LVL = 0110b	0.16	0.18	0.20	
		VDS_LVL = 0111b	0.18	0.2	0.22	
		VDS_LVL = 1000b	0.27	0.3	0.33	
		VDS_LVL = 1001b	0.36	0.4	0.44	
		VDS_LVL = 1010b	0.45	0.5	0.55	
		VDS_LVL = 1011b	0.54	0.6	0.66	
		VDS_LVL = 1100b	0.63	0.7	0.77	
		VDS_LVL = 1101b	0.9	1	1.1	
		VDS_LVL = 1110b	1.26	1.4	1.54	
		VDS_LVL = 1111b	1.8	2	2.2	
$V_{DS\_LVL, H/W}$	V_{DS} overcurrent protection threshold H/W Device	VDS six-level input 1	0.04	0.06	0.08	V
		VDS six-level input 2	0.08	0.10	0.12	
		VDS six-level input 3	0.18	0.2	0.22	
		VDS six-level input 4	0.45	0.5	0.55	
		VDS six-level input 5	0.9	1	1.1	
		VDS six-level input 6		Disabled		
$t_{DS\_DG, SPI}$	V_{DS} overcurrent protection deglitch time SPI Device	VDS_DG = 00b	0.75	1	1.5	µs
		VDS_DG = 01b	1.5	2	2.5	
		VDS_DG = 10b	3.25	4	4.75	
		VDS_DG = 11b	7.5	8	9	
$t_{DS\_DG, H/W}$	V_{DS} overcurrent protection deglitch time H/W Device		3.25	4	4.75	µs
I_{OLD}	Offline diagnostic current source	Pull up current		3		mA
		Pull down current		3		
T_{OTW}	Thermal warning temperature	T_J rising	130	150	170	°C
T_{HYS}	Thermal warning hysteresis			20		°C
T_{OTSD}	Thermal shutdown temperature	T_J rising	150	170	190	°C
T_{HYS}	Thermal shutdown hysteresis			20		°C

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
t_{SCLK}	SCLK minimum period	100			ns
t_{SCLKH}	SCLK minimum high time	50			ns
t_{SCLKL}	SCLK minimum low time	50			ns
t_{SU_SDI}	SDI input data setup time	25			ns
t_{H_SDI}	SDI input data hold time	25			ns
t_{D_SDO}	SDO output data delay time, C_L = 20 pF			30	ns
t_{SU_nSCS}	nSCS input setup time	25			ns
t_{H_nSCS}	nSCS input hold time	25			ns

		MIN	NOM	MAX	UNIT
t_{HI_nSCS}	nSCS minimum high time	450			ns
t_{EN_nSCS}	Enable delay time, nSCS low to SDO active			50	ns
t_{DIS_nSCS}	Disable delay time, nSCS high to SDO hi-Z			50	ns

6.7 Timing Diagrams

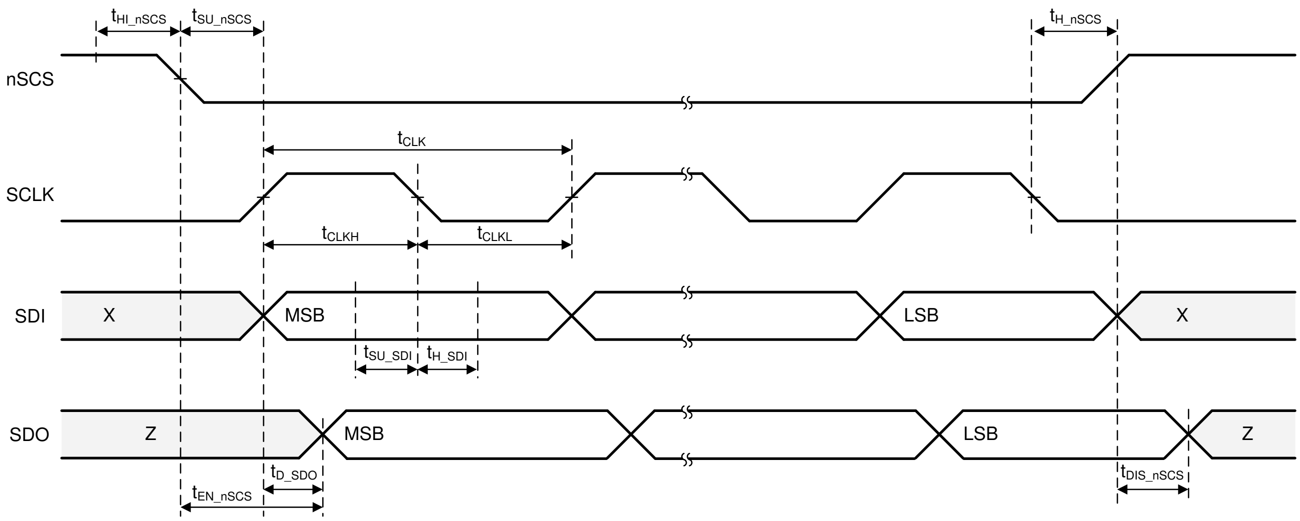


Figure 6-1. SPI Timing Diagram

6.8 Typical Characteristics

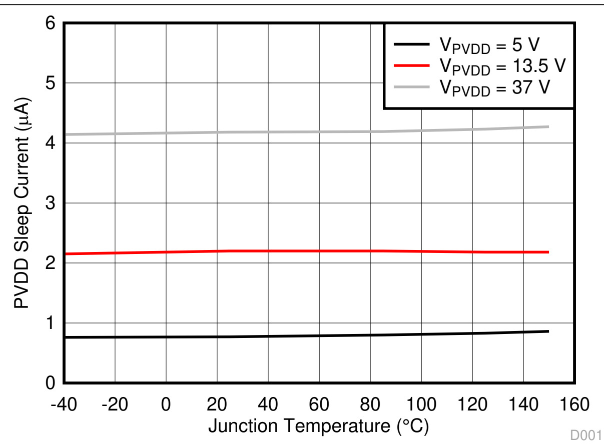


Figure 6-2. PVDD Sleep Current

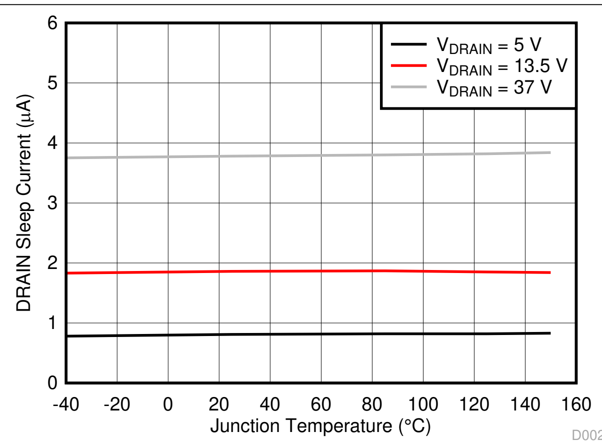


Figure 6-3. DRAIN Sleep Current

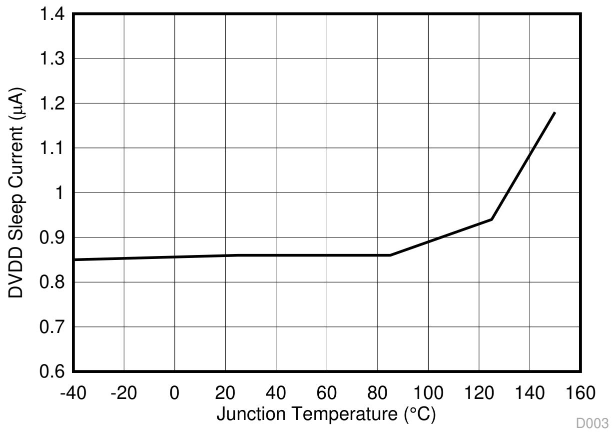


Figure 6-4. DVDD Sleep Current

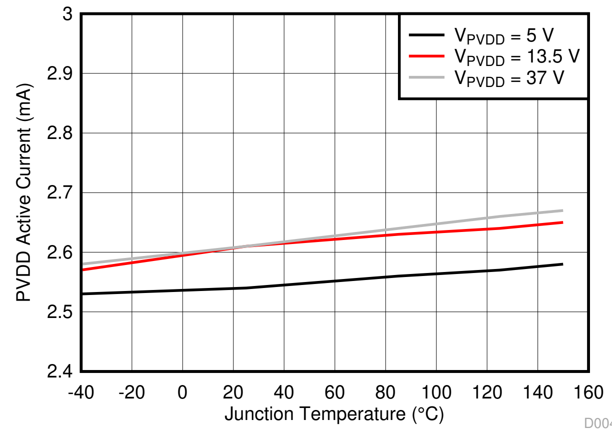


Figure 6-5. PVDD Active Current

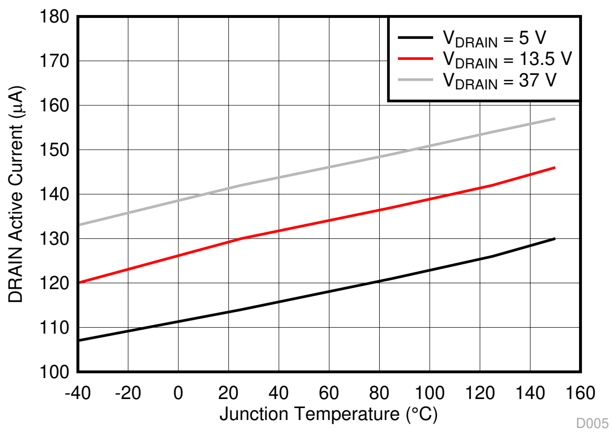


Figure 6-6. DRAIN Active Current

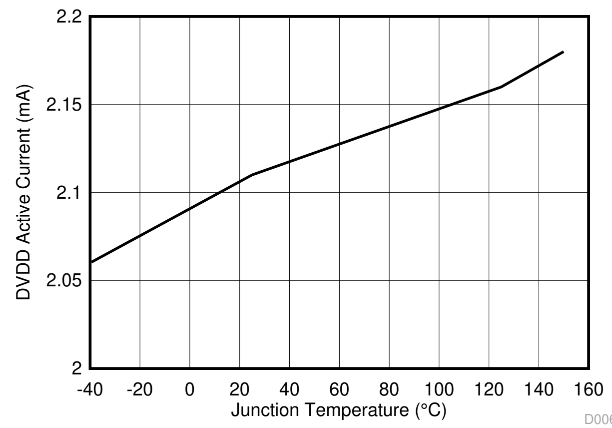
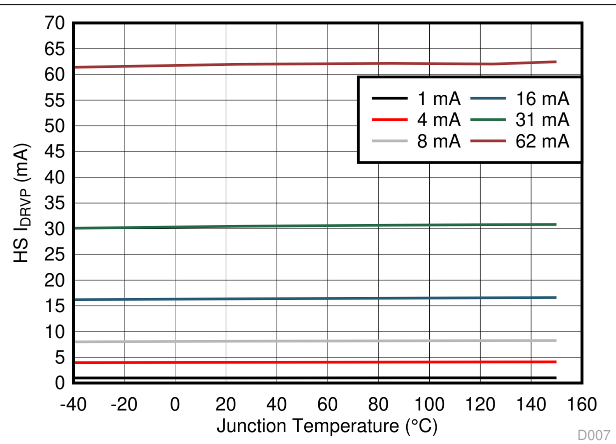
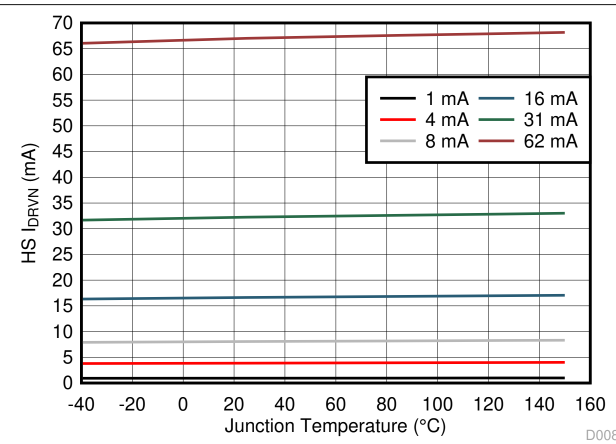


Figure 6-7. DVDD Active Current



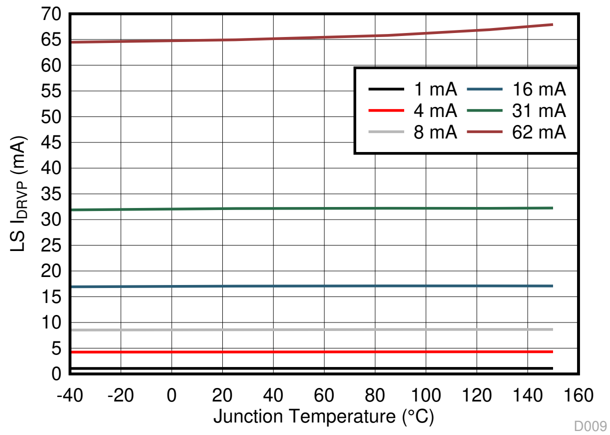
V_{PVDD} = 13.5 V

Figure 6-8. High-Side Gate Driver Source Current



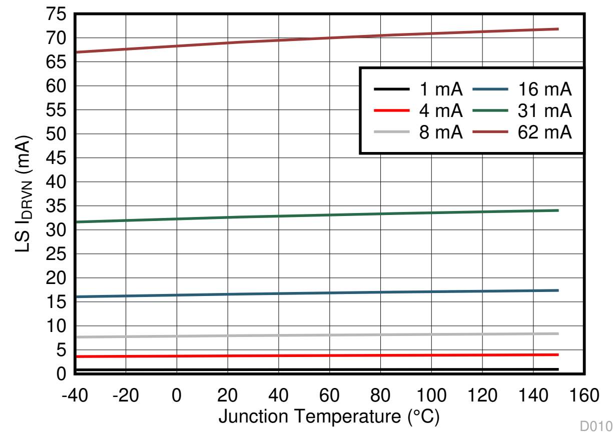
V_{PVDD} = 13.5 V

Figure 6-9. High-Side Gate Driver Sink Current



V_{PVDD} = 13.5 V

Figure 6-10. Low-Side Gate Driver Source Current



V_{PVDD} = 13.5 V

Figure 6-11. Low-Side Gate Driver Sink Current

7 Detailed Description

7.1 Overview

The DRV8106-Q1 is an integrated half-bridge smart gate driver for brushed DC motor applications. The device provides a half-bridge gate driver, capable of driving high-side and low-side N-channel power MOSFETs. The DRV8106-Q1 generates the proper gate drive voltages using an integrated doubler charge pump for the high-side and a linear regulator for the low-side. The gate drivers support up to 62-mA source and 62-mA sink peak gate drive current capability. The device supports a wide operating supply voltage range of 4.9-V to 37-V.

The DRV8106-Q1 is based on a smart gate drive architecture (SGD) to reduce system cost and improve reliability. The SGD architecture optimizes dead time to avoid shoot-through conditions, provides flexibility in decreasing electromagnetic interference (EMI) with MOSFET slew rate control through adjustable gate drive current, and protects against drain to source and gate short circuits conditions with V_{DS} and V_{GS} monitors. A strong pulldown circuit helps prevent dV/dt parasitic gate coupling. The external MOSFET slew control is supported through adjustable output gate drivers. The gate driver peak source current can be configured between 0.5-mA and 62-mA. The gate drivers peak sink current can be configured between 0.5-mA and 62-mA.

The DRV8106-Q1 can operate with either 3.3-V or 5-V external controllers (MCUs). A dedicated DVDD pins allows for external power to the device digital core and the digital outputs to be referenced to the controller I/O voltage. It communicates with the external controller through an SPI bus to manage configuration settings and diagnostic feedback. The device also has an AREF pin which allows for the shunt amplifier reference voltage to be connected to the reference voltage of the external controller ADC. The shunt amplifier outputs are also clamped to the AREF pin voltage to protect the inputs of the controller from excessive voltage spikes.

The DRV8106-Q1 provides an array of diagnostic and protection features to monitor system status before operation and protect against faults during system operation. These include under and overvoltage monitors for the power supply and charge pump, V_{DS} overcurrent and V_{GS} gate fault monitors for the external MOSFETs, offline open load and short circuit detection, and internal thermal warning and shutdown protection. The current shunt amplifier can be utilized to monitor load current of the system. The high common mode range of the amplifier allows for either inline, high-side, or low-side based shunt resistor current sensing.

7.2 Functional Block Diagram

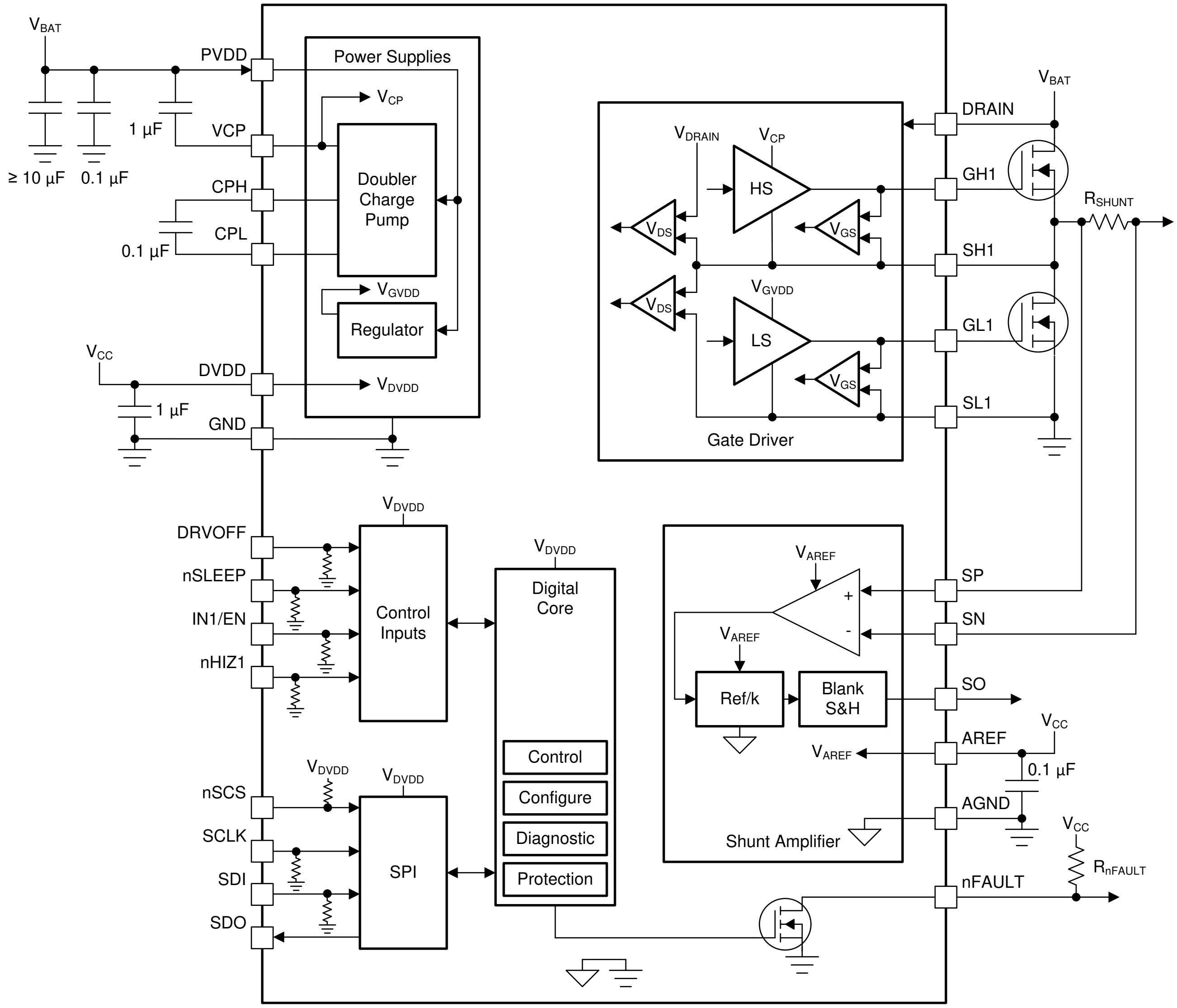


Figure 7-1. DRV8106S-Q1 Functional Block Diagram

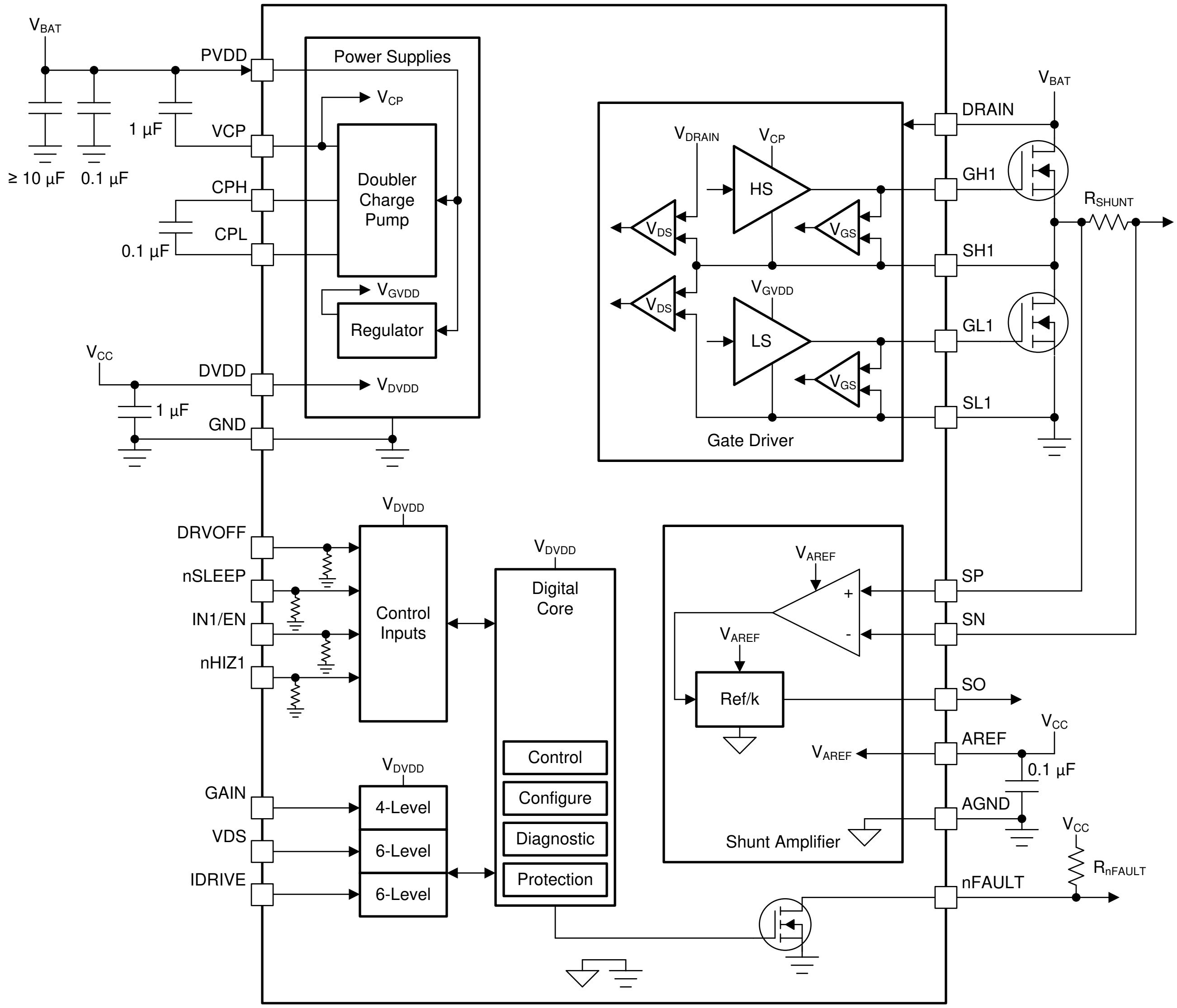


Figure 7-2. DRV8106H-Q1 Functional Block Diagram

7.3 Feature Description

7.3.1 External Components

Table 7-1 lists the recommended external components for the device.

Table 7-1. Recommended External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{PVDD1}	PVDD	GND	0.1-µF, low ESR ceramic capacitor, PVDD-rated.
C_{PVDD2}	PVDD	GND	Local bulk capacitance greater than or equal to 10-µF, PVDD-rated.
C_{DVDD} (1)	DVDD	GND	1.0-µF, 6.3-V, low ESR ceramic capacitor
C_{AREF} (1)	AREF	GND	0.1-µF, 6.3-V, low ESR ceramic capacitor
C_{VCP}	VCP	PVDD	1-µF 16-V, low ESR ceramic capacitor
C_{FLY}	CPH	CPL	0.1-µF, PVDD-rated, low ESR ceramic capacitor
R_{nFAULT}	VCC(2)	nFAULT	Pullup resistor, I_{OD} ≤ 5-mA

(1) A local bypass capacitor is recommended to reduce noise on the external low voltage power supply. If another bypass capacitor is within close proximity of the device for the external low voltage power supply and noise on the power supply is minimal, it is optional to remove this component.
(2) VCC is not a pin on the device, but the external low voltage power supply.

7.3.2 Device Interface Variants

The DRV8106-Q1 family of devices support two different interface modes (SPI and hardware) to allow the end application to design for either flexibility or simplicity. The two interface modes share the same four pins, allowing the different versions to be pin to pin compatible. This allows for application designers to evaluate with one interface version and potentially switch to another with minimal modifications to their design.

7.3.2.1 Serial Peripheral Interface (SPI)

The SPI device variant supports a serial communication bus that allows for an external controller to send and receive data with the DRV8106-Q1. This allows for the external controller to configure device settings and read detailed fault information. The interface is a four wire interface utilizing the SCLK, SDI, SDO, and nSCS pins.

- The nSCS pin is the chip select input. A logic low signal on this pin enables SPI communication.
- The SCLK pin is an input which accepts a clock signal to determine when data is captured and propagated on SDI and SDO.
- The SDI pin is the data input
- The SDO pin is the data output. The SDO pin uses a push-pull output structure referenced to the DVDD input.

For more information on the SPI, see the SPI Interface section

7.3.2.2 Hardware (H/W)

Hardware interface devices convert the four SPI pins into four resistor configurable inputs, GAIN, VDS, IDRIVE, and MODE. This allows for the application designer to configure the most commonly used device settings by tying the pin logic high or logic low, or with a simple pullup or pulldown resistor. This removes the requirement for an SPI bus from the external controller. General fault information can still be obtained through the nFAULT pin.

The hardware interface settings are latched on power up of the device. They can reconfigured by putting the device in sleep mode with the nSLEEP pin, changing the setting, and reenabling the device through nSLEEP.

- The GAIN pin configures the current shunt amplifier gain
- The VDS pin configures the voltage threshold of the V_{DS} overcurrent monitors.
- The IDRIVE pin configures the gate drive current strength.

For more information on the hardware interface, see the Pin Diagrams section.

7.3.3 Input PWM Modes

7.3.3.1 Half-Bridge Control

The half-bridge gate driver is controlled through the IN1/EN and nHIZ1 inputs pins. The nHIZ1 signal has priority over the IN1/EN signal. The DRV8106-Q1 internally handles the dead-time generation between high-side and low-side switching so that a single PWM input can control the half-bridge.

On SPI device variants, the IN1/EN and HIZ1 signals can also be controlled through the SPI registers. The IN1/EN SPI control can be enabled through the IN1/EN_MODE register setting and the signal is controlled through S_IN1/EN register setting. The HIZ1 signal is the logic OR of the nHIZ1 pin and S_HIZ1 register setting. The nHIZx pins should be tied to DVDD if this function is not required.

Table 7-2. Half-Bridge Control

nHIZ1	IN1/EN	GH1	GL1	SH1
0	X	L	L	Z
1	0	L	H	L
1	1	H	L	H

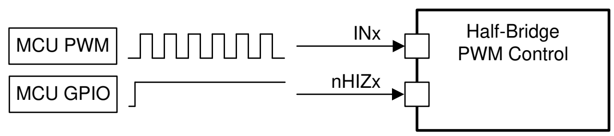


Figure 7-3. Half-Bridge Control

7.3.4 Smart Gate Driver

The DRV8106-Q1 provides an advanced, adjustable floating smart gate driver architecture to provide advanced MOSFET control and robust switching performance. The DRV8106-Q1 provides driver functions for slew rate control and a driver state machine for dead-time handshaking, parasitic dV/dt gate coupling prevention, and MOSFET gate fault detection.

Smart Gate Driver Core Functions:

- Gate Driver Functional Block Diagram
- Slew Rate Control (IDRIVE)
- Gate Drive State Machine (TDRIVE)

Table 7-3. Smart Gate Driver Terminology Descriptions

Core Function	Terminology	Description
IDRIVE / TDRIVE	I_{DRVP}	Programmable gate drive source current for adjustable MOSFET slew rate control. Configured with the IDRVP_x control register or IDRIVE pin.
	I_{DRVN}	Programmable gate drive sink current for adjustable MOSFET slew rate control. Configured with the IDRVN_x control register or IDRIVE pin.
	I_{HOLD}	Fixed gate driver hold pull up current during non-switching period.
	I_{STRONG}	Fixed gate driver strong pull down current during non-switching period.
	t_{DRIVE}	$I_{DRVP/N}$ drive current duration before I_{HOLD} or I_{STRONG}. Also provides V_{GS} and V_{DS} fault monitor blanking period. Configured with the VGS_TDRV_x control register.
	t_{PD}	Propagation delay from logic control signal to gate driver output change.
	t_{DEAD}	Body diode conduction period between high-side and low-side switch transition. Configured with the TDEAD_x control register.

7.3.4.1 Functional Block Diagram

Figure 7-4 shows a high level function block diagram for the half-bridge gate driver architecture. The gate driver blocks provide a variety of functions for MOSFET control, feedback, and protection. This includes complimentary, push-pull high-side and low-side gate drivers with adjustable drive currents, control logic level shifters, V_{DS} and V_{GS} feedback comparators, a high-side Zener clamp, plus passive and active pulldown resistors.

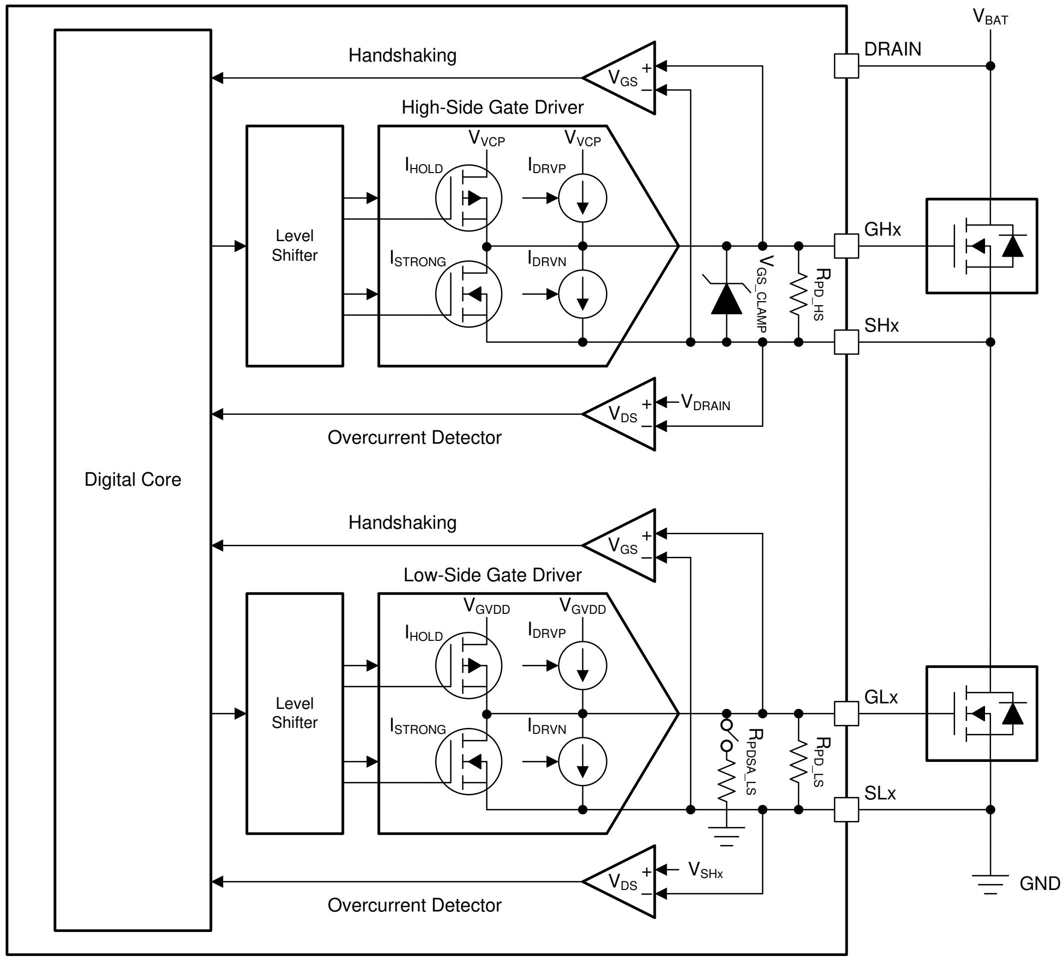


Figure 7-4. Gate Driver Functional Block Diagram

7.3.4.2 Slew Rate Control (IDRIVE)

The IDRIVE component of the smart gate drive architecture implements adjustable gate drive current control to adjust the external MOSFET V_{DS} slew rate. This is achieved by implementing adjustable pull up (I_{DRVP}) and pull down (I_{DRVN}) current sources for the internal gate driver architecture.

The external MOSFET V_{DS} slew rates are a critical factor for optimizing radiated and conducted emissions, diode reverse recovery, dV/dt parasitic gate coupling, and overvoltage or undervoltage transients on the switch-node of the half-bridge. IDRIVE operates on the principle that the V_{DS} slew rates are predominantly determined by the rate of the gate charge (or gate current) delivered during the MOSFET Q_{GD} or Miller charging region. By allowing the gate driver to adjust the gate current, it can effectively control the slew rate of the external power MOSFETs.

IDRIVE allows the DRV8106-Q1 to dynamically change the gate driver current setting through the IDRVP_x and IDRVN_x SPI registers or IDRIVE pin on H/W interface devices. The device provides 16 settings between the 0.5-mA and 62-mA range for the source and sink currents as shown in Table 7-4. The peak gate drive current is available for the t_{DRIVE} duration. After the MOSFET is switched and the t_{DRIVE} duration expires, the gate driver switches to a hold current (I_{HOLD}) for the pull up source current to limit the output current in case of a short circuit condition and to improve the efficiency of the driver.

Table 7-4. IDRIVE Source (I_{DRVP}) and Sink (I_{DRVN}) Current

IDRVP_x / IDRVN_x	Source / Sink Current (mA)
0000b	0.5
0001b	1
0010b	2
0011b	3
0100b	4
0101b	6
0110b	8
0111b	12
1000b	16
1001b	20
1010b	24
1011b	28
1100b	31
1101b	40
1110b	48
1111b	62

7.3.4.3 Gate Drive State Machine (TDRIVE)

The TDRIVE component of the smart gate drive architecture is an integrated gate drive state machine that provides automatic dead time insertion, parasitic dV/dt gate coupling prevention, and MOSFET gate fault detection.

The first component of the TDRIVE state machine is an automatic dead time handshake. Dead time is the period of body diode conduction time between the switching of the external high-side and low-side MOSFET to prevent any cross conduction or shoot through. The DRV8106-Q1 uses V_{GS} monitors to implement a break and then make dead time scheme by measuring the external MOSFET V_{GS} voltage to determine when to properly enable the external MOSFETs. This scheme allows the gate driver to adjust the dead time for variations in the system such as temperature drift, aging, voltage fluctuations, and variation in the external MOSFET parameters. An additional fixed digital dead time (t_{DEAD_D}) can be inserted if desired and is adjustable through the SPI registers.

The second component focuses on preventing parasitic dV/dt gate charge coupling. This is implemented by enabling a strong gate current pulldown (I_{STRONG}) whenever the opposite MOSFET in the half-bridge is switching. This feature helps remove parasitic charge that couples into the external MOSFET gate when the half-bridge switch node is rapidly slewing.

The third component implements a gate fault detection scheme to detect an issue with the gate voltage. This is used to detect pin-to-pin solder defects, a MOSFET gate failure, or a gate stuck high or stuck low voltage condition. This is done by using the V_{GS} monitors to measure the gate voltage after the end of the t_{DRIVE} time. If the gate voltage has not reached the proper threshold, the gate driver will report the corresponding fault condition. To ensure a false fault is not detected, a t_{DRIVE} time should be selected that is longer than the time required to charge or discharge the MOSFET gate. The t_{DRIVE} time does not impact the PWM minimum duration and will terminate early if another PWM command is received.

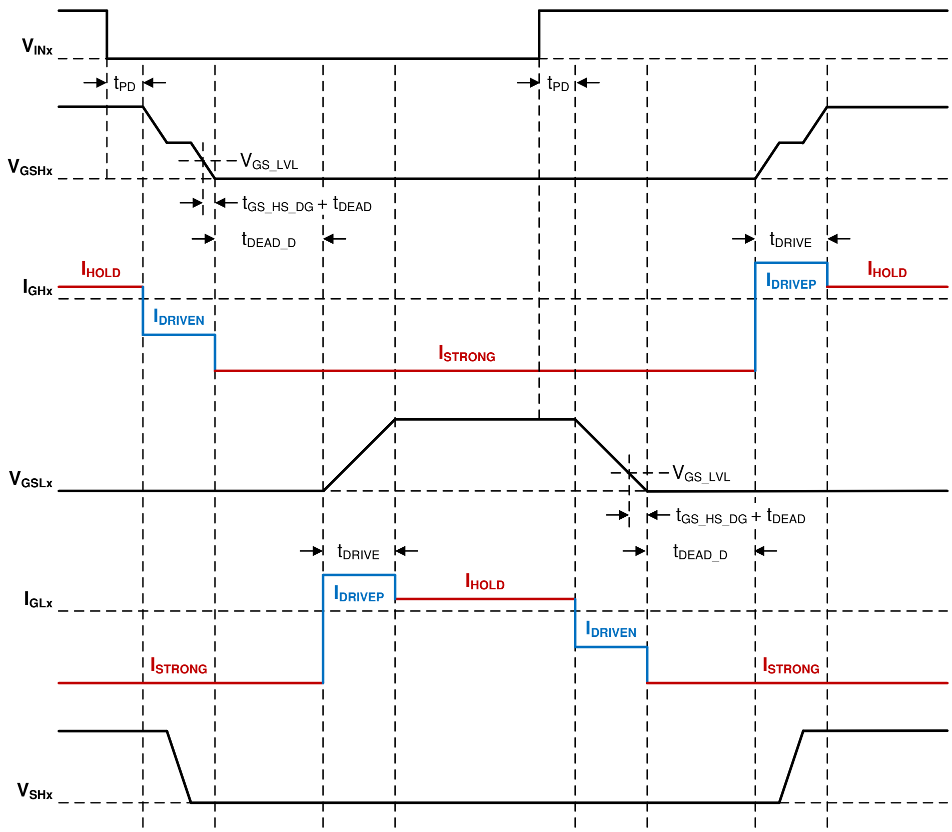


Figure 7-5. TDRIVE State Machine

7.3.5 Doubler (Single-Stage) Charge Pump

The high-side gate drive voltage for the external MOSFET is generated using a doubler charge pump that operates from the PVDD voltage supply input. The charge pump allows the high-side gate drivers to properly bias the external N-channel MOSFET with respect to its source voltage across a wide input supply voltage range. The charge pump output is regulated to maintain a fixed voltage respect to V_{PVDD} and supports an average output current capability of 15-mA. The charge pump is continuously monitored for an undervoltage event to prevent under driven MOSFET conditions.

Since the charge pump is regulated to the PVDD pin voltage the device is not designed to support significant voltage differences between the PVDD and DRAIN pins and these should be limited.

The charge pumps requires a low ESR, 1-µF, 16-V ceramic capacitor (X5R or X7R recommended) between the PVDD and VCP pins to act as the storage capacitor. Additionally, a low ESR, 100-nF, PVDD-rated ceramic capacitor (X5R or X7R recommended) is required between the CPH and CPL pins to act as the flying capacitor.

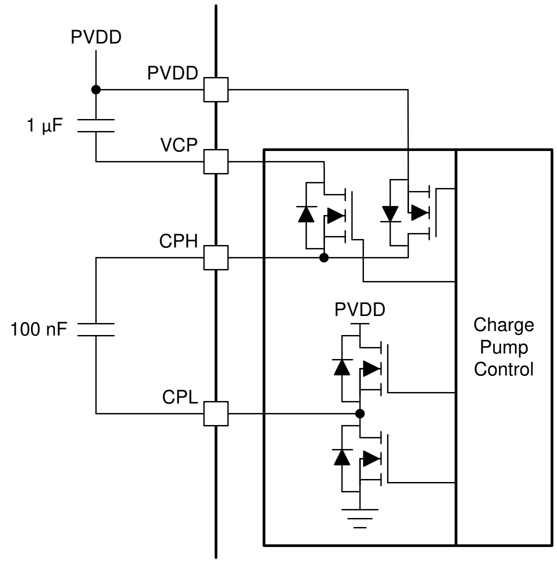


Figure 7-6. Charge Pump Architecture

7.3.6 Wide Common Mode Differential Current Shunt Amplifier

The DRV8106-Q1 integrates a high-performance, wide common-mode, bidirectional, current-shunt amplifier for current measurements using a shunt resistor in the external half-bridge. Current measurements are commonly used to implement overcurrent protection, external torque control, or commutation with an external controller. Due to the high common-mode range of the shunt amplifier it can support low-side, high-side, or inline shunt configurations. The current shunt amplifiers include features such as programmable gain, unidirectional and bidirectional support, output blanking and sample and hold switch, and a dedicated voltage reference pin (AREF) to set a mid point bias voltage for the amplifier output. A simplified block diagram is shown in Figure 7-7. SP should connect to the positive terminal of the shunt resistor and SN should connect to the negative terminal of the shunt resistor. If the amplifier is not utilized, the AREF, SN, SP inputs can be tied to AGND, AGND to PCB GND and the SO output left floating.

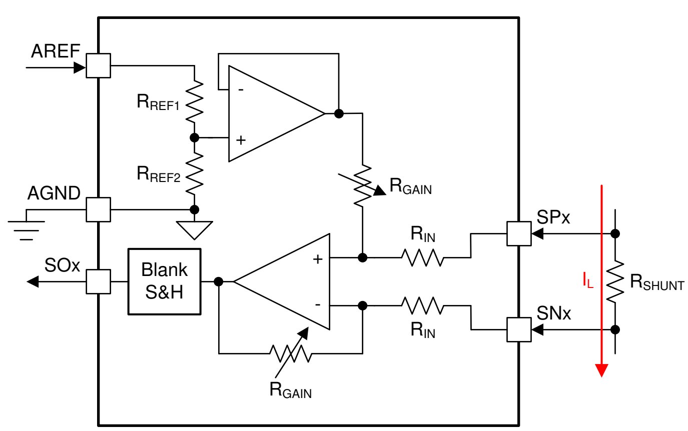


Figure 7-7. Amplifier Simplified Block Diagram

A detailed block diagram is shown in Figure 7-8. The wide common mode amplifier is implemented with a two stage differential architecture. The 1st differential stage supports a wide common mode input, differential output, and has a fixed gain, G = 2. The 2nd differential stage supports a variable gain adjustment, G = 5, 10, 20, or 40. The total gain of the two stages will be G = 10, 20, 40, or 80.

The amplifier can also generate an output voltage bias through the AREF pin. The AREF pin goes to a divider network, a buffer, and then sets the output voltage bias for the differential amplifier. On SPI device variants, the gain is configured through the register setting CSA_GAIN and the reference division ratio through CSA_DIV. On H/W device variants, the reference division ratio is fixed to V_{AREF} / 2. The gain is configured through the GAIN pin.

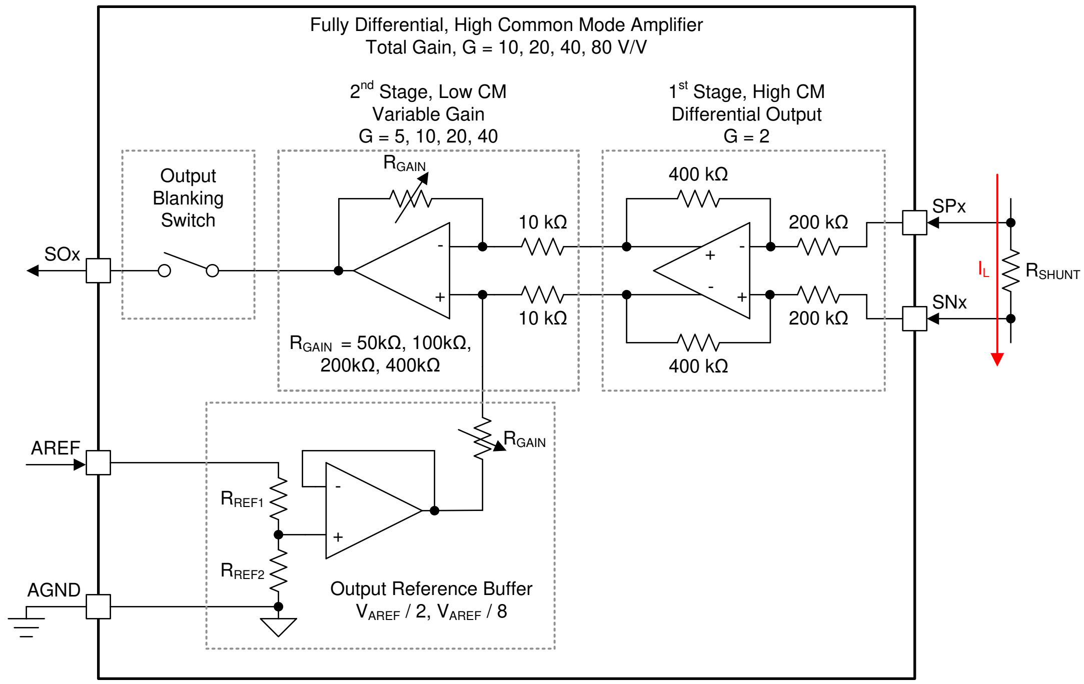


Figure 7-8. Amplifier Detailed Block Diagram

Lastly, the amplifier has an output blanking or sample and hold switch. This option is only available on SPI device variants. The output switch can be used to disconnect the amplifier output during PWM switching to reduce output noise (blanking) or during motor braking to maintain the output value if the shunt is used in high-side or low-side configuration (sample and hold). The blanking circuit can be set trigger on the active half-bridge (half-bridge 1 or half-bridge 2) through the CSA_BLK_SEL register setting. The blanking period can be configured through the CSA_BLK register setting. The sample and hold circuit can be enabled with the CSA_SH_EN register setting. When active, the sample and hold will trigger whenever the driver enters high-side or low-side braking. To utilize either the blanking or sample and hold functions and output hold up capacitor will be required to stabilize the amplifier output when it is disconnected. Typically it is recommended, that this capacitor be after a series resistor in a RC filter configuration to limit direct capacitance seen directly at the amplifier output.

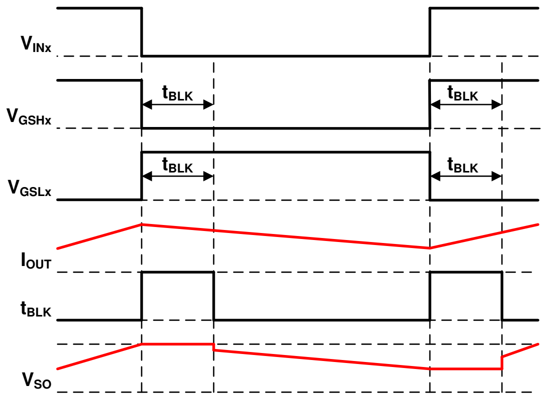


Figure 7-9. DRV8106-Q1 Amplifier Blanking Example

Figure 7-9 shows an example of the amplifier blanking function. This function can be utilized to hi-Z the amplifier output during a switching transition, but is not required by default. This function can be beneficial if noise due to wide-common mode swings or ground shifts are occurring during the PWM switching transition and interfering with the amplifier output. As shown in the image, the blanking function operates by disabling the amplifier output for a period of time after a transition on either GHx or GLx. This period of time is determined by the t_{BLK} setting configured through the CSA_BLK register setting.

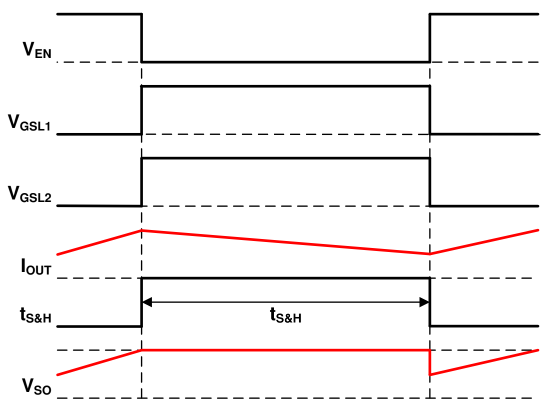


Figure 7-10. DRV8106-Q1 Amplifier Sample & Hold Example

Figure 7-10 show an example of the amplifier sample and hold function. This function can be utilized to hi-Z the amplifier output when the current is recirculating in the H-bridge, but is not required by default. The function can be beneficial if the shunt resistor is configured into the low-side or the high-side of the H-bridge in which during current recirculation the current information is lost. As shown in the image, the sample and hold function will hold the previous state of the amplifier output since the output capacitor will remain charged. The amplifier will resume operation when the H-bridge leaves the recirculation state.

7.3.7 Pin Diagrams

This section presents the I/O structure of all the digital input and output pins.

7.3.7.1 Logic Level Input Pin (DRVOFF, IN1/EN, nHIZx, nSLEEP, nSCS, SCLK, SDI)

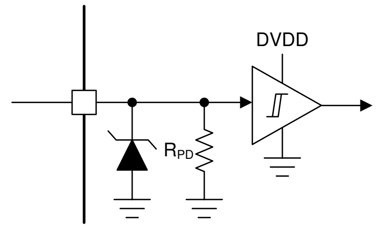


Figure 7-11. Input Pin Structure

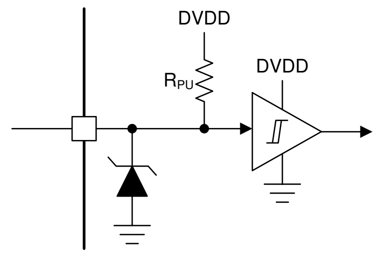


Figure 7-12. Input Pin Structure (nSCS)

7.3.7.2 Logic Level Push Pull Output (SDO)

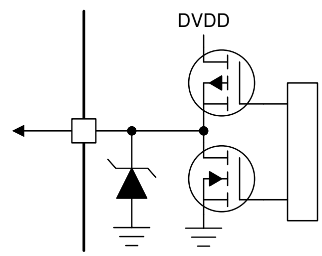


Figure 7-13. Push Pull Output Structure (SDO)

7.3.7.3 Logic Level Open Drain Output (nFAULT)

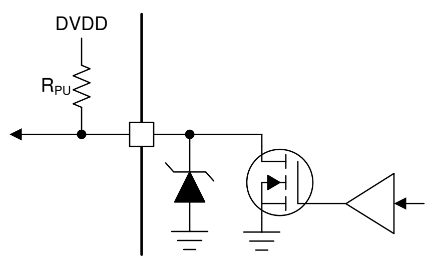


Figure 7-14. Open Drain Output Structure (nFAULT)

7.3.7.4 Quad-Level Input (GAIN)

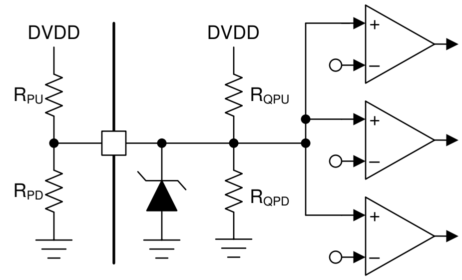


Figure 7-15. Quad-Level Input Structure (GAIN)

7.3.7.5 Six-Level Input (IDRIVE, VDS)

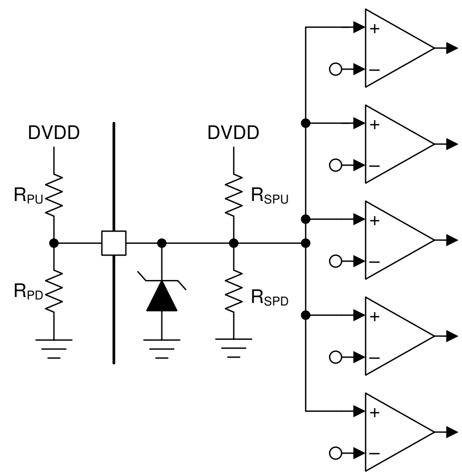


Figure 7-16. Six-Level Input Structure (IDRIVE, VDS)

7.3.8 Protection and Diagnostics

7.3.8.1 Gate Driver Disable and Enable (DRVOFF and EN_DRV)

The DRV8106-Q1 provides a dedicated driver disable with the DRVOFF pin. When DRVOFF is asserted, it will enable the gate driver pull downs regardless of the pin or SPI inputs.

On SPI device variants, the EN_DRV function is provide for a controlled power up sequence. After device power up the gate drivers remain disabled until the EN_DRV register bit is asserted. This allows for the system to power up and conduct configuration sequences before the gate drivers are enabled. On H/W devices, this functionality is not provided and the driver will automatically enable after power up.

7.3.8.2 Fault Reset (CLR_FLT)

The DRV8106-Q1 provides a specific sequence to clear fault conditions from the driver and resume operation. This function is provided through the CLR_FLT register bit. To clear fault reporting the CLR_FLT register bit must be asserted after the fault condition is removed. After being asserted, the driver will clear the fault and reset the CLR_FLT register bit. The function is only available on SPI device variants. On H/W device variants, all faults will automatically recover once the condition is removed.

7.3.8.3 DVDD Logic Supply Power on Reset (DVDD_POR)

If at any time the input logic supply voltage on the DVDD pin falls below the V_{DVDD_POR} threshold for longer than the $t_{DVDD\_POR\_DG}$ time or the nSLEEP pin is asserted low, the device enter its inactive state disabling the gate drivers, charge pump, and protection monitors. Normal operation resumes when the DVDD undervoltage condition is removed or the nSLEEP pin is asserted high. After a DVDD power on reset (POR), the POR register bit is asserted until CLR_FLT is issued.

7.3.8.4 PVDD Supply Undervoltage Monitor (PVDD_UV)

If at any time the power supply voltage on the PVDD pin falls below the V_{PVDD_UV} threshold for longer than the $t_{PVDD\_UV\_DG}$ time, the DRV8106-Q1 detects a PVDD undervoltage condition. After detecting the undervoltage condition, the gate driver pull downs are enabled, charge pump disabled and nFAULT pin, FAULT register bit, and PVDD_UV register bit asserted.

On SPI device variants, the PVDD undervoltage monitor can recover in two different modes set through the PVDD_UV_MODE register setting.

- **Latched Fault Mode:** After the undervoltage condition is removed, the fault state remains latched and charge pump disabled until CLR_FLT is issued.
- **Automatic Recovery Mode:** After the undervoltage condition is removed, the nFAULT pin and FAULT register bit are automatically cleared and the charge pump automatically reenabled. The PVDD_UV register bit remains latched until CLR_FLT is issued.

On H/W device variants, the PVDD undervoltage monitor is fixed to automatic recovery mode.

7.3.8.5 PVDD Supply Overvoltage Monitor (PVDD_OV)

If the power supply voltage on the PVDD pin exceeds the V_{PVDD_OV} threshold for longer than the $t_{PVDD\_OV\_DG}$ time, the DRV8106-Q1 detects a PVDD overvoltage condition and action is taken according to the PVDD_OV_MODE register setting. The overvoltage threshold and deglitch time can be adjusted through the PVDD_OV_LVL and PVDD_OV_DG register settings.

On SPI device variants, the PVDD overvoltage monitor can respond and recover in four different modes set through the PVDD_OV_MODE register setting.

- **Latched Fault Mode:** After detecting the overvoltage condition, the gate driver pull downs are enabled and nFAULT pin, FAULT register bit, and PVDD_OV register bit asserted. After the overvoltage condition is removed, the fault state remains latched until CLR_FLT is issued.
- **Automatic Recovery Mode:** After detecting the overvoltage condition, the gate driver pull downs are enabled and nFAULT pin, FAULT register bit, and PVDD_OV register bit asserted. After the overvoltage condition is removed, the nFAULT pin and FAULT register bit are automatically cleared and the driver automatically reenabled. The PVDD_OV register bit remains latched until CLR_FLT is issued.
- **Warning Report Only Mode:** The PVDD overvoltage condition is reported in the WARN and PVDD_OV register bits. The device will not take any action. The warning remains latched until CLR_FLT is issued.
- **Disabled Mode:** The PVDD overvoltage monitor is disabled and will not respond or report.

On H/W device variants, the PVDD overvoltage monitor is disabled.

7.3.8.6 VCP Charge Pump Undervoltage Lockout (VCP_UV)

If at any time the voltage on the VCP pin falls below the V_{VCP_UV} threshold for longer than the $t_{VCP\_UV\_DG}$ time, the DRV8106-Q1 detects a VCP undervoltage condition. After detecting the undervoltage condition, the gate driver pull downs are enabled and nFAULT pin, FAULT register bit, and VCP_UV register bit asserted. The undervoltage threshold can be adjusted through the VCP_UV_LVL register setting.

On SPI device variants, the VCP undervoltage monitor can recover in two different modes set through the VCP_UV_MODE register setting.

- **Latched Fault Mode:** Additionally the charge pump is disabled in latched fault mode. After the undervoltage condition is removed, the fault state remains latched and charge pump disabled until CLR_FLT is issued.
- **Automatic Recovery Mode:** After the undervoltage condition is removed, the nFAULT pin and FAULT register bit are automatically cleared and the driver automatically reenabled. The VCP_UV register bit remains latched until CLR_FLT is issued.

On H/W device variants, the VCP undervoltage monitor is fixed to automatic recovery mode and the threshold to 2-V.

7.3.8.7 MOSFET V_{DS} Overcurrent Protection (VDS_OCP)

If the voltage across the V_{DS} overcurrent comparator exceeds the V_{DS_LVL} for longer than the t_{DS_DG} time, the DRV8106-Q1 detects a V_{DS} overcurrent condition. The voltage threshold and deglitch time can be adjusted through the VDS_LVL and VDS_DG register settings. Additionally, in independent half-bridge and split HS/LS PWM control (BRG_MODE = 00b, 11b) the device can be configured to disable all half-bridges or only the associated half-bridge in which the fault occurred through the VDS_IND register setting.

On SPI device variants, the V_{DS} overcurrent monitor can respond and recover in four different modes set through the VDS_MODE register setting.

- **Latched Fault Mode:** After detecting the overcurrent event, the gate driver pull downs are enabled and nFAULT pin, FAULT register bit, and associated VDS register bit asserted. After the overcurrent event is removed, the fault state remains latched until CLR_FLT is issued.
- **Cycle by Cycle Mode:** After detecting the overcurrent event, the gate driver pull downs are enabled and nFAULT pin, FAULT register bit, and associated VDS register bit asserted. The next PWM input will clear the nFAULT pin and FAULT register bit and reenable the driver automatically. The associated VDS register bit will remain asserted until CLR_FLT is issued.
- **Warning Report Only Mode:** The overcurrent event is reported in the WARN and associated VDS register bits. The device will not take any action. The warning remains latched until CLR_FLT is issued.
- **Disabled Mode:** The V_{DS} overcurrent monitors are disabled and will not respond or report.

On H/W device variants, the V_{DS} overcurrent mode is fixed to cycle by cycle and t_{VDS_DG} is fixed to 4 µs. Independent half-bridge shutdown is automatically enabled for the independent half-bridge and split HS/LS PWM control modes. Additionally, the V_{DS} overcurrent protection can be disabled through level 6 of the VDS pin multi-level input.

When a V_{DS} overcurrent fault occurs, the gate pull down current can be configured in order to increase or decrease the time to disable the external MOSFET. This can help to avoid a slow-turn off during high-current short circuit conditions. This setting is configure through the VDS_IDRVN register setting on SPI devices. On hardware devices, this setting is automatically matched to the programmed I_{DRVN} current.

7.3.8.8 Gate Driver Fault (VGS_GDF)

If the V_{GS} voltage does not cross the the V_{GS_LVL} comparator level for longer than the t_{DRIVE} time, the DRV8106-Q1 detects a V_{GS} gate fault condition. Additionally, in independent half-bridge and split HS/LS PWM control (BRG_MODE = 00b, 11b) the device can be configured to disable all half-bridges or only the associated half-bridge in which the gate fault occurred through the VGS_IND register setting.

On SPI device variants, the V_{GS} gate fault monitor can respond and recover in four different modes set through the VGS_MODE register setting.

- **Latched Fault Mode:** After detecting the gate fault event, the gate driver pull downs are enabled and nFAULT pin, FAULT register bit, and associated VGS register bit asserted. After the gate fault event is removed, the fault state remains latched until CLR_FLT is issued.
- **Cycle by Cycle Mode:** After detecting the gate fault event, the gate driver pull downs are enabled and nFAULT pin, FAULT register bit, and associated VGS register bit asserted. The next PWM input will clear the nFAULT pin and FAULT register bit and reenable the driver automatically. The associated VGS register bit will remain asserted until CLR_FLT is issued.
- **Warning Report Only Mode:** The overcurrent event is reported in the WARN and associated VGS register bits. The device will not take any action. The warning remains latched until CLR_FLT is issued.
- **Disabled Mode:** The V_{GS} gate fault monitors are disabled and will not respond or report.

On H/W device variants, the V_{GS} gate fault mode is fixed to cycle by cycle and t_{DRIVE} is fixed to 4 µs. Independent half-bridge shutdown is automatically enabled for the independent half-bridge and split HS/LS PWM control modes. Additionally, the V_{GS} gate fault protection can be disabled through level 6 of the VDS pin multi-level input.

7.3.8.9 Thermal Warning (OTW)

If the die temperature exceeds the T_{OTW} thermal warning threshold the DRV8106-Q1 detects an overtemperature warning and asserts the WARN and OTW register bits. After the overtemperature condition is removed the WARN and OTW register bits remain asserted until CLR_FLT is issued.

On H/W device variants, the overtemperature warning is not detected or reported.

7.3.8.10 Thermal Shutdown (OTSD)

If the die temperature exceeds the T_{OTSD} thermal shutdown threshold the DRV8106-Q1 detects an overtemperature fault. After detecting the overtemperature fault, the gate driver pull downs are enabled, the charge pump disabled and nFAULT pin, FAULT register bit, and OTSD register bit asserted. After the overtemperature condition is removed the fault state remains latched until CLR_FLT is issued.

On H/W device variants, after the overtemperature condition is removed, the nFAULT pin is automatically cleared and the driver and charge pump automatically reenabled.

7.3.8.11 Offline Short Circuit and Open Load Detection (OOL and OSC)

The device provides the necessary hardware to conduct offline short circuit and open load diagnostics of the external power MOSFETs and load. This is accomplished by an integrated pull up and pull down current source on the SHx pin which connect to the external half-bridge switch-node. The offline diagnostics are controlled by the associated registers bits in the OLSC_CTRL register. First, the offline diagnostic mode needs to be enabled through the OLSC_EN register setting. Then the individual current sources can be enabled through the PD_SHx and PU_SHx register settings.

The voltage on the SHx pin will be continuously monitored through the internal V_{DS} comparators. During the diagnostic state the V_{DS} comparators will report the real-time voltage feedback on the SHx pin node in the SPI registers in the associated VDS register status bit.

Before enabling the offline diagnostics it is recommended to place the external MOSFET half-bridges in the disabled state through the EN_DRV register setting. Additionally, the V_{DS} comparator threshold (VDS_LVL) should be adjusted to 1-V or greater to ensure enough headroom for the internal blocking diode forward voltage drop.

On H/W device variants, this feature is not available.

To properly conduct the offline diagnostic sequence the following steps should be followed.

- Set EN_DRV control register to 0b to disable the output drivers.
- Set OLSC_EN control register to 1b to enable the offline diagnostics.
- Enable the PD_SHx and PU_SHx control registers accordingly.
- Read back the VDS_x status registers to determine output status.
- Disable the PD_SHx and PD_SHx control registers.
- Set OLSC_EN control register to 0b to disable the offline diagnostics.
- Set EN_DRV control register to 1b to enable the output drivers again.

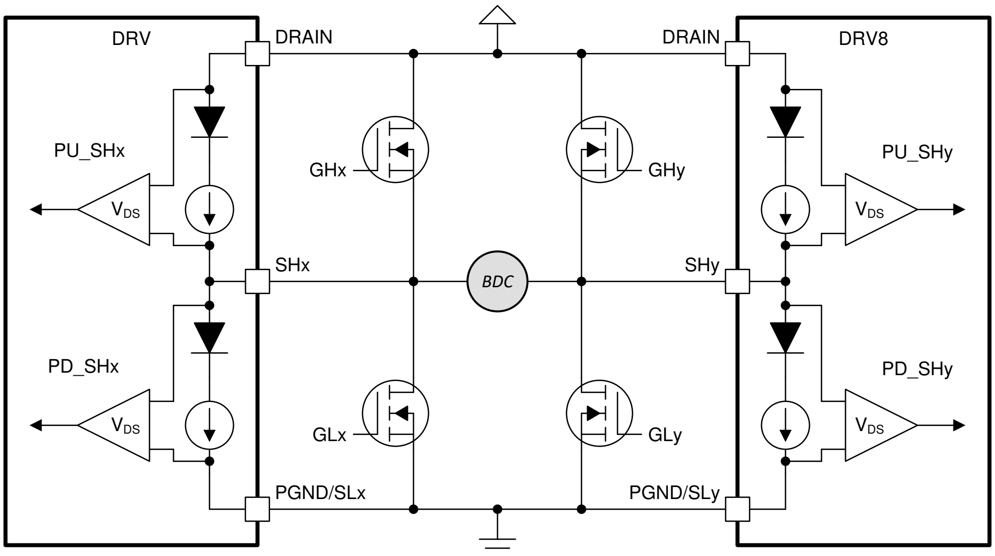


Figure 7-17. Offline Diagnostics

7.3.8.12 Fault Detection and Response Summary Table

Table 7-5. Fault Detection and Response Summary

NAME	CONDITION	SPI BIT	MODE	DIGITAL CORE	CHARGE PUMP	GATE DRIVERS	CURRENT SENSE	RESPONSE
Disable Driver	DRVOFF = High	n/a	n/a	Active	Active	Pull Down	Active	n/a
DVDD Power-on-Reset	DVDD < V_{DVDD_POR}	POR	n/a	Reset	Disabled	Semi-Active Pull Down	Disabled	SPI
PVDD Undervoltage	PVDD < V_{PVDD_UV}	UV, PVDD_UV	Latched	Active	Disabled	Semi-Active Pull Down	Disabled	nFAULT, SPI
			Automatic	Active	Disabled	Semi-Active Pull Down	Disabled	nFAULT, SPI
PVDD Overvoltage	PVDD > V_{PVDD_UV}	OV, PVDD_OV	Latched	Active	Active	Pull Down	Active	nFAULT, SPI
		OV, PVDD_OV	Automatic	Active	Active	Pull Down	Active	nFAULT, SPI
		OV, PVDD_OV	Warning	Active	Active	Active	Active	WARN, SPI
		n/a	Disabled	Active	Active	Active	Active	n/a
VCP Undervoltage	VCP < V_{VCP_UV}	UV, VCP_UV	Latched	Active	Disabled	Semi-Active Pull Down	Disabled	nFAULT, SPI
			Automatic	Active	Active	Semi-Active Pull Down	Disabled	nFAULT, SPI
VDS Overcurrent	VDS > V_{VDS_LVL}	DS_GS, VDS_X	Latched	Active	Active	I_{VDS_IDRVN} Pull Down	Active	nFAULT, SPI
			Cycle	Active	Active	I_{VDS_IDRVN} Pull Down	Active	nFAULT, SPI
			Warning	Active	Active	Active	Active	WARN, SPI
			Disabled	Active	Active	Active	Active	n/a
VGS Gate Fault	VGS > V_{VGS_LVL}	DS_GS, VGS_X	Latched	Active	Active	Pull Down	Active	nFAULT, SPI
			Cycle	Active	Active	Pull Down	Active	nFAULT, SPI
			Warning	Active	Active	Active	Active	WARN, SPI
			Disabled	Active	Active	Active	Active	n/a
Thermal Warning	$T_J > T_{OTW}$	OT, OTW	Automatic	Active	Active	Active	Active	WARN, SPI
Thermal Shutdown	$T_J > T_{OTSD}$	OT, OTSD	Latched	Active	Disabled	Semi-Active Pull Down	Disabled	nFAULT, SPI
Offline Open Load	n/a	VDS_X	MCU	Active	Active	Pull Down	Active	SPI
Offline Short Circuit	n/a	VDS_X	MCU	Active	Active	Pull Down	Active	SPI

7.4 Device Function Modes

7.4.1 Inactive or Sleep State

When the nSLEEP pin is logic low or the DVDD power supply is below the V_{DVDD_POR} threshold, the device enters a low power sleep state to reduce device quiescent current draw by the device. In this state, all major functional blocks are disabled aside from a low power monitor on the nSLEEP pin. Passive gate pull downs are provided for the external MOSFET gates to maintain the MOSFETs in an off state.

7.4.2 Standby State

When the nSLEEP pin is logic high and DVDD input has crossed the V_{DVDD_POR} threshold, the device enters a power on standby state after t_{WAKE} delay. The digital core and SPI communication will be active but the charge pump and gate drivers will remain disabled until the PVDD input has cross the V_{PVDD_UV} threshold. In this state, the SPI registers can be programmed and faults reported, but no gate driver operation is possible.

7.4.3 Operating State

When the nSLEEP pin is logic high, the DVDD input has crossed the V_{DVDD_POR} threshold, and the PVDD input has crossed the V_{PVDD_UV} threshold, the devices enters its full operating state. In this state, all major functional blocks are active aside from the gate drivers. The gate drivers must be enabled through the EN_DRV register bit before full operation can begin.

On H/W device variants, the device will automatically enable the drivers in the operating state.

7.5 Programming

7.5.1 SPI Interface

An SPI bus is used to set device configurations, operating parameters, and read out diagnostic information on the DRV8106-Q1 device. The SPI operates in slave mode and connects to a master controller. The SPI input data (SDI) word consists of a 16 bit word, with an 8 bit command and 8 bits of data. The SPI output data (SDO) word consists of the fault status indication bits and then the register data being accessed for read commands or null for write commands. The data sequence between the MCU and the SPI slave driver is shown in Figure 7-18.

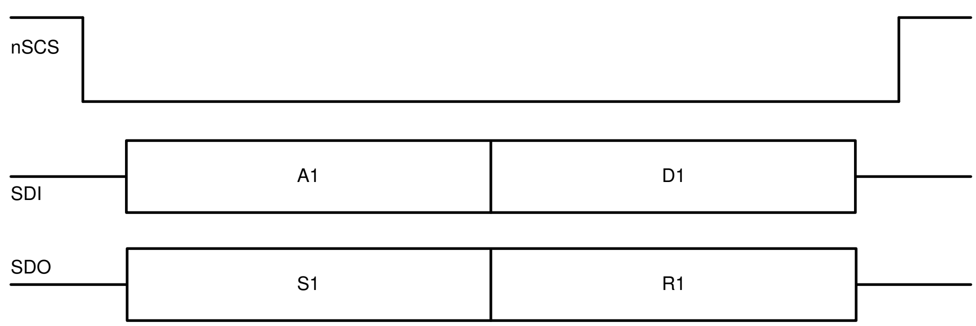


Figure 7-18. SPI Data Frame

A valid frame must meet the following conditions:

- The SCLK pin should be low when the nSCS pin transitions from high to low and from low to high.
- The nSCS pin should be pulled high between words.
- When the nSCS pin is pulled high, any signals at the SCLK and SDI pins are ignored and the SDO pin is placed in the Hi-Z state.
- Data is captured on the falling edge of SCLK and data is propagated on the rising edge of SCLK.
- The most significant bit (MSB) is shifted in and out first.
- A full 16 SCLK cycles must occur for transaction to be valid.
- If the data word sent to the SDI pin is less than or more than 16 bits, a frame error occurs and the data word is ignored.

7.5.2 SPI Format

The SDI input data word is 16 bits long and consists of the following format:

- 1 read or write bit, W (bit B14)
- 6 address bits, A (bits B13 through B8)
- 8 data bits, D (bits B7 through B0)

The SDO output data word is 16 bits long and the first 8 bits makes up the IC status register. The report word is the content of the register being accessed.

For a write command (W0 = 0), the response word consists of the fault status indication bits followed by 8 null bits.

For a read command (W0 = 1), the response word consists of the fault status indications bits followed by the data currently in the register being read.

Table 7-6. SDI Input Data Word Format

		R/W	Address						Data							
Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data	0	W0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Table 7-7. SDO Output Data Word Format

	IC Status								Report							
Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data	1	1	FAULT	WARN	DS_GS	UV	OV	OT	D7	D6	D5	D4	D3	D2	D1	D0

7.5.3 SPI Interface for Multiple Slaves

Multiple DRV8106-Q1 devices can be connected to the master controller with and without the daisy chain. For connecting a 'n' number of DRV8106-Q1 to a master controller without using a daisy chain, 'n' number of I/O resources from master controller has to utilized for nSCS pins as shown in Figure 7-19. Whereas, if the daisy chain configuration is used, then a single nSCS line can be used for connecting multiple DRV8106-Q1 devices. Figure 7-20

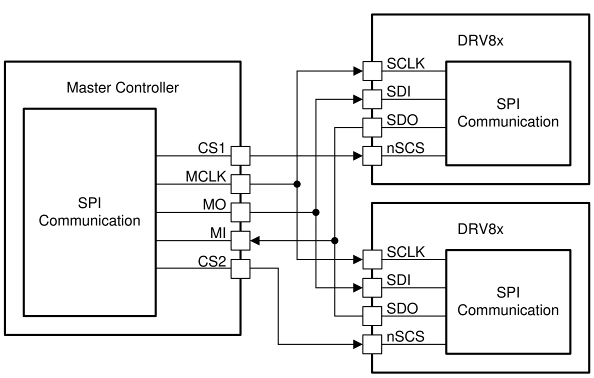


Figure 7-19. SPI Operation Without Daisy Chain

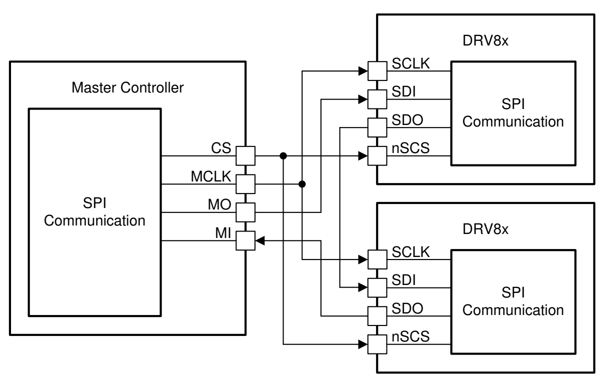


Figure 7-20. SPI Operation With Daisy Chain

7.5.3.1 SPI Interface for Multiple Slaves in Daisy Chain

The DRV8106-Q1 device can be connected in a daisy chain configuration to save GPIO ports when multiple devices are communicating to the same MCU. Figure 7-21 shows the topology when 3 devices are connected in series with waveforms.

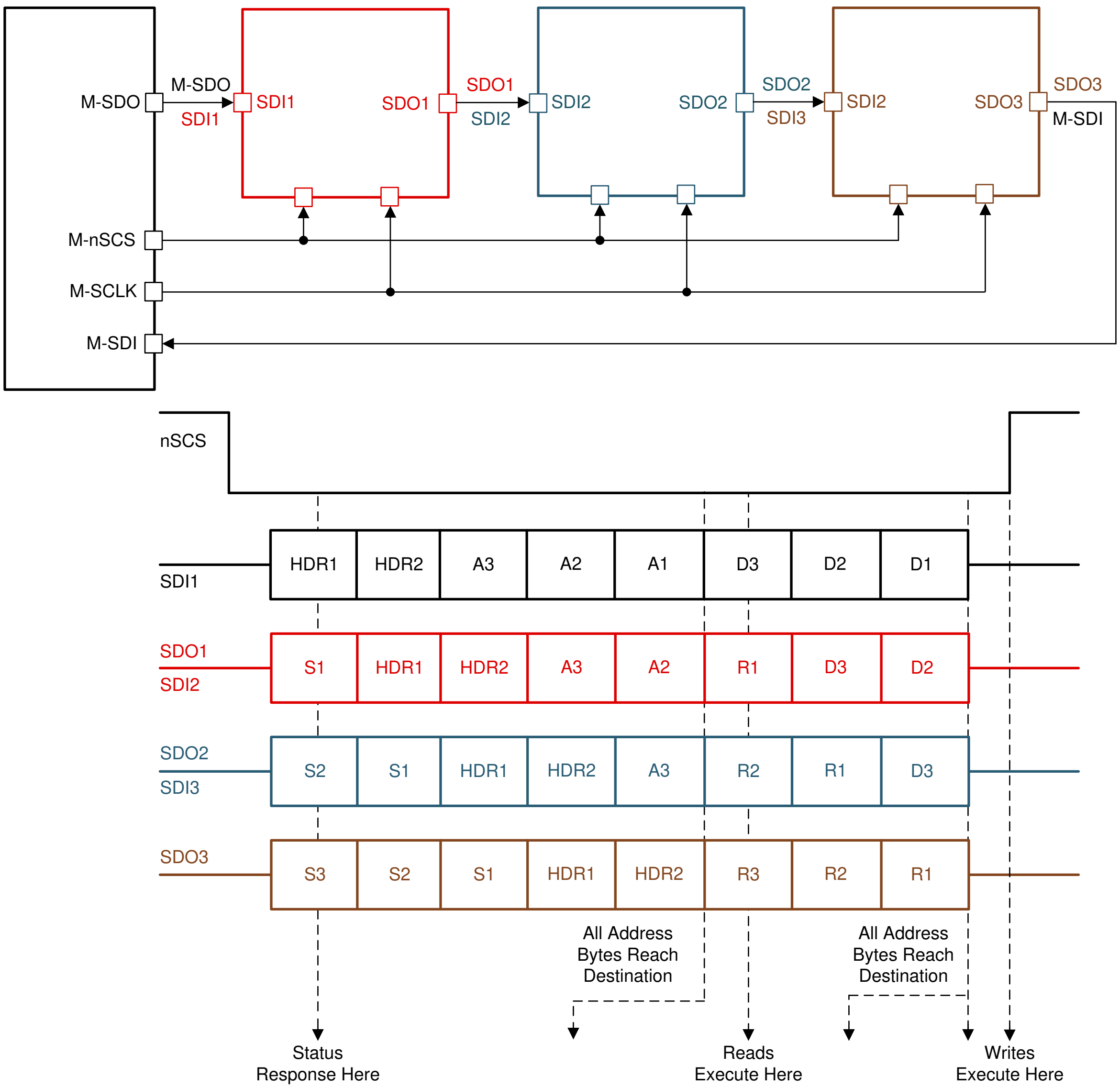


Figure 7-21. Daisy Chain SPI Operation

The first device in the chain shown above receives data from the master controller in the following format. See SDI1 in Figure 7-21

- 2 bytes of Header
- 3 bytes of Address
- 3 bytes of Data

After the data has been transmitted through the chain, the master controller receives it in the following format. See SDO3 in Figure 7-21

- 3 bytes of Status
- 2 bytes of Header (should be identical to the information controller sent)
- 3 bytes of Report

The Header bytes contain information of the number of devices connected in the chain, and a global clear fault command that will clear the fault registers of all the devices on the rising edge of the chip select (nSCS) signal. N5 through N0 are 6 bits dedicated to show the number of device in the chain as shown in Figure 7-22. Up to 63 devices can be connected in series per daisy chain connection.

The 5 LSBs of the HDR2 register are don't care bits that can be used by the MCU to determine integrity of the daisy chain connection. Header bytes must start with 1 and 0 for the two MSBs.

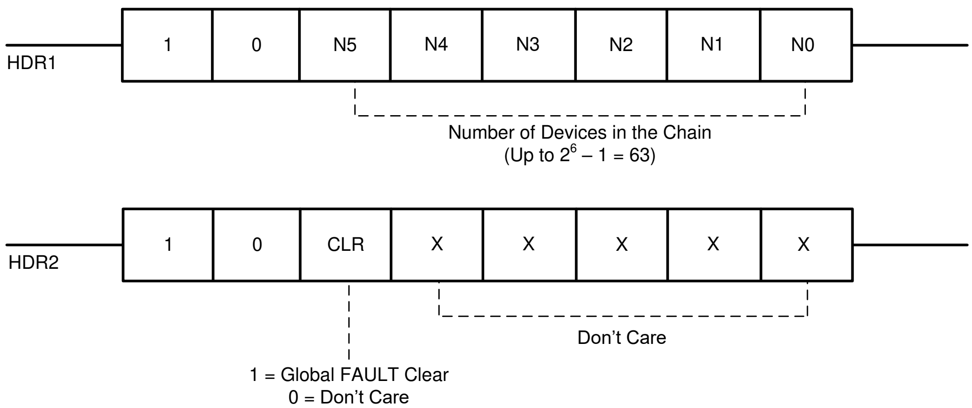


Figure 7-22. Header Bits

The Status byte provides information about the fault status register for each device in the daisy chain as shown in Figure 7-23. That way the master controller does not have to initiate a read command to read the fault status from any particular device. This saves the controller additional read commands and makes the system more efficient to determine fault conditions flagged in a device.

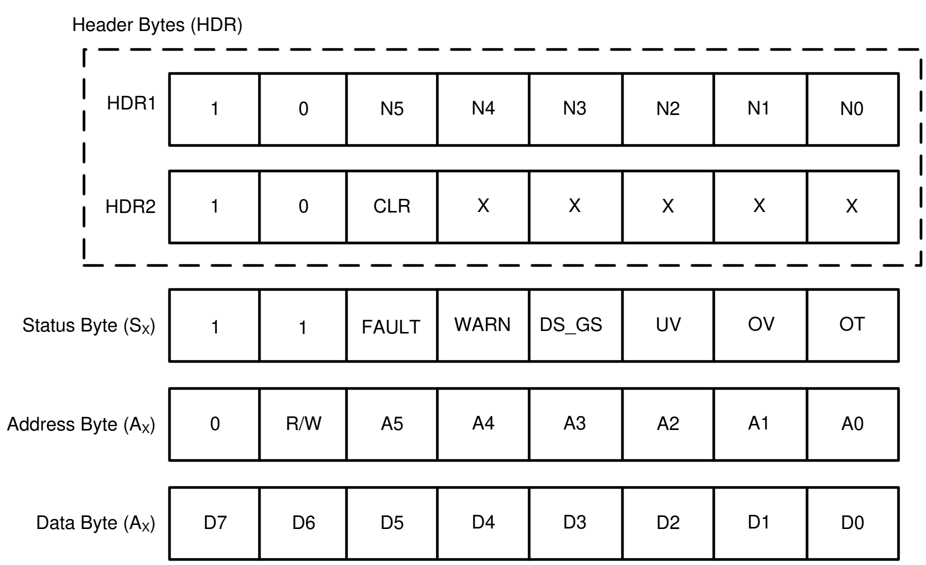


Figure 7-23. Daisy Chain Read Registers

When data passes through a device, it determines the position of itself in the chain by counting the number of Status bytes it receives following by the first Header byte. For example, in this 3 device configuration, device 2 in the chain will receive two Status bytes before receiving HDR1 byte, followed by HDR2 byte.

From the two Status bytes it knows that its position is second in the chain, and from HDR2 byte it knows how many devices are connected in the chain. That way it only loads the relevant address and data byte in its buffer and bypasses the other bits. This protocol allows for faster communication without adding latency to the system for up to 63 devices in the chain.

The address and data bytes remain the same with respect to a single device connection. The Report bytes (R1 through R3), as shown in the figure above, is the content of the register being accessed.

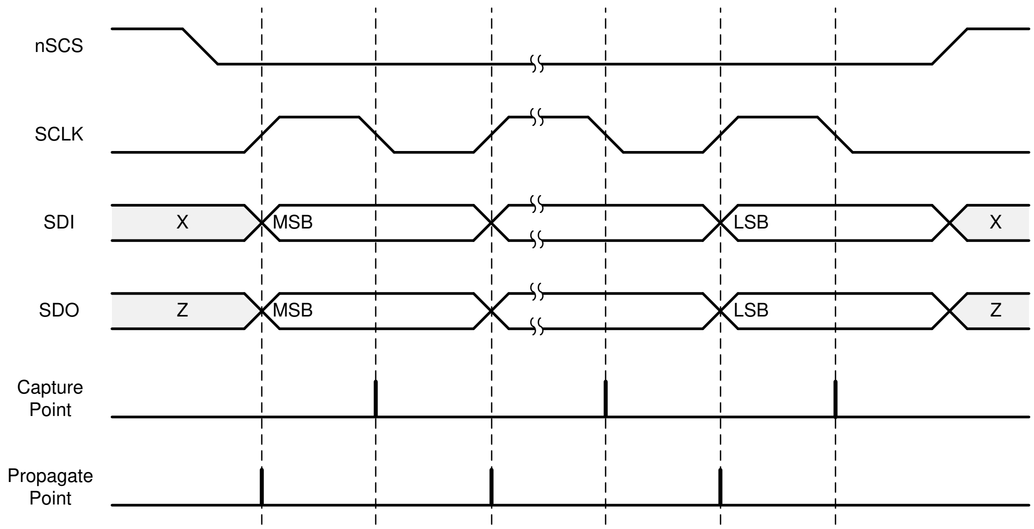


Figure 7-24. SPI Slave Timing Diagram

7.6 Register Maps

The table below lists the memory-mapped registers for the device. All register addresses not listed should be considered as reserved locations and the register contents should not be modified. Descriptions of reserved locations are provided for reference only.

Table 7-8. Register Map

Name	7	6	5	4	3	2	1	0	Type	Address
IC_STAT_1	SPI_OK	POR	FAULT	WARN	DS_GS	UV	OV	OT	R	0h
VGS_VDS_STAT	VGS_H1	VGS_L1	RSVD	RSVD	VDS_H1	VDS_L1	RSVD	RSVD	R	1h
IC_STAT_2	PVDD_UV	PVDD_OV	VCP_UV	OTW	OTSD	RSVD	CLK_FLT	ADDR_FLT	R	2h
RSVD_STAT	RSVD								R	3h
IC_CTRL	EN_DRV	SSC_DIS	IN1/EN_MODE	RVSD	LOCK			CLR_FLT	R/W	4h
BRG_CTRL	VGS_HS_DIS	RSVD		RSVD	S_IN1/EN	RSVD	S_HIZ1	RSVD	R/W	5h
DRV_CTRL_1	IDRVP_HS				IDRVN_HS				R/W	6h
DRV_CTRL_2	IDRVP_LS				IDRVN_LS				R/W	7h
DRV_CTRL_3	VGS_MODE		VGS_TDRV		VGS_TDEAD			VGS_IND	R/W	8h
VDS_CTRL_1	VDS_MODE		VDS_DG		VDS_IDRVN		VGS_LVL	VDS_IND	R/W	9h
VDS_CTRL_2	VDS_HS_LVL				VDS_LS_LVL				R/W	Ah
OLSC_CTRL	RSVD			OLSC_EN	PU_SH1	PD_SH1	RSVD	RSVD	R/W	Bh
UVOV_CTRL	PVDD_UV_MODE	PVDD_OV_MODE		PVDD_OV_DG		PVDD_OV_LVL	VCP_UV_MODE	VCP_UV_LVL	R/W	Ch
CSA_CTRL	CSA_SH_EN	CSA_BLK_SEL	CSA_BLK			CSA_DIV	CSA_GAIN		R/W	Dh

7.6.1 STATUS Registers

Table 7-9 lists the memory-mapped registers for the STATUS registers. All register offset addresses not listed in Table 7-9 should be considered as reserved locations and the register contents should not be modified.

Table 7-9. STATUS Registers

Address	Acronym	Register Name	Section
0h	IC_STAT_1	IC status register 1	Go
1h	VGS_VDS_STAT	VGS and VDS status register	Go
2h	IC_STAT_2	IC status register 2	Go
3h	RSVD_STAT	Reserved	Go

Complex bit access types are encoded to fit into small table cells. Table 7-10 shows the codes that are used for access types in this section.

Table 7-10. STATUS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

7.6.1.1 IC_STAT_1 Register (Address = 0h) [reset = 80h]

IC_STAT_1 is shown in Figure 7-25 and described in Table 7-11.

Return to Summary Table.

Status register with the primary IC fault bits

Figure 7-25. IC_STAT_1 Register

7	6	5	4	3	2	1	0

Figure 7-25. IC_STAT_1 Register (continued)

SPI_OK	POR	FAULT	WARN	DS_GS	UV	OV	OT
R-1b	R-1b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-11. IC_STAT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPI_OK	R	1b	No SPI fault is detected. 0b = One or multiple of SPI_CLK_FLT or SPI_ADR_FLT in the past frames. 1b = No SPI fault is detected
6	POR	R	1b	Indicated power-on-reset condition. 0b = No power-on-reset condition is detected. 1b = Power-on reset condition is detected.
5	FAULT	R	0b	Fault indicator. Mirrors nFAULT pin.
4	WARN	R	0b	Warning indicator.
3	DS_GS	R	0b	Logic OR of VDS and VGS indicators.
2	UV	R	0b	Undervoltage indicator.
1	OV	R	0b	Overvoltage indicator.
0	OT	R	0b	Logic OR of OTW and OTSD indicators.

7.6.1.2 VGS_VDS_STAT Register (Address = 1h) [reset = 0h]

VGS_VDS_STAT is shown in Figure 7-26 and described in Table 7-12.

Return to Summary Table.

Status register with the VGS and VDS fault bits

Figure 7-26. VGS_VDS_STAT Register

7	6	5	4	3	2	1	0
VGS_H1	VGS_L1	RESERVED	RESERVED	VDS_H1	VDS_L1	RESERVED	RESERVED
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-12. VGS_VDS_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VGS_H1	R	0b	Indicates VGS gate fault on the high-side 1 MOSFET.
6	VGS_L1	R	0b	Indicates VGS gate fault on the low-side 1 MOSFET.
5	RESERVED	R	0b	Reserved
4	RESERVED	R	0b	Reserved
3	VDS_H1	R	0b	Indicates VDS overcurrent fault on the high-side 1 MOSFET.
2	VDS_L1	R	0b	Indicates VDS overcurrent fault on the low-side 1 MOSFET.
1	RESERVED	R	0b	Reserved
0	RESERVED	R	0b	Reserved

7.6.1.3 IC_STAT_2 Register (Address = 2h) [reset = 10h]

IC_STAT_2 is shown in Figure 7-27 and described in Table 7-13.

Return to Summary Table.

Status register with IC undervoltage, overvoltage, and SPI fault bits

Figure 7-27. IC_STAT_2 Register

7	6	5	4	3	2	1	0
PVDD_UV	PVDD_OV	VCP_UV	OTW	OTSD	RESERVED	SCLK_FLT	ADDR_FLT
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-13. IC_STAT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PVDD_UV	R	0b	indicates undervoltage fault on PVDD pin.
6	PVDD_OV	R	0b	Indicates overvoltage fault on PVDD pin.
5	VCP_UV	R	0b	Indicates undervoltage fault on VCP pin.
4	OTW	R	0b	Indicates overtemperature warning.
3	OTSD	R	0b	Indicates overtemperature shutdown.
2	RESERVED	R	0b	Reserved.
1	SCLK_FLT	R	0b	Indicates SPI clock (frame) fault.
0	ADDR_FLT	R	0b	Indicates SPI address fault.

7.6.1.4 RSVD_STAT Register (Address = 3h) [reset = 0h]

RSVD_STAT is shown in Figure 7-28 and described in Table 7-14.

Return to Summary Table.

Reserved status register

Figure 7-28. RSVD_STAT Register

7	6	5	4	3	2	1	0
RESERVED							
R-0b							

Table 7-14. RSVD_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0b	Reserved

7.6.2 CONTROL Registers

Table 7-15 lists the memory-mapped registers for the CONTROL registers. All register offset addresses not listed in Table 7-15 should be considered as reserved locations and the register contents should not be modified.

Table 7-15. CONTROL Registers

Address	Acronym	Register Name	Section
4h	IC_CTRL	IC control register	Go
5h	BRG_CTRL	BRG control register	Go
6h	DRV_CTRL_1	DRV control register 1	Go
7h	DRV_CTRL_2	DRV control register 2	Go
8h	DRV_CTRL_3	DRV control register 3	Go
9h	VDS_CTRL_1	VDS control register 1	Go
Ah	VDS_CTRL_2	VDS control register 2	Go
Bh	OLSC_CTRL	OLSC control register	Go
Ch	UVOV_CTRL	UVOV control register	Go
Dh	CSA_CTRL	CSA control register	Go

Complex bit access types are encoded to fit into small table cells. Table 7-16 shows the codes that are used for access types in this section.

Table 7-16. CONTROL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.2.1 IC_CTRL Register (Address = 4h) [reset = 6h]

IC_CTRL is shown in Figure 7-29 and described in Table 7-17.

Return to Summary Table.

Control register for IC configurations

Figure 7-29. IC_CTRL Register

7	6	5	4	3	2	1	0
EN_DRV	SSC_DIS	IN1/EN_MODE	RESERVED	LOCK			CLR_FLT
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-011b			R/W-0b

Table 7-17. IC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_DRV	R/W	0b	Enable gate driver bit 0b = Driver inputs are ignored and the gate driver passive pulldowns are enabled. 1b = Gate driver outputs are enabled and controlled by the digital inputs.
6	SSC_DIS	R/W	0b	Disable device spread spectrum clocking 0b = Enabled. 1b = Disabled.
5	IN1/EN_MODE	R/W	0b	IN1/EN control mode. 0b = IN1/EN signal is sourced from the IN1/EN pin. 1b = IN1/EN signal is sourced from the S_IN1/EN bit.
4	RESERVED	R/W	0b	Reserved
3-1	LOCK	R/W	011b	Lock and unlock the control registers. Bit settings not listed have no effect. 011b = Unlock all control registers. 110b = Lock the control registers by ignoring further writes except to these bits and CLR_FLT bit.
0	CLR_FLT	R/W	0b	Clear latched fault status information. 0b = Default state. 1b = Clear faults, resets to 0b after completion.

7.6.2.2 BRG_CTRL Register (Address = 5h) [reset = 0h]

BRG_CTRL is shown in Figure 7-30 and described in Table 7-18.

Return to Summary Table.

Control register for bridge configurations and output control

Figure 7-30. BRG_CTRL Register

7	6	5	4	3	2	1	0
VGS_HS_DIS	RESERVED		RESERVED	S_IN1/EN	RESERVED	S_HIZ1	RESERVED
R/W-0b	R/W-00b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 7-18. BRG_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VGS_HS_DIS	R/W	0b	V_{GS} monitor based dead-time handshake. 0b = Enabled. 1b = Disabled. Gate drive transition based on t_{DRIVE} and t_{DEAD} time duration.
6-5	RESERVED	R/W	00b	Reserved
4	RESERVED	R/W	0b	Reserved
3	S_IN1/EN	R/W	0b	Control bit for IN1/EN input signal. Enabled through IN1/EN_MODE bit.
2	RESERVED	R/W	0b	Reserved
1	S_HIZ1	R/W	0b	Control bit for HIZ1 input signal. Logic OR with the nHIZ1 pin. Active only in half-bridge input control mode. 0b = Outputs follow IN1/EN signal. 1b = Gate drivers pulldowns are enabled. Half-bridge 1 Hi-Z
0	RESERVED	R/W	0b	Reserved

7.6.2.3 DRV_CTRL_1 Register (Address = 6h) [reset = FFh]

DRV_CTRL_1 is shown in Figure 7-31 and described in Table 7-19.

Return to Summary Table.

Control register for DRV gate current configuration

Figure 7-31. DRV_CTRL_1 Register

7	6	5	4	3	2	1	0
IDRVP_HS				IDRVN_HS			
R/W-1111b				R/W-1111b			

Table 7-19. DRV_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	IDRVP_HS	R/W	1111b	High-side peak source pull up current. 0000b = 0.5 mA 0001b = 1 mA 0010b = 2 mA 0011b = 3 mA 0100b = 4 mA 0101b = 6 mA 0110b = 8 mA 0111b = 12 mA 1000b = 16 mA 1001b = 20 mA 1010b = 24 mA 1011b = 28 mA 1100b = 31 mA 1101b = 40 mA 1110b = 48 mA 1111b = 62 mA
3-0	IDRVN_HS	R/W	1111b	High-side peak sink pull down current. 0000b = 0.5 mA 0001b = 1 mA 0010b = 2 mA 0011b = 3 mA 0100b = 4 mA 0101b = 6 mA 0110b = 8 mA 0111b = 12 mA 1000b = 16 mA 1001b = 20 mA 1010b = 24 mA 1011b = 28 mA 1100b = 31 mA 1101b = 40 mA 1110b = 48 mA 1111b = 62 mA

7.6.2.4 DRV_CTRL_2 Register (Address = 7h) [reset = FFh]

DRV_CTRL_2 is shown in Figure 7-32 and described in Table 7-20.

Return to Summary Table.

Control register for DRV gate current configuration

Figure 7-32. DRV_CTRL_2 Register

7	6	5	4	3	2	1	0
IDRVP_LS				IDRVN_LS			
R/W-1111b				R/W-1111b			

Table 7-20. DRV_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	IDRVP_LS	R/W	1111b	Low-side peak source pull up current. 0000b = 0.5 mA 0001b = 1 mA 0010b = 2 mA 0011b = 3 mA 0100b = 4 mA 0101b = 6 mA 0110b = 8 mA 0111b = 12 mA 1000b = 16 mA 1001b = 20 mA 1010b = 24 mA 1011b = 28 mA 1100b = 31 mA 1101b = 40 mA 1110b = 48 mA 1111b = 62 mA
3-0	IDRVN_LS	R/W	1111b	Low-side peak sink pull down current. 0000b = 0.5 mA 0001b = 1 mA 0010b = 2 mA 0011b = 3 mA 0100b = 4 mA 0101b = 6 mA 0110b = 8 mA 0111b = 12 mA 1000b = 16 mA 1001b = 20 mA 1010b = 24 mA 1011b = 28 mA 1100b = 31 mA 1101b = 40 mA 1110b = 48 mA 1111b = 62 mA

7.6.2.5 DRV_CTRL_3 Register (Address = 8h) [reset = 20h]

DRV_CTRL_3 is shown in Figure 7-33 and described in Table 7-21.

Return to Summary Table.

Control register for DRV dead-time, gate current drive time, and VDS blanking time

Figure 7-33. DRV_CTRL_3 Register

7	6	5	4	3	2	1	0
VGS_MODE		VGS_TDRV		VGS_TDEAD			VGS_IND
R/W-00b		R/W-10b		R/W-000b			R/W-0b

Table 7-21. DRV_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VGS_MODE	R/W	00b	VGS gate fault monitor mode. 00b = Latched fault. 01b = Cycle by cycle. 10b = Warning report only. 11b = Disabled.
5-4	VGS_TDRV	R/W	10b	VGS drive time and VDS monitor blanking time. 00b = 96 µs 01b = 2 µs 10b = 4 µs 11b = 8 µs
3-1	VGS_TDEAD	R/W	000b	Insertable digital dead-time. 000b = 0 ns 001b = 250 ns 010b = 500 ns 011b = 750 ns 100b = 1000 ns 101b = 2000 ns 110b = 4000 ns 111b = 8000 ns
0	VGS_IND	R/W	0b	VGS independent shutdown mode enable. Active for BRG_MODE = 00b, 11b. 0b = Disabled. 1b = Enabled. VGS gate fault will only shutdown the associated half-bridge.

7.6.2.6 VDS_CTRL_1 Register (Address = 9h) [reset = 20h]

VDS_CTRL_1 is shown in Figure 7-34 and described in Table 7-22.

Return to Summary Table.

Control register for VDS overcurrent comparators

Figure 7-34. VDS_CTRL_1 Register

7	6	5	4	3	2	1	0
VDS_MODE		VDS_DG		VDS_IDRVN		VGS_LVL	VDS_IND
R/W-00b		R/W-10b		R/W-00b		R/W-0b	R/W-0b

Table 7-22. VDS_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VDS_MODE	R/W	00b	VDS overcurrent monitor mode. 00b = Latched fault. 01b = Cycle by cycle. 10b = Warning report only. 11b = Disabled.
5-4	VDS_DG	R/W	10b	VDS overcurrent monitor deglitch time. 00b = 1 µs 01b = 2 µs 10b = 4 µs 11b = 8 µs

Table 7-22. VDS_CTRL_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	VDS_IDRVN	R/W	00b	I_{DRVN} gate pulldown current after V_{DS_OCP} fault. 00b = Programmed I_{DRVN} 01b = 8 mA 10b = 31 mA 11b = 62 mA
1	VGS_LVL	R/W	0b	VGS monitor threshold for dead-time handshake and gate fault detection. 0b = 1.4 V. 1b = 1.0 V
0	VDS_IND	R/W	0b	VDS independent shutdown mode enable. Active for BRG_MODE = 00b, 11b. 0b = Disabled. 1b = Enabled. VDS overcurrent fault will only shutdown the associated half-bridge.

7.6.2.7 VDS_CTRL_2 Register (Address = Ah) [reset = DDh]

VDS_CTRL_2 is shown in Figure 7-35 and described in Table 7-23.

Return to Summary Table.

Control register for VDS threshold voltage

Figure 7-35. VDS_CTRL_2 Register

7	6	5	4	3	2	1	0
VDS_HS_LVL				VDS_LS_LVL			
R/W-1101b				R/W-1101b			

Table 7-23. VDS_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	VDS_HS_LVL	R/W	1101b	High-side VDS overcurrent monitor threshold. 0000b = 0.06 V 00001b = 0.08 V 0010b = 0.10 V 0011b = 0.12 V 0100b = 0.14 V 0101b = 0.16 V 0110b = 0.18 V 0111b = 0.2 V 1000b = 0.3 V 1001b = 0.4 V 1010b = 0.5 V 1011b = 0.6 V 1100b = 0.7 V 1101b = 1 V 1110b = 1.4 V 1111b = 2 V

Table 7-23. VDS_CTRL_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	VDS_LS_LVL	R/W	1101b	Low-side VDS overcurrent monitor threshold. 0000b = 0.06 V 0001b = 0.08 V 0010b = 0.10 V 0011b = 0.12 V 0100b = 0.14 V 0101b = 0.16 V 0110b = 0.18 V 0111b = 0.2 V 1000b = 0.3 V 1001b = 0.4 V 1010b = 0.5 V 1011b = 0.6 V 1100b = 0.7 V 1101b = 1 V 1110b = 1.4 V 1111b = 2 V

7.6.2.8 OLSC_CTRL Register (Address = Bh) [reset = 0h]

OLSC_CTRL is shown in Figure 7-36 and described in Table 7-24.

Return to Summary Table.

Control register of offline diagnostics.

Figure 7-36. OLSC_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			OLSC_EN	PU_SH1	PD_SH1	RESERVED	RESERVED
R/W-000b			R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 7-24. OLSC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000b	Reserved
4	OLSC_EN	R/W	0b	Offline open load and short circuit diagnostic enable. 0b = Disabled. 1b = VDS monitors set into real-time voltage monitor mode and diagnostics current sources enabled.
3	PU_SH1	R/W	0b	Half-bridge 1 pull up diagnostic current source. Must set OLSC_EN bit to use. 0b = Disabled. 1b = Enabled.
2	PD_SH1	R/W	0b	Half-bridge 1 pull down diagnostic current source. Must set OLSC_EN bit to use. 0b = Disabled. 1b = Enabled.
1	RESERVED	R/W	0b	Reserved
0	RESERVED	R/W	0b	Reserved

7.6.2.9 UVOV_CTRL Register (Address = Ch) [reset = 14h]

UVOV_CTRL is shown in Figure 7-37 and described in Table 7-25.

Return to Summary Table.

Control register for undervoltage and overvoltage monitors

Figure 7-37. UVOV_CTRL Register

7	6	5	4	3	2	1	0
PVDD_UV_MODE	PVDD_OV_MODE		PVDD_OV_DG		PVDD_OV_LVL	VCP_UV_MODE	VCP_UV_LVL
R/W-0b	R/W-00b		R/W-10b		R/W-1b	R/W-0b	R/W-0b

Table 7-25. UVOV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PVDD_UV_MODE	R/W	0b	PVDD supply undervoltage monitor mode. 0b = Latched fault. 1b = Automatic recovery.
6-5	PVDD_OV_MODE	R/W	00b	PVDD supply overvoltage monitor mode. 00b = Latched fault. 01b = Automatic recovery. 10b = Warning report only. 11b = Disabled.
4-3	PVDD_OV_DG	R/W	10b	PVDD supply overvoltage monitor deglitch time. 00b = 1 µs 01b = 2 µs 10b = 4 µs 11b = 8 µs
2	PVDD_OV_LVL	R/W	1b	PVDD supply overvoltage monitor threshold. 0b = 21.5 V 1b = 28.5 V
1	VCP_UV_MODE	R/W	0b	VCP charge pump undervoltage monitor mode. 0b = Latched fault. 1b = Automatic recovery.
0	VCP_UV_LVL	R/W	0b	VCP charge pump undervoltage monitor threshold. 0b = 2.5 V 1b = 5 V

7.6.2.10 CSA_CTRL Register (Address = Dh) [reset = 1h]

CSA_CTRL is shown in Figure 7-38 and described in Table 7-26.

Return to Summary Table.

Control register for current shunt amplifier

Figure 7-38. CSA_CTRL Register

7	6	5	4	3	2	1	0
CSA_SH_EN	CSA_BLK_SEL	CSA_BLK			CSA_DIV	CSA_GAIN	
R/W-0b	R/W-0b	R/W-000b			R/W-0b	R/W-01b	

Table 7-26. CSA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CSA_SH_EN	R/W	0b	Current shunt amplifier sample and hold. 0b = Disabled 1b = Enabled

Table 7-26. CSA_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CSA_BLK_SEL	R/W	0b	Current shunt amplifier blanking trigger source. 0b = Half-bridge 1 1b = Half-bridge 2
5-3	CSA_BLK	R/W	000b	Current shunt amplifier blanking time. % of t_{DRV}. 000b = 0 %, Disabled 001b = 25 % 010b = 37.5 % 011b = 50 % 100b = 62.5 % 101b = 75 % 110b = 87.5 % 111b = 100 %
2	CSA_DIV	R/W	0b	Current shunt amplifier reference voltage divider. 0b = AREF / 2 1b = AREF / 8
1-0	CSA_GAIN	R/W	01b	Current shunt amplifier gain setting. 00b = 10 V/V 01b = 20 V/V 10b = 40 V/V 11b = 80 V/V

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8106-Q1 is a highly configurable half-bridge MOSFET gate driver than cane be used to drive a variety of different output loads. The design examples below highlight how to use and configure the device for different application use cases.

8.2 Typical Application

The typical application for the DRV8106-Q1 is to control an external MOSFET half-bridge for uni-directional brushed DC motor control. A high-level schematic example is shown below in Figure 8-1.

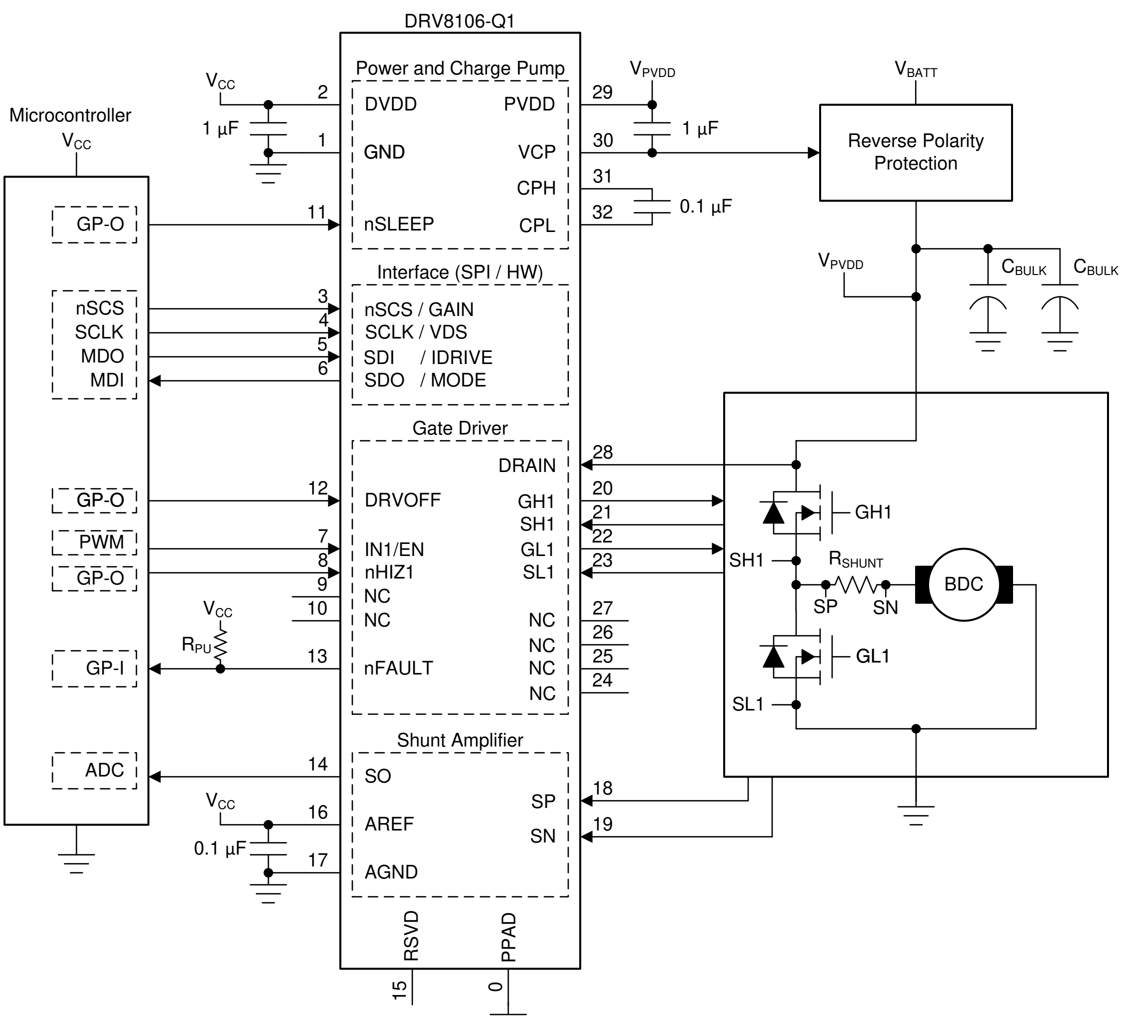


Figure 8-1. DRV8106-Q1 Typical Application

8.2.1 Design Requirements

Table 8-1 lists a set if example input parameters for the system design.

Table 8-1. Example Design Parameters

Design Parameter	Reference	Value
PVDD Nominal Supply Voltage	V_{PVDD}	12 V
PVDD Supply Voltage Range		9 to 18 V
DVDD / AREF Logic Supply Voltage	V_{CC}	3.3V
MOSFET Total Gate Charge	Q_G	30 nC (typical) at V_{GS} = 10 V
MOSFET Gate to Drain Charge	Q_{GD}	5 nC (typical)
MOSFET On Resistance	$R_{DS(on)}$	4 mΩ
Target Output Rise Time	t_{rise}	750 - 1000 ns
Target Output Fall Time	t_{fall}	250 - 500 ns
PWM Frequency	f_{PWM}	20 kHz
Maximum Motor Current	I_{MAX}	25 A
Shunt Resistor Power Capability	P_{SHUNT}	3 W

8.2.2 Detailed Design Procedure

The following sections will go through some of the common design procedures for the gate driver, shunt amplifier, and determining the device power dissipation.

8.2.2.1 Gate Driver Configuration

8.2.2.1.1 VCP Load Calculation Example

It should be ensured that the DRV8106-Q1 charge pump load capability is sufficient for the MOSFET and desired PWM frequency. This can be confirmed with a simple calculation as shown in Equation 1. In typical half-bridge drive configurations, only one high-side MOSFET will be switching at a time.

$$I_{VCP} \text{ (A)} = Q_G \text{ (C)} \times f_{PWM} \text{ (Hz)} \times \text{\# of switching HS FETs} \quad (1)$$

Using the input design parameters as an example, we can show that in this scenario that output load capability of the charge pump is sufficient in Equation 2.

$$I_{VCP} = 30 \text{ nC} \times 20 \text{ kHz} \times 1 = 0.6 \text{ mA} \quad (2)$$

8.2.2.1.2 I_{DRIVE} Calculation Example

The gate drive current strength, I_{DRIVE}, is selected based on the gate-to-drain charge of the external MOSFETs and the target rise and fall times at the switch-node. If I_{DRIVE} is selected to be too low for a given MOSFET, then the MOSFET may not turn on or off completely within the configured t_{DRIVE} time and a gate fault may be asserted. Additionally, slow rise and fall times will lead to higher switching power losses in the external power MOSFETs. It is recommended to verify these values in system with the required external MOSFETs and load to determine the optimal settings.

The I_{DRIVEP} and I_{DRIVEN} for both the high-side and low-side external MOSFETs are independently adjustable on SPI device variants. On hardware interface device variants, both source and sink settings are selected simultaneously on the IDRIVE pin.

For MOSFETs with a known gate-to-drain charge (Q_{GD}), desired rise time (t_{rise}), and a desired fall time (t_{fall}), use Equation 3 and Equation 4 to calculate the approximate values of I_{DRIVEP} and I_{DRIVEN} (respectively).

$$I_{DRIVEP} = Q_{GD} / t_{rise} \quad (3)$$

$$I_{DRIVEN} = Q_{GD} / t_{fall} \quad (4)$$

Using the input design parameters as an example, we can calculate the approximate values for I_{DRIVEP} and I_{DRIVEN}.

$$I_{DRIVEP\_HI} = 5\text{ nC} / 750\text{ ns} = 6.67\text{ mA} \quad (5)$$

$$I_{DRIVEP\_LO} = 5\text{ nC} / 1000\text{ ns} = 5\text{ mA} \quad (6)$$

Based on these calculations a value of 6 mA was chosen for I_{DRIVEP}.

$$I_{DRIVEN\_HI} = 5\text{ nC} / 250\text{ ns} = 20\text{ mA} \quad (7)$$

$$I_{DRIVEN\_LO} = 5\text{ nC} / 500\text{ ns} = 10\text{ mA} \quad (8)$$

Based on these calculations a value of 16 mA was chosen for I_{DRIVEN}.

8.2.2.2 Current Shunt Amplifier Configuration

The DRV8106-Q1 differential shunt amplifier gain and shunt resistor value are selected based on the dynamic current range, reference voltage supply, shunt resistor power rating, and operating temperature range. In bidirectional operation of the shunt amplifier, the dynamic range at the output is approximately calculated as shown in Equation 9. The output of the amplifier can swing from the midpoint reference (V_{AREF} / 2) to either 0.25 V or V_{AREF} - 0.25V depending on the polarity of the input voltage to the amplifer.

$$V_{SO\_BI} = (V_{AREF} - 0.25\text{ V}) - (V_{AREF} / 2) \quad (9)$$

If only unidirectional current sensing is required, the amplifier reference can be modified to expand the dynamic range at the output. The is modified through the CSA_DIV SPI register setting. In this mode, the dynamic range at the output is approximately calculated as shown in Equation 10.

$$V_{SO\_UNI} = (V_{AREF} - 0.25\text{ V}) - (V_{AREF} / 8) \quad (10)$$

Based on V_{AREF} = 3.3 V, the dynamic out range in both bidirectional or unidirectional sensing can be calculated as shown below.

$$V_{SO\_BI} = (3.3\text{ V} - 0.25\text{ V}) - (3.3\text{ V} / 2) = 1.4\text{ V} \quad (11)$$

$$V_{SO\_UNI} = (3.3\text{ V} - 0.25\text{ V}) - (3.3\text{ V} / 8) = 2.6375\text{ V} \quad (12)$$

The external shunt resistor value andDRV8106-Q1 shunt amplifier gain setting are selected based on the available dynamic output range, the shunt resistor power rating, and maximum motor current that needs to be measured. This exact values for the shunt resistance and amplifier gain are determine by both Equation 13 and Equation 14.

$$R_{SHUNT} < P_{SHUNT} / I_{MAX}{}^{2} \quad (13)$$

$$A_V < V_{SO} / (I_{MAX} \times R_{SHUNT}) \quad (14)$$

Based on V_{SO} = 1.4 V, I_{MAX} = 25 A and P_{SHUNT} = 3 W, the values for shunt resistance and amplifier gain can be calculated as shown below.

$$R_{SHUNT} < 3\text{ W} / 25^2\text{ A} = 4.8\text{ m}\Omega \quad (15)$$

$$A_V < 1.4\text{ V} / (25\text{ A} \times 4.8\text{ m}\Omega) = 11.67\text{ V/V} \quad (16)$$

Based on the results, a shunt resistance of 4 mΩ and an amplifier gain of 10 V/V can be selected.

8.2.2.3 Power Dissipation

In high ambient operating environments, it may be important to estimate the internal self heating of the driver. To determine the temperature of the device, first the internal power dissipation must be calculate. After this an estimate can be made with the device package thermal properties.

The internal power dissipation has four primary components.

- High-Side Driver Power Dissipation (P_{HS})
- Low-Side Driver Power Dissipation (P_{LS})
- PVDD Battery Supply Power Dissipation (P_{PVDD})
- DVDD/AREF Logic/Reference Supply Power Dissipation (P_{VCC})

The values for P_{HS} and P_{LS} can be approximated by referencing the earlier equation for charge pump load current as shown below. In a typical switch scenario, 1 high-side and 1 low-side MOSFET are switching.

$$I_{HS/LS}\ (A) = Q_G\ (C) \times f_{PWM}\ (Hz) \times \#\ \text{of switching FETs} \quad (17)$$

Using the input design parameters as an example, we can calculate the current load from the high-side and low-side drivers.

$$I_{HS} = 30\ nC \times 20\ kHz \times 1 = 0.6\ mA \quad (18)$$

$$I_{LS} = 30\ nC \times 20\ kHz \times 1 = 0.6\ mA \quad (19)$$

From this, the power dissipation can be calcuated from the equations below for the driver power dissipation. The high-side includes a doubling factor to account for the losses in the charge pump.

$$P_{HS}\ (W) = I_{HS}\ (A) \times V_{PVDD} \times 2 \quad (20)$$

$$P_{LS}\ (W) = I_{LS}\ (A) \times V_{PVDD} \quad (21)$$

Using the input design parameters as an example, we can calculate the power dissipation from the high-side and low-side drivers.

$$P_{HS}\ (W) = 0.0144\ W = 0.6\ mA \times 12\ V \times 2 \quad (22)$$

$$P_{LS}\ (W) = 0.0072\ W = 0.6\ mA \times 12\ V \quad (23)$$

The values for P_{PVDD} and P_{VCC} can be approximated by referencing the below equations.

$$P_{PVDD}\ (W) = I_{PVDD}\ (A) \times V_{PVDD} \quad (24)$$

$$P_{VCC}\ (W) = (I_{DVDD}\ (A) \times V_{DVDD}) + (I_{AREF}\ (A) \times V_{AREF}) \quad (25)$$

Using the input design parameters as an example, we can calculate the power dissipation for the power supplies.

$$P_{PVDD}\ (W) = 0.0024\ W = 2\ mA \times 12\ V \quad (26)$$

$$P_{VCC}\ (W) = 0.0015\ W = (3.5\ mA \times 3.3\ V) + (1\ mA \times 3.3\ V) \quad (27)$$

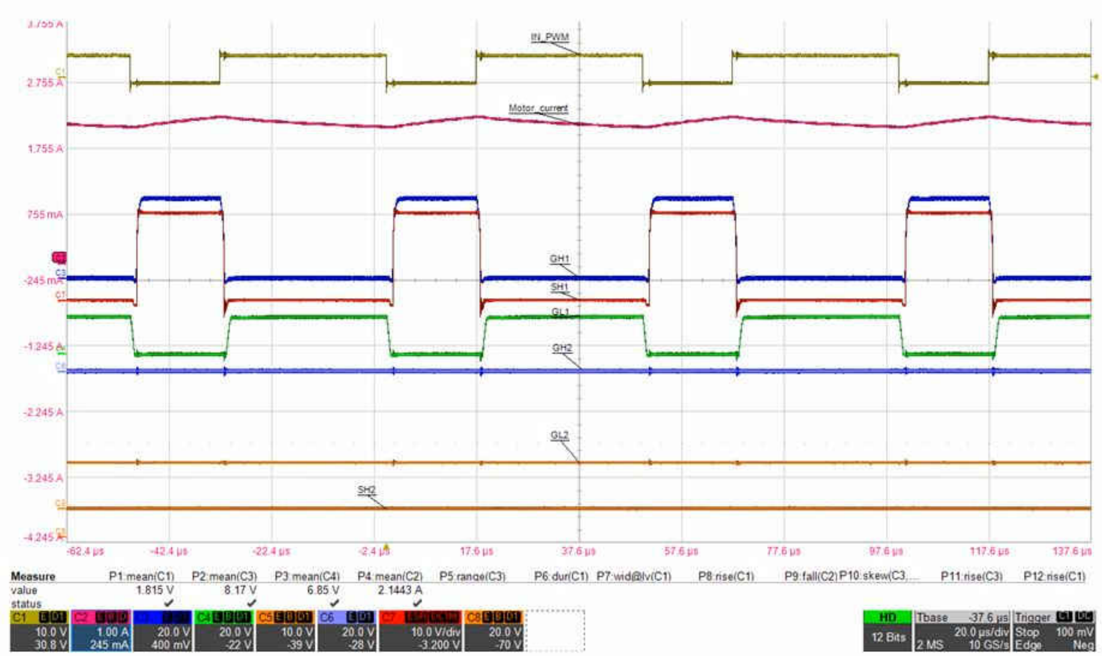
Finally to estimate device junction temeprature, can reference below equation.

$$T_{JUNCTION}\ (°C) = T_{AMBIENT}\ (°C) + (R_{θJA}\ (°C/W) \times P_{TOT}(W)) \quad (28)$$

Using the previously calculated power dissipation values and the device thermal parameter from the Thermal Information table can estimate the device internal temperature.

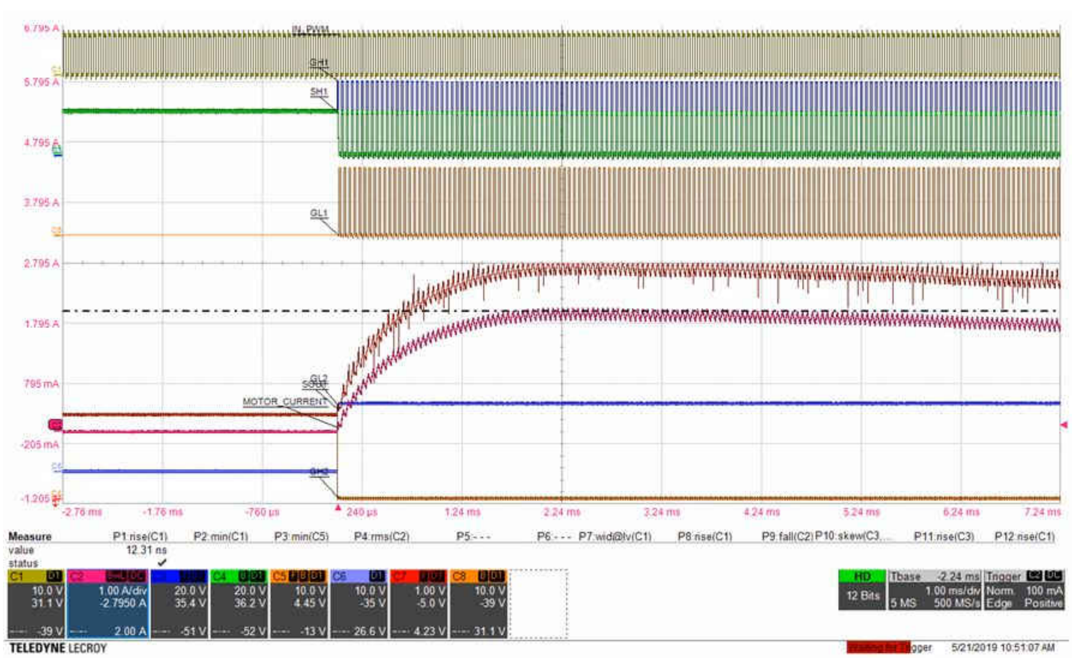
$$T_{JUNCTION}\ (°C) = 105.9\ °C = 105\ °C + (34.9\ °C/W \times 0.0255\ W) \quad (29)$$

8.2.3 Application Curves



The image above shows the driver during nominal PWM operaion, including the logic PWM control input and all driver outputs.

Figure 8-2. Driver Nominal PWM Operation



The image above shows the driver and amplifier performance during motor startup including driver outputs and current amplifier feedback..

Figure 8-3. Driver Operation During Motor Startup

Figure 8-4. Driver PWM Operation During Warm Crank Pulse

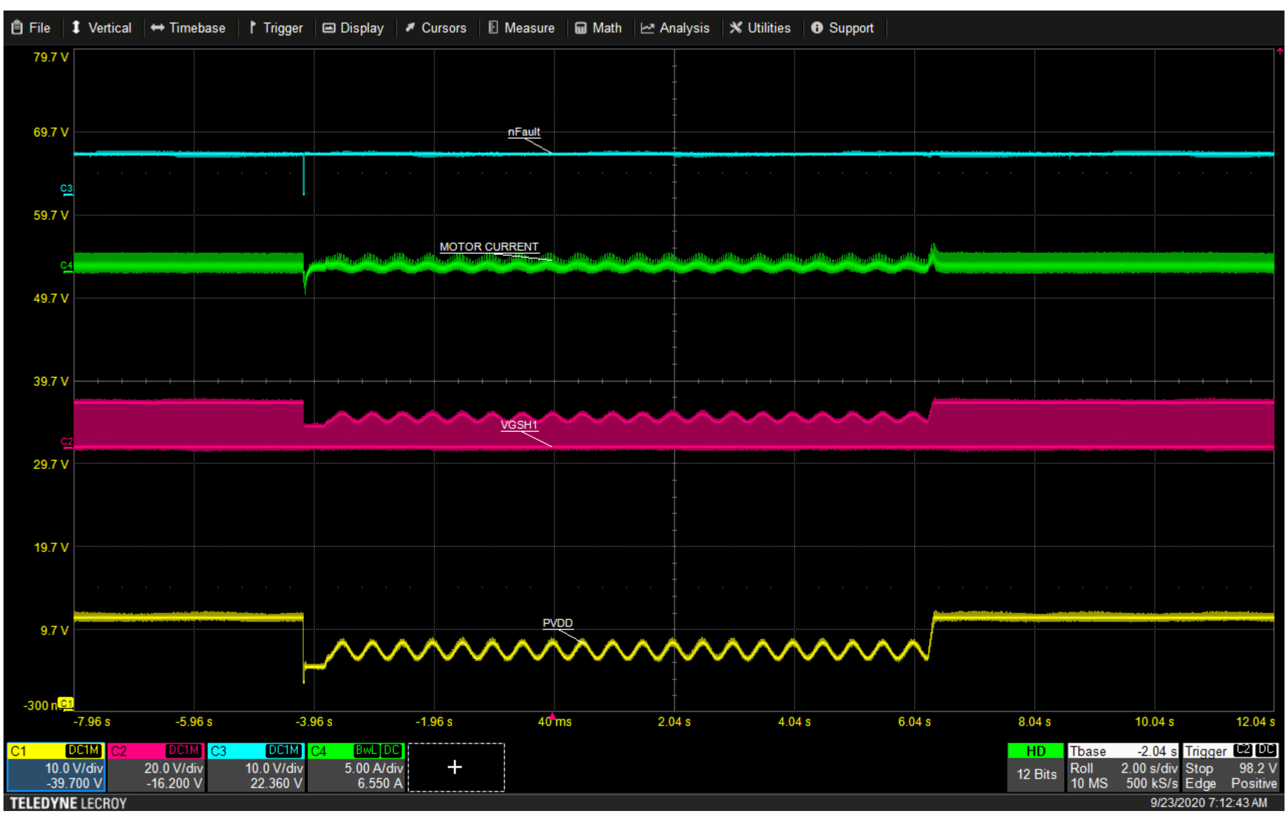


Figure 8-5. Driver PWM Operation During Cold Crank Pulse

9 Power Supply Recommendations

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. Having more bulk capacitance is generally beneficial, while the disadvantages are increased cost and physical size.

The amount of local bulk capacitance needed depends on a variety of factors, including:

- The highest current required by the motor or load
- The capacitance of the power supply and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple of the system
- The motor braking method (if applicable)

The inductance between the power supply and motor drive system limits how the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended minimum value, but system level testing is required to determine the appropriately sized bulk capacitor.

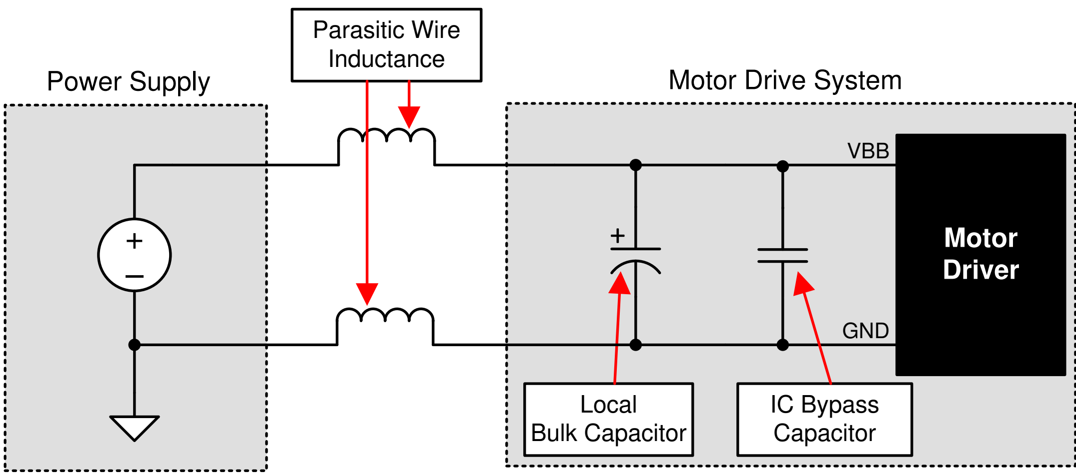


Figure 9-1. System Supply Parasitics Example

10 Layout

10.1 Layout Guidelines

Bypass the PVDD pin to the GND pin using a low-ESR ceramic bypass capacitor with a recommended value of 0.1 µF. Place this capacitor as close to the PVDD pin as possible with a thick trace or ground plane connected to the GND pin. Additionally, bypass the PVDD pin using a bulk capacitor rated for VM. This component can be electrolytic. This capacitance must be at least 10 µF. It is acceptable if this capacitance is shared with the bulk capacitance for the external power MOSFETs.

Additional bulk capacitance is required to bypass the high current path on the external MOSFETs. This bulk capacitance should be placed such that it minimizes the length of any high current paths through the external MOSFETs. The connecting metal traces should be as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Place a low-ESR ceramic capacitor between the CPL and CPH pins. This capacitor should be 0.1 µF, rated for PVDD, and be of type X5R or X7R. Additionally, place a low-ESR ceramic capacitor between the VCP and PVDD pins. This capacitor should be 1 µF, rated for 16 V, and be of type X5R or X7R.

Bypass the DVDD pin to the GND pin with a 1.0 µF low-ESR ceramic capacitor rated for 6.3 V and of type X5R or X7R. Place this capacitor as close to the pin as possible and minimize the path from the capacitor to the GND pin. If another bypass capacitor is within close proximity of the device for the external low voltage power supply and noise on the power supply is minimal, it is optional to remove this component.

Bypass the AREF pin to the GND pin with a 0.1 µF low-ESR ceramic capacitor rated for 6.3 V and of type X5R or X7R. Place this capacitor as close to the pin as possible and minimize the path from the capacitor to the GND pin. If another bypass capacitor is within close proximity of the device for the external low voltage power supply and noise on the power supply is minimal, it is optional to remove this component.

The DRAIN pin can be shorted directly to the PVDD pin. However, if a significant distance is between the device and the external MOSFETs, use a dedicated trace to connect to the common point of the drains of the high-side external MOSFETs. Do not connect the SLx pins directly to the GND plane. Instead, use dedicated traces to connect these pins to the sources of the low-side external MOSFETs. These recommendations allow for more accurate V_{DS} sensing of the external MOSFETs for overcurrent detection.

Minimize the loop length for the high-side and low-side gate drivers. The high-side loop is from the GHx pin of the device to the high-side power MOSFET gate, then follows the high-side MOSFET source back to the SHx pin. The low-side loop is from the GLx pin of the device to the low-side power MOSFET gate, then follows the low-side MOSFET source back to the SLx pin.

10.2 Layout Example

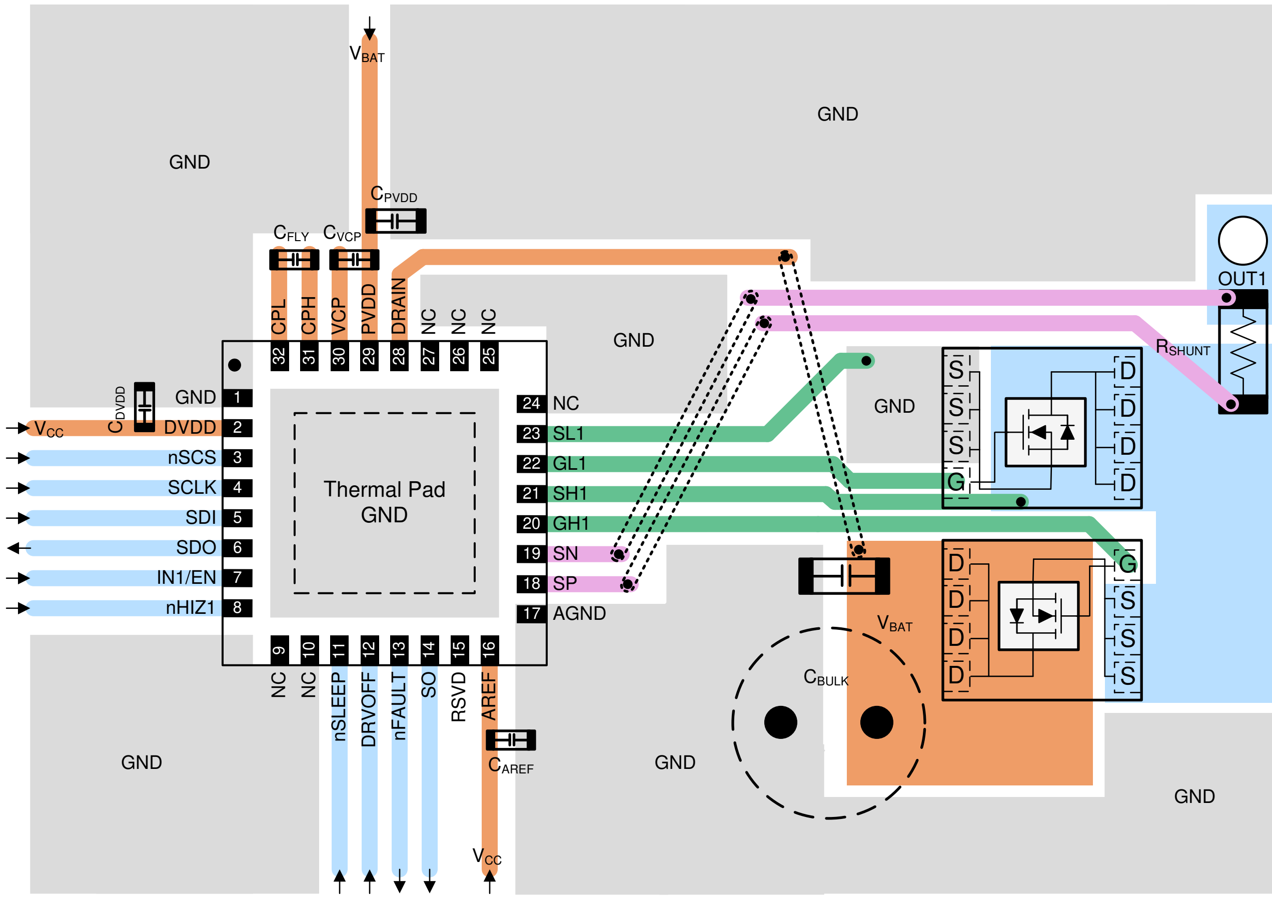


Figure 10-1. DRV8106-Q1 Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Understanding Smart Gate Drive* application report
- Texas Instruments, *Calculating Motor Driver Power Dissipation* application report
- Texas Instruments, *PowerPAD™ Made Easy* application report
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application report
- Texas Instruments, *Best Practices for Board Layout of Motor Drivers* application report

11.1.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8106HQRHBRQ1	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8106H
DRV8106HQRHBRQ1.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8106H
DRV8106SQRHBRQ1	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8106S
DRV8106SQRHBRQ1.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8106S

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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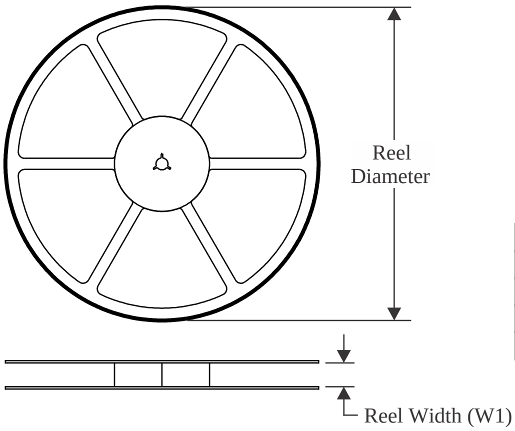
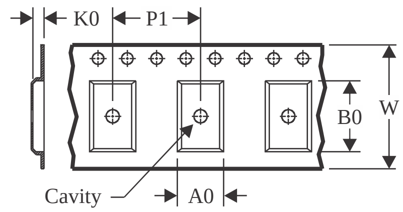
TAPE AND REEL INFORMATION

REEL DIMENSIONS

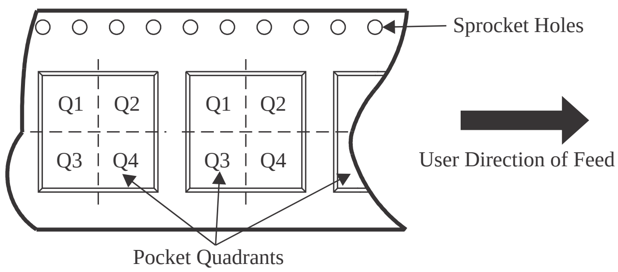


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

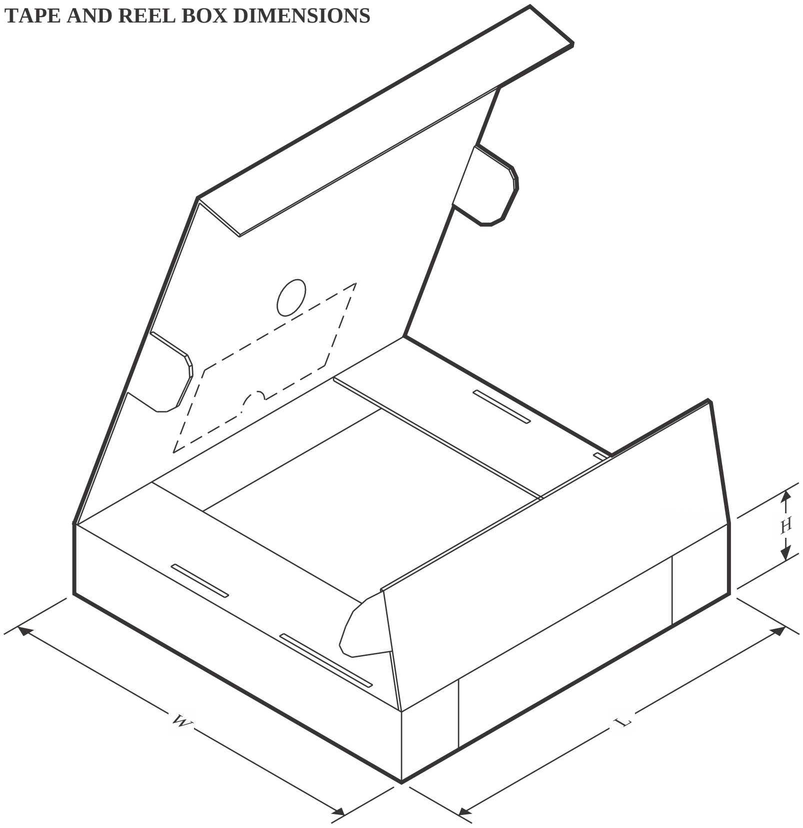
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

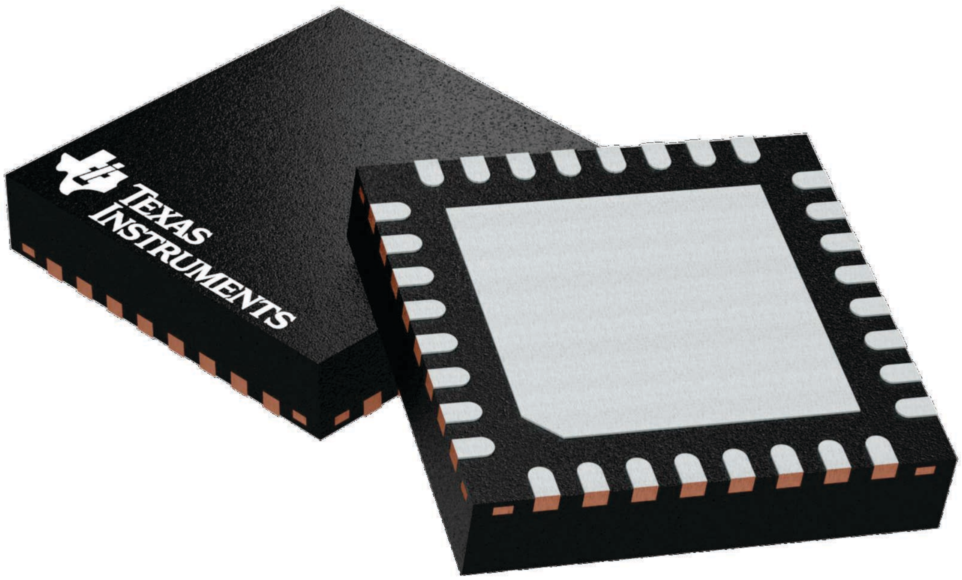
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8106HQRHBRQ1	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
DRV8106SQRHBRQ1	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

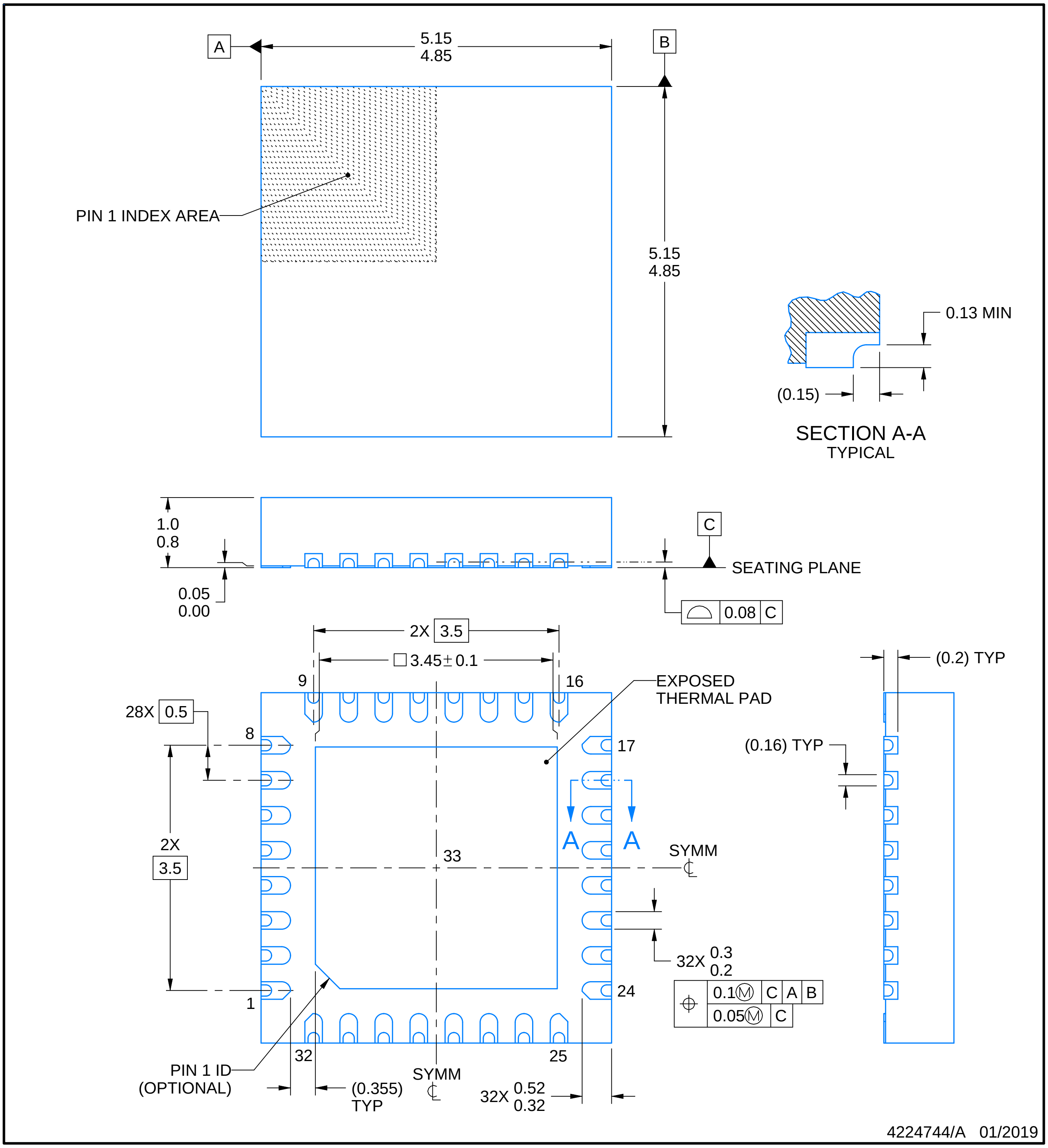


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8106HQRHBRQ1	VQFN	RHB	32	3000	367.0	367.0	35.0
DRV8106SQRHBRQ1	VQFN	RHB	32	3000	367.0	367.0	35.0

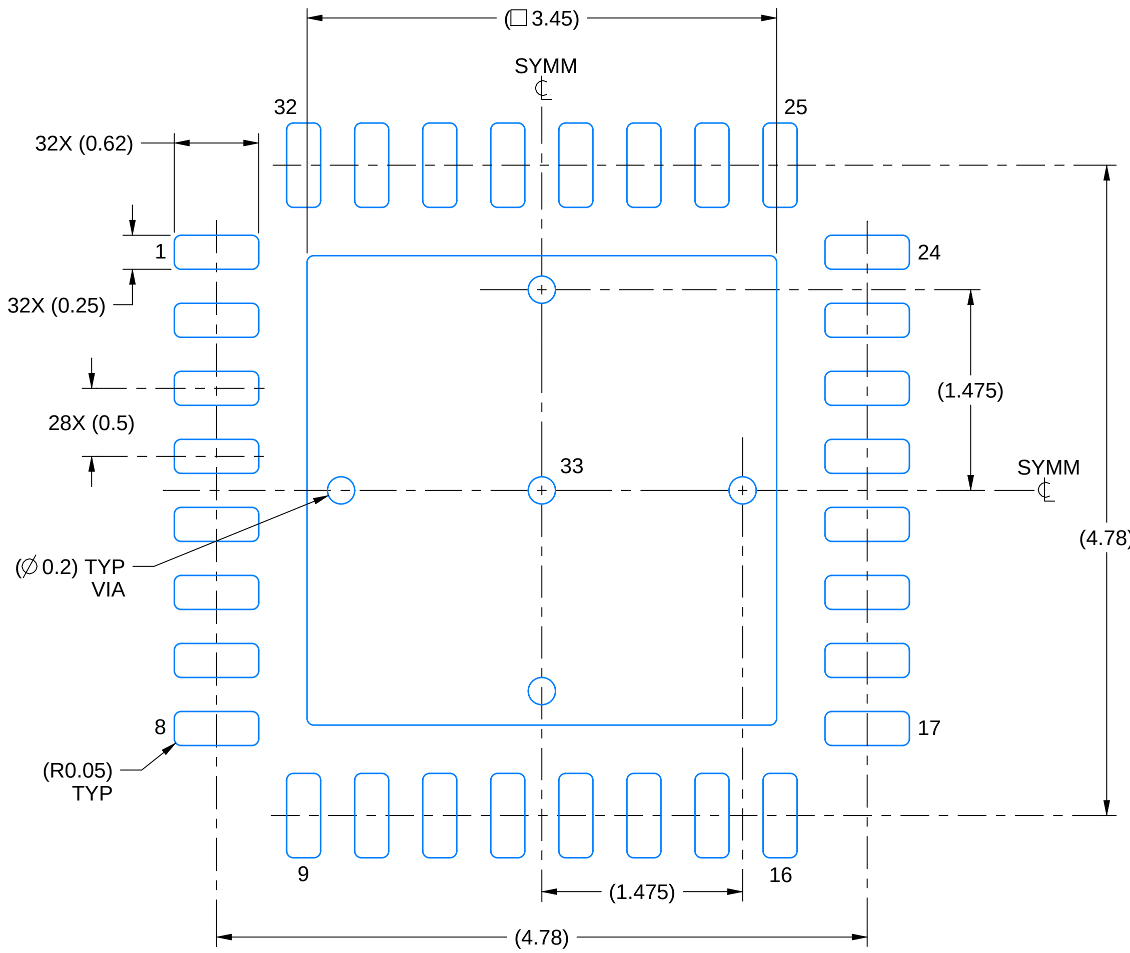


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

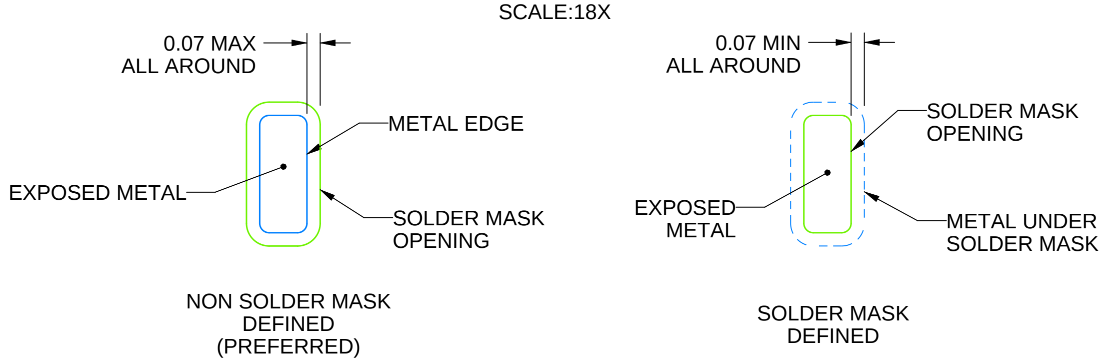


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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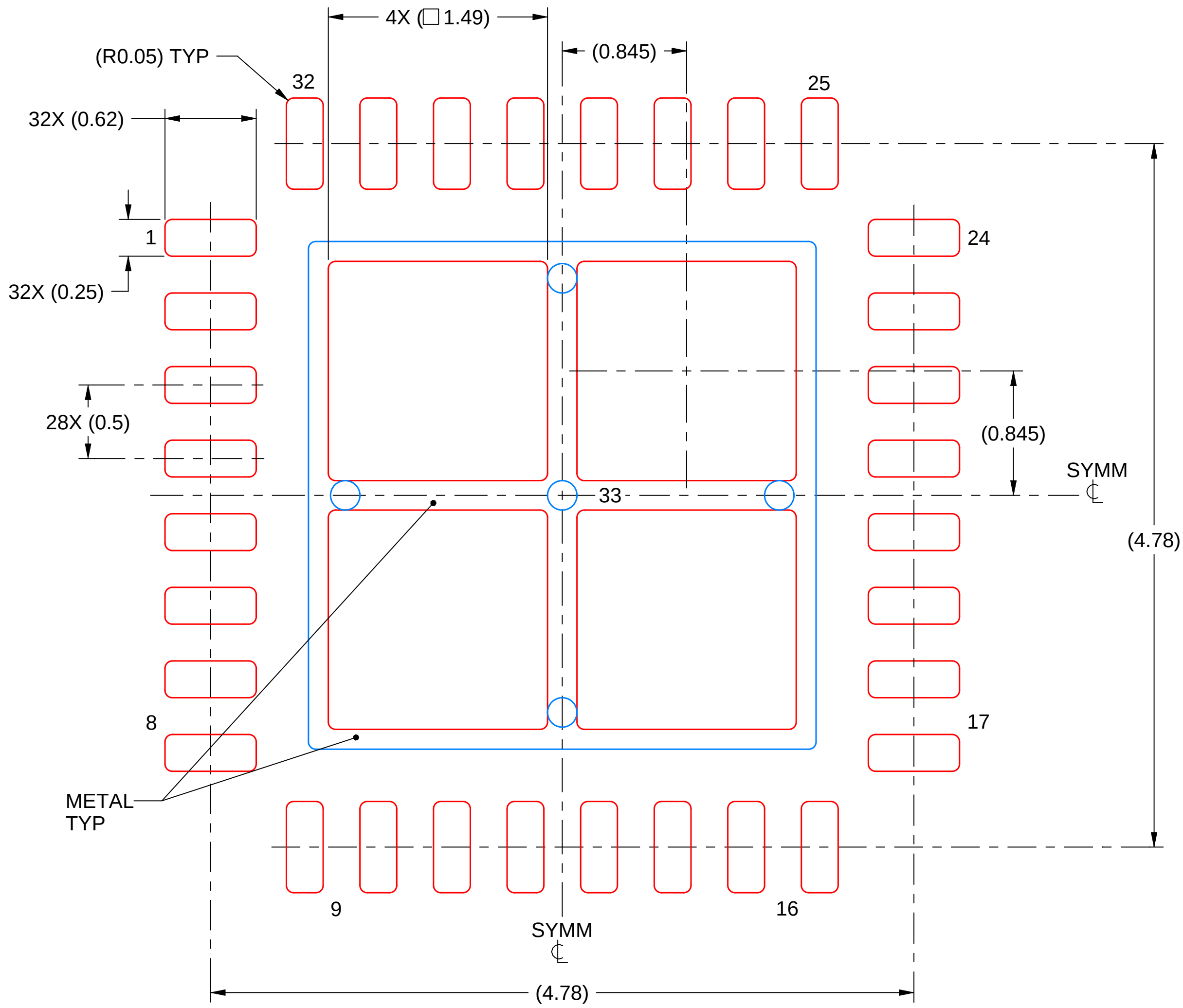
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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