

DRV8001-Q1 Automotive Highly-Integrated, Multifunction Driver for Door Control

1 Features

- AEC-Q100 qualified for automotive applications:
 - Temperature grade 1: -40°C to $+125^{\circ}\text{C}$, T_A
- 4.5V to 35V (40V absolute maximum) operating range
- 1 Integrated half-bridge with I_{OUT} maximum 8A ($R_{DS(on)} = 132\text{m}\Omega$, $66\text{m}\Omega$ per FET)
- 1 Integrated half-bridge with I_{OUT} maximum 7A ($R_{DS(on)} = 160\text{m}\Omega$, $80\text{m}\Omega$ per FET)
- 2 Integrated half-bridges with I_{OUT} maximum 4A ($R_{DS(on)} = 400\text{m}\Omega$, $200\text{m}\Omega$ per FET)
- 2 Integrated half-bridges with I_{OUT} maximum 1.3A load ($R_{DS(on)} = 1500\text{m}\Omega$, $750\text{m}\Omega$ per FET)
- 1 Configurable integrated high-side driver as lamp or LED driver with I_{OUT} maximum 1.5/0.5A ($R_{DS(on)} = 0.4/1.5\Omega$)
- 5 Integrated high-side drivers for 0.5/0.25A load ($R_{DS(on)} = 1.5\Omega$)
 - 1 High-side driver to supply electro chromic (EC) glass MOSFET
- 1 External MOSFET gate driver for charge of electro chromic glass
- 1 Integrated low-side FET for discharge of electro chromic glass
- Internal 10bit PWM generator for high-side drivers
- All high-side drivers support a low- or high- current threshold constant current mode to drive a wide range of LED modules
- 1 External MOSFET gate driver for heater
 - Offline open load detection
 - V_{DS} monitoring of low $R_{DS(on)}$ MOSFET for short-circuit detection
- Integrated driver output features current regulation (ITRIP)
- Muxable sense output (IPROPI)
 - Internal current sensing with proportional current output (IPROPI)
 - Advanced die temperature monitoring with multiple thermal clusters
 - Scaled supply voltage output
- Protection and diagnostic features with configurable fault behavior
 - Load diagnostics in both the off-state and on-state to detect open load and short-circuit
 - Overcurrent and over temperature protection
- [Device Comparison Table](#)

2 Applications

- [Door module](#)
- [Body control modules](#)

- [Zonal module](#)

3 Description

The DRV8001-Q1 device integrates multiple door control specific functions: driving and diagnosing motor (inductive), resistive and capacitive loads, driving a lamp or LEDs, drive MOSFETs for special loads such as heating element or electrochromic elements. These drivers include protection features for offline and active diagnostics such as under and over voltage monitors, offline open load and short-circuit diagnostics, and zone-based thermal monitoring and shutdown protection. The device features 6 integrated half-bridges (2 high-side alternate modes), 6 integrated high-side drivers, one external high-side gate driver for heater, one external high-side gate driver for electrochromic charge and one integrated low-side driver for electrochromic load discharge. Each individual driver has PWM input control configuration, sensing, diagnostics and device system protection. There is a dedicated internal programmable PWM generators for each high-side driver. Proportional current sense pin output is available for all integrated drivers

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE (NOM) ⁽²⁾
DRV8001-Q1	VQFN (40)	6.00mm × 6.00mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.

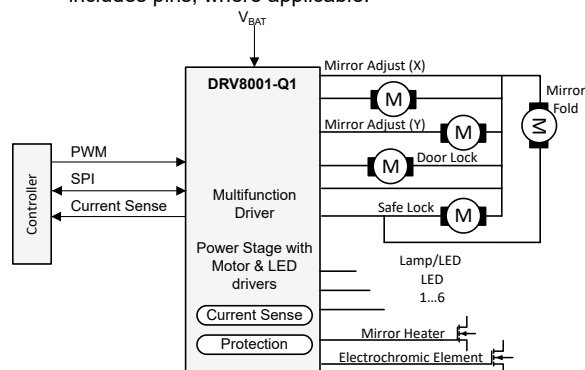


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4 Device Comparison

Table 4-1. Device Comparison

Device Name	H-Bridge Gate Driver	Half-bridge Driver	High-side Driver	Lamp/LED HS Driver	EC Gate Driver	Heater HS Gate Driver	Current Shunt Amp	Package
DRV8000-Q1	1x	6x	5x	1x	1x	1x	1x	7x7 QFN-48 Wettable Flank
DRV8001-Q1	X	6x	5x	1x	1x	1x	X	6x6 QFN-40 Wettable Flank
DRV8002-Q1	1x	6x	5x	1x	X	X	1x	7x7 QFN-48 Wettable Flank

Table 4-2. Device Orderable Information

Device	Pre-production Part Number	Orderable Part Number	EVM
DRV8000-Q1	PDRV8000QWRGZRQ1	DRV8000QRGZRQ1	DRV8000-Q1EVM
DRV8001-Q1	PDRV8001QWRHARQ1	DRV8001QRHARQ1	DRV8001-Q1EVM
DRV8002-Q1	PDRV8002QRGZRQ1	DRV8002QRGZRQ1	DRV8002-Q1EVM

ADVANCE INFORMATION

5 Pin Configuration and Functions

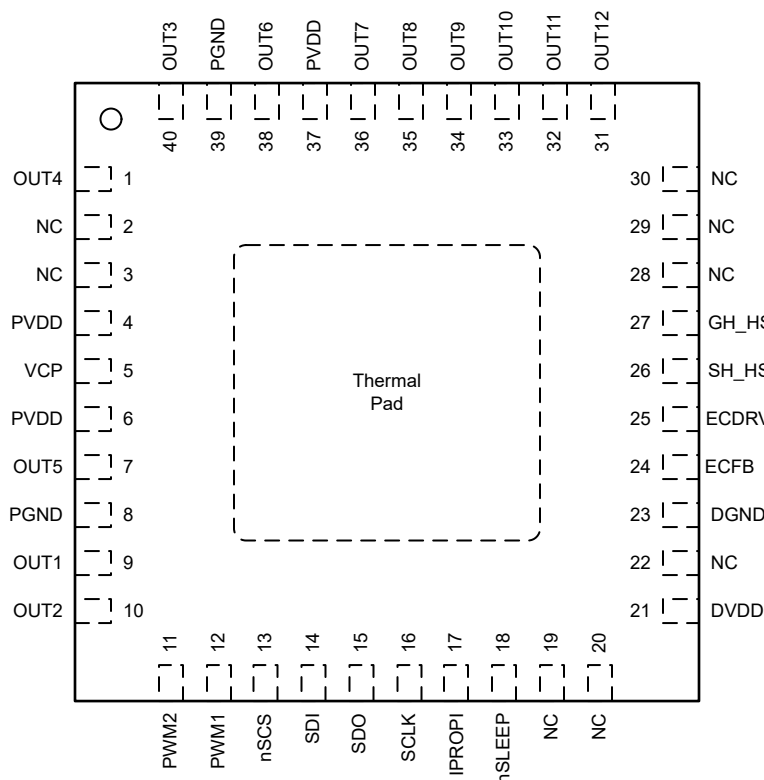


Figure 5-1. RHA Package, 40-Pin VQFN (Top View)

Table 5-1. Pin Functions

PIN		I/O ⁽¹⁾	TYPE	DESCRIPTION
NO.	NAME			
1	OUT4	O	Power	400mΩ half-bridge output 4.
2	NC	-	-	No connect.
3	NC	-	-	No connect.
4	PVDD	I	Power	Device driver power supply input. Connect to the bridge power supply. Connect a 0.1μF, PVDD-rated ceramic capacitor and local bulk capacitance greater than or equal to 10μF between PVDD and GND pins.
5	VCP	I/O	Power	Charge pump output. Connect a 1μF, 16V ceramic capacitor between VCP and PVDD pins.
6	PVDD	I	Power	Device driver power supply input. Connect to the bridge power supply. Connect a 0.1μF, PVDD-rated ceramic capacitor and local bulk capacitance greater than or equal to 10μF between PVDD and GND pins.
7	OUT5	O	Power	First pin of 130mΩ half-bridge output 5.
8	PGND	I/O	Ground	Device ground. Connect to system ground.
9	OUT1	O	Power	1.5Ω half-bridge output 1.
10	OUT2	O	Power	1.5Ω half-bridge output 2.
11	PWM2	I	Digital	PWM input 2 for regulation of all drivers except electrochrome.
12	PWM1	I	Digital	PWM input 1 for regulation of half-bridges.
13	nSCS	I	Digital	Serial chip select. A logic low on this pin enables serial interface communication. Internal pullup resistor.
14	SDI	I	Digital	Serial data input. Data is captured on the falling edge of the SCLK pin. Internal pulldown resistor.

Table 5-1. Pin Functions (continued)

PIN		I/O ⁽¹⁾	TYPE	DESCRIPTION
NO.	NAME			
15	SDO	O	Digital	Serial data output. Data is shifted out on the rising edge of the SCLK pin. Push-pull output.
16	SCLK	I	Digital	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin. Internal pulldown resistor.
17	IPROPI	I/O	Analog	Sense output is multiplexed from any of driver load current feedback, PVDD voltage feedback, or thermal cluster temperature feedback. Can also be configured as second PWM pin input for half-bridge drivers.
18	nSLEEP	I	Analog	Device enable pin. Logic low to shutdown the device and enter sleep mode. Internal pulldown resistor.
19	NC	-	-	No connect.
20	NC	-	-	No connect.
21	DVDD	I	Power	Device logic and digital output power supply input. Recommended to connect a 1.0µF, 6.3V ceramic capacitor between the DVDD and GND pins.
22	NC	-	-	No connect.
23	DGND	I/O	Ground	Device ground. Connect to system ground.
24	ECFB	I/O	Power	For EC control, pin is used as voltage monitor input and fast discharge low-side switch. If the EC drive function is not used, connect this pin to GND through 10kΩ resistor.
25	ECDRV	O	Analog	For EC control, pin controls the gate of external MOSFET for EC voltage regulation
26	SH_HS	I	Analog	Source pin of high-side heater MOSFET and output to heater load. Connect to source of high-side MOSFET.
27	GH_HS	O	Analog	Gate driver output for heater MOSFET. Connect to gate of high-side MOSFET.
28	NC	-	-	No connect.
29	NC	-	-	No connect.
30	NC	-	-	No connect.
31	OUT12	O	Power	1.5Ω high-side driver output 12. Connect to low-side load.
32	OUT11	O	Power	1.5Ω high-side driver output 11. Configurable as SC protection switch for EC drive. Connect to low-side load.
33	OUT10	O	Power	1.5Ω high-side driver output 10. Connect to low-side load.
34	OUT9	O	Power	1.5Ω high-side driver output 9. Connect to low-side load.
35	OUT8	O	Power	1.5Ω high-side driver output 8. Connect to low-side load.
36	OUT7	O	Power	High-side driver output with configurable R _{DS(on)} (400 mΩ/1500 mΩ). Connect to low-side load.
37	PVDD	I	Power	Device driver power supply input. Connect to the bridge power supply. Connect a 0.1µF, PVDD-rated ceramic capacitor and local bulk capacitance greater than or equal to 10µF between PVDD and GND pins.
38	OUT6	O	Power	160mΩ half-bridge output 6.
39	PGND	I/O	Ground	Device ground. Connect to system ground.
40	OUT3	O	Power	400mΩ half-bridge output 3.

(1) I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Power supply pin voltage	PVDD	−0.3	40	V
Power supply transient voltage ramp	PVDD		2	V/μs
Digital Logic power supply voltage ramp	DVDD		2	V/μs
Voltage difference between ground pins	GND, PGND	−0.3	0.3	V
Charge pump pin voltage	VCP	−0.3	PVDD + 15	V
Digital regulator pin voltage	DVDD	−0.3	5.75	V
Logic pin voltage	PWM1, PWM2, nSLEEP, SCLK, SDO, SDI, nSCS	−0.3	5.75	V
Output logic pin voltage	SDO	−0.3	V _{DVDD} + 0.3	V
Output pin voltage	OUT1-OUT12, ECDRV, ECFB	−0.3	40	V
Output current	OUT1-OUT12, ECDRV, ECFB	Internally Limited	Internally Limited	A
Heater and Electrochromic MOSFET gate drive pin voltage	GH_HS, ECDRV	V _{HEAT} − 0.3 to V _{HEAT} + 13	V _{VCP} + 0.3	V
Heater and Electrochromic MOSFET source pin voltage	SH_HS, ECFB	−0.3	V _{PVDD} + 0.3	V
High-side driver and Heater MOSFET source pin maximum energy dissipation, T _J = 25°C, L _{LOAD} < 100μH	OUT7-OUT12, SH_HS	-	1	mJ
Ambient temperature, T _A		−40	125	°C
Junction temperature, T _J		−40	150	°C
Storage temperature, T _{stg}		−65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings Auto

				VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD ⁽¹⁾ Classification Level 2	PVDD, OUT1 - OUT12, ECFB, GND	±4000	V
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD ⁽¹⁾ Classification Level 2	All other pins	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	Corner pins	±750	
			Other pins	±500	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _{PVDD}	Power supply voltage	PVDD	4.5		35	V
V _{DVDD}	Logic input voltage	DVDD	3		5.5	V
V _{DIN}	Digital input voltage	PWMx, SCLK, SDI	0		5.5	V
I _{DOUT}	Digital output current	SDO	0		5	mA
f _{PWM}	Input PWM frequency	PWM1, PWM2	0		25	kHz
V _{IPROPI}	Analog output voltage	IPROPI	0		3.6	V

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _{I_{PROPI}}	Analog output voltage for V _{PVDD} < 5.6 V	I _{PROPI}	0		V _{PVDD} × 2	V
T _A	Operating ambient temperature		–40		125	°C
T _J	Operating junction temperature		–40		150	°C

6.4 Thermal Information RHA Package

THERMAL METRIC ⁽¹⁾			RHA Package		UNIT
R _{θJA}	Junction-to-ambient thermal resistance		35		°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance		31		°C/W
R _{θJB}	Junction-to-board thermal resistance		26		°C/W
Ψ _{JT}	Junction-to-top characterization parameter		0.1		°C/W
Ψ _{JB}	Junction-to-board characterization parameter		6.7		°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance		1.8		°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

4.5 V ≤ V_{PVDD} ≤ 35 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (DVDD, VCP, PVDD)						
I _{PVDDQ}	PVDD sleep mode current	V _{PVDD} = 13.5 V, nSLEEP = 0 V –40 ≤ T _J ≤ 85°C		2.5	5	μA
I _{DVDDQ}	DVDD sleep mode current	V _{PVDD} = 13.5 V, nSLEEP = 0 V –40 ≤ T _J ≤ 85°C		1	3	μA
I _{PVDD}	PVDD active mode current	V _{PVDD} = 13.5, nSLEEP = 5 V		6.1		mA
I _{DVDD}	DVDD active mode current	V _{DVDD} = 5 V, SDO = 0 V		7.8	8.5	mA
I _{PVDD_CP_DIS}	PVDD charge pump disabled mode current	V _{PVDD} = 13.5 V, DIS_CP = 1, –40 ≤ T _J ≤ 85°C		2		mA
I _{DVDD_CP_DIS}	DVDD charge pump disabled mode current	V _{PVDD} = 13.5 V, V _{DVDD} = 5 V, SDO = 0 V, DIS_CP = 1, –40 ≤ T _J ≤ 85°C		7		mA
t _{SLEEP}	Turnoff time	nSLEEP = 0 V to sleep mode			1	ms
t _{READY_HB_HS}	Turnon time for half-bridges and high-side drivers				5	ms
t _{READY_HEAT}	Turnon time for heater				10	ms
f _{VDD}	Digital oscillator switching frequency	Primary frequency of spread spectrum		14.25		MHz
V _{VCP}	Charge pump regulator voltage with respect to PVDD	V _{PVDD} ≥ 9 V, I _{VCP} ≤ 100 μA	9.5	10.5	11	V
V _{VCP}	Charge pump regulator voltage with respect to PVDD	V _{PVDD} = 7 V, I _{VCP} ≤ 80 μA	8.5	9	11	V
V _{VCP}	Charge pump regulator voltage with respect to PVDD	V _{PVDD} = 5 V, I _{VCP} ≤ 60 μA	7	7.5	11	V
I _{VCP_LIM}	Charge pump output current limit				750	μA
LOGIC-LEVEL INPUTS (INx, nSLEEP, SCLK, SDI, etc)						
V _{IL}	Input logic low voltage	INx, I _{PROPI} , nSLEEP, SCLK, SDI	0.3		V _{DVDD} × 0.3	V
V _{IH}	Input logic high voltage	INx, I _{PROPI} , nSLEEP, SCLK, SDI		V _{DVDD} × 0.7	5.5	V
V _{HYS}	Input hysteresis	INx, I _{PROPI} , nSLEEP, SCLK, SDI		V _{DVDD} × 0.15		V

4.5 V ≤ V_{PVDD} ≤ 35 V, -40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{IL}	Input logic low current	V _{DIN} = 0 V, INx, IPROPI, nSLEEP, SCLK, SDI	-5		5	μA
I _{IL}	Input logic low current	V _{DIN} = 0 V, nSCS		25	50	μA
I _{IH}	Input logic high current	V _{DIN} = 5 V, nSCS	-5		5	μA
I _{IH}	Input logic high current	V _{DIN} = 5 V, INx, IPROPI, nSLEEP, SCLK, SDI		25	50	μA
R _{PD}	Input pulldown resistance	To GND, INx, nSLEEP, SCLK, SDI	140	200	260	kΩ
R _{PU}	Input pullup resistance	To DVDD, nSCS	140	200	265	kΩ
PUSH-PULL OUTPUT SDO						
V _{OL}	Output logic low voltage	I _{OD} = 5 mA			0.5	V
V _{OH}	Output logic high voltage	I _{OD} = -5 mA, SDO	0.8			V
HEATER MOSFET DRIVER						
I _{GH_HS_HEAT}	Average charge-current	T _J = 25 °C		50		mA
R _{GL_HEAT}	On-resistance (discharge stage)	I _{GH_HS_HEAT} = 25 mA; T _J = 25 °C	15	20	25	Ω
		I _{GH_HS_HEAT} = 25 mA; T _J = 125 °C		28	36	Ω
V _{GH_HS_HIGH}	GH_HS high level output voltage	V _{PVDD} = 4.5 V; I _{CP} = 15 mA	V _{SH_HS} + 6			V
		V _{PVDD} = 13.5 V; I _{CP} = 15 mA	V _{SH_HS} + 8 V _{SH_HS} + 10 V _{SH_HS} + 11.5			V
I _{HEAT_SH_STBY_LK}	SH_HS leakage current standby				25	μA
R _{GS_HEAT}	Passive gate-clamp resistance			150		kΩ
t _{PDR_GH_HS}	GH_HS rising propagation delay	V _{PVDD} = 13.5 V; R _G = 0 Ω; C _G = 2.7 nF		0.5		μs
t _{PDF_GH_HS}	GH_HS falling propagation delay	V _{PVDD} = 13.5 V; V _{SH_HS} = 0 V; R _G = 0 Ω; C _G = 2.7 nF		0.5		μs
t _{RISE_GH_HS}	Rise time (switch mode)	V _{PVDD} = 13.5 V; V _{SH_HS} = 0 V; R _G = 0 Ω; C _G = 2.7 nF		300		ns
t _{FALL_GH_HS}	Fall time (switch mode)	V _{PVDD} = 13.5 V; V _{SH_HS} = 0 V; R _G = 0 Ω; C _G = 2.7 nF		170		ns
HEATER PROTECTION CIRCUITS						
V _{DS_LVL_HEAT}	V _{DS} overcurrent protection threshold for heater MOSFET	HEAT_VDS_LVL = 0000b	0.051	0.06	0.069	V
		HEAT_VDS_LVL = 0001b	0.068	0.08	0.092	V
		HEAT_VDS_LVL = 0010b	0.085	0.10	0.115	V
		HEAT_VDS_LVL = 0011b	0.102	0.12	0.138	V
		HEAT_VDS_LVL = 0100b	0.119	0.14	0.161	V
		HEAT_VDS_LVL = 0101b	0.136	0.16	0.184	V
		HEAT_VDS_LVL = 0110b	0.153	0.18	0.207	V
		HEAT_VDS_LVL = 0111b	0.17	0.2	0.23	V
		HEAT_VDS_LVL = 1000b	0.204	0.240	0.276	V
		HEAT_VDS_LVL = 1001b	0.238	0.280	0.322	V
		HEAT_VDS_LVL = 1010b	0.272	0.320	0.368	V
		HEAT_VDS_LVL = 1011b	0.306	0.360	0.414	V
		HEAT_VDS_LVL = 1100b	0.340	0.400	0.460	V
		HEAT_VDS_LVL = 1101b	0.374	0.440	0.506	V
		HEAT_VDS_LVL = 1110b	0.476	0.560	0.644	V
		HEAT_VDS_LVL = 1111b	0.85	1	1.15	V

4.5 V ≤ V_{PVDD} ≤ 35 V, -40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{DS_HEAT_DG}	V _{DS} overcurrent protection deglitch time	HEAT_VDS_DG = 00b	0.75	1	1.5	μs
		HEAT_VDS_DG = 01b	1.5	2	2.5	μs
		HEAT_VDS_DG = 10b	3.25	4	4.75	μs
		HEAT_VDS_DG = 11b	7.5	8	9	μs
t _{DS_HEAT_BLK}	V _{DS} overcurrent protection blanking time	HEAT_VDS_BLK = 00b	3.25	4	4.75	μs
		HEAT_VDS_BLK = 01b	7.5	8	9	μs
		HEAT_VDS_BLK = 10b	14	16	18	μs
		HEAT_VDS_BLK = 11b	28	32	36	μs
V _{OL_HEAT}	Open load threshold voltage	V _{SLx} = 0 V	1.8	2	2.2	V
I _{OL_HEAT}	Pullup current source open-load diagnosis activated	V _{SLx} = 0 V; V _{SHheater} = 4.5 V		1		mA
t _{OL_HEAT}	Open-load filter time for heater MOSFET			2		ms
ELECTROCHROMIC DRIVER						
R _{DS(on)} ECFB	Low-side MOSFET on resistance for EC discharge	V _{PVDD} = 13.5 V; T _J = 25 °C; I _{ECFB} = ±0.5 A ECFB_LS_EN = 1b		1500		mΩ
R _{DS(on)} ECFB	Low-side MOSFET on resistance for EC discharge	V _{PVDD} = 13.5 V; T _J = 150 °C; I _{ECFB} = ±0.5 A ECFB_LS_EN = 1b			3000	mΩ
I _{OC_ECFB}	Output current threshold of low-side MOSFET	V _{PVDD} = 13.5 V; T _J = 25 °C; I _{ECFB} current sink	0.5		1	A
t _{DG_OC_ECFB}	Overcurrent shutdown deglitch time	V _{PVDD} = 13.5 V; T _J = 25 °C; I _{ECFB} current sink	10		50	μs
dV _{ECFB} /dt	Slew rate of ECFB, low-side MOSFET	V _{PVDD} = 13.5 V, V _{DVDD} = 5 V, R _{load} = 64 Ω		7		V/μs
I _{OLP_ECFB}	Open load detection threshold for EC during discharge	EC_OLEN = 1b, ECFB_LS_EN = 1b	10	20	30	mA
t _{DG_OLP_ECFB}	Open load detection deglitch time	EC_OLEN = 1b, ECFB_LS_EN = 1b	400		600	μs
I _{OLA_ECFB}	ECFB Open load pullup current source, OUT11 independent mode	OUT11_EC_MODE = 0b, ECDRV_OL_EN = 1b, EC_ON = 1b		200		μA
V _{EC_CTRLmax}	Maximum EC-control voltage target for ECFB	ECFB_MAX = 1b	1.4		1.6	V
V _{EC_CTRLmax}	Maximum EC-control voltage target for ECFB	ECFB_MAX = 0b	1.12		1.28	V
V _{EC_res}	Minimum resolution for adjustable voltage of ECFB	EC_ON = 1b		23.8		mV
DNL _{ECFB}	Differential Non Linearity	EC_ON = 1b	-2		2	LSB
dV _{ECFB}	Voltage deviation between target and ECFB	V _{target} = 1.5V, dV _{ECFB} = V _{target} - V _{ECFB} ; I _{ECDRV} < 1 μA	-5% (-1LSB)		+5% (+1LSB)	mV
dV _{ECFB}	Voltage deviation between target and ECFB	V _{target} = 23.8 mV, dV _{ECFB} = V _{target} - V _{ECFB} ; I _{ECDRV} < 1 μA	-5% (-1LSB)		+5% (+1LSB)	mV
V _{ECFB_HI}	Indicates voltage at ECFB is higher than target	EC_ON = 1b		V _{target} + 0.12		V
V _{ECFB_LO}	Indicates voltage at ECFB is lower than target	EC_ON = 1b		V _{target} - 0.12		V
t _{FT_ECFB}	Filter time of ECFB high/low flag	EC_ON = 1b		32		μs
t _{BLK_ECFB}	Blanking time of EC regulation flags	Any EC target voltage change	200	250	300	μs
V _{ECFB_UV}	Threshold for undervoltage on ECFB	ECFB_UV_EN = 1b, EC_ON = 1b, ECFB_UV_TH = 0b	75	100	125	mV

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4.5 V ≤ V_{PVDD} ≤ 35 V, -40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{ECFB_UV}	Threshold for undervoltage on ECFB	ECFB_UV_EN = 1b, EC_ON = 1b, ECFB_UV_TH = 1b	170	200	230	mV
t _{ECFB_UV_DG}	Deglitch time for undervoltage flag on ECFB	ECFB_UV_EN = 1b, ECFB_UV_DG = 00b	16	20	24	μs
t _{ECFB_UV_DG}	Deglitch time for undervoltage flag on ECFB	ECFB_UV_EN = 1b, ECFB_UV_DG = 01b	40	50	60	μs
t _{ECFB_UV_DG}	Deglitch time for undervoltage flag on ECFB	ECFB_UV_EN = 1b, ECFB_UV_DG = 10b	80	100	120	μs
t _{ECFB_UV_DG}	Deglitch time for undervoltage flag on ECFB	ECFB_UV_EN = 1b, ECFB_UV_DG = 11b	160	200	240	μs
V _{ECFB_OV}	Threshold for overvoltage on ECFB	ECFB_OV_EN = 1b, EC_ON = 1b	V _{PVDD} - 1V			V
t _{ECFB_OV_DG}	Deglitch time for overvoltage flag on ECFB	ECFB_OV_EN = 1b, ECFB_OV_DG = 00b	16	20	24	μs
t _{ECFB_OV_DG}	Deglitch time for overvoltage flag on ECFB	ECFB_OV_EN = 1b, ECFB_OV_DG = 01b	40	50	60	μs
t _{ECFB_OV_DG}	Deglitch time for overvoltage flag on ECFB	ECFB_OV_EN = 1b, ECFB_OV_DG = 10b	80	100	120	μs
t _{ECFB_OV_DG}	Deglitch time for overvoltage flag on ECFB	ECFB_OV_EN = 1b, ECFB_OV_DG = 11b	160	200	240	μs
V _{ECDRVminHI} GH	Output voltage range of ECDRV when EC_ON = 1	I _{ECDRV} = -10μA	4.3		6.7	V
V _{ECDRVmaxL} OW	Output voltage range of ECDRV when EC_ON = 0	I _{ECDRV} = 10μA	0		0.7	V
I _{ECDRV}	Current into ECDRV	V _{target} > V _{ECFB} + 500 mV; V _{ECDRV} = 3.5 V	-950		-100	μA
I _{ECDRV}	Current into ECDRV	V _{target} < V _{ECFB} - 500 mV; V _{ECDRV} = 1.0 V; V _{target} = 0 V; V _{ECFB} = 0.5 V	150		350	μA
R _{ECDRV_DIS}	Pulldown resistance at ECDRV in fast discharge mode	V _{ECDRV} = 0.7 V; EC enabled, then EC<5:0> = 0 or EC disabled			11	kΩ
t _{DISCHARGE}	Auto-discharge pulse width	ECFB_LS_PWM = 1b, ECFB_LS_EN = 1b	240	300	360	ms
t _{ECFB_DISC_B} LK	Auto-discharge blanking time	ECFB_LS_PWM = 1b, ECFB_LS_EN = 1b	2.25	3	3.75	ms
V _{DISC_TH}	PWM discharge level V _{ECDRV}	ECFB_LS_PWM = 1b, ECFB_LS_EN = 1b	350	400	450	mV
V _{DISC_TH_DIF} F	PWM discharge threshold level V _{ECDRV} - V _{ECFB}	ECFB_LS_PWM = 1b, ECFB_LS_EN = 1b	-50	0	50	mV
HALF-BRIDGE DRIVERS						
R _{ON_OUT1,2_} HS	High-side MOSFET on resistance	I _{OUT} = 1 A, T _J = 25 °C		750		mΩ
		I _{OUT} = 0.5 A, T _J = 150 °C			1425	mΩ
R _{ON_OUT1,2_} LS	Low-side MOSFET on resistance	I _{OUT} = 1 A, T _J = 25 °C		750		mΩ
		I _{OUT} = 0.5 A, T _J = 150 °C			1425	mΩ
R _{ON_OUT3,4_} HS	High-side MOSFET on resistance	I _{OUT} = 4 A, T _J = 25 °C		200		mΩ
		I _{OUT} = 2 A, T _J = 150 °C			400	mΩ
R _{ON_OUT3,4_} LS	Low-side MOSFET on resistance	I _{OUT} = 4 A, T _J = 25 °C		200		mΩ
		I _{OUT} = 2 A, T _J = 150 °C			400	mΩ
R _{ON_OUT5_H} S	High-side MOSFET on resistance	I _{OUT} = 8 A, T _J = 25 °C		66		mΩ
		I _{OUT} = 4 A, T _J = 150 °C			132	mΩ

4.5 V ≤ V_{PVDD} ≤ 35 V, -40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R _{ON_OUT5_LS}	Low-side MOSFET on resistance	I _{OUT} = 8 A, T _J = 25 °C		66		mΩ
		I _{OUT} = 4 A, T _J = 150 °C			132	mΩ
R _{ON_OUT6_HS}	High-side MOSFET on resistance	I _{OUT} = 8 A, T _J = 25 °C		80		mΩ
R _{ON_OUT6_HS}	High-side MOSFET on resistance	I _{OUT} = 4 A, T _J = 150 °C			160	mΩ
R _{ON_OUT6_LS}	Low-side MOSFET on resistance	I _{OUT} = 8 A, T _J = 25 °C		80		mΩ
R _{ON_OUT6_LS}	Low-side MOSFET on resistance	I _{OUT} = 4 A, T _J = 150 °C			160	mΩ
SR _{OUT_HB}	Output voltage rise/fall time for all half-bridge OUTx, 10% - 90%	PVDD = 13.5 V; OUTx_SR = 00b		1.6		V/μs
SR _{OUT_HB}	Output voltage rise/fall time for all half-bridge OUTx, 10% - 90%	PVDD = 13.5 V; OUTx_SR = 01b		13.5		V/μs
SR _{OUT_HB}	Output voltage rise/fall time for all half-bridge OUTx, 10% - 90%	PVDD = 13.5 V; OUTx_SR = 10b		24		V/μs
t _{PD_OUT_HB_HS_R}	Propagation time during output voltage rise for HS	ON command or INx (SPI last transition) to OUTx 10% voltage rise (any SR setting)	1.8		8.7	μs
t _{PD_OUT_HB_HS_F}	Propagation time during output voltage fall for HS	ON command or INx (SPI last transition) to OUTx 10% voltage fall (any SR setting)	1.2		9.2	μs
t _{PD_OUT_HB_LS_R}	Propagation time during output voltage rise for LS	ON command or INx (SPI last transition) to OUTx 10% voltage rise (any SR setting)	1.5		8	μs
t _{PD_OUT_HB_LS_F}	Propagation time during output voltage fall for LS	ON command or INx (SPI last transition) to OUTx 10% voltage fall (any SR setting)	1.4		8	μs
t _{DEAD_HS_ON}	Dead time during output voltage rise for HS	PVDD = 13.5 V; OUTx_ITRIP_LVL = 00b, All SRs	1.3		4.7	μs
t _{DEAD_HS_OF}	Dead time during output voltage fall for HS	PVDD = 13.5 V; OUTx_ITRIP_LVL = 00b, All SRs	1.1		4.8	μs
t _{DEAD_LS_ON}	Dead time during output voltage rise for LS	PVDD = 13.5 V; OUTx_ITRIP_LVL = 00b, All SRs	1.4		5.8	μs
t _{DEAD_LS_OF}	Dead time during output voltage fall for LS	PVDD = 13.5 V; OUTx_ITRIP_LVL = 00b, All SRs	1.7		14	μs
HALF-BRIDGE PROTECTION CIRCUITS						
I _{OC_P_OUT1,2}	Overcurrent protection threshold		1.3		2	A
I _{OC_P_OUT3,4}	Overcurrent protection threshold		4		8	A
I _{OC_P_OUT5}	Overcurrent protection threshold		8		16	A
I _{OC_P_OUT6}	Overcurrent protection threshold		7		13	A
t _{DG_OCP_HB}	Overcurrent protection deglitch time in half-bridge drivers ^{(1) (2)}	OUTX_Y_OCP_DG = 00b (if V _{PVDD} ≥ 28 V, only option)	4.5	6	7.3	μs
		V _{PVDD} ≤ 28 V, OUTX_Y_OCP_DG = 01b	8	10	12	μs
		V _{PVDD} ≤ 28 V, OUTX_Y_OCP_DG = 10b	16	20	24	μs
		V _{PVDD} ≤ 20 V, OUTX_Y_OCP_DG = 11b	48	60	72	μs
I _{ITRIP_OUT1,2}	Current limit to trigger ITRIP regulation for OUT1 and OUT2	OUT1_ITRIP_LVL = 1b and OUT2_ITRIP_LVL = 1b	0.75		1	A
		OUT1_ITRIP_LVL = 0b and OUT2_ITRIP_LVL = 0b	0.60		0.8	A

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4.5 V ≤ V_{PVDD} ≤ 35 V, -40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{ITRIP_OUT3,4}	Current limit to trigger ITRIP regulation for OUT3 and OUT4	OUT3_ITRIP_LVL = 10b and OUT4_ITRIP_LVL = 10b	3		4	A
		OUT3_ITRIP_LVL = 01b and OUT4_ITRIP_LVL = 01b	1.7		3.15	A
		OUT3_ITRIP_LVL = 00b and OUT4_ITRIP_LVL = 00b	1.1		1.5	A
I _{ITRIP_OUT5}	Current threshold to trigger ITRIP regulation for OUT5	OUT5_ITRIP_LVL = 10b	6.6		8.7	A
		OUT5_ITRIP_LVL = 01b	5.6		7.5	A
		OUT5_ITRIP_LVL = 00b	2.5		3.1	A
I _{ITRIP_OUT6}	Current threshold to trigger ITRIP regulation for OUT6	OUT6_ITRIP_LVL = 10b	5.5		7.1	A
I _{ITRIP_OUT6}	Current threshold to trigger ITRIP regulation for OUT6	OUT6_ITRIP_LVL = 01b	4.7		6.1	A
I _{ITRIP_OUT6}	Current threshold to trigger ITRIP regulation for OUT6	OUT6_ITRIP_LVL = 00b	1.9		2.6	A
f _{ITRIP_HB}	Fixed frequency of ITRIP regulation for half-bridge drivers	OUTX_ITRIP_FREQ = 00b	18	20	22	kHz
		OUTX_ITRIP_FREQ = 01b	9	10	11	kHz
		OUTX_ITRIP_FREQ = 10b	4	5	6	kHz
		OUTX_ITRIP_FREQ = 11b	2	2.5	3	kHz
t _{DG_ITRIP_HB}	ITRIP regulation deglitch time for half-bridge drivers	OUTX_ITRIP_DG = 00b	1.5	2	2.5	μs
		OUTX_ITRIP_DG = 01b	4.5	5	5.5	μs
		OUTX_ITRIP_DG = 10b	8	10	12	μs
		OUTX_ITRIP_DG = 11b	16	20	24	μs
I _{OLA_OUT1,2}	Under-current threshold for half-bridges 1 and 2		6	20	30	mA
I _{OLA_OUT3,4}	Under-current threshold for half-bridges 3 and 4		15	50	90	mA
I _{OLA_OUT5}	Under-current threshold for half-bridges 5		40	150	300	mA
I _{OLA_OUT6}	Under-current threshold for half-bridges 6		30	120	240	mA
t _{OLA_HB}	Filter time of open-load signal for half-bridges	Duration of open-load condition to set the status bit		4		ms
A _{IPROP1,2}	Current scaling factor for OUT1-2			650		A/A
A _{IPROP3,4}	Current scaling factor for OUT3-4			2000		A/A
A _{IPROP5}	Current scaling factor for OUT5			4000		A/A
A _{IPROP6}	Current scaling factor for OUT6			3500		A/A
I _{ACC_1,2}	Current sense output accuracy for low current OUT1-2	0.1 A < I _{OUT1,2} < 1 A	-7		7	%
I _{ACC_3,4_LOW}	Current sense output accuracy for low current OUT3-4	0.1 A < I _{OUT3,4} < 0.8 A	-10		10	%
I _{ACC_3,4_HI}	Current sense output accuracy for high current OUT3-4	0.8 A < I _{OUT3,4} < 4 A	-8		8	%
I _{ACC_5_LOW}	Current sense output accuracy for low current OUT5	0.1 A < I _{OUT5} < 0.8 A	-30		30	%
I _{ACC_5_HI}	Current sense output accuracy for high current OUT5	0.8 A < I _{OUT5} < 8 A	-7		7	%
I _{ACC_6_LOW}	Current sense output error for low current OUT6	0.1 A < I _{OUT6} < 0.8 A	-30		30	%
I _{ACC_6_HI}	Current sense output accuracy for high current OUT6	0.8 A < I _{OUT6} < 8 A	-7		7	%

4.5 V ≤ V_{PVDD} ≤ 35 V, -40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R _{S_GND}	Resistance on OUTx to GND detected as a short	V _{DVDD} = 5 V, V _{OLP_REF} = 2.65 V			1	kΩ
R _{S_PVDD}	Resistance on OUTx to PVDD detected as a short	V _{DVDD} = 5 V, V _{OLP_REF} = 2.65 V			1	kΩ
R _{OPEN_HB}	Resistance on OUTx detected as an open	V _{DVDD} = 5 V, V _{OLP_REF} = 2.65 V	1.5			kΩ
V _{OLP_REFH}	OLP comparator Reference High			2.65		V
V _{OLP_REFL}	OLP comparator Reference Low			2		V
R _{OLP_PU}	Internal pullup resistance on OUTx to VDD during OLP			1		kΩ
R _{OLP_PD}	Internal pulldown resistance on OUTx to VDD during OLP			1		kΩ
HIGH-SIDE DRIVERS						
R _{DS(on)} OUT7 (low R _{DS(on)} mode)	High-side MOSFET on resistance in low resistance mode	T _J = 25 °C; I _{OUT7} = ±0.5 A		400		mΩ
		T _J = 150 °C; I _{OUT7} = ±0.25 A			800	mΩ
R _{DS(on)} OUT7 (high R _{DS(on)} mode)	High-side MOSFET on resistance in high resistance mode	T _J = 25 °C; I _{OUT7} = ±0.5 A		1500		mΩ
		T _J = 150 °C; I _{OUT7} = ±0.25 A			2800	mΩ
R _{DS(on)} OUT8	High-side MOSFET on resistance	T _J = 25 °C; I _{OUT8} = ±0.25 A		1500		mΩ
		T _J = 150 °C; I _{OUT8} = ±0.125 A			2800	mΩ
R _{DS(on)} OUT9	High-side MOSFET on resistance	T _J = 25 °C; I _{OUT9} = ±0.25 A		1500		mΩ
		T _J = 150 °C; I _{OUT9} = ±0.125 A			2800	mΩ
R _{DS(on)} OUT10	High-side MOSFET on resistance	T _J = 25 °C; I _{OUT10} = ±0.25 A		1500		mΩ
		T _J = 150 °C; I _{OUT10} = ±0.125 A			2800	mΩ
R _{DS(on)} OUT11	High-side MOSFET on resistance	T _J = 25 °C; I _{OUT11} = ±0.25 A		1500		mΩ
		T _J = 150 °C; I _{OUT11} = ±0.125 A			2800	mΩ
R _{DS(on)} OUT12	High-side MOSFET on resistance	T _J = 25 °C; I _{OUT12} = ±0.25 A		1500		mΩ
		T _J = 150 °C; I _{OUT12} = ±0.125 A			2800	mΩ
SR _{HS_OUT7_HI}	Slew rate for OUT7 High R _{DS(on)} mode	OUT7_RDSON_MODE = 0b, 10 to 90%		0.35		V/μs
SR _{HS_OUT7_LO}	Slew rate for OUT7 Low R _{DS(on)} mode	OUT7_RDSON_MODE = 1b, 10 to 90%		0.29		V/μs
SR _{HS}	Slew rate for OUT8 – OUT12	10 to 90%		1.54		V/μs
t _{PD_OUT7_HI}	Propagation delay time driver for OUT7 High R _{DS(on)} mode	High-side ON command (SPI last transition) to OUT7 transition from Hi-Z state		16		μs
t _{PD_OUT7_LO}	Propagation delay time driver for OUT7 Low R _{DS(on)} mode	High-side ON command (SPI last transition) to OUT7 transition from Hi-Z state		19		μs
t _{PD_HS}	Propagation delay time driver for high-side drivers OUT8 – OUT12	High-side OFF command (SPI last transition) to OUTx transition from ON state		2		μs
f _{PWMx(00)}	PWM switching frequency	PWM_OUTX_FREQ = 00b	78	108	138	Hz
f _{PWMx(01)}	PWM switching frequency	PWM_OUTX_FREQ = 01b	157	217	277	Hz
f _{PWMx(10)}	PWM switching frequency	PWM_OUTX_FREQ = 10b	229	289	359	Hz
I _{LEAK_H}	Switched-off output current high-side drivers of OUT7-12	V _{OUT} = 0 V; standby mode	-10			μA
HIGH-SIDE DRIVER PROTECTION CIRCUITS						

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4.5 V ≤ V_{PVDD} ≤ 35 V, -40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{OC7}	Overcurrent threshold in high R _{DS(on)} mode	OUT7_RDSON_MODE = 0b	500		750	mA
	Overcurrent threshold in low R _{DS(on)} mode	OUT7_RDSON_MODE = 1b	1500		2500	mA
I _{OC8} , I _{OC9} , I _{OC10} , I _{OC11} , I _{OC12}	Overcurrent threshold OUT8 - OUT12	OUTX_OC_TH = 0b	250		500	mA
I _{OC8} , I _{OC9} , I _{OC10} , I _{OC11} , I _{OC12}	Overcurrent threshold OUT8 - OUT12	OUTX_OC_TH = 1b	500		1000	mA
I _{CCM_OUT7}	Constant current level for high-side driver OUT7 High R _{DS(on)}	OUT7_RDSON_MODE = 0b, OUT7_CCM_EN = 1b, OUT7_CCM_TO = 0b	100		175	mA
I _{CCM_OUT7}	Constant current level for high-side driver OUT7 High R _{DS(on)}	OUT7_RDSON_MODE = 0b, OUT7_CCM_EN = 1b, OUT7_CCM_TO = 1b	200		350	mA
I _{CCM}	Constant current level for high-side drivers	OUTX_CCM_EN = 1b, OUTX_CCM_TO = 0b	100		175	mA
		OUTX_CCM_EN = 1b, OUTX_CCM_TO = 1b	200		350	mA
t _{CCMto}	Constant current mode time expiration	OUTX_CCM_EN = 1b, OUTX_CCM_TO = 0b	16	20	24	ms
		OUTX_CCM_EN = 1b, OUTX_CCM_TH = 1b	8	10	12	ms
t _{OCP_HS_DG}	Overcurrent protection deglitch time in high side drivers ⁽¹⁾ ⁽²⁾	OUTX_HS_OCP_DG = 00b	4.5	6	7.3	μs
		OUTX_HS_OCP_DG = 01b	8	10	12	μs
		OUTX_HS_OCP_DG = 10b	16	20	24	μs
		OUTX_HS_OCP_DG = 11b	48	60	72	μs
t _{ITRIP_HS_BLK}	Blanking time of OUT7 ITRIP	OUT7_ITRIP_EN = 1b; OUT_ITRIP_BLK = 01b		0		μs
		OUT7_ITRIP_EN = 1b; OUT_ITRIP_BLK = 10b	16	20	24	μs
		OUT7_ITRIP_EN = 1b; OUT_ITRIP_BLK = 11b	32	40	48	μs
t _{ITRIP_HS_DG}	ITRIP filter time for high-side driver OUT7	OUT7_ITRIP_DG = 00b	39	48	59	μs
		OUT7_ITRIP_DG = 01b	32	40	48	μs
		OUT7_ITRIP_DG = 10b	26	32	38	μs
		OUT7_ITRIP_DG = 11b	19	24	29	μs
f _{ITRIP_HS}	ITRIP frequency for high-side driver OUT7	OUT7_ITRIP_FREQ = 00b		1.7		kHz
		OUT7_ITRIP_FREQ = 01b		2.2		kHz
		OUT7_ITRIP_FREQ = 10b		3		kHz
		OUT7_ITRIP_FREQ = 11b		4.4		kHz
I _{OLD7}	Open-load threshold for OUT7	OUT7_OLA_TH = 0b	15		40	mA
	Open-load threshold for OUT7	OUT7_OLA_TH = 1b	5		15	mA
I _{OLD8} , I _{OLD9} , I _{OLD10} , I _{OLD11} , I _{OLD12}	Open-load threshold for OUT8 - OUT12	OUTX_OLA_TH = 0b	0.5		4	mA
		OUTX_OLA_TH = 1b	6		16	mA
t _{OLD_HS}	Filter time of open-load signal for high-side drivers	Duration of open-load condition to set the status bit		200	250	μs
A _{I_{PROPI7_LO}}	Current scaling factor for OUT7 in low on-resistance mode	OUT7_RDSON_MODE = 1b		750		A/A

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
A _{IPROPI7_HI}	Current scaling factor for OUT7 in high on-resistance mode	OUT7_RDSON_MODE = 0b		250		A/A
A _{IPROPI8} , A _{IPROPI9} , A _{IPROPI10} , A _{IPROPI11} , A _{IPROPI12}	Current scaling factor for OUT8-12			250		A/A
I _{ACC_7_HI_RDSON}	Current sense output accuracy for OUT7 in high RDSON mode	0.1 A < I _{OUT7} < 0.5 A	-18		18	%
I _{ACC_7_LOW_RDSON}	Current sense output accuracy for OUT7 in low RDSON mode	0.5 A < I _{OUT7} < 1.5 A	-14		14	%
I _{ACC_8-12_LO}	Current sense output accuracy for low current OUT8-12	0.05 A < I _{OUT8-12} < 0.1 A	-28		28	%
I _{ACC_8-12_HI}	Current sense output accuracy for high current OUT8-12	0.1 A < I _{OUT8-12} < 0.5 A	-18		18	%
t _{IPROPI_BLK}	IPROPI blanking time			32		µs
PROTECTION CIRCUITS						
V _{CP_UV}	Charge pump undervoltage threshold	V _{VCP} - V _{PVDD} , V _{VCP} falling	5.5	6	7	V
t _{CP_UV_DG}	Charge pump undervoltage deglitch time		8	10	12.75	µs
V _{PVDD_UV}	PVDD undervoltage threshold	V _{PVDD} rising	4.425	4.725	5	V
		V _{PVDD} falling	4.15	4.425	4.7	V
V _{PVDD_UV_HYS}	PVDD undervoltage hysteresis	Rising to falling threshold		200		mV
t _{PVDD_UV_DG}	PVDD undervoltage deglitch time		8	10	12.75	µs
V _{PVDD_OV}	PVDD overvoltage threshold	V _{PVDD} rising, PVDD_OV_LVL = 0b	21	22	23	V
		V _{PVDD} falling, PVDD_OV_LVL = 0b	20	21	22	V
		V _{PVDD} rising, PVDD_OV_LVL = 1b	27	28	29	V
		V _{PVDD} falling, PVDD_OV_LVL = 1b	26	27	28	V
V _{PVDD_OV_HYS}	PVDD overvoltage hysteresis	Rising to falling threshold		1		V
t _{PVDD_OV_DG}	PVDD overvoltage deglitch time	PVDD_OV_DG = 00b	0.75	1	1.5	µs
		PVDD_OV_DG = 01b	1.5	2	2.5	µs
		PVDD_OV_DG = 10b	3.25	4	4.75	µs
		PVDD_OV_DG = 11b	7	8	9	µs
V _{DVDD_POR}	DVDD supply POR threshold	DVDD falling	2.5	2.7	2.9	V
		DVDD rising	2.6	2.8	3	V
V _{DVDD_POR_HYS}	DVDD POR hysteresis	Rising to falling threshold		100		mV
t _{DVDD_POR_DG}	DVDD POR deglitch time		5	12	25	µs
t _{WD}	Watchdog timer period	WD_WIN = 0b	36	40	44	ms
		WD_WIN = 1b	90	100	110	ms
A _{IPROPI_PVD_D_VOUT}	IPROPI PVDD Voltage Sense Output Scaling Factor		30	32	34	V/V
V _{IPROPI_TEMP_VOUT}	IPROPI Temperature Sense Output		-17		+17	°C
T _{OTW1}	Low Thermal warning temperature	T _J rising	100	115	130	°C
T _{OTW2}	High Thermal warning temperature	T _J rising	125	140	155	°C
T _{HYS}	Thermal warning hysteresis			20		°C
T _{OTSD}	Thermal shutdown temperature	T _J rising	155	170	185	°C

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4.5 V ≤ V_{PVDD} ≤ 35 V, -40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T _{HYS}	Thermal shutdown hysteresis			20		°C
t _{OTSD_DG}	Thermal shutdown deglitch time			10		μs

- (1) For 20-V < V_{PVDD} < 28-V, the OCP deglitch time must be limited to up to 20-μs (OUTX_HB_OCP_DEG or OUTX_HS_OCP_DEG = 10b).
- (2) For V_{PVDD} > 28 V, the OCP deglitch time must be limited to 6-μs (Lowest Deglitch Value, (OUTX_HB_OCP_DEG or OUTX_HS_OCP_DEG = 00b).

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
t _{READY_SPI}	SPI ready after power up			1	ms
t _{SCLK}	SCLK minimum period	100			ns
t _{SCLKH}	SCLK minimum high time	50			ns
t _{SCLKL}	SCLK minimum low time	50			ns
t _{SU_SDI}	SDI input data setup time	25			ns
t _{H_SDI}	SDI input data hold time	25			ns
t _{D_SDO}	SDI output data delay time			30	ns
t _{SU_nSCS}	nSCS input setup time	25			ns
t _{H_nSCS}	nSCS input hold time	25			ns
t _{HI_nSCS}	SDO minimum high time	125			ns
t _{EN}	SDO enable delay time			50	ns
t _{DIS}	SDO disable delay time			50	ns

7 Detailed Description

7.1 Overview

The DRV8001-Q1 device integrates multiple types of drivers intended for multiple functions: driving and diagnosing motor (inductive), resistive and capacitive loads. The device features 6 integrated half-bridges, 6 integrated high-side drivers, one high-side external MOSFET gate driver for heater, one high-side gate driver for electrochromic charge and one integrated low-side driver for electrochromic load discharge. Each driver features current sensing, protection and diagnostics along with system protection and diagnostics, which increases system integration and reduces total system size and cost.

The half-bridge drivers can be controlled through SPI register or PWM pins PWM1 and PWM2. The half-bridges have configurable current chopping scheme called ITRIP. Protection circuits include short-circuit protection, active and passive open load detection.

The high-side drivers can be controlled through SPI register, external PWM pin (PWM1), or with a dedicated PWM generator which enables load regulation during operation. High-side drivers also have optional constant current mode regulation for LED module loads. One high-side driver is configurable to drive either a lamp or LED load. Protection circuits include short-circuit protection and open load detection.

The device also has an external MOSFET drivers for resistive heating element. The heater MOSFET driver can be controlled with SPI register or with PWM pin (PWM1) and feature both short-circuit and open load detection.

There is also an electrochromic (EC) mirror driver. The EC driver is controlled only through SPI register. For EC drive, the driver control loop regulates the EC voltage to a 6-bit target voltage. To discharge the EC element or change target voltage, there is an integrated low-side MOSFET to discharge the EC element in either two discharge modes, a PWM discharge and fast discharge options. The EC driver protection includes LS overcurrent and open load detection.

IPROPI pin is an output pin that can provide proportional current sense from any integrated driver with current sense. IPROPI can be also configured to output a scaled down PVDD input voltage or one of four internal temperature cluster output voltage.

7.2 Functional Block Diagram

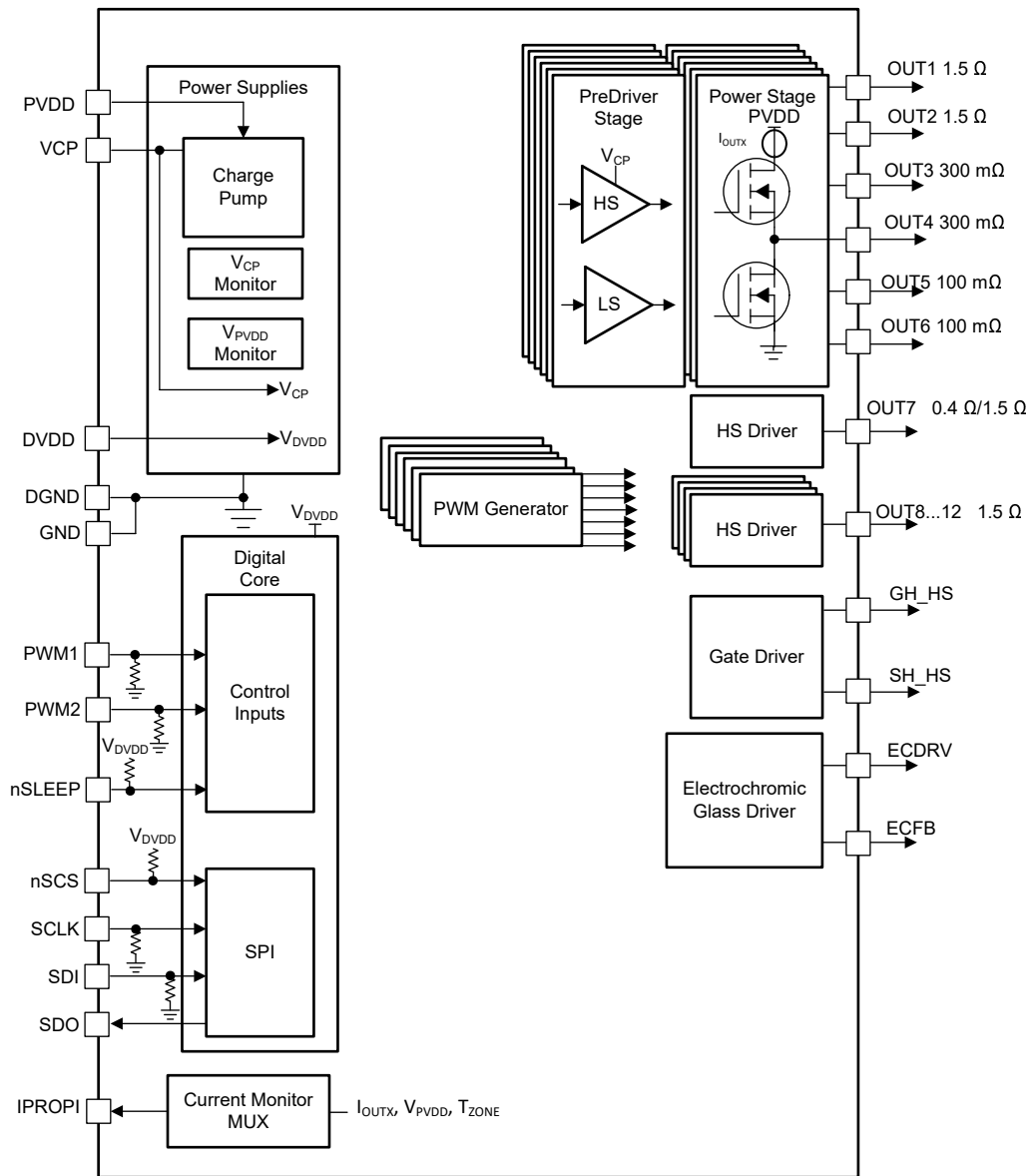


Figure 7-1. Block Diagram for DRV8001-Q1

7.3 External Components

Table 7-1 lists the recommended external components for the device.

Table 7-1. Recommended External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C _{PVDD1}	PVDD	GND	0.1 μF, low ESR ceramic capacitor, PVDD-rated.
C _{PVDD2}	PVDD	GND	Local bulk capacitance greater than or equal to 10 μF, PVDD-rated.
C _{DVDD}	DVDD	GND	1 μF, 6.3V, low ESR ceramic capacitor
C _{VCP}	VCP	PVDD	1 μF 16V, low ESR ceramic capacitor
R _{IPROPI}	IPROPI	GND	Typically 1000 - 1800 Ω 0.063W resistor to GND, depending on the controller supply voltage rail.
C _{IPROPI}	IPROPI		4.7 nF, 6.3V, low ESR ceramic capacitor.

Table 7-1. Recommended External Components (continued)

COMPONENT	PIN 1	PIN 2	RECOMMENDED
R_{ECDRV}	ECDRV	GND	Typically 220 Ω series resistance between ECDRV pin and gate of external MOSFET to stabilize control loop
C_{ECDRV}	ECDRV	GND	4.7nF, low ESR ceramic capacitor Note Voltage rating for this capacitor is based on short to battery assumptions for ECFB.
C_{ECFB}	ECFB	GND	220nF, low ESR ceramic capacitor Note Voltage rating for this capacitor is based on short to battery assumptions for ECFB.

7.4 Feature Description

The table below provides links to all feature descriptions of key blocks of the device.

Table 7-2. Table of Device Features by Section

Device Block
Heater MOSFET Driver
Electrochromic Glass Driver
High-side Drivers
Half-bridge Drivers
IPROPI
Protection Circuits
Thermal Clusters
Fault Table

7.4.1 Heater MOSFET Driver

Table 7-3. Heater Driver Section Table of Contents

Heater Section	Link to Section
Back to Top of Feature Section	Section 7.4
Heater Driver Control	Section 7.4.1.1
Heater Driver Protection	Section 7.4.1.2

This is an external high-side MOSFET gate driver that can be used for driving resistive heating elements. The driver is controlled through SPI or PWM, and has programmable active short detection and off-state open-load detection.

7.4.1.1 Heater MOSFET Driver Control

The heater MOSFET driver control mode is configured with [HEAT_OUT_CNFG](#) bits in register [HS_HEAT_OUT_CNFG](#). The heater configuration bits enable or disable control of the heater output, and configures the control source. For the heater driver, the control sources are SPI register control and PWM pin control.

When in SPI register control mode ([HEAT_OUT_CNFG](#) = 01b), the heater MOSFET gate drive is enabled and disabled by setting bit [HEAT_EN](#) in the register [HS_EC_HEAT_CTRL](#).

When in PWM control mode ([HEAT_OUT_CNFG](#) = 10b), the gate driver is controlled with an external PWM signal on pin PWM1. If the heater driver is in PWM control mode, then [HEAT_EN](#) is ignored.

The table below summarizes the heater driver configuration and control options:

Table 7-4. Heater Configuration

HEAT_OUT_CNFG bits	Configuration	Description
00b	OFF	Heater control disabled
01b	SPI register control	Heater SPI control enabled
10b	PWM1 control	Heater control by PWM pin 1
11b	OFF	Heater control disabled

Below is the block diagram for the heater driver block:

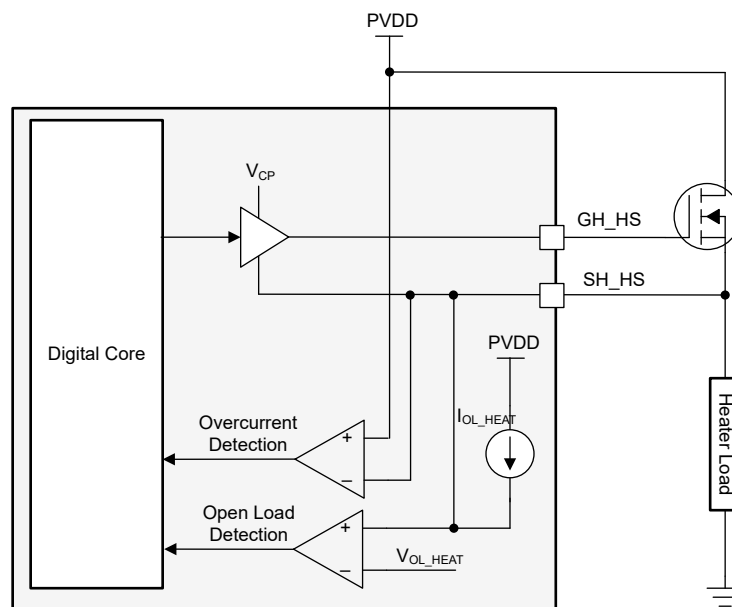


Figure 7-2. Heater MOSFET Driver Block Diagram

The timing waveform below shows the expected timing for the heater driver:

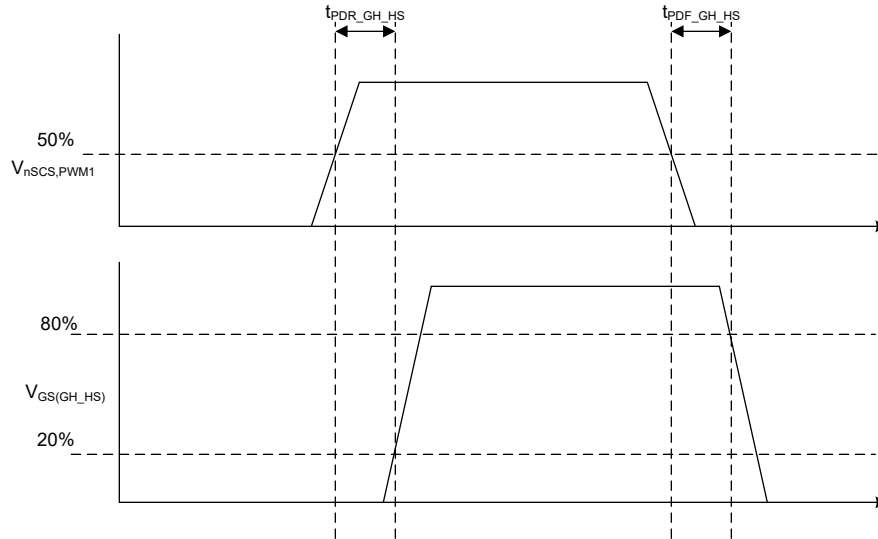


Figure 7-3. Heater Timing Diagram

7.4.1.2 Heater MOSFET Driver Protection

The heater driver has an active short-circuit detection and an off-state open-load detection.

7.4.1.2.1 Heater SH_HS Internal Diode

Only a limited amount of energy (<1mJ) can be dissipated by the internal ESD diodes on SH_HS pin. TI recommends adding an external diode from ground to SH_HS pin in case of a load short condition. During a heater load short condition, the current is limited only by the saturation current of the external heater MOSFET. If the heater output is configured to shut off due to short-circuit detection, this same current dissipates through the internal ESD diode from ground to SH_HS, which is larger than the what the internal ESD diode can dissipate.

7.4.1.2.2 Heater MOSFET V_{DS} Overcurrent Protection (HEAT_VDS)

If the voltage across the heater driver V_{DS} overcurrent comparator exceeds the $V_{DS_LVL_HEAT}$ for longer than the $t_{DS_HEAT_DG}$ time, a heater overcurrent condition is detected. The voltage threshold and deglitch time can be adjusted through the [EC_CNFG](#) and [HEAT_CNFG](#) register settings.

Table 7-5. Heater VDS Levels

HEAT_VDS_LVL	VDS Voltage Level
0000b	0.06V
0001b	0.08V
0010b	0.10V
0011b	0.12V
0100b	0.14V
0101b	0.16V
0110b	0.18V
0111b	0.2V
1000b	0.24V
1001b	0.28V
1010b	0.32V
1011b	0.36V
1100b	0.4V
1101b	0.44V

Table 7-5. Heater VDS Levels (continued)

HEAT_VDS_LVL	VDS Voltage Level
1110b	0.56V
1111b	1V

Table 7-6. Heater VDS Deglitch Times

HEAT_VDS_DG	Time
00b	1μs
01b	2μs
10b	4μs
11b	8μs

There is also a heater MOSFET V_{DS} monitor blanking period that is configured in bit [HEAT_VDS_BLK](#) in register [HEAT_CNFG](#). There are four blanking time options:

Table 7-7. Heater VDS Blanking Times

HEAT_VDS_BLK	Time
00b	4μs
01b	8μs
10b	16μs
11b	32μs

The heater overcurrent monitor can respond and recover in four different modes set through the [HEAT_VDS_MODE](#) register setting.

- **Latched Fault Mode:** After detecting the overcurrent event, the gate driver pulldown is enabled and [HEAT_VDS](#) is asserted. After the overcurrent event is removed, the fault state remains latched until [CLR_FLT](#) is issued.
- **Cycle by Cycle Mode:** After detecting the overcurrent event, the gate driver pulldown is enabled and [HEAT_VDS](#), [EC_HEAT](#) and [FAULT](#) bits are asserted. [EC_HEAT](#) and [FAULT](#) status bit in register [IC_STAT1](#) remains asserted until driver control input changes (SPI or PWM). **To clear [HEAT_VDS](#) bit, a [CLR_FLT](#) command must be sent after an input change.** If [CLR_FLT](#) is issued before an input change, all three status bits remain asserted and the driver pulldown stays enabled.
- **Warning Report Only Mode:** The heater overcurrent event is reported in the [WARN](#) and [HEAT_VDS](#) bits. The device does not take any action. The warning remains latched until [CLR_FLT](#) is issued.
- **Disabled Mode:** The heater V_{DS} overcurrent monitors are disabled and do not respond or report.

7.4.1.2.3 Heater MOSFET Open Load Detection

Off-state open-load monitoring is done by comparing the voltage difference SH_HS node when pulled up by current source against open-load threshold voltage V_{OL_HEAT} . If SH_HS voltage exceeds the open-load threshold V_{OL_HEAT} for longer than filter time t_{OL_HEAT} , the open-load bit [HEAT_OL](#) is set. Open-load monitor is controlled by bit [HEAT_OLP_EN](#).

Note

The heater open load diagnostics only works when the heater configuration is disabled, where bits [HEAT_OUT_CNFG](#) must be 00b.

7.4.2 High-Side Drivers

Table 7-8. High-Side Driver Section Table of Contents

Half-bridge Section	Link to Section
Back to Top of Feature Section	Section 7.4
High-side Driver Control	Section 7.4.2.1
High-side Driver (OUT7) Regulation	Section 7.4.2.1.2.2
High-side Driver Protection	Section 7.4.2.1.3

The device integrates 6 high-side drivers, OUT7 - OUT12, that can be programmed to drive several load types. Each high-side driver has selectable high or low current protection and open-load current thresholds. OUT7 can be configured to drive lamps, bulbs, or LEDs. All high-side drivers also have a fixed-time constant current mode intended for driving high capacitance LED modules.

Every high-side driver has open-load detection and short-circuit protection (OCP). OUT7 has an optional ITRIP regulation for lamp or bulb loads. If the electrochromic driver is used, OUT11 is used to provide protected battery voltage for the EC element.

Below is a block diagram of the high-side drivers:

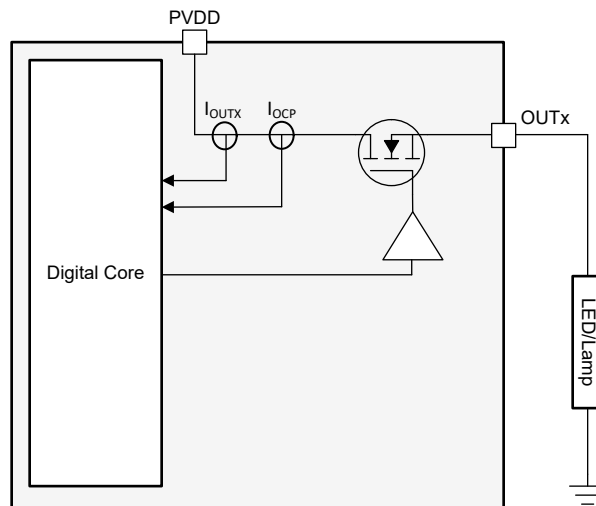


Figure 7-4. High-Side Driver Block Diagram

The table below summarizes all the device high-side drivers with their corresponding feature sets:

Table 7-9. High-Side Drivers and Features

High-Side Driver	RDSON (Ω)	OL Detect	OCP Latch	ITRIP	CCM	Used for EC Supply
OUT7	0.4/1.5	Yes	Yes	Yes	Yes	No
OUT8	1.5	Yes	Yes	No	Yes	No
OUT9	1.5	Yes	Yes	No	Yes	No
OUT10	1.5	Yes	Yes	No	Yes	No
OUT11	1.5	Yes	Yes	No	Yes	Yes
OUT12	1.5	Yes	Yes	No	Yes	No

7.4.2.1 High-side Driver Control

The high-side drivers can be configured for control by SPI register, an internally generated PWM signal from 10-bit PWM generator or an external PWM signal from PWM1 pin. This configuration is done by setting [OUTx_CNFG](#) (OUT7-OUT12) bits in register [HS_HEAT_OUT_CNFG](#).

In SPI register control mode, ([OUTx_CNFG](#) = 01b), the high-side output follows the [OUTx_EN](#) bit (ON/OFF).

The table below summarizes the high-side driver configuration options:

Table 7-10. High-side Driver Configuration

OUTx_CNFG bits	Configuration	Description
00	OFF	High-side driver control disabled
01	SPI register control	High-side driver SPI control enabled
10	PWM1 pin control	High-side driver control by PWM pin 1
11	PWM Generator	High-side driver control with dedicated internal PWM generator

7.4.2.1.1 High-side Drivers - Parallel Outputs

The high-side drivers OUT8 through OUT12 can be connected in parallel combinations to support even higher current loads. For example, OUT8 and OUT9 can be connected in parallel as a 600mΩ driver effectively, or OUT9, OUT10, and OUT12 can be connected in parallel as a 400mΩ driver effectively.

However, there are limitations with this mode of operation:

- Internal PWM control does not work for parallel high-side drivers and must not be configured for this mode of operation.
- Constant current mode is not possible and must be disabled.
- Protection circuitry functions, but trip at different thresholds.

If operating in parallel, the high-side drivers must be configured for ON/OFF SPI register control or external PWM signal control through pin.

7.4.2.1.2 High-side Driver PWM Generator

Each high-side driver has a dedicated PWM generator with 10-bit duty cycle resolution. The frequency and duty of each PWM generator can be controlled independently.

When configuring the high-side driver for operation with internal PWM generator, the frequency must be selected before configuring the high-side driver with internal PWM generator.

Required Register Configuration Sequence:

1. Configure the high-side driver PWM frequency mode in register [HS_PWM_FREQ_CNFG](#)
2. Set the duty cycle in register [OUTx_PWM_DC](#)
3. Configure the driver mode of operation in register [HS_HEAT_OUT_CNFG](#)

The frequency of the PWM generator is controlled by bits [PWM_OUTX_FREQ](#) from register [HS_PWM_FREQ_CNFG](#) as shown in the table below:

Table 7-11. PWM Frequency

PWM_OUTX_FREQ	PWM Frequency (Hz)
00b	108
01b	217
10b	289
11b	Reserved

7.4.2.1.2.1 Constant Current Mode

All high-side drivers have a timed constant current mode feature, which can be used to provide a constant current for a short duration to the desired output. This mode is enabled with bit [OUTx_CCM_EN](#) in register [HS_REG_CNFG2](#). When enabled, the current from the high-side driver is limited to the configured limit for a short duration (10 or 20 ms).

There are two timing and current limit options for constant current mode. This is configured with bit [OUTX_CCM_TO](#) in register [HS_REG_CNFG2](#), summarized in the table below:

Table 7-12. Constant Current Mode Options

OUTX_CCM_TO	Current Limit (I_{CCM})	Timeout (t_{CCMto})
0b	200 mA	20 ms
1b	390 mA	10 ms

This constant current mode feature is enabled only if the [OUTx_CCM_EN](#) bit is set prior to enabling the high-side driver. CCM automatically expires after expiration time $t_{CCMtimeout}$. After timeout, the driver remains enabled and configured based on [OUTx_CNFG](#) bits in register [HS_EC_HEAT_CTRL](#).

Required Register Configuration Sequence:

1. Configure the high-side driver CCM mode in register [HS_REG_CNFG2](#)
2. Configure the high-side driver operation in register [HS_HEAT_OUT_CNFG](#)

If constant current mode is configured after configuring the high-side driver, the CCM mode does not regulate.

For [OUTx_CCM_EN](#) bit:

- If [OUTx_CCM_EN](#) is cleared by the controller before constant current mode timeout, the driver follows the command and is switched to the mode corresponding to [OUTx_CNFG](#) bits
- If [OUTx_CCM_EN](#) is set after the driver has already been enabled, the [OUTx_CCM_EN](#) bit is ignored; in this case [OUTx_CCM_EN](#) remains off

The short-circuit and overcurrent detection are active/enabled when the driver is ON, PWM driven, but NOT in constant current mode. Open load detection is always active.

7.4.2.1.2.2 OUT7 HS ITRIP Behavior

For OUT7 in low-RDSON mode, there is a fixed frequency current regulation feature called HS ITRIP that can be used to restart the driver if overcurrent occurs. This ITRIP feature (separate from ITRIP for half-bridges) is available for OUT7 (and EC driver) of the high-side drivers, and intended for loads which have inrush currents that are higher than the overcurrent protection threshold of a driver, such as a lamp or bulb.

For HS ITRIP to work, [OUT7 OCP](#) must be disabled.

If bit [OUT7_ITRIP_CNFG](#) bits are non-zero, and the load current on OUT7 exceeds I_{OC7} threshold, ITRIP regulation takes place. The status bit is [OUT7_ITRIP_STAT](#) in register [EC_HEAT_ITRIP_STAT](#) is asserted depending on [OUT7_ITRIP_CNFG](#) configuration.

There is also an optional OUT7 ITRIP timeout feature. Depending on [OUT7_ITRIP_CNFG](#) settings, OUT7 or ITRIP regulation can be disabled after timeout is exceeded. For [OUT7_ITRIP_CNFG](#) = 01b, OUT7 is disabled if ITRIP regulation time t_{OUT7_ITRIP} occurs for longer than the configured timeout $t_{OUT7_ITRIP_TO}$. For [OUT7_ITRIP_CNFG](#) = 11b, ITRIP Regulation is disabled if ITRIP regulation time t_{OUT7_ITRIP} occurs for longer than the configured timeout $t_{OUT7_ITRIP_TO}$. In both cases, the status bit [OUT7_ITRIP_TO](#) is latched. Bits [OUT7_ITRIP_CNFG](#) is located in register [HS_REG_CNFG1](#). To configure OUT7 ITRIP regulation for indefinite operation, set [OUT7_ITRIP_CNFG](#) = 10b.

The table below summarizes the regulation, status and fault behavior of OUT7 ITRIP.

Table 7-13. OUT7 ITRIP Configuration and Status Summary

OUT7_ITRIP_CNFG[1]	OUT7_ITRIP_CNFG[0]	Mode Description	OUT7_ITRIP_STAT	ITRIP Stat Fault Clear	OUT7_ITRIP_TO	ITRIP Timeout Fault Clear
0b	0b	No ITRIP regulation	Latches when OUT7 overcurrent threshold exceeded	CLR_FLT command	Timeout disabled	n/a

Table 7-13. OUT7 ITRIP Configuration and Status Summary (continued)

OUT7_ITRIP_CN FG[1]	OUT7_ITRIP_CN FG[0]	Mode Description	OUT7_ITRIP_STA T	ITRIP Stat Fault Clear	OUT7_ITRIP_TO	ITRIP Timeout Fault Clear
0b	1b	ITRIP regulation	Latches after timeout	CLR_FLT command. Auto-clears if previously latched.	Latched after timeout limit reached.	CLR_FLT restarts the driver if disabled.
1b	0b	Safe Retry with ITRIP regulation	Latches when OUT7 overcurrent threshold exceeded	CLR_FLT restarts the driver with regulation.	Timeout disabled	n/a
1b	1b	ITRIP regulation with timeout and regulation disable	Latches after timeout limit reached. After fault clear, re-latches if OUT7 overcurrent threshold still exceeded	CLR_FLT command. Auto-clear at start.	Latched after timeout limit reached.	CLR_FLT restarts the regulation if disabled.

The table below summarizes time limit options:

Table 7-14. OUT7 ITRIP Timeout Options

ITRIP_TO_SEL	Timeout Time
00b	100ms
01b	200ms
10b	250ms
11b	290ms

HS ITRIP mode is disabled as the default setting for OUT7. To set OUT7 in HS ITRIP mode:

1. Configure OUT7 for low-RDSON mode by setting bit [OUT7_RDSON_MODE](#) = 1 in register [HS_OC_CNFG](#).
2. Enable and configure OUT7 ITRIP by setting bits [OUT7_ITRIP_CNFG](#) = 1Xb in register [HS_REG_CNFG1](#) per the [OUT7 ITRIP configuration summary table](#).
3. If timeout is used, configure timeout limit with [ITRIP_TO_SEL](#) bits in [HS_REG_CNFG1](#).
4. Set ITRIP timing parameters. ITRIP frequency, blanking and deglitch configured with bits [OUT7_ITRIP_FREQ](#), [OUT7_ITRIP_BLK](#) and [OUT7_ITRIP_DG](#) in register [HS_REG_CNFG1](#).
5. Disable OCP for OUT7 with bit [OUT7_OCP_DIS](#) in register [HS_REG_CNFG1](#).

Table 7-15. OUT7 ITRIP Frequency Option Summary

Frequency (f_{ITRIP_HS})	OUT7_ITRIP_FREQ
1.7kHz	00b
2.2kHz	01b
3kHz	10b
4.4kHz	11b

Table 7-16. OUT7 ITRIP Blanking Option Summary

Blanking Time ($t_{ITRIP_HS_BLK}$)	OUT7_ITRIP_BLK
RSVD	00b
0 μ s	01b
20 μ s	10b
40 μ s	11b

Table 7-17. OUT7 ITRIP Deglitch Option Summary

Deglitch Time ($t_{ITRIP_HS_DG}$)	OUT7_ITRIP_DG
48 μ s	00b
40 μ s	01b
32 μ s	10b
24 μ s	11b

The ITRIP deglitch timer starts when the OUT7 ITRIP blank time expires. The minimum OUT7 ITRIP ON time is the sum of blanking and deglitch times, and total period is determined by the OUT7 ITRIP frequency. The diagram below shows the ITRIP behavior for OUT7.

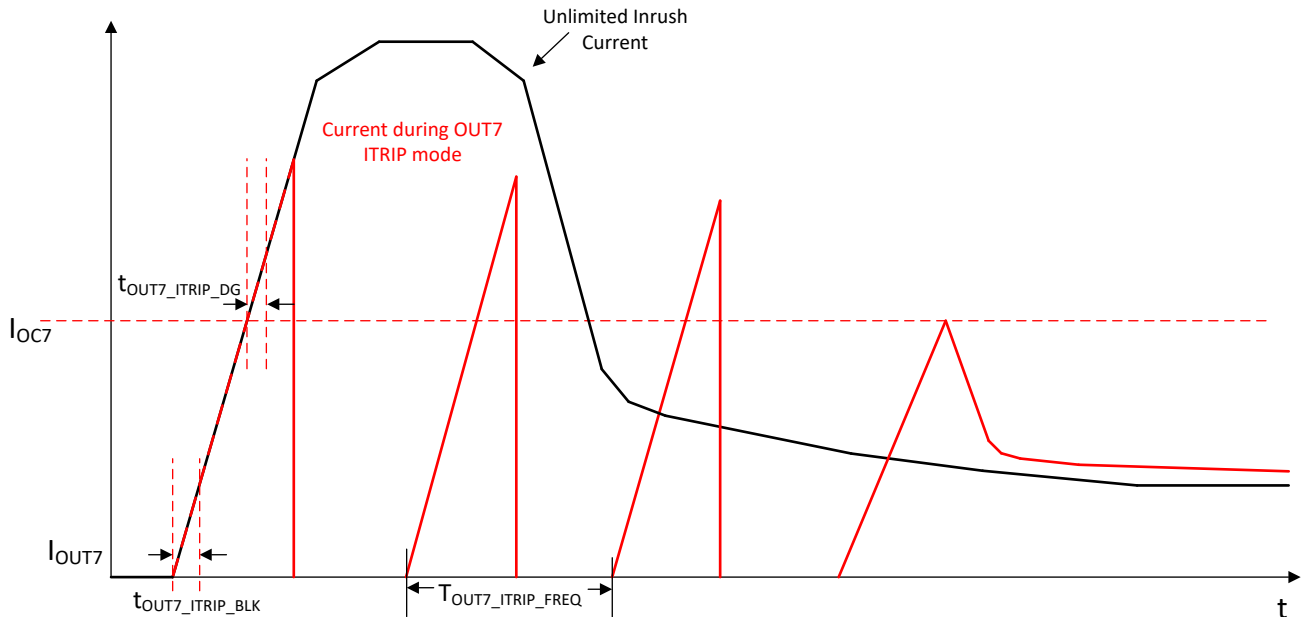


Figure 7-5. OUT7 ITRIP Behavior with Incandescent Bulb

The recovery activation sequence for OUT7 in HS ITRIP mode has three configurable timing parameters:

- $t_{OUT7_ITRIP_FREQ}$ ($1/T_{OUT7_ITRIP_FREQ}$)
- $t_{OUT7_ITRIP_BLK}$
- $t_{OUT7_ITRIP_DG}$

The blanking time $t_{OUT7_ITRIP_BLK}$ is default 40 μ s (typ), after which the overcurrent condition can be detected. $t_{OUT7_ITRIP_DG}$ is the time OUT7 remains on after overcurrent protection threshold is exceeded. $T_{OUT7_ITRIP_FREQ}$ is the time period of the ITRIP loop, inverse of $t_{OUT7_ITRIP_FREQ}$. These settings are configurable in register [HS_REG_CNFG1](#).

7.4.2.1.2.3 High-side Drivers - Parallel Outputs

The high-side drivers OUT8 through OUT12 can be connected in parallel combinations to support even higher current loads. For example, OUT8 and OUT9 can be connected in parallel as a 600m Ω driver effectively, or OUT9, OUT10, and OUT12 can be connected in parallel as a 400m Ω driver effectively.

However, there are limitations with this mode of operation:

- Internal PWM control does not work for parallel high-side drivers and must not be configured for this mode of operation.
- Constant current mode is not possible and must be disabled.
- Protection circuitry functions, but trip at different thresholds.

If operating in parallel, the high-side drivers must be configured for ON/OFF SPI register control or external PWM signal control through pin.

7.4.2.1.3 High-side Driver Protection Circuits

7.4.2.1.3.1 High-side Drivers Internal Diode

Each high-side driver has an internal diode from ground to the high-side OUTx node for ESD protection. If either of the following occurs, this diode can be subjected to high energy dissipation:

- Both a loss of ground connection and short to ground on a high-side output.
- There is an inductive load on the high-side output.

Only a limited amount of energy (<1mJ) can be dissipated by the internal ESD diodes during freewheeling. For inductive loads greater than 100μH, a connection to an external freewheeling diode between GND and the corresponding output is required

7.4.2.1.3.2 High-side Driver Overcurrent Protection

High-side drivers OUT7 through OUT12 overcurrent fault detection leads to shutting off of faulty output (latch).

The overcurrent threshold I_{OCx} for high-side drivers is configurable between high and low-current thresholds with bit [OUTX_OC_TH](#) in register [HS_OC_CNFG](#). The two options are 250 mA for low-current mode and 500 mA high-current mode. There is also a configurable deglitch time $t_{OCP_HS_DG}$ similar to the half-bridge drivers, which can be configured with bits [OUTX_OCP_DG](#) in register [HS_OCP_DG](#).

For OUT7, the current protection threshold bit is set with [OUT7_RDSON_MODE](#) bit in register [HS_OC_CNFG](#). The two options for OUT7 $R_{DS(on)}$ modes set the thresholds at 500 mA and 1.5 A (0b for high $R_{DS(on)}$ mode and 1b for low $R_{DS(on)}$ mode respectively). 1.5 A threshold is intended as an application limit when a lamp or bulb load is driven with OUT7, and the 500 mA is intended for LED loads.

However, to drive a load like lamp or bulb in application with OUT7, the overcurrent limit must be disabled with [OUT7_OCP_DIS](#) bit in register [HS_REG_CNFG1](#).

If the load current on any active output exceeds this configured current threshold for longer than $t_{OCP_HS_DG}$, the overcurrent [OUTx_OCP](#) and HS fault status bits are latched, and the corresponding output is shutoff. The bit remains set until the [CLR_FLT](#) bit has been set. The diagram below shows the overcurrent behavior for high-side drivers:

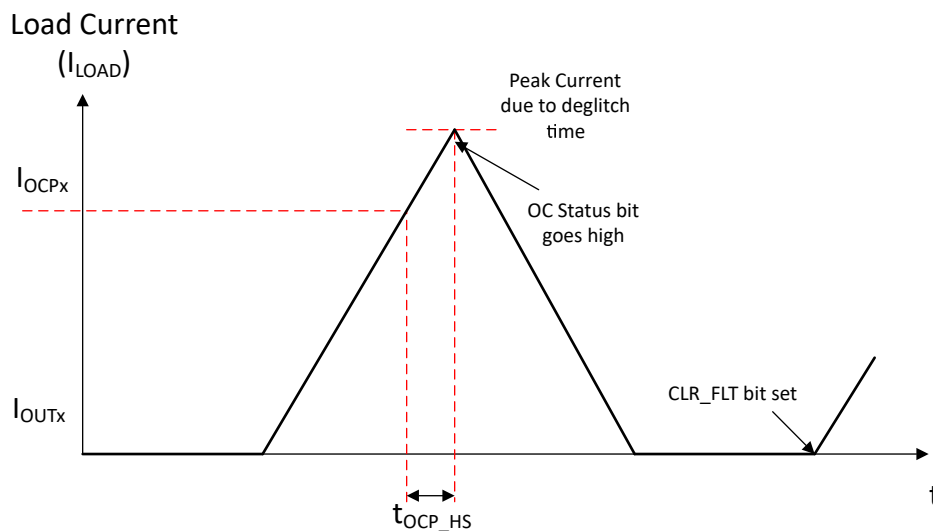


Figure 7-6. High-side Drivers Overcurrent Protection

7.4.2.1.3.3 High-side Driver Open Load Detection

The high-side drivers have open-load detection. Similar to the half-bridge drivers OLA detection scheme of the DRV800x-Q1, the high-side drivers open-load detection scheme sequences through each driver checking if the load current is below the open-load current threshold. The open-load current threshold I_{OLDx} is configurable between high- and low-current thresholds with bit **OUTX_OLA_TH** in register **HS_OL_CNFG**.

Open-load detection must be enabled with bit **OUTX_OLA_EN** in register **HS_OL_CNFG**.

If the load current I_{OUTx} is below the open-load threshold (I_{OLD_HS}) for $t > t_{OL_HS_OUT}$, then the corresponding high-side open load status bit **OUTx_OLA** is set in the status register. The driver detected with open-load is not switched off.

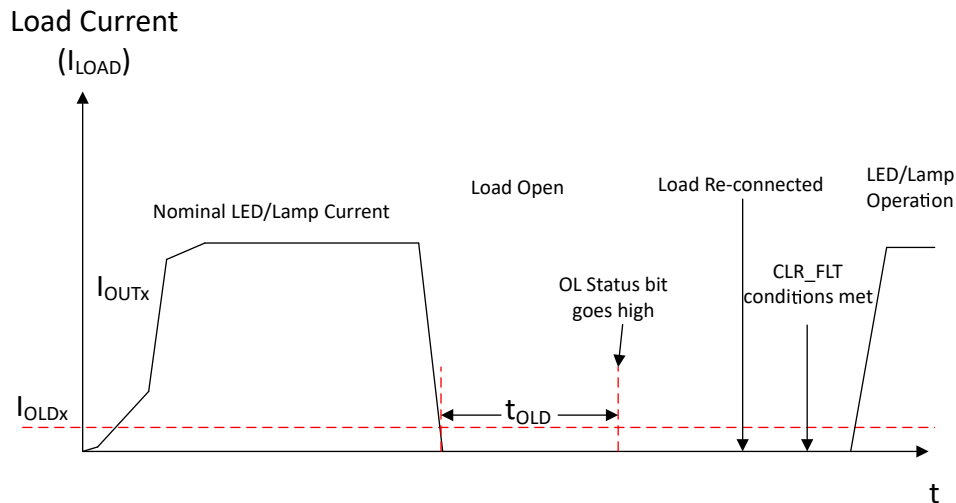


Figure 7-7. Open-Load Detection for High-side Drivers

The open-load detection test time for each high-side driver is 200 μ s. The timer does not start until the output is enabled. Once all enabled drivers have been cycled through, the detection circuit stops. The high-side driver OLA circuit requires a CLR_FLT to restart the open-load detection cycle.

The high-side driver must be ON for minimum 200 μ s for the OLA detection to complete. Otherwise, the device waits until the next PWM cycle. The OFF counter for the OLA detection starts when the high-side driver turns OFF and ends OLA detection if the driver is detected OFF for more than 10ms.

7.4.3 Electrochromic Glass Driver

Table 7-18. EC Driver Section Table of Contents

EC Driver Section	Link to Section
Back to Top of Feature Section	Section 7.4
EC Driver Control	Section 7.4.3.1
EC Driver Protection	Section 7.4.3.2

The device features an integrated electrochromic driver block that can be used to charge or discharge an electrochromic element of a mirror. The electrochromic driver block charges an external MOSFET to control the charging and discharge voltage of the element. The driver configuration operates with either high-side driver OUT11 as protected supply to the element or without OUT11 (independent OUT11 control).

7.4.3.1 Electrochromic Driver Control

Below is the block diagram for the electrochromic driver:

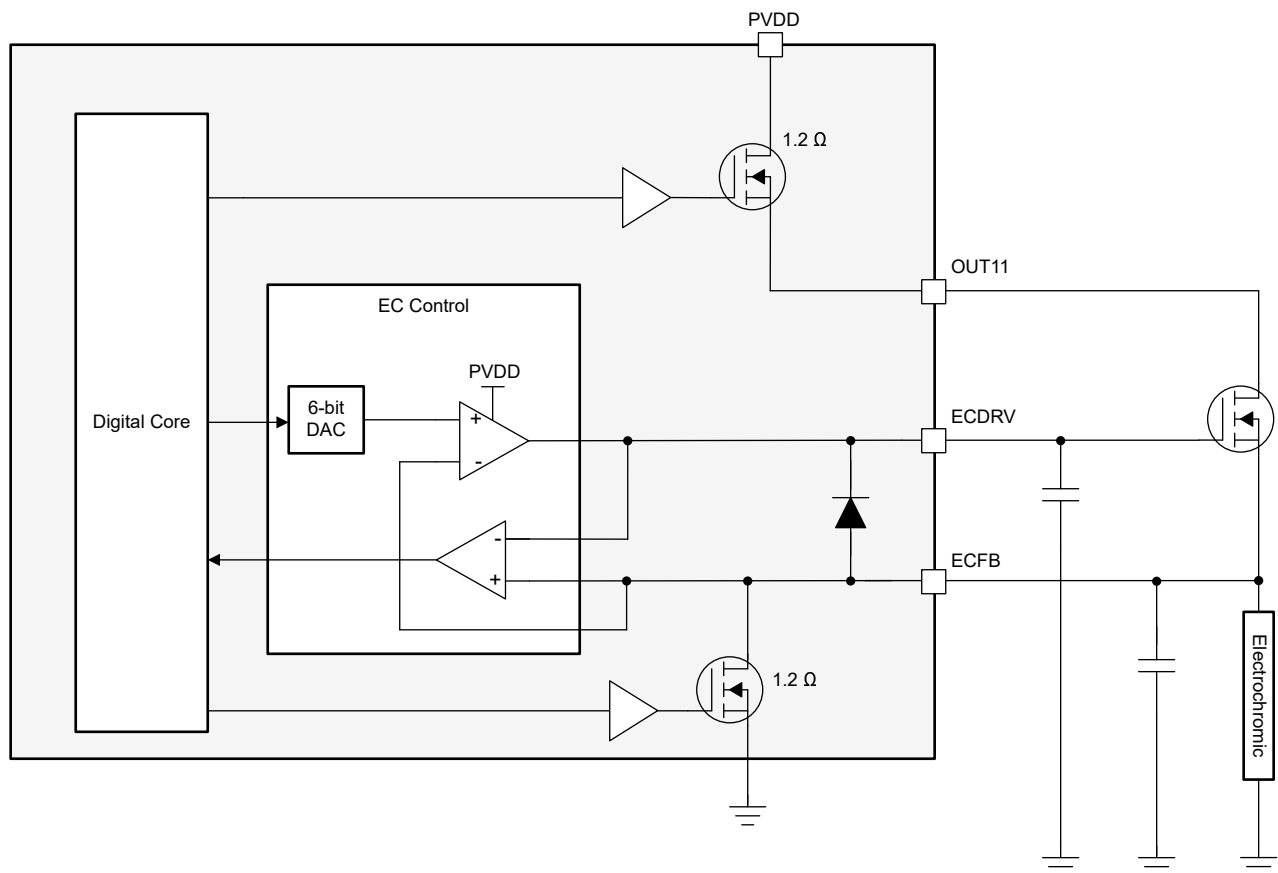


Figure 7-8. Electrochromic Driver Block Diagram - Default Configuration

Depending on the system implementation, the device electrochrome driver supports configuration where the drain of electrochrome high-side charge MOSFET can be supplied from either high-side driver OUT11, or directly from the supply voltage (PVDD). The EC control block can operate independently of the supply, with independent protection circuits in either configuration. This can be useful if an extra high-side driver is needed to drive another load. The main limitation in this configuration is that if the charge MOSFET fails short, the connection to supply cannot be shut off as when OUT11 is used as EC supply. A short and open-load condition can still be detected when EC supplied with PVDD directly (OUT11 is configured as independent).

OUT11 for EC supply: This configuration is set in register [HS_OC_CNFG](#), bit [OUT11_EC_MODE](#). By default, [OUT11_EC_MODE](#) = 1b, which is configured as the supply for EC drive as shown in the block diagram above. When in this configuration, bits [OUT11_CNFG](#) in register [HS_HEAT_OUT_CNFG](#) are ignored (ON/OFF, SPI/PWM). Both OUT11 and the 1.5Ω ECFB low-side discharge MOSFET have overcurrent and open load detection active during EC charge and discharge states, respectfully.

PVDD for EC supply, independent OUT11: To use OUT11 as an independent high-side driver (independent of EC control) to drive a separate load, where the drain of the EC charge MOSFET is connected directly to supply voltage, set [OUT11_EC_MODE](#) = 0b in register [HS_OC_CNFG](#). In this configuration, there is short to battery, short to ground, and open load detection on ECFB that can be independently enabled during EC charge state, replacing the diagnostics of OUT11. As before, the ECFB low-side discharge MOSFET protection circuits are active during EC discharge state. The diagram below shows this configuration:

To enable the EC driver: Set bits [EC_ON](#) and [EC_V_TAR](#) to the desired target voltage in register [HS_EC_HEAT_CTRL](#) to enable the EC driver control loop. Once these bits are set, EC driver control loop is enabled.

For EC element voltage control: Once the EC driver is enabled, the feedback loop of the driver is activated, and regulates ECFB pin voltage to the target voltage set in bits [EC_V_TAR](#) in register [HS_EC_HEAT_CTRL](#). The target voltage on ECFB pin is binary coded with a full-scale range of either 1.5V or 1.2V, depending if bit [ECFB_MAX](#) in register [EC_CNFG](#) is set to 1 or 0, respectively. [ECFB_MAX](#) = 0b is the default value (1.2V).

Whenever a new value for the EC voltage is set, there is a blanking time t_{BLK_ECFB} of 250μs for [ECFB_HI](#) or [ECFB_LO](#) status indication of ECFB once the control loop begins regulation to the new target value.

The device provides two discharge modes: fast discharge and PWM discharge.

Fast discharge of the EC element: To fully discharge the EC element with fast discharge, the target output voltage [EC_V_TAR](#) must be set to '0b', and bits [ECFB_LS_EN](#) and [EC_ON](#) must be set to '1b'. When these three conditions are met, the voltage at pin ECFB is discharged by pulling the internal 1.5Ω low-side MOSFET on ECFB pin to ground.

1. Configure [ECFB_LS_PWM](#) = 0b in register [EC_CNFG](#)
2. Set bits [ECFB_LS_EN](#) = 1b, [EC_ON](#) = 1b and [EC_V_TAR](#) = 0b in register [HS_EC_HEAT_CTRL](#).
3. ECFB LS MOSFET is enabled and performs fast discharge of EC mirror.

PWM discharge of the EC element: The steps below outline the PWM discharge cycle of electrochrome driver:

1. Configure [ECFB_LS_PWM](#) = 1b in register [EC_CNFG](#)
2. Set bits [ECFB_LS_EN](#) = 1b, [EC_ON](#) = 1b, [EC_V_TAR](#) = 0b in register [HS_EC_HEAT_CTRL](#).
3. If the regulation loop detects V_{ECDRV} is less than V_{ECFB} for longer than $t_{RECHARGE}$ or 3ms, the ECDRV regulator is switched off and the LS MOSFET on ECFB is activated for approximately 300ms ($t_{DISCHARGE}$). During this discharge, the ECDRV output is pulled low to prevent shoot-thru currents.
4. At the end of the discharge pulse $t_{DISCHARGE}$, the discharge MOSFET is switched off and the regulation loop is activated again with the new lower value. The regulation loop goes back to step 2, and out of regulation is again observed ($V_{ECDRV} - V_{ECFB}$).

The diagram below shows the PWM discharge cycle of the electrochrome driver:

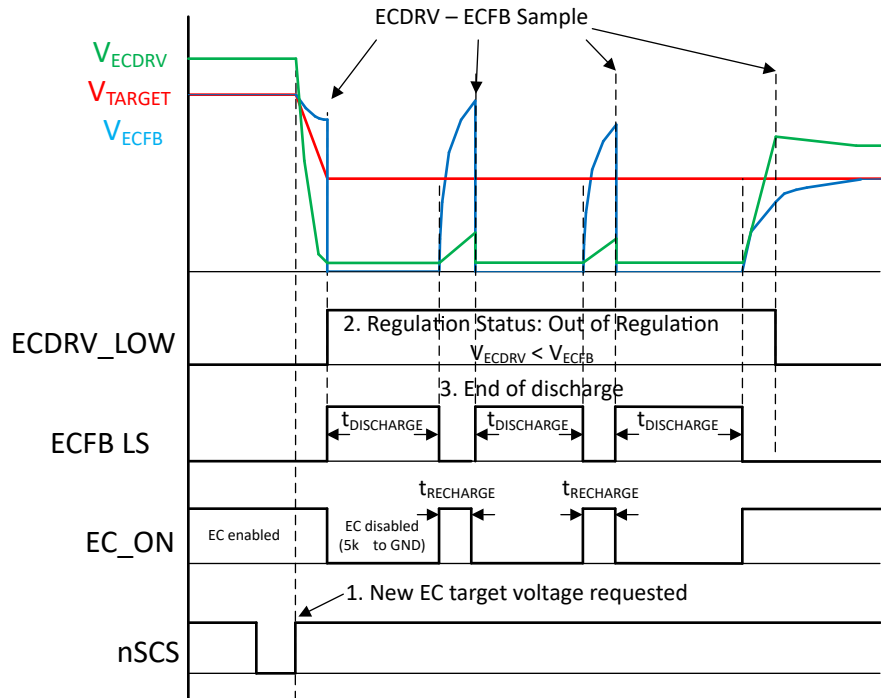


Figure 7-9. Electrochrome Discharge with PWM

The status of the voltage control loop is reported through SPI, and TI recommends to observe the report to determine the EC charge and discharge control timing. If the voltage at pin ECFB is higher than the target value, then bit **ECFB_HI** is set. If the voltage at pin ECFB is lower than the target value, **ECFB_LO** is set. Both ECFB status bits **ECFB_HI** and **ECFB_LO** are valid if the bits are stable for at least the filter time t_{FT_ECFB} . The bits are not latched, and are not assigned as global faults.

Exit discharge mode: To exit discharge mode, **ECFB_LS_EN** must be deasserted. If **ECFB_LS_EN** bit is left high when a new target voltage is programmed, the control loop does not respond because the internal logic prevents both OUT11 and ECFB LS from being simultaneously on.

A capacitor of at least 4.7nF has to be added to pin ECDRV, and 220nF capacitor between ECFB and ground to increase control loop stability. For noise immunity reasons, TI recommends to place the loop capacitors as close as possible to the respective pins.

If the EC driver is not used, connect ECFB pin to ground.

7.4.3.2 Electrochromic Driver Protection

The electrochromic driver block has multiple protection and detection circuits for both charge and discharge states. There are the comparator-based detection circuits, protection circuits of OUT11 which are active during EC charge state (when configured with OUT11 as supply), and protection circuits on ECFB low-side discharge MOSFET.

EC supplied by OUT11: When the electrochrome drive is configured to be supplied by integrated high-side driver OUT11, the same protection and diagnostic functions as the other high-side drivers are available (for example: during an overcurrent detection, the control loop is switched off). These high-side driver protections are active when the electrochrome is in the charge state (voltage ramp up). When in OUT11 EC mode (**OUT11_EC_MODE** = 1b), OUT11 cannot be controlled in PWM mode.

Fault on OUT11 during EC charge: In case of an overtemperature shutdown fault (zone 3 or 4) or overcurrent fault on OUT11 while **EC_ON** = 1b (EC control enabled):

- OUT11 is shut off (status register set)
- DAC is reset (**EC_V_TAR** set to '00000')

- ECDRV pin is pulled to ground
- [EC_ON](#) remains '1'
- [ECFB_LS_EN](#) remains as programmed

To restart EC control after OUT11 failure, the controller must read and clear the corresponding fault, and write the desired value to bits [EC_V_TAR](#) in register [HS_EC_HEAT_CTRL](#).

If an open load is detected on OUT11 during EC charge, the OUT11_OLA bit in register HS_STAT is set.

Discharge overcurrent protection: If the load current into the ECFB pin LS MOSFET during discharge exceeds the overcurrent threshold I_{OC_ECFB} for longer than $t_{DG_OC_ECFB}$, then the LS MOSFET is either Hi-Z (latch) or enters fixed-frequency regulation mode based on OUT7 ITRIP settings. The overcurrent status bit [ECFB_OC](#) is set, and [EC_HEAT](#) is set. Overcurrent fault response is configurable with [EC_FLT_MODE](#) bit in register [EC_CNFG](#). The ITRIP settings are shared with [OUT7 ITRIP settings](#).

Table 7-19. Discharge Overcurrent Protection

EC_FLT_MODE	Fault Response
0b	Latch (Hi-Z)
1b	ITRIP (OUT7 settings)

Discharge open load detection: While discharging the EC, open-load can also be detected. Bit [EC_OLEN](#) in register [EC_CNFG](#) must be set. If the load current on ECFB is below $I_{OL_ECFB_LS}$ for longer than $t_{DG_OL_ECFB_LS}$, then the open load status bit [ECFB_OL](#) is set, and [WARN](#) bit is set in register [IC_STAT1](#).

For EC direct PVDD supply configuration, there are three comparator-based detection circuits that can be used when EC regulation is active in place of relying on the OUT11 protection and detection circuits. These include:

- Short to Battery detection on ECFB (overvoltage)
- Short to Ground detection on ECFB (undervoltage)
- Open-load detection on ECFB

EC supply direct to PVDD: When the EC block is supplied directly to PVDD, short to battery, short to ground, and open load detection circuits can be independently enabled with bits [ECFB_OV_MODE](#), [ECFB_UV_MODE](#), and [ECDRV_OL_EN](#) in register [EC_CNFG](#). These detection circuits can be enabled regardless of EC supply configuration if extra diagnostics are desired. However, if the circuits are not desired, then TI recommends to disable the circuits in the register.

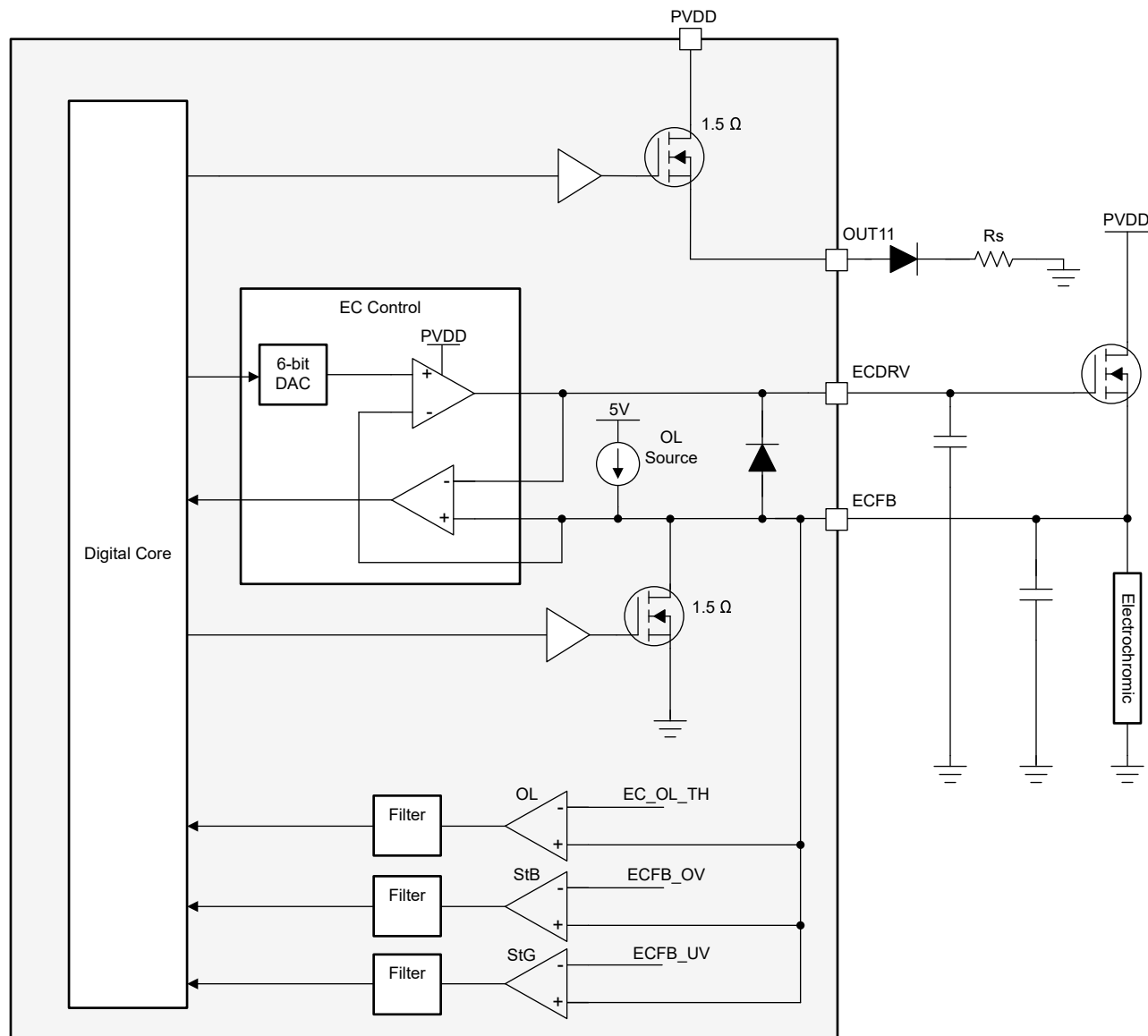


Figure 7-10. Electrochrome with Direct PVDD Supply (OUT11 Independent)

Short to battery/OV detection: ECFB overvoltage or short to battery is detected when ECFB voltage exceeds $PVDD - 1V$, or threshold V_{ECFB_OV} , for longer than the deglitch time $t_{ECFB_OV_DG}$. Bit [ECFB_OV_MODE](#) determines the driver ECFB overvoltage fault response. The EC overvoltage deglitch time is configured with bit [ECFB_OV_DG](#) in register [EC_CNFG](#).

For over voltage fault response control, bit [ECFB_OV_MODE](#) can be configured in register [EC_CNFG](#). If [ECFB_OV_MODE](#) = 00b, then no action is taken during this fault. For [ECFB_OV_MODE](#) = 10b, when ECFB voltage exceeds V_{ECFB_OV} for longer than programmed deglitch time $t_{ECFB_OV_DG}$, then the [ECFB_OV](#) bit is set in [EC_HEAT_ITRIP_STAT](#) register, and [EC_HEAT](#) fault bit is set in register [IC_STAT1](#). For [ECFB_OV_MODE](#) = 10b, when OV on ECFB occurs, the [ECDRV](#) pin is pulled down, and the ECFB LS FET is Hi-Z. Faults are reported in the same registers as for when [ECFB_OV_MODE](#) = 01b. The fault responses and bit values are summarized in the table below:

Table 7-20. Electrochrome Overvoltage Fault Response

ECFB_OV_MODE	Fault Response
00b	No action
01b	Report fault in register
10b	Pulldown ECDRV and ECFB LS FET, report fault in register

Table 7-21. EC Overvoltage Deglitch Times

ECFB_OV_DG	Deglitch Time
00b	20 μs
01b	50 μs
10b	100 μs
11b	200 μs

Short to ground/UV detection: ECFB undervoltage or short to ground is detected when ECFB voltage is detected below the programmed threshold $V_{ECFB_UV_TH}$ for longer than the programmed deglitch time $t_{ECFB_UV_DG}$. Bits [ECFB_UV_TH](#) and [ECFB_UV_DG](#) are set in register [EC_CNFG](#).

Table 7-22. Electrochrome Undervoltage Thresholds

ECFB_UV_TH	Undervoltage Threshold
0b	100 mV
1b	200 mV

Note

When the short to ground/undervoltage detection is enabled, if the ECFB target voltage is set below the programmed threshold, which is either the lowest 4 or 8 bits of resolution depending on [ECFB_UV_TH](#), a short to ground/undervoltage is detected. If short to ground/undervoltage detection is desired, avoid these target voltage values to prevent misdiagnosis of a short to ground/undervoltage condition.

For undervoltage fault response control, bit [ECFB_UV_MODE](#) can be configured in register [EC_CNFG](#). If [ECFB_UV_MODE](#) = 00b, then no action is taken when ECFB voltage falls below [ECFB_UV](#). For [ECFB_UV_MODE](#) = 10b, then the [ECFB_UV](#) bit is set in [EC_HEAT_ITRIP_STAT](#) register, and [EC_HEAT](#) fault bit is set in register [IC_STAT1](#). For [ECFB_UV_MODE](#) = 10b, when UV on ECFB occurs, the ECDRV pin is pulled down, and the ECFB LS FET is Hi-Z. Faults are reported in the same registers as for when [ECFB_UV_MODE](#) = 01b. The fault responses and bit values are summarized in the table below:

Table 7-23. Electrochrome Undervoltage Fault Response

ECFB_UV_MODE	Fault Response
00b	No action
01b	Report fault in register
10b	Pulldown ECDRV and ECFB LS FET, report fault in register

Table 7-24. EC Undervoltage Deglitch Times

ECFB_UV_DG	Deglitch Time
00b	20 μ s
01b	50 μ s
10b	100 μ s
11b	200 μ s

PVDD supplied EC Open-load detection: If the EC block is not configured to be supplied with OUT11, a separate EC open-load detection circuit can be enabled with bit [ECDRV_OL_EN](#) in register [EC_CNFG](#). When enabled, a current source injects a small current into the ECFB node, and the ECFB voltage is compared with the open-load threshold voltage. If the open-load threshold is exceeded, an open load condition is detected and the [ECFB_OL](#) bit is set. The truth table below shows possible values for both open load and short to battery detection status:

Table 7-25. Open Load and Over Voltage Detection Truth Table

ECFB_OL	ECFB_OV	Status
1b	1b	Short to battery/overvoltage
1b	0b	Open-load
0b	1b	Not possible
0b	0b	Normal operation

7.4.4 Half-bridge Drivers

Table 7-26. Half-bridge Section Table of Contents

Half-bridge Section	Link to Section
Back to Top of Feature Section	Section 7.4
Half-bridge Control	Section 7.4.4.1
Half-bridge Regulation	Section 7.4.4.2
Half-bridge Protection	Half-bridge Protection and Diagnostics

The device integrates six total half-bridge high-side and low-side FETs, supporting bidirectional drive for up to five motors; two 1.5-Ω half-bridges, two 300-Ω half-bridges, and two 100-Ω half-bridges. All of these drivers can be controlled with SPI register, PWM signal that can be sourced from the PWM1 pin or IPROPI/PWM2 pin. Each driver also has configurable current regulation feature called ITRIP. Half-bridge protection circuits include overcurrent protection, off-state and active open-load diagnostics.

The diagrams below show common configurations for the integrated half-bridges to support up to five mirror and lock motors, and all mirror motors:

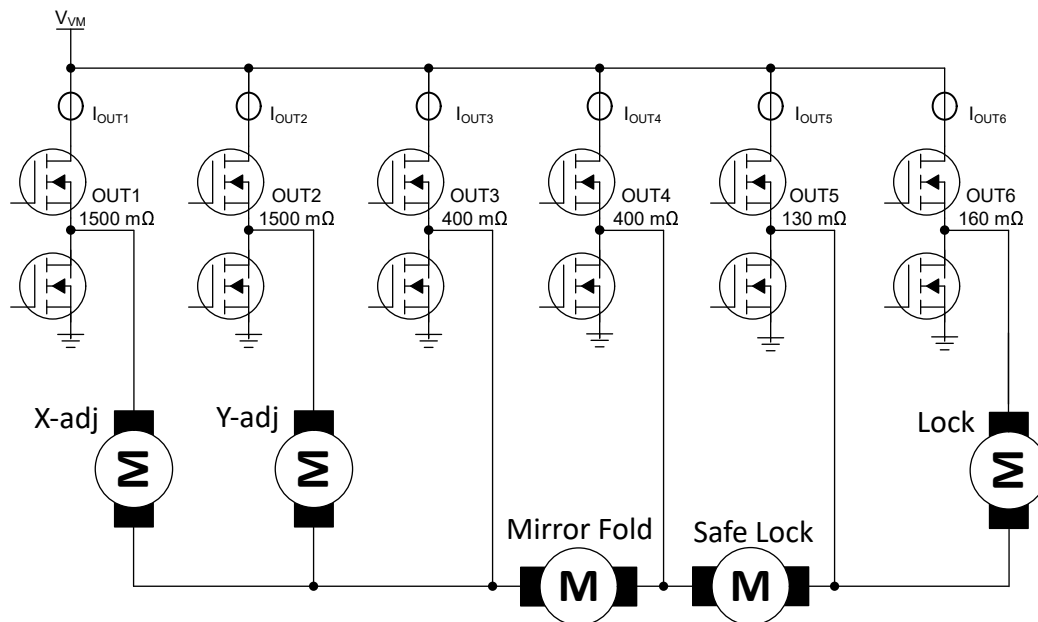


Figure 7-11. Half-bridge Configuration for up to Five Motors (Mirror and Lock)

The diagram below shows a configuration for mirror only loads:

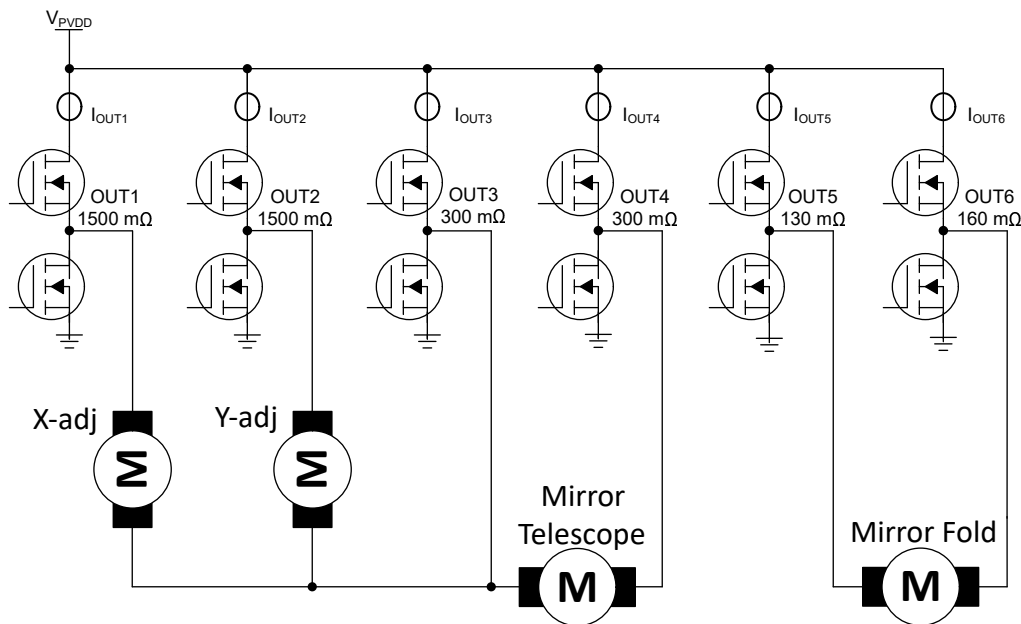


Figure 7-12. Half-bridge Configuration for up to Four Motors (Mirrors only)

7.4.4.1 Half-bridge Control

The half-bridge drivers can be controlled in two modes to support control schemes with either PWM input pins or SPI register control. The half-bridge drivers also have configuration registers ([HB_OUT_CNFG1](#) and [HB_OUT_CNFG2](#)) to enable half-bridge control and to set up control mode (PWM or SPI).

The half-bridges can be configured for control by input signal from either PWM1 or /PWM2 pins. The signal to PWM1 pin can be multiplexed internally to half-bridges, high-side drivers, and heater driver. PWM control from PWM2 pin is only available for half-bridges.

The configuration table is shown below. Note that OUT5 and OUT6 are configured in [HB_OUT_CNFG2](#) and OUT1 through OUT4 are configured in [HB_OUT_CNFG1](#):

Table 7-27. OUTX_CNFG Half-bridge Configuration

OUTX_CNFG[2]	OUTX_CNFG[1]	OUTX_CNFG[0]	OUTx	HS ON	LS ON
0	0	0	OFF	OFF	OFF
0	0	1	SPI Register Control	OUTX_CTRL	OUTX_CTRL
0	1	0	PWM 1 Complementary Control	~PWM1	PWM1
0	1	1	PWM 1 LS Control	OFF	PWM1
1	0	0	PWM 1 HS Control	PWM1	OFF
1	0	1	PWM 2 Complementary Control	~IPROPI/PWM2	IPROPI/PWM2
1	1	0	PWM 2 LS Control	OFF	IPROPI/PWM2
1	1	1	PWM 2 HS Control	IPROPI/PWM2	OFF

When the half-bridges are configured for SPI register control ([OUTx_CNFG](#) = 01b), the half-bridges high- and low-side MOSFETs can be individually controlled in register [HB_CTRL](#) with bits [OUTx_CTRL](#). The control truth table for the half-bridge outputs is shown below:

Table 7-28. Half-bridge Driver Controls

OUTx_CTRL (OUT1-6) bits	Configuration	Description
00	OFF	Half-bridge control OFF
01	HS ON	High-side MOSFET ON
10	LS ON	Low-side MOSFET ON
11	RSVD	Reserved.

The half-bridge control mode can be changed anytime SPI communication is available by writing to the bits. This change is immediately reflected.

When the half-bridges are configured for PWM operation ([OUTx_CNFG](#) = 01Xb or 10Xb), the inputs can accept static or pulse-width modulated (PWM) voltage signals for either 100% or PWM drive modes. The default behavior for half-bridges during off-state of PWM signal is to Hi-Z the output.

The device automatically generates the dead-time needed during transitioning between the high-side and low-side FET on the switching half-bridge. This timing is based on internal FET gate-source voltage. No external timing is required. This scheme provides minimum dead time while preventing shoot-through current.

7.4.4.2 Half-Bridge ITRIP Regulation

The device half-bridges have optional fixed-frequency load current regulation called ITRIP. This is done by comparing the active output current against configured current thresholds determined by [OUTX_ITRIP_LVL](#). OUT1-2 has two possible ITRIP current thresholds, and OUT3-6 also have three current threshold options. ITRIP thresholds, enables, and timing settings are set individually for each half-bridge in the [HB_ITRIP_CONFIG](#), [HB_ITRIP_FREQ](#) and [HB_ITRIP_DG](#).

As this device has multiple integrated drivers which are enabled at any given time, there is freewheeling configuration intended to reduce power dissipation during ITRIP half-bridge regulation. Power dissipation is lower with synchronous rectification (MOSFETs) compared with asynchronous rectification (diodes). The half-bridge freewheeling is configurable between non- and synchronous rectification (active and passive freewheeling). The freewheeling settings are shared between half-bridge pairs. The synchronous rectification for half-bridges during ITRIP regulation is enabled by setting bits [NSR_OUTX_DIS](#) in configuration register [HB_OUT_CNFG1](#).

ITRIP detection is done on both high- and low-side MOSFETs of each half-bridge. ITRIP is dynamically blanked by internal overcurrent protection circuitry.

The configurable ITRIP timing parameters are frequency and deglitch. The tables below summarize the ITRIP configuration options.

Table 7-29. Half-bridge ITRIP Synchronous Rectification Settings

NSR_OUTX_DIS	ITRIP Half-bridge Off-time Response
0b	Hi-Z
1b	complementary MOSFET ON

Table 7-30. ITRIP Current Thresholds for Half-bridges

Half-bridges	Typ ITRIP Current Thresholds	OUTX_ITRIP_LVL
OUT6	6.25A	10b
	5.5A	01b
	2.25A	00b
OUT5	7.5A	11b
	6.5A	01b
	2.75A	00b

Table 7-30. ITRIP Current Thresholds for Half-bridges (continued)

Half-bridges	Typ ITRIP Current Thresholds	OUTX_ITRIP_LVL
OUT3 & OUT4	3.5A	10b
	2.5A	01b
	1.25A	00b
OUT1 & OUT2	0.875A	1b
	0.7A	0b

Table 7-31. ITRIP Timing - Deglitch Options

Deglitch Time	OUTX_ITRIP_DG
2μs	00b
5μs	01b
10μs	10b
20μs	11b

Table 7-32. ITRIP Timing - Frequency Options

ITRIP Frequency	OUTX_ITRIP_FREQ
20kHz	00b
10kHz	01b
5kHz	10b
2.5kHz	11b

Note

If 20kHz ITRIP frequency is desired, the fastest deglitch time is recommended (2μs).

ITRIP regulation follows these steps:

- The low- or high-side of a half-bridge is enabled. The first ITRIP clock edge occurs when half-bridge enabled.
- If ITRIP limit is exceeded on either low- or high-side, the device waits for longer than deglitch time $t_{DG_ITRIP_HB}$.
- If ITRIP limit is still exceeded after the deglitch time, then either the half-bridge enters the Hi-Z or turns on the opposite MOSFET for the remainder of the ITRIP cycle, depending on [NSR_OUTX_DIS](#) bit setting. [ITRIP](#) status bit is set, and the regulation loop restarts.
- If [NSR_OUTX_DIS](#) = 1b (synchronous rectification enabled), the current through the enabled MOSFET is monitored for current reversal. If current reversal is detected, the half-bridge output is Hi-Z for the remainder of the ITRIP cycle.

The synchronous rectification or freewheeling feature is enabled by setting bits [NSR_OUTX_DIS](#) in configuration register [HB_OUT_CNFG1](#). When [NSR_OUTX_DIS](#) = 0b, if ITRIP occurs on either MOSFET, the half-bridge goes Hi-Z. If [NSR_OUTX_DIS](#) = 1b, if ITRIP occurs on either MOSFET, the opposite MOSFET is enabled.

For example, [NSR_OUTX_DIS](#) = 1b and [OUTX_CNFG](#) = 100b or 010b. If the PWM input sets HS MOSFET ON, and ITRIP is reached on HS MOSFET, the LS MOSFET turns on for the remainder of the ITRIP cycle. The HS MOSFET is turned ON at the end of the cycle. If the PWM input changes within the ITRIP period, the ITRIP counter is reset and ITRIP regulation is active while the LS MOSFET is ON.

If synchronous rectification is enabled and MOSFET turns on when ITRIP occurs, current is monitored for a current reversal, or zero-crossing detection. There is zero-crossing detection on both high-side and low-side MOSFETs. If the detected load current reaches 0A during ITRIP regulation for longer than the deglitch time,

then the half-bridge output goes Hi-Z for the remainder of the ITRIP cycle. The zero-crossing deglitch time is the same ITRIP deglitch time.

The diagram below shows the ITRIP behavior for a half-bridge:

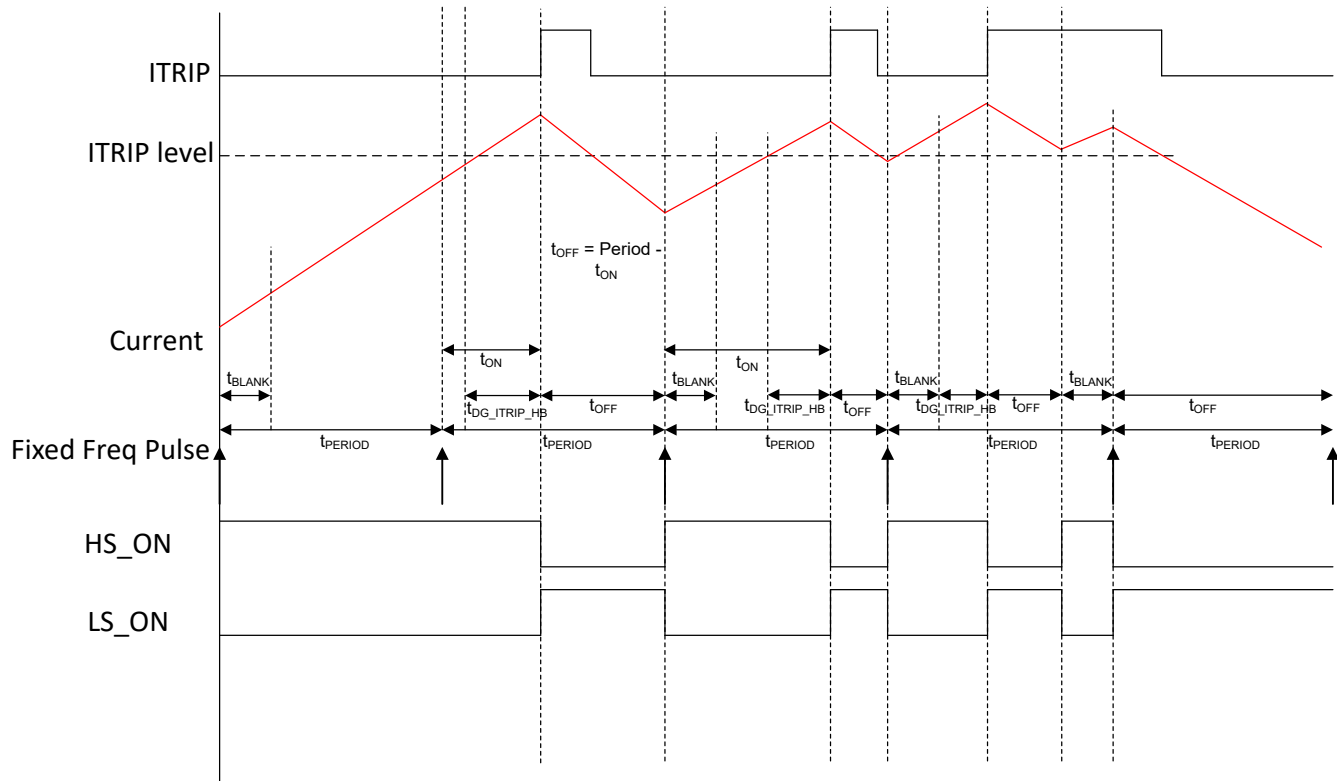


Figure 7-13. Fixed Frequency ITRIP Current Regulation for Half-bridges

The ITRIP setting can be changed at any time when SPI communication is available by writing to the [OUTX_ITRIP_LVL](#) bits. The change is immediately reflected in device behavior.

If a half-bridge is configured for PWM control and ITRIP, when ITRIP is reached, the behavior is the same as for SPI register control, but the input now comes from the configured PWM pin.

7.4.4.3 Half-bridge Protection and Diagnostics

The half-bridge drivers are protected against overcurrent. The device also offers on-state and off-state load monitoring. Fault signaling is done through register HB_STATX.

7.4.4.3.1 Half-Bridge Off-State Diagnostics (OLP)

The user can determine the impedance on a pair of half-bridges using off-state diagnostics while the half-bridges are disabled in register [HB_OUT_CNFGx](#). This diagnostic passively detects the following fault conditions:

- Output short to VM or GND < 1000Ω
- Open load > 1.5KΩ for high-side load, VM = 13.5V

Note

This diagnostic can NOT detect a **load short**. However, the user can deduce this logically if an overcurrent fault (OCP) occurs when an output is actively driven, but OLP diagnostics do not report any fault in the when the output is disabled. Occurrence of both OCP when an output is actively drive and OLP when the output is disabled IMP a terminal short (short on selected output node).

- The user can configure the following combinations

- Internal pullup resistor (R_{OLP_PU}) on OUTx
- Internal pulldown resistor (R_{OLP_PD}) on OUTx
- Comparator reference level
- This combination is determined by the **HB_OLP_CNFG** bits in the **HB_OL_CNFG1** register.
- The half-bridge pairs to be diagnosed are determined by the **HB_OLP_SEL** bits in the **HB_OL_CNFG1** register.
- The off-state diagnostics comparator output is available on **HB_OLP_STAT** bit in **HB_STAT2** register. The output is not latched.
- The user is expected to toggle through all the combinations and record the status bit output after the output is settled.
- Based on the input combinations and status register, the user can determine if there is a fault on the output.

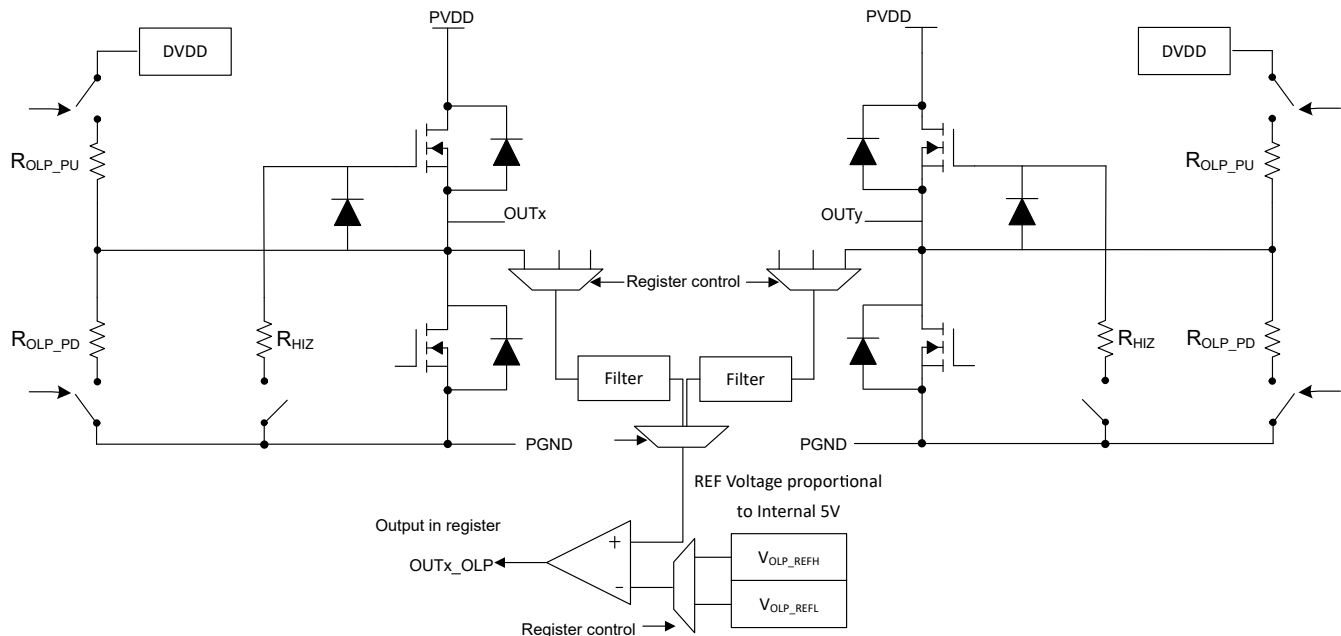


Figure 7-14. Off-State (Passive) Diagnostics

The following output, pulldown/pullup and VREF combinations are shown below:

Table 7-33. Off-state Output Pullup/Pulldown and VREF Options

HB_OLP_CNFG	Description
00b	OLP Off
01b	Output X Pullup enabled, Output Y pulldown enabled, Output Y selected, VREF Low
10b	Output X Pullup enabled, Output Y pulldown enabled, Output X selected, VREF High
11b	Output X Pulldown enabled, Output Y pullup enabled, Output Y selected, VREF Low

The OLP combinations and truth table for a no fault scenario vs. fault scenario for a low-side load is shown in [Table 7-34](#). For the diagnostics to be active and valid, all half-bridge configurations in bits **OUTx_CNFG** in registers **HB_OUT_CNFGx** must be zero (disabled).

Table 7-34. Off-State Diagnostics Control Table

User Inputs		OLP Set-Up				HB_OLP_STAT			
HB_OLP_C NFG	nSLEEP	OUTX	OUTY	CMP REF	Output Selected	Normal	Open	Short	VM Short
01b	1	ROL_PU	ROL_PD	VOLP_REFL	OUTY	1b	0b	0b	1b
10b	1	ROL_PU	ROL_PD	VOLP_REFH	OUTX	0b	1b	0b	1b
11b	1	ROL_PD	ROL_PU	VOLP_REFL	OUTY	1b	1b	0b	1b

The following half-bridge pair off-state combinations and selection values are shown below.

Note

If any half-bridge is enabled, then all half-bridge OLP bits are automatically disabled (0b).

Table 7-35. OUTx & OUTy Configurations

HB_OLP_SEL	OUTX & OUTY Pairs Selected
0000b	No output
0001b	OUT1 & OUT2
0010b	OUT1 & OUT3
0011b	OUT1 & OUT4
0100b	OUT1 & OUT5
0101b	OUT1 & OUT6
0110b	OUT2 & OUT3
0111b	OUT2 & OUT4
1000b	OUT2 & OUT5
1001b	OUT2 & OUT6
1010b	OUT3 & OUT4
1011b	OUT3 & OUT5
1100b	OUT3 & OUT6
1101b	OUT4 & OUT5
1110b	OUT4 & OUT6
1111b	OUT5 & OUT6

7.4.4.3.2 Half-Bridge Active Open Load Detection (OLA)

When the device is active and waiting for drive commands (nSLEEP is HI), there is an open-load detection loop for half-bridges OUT1 - OUT6. The detection scheme sequentially checks the open-load status for each high- and low-side of each half-bridge output and reports the status in bit **OUTx_OLA** in register **HB_STAT2** and **WARN** bit in register **IC_STAT1**.

From standby or sleep mode, starting with OUT1, the control loop begins to check open-load status. The open-load detection threshold is configurable for either 32 or 128 cycles with bit **OUTx_OLA_TH** in register **HB_OL_CNFG2**. If an output is driven with EN/DIS only (no PWM switching) then the open-load detection time is 5 ms.

If open-load is detected for longer than the cycle count threshold or before timeout occurs, then bit **OUTx_OLA** is reported. If no open-load is detected after 32 or 128 cycles, then the loop moves to the next half-bridge. The loop continues checking each output through OUT6, then goes back to OUT1 to restart the OLA loop. For the open-load check to be valid, the half-bridge open-load detection must be enabled (**OUTx_OLA** = 1b) and the output must be enabled (**OUTx_CNFG** = X1b). The diagram below shows the OLA scheme:

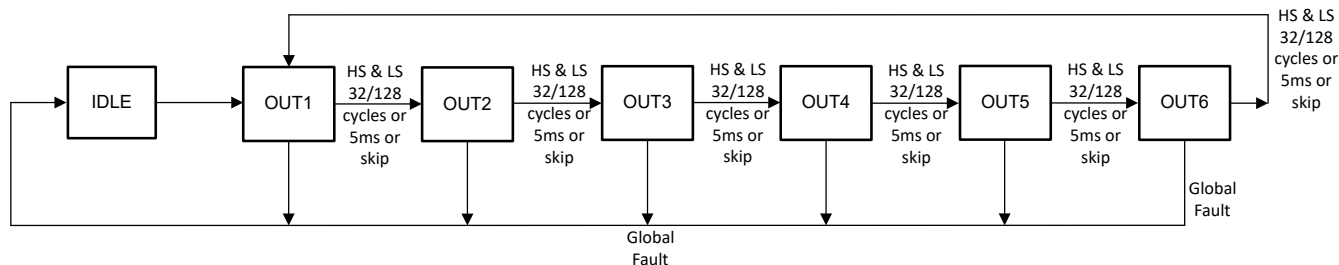


Figure 7-15. Half-bridge Open-Load Active Detection

Any given half-bridge is skipped if any of the following three conditions are met:

1. OUTx is disabled ([OUTx_CNFG](#) = 00b).
2. Open-load detect is not enabled ([OUTx_OLA](#) = 0b) for the half-bridge.
3. OUTx is OFF for more than 5ms
4. OLA has already been detected and flagged, or other fault condition on OUTx (overcurrent, over temperature)

With all half-bridge OUTx enabled without PWM, the total loop time can take up to 46 ms to cycle through all half-bridges. When a half-bridge is driven individually or sequentially, the loop detects open load within 5 ms or faster (depending on EN or PWM control). If a half-bridge is driven with a low frequency external PWM signal, the OFF time of the output can exceed the open-load detection window of 5 ms, and so the half-bridge is skipped.

7.4.4.3.3 Half-Bridge Overcurrent Protection

When a half-bridge is active, an analog current protection circuit on each MOSFET shuts off the MOSFET during hard short-circuit events. If the output current exceeds the overcurrent threshold I_{OCP_OUTX} for longer than $t_{DG_OCP_HB}$, an overcurrent fault is detected. The corresponding output is Hi-Z (latch behavior) and the fault is latched in register ([HB_STAT1](#)).

For overcurrent deglitch time $t_{DG_OCP_HB}$ of half-bridge drivers, there are four overcurrent deglitch options summarized in the table below.

Table 7-36. Half-bridge Overcurrent Deglitch

Deglitch time	OUTX_OCP_DG	Voltage Limitation
6 μ s	00b	Forced option if $V_{PVDD} > 28$ V
10 μ s	01b	< 28 V
20 μ s	10b	< 28 V
60 μ s	11b	< 20 V

To re-activate the driver, the fault must first be cleared in register by the MCU by reading the status register. The diagram below shows the overcurrent behavior of a half-bridge:

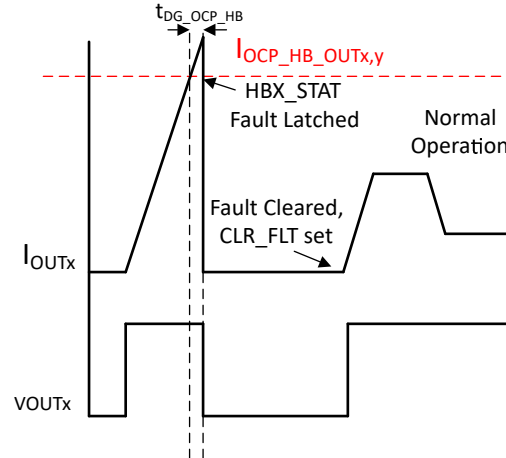


Figure 7-16. Overcurrent Behavior for Half-bridges

7.4.5 Sense Output (IPROPI)

The device features an output for current sensing, voltage node monitoring, and die temperature on the IPROPI pin. This information can be used for status or regulation of loads (on OUTx), check die temperature, or to provide local motor voltage. These integrated features eliminate the need for multiple external sense resistors or sense circuitry, reducing system size, cost and complexity.

The load currents are sensed by using a shunt-less high-side current mirror topology. The output is a fixed ratio of the instantaneous current of the enabled driver (OUTx). The signal at the output IPROPI is blanked for t_{IPROPI_BLK} after switching on the driver to allow time for the circuitry to settle. Bit IPROPI_SEL defines which of the outputs is multiplexed to the IPROPI pin, the control values shown in the table below:

Table 7-37. IPROPI_SEL Options

IPROPI_SEL	Output
00000b	No output
00001b	OUT1 Current Sense
00010b	OUT2 Current Sense
00011b	OUT3 Current Sense
00100b	OUT4 Current Sense
00101b	OUT5 Current Sense
00110b	OUT6 Current Sense
00111b	OUT7 Current Sense
01000b	OUT8 Current Sense
01001b	OUT9 Current Sense
01010b	OUT10 Current Sense
01011b	OUT11 Current Sense
01100b	OUT12 Current Sense
01101b	RSVD
01110b	RSVD
01111b	RSVD
10000b	PVDD Output voltage
10001b	Thermal Cluster 1
10010	Thermal Cluster 2
10011	Thermal Cluster 3
10100	Thermal Cluster 4

The IPROPI pin is a multipurpose pin which can also be used as second PWM pin control input option for half-bridges, therefore the IPROPI/PWM2 pin mode is controlled with bit IPROPI_MODE in register IC_CTRL.

The diagram below shows the simple block diagram for the selectable IPROPI output:

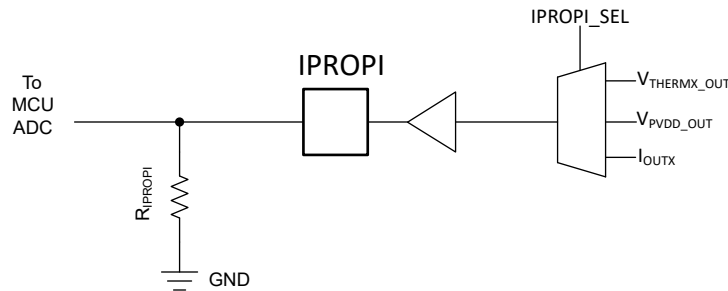


Figure 7-17. IPROPI Output Circuit

For current output, the IPROPI output analog current is scaled by A_{IPROPI} as follows:

$$I_{IPROPI} = I_{OUTX} / A_{IPROPI} \quad (1)$$

For voltage output of PVDD, the voltage is scaled down by a factor of 32 from a range of 4.5V to 40V. The PVDD voltage output is as follows:

$$V_{IPROPI} = V_{PVDD} / 32$$

For example:

- IPROPI_SEL is selected for PVDD
- PVDD is 13.5V
- $V_{IPROPI} = 0.422V$

The IPROPI output can also provide analog voltage representation of any single of the four thermal cluster temperature. This is intended for use in testing and evaluation, but not during device run-time.

For voltage conversion of thermal cluster temperature output reading, the voltage is scaled according to the temperature range $-40^{\circ}C$ to $185^{\circ}C$ and output voltage range of 0V to 3V. The voltage read out :

$$V_{IPROPI} = A + B \times \text{Cluster Temperature}$$

where A is offset roughly equal to 980mV, and B is slope of 2mV/ $^{\circ}C$.

When the cluster temperature is $-40^{\circ}C$, the IPROPI output voltage is 980mV. At $185^{\circ}C$ the IPROPI voltage is 1.35V.

The IPROPI pin must be connected to an external resistor (R_{IPROPI}) to ground to generate proportional voltage V_{IPROPI} . This allows for the load current to be measured as a voltage-drop across the R_{IPROPI} resistor in the application so that the full range of the controller ADC is utilized.

When the output is switched off, the current monitor output is in high impedance mode. The IPROPI output also has an optional sample and hold circuit that can be enabled with bit IPROPI_SH_EN in register HB_OUT_CNFG1.

7.4.6 Protection Circuits

7.4.6.1 Fault Reset (CLR_FLT)

The DRV8001-Q1 provides a specific sequence to clear fault conditions from the driver and resume operation. This function is provided through the CLR_FLT register bit. To clear fault reporting the CLR_FLT register bit must be asserted after the fault condition is removed. After being asserted, the driver clears the fault and reset the CLR_FLT register bit.

7.4.6.2 DVDD Logic Supply Power on Reset (DVDD_POR)

If at any time the input logic supply voltage on the DVDD pin falls below the V_{DVDD_POR} threshold for longer than the $t_{DVDD_POR_DG}$ time or the nSLEEP pin is asserted low, the device enters the inactive state disabling the gate drivers, charge pump, and protection monitors. Normal operation resumes when the DVDD undervoltage condition is removed or the nSLEEP pin is asserted high. After a DVDD power on reset (POR), the **POR** register bit is asserted until **CLR_FLT** is issued.

7.4.6.3 PVDD Supply Undervoltage Monitor (PVDD_UV)

If at any time the power supply voltage on the PVDD pin falls below the V_{PVDD_UV} threshold for longer than the $t_{PVDD_UV_DG}$ time, the DRV8001-Q1 detects a PVDD undervoltage condition. After detecting the undervoltage condition, the gate driver pulldowns are enabled, charge pump disabled, **FAULT** register bit, and **PVDD_UV** register bit are asserted.

The PVDD undervoltage monitor can recover in two different modes set through the **PVDD_UV_MODE** register setting.

- **Latched Fault Mode:** After the undervoltage condition is removed, the fault state remains latched and charge pump disabled until **CLR_FLT** is issued.
- **Automatic Recovery Mode:** After the undervoltage condition is removed, the **FAULT** register bit is automatically cleared and the charge pump automatically reenabled. The **PVDD_UV** register bit remains latched until **CLR_FLT** is issued.

7.4.6.4 VCP Charge Pump Undervoltage Lockout (VCP_UV)

If at any time the voltage on the VCP pin falls below the V_{VCP_UV} threshold for longer than the $t_{VCP_UV_DG}$ time, the DRV8001-Q1 detects a VCP undervoltage condition. After detecting the undervoltage condition, the gate driver pulldowns are enabled and **FAULT** register bit, and **VCP_UV** register bit is asserted. The undervoltage threshold can be adjusted through the **VCP_UV_LVL** register setting.

The VCP undervoltage monitor can recover in two different modes set through the **VCP_UV_MODE** register setting.

- **Latched Fault Mode:** Additionally the charge pump is disabled in latched fault mode. After the undervoltage condition is removed, the fault state remains latched and charge pump disabled until **CLR_FLT** is issued.
- **Automatic Recovery Mode:** After the undervoltage condition is removed, the **FAULT** register bit is automatically cleared and the driver automatically reenabled. The **VCP_UV** register bit remains latched until **CLR_FLT** is issued.

7.4.6.5 Thermal Clusters

As there are multiple drivers and types of drivers on this device, there are multiple dedicated thermal sensors located on chip to monitor key block temperatures on the chip. Each of these sensors, called thermal clusters, measure local die temperature for specific device blocks. These measurements can be converted to a voltage for output on IPROPI pin, used to trigger temperature warnings or to shutdown a specific cluster which is exceeding acceptable temperature range or the entire device.

The device response to thermal cluster warnings can be configured with bit **OTSD_MODE** in the **IC_CNFG1** register:

- Default mode (**OTSD_MODE** = 0b): if any cluster reaches thermal shutdown threshold for longer than t_{OTSD_DG} , the entire device is shutoff.
- Cluster mode (**OTSD_MODE** = 1b): if a cluster reaches thermal shutdown threshold for longer than t_{OTSD_DG} , only that cluster is shutoff.

There are four zones defined with thermal clusters, shown in the table and diagram below:

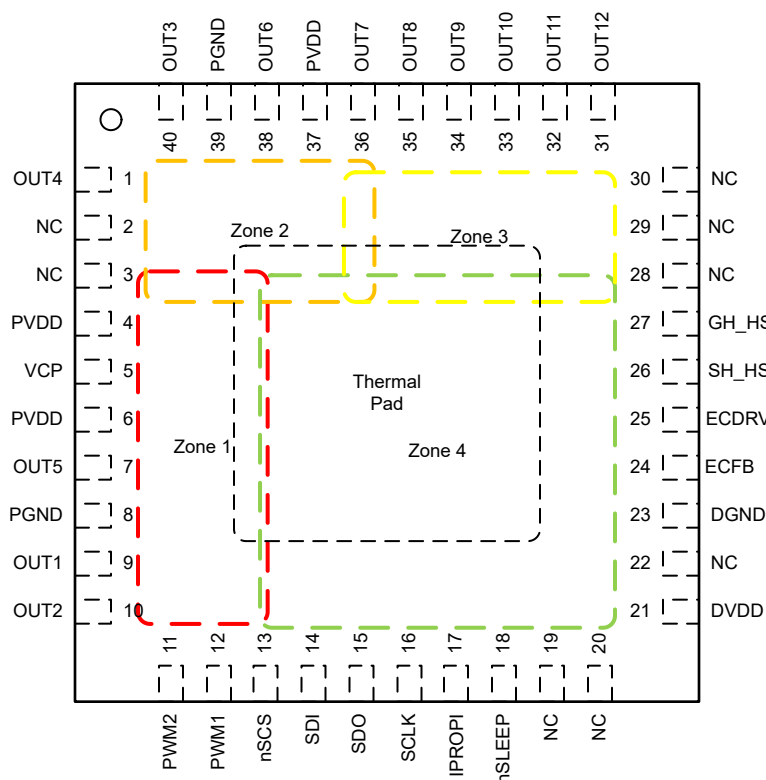


Figure 7-18. Thermal Sensor Zones

Table 7-38. Thermal Cluster Locations

Thermal Cluster 1	Thermal Cluster 2	Thermal Cluster 3	Thermal Cluster 4
Half-bridges OUT5, OUT1 and OUT2	Half-bridges OUT3, OUT4 and OUT6	All high-side drivers	Global and remaining drivers

For each zone, there are comparator-based warnings for two temperature points, 115° for low and 140°C for high. Bit [ZONEX_OTW_X](#) (L or H) is latched in register [IC_STAT2](#). Each warning can be individually disabled with bit [ZONEX_OTW_X_DIS](#) in register [IC_CNFG2](#). If overtemperature shutdown occurs, [ZONEX_OTSD](#) bit is latched in register [IC_STAT2](#).

7.4.6.6 Watchdog Timer

The device integrates a programmable window type SPI watchdog timer to verify that the external controller is operating and the SPI bus integrity is monitored. The SPI watchdog timer can be enabled by through the [WD_EN](#) SPI register bit. The watchdog timer is disabled by default. When the watchdog timer is enabled, an internal timer starts to count up. The watch dog timer is reset by inverting the [WD_RST](#) SPI register. This [WD_RST](#) must be issued between the lower window time and the upper window time. If a watchdog timer fault is detected, the device response can be configured to either report only a warning or report a fault and disable all drivers. The watch dog fault can be cleared with a [CLR_FLT](#) command. If the watchdog is set to disable all drivers, the drivers are enabled after a [CLR_FLT](#) command is sent to remove the watchdog fault condition.

7.4.6.7 Fault Detection and Response Summary Table

Table 7-39. Fault Detection and Response Summary

NAME	CONDITION	SPI BIT	MODE	DIGITAL CORE	CHARGE PUMP	DRIVERS	CURRENT SENSE	RESPONSE
SPI Clock Fault	Invalid SPI Clock Frame	SCLK_FLT	Latched	Active	Active	Active	Active	SPI_ERR, SPI, Reject Frame
DVDD Power-on-Reset	DVDD < V _{DVDD_POR}	POR	n/a	Reset	Disabled	Semi-Active Pulldown	Disabled	SPI
PVDD Undervoltage	PVDD < V _{PVDD_UV}	PVDD_UV	Latched	Active	Disabled	Semi-Active Pulldown	Disabled	SPI
			Automatic	Active	Disabled	Semi-Active Pulldown	Disabled	SPI
PVDD Overvoltage	PVDD > V _{PVDD_OV}	PVDD_OV	Latched	Active	Active	Pulldown	Active	SPI
		PVDD_OV	Automatic	Active	Active	Pulldown	Active	SPI
		PVDD_OV	Warning	Active	Active	Active	Active	WARN, SPI
		n/a	Disabled	Active	Active	Active	Active	n/a
VCP Undervoltage	VCP < V _{VCP_UV}	VCP_UV	Latched	Active	Disabled	Semi-Active Pulldown	Disabled	SPI
			Automatic	Active	Active	Semi-Active Pulldown	Disabled	SPI
Half-bridge Overcurrent Fault (OUT1-OUT6)	I _{OUTx} > I _{OCpx}	HB, OUTx_HS_OC, OUTx_LS_OC	Latched	Active	Active	Affected driver Hi-Z	Active	SPI
Half-bridge active open load Fault (OUT1-OUT6)	I _{OUTx} < I _{OLP_OUTx}	HB, OUTx_OLA	Latched	Active	Active	Active	Active	WARN
Half-bridge passive open load Fault (OUT1-OUT6)	I _{OUTx} < I _{OLP_OUTx}	HB, HB_OLP_STAT	Live	Active	Active	n/a	Active	WARN
High-side Driver overcurrent Fault (OUT7-OUT12)	I _{OUTx} > I _{OCpx}	HS, OUTx_OCP	Latched	Active	Active	Affected driver Hi-Z	Active	SPI
High-side Driver OUT7 ITRIP	I _{OUT7} > I _{OC7}	ITRIP, OUT7_ITRIP_STAT	Warning	Active	Active	n/a	Active	WARN
	t _{OUT7_ITRIP} > t _{OUT7_ITRIP_TO}	HS, ITRIP, OUT7_ITRIP_TO, OUT7_ITRIP_STAT	Latched	Active	Active	OUT7 Hi-Z after timeout	Active	SPI
	I _{OUT7} > I _{OC7}	ITRIP, OUT7_ITRIP_STAT	Warning	Active	Active	OUT7 ITRIP regulation indefinite	Active	WARN
	t _{OUT7_ITRIP} > t _{OUT7_ITRIP_TO}	ITRIP, OUT7_ITRIP_TO, OUT7_ITRIP_STAT	Warning	Active	Active	OUT7 ITRIP regulation disabled;	Active	WARN

Table 7-39. Fault Detection and Response Summary (continued)

NAME	CONDITION	SPI BIT	MODE	DIGITAL CORE	CHARGE PUMP	DRIVERS	CURRENT SENSE	RESPONSE
High-side Driver open load Fault (OUT7-OUT12)	$I_{OUTx} < I_{OCPx}$	HS, OUTx_OLP	Warning	Active	Active	Active	Active	WARN
ECFB Overvoltage	$V_{ECFB} > V_{ECFB_OV}$	EC_HEAT, ECFB_OV	Disabled	Active	Active	n/a	Active	n/a
	$V_{ECFB} > V_{ECFB_OV}$	EC_HEAT, ECFB_OV	Latched	Active	Active	n/a	Active	SPI
	$V_{ECFB} > V_{ECFB_OV}$	EC_HEAT, ECFB_OV	Latched	Active	Active	ECDRV pulled down, ECFB LS FET Hi-Z	Active	SPI
ECFB Undervoltage	$V_{ECFB} > V_{ECFB_UV}$	EC_HEAT, ECFB_UV	Disabled	Active	Active	n/a	Active	n/a
	$V_{ECFB} > V_{ECFB_UV}$	EC_HEAT, ECFB_UV	Latched	Active	Active	n/a	Active	SPI
	$V_{ECFB} > V_{ECFB_UV}$	EC_HEAT, ECFB_UV	Latched	Active	Active	ECDRV pulled down, ECFB LS FET Hi-Z	Active	SPI
ECFB Above Target Voltage	$V_{ECFB} > V_{EC_V_TAR}$	EC_HEAT, ECFB_HI	Live	Active	Active	n/a	Active	WARN
ECFB Below Target Voltage	$V_{ECFB} < V_{EC_V_TAR}$	EC_HEAT, ECFB_LO	Live	Active	Active	n/a	Active	WARN
ECFB Overcurrent (discharge)	$I_{ECFB} > I_{ECFB_OC}$	EC_HEAT, ECFB_OC	Latched	Active	Active	ECFB Hi-Z	Active	SPI
ECFB Open load (discharge)	$I_{ECFB} < I_{OL_ECFB_LS}$	EC_HEAT, ECFB_OL	Latched	Active	Active	n/a	Active	WARN, SPI
ECFB Open load (active/charge, OUT11 independent mode, ECDRV_OL_EN enabled)	$V_{ECFB} > V_{ECFB_OV}$	EC_HEAT, ECFB_OL, ECFB_OV	Latched	Active	Active	n/a	Active	WARN, SPI
Heater VDS Overcurrent Fault	$V_{HEAT_VDS} > V_{HEAT_VDS_LVL}$	EC_HEAT, HEAT_VDS	Latched	Active	Active	Pulldown	Active	SPI
			Cycle	Active	Active	Pulldown	Active	SPI
			Warning	Active	Active	Active	Active	WARN, SPI
			Disabled	Active	Active	Active	Active	n/a
Heater VDS Open load Fault	$V_{SH_HS} > V_{OL_HEAT}$	EC_HEAT, HEAT_OL	Latched	Active	Active	Pulldown	Active	SPI
Zone X Thermal Warning	$T_J > T_{OTW_X}$	OTW, ZONEx_OTW_X	Automatic	Active	Active	Active	Active	WARN, SPI
Zone X Thermal Shutdown	$T_J > T_{OTSD}$	OTSD, ZONEx_OTSD	Latched	Active	Disabled	Semi-Active Pulldown, Hi-Z	Disabled	SPI

Table 7-39. Fault Detection and Response Summary (continued)

NAME	CONDITION	SPI BIT	MODE	DIGITAL CORE	CHARGE PUMP	DRIVERS	CURRENT SENSE	RESPONSE
Watchdog	Invalid Access or Expiration	WD_FLT	Warning	Active	Active	Active	Active	WARN, SPI
			Latched Fault	Active	Active	Pulldown	Active	SPI

7.5 Programming

7.5.1 Serial Peripheral Interface (SPI)

An SPI bus is used to set device configurations, operating parameters, and read out diagnostic information on the DRV8001-Q1 device. The SPI operates in peripheral mode and connects to a controller. The SPI input data (SDI) word consists of a 24 bit word, with an 8 bit command and 16 bits of data. The SPI output data (SDO) word for read commands consists of the fault status indication bits and then the register data being accessed for read commands. The SDO word for write commands consists of the command data followed by the existing data in the written register. The data sequence between the MCU and the SPI peripheral driver is shown in [Figure 7-19](#).

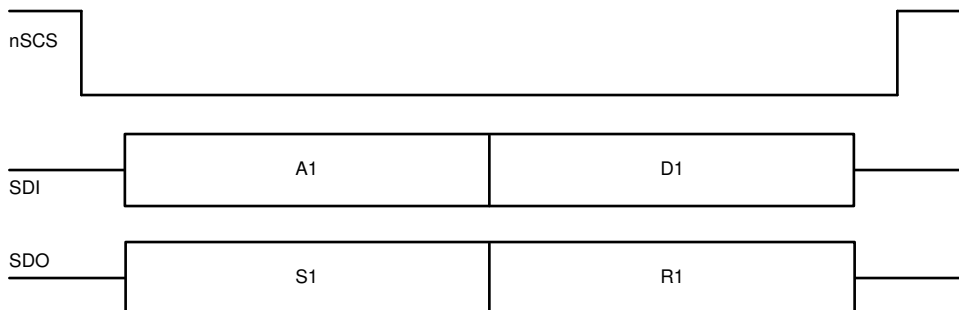


Figure 7-19. SPI Data Frame

A valid frame must meet the following conditions:

- The SCLK pin is pulled low when the nSCS pin transitions from high to low and from low to high.
- The nSCS pin is pulled high between words.
- When the nSCS pin is pulled high, any signals at the SCLK and SDI pins are ignored and the SDO pin is placed in the Hi-Z state.
- Data is captured on the falling edge of SCLK and data is propagated on the rising edge of SCLK.
- The most significant bit (MSB) is shifted in and out first.
- A full 24 SCLK cycles must occur for transaction to be valid.
- If the data word sent to the SDI pin is less than or more than 24 bits, a frame error (SCLK_FLT) occurs and the data word is ignored.
- For a write command, following the 16-bit command data, the existing data in the register being written to is shifted out on the SDO pin starting with fault status byte then 16-bit data .

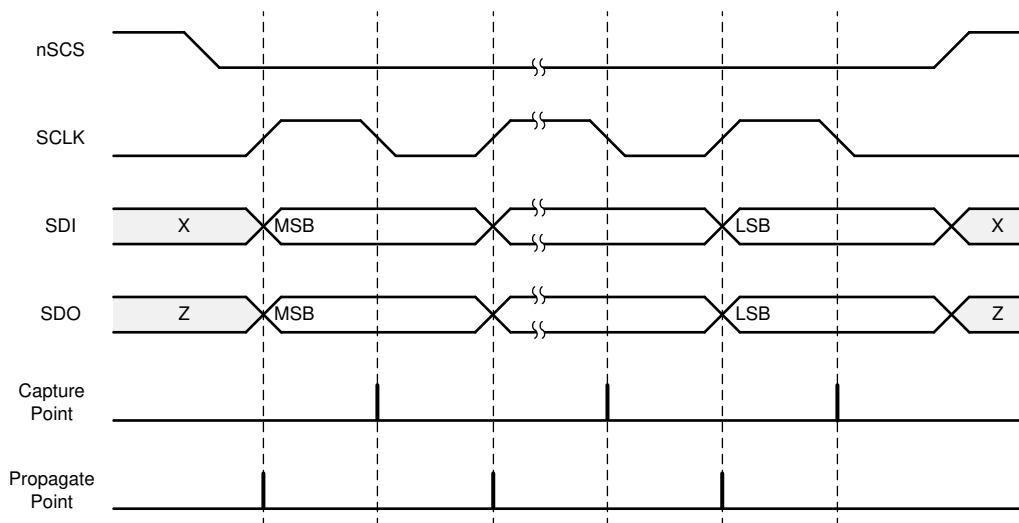


Figure 7-20. SPI peripheral Timing Diagram

7.5.2 SPI Format

The SDI input data word is 24 bits long and consists of the following format:

- MSB bit indicates frame type (bit B23 = 0 for standard frame)
- 1 read or write bit, W (bit B22, write = 0, read = 1)
- 6 address bits, A (bits B21 through B16)
- 16 data bits, D (bits B15 through B0). For a read operation, these bits are typically set to null values, while for a write operation, these bits have the data value for the addressed register.

Table 7-40. SDI Input Data Word Format

		R/W	Address						Data															
Bit	B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data	0	W0	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

The SDO output data word is 24 bits long and the first 8 bits makes up the IC status register. The report word is the content of the register being accessed.

For a write command (W0 = 0), the response word consists of the fault status indication bits followed by the existing data in the register being written to.

For a read command (W0 = 1), the response word consists of the fault status indications bits followed by the data currently in the register being read.

Table 7-41. SDO Output Data Word Format

	IC Status									Report							
Bit	B23	B22	B21	B20	B19	B18	B17	B16		B15	B14	B13	B12	B11	B10	B9	B8
										B7	B6	B5	B4	B3	B2	B1	B0
Data	1	1	FAULT	WARN	OV_UV	DRV	OTSD	SPI_ERR		D15	D14	D13	D12	D11	D10	D9	D8
										D7	D6	D5	D4	D3	D2	D1	D0

- FAULT - 'OR' of any device fault (global or driver)
- WARN - 'OR' of any device warnings
- OV_UV - 'OR' of PVDD overvoltage and undervoltage status

- DRV - 'OR' of any driver fault
- OTSD - Set when over temperature shutdown occurs
- SPI_ERR - Set when incorrect number of SCLKs received

7.5.3 Timing Diagrams

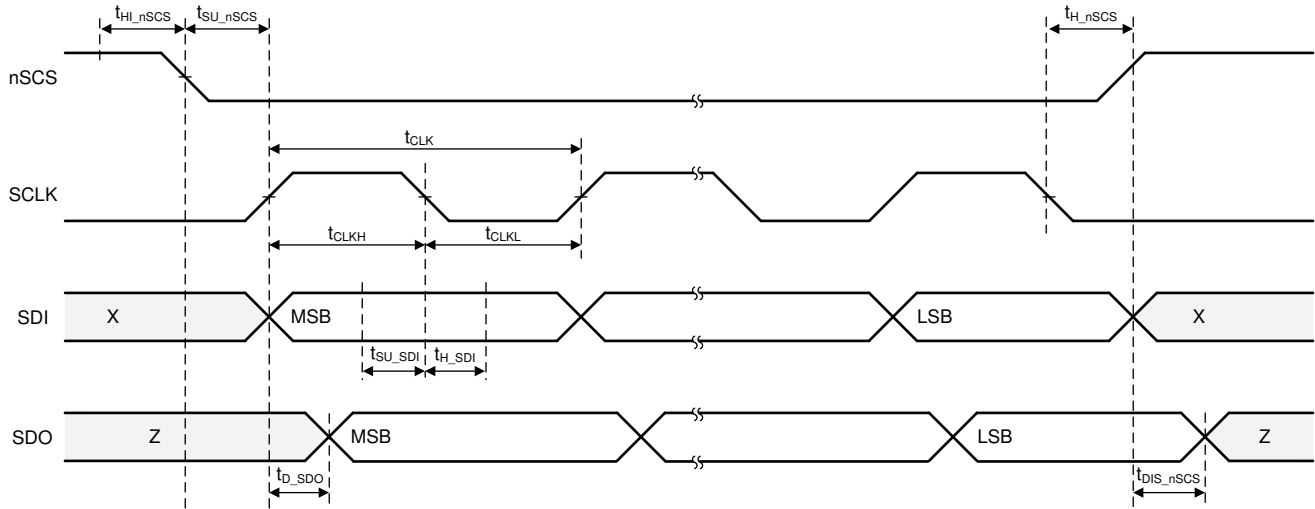


Figure 7-21. SPI Timing Diagram

8 DRV8001-Q1 Register Map

[DRV8001-Q1 Register Map](#) lists the memory-mapped registers for the DRV8001-Q1. All register addresses not listed are considered as reserved locations and the register contents are not be modified. Descriptions of reserved locations are provided for reference only. The device ID table summarizes the device IDs for DRV800x devices.

Table 8-1. Device ID Summary

Device	Device ID
DRV8000-Q1	Reg Address 0x8h, DEVICE_ID=0x01
DRV8001-Q1	Reg Address 0x8h, DEVICE_ID=0x11
DRV8002-Q1	Reg Address 0x8h, DEVICE_ID=0x01

Table 8-2. DRV8001-Q1 Register Map

Name	15	14	13	12	11	10	9	8	Type	Addr
	7	6	5	4	3	2	1	0		
IC_STAT1	SPI_OK	POR	FAULT	WARN	RSVD	HB	EC_HEAT	HS	R	00h
	PVDD_UV	PVDD_OV	VCP_UV	OTW	OTSD	WD_FLT	ITRIP	OUT7_ITRIP_TO		
IC_STAT2	PARITY	RSVD	SCLK_FLT	RSVD	ZONE4_OTSD	ZONE3_OTSD	ZONE2_OTSD	ZONE1_OTSD	R	01h
	ZONE4_OTW_H	ZONE3_OTW_H	ZONE2_OTW_H	ZONE1_OTW_H	ZONE4_OTW_L	ZONE3_OTW_L	ZONE2_OTW_L	ZONE1_OTW_L		
RSVD	RSVD								R	02h
HB_STAT1	RSVD		OUT6_LS_OCP	OUT5_LS_OCP	OUT4_LS_OCP	OUT3_LS_OCP	OUT2_LS_OCP	OUT1_LS_OCP	R	03h
	RSVD		OUT6_HS_OCP	OUT5_HS_OCP	OUT4_HS_OCP	OUT3_HS_OCP	OUT2_HS_OCP	OUT1_HS_OCP		
HB_STAT2	RSVD		OUT6_OLP	OUT5_OLP	OUT4_OLP	OUT3_OLP	OUT2_OLP	OUT1_OLP	R	04h
	RSVD		OUT6_OLA	OUT5_OLA	OUT4_OLA	OUT3_OLA	OUT2_OLA	OUT1_OLA		
EC_HEAT_ITRIP_STAT	ECFB_UV	ECFB_OV	ECFB_OV	ECFB_UV	ECFB_OC	ECFB_OL	HEAT_OL	HEAT_VDS	R	05h
	OUT7_ITRIP_TO	OUT7_ITRIP_ST_AT	OUT6_ITRIP_ST_AT	OUT5_ITRIP_ST_AT	OUT4_ITRIP_ST_AT	OUT3_ITRIP_ST_AT	OUT2_ITRIP_ST_AT	OUT1_ITRIP_ST_AT		
HS_STAT	RSVD		OUT12_OLA	OUT11_OLA	OUT10_OLA	OUT9_OLA	OUT8_OLA	OUT7_OLA	R	06h
	RSVD		OUT12_OCP	OUT11_OCP	OUT10_OCP	OUT9_OCP	OUT8_OCP	OUT7_OCP		
SPARE_STAT_1	RSVD								R	07h
SPARE_STAT_2	DEVICE_ID								R	08h
IC_CNFG1	OTSD_MODE	DIS_CP	PVDD_OV_MODE		PVDD_OV_DG		PVD_OV_LVL	VCP_UV_LVL	R/W	09h
	CP_MODE		VCP_UV_MODE	PVDD_UV_MODE_E	WD_EN	WD_FLT_M	WD_WIN	EN_SSC		
IC_CNFG2	RSVD								R/W	0Ah
	ZONE4_OTW_H_DIS	ZONE3_OTW_H_DIS	ZONE2_OTW_H_DIS	ZONE1_OTW_H_DIS	ZONE4_OTW_L_DIS	ZONE3_OTW_L_DIS	ZONE2_OTW_L_DIS	ZONE1_OTW_L_DIS		
RSVD	RSVD from 0Bh to 13h								R	0Bh - 13h
HB_ITRIP_DG	RSVD				OUT6_ITRIP_DG		OUT5_ITRIP_DG		R/W	14h
	OUT4_ITRIP_DG		OUT3_ITRIP_DG		OUT2_ITRIP_DG		OUT1_ITRIP_DG			
HB_OUT_CNFG1	RSVD	NSR_OUT6_DIS	NSR_OUT5_DIS	NSR_OUT4_DIS	NSR_OUT3_DIS	NSR_OUT2_DIS	NSR_OUT1_DIS	IPROPI_SH_EN	R/W	15h
	RSVD		OUT6_CNFG			OUT5_CNFG				
HB_OUT_CNFG2	RSVD		OUT3_CNFG			OUT4_CNFG			R/W	16h
	RSVD		OUT2_CNFG			OUT1_CNFG				
HB_OCP_CNFG	RSVD				OUT6_OCP_DG		OUT5_OCP_DG		R/W	17h
	OUT4_OCP_DG		OUT3_OCP_DG		OUT2_OCP_DG		OUT1_OCP_DG			
HB_OL_CNF_G1	RSVD		OUT6_OLP_EN	OUT5_OLP_EN	OUT4_OLP_EN	OUT3_OLP_EN	OUT2_OLP_EN	OUT1_OLP_EN	R/W	18h
	RSVD		OUT6_OLA_EN	OUT5_OLA_EN	OUT4_OLA_EN	OUT3_OLA_EN	OUT2_OLA_EN	OUT1_OLA_EN		
HB_OL_CNF_G2	RSVD		RSVD						R/W	19h
	RSVD		OUT6_OLA_TH	OUT5_OLA_TH	OUT4_OLA_TH	OUT3_OLA_TH	OUT2_OLA_TH	OUT1_OLA_TH		
HB_SR_CNF_G	RSVD				OUT6_SR		OUT5_SR		R/W	1Ah
	OUT4_SR		OUT3_SR		OUT2_SR		OUT1_SR			
HB_ITRIP_CNFG	OUT6_ITRIP_EN	OUT5_ITRIP_EN	OUT4_ITRIP_EN	OUT3_ITRIP_EN	OUT2_ITRIP_EN	OUT1_ITRIP_EN	OUT6_ITRIP_LVL		R/W	1Bh
	OUT5_ITRIP_LVL		OUT4_ITRIP_LVL		OUT3_ITRIP_LVL		OUT2_ITRIP_LVL_L	OUT1_ITRIP_LVL_L		

Table 8-2. DRV8001-Q1 Register Map (continued)

Name	15	14	13	12	11	10	9	8	Type	Address
	7	6	5	4	3	2	1	0		
HB_ITRIP_FREQ	RSVD				OUT6_ITRIP_FREQ		OUT5_ITRIP_FREQ		R/W	1Ch
	OUT4_ITRIP_FREQ		OUT3_ITRIP_FREQ		OUT2_ITRIP_FREQ		OUT1_ITRIP_FREQ			
HS_HEAT_OUT_CNFG	HEAT_CNFG		RSVD		OUT12_CNFG		OUT11_CNFG		R/W	1Dh
	OUT10_CNFG		OUT9_CNFG		OUT8_CNFG		OUT7_CNFG			
HS_OC_CFG	RSVD			OUT11_EC_MODE	RSVD				R/W	1Eh
	RSVD		OUT12_OC_TH	OUT11_OC_TH	OUT10_OC_TH	OUT9_OC_TH	OUT8_OC_TH	OUT7_RDSON_MODE		
HS_OL_CFG	RSVD		OUT12_OLA_TH	OUT11_OLA_TH	OUT10_OLA_TH	OUT9_OLA_TH	OUT8_OLA_TH	OUT7_OLA_TH	R/W	1Fh
	RSVD		OUT12_OLA_EN	OUT11_OLA_EN	OUT10_OLA_EN	OUT9_OLA_EN	OUT8_OLA_EN	OUT7_OLA_EN		
HS_REG_CFG1	RSVD					OUT7_OCP_DIS	ITRIP_TO_SEL		R/W	20h
	OUT7_ITRIP_CNFG		OUT7_ITRIP_BLK		OUT7_ITRIP_FREQ		OUT7_ITRIP_DG			
HS_REG_CFG2	RSVD		OUT12_CCM_TO	OUT11_CCM_TO	OUT10_CCM_TO	OUT9_CCM_TO	OUT8_CCM_TO	OUT7_CCM_TO	R/W	21h
	RSVD		OUT12_CCM_EN	OUT11_CCM_EN	OUT10_CCM_EN	OUT9_CCM_EN	OUT8_CCM_EN	OUT7_CCM_EN		
HS_PWM_FREQ_CNFG	RSVD				PWM_OUT12_FREQ		PWM_OUT11_FREQ		R/W	22h
	PWM_OUT10_FREQ		PWM_OUT9_FREQ		PWM_OUT8_FREQ		PWM_OUT7_FREQ			
HEAT_CNFG	RSVD				HEAT_VDS_LVL				R/W	23h
	HS_VDS_MODE		HEAT_VDS_BLK		HEAT_VDS_DG		HEAT_OLP_EN	RSVD		
EC_CNFG	ECDRV_OL_EN	ECFB_UV_TH	RSVD		ECFB_UV_DG		ECFB_OV_DG		R/W	24h
	RSVD		EC_OV_MODE		EC_FLT_MODE	ECFB_LS_PWM	EC_OLEN	ECFB_MAX		
HS_OCP_DG	RSVD				OUT12_OCP_DG		OUT11_OCP_DG		R/W	25h
	OUT10_OCP_DG		OUT9_OCP_DG		OUT8_OCP_DG		OUT7_OCP_DG			
SPARE_CFG2	RSVD								R/W	26h
SPARE_CFG3	RSVD								R/W	27h
SPARE_CFG4	RSVD								R/W	28h
IC_CTRL	RSVD		IPROPI_MODE	IPROPI_SEL					R/W	29h
	CTRL_LOCK			CNFG_LOCK			RSVD	CLR_FLT		
HB_CTRL	RSVD				OUT6_CTRL		OUT5_CTRL		R/W	2Ah
	OUT4_CTRL		OUT3_CTRL		OUT2_CTRL		OUT1_CTRL			
HS_EC_HEAT_CTRL	ECFB_LS_EN	EC_ON	EC_V_TAR						R/W	2Bh
	HEAT_EN	RSVD	OUT12_EN	OUT11_EN	OUT10_EN	OUT9_EN	OUT8_EN	OUT7_EN		
OUT7_PWM_DC	RSVD						OUT7_DC		R/W	2Ch
						OUT7_DC				
OUT8_PWM_DC	RSVD						OUT8_DC		R/W	2Dh
							OUT8_DC			
OUT9_PWM_DC	RSVD						OUT9_DC		R/W	2Eh
							OUT9_DC			
OUT10_PWM_DC	RSVD						OUT10_DC		R/W	2Fh
							OUT10_DC			
OUT11_PWM_DC	RSVD						OUT11_DC		R/W	30h
							OUT11_DC			
OUT12_PWM_DC	RSVD						OUT12_DC		R/W	31h
							OUT12_DC			

8.1 DRV8000-Q1_STATUS Registers

Table 8-3 lists the memory-mapped registers for the DRV8000-Q1_STATUS registers. All register offset addresses not listed in Table 8-3 are considered as reserved locations and the register contents are not to be modified.

Table 8-3. DRV8000-Q1_STATUS Registers

Offset	Acronym	Register Name	Section
0h	IC_STAT1	Device status summary 1.	Section 8.1.1
1h	IC_STAT2	Device status summary 2.	Section 8.1.2
2h	GD_STAT	Gate driver status.	Section 8.1.3
3h	HB_STAT1	Half-bridge overcurrent status.	Section 8.1.4
4h	HB_STAT2	Half-bridge open-load status.	Section 8.1.5
5h	EC_HEAT_ITRIP_STAT	Electrochrome, Heater, and ITRIP status.	Section 8.1.6
6h	HS_STAT	High-side driver status.	Section 8.1.7
7h	SPARE_STAT1	Spare status 1.	Section 8.1.8
8h	SPARE_STAT2	Spare status 2.	Section 8.1.9

Complex bit access types are encoded to fit into small table cells. Table 8-4 shows the codes that are used for access types in this section.

Table 8-4. DRV8000-Q1_STATUS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

8.1.1 IC_STAT1 Register (Offset = 0h) [Reset = C000h]

IC_STAT1 is shown in [Table 8-5](#).

Return to the [Summary Table](#).

Main device status register for driver, supply and over temperature fault status. Also includes watchdog and ITRIP regulation fault status.

Table 8-5. IC_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SPI_OK	R	1h	Indicates if a SPI communications fault has been detected. 0b = One or multiple of SCLK_FLT in the prior frames. 1b = No SPI fault has been detected.
14	POR	R	1h	Indicates power-on-reset condition. 0b = No power-on-reset condition detected. 1b = Power-on reset condition detected.
13	FAULT	R	0h	General Fault indicator. Indicates a device or driver fault has occurred. 0b = No fault. 1b = Fault detected.
12	WARN	R	0h	General warning indicator. Indicates a warning is present. 0b = No warning. 1b = Warning is present.
11	GD	R	0h	Logic OR of VDS and VGS fault indicators for gate driver.
10	HB	R	0h	Logic OR of overcurrent and open load fault indicators for half-bridges.
9	EC_HEAT	R	0h	Logic OR of EC OV/UV, overcurrent, open load fault indicators for EC and heater.
8	HS	R	0h	Logic OR of overcurrent and open load fault indicators for high-side drivers.
7	PVDD_UV	R	0h	Indicates undervoltage fault on PVDD pin.
6	PVDD_OV	R	0h	Indicates overvoltage fault on PVDD pin.
5	VCP_UV	R	0h	Indicates undervoltage fault on VCP pin.
4	OTW	R	0h	Indicates overtemperature warning.
3	OTSD	R	0h	Indicates overtemperature shutdown
2	WD_FLT	R	0h	Indicates watchdog timer fault.
1	ITRIP	R	0h	Indicates ITRIP regulation warning when any OUTx entered ITRIP.
0	OUT7_ITRIP_TO	R	0h	Indicates OUT7 ITRIP timeout has occurred when set.

8.1.2 IC_STAT2 Register (Offset = 1h) [Reset = 0000h]

IC_STAT2 is shown in [Table 8-6](#).

Return to the [Summary Table](#).

Second device status register with SPI faults and specific thermal cluster fault/warning status.

Table 8-6. IC_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	SCLK_FLT	R	0h	Indicates SPI clock (frame) fault when the number of SCLK pulses in a transaction frame are not equal to 16. Reported on bit SPI_ERR.
12	RESERVED	R	0h	Reserved
11	ZONE4_OTSD	R	0h	Indicates overtemperature shutdown has occurred in zone 4.
10	ZONE3_OTSD	R	0h	Indicates overtemperature shutdown has occurred in zone 3.
9	ZONE2_OTSD	R	0h	Indicates overtemperature shutdown has occurred in zone 2.
8	ZONE1_OTSD	R	0h	Indicates overtemperature shutdown has occurred in zone 1.
7	ZONE4_OTW_H	R	0h	Indicates high temperature warning (above 125°C) has occurred in zone 4.
6	ZONE3_OTW_H	R	0h	Indicates high temperature warning (above 125°C) has occurred in zone 3.
5	ZONE2_OTW_H	R	0h	Indicates high temperature warning (above 125°C) has occurred in zone 2.
4	ZONE1_OTW_H	R	0h	Indicates high temperature warning (above 125°C) has occurred in zone 1.
3	ZONE4_OTW_L	R	0h	Indicates low temperature warning (above 105°C) has occurred in zone 4.
2	ZONE3_OTW_L	R	0h	Indicates low temperature warning (above 105°C) has occurred in zone 3.
1	ZONE2_OTW_L	R	0h	Indicates low temperature warning (above 105°C) has occurred in zone 2.
0	ZONE1_OTW_L	R	0h	Indicates low temperature warning (above 105°C) has occurred in zone 1.

8.1.3 GD_STAT Register (Offset = 2h) [Reset = 0000h]

GD_STAT is shown in [Table 8-7](#).

Return to the [Summary Table](#).

Gate driver status register with all gate driver faults and warnings, including smart gate driver faults and warnings.

Table 8-7. GD_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DRVOFF_STAT	R	0h	Indicates the status (high or low) of DRVOFF pin. If DRVOFF pin is asserted, DRVOFF_STAT = 1b. If DRVOFF pin is deasserted, DRVOFF_STAT = 0b.
14	RESERVED	R	0h	Reserved
13	STC_WARN_R	R	0h	Indicates rising slew time TDRV overflow for half-bridge 1 and 2.
12	STC_WARN_F	R	0h	Indicates falling slew time TDRV overflow for half-bridge 1 and 2.
11	PCHR_WARN	R	0h	Indicates pre-charge underflow or overflow fault for half-bridge 1 and 2.
10	PDCHR_WARN	R	0h	Indicates pre-discharge underflow or overflow fault for half-bridge 1 and 2.
9	IDIR_WARN	R	0h	Indicates unknown current direction for half-bridge 1 and 2
8	IDIR	R	0h	Indicates current direction for half-bridge 1 and 2.
7	VGS_L2	R	0h	Indicates VGS gate fault on the low-side 2 MOSFET.
6	VGS_H2	R	0h	Indicates VGS gate fault on the high-side 2 MOSFET.
5	VGS_L1	R	0h	Indicates VGS gate fault on the low-side 1 MOSFET.
4	VGS_H1	R	0h	Indicates VGS gate fault on the high-side 1 MOSFET.
3	VDS_L2	R	0h	Indicates VDS overcurrent fault on the low-side 2 MOSFET.
2	VDS_H2	R	0h	Indicates VDS overcurrent fault on the high-side 2 MOSFET.
1	VDS_L1	R	0h	Indicates VDS overcurrent fault on the low-side 1 MOSFET.
0	VDS_H1	R	0h	Indicates VDS overcurrent fault on the high-side 1 MOSFET.

8.1.4 HB_STAT1 Register (Offset = 3h) [Reset = 0000h]

HB_STAT1 is shown in [Table 8-8](#).

Return to the [Summary Table](#).

Half-bridge overcurrent faults for either high- or low-side of each half-bridge.

Table 8-8. HB_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	OUT6_LS_OCP	R	0h	Indicates overcurrent fault on low-side of half-bridge OUT6.
12	OUT5_LS_OCP	R	0h	Indicates overcurrent fault on low-side of half-bridge OUT5.
11	OUT4_LS_OCP	R	0h	Indicates overcurrent fault on low-side of half-bridge OUT4.
10	OUT3_LS_OCP	R	0h	Indicates overcurrent fault on low-side of half-bridge OUT3.
9	OUT2_LS_OCP	R	0h	Indicates overcurrent fault on low-side of half-bridge OUT2.
8	OUT1_LS_OCP	R	0h	Indicates overcurrent fault on low-side of half-bridge OUT1.
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	OUT6_HS_OCP	R	0h	Indicates overcurrent fault on high-side of half-bridge OUT6.
4	OUT5_HS_OCP	R	0h	Indicates overcurrent fault on high-side of half-bridge OUT5.
3	OUT4_HS_OCP	R	0h	Indicates overcurrent fault on high-side of half-bridge OUT4.
2	OUT3_HS_OCP	R	0h	Indicates overcurrent fault on high-side of half-bridge OUT3.
1	OUT2_HS_OCP	R	0h	Indicates overcurrent fault on high-side of half-bridge OUT2.
0	OUT1_HS_OCP	R	0h	Indicates overcurrent fault on high-side of half-bridge OUT1.

8.1.5 HB_STAT2 Register (Offset = 4h) [Reset = 0000h]

HB_STAT2 is shown in [Table 8-9](#).

Return to the [Summary Table](#).

Half-bridge active and off-state open load faults.

Table 8-9. HB_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	HB_OLP_STAT	R	0h	Indicates off-state open load fault on the selected half-bridge output per HB_OLP_CNFG bits (OUTX or OUTY).
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	OUT6_OLA	R	0h	Indicates active open load fault on half-bridge OUT6.
4	OUT5_OLA	R	0h	Indicates active open load fault on half-bridge OUT5.
3	OUT4_OLA	R	0h	Indicates active open load fault on half-bridge OUT4.
2	OUT3_OLA	R	0h	Indicates active open load fault on half-bridge OUT3.
1	OUT2_OLA	R	0h	Indicates active open load fault on half-bridge OUT2.
0	OUT1_OLA	R	0h	Indicates active open load fault on half-bridge OUT1.

8.1.6 EC_HEAT_ITRIP_STAT Register (Offset = 5h) [Reset = 0000h]

EC_HEAT_ITRIP_STAT is shown in [Table 8-10](#).

Return to the [Summary Table](#).

Includes all electrochrom and heater driver faults and warnings. Also includes ITRIP regulation status warnings.

Table 8-10. EC_HEAT_ITRIP_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ECFB_UV	R	0h	Indicates undervoltage (short to ground) fault on ECFB pin.
14	ECFB_OV	R	0h	Indicates overvoltage (short to battery) fault on ECFB pin.
13	ECFB_HI	R	0h	Indicates regulation overvoltage fault on ECFB pin.
12	ECFB_LO	R	0h	Indicates regulation undervoltage fault on ECFB pin.
11	ECFB_OC	R	0h	Indicates overcurrent fault on ECFB pin.
10	ECFB_OL	R	0h	Indicates open load fault on ECFB pin.
9	HEAT_OL	R	0h	Indicates open load fault on SH_HS pin.
8	HEAT_VDS	R	0h	Indicates overcurrent fault on heater MOSFET.
7	OUT7_ITRIP_TO	R	0h	Indicates ITRIP timeout occurred on OUT7.
6	OUT7_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT7.
5	OUT6_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT6.
4	OUT5_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT5.
3	OUT4_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT4.
2	OUT3_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT3.
1	OUT2_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT2.
0	OUT1_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT1.

8.1.7 HS_STAT Register (Offset = 6h) [Reset = 0000h]

HS_STAT is shown in [Table 8-11](#).

Return to the [Summary Table](#).

High-side driver overcurrent and open load fault status.

Table 8-11. HS_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	OUT12_OLA	R	0h	Indicates open load fault on OUT12.
12	OUT11_OLA	R	0h	Indicates open load fault on OUT11.
11	OUT10_OLA	R	0h	Indicates open load fault on OUT10.
10	OUT9_OLA	R	0h	Indicates open load fault on OUT9.
9	OUT8_OLA	R	0h	Indicates open load fault on OUT8.
8	OUT7_OLA	R	0h	Indicates open load fault on OUT7.
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	OUT12_OCP	R	0h	Indicates overcurrent fault on OUT12.
4	OUT11_OCP	R	0h	Indicates overcurrent fault on OUT11.
3	OUT10_OCP	R	0h	Indicates overcurrent fault on OUT10.
2	OUT9_OCP	R	0h	Indicates overcurrent fault on OUT9.
1	OUT8_OCP	R	0h	Indicates overcurrent fault on OUT8.
0	OUT7_OCP	R	0h	Indicates overcurrent fault on OUT7.

8.1.8 SPARE_STAT1 Register (Offset = 7h) [Reset = 0000h]

SPARE_STAT1 is shown in [Table 8-12](#).

Return to the [Summary Table](#).

Spare status register.

Table 8-12. SPARE_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

8.1.9 SPARE_STAT2 Register (Offset = 8h) [Reset = 0001h]

SPARE_STAT2 is shown in [Table 8-13](#).

Return to the [Summary Table](#).

Spare status register.

Table 8-13. SPARE_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	DEVICE_ID_7	R	0h	Device ID bit field 7.
6	DEVICE_ID_6	R	0h	Device ID bit field 6.
5	DEVICE_ID_5	R	0h	Device ID bit field 5.
4	DEVICE_ID_4	R	0h	Device ID bit field 4.
3	DEVICE_ID_3	R	0h	Device ID bit field 3.
2	DEVICE_ID_2	R	0h	Device ID bit field 2.
1	DEVICE_ID_1	R	0h	Device ID bit field 1.
0	DEVICE_ID_0	R	1h	Device ID bit field 0. DRV8000-Q1 address is 0x01.

8.2 DRV8000-Q1_CNFG Registers

Table 8-14 lists the memory-mapped registers for the DRV8000-Q1_CNFG registers. All register offset addresses not listed in Table 8-14 are considered as reserved locations and the register contents are not to be modified.

Table 8-14. DRV8000-Q1_CNFG Registers

Offset	Acronym	Register Name	Section
9h	IC_CNFG1	IC configuration register 1.	Section 8.2.1
Ah	IC_CNFG2	IC configuration register 2.	Section 8.2.2
Bh	GD_CNFG	Gate driver configuration register.	Section 8.2.3
Ch	GD_IDRV_CNFG	IDRIVE setting configuration register.	Section 8.2.4
Dh	GD_VGS_CNFG	VGS detection configuration register.	Section 8.2.5
Eh	GD_VDS_CNFG	VDS monitoring configuration register.	Section 8.2.6
Fh	GD_CSA_CNFG	CSA configuration register.	Section 8.2.7
10h	GD_AGD_CNFG	Advanced smart gate driver configuration register.	Section 8.2.8
11h	GD_PDR_CNFG	Propagation Delay Reduction configuration register.	Section 8.2.9
12h	GD_STC_CNFG	Slew time control configuration register.	Section 8.2.10
13h	GD_SPARE_CNFG1	Spare gate driver configuration register 1.	Section 8.2.11
14h	HB_ITRIP_DG	Half-bridge ITRIP deglitch configuration register 2.	Section 8.2.12
15h	HB_OUT_CNFG1	Half-bridge output 5 and 6 configuration register.	Section 8.2.13
16h	HB_OUT_CNFG2	Half-bridge output 1-4 configuration register.	Section 8.2.14
17h	HB_OCP_CNFG	Half-bridge overcurrent deglitch configuration register.	Section 8.2.15
18h	HB_OL_CNFG1	Half-bridge active and passive open-load enable register	Section 8.2.16
19h	HB_OL_CNFG2	Half-bridge active open-load threshold select register.	Section 8.2.17
1Ah	HB_SR_CNFG	Half-bridge slew rate configuration register.	Section 8.2.18
1Bh	HB_ITRIP_CNFG	Half-bridge ITRIP configuration register 1.	Section 8.2.19
1Ch	HB_ITRIP_FREQ	Half-bridge ITRIP frequency configuration register 2.	Section 8.2.20
1Dh	HS_HEAT_OUT_CNFG	High-side and heater driver output configuration register.	Section 8.2.21
1Eh	HS_OC_CNFG	High-side driver overcurrent threshold configuration register.	Section 8.2.22
1Fh	HS_OL_CNFG	High-side driver open load threshold configuration register.	Section 8.2.23
20h	HS_REG_CNFG1	High-side driver regulation configuration register.	Section 8.2.24
21h	HS_REG_CNFG2	High-side driver regulation configuration register.	Section 8.2.25
22h	HS_PWM_FREQ_CNFG	High-side driver PWM generator frequency configuration register.	Section 8.2.26
23h	HEAT_CNFG	Heater configuration register.	Section 8.2.27
24h	EC_CNFG	Electrochrome configuration register.	Section 8.2.28
25h	HS_OCP_DG	High-side driver regulation configuration register.	Section 8.2.29
26h	SPARE_CNFG2	Spare configuration 2.	Section 8.2.30
27h	SPARE_CNFG3	Spare configuration 3.	Section 8.2.31
28h	SPARE_CNFG4	Spare configuration 4.	Section 8.2.32

Complex bit access types are encoded to fit into small table cells. Table 8-15 shows the codes that are used for access types in this section.

Table 8-15. DRV8000-Q1_CNFG Access Type Codes

Access Type	Code	Description
Read Type		

**Table 8-15. DRV8000-Q1_CNFG Access Type Codes
(continued)**

Access Type	Code	Description
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.2.1 IC_CNFG1 Register (Offset = 9h) [Reset = 0002h]

IC_CNFG1 is shown in [Table 8-16](#).

Return to the [Summary Table](#).

Includes configurations charge pump and watchdog, and fault levels and reactions for supply, charge pump, thermal, and watch dog faults.

Table 8-16. IC_CNFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OTSD_MODE	R/W	0h	Sets overtemperature shutdown behavior. If any thermal cluster reaches OT, the device either shuts down all drivers or affected drivers only (drivers in zone 3, for example). 0b = Global shutdown. 1b = Affected driver shutdown only.
14	DIS_CP	R/W	0h	When EN_GD = 0, the charge pump can be disabled, putting the device in a communication only mode. 0b = Charge pump enabled. 1b = Charge pump disabled.
13-12	PVDD_OV_MODE	R/W	0h	PVDD supply overvoltage monitor mode. 00b = Latched fault. 01b = Automatic recovery. 10b = Warning report only. 11b = Disabled.
11-10	PVDD_OV_DG	R/W	0h	PVDD supply overvoltage monitor deglitch time. 00b = 1µs 01b = 2µs 10b = 4µs 11b = 8µs
9	PVDD_OV_LVL	R/W	0h	PVDD supply overvoltage monitor threshold. 0b = 21.5V 1b = 28.5V
8	VCP_UV_LVL	R/W	0h	VCP charge pump undervoltage monitor threshold. 0b = 4.75V 1b = 6.25V
7-6	CP_MODE	R/W	0h	Charge pump operating mode. 00b = Automatic switch between tripler and doubler mode. 01b = Always doubler mode. 10b = Always tripler mode. 11b = RSVD
5	VCP_UV_MODE	R/W	0h	VCP charge pump undervoltage monitor mode. 0b = Latched fault. 1b = Automatic recovery.
4	PVDD_UV_MODE	R/W	0h	PVDD supply undervoltage monitor mode. 0b = Latched fault. 1b = Automatic recovery.
3	WD_EN	R/W	0h	Watchdog timer enable. 0b = Watchdog timer disabled. 1b = Watchdog timer enabled.
2	WD_FLT_M	R/W	0h	Watchdog fault mode. Watchdog fault is cleared by CLR_FLT. 0b = Watchdog fault is reported to WD_FLT and WARN register bits. Drivers remain enabled and FAULT bit is not asserted. 1b = Watchdog fault is reported to WD_FLT and FAULT register bits. All drivers are disabled in response to watchdog fault.
1	WD_WIN	R/W	1h	Watchdog timer window. 0b = 4 to 40ms 1b = 10 to 100ms

Table 8-16. IC_CNFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	EN_SSC	R/W	0h	Spread spectrum clocking. 0b = Disabled. 1b = Enabled.

8.2.2 IC_CNFG2 Register (Offset = Ah) [Reset = 0000h]

IC_CNFG2 is shown in [Table 8-17](#).

Return to the [Summary Table](#).

Includes thermal cluster warning disable bits.

Table 8-17. IC_CNFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	ZONE4_OTW_H_DIS	R/W	0h	Disables the high overtemperature warning for zone 4. Enabled = 0b Disabled = 1b
6	ZONE3_OTW_H_DIS	R/W	0h	Disables the high overtemperature warning for zone 3. Enabled = 0b Disabled = 1b
5	ZONE2_OTW_H_DIS	R/W	0h	Disables the high overtemperature warning for zone 2. Enabled = 0b Disabled = 1b
4	ZONE1_OTW_H_DIS	R/W	0h	Disables the high overtemperature warning for zone 1. Enabled = 0b Disabled = 1b
3	ZONE4_OTW_L_DIS	R/W	0h	Disables the low overtemperature warning for zone 4. Enabled = 0b Disabled = 1b
2	ZONE3_OTW_L_DIS	R/W	0h	Disables the low overtemperature warning for zone 3. Enabled = 0b Disabled = 1b
1	ZONE2_OTW_L_DIS	R/W	0h	Disables the low overtemperature warning for zone 2. Enabled = 0b Disabled = 1b
0	ZONE1_OTW_L_DIS	R/W	0h	Disables the low overtemperature warning for zone 1. Enabled = 0b Disabled = 1b

8.2.3 GD_CNFG Register (Offset = Bh) [Reset = 0000h]

GD_CNFG is shown in [Table 8-18](#).

Return to the [Summary Table](#).

General gate driver controls. Includes gate driver enable, bridge configuration, input pin modes, and open load enable.

Table 8-18. GD_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	IDRV_LO1	R/W	0h	Enable low current IDRVN and IDRVP mode for half-bridge 1. 0b = IDRVP_1 and IDRVN_1 utilize standard values. 1b = IDRVP_1 and IDRVN_1 utilize low current values.
12	IDRV_LO2	R/W	0h	Enable low current IDRVN and IDRVP mode for half-bridge 2. 0b = IDRVP_2 and IDRVN_2 utilize standard values. 1b = IDRVP_2 and IDRVN_2 utilize low current values.
11	PU_SH_1	R/W	0h	Gate driver 1 pull up diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
10	PD_SH_1	R/W	0h	Gate driver 1 pull down diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
9	PU_SH_2	R/W	0h	Gate driver 2 pull up diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
8	PD_SH_2	R/W	0h	Gate driver 2 pull down diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
7	RESERVED	R	0h	Reserved
6	IN2_MODE	R/W	0h	Sets gate driver 2 control source. 0b = Input pin IN2. 1b = SPI control bit S_IN2.
5	IN1_MODE	R/W	0h	Sets gate driver 1 control source. 0b = Input pin IN1. 1b = SPI control bit S_IN1.
4	BRG_FW	R/W	0h	Gate driver 1 and 2 control freewheeling setting. Settings shared between half-bridges 1 and 2. 0b = Low-side freewheeling. 1b = High-side freewheeling.
3-2	BRG_MODE	R/W	0h	Gate driver 1 and 2 input control mode. 00b = Independent half-bridge input control. 01b = PH/EN H-bridge input control. 10b = PWM H-bridge input control.
1	EN_OLSC	R/W	0h	Offline open load and short circuit diagnostic enable. 0b = Disabled. 1b = VDS monitors set into real-time voltage monitor mode and diagnostics current sources enabled.
0	EN_GD	R/W	0h	Enable gate driver bit 0b = Driver inputs are ignored and the gate driver passive pull-downs are enabled. 1b = Gate driver outputs are enabled and controlled by the digital inputs.

8.2.4 GD_IDRV_CNFG Register (Offset = Ch) [Reset = FFFFh]

GD_IDRV_CNFG is shown in [Table 8-19](#).

Return to the [Summary Table](#).

Includes IDRV drive current levels for each half-bridge gate driver.

Table 8-19. GD_IDRV_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	IDRVP_1	R/W	Fh	Gate driver 1 peak source pull up current. Alternative low current value in parenthesis (IDRV_LO1). 0000b = 0.5mA (50μA) 0001b = 1mA (110μA) 0010b = 2mA (170μA) 0011b = 3mA (230μA) 0100b = 4mA (290μA) 0101b = 5mA (350μA) 0110b = 6mA (410μA) 0111b = 7mA (600μA) 1000b = 8mA (725μA) 1001b = 12mA (850μA) 1010b = 16mA (1mA) 1011b = 20mA (1.2mA) 1100b = 24mA (1.4mA) 1101b = 31mA (1.6mA) 1110b = 48mA (1.8mA) 1111b = 62mA (2.3mA)
11-8	IDRVN_1	R/W	Fh	Gate driver 1 peak sink pull down current. Alternative low current value in parenthesis (IDRV_LO1). 0000b = 0.5mA (50μA) 0001b = 1mA (110μA) 0010b = 2mA (170μA) 0011b = 3mA (230μA) 0100b = 4mA (290μA) 0101b = 5mA (350μA) 0110b = 6mA (410μA) 0111b = 7mA (600μA) 1000b = 8mA (725μA) 1001b = 12mA (850μA) 1010b = 16mA (1mA) 1011b = 20mA (1.2mA) 1100b = 24mA (1.4mA) 1101b = 31mA (1.6mA) 1110b = 48mA (1.8mA) 1111b = 62mA (2.3mA)
7-4	IDRVP_2	R/W	Fh	Gate driver 2 peak source pull up current. Alternative low current value in parenthesis (IDRV_LO2). 0000b = 0.5mA (50μA) 0001b = 1mA (110μA) 0010b = 2mA (170μA) 0011b = 3mA (230μA) 0100b = 4mA (290μA) 0101b = 5mA (350μA) 0110b = 6mA (410μA) 0111b = 7mA (600μA) 1000b = 8mA (725μA) 1001b = 12mA (850μA) 1010b = 16mA (1mA) 1011b = 20mA (1.2mA) 1100b = 24mA (1.4mA) 1101b = 31mA (1.6mA) 1110b = 48mA (1.8mA) 1111b = 62mA (2.3mA)

Table 8-19. GD_IDRV_CNFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	IDRVN_2	R/W	Fh	Gate driver 2 peak sink pull down current. Alternative low current value in parenthesis (IDRV_LO2). 0000b = 0.5mA (50µA) 0001b = 1mA (110µA) 0010b = 2mA (170µA) 0011b = 3mA (230µA) 0100b = 4mA (290µA) 0101b = 5mA (350µA) 0110b = 6mA (410µA) 0111b = 7mA (600µA) 1000b = 8mA (725µA) 1001b = 12mA (850µA) 1010b = 16mA (1mA) 1011b = 20mA (1.2mA) 1100b = 24mA (1.4mA) 1101b = 31mA (1.6mA) 1110b = 48mA (1.8mA) 1111b = 62mA (2.3mA)

8.2.5 GD_VGS_CNFG Register (Offset = Dh) [Reset = 0030h]

GD_VGS_CNFG is shown in [Table 8-20](#).

Return to the [Summary Table](#).

VGS fault detection configurations.

Table 8-20. GD_VGS_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	VGS_IND	R/W	0h	VGS independent shutdown mode enable. Active for BRG_MODE = 00b, 11b. 0b = Disabled. 1b = Enabled. VGS gate fault only shutdown the associated half-bridge.
10-9	VGS_TDEAD	R/W	0h	Insertable digital dead-time. 00b = 0ns 01b = 2µs 10b = 4µs 11b = 8µs
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6-4	VGS_TDRV	R/W	3h	VGS drive time and VDS monitor blanking time. 000b = 2µs 001b = 4µs 010b = 8µs 011b = 12µs 100b = 16µs 101b = 24µs 110b = 32µs 111b = 96µs
3	VGS_HS_DIS	R/W	0h	VGS monitor based dead-time handshake. 0b = Enabled. 1b = Disabled. Gate drive transition based on tDRIVE and tDEAD time duration
2	VGS_LVL	R/W	0h	VGS monitor threshold for dead-time handshake and gate fault detection. 0b = 1.4V. 1b = 1.0V
1-0	VGS_MODE	R/W	0h	VGS gate fault monitor mode. 00b = Latched fault. 01b = Cycle by cycle. 10b = Warning report only. 11b = Disabled.

8.2.6 GD_VDS_CNFG Register (Offset = Eh) [Reset = 0D2Dh]

GD_VDS_CNFG is shown in [Table 8-21](#).

Return to the [Summary Table](#).

VDS monitoring or short-circuit detection configuration register.

Table 8-21. GD_VDS_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RSVD	R/W	0h	Reserved.
14	VDS_IND	R/W	0h	VDS fault independent shutdown mode configuration. 0b = Disabled. VDS fault shuts down all gate drivers. 1b = Enabled. VDS gate fault only shutdowns the associated gate driver.
13-12	VDS_IDRVN	R/W	0h	IDRVN gate pulldown current after VDS_OCP fault for gate driver 1 and 2. 00b = Programmed IDRVN 01b = 8mA 10b = 31mA 11b = 62mA
11-8	VDS_LVL_1	R/W	Dh	Gate Driver 1 HS and LS VDS overcurrent monitor threshold. 0000b = 0.06V 00001b = 0.08V 0010b = 0.10V 0011b = 0.12V 0100b = 0.14V 0101b = 0.16V 0110b = 0.18V 0111b = 0.2V 1000b = 0.3V 1001b = 0.4V 1010b = 0.5V 1011b = 0.6V 1100b = 0.7V 1101b = 1V 1110b = 1.4V 1111b = 2V
7-6	VDS_MODE	R/W	0h	VDS overcurrent monitor mode. 00b = Latched fault. 01b = Cycle by cycle. 10b = Warning report only. 11b = Disabled.
5-4	VDS_DG	R/W	2h	VDS overcurrent monitor deglitch time. 00b = 1μs 01b = 2μs 10b = 4μs 11b = 8μs

Table 8-21. GD_VDS_CNFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	VDS_LVL_2	R/W	Dh	Gate Driver 2 HS and LS VDS overcurrent monitor threshold. 0000b = 0.06V 0001b = 0.08V 0010b = 0.10V 0011b = 0.12V 0100b = 0.14V 0101b = 0.16V 0110b = 0.18V 0111b = 0.2V 1000b = 0.3V 1001b = 0.4V 1010b = 0.5V 1011b = 0.6V 1100b = 0.7V 1101b = 1V 1110b = 1.4V 1111b = 2V

8.2.7 GD_CSA_CNFG Register (Offset = Fh) [Reset = 0004h]

GD_CSA_CNFG is shown in [Table 8-22](#).

Return to the [Summary Table](#).

CSA configurations and controls.

Table 8-22. GD_CSA_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7-5	CSA_BLK	R/W	0h	Current shunt amplifier blanking time. % of tDRV. 000b = 0 %, Disabled 001b = 25 % 010b = 37.5 % 011b = 50 % 100b = 62.5 % 101b = 75 % 110b = 87.5 % 111b = 100 %
4	CSA_BLK_SEL	R/W	0h	Current shunt amplifier blanking trigger source. 0b = Gate driver 1 1b = Gate driver 2
3-2	CSA_GAIN	R/W	1h	Current shunt amplifier gain setting. 00b = 10V/V 01b = 20V/V 10b = 40V/V 11b = 80V/V
1	CSA_DIV	R/W	0h	Current shunt amplifier internal reference voltage divider. 0b = VREF / 2 1b = VREF / 8
0	RESERVED	R	0h	Reserved

8.2.8 GD_AGD_CNFG Register (Offset = 10h) [Reset = 0402h]

GD_AGD_CNFG is shown in [Table 8-23](#).

Return to the [Summary Table](#).

Includes Advanced smart gate driver configurations, enables for DCC and PDR, post-charge settings.

Table 8-23. GD_AGD_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	PDR_ERR	R/W	0h	PDR loop error limit for gate driver 1 and 2. 0b = 1-bit error 1b = Actual error
13-12	AGD_ISTRONG	R/W	0h	Adaptive gate driver ISTRONG configuration. 00b = ISTRONG pull-down decoded from initial IDRVP_x register setting. 01b = 62mA 10b = 124mA 11b = RSVD
11-10	AGD_THR	R/W	1h	Adaptive gate driver VSH threshold configuration. 00b = 1V, VPVDD - 0.5V 01b = 1V, VPVDD - 1V 10b = 2V, VPVDD - 1.5V 11b = 2V, VPVDD - 2V
9	SET_AGD	R/W	0h	Set active half-bridge for adaptive gate drive control loops. 0b = Gate driver 1 1b = Gate driver 2
8	FW_MAX	R/W	0h	Gate drive current used for freewheeling MOSFET for gate driver 1 and 2. 0b = PRE_CHR_MAX_12 [1:0] 1b = 64mA
7	EN_DCC	R/W	0h	Enable duty cycle compensation for half-bridge 1 and 2.
6	IDIR_MAN	R/W	0h	Current polarity detection mode for half-bridge 1 and 2. 0b = Automatic 1b = Manual (Set by HBx_HL)
5-4	KP_PST	R/W	0h	Post charge proportional control gain setting for half-bridges 1 and 2. 00b = Disabled 01b = 2 10b = 4 11b = 15
3	EN_PST_DLY	R/W	0h	Enable post-charge time delay. Time delay is equal to T_DON_DOFF_12 - T_PRE_CHR_12.
2-1	KP_PDR	R/W	1h	PDR proportional controller gain setting for half-bridge 1 and 2. 00b = 1 01b = 2 10b = 3 11b = 4
0	EN_PDR	R/W	0h	Enable PDR loop control for half-bridge 1 and 2.

8.2.9 GD_PDR_CNFG Register (Offset = 11h) [Reset = 0AF6h]

GD_PDR_CNFG is shown in [Table 8-24](#).

Return to the [Summary Table](#).

Includes remaining PDR controls, pre-charge settings and timing.

Table 8-24. GD_PDR_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	PRE_MAX	R/W	0h	Maximum gate drive current limit for pre-charge and pre-discharge for half-bridge 1 and 2. 00b = 64mA 01b = 32mA 10b = 16mA 11b = 8mA
13-8	T_DON_DOFF	R/W	Ah	On and off time delay for half-bridge 1 and 2. 140ns x T_DON_DOFF [3:0] Default time: 001010b (1.4us)
7-6	T_PRE_CHR	R/W	3h	PDR control loop pre-charge time for half-bridge 1 and 2. Set as ratio of T_DON_DOFF_12 [5:0] 00b = 1/8 01b = 1/4 10b = 3/8 11b = 1/2
5-4	T_PRE_DCHR	R/W	3h	PDR control loop pre-discharge time for half-bridge 1 and 2. Set as ratio of T_DON_DOFF_12 [5:0] 00b = 1/8 01b = 1/4 10b = 3/8 11b = 1/2
3-2	PRE_CHR_INIT	R/W	1h	PDR control loop initial pre-charge current setting for half-bridge 1 and 2. 00b = 4mA 01b = 8mA 10b = 16mA 11b = 32mA
1-0	PRE_DCHR_INIT	R/W	2h	PDR control loop initial pre-discharge current setting for half-bridge 1 and 2. 00b = 4mA 01b = 8mA 10b = 16mA 11b = 32mA

8.2.10 GD_STC_CNFG Register (Offset = 12h) [Reset = 0026h]

GD_STC_CNFG is shown in [Table 8-25](#).

Return to the [Summary Table](#).

Includes configurations and enable for slew time control.

Table 8-25. GD_STC_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7-4	T_RISE_FALL	R/W	2h	Set switch-node VSH rise and fall time for half-bridge 1 and 2. 0000b = 0.35us 0001b = 0.56us 0010b = 0.77us 0011b = 0.98us 0100b = 1.33us 0101b = 1.68us 0110b = 2.03us 0111b = 2.45us 1000b = 2.94us 1001b = 3.99us 1010b = 4.97us 1011b = 5.95us 1100b = 7.98us 1101b = 9.94us 1110b = 11.97us 1111b = 15.96us
3	STC_ERR	R/W	0h	STC loop error limit for half-bridge 1 and 2 0b = 1-bit error 1b = Actual error
2-1	KP_STC	R/W	3h	STC proportional controller gain setting for half-bridge 1 and 2. 00b = 1 01b = 2 10b = 3 11b = 4
0	EN_STC	R/W	0h	Enable STC loop control for half-bridge 1 and 2.

8.2.11 GD_SPARE_CNFG1 Register (Offset = 13h) [Reset = 0000h]

GD_SPARE_CNFG1 is shown in [Table 8-26](#).

Return to the [Summary Table](#).

Spare configuration register for gate driver.

Table 8-26. GD_SPARE_CNFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

8.2.12 HB_ITRIP_DG Register (Offset = 14h) [Reset = 0000h]

HB_ITRIP_DG is shown in [Table 8-27](#).

Return to the [Summary Table](#).

Configures ITRIP deglitch for each half-bridge. ITRIP timing is shared between half-bridge pairs.

Table 8-27. HB_ITRIP_DG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11-10	OUT6_ITRIP_DG	R/W	0h	Configures ITRIP deglitch time for half-bridge 6. 00b = 2μs 01b = 5μs 10b = 10μs 11b = 20μs
9-8	OUT5_ITRIP_DG	R/W	0h	Configures ITRIP deglitch time for half-bridge 5. 00b = 2μs 01b = 5μs 10b = 10μs 11b = 20μs
7-6	OUT4_ITRIP_DG	R/W	0h	Configures ITRIP deglitch time for half-bridge 4. 00b = 2μs 01b = 5μs 10b = 10μs 11b = 20μs
5-4	OUT3_ITRIP_DG	R/W	0h	Configures ITRIP deglitch time for half-bridge 3. 00b = 2μs 01b = 5μs 10b = 10μs 11b = 20μs
3-2	OUT2_ITRIP_DG	R/W	0h	Configures ITRIP deglitch time for half-bridge 2. 00b = 2μs 01b = 5μs 10b = 10μs 11b = 20μs
1-0	OUT1_ITRIP_DG	R/W	0h	Configures ITRIP deglitch time for half-bridge 1. 00b = 2μs 01b = 5μs 10b = 10μs 11b = 20μs

8.2.13 HB_OUT_CNFG1 Register (Offset = 15h) [Reset = 0000h]

HB_OUT_CNFG1 is shown in [Table 8-28](#).

Return to the [Summary Table](#).

Configures the output mode for each half-bridge, sets IPROPI sample and hold circuit, and half-bridge pair freewheeling.

Table 8-28. HB_OUT_CNFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RSVD	R/W	0h	Reserved.
14	NSR_OUT6_DIS	R/W	0h	Disables non-synchronous rectification during ITRIP regulation (sets active freewheeling) for half-bridge 6. Passive freewheeling = 0b Active freewheeling = 1b
13	NSR_OUT5_DIS	R/W	0h	Disables non-synchronous rectification during ITRIP regulation (sets active freewheeling) for half-bridge 5. Passive freewheeling = 0b Active freewheeling = 1b
12	NSR_OUT4_DIS	R/W	0h	Disables non-synchronous rectification during ITRIP regulation (sets active freewheeling) for half-bridge 4. Passive freewheeling = 0b Active freewheeling = 1b
11	NSR_OUT3_DIS	R/W	0h	Disables non-synchronous rectification during ITRIP regulation (sets active freewheeling) for half-bridges 3. Passive freewheeling = 0b Active freewheeling = 1b
10	NSR_OUT2_DIS	R/W	0h	Disables non-synchronous rectification during ITRIP regulation (sets active freewheeling) for half-bridge 2. Passive freewheeling = 0b Active freewheeling = 1b
9	NSR_OUT1_DIS	R/W	0h	Disables non-synchronous rectification during ITRIP regulation (sets active freewheeling) for half-bridge 1. Passive freewheeling = 0b Active freewheeling = 1b
8	IPROPI_SH_EN	R/W	0h	Enables IPROPI sample and hold circuit.
7	RSVD_7	R/W	0h	Reserved.
6	RSVD_6	R/W	0h	Reserved.
5-3	OUT6_CNFG	R/W	0h	Configuration for half-bridge 6. Enables or disables control of half-bridge, and sets control mode between PWM or SPI. 000b = Disabled 001b = Enabled (SPI register control) 010b = PWM1 Complementary Control 011b = PWM1 LS Control 100b = PWM1 HS Control 101b = PWM2 Complementary Control 110b = PWM2 PWM LS Control 111b = PWM2 HS Control
2-0	OUT5_CNFG	R/W	0h	Configuration for half-bridge 5. Enables or disables control of half-bridge, and sets control mode between PWM or SPI. 000b = Disabled 001b = Enabled (SPI register control) 010b = PWM1 Complementary Control 011b = PWM1 LS Control 100b = PWM1 HS Control 101b = PWM2 Complementary Control 110b = PWM2 PWM LS Control 111b = PWM2 HS Control

8.2.14 HB_OUT_CNFG2 Register (Offset = 16h) [Reset = 0000h]

HB_OUT_CNFG2 is shown in [Table 8-29](#).

Return to the [Summary Table](#).

Configures the output mode for each half-bridge.

Table 8-29. HB_OUT_CNFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RSVD_15	R/W	0h	Reserved.
14	RSVD_14	R/W	0h	Reserved.
13-11	OUT4_CNFG	R/W	0h	Configuration for half-bridge 4. Enables or disables control of half-bridge, and sets control mode between PWM or SPI. 000b = Disabled 001b = Enabled (SPI register control) 010b = PWM1 Complementary Control 011b = PWM1 LS Control 100b = PWM1 HS Control 101b = PWM2 Complementary Control 110b = PWM2 PWM LS Control 111b = PWM2 HS Control
10-8	OUT3_CNFG	R/W	0h	Configuration for half-bridge 3. Enables or disables control of half-bridge, and sets control mode between PWM or SPI. 000b = Disabled 001b = Enabled (SPI register control) 010b = PWM1 Complementary Control 011b = PWM1 LS Control 100b = PWM1 HS Control 101b = PWM2 Complementary Control 110b = PWM2 PWM LS Control 111b = PWM2 HS Control
7	RSVD_7	R/W	0h	Reserved.
6	RSVD_6	R/W	0h	Reserved.
5-3	OUT2_CNFG	R/W	0h	Configuration for half-bridge 2. Enables or disables control of half-bridge, and sets control mode between PWM or SPI. 000b = Disabled 001b = Enabled (SPI register control) 010b = PWM1 Complementary Control 011b = PWM1 LS Control 100b = PWM1 HS Control 101b = PWM2 Complementary Control 110b = PWM2 PWM LS Control 111b = PWM2 HS Control
2-0	OUT1_CNFG	R/W	0h	Configuration for half-bridge 1. Enables or disables control of half-bridge, and sets control mode between PWM or SPI. 000b = Disabled 001b = Enabled (SPI register control) 010b = PWM1 Complementary Control 011b = PWM1 LS Control 100b = PWM1 HS Control 101b = PWM2 Complementary Control 110b = PWM2 PWM LS Control 111b = PWM2 HS Control

8.2.15 HB_OCP_CNFG Register (Offset = 17h) [Reset = 0000h]

HB_OCP_CNFG is shown in [Table 8-30](#).

Return to the [Summary Table](#).

Overcurrent deglitch for half-bridges configuration register.

Table 8-30. HB_OCP_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RSVD	R/W	0h	Reserved.
14	RSVD	R/W	0h	Reserved.
13	RSVD	R/W	0h	Reserved.
12	RSVD	R/W	0h	Reserved.
11-10	OUT6_OCP_DG	R/W	0h	Overcurrent deglitch time for half-bridge 6. 00b = 6μs 01b = 10μs 10b = 20μs 11b = 60μs
9-8	OUT5_OCP_DG	R/W	0h	Overcurrent deglitch time for half-bridge 5. 00b = 6μs 01b = 10μs 10b = 20μs 11b = 60μs
7-6	OUT4_OCP_DG	R/W	0h	Overcurrent deglitch time for half-bridge 4. 00b = 6μs 01b = 10μs 10b = 20μs 11b = 60μs
5-4	OUT3_OCP_DG	R/W	0h	Overcurrent deglitch time for half-bridge 3. 00b = 6μs 01b = 10μs 10b = 20μs 11b = 60μs
3-2	OUT2_OCP_DG	R/W	0h	Overcurrent deglitch time for half-bridge 2. 00b = 6μs 01b = 10μs 10b = 20μs 11b = 60μs
1-0	OUT1_OCP_DG	R/W	0h	Overcurrent deglitch time for half-bridge 1. 00b = 6μs 01b = 10μs 10b = 20μs 11b = 60μs

8.2.16 HB_OL_CNFG1 Register (Offset = 18h) [Reset = 0000h]

HB_OL_CNFG1 is shown in [Table 8-31](#).

Return to the [Summary Table](#).

Configures active and off-state open load detection circuits for half-bridges.

Table 8-31. HB_OL_CNFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RSVD_15	R/W	0h	Reserved.
14	RSVD_14	R/W	0h	Reserved.
13-12	HB_OLP_CNFG	R/W	0h	Off-state diagnostics configuration. 00b = Off-state disabled 01b = OUT X Pull-up enabled, OUT Y pull-down enabled, OUT Y selected, VREF Low 10b = OUT X Pull-up enabled, OUT Y pull-down enabled, OUT X selected, VREF High 11b = OUT X Pull-down enabled, OUT Y pull-up enabled, OUT Y selected, VREF Low
11-8	HB_OLP_SEL	R/W	0h	Off-state open load diagnostics enable for half-bridge 5. 0000b = Disabled 0001b = OUT1 and OUT2 0010b = OUT1 and OUT3 0011b = OUT1 and OUT4 0100b = OUT1 and OUT5 0101b = OUT1 and OUT6 0110b = OUT2 and OUT3 0111b = OUT2 and OUT4 1000b = OUT2 and OUT5 1001b = OUT2 and OUT6 1010b = OUT3 and OUT4 1011b = OUT3 and OUT5 1100b = OUT3 and OUT6 1101b = OUT4 and OUT5 1110b = OUT4 and OUT6 1111b = OUT5 and OUT6
7	RSVD_7	R/W	0h	Reserved.
6	RSVD_6	R/W	0h	Reserved.
5	OUT6_OLA_EN	R/W	0h	Active open load diagnostics enable for half-bridge 6. 0b = Enabled 1b = Disabled
4	OUT5_OLA_EN	R/W	0h	Active open load diagnostics enable for half-bridge 5. 0b = Enabled 1b = Disabled
3	OUT4_OLA_EN	R/W	0h	Active open load diagnostics enable for half-bridge 4. 0b = Enabled 1b = Disabled
2	OUT3_OLA_EN	R/W	0h	Active open load diagnostics enable for half-bridge 3. 0b = Enabled 1b = Disabled
1	OUT2_OLA_EN	R/W	0h	Active open load diagnostics enable for half-bridge 2. 0b = Enabled 1b = Disabled
0	OUT1_OLA_EN	R/W	0h	Active open load diagnostics enable for half-bridge 1. 0b = Enabled 1b = Disabled

8.2.17 HB_OL_CNFG2 Register (Offset = 19h) [Reset = 0000h]

HB_OL_CNFG2 is shown in [Table 8-32](#).

Return to the [Summary Table](#).

Configures cycle count threshold for active open load detection circuits of half-bridges.

Table 8-32. HB_OL_CNFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RSVD_15	R/W	0h	Reserved.
14	RSVD_14	R/W	0h	Reserved.
13	RSVD_13	R/W	0h	Reserved.
12	RSVD_12	R/W	0h	Reserved.
11	RSVD_11	R/W	0h	Reserved.
10	RSVD_10	R/W	0h	Reserved.
9	RSVD_9	R/W	0h	Reserved.
8	RSVD_8	R/W	0h	Reserved.
7	RSVD_7	R/W	0h	Reserved.
6	RSVD_6	R/W	0h	Reserved.
5	OUT6_OLA_TH	R/W	0h	Sets the half-bridge 6 active open load cycle count threshold. 0b = 32 cycles 1b = 128 cycles
4	OUT5_OLA_TH	R/W	0h	Sets the half-bridge 5 active open load cycle count threshold. 0b = 32 cycles 1b = 128 cycles
3	OUT4_OLA_TH	R/W	0h	Sets the half-bridge 4 active open load cycle count threshold. 0b = 32 cycles 1b = 128 cycles
2	OUT3_OLA_TH	R/W	0h	Sets the half-bridge 3 active open load cycle count threshold. 0b = 32 cycles 1b = 128 cycles
1	OUT2_OLA_TH	R/W	0h	Sets the half-bridge 2 active open load cycle count threshold. 0b = 32 cycles 1b = 128 cycles
0	OUT1_OLA_TH	R/W	0h	Sets the half-bridge 1 active open load cycle count threshold. 0b = 32 cycles 1b = 128 cycles

8.2.18 HB_SR_CNFG Register (Offset = 1Ah) [Reset = 0000h]

HB_SR_CNFG is shown in [Table 8-33](#).

Return to the [Summary Table](#).

Configures slew rate timing for each half-bridge.

Table 8-33. HB_SR_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RSVD_15	R/W	0h	Reserved.
14	RSVD_14	R/W	0h	Reserved.
13	RSVD_13	R/W	0h	Reserved.
12	RSVD_12	R/W	0h	Reserved.
11-10	OUT6_SR	R/W	0h	Configures slew rate for half-bridge 6. 00b = 1.6V/μs 01b = 10V/μs 10b = 20V/μs
9-8	OUT5_SR	R/W	0h	Configures slew rate for half-bridge 5. 00b = 1.6V/μs 01b = 10V/μs 10b = 20V/μs
7-6	OUT4_SR	R/W	0h	Configures slew rate for half-bridge 4. 00b = 1.6V/μs 01b = 10V/μs 10b = 20V/μs
5-4	OUT3_SR	R/W	0h	Configures slew rate for half-bridge 3. 00b = 1.6V/μs 01b = 10V/μs 10b = 20V/μs
3-2	OUT2_SR	R/W	0h	Configures slew rate for half-bridge 2. 00b = 1.6V/μs 01b = 10V/μs 10b = 20V/μs
1-0	OUT1_SR	R/W	0h	Configures slew rate for half-bridge 1. 00b = 1.6V/μs 01b = 10V/μs 10b = 20V/μs

8.2.19 HB_ITRIP_CNFG Register (Offset = 1Bh) [Reset = 0000h]

HB_ITRIP_CNFG is shown in [Table 8-34](#).

Return to the [Summary Table](#).

Configures ITRIP levels and enables ITRIP for each half-bridge. ITRIP levels are shared between half-bridge pairs.

Table 8-34. HB_ITRIP_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OUT6_ITRIP_EN	R/W	0h	Enables ITRIP regulation for half-bridge 6.
14	OUT5_ITRIP_EN	R/W	0h	Enables ITRIP regulation for half-bridge 5.
13	OUT4_ITRIP_EN	R/W	0h	Enables ITRIP regulation for half-bridge 4.
12	OUT3_ITRIP_EN	R/W	0h	Enables ITRIP regulation for half-bridge 3.
11	OUT2_ITRIP_EN	R/W	0h	Enables ITRIP regulation for half-bridge 2.
10	OUT1_ITRIP_EN	R/W	0h	Enables ITRIP regulation for half-bridge 1.
9-8	OUT6_ITRIP_LVL	R/W	0h	Configures ITRIP current threshold for half-bridge 6. 00b = 2.25A 01b = 5.5A 10b = 6.25A 11b = Reserved.
7-6	OUT5_ITRIP_LVL	R/W	0h	Configures ITRIP current threshold for half-bridge 5. 00b = 2.75A 01b = 6.5A 10b = 7.5A 11b = Reserved.
5-4	OUT4_ITRIP_LVL	R/W	0h	Configures ITRIP current threshold for half-bridge 4. 00b = 1.25A 01b = 2.75A 10b = 3.5A 11b = Reserved.
3-2	OUT3_ITRIP_LVL	R/W	0h	Configures ITRIP current threshold for half-bridge 3. 00b = 1.25A 01b = 2.5A 10b = 3.5A 11b = Reserved.
1	OUT2_ITRIP_LVL	R/W	0h	Configures ITRIP current threshold for half-bridge 2. 0b = 0.7A 1b = 0.875A
0	OUT1_ITRIP_LVL	R/W	0h	Configures ITRIP current threshold for half-bridge 1. 0b = 0.7A 1b = 0.875A

8.2.20 HB_ITRIP_FREQ Register (Offset = 1Ch) [Reset = 0000h]

HB_ITRIP_FREQ is shown in [Table 8-35](#).

Return to the [Summary Table](#).

Configures ITRIP frequency and deglitch for each half-bridge. ITRIP timing is shared between half-bridge pairs.

Table 8-35. HB_ITRIP_FREQ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RSVD_15	R/W	0h	Reserved.
14	RSVD_14	R/W	0h	Reserved.
13	RSVD_13	R/W	0h	Reserved.
12	RSVD_12	R/W	0h	Reserved.
11-10	OUT6_ITRIP_FREQ	R/W	0h	Configures ITRIP regulation frequency for half-bridge 6. 00b = 20kHz 01b = 10kHz 10b = 5kHz 11b = 2.5kHz
9-8	OUT5_ITRIP_FREQ	R/W	0h	Configures ITRIP regulation frequency for half-bridge 5. 00b = 20kHz 01b = 10kHz 10b = 5kHz 11b = 2.5kHz
7-6	OUT4_ITRIP_FREQ	R/W	0h	Configures ITRIP regulation frequency for half-bridge 4. 00b = 20kHz 01b = 10kHz 10b = 5kHz 11b = 2.5kHz
5-4	OUT3_ITRIP_FREQ	R/W	0h	Configures ITRIP regulation frequency for half-bridge 3. 00b = 20kHz 01b = 10kHz 10b = 5kHz 11b = 2.5kHz
3-2	OUT2_ITRIP_FREQ	R/W	0h	Configures ITRIP regulation frequency for half-bridge 2. 00b = 20kHz 01b = 10kHz 10b = 5kHz 11b = 2.5kHz
1-0	OUT1_ITRIP_FREQ	R/W	0h	Configures ITRIP regulation frequency for half-bridge 1. 00b = 20kHz 01b = 10kHz 10b = 5kHz 11b = 2.5kHz

8.2.21 HS_HEAT_OUT_CNFG Register (Offset = 1Dh) [Reset = 0000h]

HS_HEAT_OUT_CNFG is shown in [Table 8-36](#).

Return to the [Summary Table](#).

Configures the output mode for each high-side driver and heater.

Table 8-36. HS_HEAT_OUT_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	HEAT_OUT_CNFG	R/W	0h	Configuration for heater driver. Enables or disables control of heater, and sets control mode between PWM or SPI. 00b = Disabled 01b = SPI control enabled 10b = PWM pin control 11b = Reserved
13	RSVD_13	R/W	0h	Reserved.
12	RSVD_12	R/W	0h	Reserved.
11-10	OUT12_CNFG	R/W	0h	Configuration for high-side driver 12. Enables or disables control of high-side driver, and sets control mode between PWM or SPI. 00b = Disabled 01b = SPI control enabled 10b = PWM pin control 11b = PWM Generator
9-8	OUT11_CNFG	R/W	0h	Configuration for high-side driver 11. Enables or disables control of high-side driver, and sets control mode between PWM or SPI. 00b = Disabled 01b = SPI control enabled 10b = PWM pin control 11b = PWM Generator
7-6	OUT10_CNFG	R/W	0h	Configuration for high-side driver 10. Enables or disables control of high-side driver, and sets control mode between PWM or SPI. 00b = Disabled 01b = SPI control enabled 10b = PWM pin control 11b = PWM Generator
5-4	OUT9_CNFG	R/W	0h	Configuration for high-side driver 9. Enables or disables control of high-side driver, and sets control mode between PWM or SPI. 00b = Disabled 01b = SPI control enabled 10b = PWM pin control 11b = PWM Generator
3-2	OUT8_CNFG	R/W	0h	Configuration for high-side driver 8. Enables or disables control of high-side driver, and sets control mode between PWM or SPI. 00b = Disabled 01b = SPI control enabled 10b = PWM pin control 11b = PWM Generator
1-0	OUT7_CNFG	R/W	0h	Configuration for high-side driver 7. Enables or disables control of high-side driver, and sets control mode between PWM or SPI. 00b = Disabled 01b = SPI control enabled 10b = PWM pin control 11b = PWM Generator

8.2.22 HS_OC_CNFG Register (Offset = 1Eh) [Reset = 1000h]

HS_OC_CNFG is shown in [Table 8-37](#).

Return to the [Summary Table](#).

Configures overcurrent threshold for each high-side driver.

Table 8-37. HS_OC_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RSVD_15	R/W	0h	Reserved.
14	RSVD_14	R/W	0h	Reserved.
13	RSVD_13	R/W	0h	Reserved.
12	OUT11_EC_MODE	R/W	1h	Bit sets high-side OUT11 for independent control through OUT11_CNFG bits or for EC mode. Default configuration is for EC mode. OUT11_CNFG mode = 0b EC mode = 1b
11	RSVD_12	R/W	0h	Reserved.
10	RSVD_11	R/W	0h	Reserved.
9	RSVD_10	R/W	0h	Reserved.
8	RSVD_9	R/W	0h	Reserved.
7	RSVD_8	R/W	0h	Reserved.
6	RSVD_6	R/W	0h	Reserved.
5	OUT12_OC_TH	R/W	0h	Configures overcurrent threshold between high or low for high-side driver 12. 0b = Low current threshold 1b = High current threshold
4	OUT11_OC_TH	R/W	0h	Configures overcurrent threshold between high or low for high-side driver 11. 0b = Low current threshold 1b = High current threshold
3	OUT10_OC_TH	R/W	0h	Configures overcurrent threshold between high or low for high-side driver 10. 0b = Low current threshold 1b = High current threshold
2	OUT9_OC_TH	R/W	0h	Configures overcurrent threshold between high or low for high-side driver 9. 0b = Low current threshold 1b = High current threshold
1	OUT8_OC_TH	R/W	0h	Configures overcurrent threshold between high or low for high-side driver 8. 0b = Low current threshold 1b = High current threshold
0	OUT7_RDSON_MODE	R/W	0h	Configures high-side driver 7 between high RDSON mode and low RDSON mode (for bulb/lamp load). 0b = High RDSON mode (LED driver mode) 1b = Low RDSON mode (bulb/lamp driver mode)

8.2.23 HS_OL_CNFG Register (Offset = 1Fh) [Reset = 0000h]

HS_OL_CNFG is shown in [Table 8-38](#).

Return to the [Summary Table](#).

Configures open load threshold for each high-side driver.

Table 8-38. HS_OL_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RSVD_15	R/W	0h	Reserved.
14	RSVD_14	R/W	0h	Reserved.
13	OUT12_OLA_TH	R/W	0h	Configures high-side driver 12 open load threshold. 0b = Low threshold 1b = High threshold
12	OUT11_OLA_TH	R/W	0h	Configures high-side driver 11 open load threshold. 0b = Low threshold 1b = High threshold
11	OUT10_OLA_TH	R/W	0h	Configures high-side driver 10 open load threshold. 0b = Low threshold 1b = High threshold
10	OUT9_OLA_TH	R/W	0h	Configures high-side driver 9 open load threshold. 0b = Low threshold 1b = High threshold
9	OUT8_OLA_TH	R/W	0h	Configures high-side driver 8 open load threshold. 0b = Low threshold 1b = High threshold
8	OUT7_OLA_TH	R/W	0h	Configures high-side driver 7 open load threshold. 0b = Low threshold 1b = High threshold
7	RSVD_7	R/W	0h	Reserved.
6	RSVD_6	R/W	0h	Reserved.
5	OUT12_OLA_EN	R/W	0h	Enables open load detection circuit for high-side driver 12.
4	OUT11_OLA_EN	R/W	0h	Enables open load detection circuit for high-side driver 11.
3	OUT10_OLA_EN	R/W	0h	Enables open load detection circuit for high-side driver 10.
2	OUT9_OLA_EN	R/W	0h	Enables open load detection circuit for high-side driver 9.
1	OUT8_OLA_EN	R/W	0h	Enables open load detection circuit for high-side driver 8.
0	OUT7_OLA_EN	R/W	0h	Enables open load detection circuit for high-side driver 7.

8.2.24 HS_REG_CNFG1 Register (Offset = 20h) [Reset = 0000h]

HS_REG_CNFG1 is shown in [Table 8-39](#).

Return to the [Summary Table](#).

Configures OUT7 ITRIP settings.

Table 8-39. HS_REG_CNFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	OUT7_OCP_DIS	R/W	0h	Disables second current limit of 2.5A on OUT7 in low RDSOn mode. 0b = OUT7 OCP enable 1b = OUT7 OCP disable
9-8	ITRIP_TO_SEL	R/W	0h	Selects the timeout limit for OUT7 ITRIP regulation. 00b = 100ms 01b = 200ms 10b = 400ms 11b = 800ms
7-6	OUT7_ITRIP_CNFG	R/W	0h	Configures OUT7 ITRIP behavior, fault clearing and latching. 00b = ITRIP fault report only 01b = ITRIP regulation with timeout and driver disable 10b = ITRIP regulation always 11b = ITRIP regulation with timeout and regulation disable
5-4	OUT7_ITRIP_BLK	R/W	0h	Configures OUT7 ITRIP blanking time. 00b = Reserved. 01b = 0μs 10b = 20μs 11b = 40μs
3-2	OUT7_ITRIP_FREQ	R/W	0h	Configures OUT7 ITRIP regulation frequency. 00b = 1.7kHz 01b = 2.2kHz 10b = 3kHz 11b = 4.4kHz
1-0	OUT7_ITRIP_DG	R/W	0h	Configures OUT7 ITRIP deglitch time. 00b = 48μs 01b = 40μs 10b = 32μs 11b = 24μs

8.2.25 HS_REG_CNFG2 Register (Offset = 21h) [Reset = 0000h]

HS_REG_CNFG2 is shown in [Table 8-40](#).

Return to the [Summary Table](#).

Configures constant current mode for each high-side driver.

Table 8-40. HS_REG_CNFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	OUT12_CCM_TO	R/W	0h	Configures the constant current mode timing and current limit option of high-side output 12. 200mA for 20ms = 0b 390mA for 10ms = 1b
12	OUT11_CCM_TO	R/W	0h	Configures the constant current mode timing and current limit option of high-side output 11. 200mA for 20ms = 0b 390mA for 10ms = 1b
11	OUT10_CCM_TO	R/W	0h	Configures the constant current mode timing and current limit option of high-side output 10. 200mA for 20ms = 0b 390mA for 10ms = 1b
10	OUT9_CCM_TO	R/W	0h	Configures the constant current mode timing and current limit option of high-side output 9. 200mA for 20ms = 0b 390mA for 10ms = 1b
9	OUT8_CCM_TO	R/W	0h	Configures the constant current mode timing and current limit option of high-side output 8. 200mA for 20ms = 0b 390mA for 10ms = 1b
8	OUT7_CCM_TO	R/W	0h	Configures the constant current mode timing and current limit option of high-side output 7. 200mA for 20ms = 0b 390mA for 10ms = 1b
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	OUT12_CCM_EN	R/W	0h	Enables constant current mode circuit for high-side driver 12.
4	OUT11_CCM_EN	R/W	0h	Enables constant current mode circuit for high-side driver 11.
3	OUT10_CCM_EN	R/W	0h	Enables constant current mode circuit for high-side driver 10.
2	OUT9_CCM_EN	R/W	0h	Enables constant current mode circuit for high-side driver 9.
1	OUT8_CCM_EN	R/W	0h	Enables constant current mode circuit for high-side driver 8.
0	OUT7_CCM_EN	R/W	0h	Enables constant current mode circuit for high-side driver 7.

8.2.26 HS_PWM_FREQ_CNFG Register (Offset = 22h) [Reset = 0000h]

HS_PWM_FREQ_CNFG is shown in [Table 8-41](#).

Return to the [Summary Table](#).

Configures the frequency for each dedicated PWM generator.

Table 8-41. HS_PWM_FREQ_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11-10	PWM_OUT12_FREQ	R/W	0h	Configures frequency output of dedicated PWM generator for high-side driver 12. 00b = 108Hz 01b = 217Hz 10b = 289Hz 11b = Reserved
9-8	PWM_OUT11_FREQ	R/W	0h	Configures frequency output of dedicated PWM generator for high-side driver 11. 00b = 108Hz 01b = 217Hz 10b = 289Hz 11b = Reserved
7-6	PWM_OUT10_FREQ	R/W	0h	Configures frequency output of dedicated PWM generator for high-side driver 10. 00b = 108Hz 01b = 217Hz 10b = 289Hz 11b = Reserved
5-4	PWM_OUT9_FREQ	R/W	0h	Configures frequency output of dedicated PWM generator for high-side driver 9. 00b = 108Hz 01b = 217Hz 10b = 289Hz 11b = Reserved
3-2	PWM_OUT8_FREQ	R/W	0h	Configures frequency output of dedicated PWM generator for high-side driver 8. 00b = 108Hz 01b = 217Hz 10b = 289Hz 11b = Reserved
1-0	PWM_OUT7_FREQ	R/W	0h	Configures frequency output of dedicated PWM generator for high-side driver 7. 00b = 108Hz 01b = 217Hz 10b = 289Hz 11b = Reserved

8.2.27 HEAT_CNFG Register (Offset = 23h) [Reset = 0A3Ch]

HEAT_CNFG is shown in [Table 8-42](#).

Return to the [Summary Table](#).

Configures heater driver and fault responses.

Table 8-42. HEAT_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11-8	HEAT_VDS_LVL	R/W	Ah	Heater MOSFET VDS monitor protection threshold. 0000b = 0.06V 00001b = 0.08V 0010b = 0.10V 0011b = 0.12V 0100b = 0.14V 0101b = 0.16V 0110b = 0.18V 0111b = 0.2V 1000b = 0.24V 1001b = 0.28V 1010b = 0.32V 1011b = 0.36V 1100b = 0.4V 1101b = 0.44V 1110b = 0.56V 1111b = 1V
7-6	HEAT_VDS_MODE	R/W	0h	Heater MOSFET VDS overcurrent monitor fault mode. 00b = Latched fault. 01b = Cycle by cycle. 10b = Warning report only. 11b = Disabled.
5-4	HEAT_VDS_BLK	R/W	3h	Heater MOSFET VDS monitor blanking time. 00b = 4μs 01b = 8μs 10b = 16μs 11b = 32μs
3-2	HEAT_VDS_DG	R/W	3h	Heater MOSFET VDS overcurrent monitor deglitch time. 00b = 1μs 01b = 2μs 10b = 4μs 11b = 8μs
1	HEAT_OLP_EN	R/W	0h	Enables heater offline open load detection circuit.
0	RESERVED	R	0h	Reserved

8.2.28 EC_CNFG Register (Offset = 24h) [Reset = 0000h]

EC_CNFG is shown in [Table 8-43](#).

Return to the [Summary Table](#).

Configures electrochrome driver and fault responses.

Table 8-43. EC_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ECDRV_OL_EN	R/W	0h	When the EC driver is in PVDD Supply/OUT11 Independent EC Mode (OUT11_EC_MODE = 0b), this bit enables the current source for open-load detection on ECFB. This bit can be ignored if the default configuration of EC is used (OUT11_EC_MODE = 1b). 0b = EC Open-load current source disabled 1b = EC Open-load current source enabled
14	ECFB_UV_TH	R/W	0h	Sets the ECFB undervoltage (short to ground) threshold. 0b = 100mV 1b = 200mV
13	RSVD_13	R/W	0h	Reserved.
12	RSVD_12	R/W	0h	Reserved.
11-10	ECFB_UV_DG	R/W	0h	Configures undervoltage fault deglitch time. 00b = 20μs 01b = 50μs 10b = 100μs 11b = 200μs
9-8	ECFB_OV_DG	R/W	0h	Configures overvoltage fault deglitch time. 00b = 20μs 01b = 50μs 10b = 100μs 11b = 200μs
7-6	ECFB_UV_MODE	R/W	0h	Configures ECFB UV fault response for EC driver. 0b = No action 01b = Report ECFB voltage < ECFB_UV_TH 10b = Report ECFB voltage < ECFB_UV_TH and disable EC driver.
5-4	ECFB_OV_MODE	R/W	0h	Configures ECFB OV fault response for EC driver. 0b = No action 01b = Report ECFB voltage < ECFB_OV_TH 10b = Report ECFB voltage < ECFB_OV_TH and disable EC driver.
3	EC_FLT_MODE	R/W	0h	Configures overcurrent fault response for EC driver. 0b = Hi-Z EC Driver 1b = Retry with OUT7 ITRIP settings
2	ECFB_LS_PWM	R/W	0h	Enables LS PWM discharge for EC load. 0b = No PWM discharge (Fast discharge) 1b = PWM discharge enabled
1	EC_OLEN	R/W	0h	This bit enables the open load detection circuit during EC discharge. 0b = Open load detection disabled during EC discharge 1b = Open load detection enabled during EC discharge
0	ECFB_MAX	R/W	0h	Configures the maximum target voltage for EC. 0b = 1.2V 1b = 1.5V

8.2.29 HS_OCP_DG Register (Offset = 25h) [Reset = 0000h]

HS_OCP_DG is shown in [Table 8-44](#).

Return to the [Summary Table](#).

High-side driver overcurrent deglitch configuration register.

Table 8-44. HS_OCP_DG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11-10	OUT12_OCP_DG	R/W	0h	Overcurrent deglitch time for high-side driver 12. 00b = 6μs 01b = 10μs 10b = 20μs 11b = 60μs
9-8	OUT11_OCP_DG	R/W	0h	Overcurrent deglitch time for high-side driver 11. 00b = 6μs 01b = 10μs 10b = 20μs 11b = 60μs
7-6	OUT10_OCP_DG	R/W	0h	Overcurrent deglitch time for high-side driver 10. 00b = 6μs 01b = 10μs 10b = 20μs 11b = 60μs
5-4	OUT9_OCP_DG	R/W	0h	Overcurrent deglitch time for high-side driver 9. 00b = 6μs 01b = 10μs 10b = 20μs 11b = 60μs
3-2	OUT8_OCP_DG	R/W	0h	Overcurrent deglitch time for high-side driver 8. 00b = 6μs 01b = 10μs 10b = 20μs 11b = 60μs
1-0	OUT7_OCP_DG	R/W	0h	Overcurrent deglitch time for high-side driver 7. 00b = 6μs 01b = 10μs 10b = 20μs 11b = 60μs

8.2.30 SPARE_CNFG2 Register (Offset = 26h) [Reset = 0000h]

SPARE_CNFG2 is shown in [Table 8-45](#).

Return to the [Summary Table](#).

Spare configuration 2.

Table 8-45. SPARE_CNFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

8.2.31 SPARE_CNFG3 Register (Offset = 27h) [Reset = 0000h]

SPARE_CNFG3 is shown in [Table 8-46](#).

Return to the [Summary Table](#).

Spare configuration 3.

Table 8-46. SPARE_CNFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

8.2.32 SPARE_CNFG4 Register (Offset = 28h) [Reset = 0000h]

SPARE_CNFG4 is shown in [Table 8-47](#).

Return to the [Summary Table](#).

Spare configuration 4.

Table 8-47. SPARE_CNFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

8.3 DRV8000-Q1_CTRL Registers

[Table 8-48](#) lists the memory-mapped registers for the DRV8000-Q1_CTRL registers. All register offset addresses not listed in [Table 8-48](#) are considered as reserved locations and the register contents are not to be modified.

Table 8-48. DRV8000-Q1_CTRL Registers

Offset	Acronym	Register Name	Section
29h	IC_CTRL	IC control register.	Section 8.3.1
2Ah	GD_HB_CTRL	Gate driver and half-bridge control register.	Section 8.3.2
2Bh	HS_EC_HEAT_CTRL	High-side driver, EC, and heater driver control register.	Section 8.3.3
2Ch	OUT7_PWM_DC	OUT7 PWM Duty cycle control register.	Section 8.3.4
2Dh	OUT8_PWM_DC	OUT8 PWM Duty cycle control register.	Section 8.3.5
2Eh	OUT9_PWM_DC	OUT9 PWM Duty cycle control register.	Section 8.3.6
2Fh	OUT10_PWM_DC	OUT10 PWM Duty cycle control register.	Section 8.3.7
30h	OUT11_PWM_DC	OUT11 PWM Duty cycle control register.	Section 8.3.8
31h	OUT12_PWM_DC	OUT12 PWM Duty cycle control register.	Section 8.3.9

Complex bit access types are encoded to fit into small table cells. [Table 8-49](#) shows the codes that are used for access types in this section.

Table 8-49. DRV8000-Q1_CTRL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.3.1 IC_CTRL Register (Offset = 29h) [Reset = 006Ch]

IC_CTRL is shown in [Table 8-50](#).

Return to the [Summary Table](#).

Control register to lock and unlock configuration or control registers, and clear faults.

Table 8-50. IC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	IPROPI_MODE	R/W	0h	Selects IPROPI/PWM2 pin mode between input and output modes. 0b = Output (IPROPI mode) 1b = Input (PWM mode)
12-8	IPROPI_SEL	R/W	0h	Controls IPROPI MUX output between current, voltage, and temperature sense output. 00000b = No output 00001b = OUT1 current sense output 00010b = OUT2 current sense output 00011b = OUT3 current sense output 00100b = OUT4 current sense output 00101b = OUT5 current sense output 00110b = OUT6 current sense output 00111b = OUT7 current sense output 01000b = OUT8 current sense output 01001b = OUT9 current sense output 01010b = OUT10 current sense output 01011b = OUT11 current sense output 01100b = OUT12 current sense output 01101b - 01111b = Reserved. 10000b = PVDD voltage sense output 10001b = Thermal cluster 1 output 10010b = Thermal cluster 2 output 10011b = Thermal cluster 3 output 10100b = Thermal cluster 4 output
7-5	CTRL_LOCK	R/W	3h	Lock and unlock the control registers. Bit settings not listed have no effect. 011b = Unlock all control registers. 110b = Lock the control registers by ignoring further writes except to the IC_CTRL register.
4-2	CNFG_LOCK	R/W	3h	Lock and unlock the configuration registers. Bit settings not listed have no effect. 011b = Unlock all configuration registers. 110b = Lock the configuration registers by ignoring further writes except to the IC_CTRL register.
1	WD_RST	R/W	0h	Watchdog timer restart. 0b by default after power up. Invert this bit to restart the watchdog timer. After written, the bit reflects the new inverted value.
0	CLR_FLT	R/W	0h	Clear latched fault status information. 0b = Default state. 1b = Clear latched fault bits, resets to 0b after completion. Also clears SPI fault and watchdog fault status.

8.3.2 GD_HB_CTRL Register (Offset = 2Ah) [Reset = 0000h]

GD_HB_CTRL is shown in [Table 8-51](#).

Return to the [Summary Table](#).

Gate driver and half-bridge output control register.

Table 8-51. GD_HB_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	S_HIZ2	R/W	0h	Gate driver 2 Hi-Z control bit. Active only in half-bridge input control mode. 0b = Outputs follow IN1/EN signal. 1b = Gate drivers pull-downs are enabled. Half-bridge 1 Hi-Z
14	S_HIZ1	R/W	0h	Gate driver 1 Hi-Z control bit. Active only in half-bridge input control mode. 0b = Outputs follow IN1/EN signal. 1b = Gate drivers pull-downs are enabled. Half-bridge 1 Hi-Z
13	S_IN2	R/W	0h	Control bit for IN1 input signal. Enabled through IN1_MODE bit.
12	S_IN1	R/W	0h	Control bit for IN2 input signal. Enabled through IN2_MODE bit.
11-10	OUT6_CTRL	R/W	0h	Integrated half-bridge output 6 control. 00b = OFF 01b = HS ON 10b = LS ON 11b = RSVD
9-8	OUT5_CTRL	R/W	0h	Integrated half-bridge output 5 control. 00b = OFF 01b = HS ON 10b = LS ON 11b = RSVD
7-6	OUT4_CTRL	R/W	0h	Integrated half-bridge output 4 control. 00b = OFF 01b = HS ON 10b = LS ON 11b = RSVD
5-4	OUT3_CTRL	R/W	0h	Integrated half-bridge output 3 control. 00b = OFF 01b = HS ON 10b = LS ON 11b = RSVD
3-2	OUT2_CTRL	R/W	0h	Integrated half-bridge output 2 control. 00b = OFF 01b = HS ON 10b = LS ON 11b = RSVD
1-0	OUT1_CTRL	R/W	0h	Integrated half-bridge output 1 control. 00b = OFF 01b = HS ON 10b = LS ON 11b = RSVD

8.3.3 HS_EC_HEAT_CTRL Register (Offset = 2Bh) [Reset = 0000h]

HS_EC_HEAT_CTRL is shown in [Table 8-52](#).

Return to the [Summary Table](#).

High-side driver, EC, and heater driver output control register.

Table 8-52. HS_EC_HEAT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ECFB_LS_EN	R/W	0h	Enables EC discharge with LS MOSFET on ECFB while the EC regulation is active.
14	EC_ON	R/W	0h	Enables the EC output.
13-8	EC_V_TAR	R/W	0h	6-bits of resolution to control the target voltage on ECFB. 0V to ECFB max (1.2 or 1.5V).
7	HEAT_EN	R/W	0h	Enables heater output.
6	RSVD_6	R/W	0h	Reserved.
5	OUT12_EN	R/W	0h	Enables high-side driver 12.
4	OUT11_EN	R/W	0h	Enables high-side driver 11.
3	OUT10_EN	R/W	0h	Enables high-side driver 10.
2	OUT9_EN	R/W	0h	Enables high-side driver 9.
1	OUT8_EN	R/W	0h	Enables high-side driver 8.
0	OUT7_EN	R/W	0h	Enables high-side driver 7.

8.3.4 OUT7_PWM_DC Register (Offset = 2Ch) [Reset = 0000h]

OUT7_PWM_DC is shown in [Table 8-53](#).

Return to the [Summary Table](#).

10-bit duty cycle control for high-side driver 7.

Table 8-53. OUT7_PWM_DC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9-0	OUT7_DC	R/W	0h	10-bit resolution control of Duty Cycle for dedicated PWM generator for high-side driver 7.

8.3.5 OUT8_PWM_DC Register (Offset = 2Dh) [Reset = 0000h]

OUT8_PWM_DC is shown in [Table 8-54](#).

Return to the [Summary Table](#).

10-bit duty cycle control for high-side driver 8.

Table 8-54. OUT8_PWM_DC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9-0	OUT8_DC	R/W	0h	10-bit resolution control of Duty Cycle for dedicated PWM generator for high-side driver 8.

8.3.6 OUT9_PWM_DC Register (Offset = 2Eh) [Reset = 0000h]

OUT9_PWM_DC is shown in [Table 8-55](#).

Return to the [Summary Table](#).

10-bit duty cycle control for high-side driver 9.

Table 8-55. OUT9_PWM_DC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9-0	OUT9_DC	R/W	0h	10-bit resolution control of Duty Cycle for dedicated PWM generator for high-side driver 9.

8.3.7 OUT10_PWM_DC Register (Offset = 2Fh) [Reset = 0000h]

OUT10_PWM_DC is shown in [Table 8-56](#).

Return to the [Summary Table](#).

10-bit duty cycle control for high-side driver 10.

Table 8-56. OUT10_PWM_DC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9-0	OUT10_DC	R/W	0h	10-bit resolution control of Duty Cycle for dedicated PWM generator for high-side driver 10.

8.3.8 OUT11_PWM_DC Register (Offset = 30h) [Reset = 0000h]

OUT11_PWM_DC is shown in [Table 8-57](#).

Return to the [Summary Table](#).

10-bit duty cycle control for high-side driver 11.

Table 8-57. OUT11_PWM_DC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9-0	OUT11_DC	R/W	0h	10-bit resolution control of Duty Cycle for dedicated PWM generator for high-side driver 11.

8.3.9 OUT12_PWM_DC Register (Offset = 31h) [Reset = 0000h]

OUT12_PWM_DC is shown in [Table 8-58](#).

Return to the [Summary Table](#).

10-bit duty cycle control for high-side driver 12.

Table 8-58. OUT12_PWM_DC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9-0	OUT12_DC	R/W	0h	10-bit resolution control of Duty Cycle for dedicated PWM generator for high-side driver 12.

8.4 DRV8001-Q1_STATUS Registers

Table 8-59 lists the memory-mapped registers for the DRV8001-Q1_STATUS registers. All register offset addresses not listed in **Table 8-59** are be considered as reserved locations and the register contents are not to be modified.

Table 8-59. DRV8001-Q1_STATUS Registers

Offset	Acronym	Register Name	Section
0h	IC_STAT1		Section 8.4.1
1h	IC_STAT2		Section 8.4.2
2h	RSVD_REG_2		Section 8.4.3
3h	HB_STAT1		Section 8.4.4
4h	HB_STAT2		Section 8.4.5
5h	EC_HEAT_ITRIP_STAT		Section 8.4.6
6h	HS_STAT		Section 8.4.7
7h	SPARE_STAT1		Section 8.4.8
8h	SPARE_STAT2		Section 8.4.9

Complex bit access types are encoded to fit into small table cells. **Table 8-60** shows the codes that are used for access types in this section.

Table 8-60. DRV8001-Q1_STATUS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

8.4.1 IC_STAT1 Register (Offset = 0h) [Reset = C000h]

IC_STAT1 is shown in [Table 8-61](#).

Return to the [Summary Table](#).

Table 8-61. IC_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SPI_OK	R	1h	Indicates if a SPI communications fault has been detected. 0b = One or multiple of SCLK_FLT in the prior frames. 1b = No SPI fault has been detected.
14	POR	R	1h	Indicates power-on-reset condition. 0b = No power-on-reset condition detected. 1b = Power-on reset condition detected.
13	FAULT	R	0h	General Fault indicator. Indicates a device or driver fault has occurred. 0b = No fault. 1b = Fault detected.
12	WARN	R	0h	General warning indicator. Indicates a warning is present. 0b = No warning. 1b = Warning is present.
11	GD	R	0h	Logic OR of VDS and VGS fault indicators for gate driver.
10	HB	R	0h	Logic OR of overcurrent and open load fault indicators for half-bridges.
9	EC_HEAT	R	0h	Logic OR of EC OV/UV, overcurrent, open load fault indicators for EC and heater.
8	HS	R	0h	Logic OR of overcurrent and open load fault indicators for high-side drivers.
7	PVDD_UV	R	0h	Indicates undervoltage fault on PVDD pin.
6	PVDD_OV	R	0h	Indicates overvoltage fault on PVDD pin.
5	VCP_UV	R	0h	Indicates undervoltage fault on VCP pin.
4	OTW	R	0h	Indicates overtemperature warning.
3	OTSD	R	0h	Indicates overtemperature shutdown
2	WD_FLT	R	0h	Indicates watchdog timer fault.
1	ITRIP	R	0h	Indicates ITRIP regulation warning when any OUTx entered ITRIP.
0	OUT7_ITRIP_TO	R	0h	Indicates OUT7 ITRIP timeout has occurred when set.

8.4.2 IC_STAT2 Register (Offset = 1h) [Reset = 0000h]

IC_STAT2 is shown in [Table 8-62](#).

Return to the [Summary Table](#).

Table 8-62. IC_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	SCLK_FLT	R	0h	Indicates SPI clock (frame) fault when the number of SCLK pulses in a transaction frame are not equal to 16. Reported on bit SPI_ERR.
12	RESERVED	R	0h	Reserved
11	ZONE4_OTSD	R	0h	Indicates overtemperature shutdown has occurred in zone 4.
10	ZONE3_OTSD	R	0h	Indicates overtemperature shutdown has occurred in zone 3.
9	ZONE2_OTSD	R	0h	Indicates overtemperature shutdown has occurred in zone 2.
8	ZONE1_OTSD	R	0h	Indicates overtemperature shutdown has occurred in zone 1.
7	ZONE4_OTW_H	R	0h	Indicates high temperature warning (above 125°C) has occurred in zone 4.
6	ZONE3_OTW_H	R	0h	Indicates high temperature warning (above 125°C) has occurred in zone 3.
5	ZONE2_OTW_H	R	0h	Indicates high temperature warning (above 125°C) has occurred in zone 2.
4	ZONE1_OTW_H	R	0h	Indicates high temperature warning (above 125°C) has occurred in zone 1.
3	ZONE4_OTW_L	R	0h	Indicates low temperature warning (above 105°C) has occurred in zone 4.
2	ZONE3_OTW_L	R	0h	Indicates low temperature warning (above 105°C) has occurred in zone 3.
1	ZONE2_OTW_L	R	0h	Indicates low temperature warning (above 105°C) has occurred in zone 2.
0	ZONE1_OTW_L	R	0h	Indicates low temperature warning (above 105°C) has occurred in zone 1.

8.4.3 RSVD_REG_2 Register (Offset = 2h) [Reset = 0000h]

RSVD_REG_2 is shown in [Table 8-63](#).

Return to the [Summary Table](#).

Table 8-63. RSVD_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

8.4.4 HB_STAT1 Register (Offset = 3h) [Reset = 0000h]

HB_STAT1 is shown in [Table 8-64](#).

Return to the [Summary Table](#).

Table 8-64. HB_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	OUT6_LS_OCP	R	0h	Indicates overcurrent fault on low-side of half-bridge OUT6.
12	OUT5_LS_OCP	R	0h	Indicates overcurrent fault on low-side of half-bridge OUT5.
11	OUT4_LS_OCP	R	0h	Indicates overcurrent fault on low-side of half-bridge OUT4.
10	OUT3_LS_OCP	R	0h	Indicates overcurrent fault on low-side of half-bridge OUT3.
9	OUT2_LS_OCP	R	0h	Indicates overcurrent fault on low-side of half-bridge OUT2.
8	OUT1_LS_OCP	R	0h	Indicates overcurrent fault on low-side of half-bridge OUT1.
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	OUT6_HS_OCP	R	0h	Indicates overcurrent fault on high-side of half-bridge OUT6.
4	OUT5_HS_OCP	R	0h	Indicates overcurrent fault on high-side of half-bridge OUT5.
3	OUT4_HS_OCP	R	0h	Indicates overcurrent fault on high-side of half-bridge OUT4.
2	OUT3_HS_OCP	R	0h	Indicates overcurrent fault on high-side of half-bridge OUT3.
1	OUT2_HS_OCP	R	0h	Indicates overcurrent fault on high-side of half-bridge OUT2.
0	OUT1_HS_OCP	R	0h	Indicates overcurrent fault on high-side of half-bridge OUT1.

8.4.5 HB_STAT2 Register (Offset = 4h) [Reset = 0000h]

HB_STAT2 is shown in [Table 8-65](#).

Return to the [Summary Table](#).

Table 8-65. HB_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	HB_OLP_STAT	R	0h	Indicates off-state open load fault on the selected half-bridge output per HB_OLP_CNFG bits (OUTX or OUTY).
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	OUT6_OLA	R	0h	Indicates active open load fault on half-bridge OUT6.
4	OUT5_OLA	R	0h	Indicates active open load fault on half-bridge OUT5.
3	OUT4_OLA	R	0h	Indicates active open load fault on half-bridge OUT4.
2	OUT3_OLA	R	0h	Indicates active open load fault on half-bridge OUT3.
1	OUT2_OLA	R	0h	Indicates active open load fault on half-bridge OUT2.
0	OUT1_OLA	R	0h	Indicates active open load fault on half-bridge OUT1.

8.4.6 EC_HEAT_ITRIP_STAT Register (Offset = 5h) [Reset = 0000h]

EC_HEAT_ITRIP_STAT is shown in [Table 8-66](#).

Return to the [Summary Table](#).

Table 8-66. EC_HEAT_ITRIP_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ECFB_UV	R	0h	Indicates undervoltage (short to ground) fault on ECFB pin.
14	ECFB_OV	R	0h	Indicates overvoltage (short to battery) fault on ECFB pin.
13	ECFB_HI	R	0h	Indicates regulation overvoltage fault on ECFB pin.
12	ECFB_LO	R	0h	Indicates regulation undervoltage fault on ECFB pin.
11	ECFB_OC	R	0h	Indicates overcurrent fault on ECFB pin.
10	ECFB_OL	R	0h	Indicates open load fault on ECFB pin.
9	HEAT_OL	R	0h	Indicates open load fault on SH_HS pin.
8	HEAT_VDS	R	0h	Indicates overcurrent fault on heater MOSFET.
7	OUT7_ITRIP_TO	R	0h	Indicates ITRIP timeout occurred on OUT7.
6	OUT7_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT7.
5	OUT6_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT6.
4	OUT5_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT5.
3	OUT4_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT4.
2	OUT3_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT3.
1	OUT2_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT2.
0	OUT1_ITRIP_STAT	R	0h	Indicates ITRIP regulation warning on OUT1.

8.4.7 HS_STAT Register (Offset = 6h) [Reset = 0000h]

HS_STAT is shown in [Table 8-67](#).

Return to the [Summary Table](#).

Table 8-67. HS_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	OUT12_OLA	R	0h	Indicates open load fault on OUT12.
12	OUT11_OLA	R	0h	Indicates open load fault on OUT11.
11	OUT10_OLA	R	0h	Indicates open load fault on OUT10.
10	OUT9_OLA	R	0h	Indicates open load fault on OUT9.
9	OUT8_OLA	R	0h	Indicates open load fault on OUT8.
8	OUT7_OLA	R	0h	Indicates open load fault on OUT7.
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	OUT12_OCP	R	0h	Indicates overcurrent fault on OUT12.
4	OUT11_OCP	R	0h	Indicates overcurrent fault on OUT11.
3	OUT10_OCP	R	0h	Indicates overcurrent fault on OUT10.
2	OUT9_OCP	R	0h	Indicates overcurrent fault on OUT9.
1	OUT8_OCP	R	0h	Indicates overcurrent fault on OUT8.
0	OUT7_OCP	R	0h	Indicates overcurrent fault on OUT7.

8.4.8 SPARE_STAT1 Register (Offset = 7h) [Reset = 0000h]

SPARE_STAT1 is shown in [Table 8-68](#).

Return to the [Summary Table](#).

Table 8-68. SPARE_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

8.4.9 SPARE_STAT2 Register (Offset = 8h) [Reset = 0001h]

SPARE_STAT2 is shown in [Table 8-69](#).

Return to the [Summary Table](#).

Table 8-69. SPARE_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	DEVICE_ID_7	R	0h	Device ID bit field 7.
6	DEVICE_ID_6	R	0h	Device ID bit field 6.
5	DEVICE_ID_5	R	0h	Device ID bit field 5.
4	DEVICE_ID_4	R	0h	Device ID bit field 4.
3	DEVICE_ID_3	R	0h	Device ID bit field 3.
2	DEVICE_ID_2	R	0h	Device ID bit field 2.
1	DEVICE_ID_1	R	0h	Device ID bit field 1.
0	DEVICE_ID_0	R	1h	Device ID bit field 0. DRV8001-Q1 address is 0x11.

8.5 DRV8001-Q1_CNFG Registers

Table 8-70 lists the memory-mapped registers for the DRV8001-Q1_CNFG registers. All register offset addresses not listed in **Table 8-70** are be considered as reserved locations and the register contents are not to be modified.

Table 8-70. DRV8001-Q1_CNFG Registers

Offset	Acronym	Register Name	Section
9h	IC_CNFG1		Section 8.5.1
Ah	IC_CNFG2		Section 8.5.2
Bh	RSVD_REG_B		Section 8.5.3
Ch	RSVD_REG_C		Section 8.5.4
Dh	RSVD_REG_D		Section 8.5.5
Eh	RSVD_REG_E		Section 8.5.6
Fh	RSVD_REG_F		Section 8.5.7
10h	RSVD_REG_10		Section 8.5.8
11h	RSVD_REG_11		Section 8.5.9
12h	RSVD_REG_12		Section 8.5.10
13h	RSVD_REG_13		Section 8.5.11
14h	HB_ITRIP_DG		Section 8.5.12
15h	HB_OUT_CNFG1		Section 8.5.13
16h	HB_OUT_CNFG2		Section 8.5.14
17h	HB_OCP_CNFG		Section 8.5.15
18h	HB_OL_CNFG1		Section 8.5.16
19h	HB_OL_CNFG2		Section 8.5.17
1Ah	HB_SR_CNFG		Section 8.5.18
1Bh	HB_ITRIP_CNFG		Section 8.5.19
1Ch	HB_ITRIP_FREQ		Section 8.5.20
1Dh	HS_HEAT_OUT_CNFG		Section 8.5.21
1Eh	HS_OC_CNFG		Section 8.5.22
1Fh	HS_OL_CNFG		Section 8.5.23
20h	HS_REG_CNFG1		Section 8.5.24
21h	HS_REG_CNFG2		Section 8.5.25
22h	HS_PWM_FREQ_CNFG		Section 8.5.26
23h	HEAT_CNFG		Section 8.5.27
24h	EC_CNFG		Section 8.5.28
25h	HS_OCP_DG		Section 8.5.29
26h	SPARE_CNFG2		Section 8.5.30
27h	SPARE_CNFG3		Section 8.5.31
28h	SPARE_CNFG4		Section 8.5.32

Complex bit access types are encoded to fit into small table cells. **Table 8-71** shows the codes that are used for access types in this section.

Table 8-71. DRV8001-Q1_CNFG Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		

**Table 8-71. DRV8001-Q1_CNFG Access Type Codes
(continued)**

Access Type	Code	Description
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.5.1 IC_CNFG1 Register (Offset = 9h) [Reset = 0002h]

IC_CNFG1 is shown in [Table 8-72](#).

Return to the [Summary Table](#).

Table 8-72. IC_CNFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OTSD_MODE	R/W	0h	Sets overtemperature shutdown behavior. If any thermal cluster reaches OT, the device either shuts down all drivers or affected drivers only (drivers in zone 3, for example). 0b = Global shutdown. 1b = Affected driver shutdown only.
14	DIS_CP	R/W	0h	When EN_GD = 0, the charge pump can be disabled, putting the device in a communication only mode. 0b = Charge pump enabled. 1b = Charge pump disabled.
13-12	PVDD_OV_MODE	R/W	0h	PVDD supply overvoltage monitor mode. 00b = Latched fault. 01b = Automatic recovery. 10b = Warning report only. 11b = Disabled.
11-10	PVDD_OV_DG	R/W	0h	PVDD supply overvoltage monitor deglitch time. 00b = 1μs 01b = 2μs 10b = 4μs 11b = 8μs
9	PVDD_OV_LVL	R/W	0h	PVDD supply overvoltage monitor threshold. 0b = 21.5V 1b = 28.5V
8	VCP_UV_LVL	R/W	0h	VCP charge pump undervoltage monitor threshold. 0b = 4.75V 1b = 6.25V
7-6	CP_MODE	R/W	0h	Charge pump operating mode. 00b = Automatic switch between tripler and doubler mode. 01b = Always doubler mode. 10b = Always tripler mode. 11b = RSVD
5	VCP_UV_MODE	R/W	0h	VCP charge pump undervoltage monitor mode. 0b = Latched fault. 1b = Automatic recovery.
4	PVDD_UV_MODE	R/W	0h	PVDD supply undervoltage monitor mode. 0b = Latched fault. 1b = Automatic recovery.
3	WD_EN	R/W	0h	Watchdog timer enable. 0b = Watchdog timer disabled. 1b = Watchdog timer enabled.
2	WD_FLT_M	R/W	0h	Watchdog fault mode. Watchdog fault is cleared by CLR_FLT. 0b = Watchdog fault is reported to WD_FLT and WARN register bits. Drivers remain enabled and FAULT bit is not asserted. 1b = Watchdog fault is reported to WD_FLT and FAULT register bits. All drivers are disabled in response to watchdog fault.
1	WD_WIN	R/W	1h	Watchdog timer window. 0b = 4 to 40ms 1b = 10 to 100ms
0	EN_SSC	R/W	0h	Spread spectrum clocking. 0b = Disabled. 1b = Enabled.

8.5.2 IC_CNFG2 Register (Offset = Ah) [Reset = 0000h]

IC_CNFG2 is shown in [Table 8-73](#).

Return to the [Summary Table](#).

Table 8-73. IC_CNFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9	RESERVED	R/W	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7	ZONE4_OTW_H_DIS	R/W	0h	Disables the high overtemperature warning for zone 4. Enabled = 0b Disabled = 1b
6	ZONE3_OTW_H_DIS	R/W	0h	Disables the high overtemperature warning for zone 3. Enabled = 0b Disabled = 1b
5	ZONE2_OTW_H_DIS	R/W	0h	Disables the high overtemperature warning for zone 2. Enabled = 0b Disabled = 1b
4	ZONE1_OTW_H_DIS	R/W	0h	Disables the high overtemperature warning for zone 1. Enabled = 0b Disabled = 1b
3	ZONE4_OTW_L_DIS	R/W	0h	Disables the low overtemperature warning for zone 4. Enabled = 0b Disabled = 1b
2	ZONE3_OTW_L_DIS	R/W	0h	Disables the low overtemperature warning for zone 3. Enabled = 0b Disabled = 1b
1	ZONE2_OTW_L_DIS	R/W	0h	Disables the low overtemperature warning for zone 2. Enabled = 0b Disabled = 1b
0	ZONE1_OTW_L_DIS	R/W	0h	Disables the low overtemperature warning for zone 1. Enabled = 0b Disabled = 1b

8.5.3 RSVD_REG_B Register (Offset = Bh) [Reset = 0000h]

RSVD_REG_B is shown in [Table 8-74](#).

Return to the [Summary Table](#).

Table 8-74. RSVD_REG_B Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

8.5.4 RSVD_REG_C Register (Offset = Ch) [Reset = 0000h]

RSVD_REG_C is shown in [Table 8-75](#).

Return to the [Summary Table](#).

Table 8-75. RSVD_REG_C Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

8.5.5 RSVD_REG_D Register (Offset = Dh) [Reset = 0000h]

RSVD_REG_D is shown in [Table 8-76](#).

Return to the [Summary Table](#).

Table 8-76. RSVD_REG_D Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

8.5.6 RSVD_REG_E Register (Offset = Eh) [Reset = 0000h]

RSVD_REG_E is shown in [Table 8-77](#).

Return to the [Summary Table](#).

Table 8-77. RSVD_REG_E Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

8.5.7 RSVD_REG_F Register (Offset = Fh) [Reset = 0000h]

RSVD_REG_F is shown in [Table 8-78](#).

Return to the [Summary Table](#).

Table 8-78. RSVD_REG_F Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

8.5.8 RSVD_REG_10 Register (Offset = 10h) [Reset = 0000h]

RSVD_REG_10 is shown in [Table 8-79](#).

Return to the [Summary Table](#).

Table 8-79. RSVD_REG_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

8.5.9 RSVD_REG_11 Register (Offset = 11h) [Reset = 0000h]

RSVD_REG_11 is shown in [Table 8-80](#).

Return to the [Summary Table](#).

Table 8-80. RSVD_REG_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

8.5.10 RSVD_REG_12 Register (Offset = 12h) [Reset = 0000h]

RSVD_REG_12 is shown in [Table 8-81](#).

Return to the [Summary Table](#).

Table 8-81. RSVD_REG_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

8.5.11 RSVD_REG_13 Register (Offset = 13h) [Reset = 0000h]

RSVD_REG_13 is shown in [Table 8-82](#).

Return to the [Summary Table](#).

Table 8-82. RSVD_REG_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

8.5.12 HB_ITRIP_DG Register (Offset = 14h) [Reset = 0000h]

HB_ITRIP_DG is shown in [Table 8-83](#).

Return to the [Summary Table](#).

Table 8-83. HB_ITRIP_DG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11-10	OUT6_ITRIP_DG	R/W	0h	Configures ITRIP deglitch time for half-bridge 6. 00b = 2μs 01b = 5μs 10b = 10μs 11b = 20μs
9-8	OUT5_ITRIP_DG	R/W	0h	Configures ITRIP deglitch time for half-bridge 5. 00b = 2μs 01b = 5μs 10b = 10μs 11b = 20μs
7-6	OUT4_ITRIP_DG	R/W	0h	Configures ITRIP deglitch time for half-bridge 4. 00b = 2μs 01b = 5μs 10b = 10μs 11b = 20μs
5-4	OUT3_ITRIP_DG	R/W	0h	Configures ITRIP deglitch time for half-bridge 3. 00b = 2μs 01b = 5μs 10b = 10μs 11b = 20μs
3-2	OUT2_ITRIP_DG	R/W	0h	Configures ITRIP deglitch time for half-bridge 2. 00b = 2μs 01b = 5μs 10b = 10μs 11b = 20μs
1-0	OUT1_ITRIP_DG	R/W	0h	Configures ITRIP deglitch time for half-bridge 1. 00b = 2μs 01b = 5μs 10b = 10μs 11b = 20μs

8.5.13 HB_OUT_CNFG1 Register (Offset = 15h) [Reset = 0000h]

HB_OUT_CNFG1 is shown in [Table 8-84](#).

Return to the [Summary Table](#).

Table 8-84. HB_OUT_CNFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RSVD	R/W	0h	Reserved.
14	NSR_OUT6_DIS	R/W	0h	Disables non-synchronous rectification during ITRIP regulation (sets active freewheeling) for half-bridge 6. Passive freewheeling = 0b Active freewheeling = 1b
13	NSR_OUT5_DIS	R/W	0h	Disables non-synchronous rectification during ITRIP regulation (sets active freewheeling) for half-bridge 5. Passive freewheeling = 0b Active freewheeling = 1b
12	NSR_OUT4_DIS	R/W	0h	Disables non-synchronous rectification during ITRIP regulation (sets active freewheeling) for half-bridge 4. Passive freewheeling = 0b Active freewheeling = 1b
11	NSR_OUT3_DIS	R/W	0h	Disables non-synchronous rectification during ITRIP regulation (sets active freewheeling) for half-bridges 3. Passive freewheeling = 0b Active freewheeling = 1b
10	NSR_OUT2_DIS	R/W	0h	Disables non-synchronous rectification during ITRIP regulation (sets active freewheeling) for half-bridge 2. Passive freewheeling = 0b Active freewheeling = 1b
9	NSR_OUT1_DIS	R/W	0h	Disables non-synchronous rectification during ITRIP regulation (sets active freewheeling) for half-bridge 1. Passive freewheeling = 0b Active freewheeling = 1b
8	IPROPI_SH_EN	R/W	0h	Enables IPROPI sample and hold circuit.
7	RSVD_7	R/W	0h	Reserved.
6	RSVD_6	R/W	0h	Reserved.
5-3	OUT6_CNFG	R/W	0h	Configuration for half-bridge 6. Enables or disables control of half-bridge, and sets control mode between PWM or SPI. 000b = Disabled 001b = Enabled (SPI register control) 010b = PWM1 Complementary Control 011b = PWM1 LS Control 100b = PWM1 HS Control 101b = PWM2 Complementary Control 110b = PWM2 PWM LS Control 111b = PWM2 HS Control
2-0	OUT5_CNFG	R/W	0h	Configuration for half-bridge 5. Enables or disables control of half-bridge, and sets control mode between PWM or SPI. 000b = Disabled 001b = Enabled (SPI register control) 010b = PWM1 Complementary Control 011b = PWM1 LS Control 100b = PWM1 HS Control 101b = PWM2 Complementary Control 110b = PWM2 PWM LS Control 111b = PWM2 HS Control

8.5.14 HB_OUT_CNFG2 Register (Offset = 16h) [Reset = 0000h]

HB_OUT_CNFG2 is shown in [Table 8-85](#).

Return to the [Summary Table](#).

Table 8-85. HB_OUT_CNFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RSVD_15	R/W	0h	Reserved.
14	RSVD_14	R/W	0h	Reserved.
13-11	OUT4_CNFG	R/W	0h	Configuration for half-bridge 4. Enables or disables control of half-bridge, and sets control mode between PWM or SPI. 000b = Disabled 001b = Enabled (SPI register control) 010b = PWM1 Complementary Control 011b = PWM1 LS Control 100b = PWM1 HS Control 101b = PWM2 Complementary Control 110b = PWM2 PWM LS Control 111b = PWM2 HS Control
10-8	OUT3_CNFG	R/W	0h	Configuration for half-bridge 3. Enables or disables control of half-bridge, and sets control mode between PWM or SPI. 000b = Disabled 001b = Enabled (SPI register control) 010b = PWM1 Complementary Control 011b = PWM1 LS Control 100b = PWM1 HS Control 101b = PWM2 Complementary Control 110b = PWM2 PWM LS Control 111b = PWM2 HS Control
7	RSVD_7	R/W	0h	Reserved.
6	RSVD_6	R/W	0h	Reserved.
5-3	OUT2_CNFG	R/W	0h	Configuration for half-bridge 2. Enables or disables control of half-bridge, and sets control mode between PWM or SPI. 000b = Disabled 001b = Enabled (SPI register control) 010b = PWM1 Complementary Control 011b = PWM1 LS Control 100b = PWM1 HS Control 101b = PWM2 Complementary Control 110b = PWM2 PWM LS Control 111b = PWM2 HS Control
2-0	OUT1_CNFG	R/W	0h	Configuration for half-bridge 1. Enables or disables control of half-bridge, and sets control mode between PWM or SPI. 000b = Disabled 001b = Enabled (SPI register control) 010b = PWM1 Complementary Control 011b = PWM1 LS Control 100b = PWM1 HS Control 101b = PWM2 Complementary Control 110b = PWM2 PWM LS Control 111b = PWM2 HS Control

8.5.15 HB_OCP_CNFG Register (Offset = 17h) [Reset = 0000h]

HB_OCP_CNFG is shown in [Table 8-86](#).

Return to the [Summary Table](#).

Table 8-86. HB_OCP_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RSVD	R/W	0h	Reserved.
14	RSVD	R/W	0h	Reserved.
13	RSVD	R/W	0h	Reserved.
12	RSVD	R/W	0h	Reserved.
11-10	OUT6_OCP_DG	R/W	0h	Overcurrent deglitch time for half-bridge 6. 00b = 6μs 01b = 10μs 10b = 20μs 11b = 60μs
9-8	OUT5_OCP_DG	R/W	0h	Overcurrent deglitch time for half-bridge 5. 00b = 6μs 01b = 10μs 10b = 20μs 11b = 60μs
7-6	OUT4_OCP_DG	R/W	0h	Overcurrent deglitch time for half-bridge 4. 00b = 6μs 01b = 10μs 10b = 20μs 11b = 60μs
5-4	OUT3_OCP_DG	R/W	0h	Overcurrent deglitch time for half-bridge 3. 00b = 6μs 01b = 10μs 10b = 20μs 11b = 60μs
3-2	OUT2_OCP_DG	R/W	0h	Overcurrent deglitch time for half-bridge 2. 00b = 6μs 01b = 10μs 10b = 20μs 11b = 60μs
1-0	OUT1_OCP_DG	R/W	0h	Overcurrent deglitch time for half-bridge 1. 00b = 6μs 01b = 10μs 10b = 20μs 11b = 60μs

8.5.16 HB_OL_CNFG1 Register (Offset = 18h) [Reset = 0000h]

HB_OL_CNFG1 is shown in [Table 8-87](#).

Return to the [Summary Table](#).

Table 8-87. HB_OL_CNFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RSVD_15	R/W	0h	Reserved.
14	RSVD_14	R/W	0h	Reserved.
13-12	HB_OLP_CNFG	R/W	0h	Off-state diagnostics configuration. 00b = Off-state disabled 01b = OUT X Pull-up enabled, OUT Y pull-down enabled, OUT Y selected, VREF Low 10b = OUT X Pull-up enabled, OUT Y pull-down enabled, OUT X selected, VREF High 11b = OUT X Pull-down enabled, OUT Y pull-up enabled, OUT Y selected, VREF Low
11-8	HB_OLP_SEL	R/W	0h	Off-state open load diagnostics enable for half-bridge 5. 0000b = Disabled 0001b = OUT1 and OUT2 0010b = OUT1 and OUT3 0011b = OUT1 and OUT4 0100b = OUT1 and OUT5 0101b = OUT1 and OUT6 0110b = OUT2 and OUT3 0111b = OUT2 and OUT4 1000b = OUT2 and OUT5 1001b = OUT2 and OUT6 1010b = OUT3 and OUT4 1011b = OUT3 and OUT5 1100b = OUT3 and OUT6 1101b = OUT4 and OUT5 1110b = OUT4 and OUT6 1111b = OUT5 and OUT6
7	RSVD_7	R/W	0h	Reserved.
6	RSVD_6	R/W	0h	Reserved.
5	OUT6_OLA_EN	R/W	0h	Active open load diagnostics enable for half-bridge 6. 0b = Enabled 1b = Disabled
4	OUT5_OLA_EN	R/W	0h	Active open load diagnostics enable for half-bridge 5. 0b = Enabled 1b = Disabled
3	OUT4_OLA_EN	R/W	0h	Active open load diagnostics enable for half-bridge 4. 0b = Enabled 1b = Disabled
2	OUT3_OLA_EN	R/W	0h	Active open load diagnostics enable for half-bridge 3. 0b = Enabled 1b = Disabled
1	OUT2_OLA_EN	R/W	0h	Active open load diagnostics enable for half-bridge 2. 0b = Enabled 1b = Disabled
0	OUT1_OLA_EN	R/W	0h	Active open load diagnostics enable for half-bridge 1. 0b = Enabled 1b = Disabled

8.5.17 HB_OL_CNFG2 Register (Offset = 19h) [Reset = 0000h]

HB_OL_CNFG2 is shown in [Table 8-88](#).

Return to the [Summary Table](#).

Table 8-88. HB_OL_CNFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RSVD_15	R/W	0h	Reserved.
14	RSVD_14	R/W	0h	Reserved.
13	RSVD_13	R/W	0h	Reserved.
12	RSVD_12	R/W	0h	Reserved.
11	RSVD_11	R/W	0h	Reserved.
10	RSVD_10	R/W	0h	Reserved.
9	RSVD_9	R/W	0h	Reserved.
8	RSVD_8	R/W	0h	Reserved.
7	RSVD_7	R/W	0h	Reserved.
6	RSVD_6	R/W	0h	Reserved.
5	OUT6_OLA_TH	R/W	0h	Sets the half-bridge 6 active open load cycle count threshold. 0b = 32 cycles 1b = 128 cycles
4	OUT5_OLA_TH	R/W	0h	Sets the half-bridge 5 active open load cycle count threshold. 0b = 32 cycles 1b = 128 cycles
3	OUT4_OLA_TH	R/W	0h	Sets the half-bridge 4 active open load cycle count threshold. 0b = 32 cycles 1b = 128 cycles
2	OUT3_OLA_TH	R/W	0h	Sets the half-bridge 3 active open load cycle count threshold. 0b = 32 cycles 1b = 128 cycles
1	OUT2_OLA_TH	R/W	0h	Sets the half-bridge 2 active open load cycle count threshold. 0b = 32 cycles 1b = 128 cycles
0	OUT1_OLA_TH	R/W	0h	Sets the half-bridge 1 active open load cycle count threshold. 0b = 32 cycles 1b = 128 cycles

8.5.18 HB_SR_CNFG Register (Offset = 1Ah) [Reset = 0000h]

HB_SR_CNFG is shown in [Table 8-89](#).

Return to the [Summary Table](#).

Table 8-89. HB_SR_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RSVD_15	R/W	0h	Reserved.
14	RSVD_14	R/W	0h	Reserved.
13	RSVD_13	R/W	0h	Reserved.
12	RSVD_12	R/W	0h	Reserved.
11-10	OUT6_SR	R/W	0h	Configures slew rate for half-bridge 6. 00b = 1.6V/ μ s 01b = 10V/ μ s 10b = 20V/ μ s
9-8	OUT5_SR	R/W	0h	Configures slew rate for half-bridge 5. 00b = 1.6V/ μ s 01b = 10V/ μ s 10b = 20V/ μ s
7-6	OUT4_SR	R/W	0h	Configures slew rate for half-bridge 4. 00b = 1.6V/ μ s 01b = 10V/ μ s 10b = 20V/ μ s
5-4	OUT3_SR	R/W	0h	Configures slew rate for half-bridge 3. 00b = 1.6V/ μ s 01b = 10V/ μ s 10b = 20V/ μ s
3-2	OUT2_SR	R/W	0h	Configures slew rate for half-bridge 2. 00b = 1.6V/ μ s 01b = 10V/ μ s 10b = 20V/ μ s
1-0	OUT1_SR	R/W	0h	Configures slew rate for half-bridge 1. 00b = 1.6V/ μ s 01b = 10V/ μ s 10b = 20V/ μ s

8.5.19 HB_ITRIP_CNFG Register (Offset = 1Bh) [Reset = 0000h]

HB_ITRIP_CNFG is shown in [Table 8-90](#).

Return to the [Summary Table](#).

Table 8-90. HB_ITRIP_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OUT6_ITRIP_EN	R/W	0h	Enables ITRIP regulation for half-bridge 6.
14	OUT5_ITRIP_EN	R/W	0h	Enables ITRIP regulation for half-bridge 5.
13	OUT4_ITRIP_EN	R/W	0h	Enables ITRIP regulation for half-bridge 4.
12	OUT3_ITRIP_EN	R/W	0h	Enables ITRIP regulation for half-bridge 3.
11	OUT2_ITRIP_EN	R/W	0h	Enables ITRIP regulation for half-bridge 2.
10	OUT1_ITRIP_EN	R/W	0h	Enables ITRIP regulation for half-bridge 1.
9-8	OUT6_ITRIP_LVL	R/W	0h	Configures ITRIP current threshold for half-bridge 6. 00b = 2.25A 01b = 5.5A 10b = 6.25A 11b = Reserved.
7-6	OUT5_ITRIP_LVL	R/W	0h	Configures ITRIP current threshold for half-bridge 5. 00b = 2.75A 01b = 6.5A 10b = 7.5A 11b = Reserved.
5-4	OUT4_ITRIP_LVL	R/W	0h	Configures ITRIP current threshold for half-bridge 4. 00b = 1.25A 01b = 2.75A 10b = 3.5A 11b = Reserved.
3-2	OUT3_ITRIP_LVL	R/W	0h	Configures ITRIP current threshold for half-bridge 3. 00b = 1.25A 01b = 2.5A 10b = 3.5A 11b = Reserved.
1	OUT2_ITRIP_LVL	R/W	0h	Configures ITRIP current threshold for half-bridge 2. 0b = 0.7A 1b = 0.875A
0	OUT1_ITRIP_LVL	R/W	0h	Configures ITRIP current threshold for half-bridge 1. 0b = 0.7A 1b = 0.875A

8.5.20 HB_ITRIP_FREQ Register (Offset = 1Ch) [Reset = 0000h]

HB_ITRIP_FREQ is shown in [Table 8-91](#).

Return to the [Summary Table](#).

Table 8-91. HB_ITRIP_FREQ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RSVD_15	R/W	0h	Reserved.
14	RSVD_14	R/W	0h	Reserved.
13	RSVD_13	R/W	0h	Reserved.
12	RSVD_12	R/W	0h	Reserved.
11-10	OUT6_ITRIP_FREQ	R/W	0h	Configures ITRIP regulation frequency for half-bridge 6. 00b = 20kHz 01b = 10kHz 10b = 5kHz 11b = 2.5kHz
9-8	OUT5_ITRIP_FREQ	R/W	0h	Configures ITRIP regulation frequency for half-bridge 5. 00b = 20kHz 01b = 10kHz 10b = 5kHz 11b = 2.5kHz
7-6	OUT4_ITRIP_FREQ	R/W	0h	Configures ITRIP regulation frequency for half-bridge 4. 00b = 20kHz 01b = 10kHz 10b = 5kHz 11b = 2.5kHz
5-4	OUT3_ITRIP_FREQ	R/W	0h	Configures ITRIP regulation frequency for half-bridge 3. 00b = 20kHz 01b = 10kHz 10b = 5kHz 11b = 2.5kHz
3-2	OUT2_ITRIP_FREQ	R/W	0h	Configures ITRIP regulation frequency for half-bridge 2. 00b = 20kHz 01b = 10kHz 10b = 5kHz 11b = 2.5kHz
1-0	OUT1_ITRIP_FREQ	R/W	0h	Configures ITRIP regulation frequency for half-bridge 1. 00b = 20kHz 01b = 10kHz 10b = 5kHz 11b = 2.5kHz

8.5.21 HS_HEAT_OUT_CNFG Register (Offset = 1Dh) [Reset = 0000h]

HS_HEAT_OUT_CNFG is shown in [Table 8-92](#).

Return to the [Summary Table](#).

Table 8-92. HS_HEAT_OUT_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	HEAT_OUT_CNFG	R/W	0h	Configuration for heater driver. Enables or disables control of heater, and sets control mode between PWM or SPI. 00b = Disabled 01b = SPI control enabled 10b = PWM pin control 11b = Reserved
13	RSVD_13	R/W	0h	Reserved.
12	RSVD_12	R/W	0h	Reserved.
11-10	OUT12_CNFG	R/W	0h	Configuration for high-side driver 12. Enables or disables control of high-side driver, and sets control mode between PWM or SPI. 00b = Disabled 01b = SPI control enabled 10b = PWM pin control 11b = PWM Generator
9-8	OUT11_CNFG	R/W	0h	Configuration for high-side driver 11. Enables or disables control of high-side driver, and sets control mode between PWM or SPI. 00b = Disabled 01b = SPI control enabled 10b = PWM pin control 11b = PWM Generator
7-6	OUT10_CNFG	R/W	0h	Configuration for high-side driver 10. Enables or disables control of high-side driver, and sets control mode between PWM or SPI. 00b = Disabled 01b = SPI control enabled 10b = PWM pin control 11b = PWM Generator
5-4	OUT9_CNFG	R/W	0h	Configuration for high-side driver 9. Enables or disables control of high-side driver, and sets control mode between PWM or SPI. 00b = Disabled 01b = SPI control enabled 10b = PWM pin control 11b = PWM Generator
3-2	OUT8_CNFG	R/W	0h	Configuration for high-side driver 8. Enables or disables control of high-side driver, and sets control mode between PWM or SPI. 00b = Disabled 01b = SPI control enabled 10b = PWM pin control 11b = PWM Generator
1-0	OUT7_CNFG	R/W	0h	Configuration for high-side driver 7. Enables or disables control of high-side driver, and sets control mode between PWM or SPI. 00b = Disabled 01b = SPI control enabled 10b = PWM pin control 11b = PWM Generator

8.5.22 HS_OC_CNFG Register (Offset = 1Eh) [Reset = 1000h]

HS_OC_CNFG is shown in [Table 8-93](#).

Return to the [Summary Table](#).

Table 8-93. HS_OC_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RSVD_15	R/W	0h	Reserved.
14	RSVD_14	R/W	0h	Reserved.
13	RSVD_13	R/W	0h	Reserved.
12	OUT11_EC_MODE	R/W	1h	Bit sets high-side OUT11 for independent control through OUT11_CNFG bits or for EC mode. Default configuration is for EC mode. OUT11_CNFG mode = 0b EC mode = 1b
11	RSVD_12	R/W	0h	Reserved.
10	RSVD_11	R/W	0h	Reserved.
9	RSVD_10	R/W	0h	Reserved.
8	RSVD_9	R/W	0h	Reserved.
7	RSVD_8	R/W	0h	Reserved.
6	RSVD_6	R/W	0h	Reserved.
5	OUT12_OC_TH	R/W	0h	Configures overcurrent threshold between high or low for high-side driver 12. 0b = Low current threshold 1b = High current threshold
4	OUT11_OC_TH	R/W	0h	Configures overcurrent threshold between high or low for high-side driver 11. 0b = Low current threshold 1b = High current threshold
3	OUT10_OC_TH	R/W	0h	Configures overcurrent threshold between high or low for high-side driver 10. 0b = Low current threshold 1b = High current threshold
2	OUT9_OC_TH	R/W	0h	Configures overcurrent threshold between high or low for high-side driver 9. 0b = Low current threshold 1b = High current threshold
1	OUT8_OC_TH	R/W	0h	Configures overcurrent threshold between high or low for high-side driver 8. 0b = Low current threshold 1b = High current threshold
0	OUT7_RDSON_MODE	R/W	0h	Configures high-side driver 7 between high RDSON mode and low RDSON mode (for bulb/lamp load). 0b = High RDSON mode (LED driver mode) 1b = Low RDSON mode (bulb/lamp driver mode)

8.5.23 HS_OL_CNFG Register (Offset = 1Fh) [Reset = 0000h]

HS_OL_CNFG is shown in [Table 8-94](#).

Return to the [Summary Table](#).

Table 8-94. HS_OL_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RSVD_15	R/W	0h	Reserved.
14	RSVD_14	R/W	0h	Reserved.
13	OUT12_OLA_TH	R/W	0h	Configures high-side driver 12 open load threshold. 0b = Low threshold 1b = High threshold
12	OUT11_OLA_TH	R/W	0h	Configures high-side driver 11 open load threshold. 0b = Low threshold 1b = High threshold
11	OUT10_OLA_TH	R/W	0h	Configures high-side driver 10 open load threshold. 0b = Low threshold 1b = High threshold
10	OUT9_OLA_TH	R/W	0h	Configures high-side driver 9 open load threshold. 0b = Low threshold 1b = High threshold
9	OUT8_OLA_TH	R/W	0h	Configures high-side driver 8 open load threshold. 0b = Low threshold 1b = High threshold
8	OUT7_OLA_TH	R/W	0h	Configures high-side driver 7 open load threshold. 0b = Low threshold 1b = High threshold
7	RSVD_7	R/W	0h	Reserved.
6	RSVD_6	R/W	0h	Reserved.
5	OUT12_OLA_EN	R/W	0h	Enables open load detection circuit for high-side driver 12.
4	OUT11_OLA_EN	R/W	0h	Enables open load detection circuit for high-side driver 11.
3	OUT10_OLA_EN	R/W	0h	Enables open load detection circuit for high-side driver 10.
2	OUT9_OLA_EN	R/W	0h	Enables open load detection circuit for high-side driver 9.
1	OUT8_OLA_EN	R/W	0h	Enables open load detection circuit for high-side driver 8.
0	OUT7_OLA_EN	R/W	0h	Enables open load detection circuit for high-side driver 7.

8.5.24 HS_REG_CNFG1 Register (Offset = 20h) [Reset = 0000h]

HS_REG_CNFG1 is shown in [Table 8-95](#).

Return to the [Summary Table](#).

Table 8-95. HS_REG_CNFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	OUT7_OCP_DIS	R/W	0h	Disables second current limit of 2.5A on OUT7 in low RDSO mode. 0b = OUT7 OCP enable 1b = OUT7 OCP disable
9-8	ITRIP_TO_SEL	R/W	0h	Selects the timeout limit for OUT7 ITRIP regulation. 00b = 100ms 01b = 200ms 10b = 400ms 11b = 800ms
7-6	OUT7_ITRIP_CNFG	R/W	0h	Configures OUT7 ITRIP behavior, fault clearing and latching. 00b = ITRIP fault report only 01b = ITRIP regulation with timeout and driver disable 10b = ITRIP regulation always 11b = ITRIP regulation with timeout and regulation disable
5-4	OUT7_ITRIP_BLK	R/W	0h	Configures OUT7 ITRIP blanking time. 00b = Reserved. 01b = 0μs 10b = 20μs 11b = 40μs
3-2	OUT7_ITRIP_FREQ	R/W	0h	Configures OUT7 ITRIP regulation frequency. 00b = 1.7kHz 01b = 2.2kHz 10b = 3kHz 11b = 4.4kHz
1-0	OUT7_ITRIP_DG	R/W	0h	Configures OUT7 ITRIP deglitch time. 00b = 48μs 01b = 40μs 10b = 32μs 11b = 24μs

8.5.25 HS_REG_CNFG2 Register (Offset = 21h) [Reset = 0000h]

HS_REG_CNFG2 is shown in [Table 8-96](#).

Return to the [Summary Table](#).

Table 8-96. HS_REG_CNFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	OUT12_CCM_TO	R/W	0h	Configures the constant current mode timing and current limit option of high-side output 12. 100mA for 20ms = 0b 200mA for 1ms = 1b
12	OUT11_CCM_TO	R/W	0h	Configures the constant current mode timing and current limit option of high-side output 11. 100mA for 20ms = 0b 200mA for 10ms = 1b
11	OUT10_CCM_TO	R/W	0h	Configures the constant current mode timing and current limit option of high-side output 10. 100mA for 20ms = 0b 200mA for 10ms = 1b
10	OUT9_CCM_TO	R/W	0h	Configures the constant current mode timing and current limit option of high-side output 9. 100mA for 20ms = 0b 200mA for 10ms = 1b
9	OUT8_CCM_TO	R/W	0h	Configures the constant current mode timing and current limit option of high-side output 8. 100mA for 20ms = 0b 200mA for 10ms = 1b
8	OUT7_CCM_TO	R/W	0h	Configures the constant current mode timing and current limit option of high-side output 7. 100mA for 20ms = 0b 200mA for 10ms = 1b
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	OUT12_CCM_EN	R/W	0h	Enables constant current mode circuit for high-side driver 12.
4	OUT11_CCM_EN	R/W	0h	Enables constant current mode circuit for high-side driver 11.
3	OUT10_CCM_EN	R/W	0h	Enables constant current mode circuit for high-side driver 10.
2	OUT9_CCM_EN	R/W	0h	Enables constant current mode circuit for high-side driver 9.
1	OUT8_CCM_EN	R/W	0h	Enables constant current mode circuit for high-side driver 8.
0	OUT7_CCM_EN	R/W	0h	Enables constant current mode circuit for high-side driver 7.

8.5.26 HS_PWM_FREQ_CNFG Register (Offset = 22h) [Reset = 0000h]

HS_PWM_FREQ_CNFG is shown in [Table 8-97](#).

Return to the [Summary Table](#).

Table 8-97. HS_PWM_FREQ_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11-10	PWM_OUT12_FREQ	R/W	0h	Configures frequency output of dedicated PWM generator for high-side driver 12. 00b = 108Hz 01b = 217Hz 10b = 289Hz 11b = Reserved
9-8	PWM_OUT11_FREQ	R/W	0h	Configures frequency output of dedicated PWM generator for high-side driver 11. 00b = 108Hz 01b = 217Hz 10b = 289Hz 11b = Reserved
7-6	PWM_OUT10_FREQ	R/W	0h	Configures frequency output of dedicated PWM generator for high-side driver 10. 00b = 108Hz 01b = 217Hz 10b = 289Hz 11b = Reserved
5-4	PWM_OUT9_FREQ	R/W	0h	Configures frequency output of dedicated PWM generator for high-side driver 9. 00b = 108Hz 01b = 217Hz 10b = 289Hz 11b = Reserved
3-2	PWM_OUT8_FREQ	R/W	0h	Configures frequency output of dedicated PWM generator for high-side driver 8. 00b = 108Hz 01b = 217Hz 10b = 289Hz 11b = Reserved
1-0	PWM_OUT7_FREQ	R/W	0h	Configures frequency output of dedicated PWM generator for high-side driver 7. 00b = 108Hz 01b = 217Hz 10b = 289Hz 11b = Reserved

8.5.27 HEAT_CNFG Register (Offset = 23h) [Reset = 0A3Ch]

HEAT_CNFG is shown in [Table 8-98](#).

Return to the [Summary Table](#).

Table 8-98. HEAT_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11-8	HEAT_VDS_LVL	R/W	Ah	Heater MOSFET VDS monitor protection threshold. 0000b = 0.06V 00001b = 0.08V 0010b = 0.10V 0011b = 0.12V 0100b = 0.14V 0101b = 0.16V 0110b = 0.18V 0111b = 0.2V 1000b = 0.24V 1001b = 0.28V 1010b = 0.32V 1011b = 0.36V 1100b = 0.4V 1101b = 0.44V 1110b = 0.56V 1111b = 1V
7-6	HEAT_VDS_MODE	R/W	0h	Heater MOSFET VDS overcurrent monitor fault mode. 00b = Latched fault. 01b = Cycle by cycle. 10b = Warning report only. 11b = Disabled.
5-4	HEAT_VDS_BLK	R/W	3h	Heater MOSFET VDS monitor blanking time. 00b = 4μs 01b = 8μs 10b = 16μs 11b = 32μs
3-2	HEAT_VDS_DG	R/W	3h	Heater MOSFET VDS overcurrent monitor deglitch time. 00b = 1μs 01b = 2μs 10b = 4μs 11b = 8μs
1	HEAT_OLP_EN	R/W	0h	Enables heater offline open load detection circuit.
0	RESERVED	R/W	0h	Reserved

8.5.28 EC_CNFG Register (Offset = 24h) [Reset = 0000h]

EC_CNFG is shown in [Table 8-99](#).

Return to the [Summary Table](#).

Table 8-99. EC_CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ECDRV_OL_EN	R/W	0h	Enables open-load detection circuit on ECFB.
14	ECFB_UV_TH	R/W	0h	Sets the ECFB undervoltage (short to ground) threshold. 0b = 100mV 1b = 200mV
13	RSVD_13	R/W	0h	Reserved.
12	RSVD_12	R/W	0h	Reserved.
11-10	ECFB_UV_DG	R/W	0h	Configures undervoltage fault deglitch time. 00b = 20µs 01b = 50µs 10b = 100µs 11b = 200µs
9-8	ECFB_OV_DG	R/W	0h	Configures overvoltage fault deglitch time. 00b = 20µs 01b = 50µs 10b = 100µs 11b = 200µs
7-6	ECFB_UV_MODE	R/W	0h	Configures ECFB UV fault response for EC driver. 0b = No action 01b = Report ECFB voltage < ECFB_UV_TH 10b = Report ECFB voltage < ECFB_UV_TH and disable EC driver.
5-4	ECFB_OV_MODE	R/W	0h	Configures ECFB OV fault response for EC driver. 0b = No action 01b = Report ECFB voltage < ECFB_OV_TH 10b = Report ECFB voltage < ECFB_OV_TH and disable EC driver.
3	EC_FLT_MODE	R/W	0h	Configures overcurrent fault response for EC driver. 0b = Hi-Z EC Driver 1b = Retry with OUT7 ITRIP settings
2	ECFB_LS_PWM	R/W	0h	Enables LS PWM discharge for EC load. 0b = No PWM discharge (Fast discharge) 1b = PWM discharge enabled
1	EC_OLEN	R/W	0h	Enables open load detection circuit ECFB.
0	ECFB_MAX	R/W	0h	Configures the maximum target voltage for EC. 0b = 1.2V 1b = 1.5V

8.5.29 HS_OCP_DG Register (Offset = 25h) [Reset = 0000h]

HS_OCP_DG is shown in [Table 8-100](#).

Return to the [Summary Table](#).

Table 8-100. HS_OCP_DG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11-10	OUT12_OCP_DG	R/W	0h	Overcurrent deglitch time for high-side driver 12. 00b = 6μs 01b = 10μs 10b = 20μs 11b = 60μs
9-8	OUT11_OCP_DG	R/W	0h	Overcurrent deglitch time for high-side driver 11. 00b = 6μs 01b = 10μs 10b = 20μs 11b = 60μs
7-6	OUT10_OCP_DG	R/W	0h	Overcurrent deglitch time for high-side driver 10. 00b = 6μs 01b = 10μs 10b = 20μs 11b = 60μs
5-4	OUT9_OCP_DG	R/W	0h	Overcurrent deglitch time for high-side driver 9. 00b = 6μs 01b = 10μs 10b = 20μs 11b = 60μs
3-2	OUT8_OCP_DG	R/W	0h	Overcurrent deglitch time for high-side driver 8. 00b = 6μs 01b = 10μs 10b = 20μs 11b = 60μs
1-0	OUT7_OCP_DG	R/W	0h	Overcurrent deglitch time for high-side driver 7. 00b = 6μs 01b = 10μs 10b = 20μs 11b = 60μs

8.5.30 SPARE_CNFG2 Register (Offset = 26h) [Reset = 0000h]

SPARE_CNFG2 is shown in [Table 8-101](#).

Return to the [Summary Table](#).

Table 8-101. SPARE_CNFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9	RESERVED	R/W	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3	RESERVED	R/W	0h	Reserved
2	RESERVED	R/W	0h	Reserved
1	RESERVED	R/W	0h	Reserved
0	RESERVED	R/W	0h	Reserved

8.5.31 SPARE_CNFG3 Register (Offset = 27h) [Reset = 0000h]

SPARE_CNFG3 is shown in [Table 8-102](#).

Return to the [Summary Table](#).

Table 8-102. SPARE_CNFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9	RESERVED	R/W	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3	RESERVED	R/W	0h	Reserved
2	RESERVED	R/W	0h	Reserved
1	RESERVED	R/W	0h	Reserved
0	RESERVED	R/W	0h	Reserved

8.5.32 SPARE_CNFG4 Register (Offset = 28h) [Reset = 0000h]

SPARE_CNFG4 is shown in [Table 8-103](#).

Return to the [Summary Table](#).

Table 8-103. SPARE_CNFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9	RESERVED	R/W	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3	RESERVED	R/W	0h	Reserved
2	RESERVED	R/W	0h	Reserved
1	RESERVED	R/W	0h	Reserved
0	RESERVED	R/W	0h	Reserved

8.6 DRV8001-Q1_CTRL Registers

[Table 8-104](#) lists the memory-mapped registers for the DRV8001-Q1_CTRL registers. All register offset addresses not listed in [Table 8-104](#) are considered as reserved locations and the register contents are not to be modified.

Table 8-104. DRV8001-Q1_CTRL Registers

Offset	Acronym	Register Name	Section
29h	IC_CTRL		Section 8.6.1
2Ah	HB_CTRL		Section 8.6.2
2Bh	HS_EC_HEAT_CTRL		Section 8.6.3
2Ch	OUT7_PWM_DC		Section 8.6.4
2Dh	OUT8_PWM_DC		Section 8.6.5
2Eh	OUT9_PWM_DC		Section 8.6.6
2Fh	OUT10_PWM_DC		Section 8.6.7
30h	OUT11_PWM_DC		Section 8.6.8
31h	OUT12_PWM_DC		Section 8.6.9

Complex bit access types are encoded to fit into small table cells. [Table 8-105](#) shows the codes that are used for access types in this section.

Table 8-105. DRV8001-Q1_CTRL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.1 IC_CTRL Register (Offset = 29h) [Reset = 006Ch]

IC_CTRL is shown in [Table 8-106](#).

Return to the [Summary Table](#).

Table 8-106. IC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	IPROPI_MODE	R/W	0h	Selects IPROPI/PWM2 pin mode between input and output modes. 0b = Output (IPROPI mode) 1b = Input (PWM mode)
12-8	IPROPI_SEL	R/W	0h	Controls IPROPI MUX output between current, voltage, and temperature sense output. 00000b = No output 00001b = OUT1 current sense output 00010b = OUT2 current sense output 00011b = OUT3 current sense output 00100b = OUT4 current sense output 00101b = OUT5 current sense output 00110b = OUT6 current sense output 00111b = OUT7 current sense output 01000b = OUT8 current sense output 01001b = OUT9 current sense output 01010b = OUT10 current sense output 01011b = OUT11 current sense output 01100b = OUT12 current sense output 01101b - 01111b = Reserved. 10000b = PVDD voltage sense output 10001b = Thermal cluster 1 output 10010b = Thermal cluster 2 output 10011b = Thermal cluster 3 output 10100b = Thermal cluster 4 output
7-5	CTRL_LOCK	R/W	3h	Lock and unlock the control registers. Bit settings not listed have no effect. 011b = Unlock all control registers. 110b = Lock the control registers by ignoring further writes except to the IC_CTRL register.
4-2	CNFG_LOCK	R/W	3h	Lock and unlock the configuration registers. Bit settings not listed have no effect. 011b = Unlock all configuration registers. 110b = Lock the configuration registers by ignoring further writes except to the IC_CTRL register.
1	WD_RST	R/W	0h	Watchdog timer restart. 0b by default after power up. Invert this bit to restart the watchdog timer. After written, the bit reflects the new inverted value.
0	CLR_FLT	R/W	0h	Clear latched fault status information. 0b = Default state. 1b = Clear latched fault bits, resets to 0b after completion. Also clears SPI fault and watchdog fault status.

8.6.2 HB_CTRL Register (Offset = 2Ah) [Reset = 0000h]

HB_CTRL is shown in [Table 8-107](#).

Return to the [Summary Table](#).

Table 8-107. HB_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11-10	OUT6_CTRL	R/W	0h	Integrated half-bridge output 6 control. 00b = OFF 01b = HS ON 10b = LS ON 11b = RSVD
9-8	OUT5_CTRL	R/W	0h	Integrated half-bridge output 5 control. 00b = OFF 01b = HS ON 10b = LS ON 11b = RSVD
7-6	OUT4_CTRL	R/W	0h	Integrated half-bridge output 4 control. 00b = OFF 01b = HS ON 10b = LS ON 11b = RSVD
5-4	OUT3_CTRL	R/W	0h	Integrated half-bridge output 3 control. 00b = OFF 01b = HS ON 10b = LS ON 11b = RSVD
3-2	OUT2_CTRL	R/W	0h	Integrated half-bridge output 2 control. 00b = OFF 01b = HS ON 10b = LS ON 11b = RSVD
1-0	OUT1_CTRL	R/W	0h	Integrated half-bridge output 1 control. 00b = OFF 01b = HS ON 10b = LS ON 11b = RSVD

8.6.3 HS_EC_HEAT_CTRL Register (Offset = 2Bh) [Reset = 0000h]

HS_EC_HEAT_CTRL is shown in [Table 8-108](#).

Return to the [Summary Table](#).

Table 8-108. HS_EC_HEAT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ECFB_LS_EN	R/W	0h	Enables EC discharge with LS MOSFET on ECFB while the EC regulation is active.
14	EC_ON	R/W	0h	Enables the EC output.
13-8	EC_V_TAR	R/W	0h	6-bits of resolution to control the target voltage on ECFB. 0V to ECFB max (1.2 or 1.5V).
7	HEAT_EN	R/W	0h	Enables heater output.
6	RSVD_6	R/W	0h	Reserved.
5	OUT12_EN	R/W	0h	Enables high-side driver 12.
4	OUT11_EN	R/W	0h	Enables high-side driver 11.
3	OUT10_EN	R/W	0h	Enables high-side driver 10.
2	OUT9_EN	R/W	0h	Enables high-side driver 9.
1	OUT8_EN	R/W	0h	Enables high-side driver 8.
0	OUT7_EN	R/W	0h	Enables high-side driver 7.

8.6.4 OUT7_PWM_DC Register (Offset = 2Ch) [Reset = 0000h]

OUT7_PWM_DC is shown in [Table 8-109](#).

Return to the [Summary Table](#).

Table 8-109. OUT7_PWM_DC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9-0	OUT7_DC	R/W	0h	10-bit resolution control of Duty Cycle for dedicated PWM generator for high-side driver 7.

8.6.5 OUT8_PWM_DC Register (Offset = 2Dh) [Reset = 0000h]

OUT8_PWM_DC is shown in [Table 8-110](#).

Return to the [Summary Table](#).

Table 8-110. OUT8_PWM_DC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9-0	OUT8_DC	R/W	0h	10-bit resolution control of Duty Cycle for dedicated PWM generator for high-side driver 8.

8.6.6 OUT9_PWM_DC Register (Offset = 2Eh) [Reset = 0000h]

OUT9_PWM_DC is shown in [Table 8-111](#).

Return to the [Summary Table](#).

Table 8-111. OUT9_PWM_DC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9-0	OUT9_DC	R/W	0h	10-bit resolution control of Duty Cycle for dedicated PWM generator for high-side driver 9.

8.6.7 OUT10_PWM_DC Register (Offset = 2Fh) [Reset = 0000h]

OUT10_PWM_DC is shown in [Table 8-112](#).

Return to the [Summary Table](#).

Table 8-112. OUT10_PWM_DC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9-0	OUT10_DC	R/W	0h	10-bit resolution control of Duty Cycle for dedicated PWM generator for high-side driver 10.

8.6.8 OUT11_PWM_DC Register (Offset = 30h) [Reset = 0000h]

OUT11_PWM_DC is shown in [Table 8-113](#).

Return to the [Summary Table](#).

Table 8-113. OUT11_PWM_DC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9-0	OUT11_DC	R/W	0h	10-bit resolution control of Duty Cycle for dedicated PWM generator for high-side driver 11.

8.6.9 OUT12_PWM_DC Register (Offset = 31h) [Reset = 0000h]

OUT12_PWM_DC is shown in [Table 8-114](#).

Return to the [Summary Table](#).

Table 8-114. OUT12_PWM_DC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9-0	OUT12_DC	R/W	0h	10-bit resolution control of Duty Cycle for dedicated PWM generator for high-side driver 12.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The DRV800x-Q1 is a highly configurable multichannel integrated half-bridge and half-bridge MOSFET gate driver that can be used to drive a variety of different output loads. The design examples below highlight how to use and configure the device for different application use cases.

9.2 Typical Application

The typical application for the DRV8001-Q1 is to control multiple loads in a typical automotive door. These include multiple integrated half-bridges and high-side drivers, an electrochromic mirror driver and external high-side MOSFET driver for a heating element. A high-level schematic example is shown in [DRV8001-Q1 Typical Application](#) below.

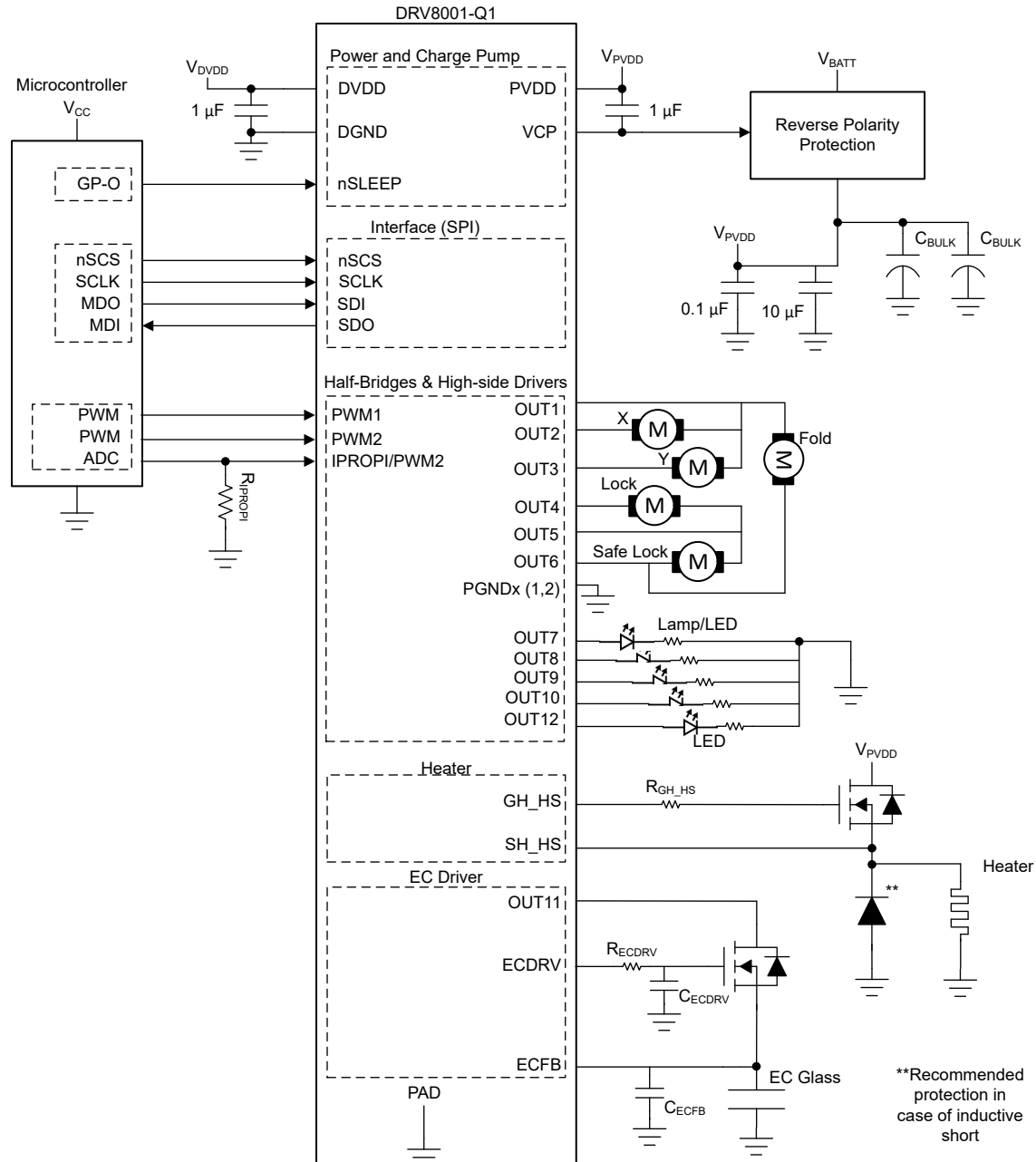


Figure 9-1. DRV8001-Q1 Typical Application

9.2.1 Design Requirements

The table below lists a set of example input parameters for the system design.

Table 9-1. Design Parameters

PARAMETER	VALUE
PVDD Supply Voltage Range	9 to 18V
PVDD Nominal Supply Voltage	13.5V
DVDD Logic Supply Voltage Range	3.3V
I _{PROPI} Resistance	1kΩ
PWM Frequency	20kHz

9.3 Initialization Setup

9.4 Power Supply Recommendations

9.4.1 Bulk Capacitance Sizing

Having appropriate local bulk capacitance is an important factor in motor drive system design. Having more bulk capacitance is generally beneficial, while the disadvantages are increased cost and physical size. The amount of local capacitance depends on a variety of factors including:

- The highest current required by the motor system
- The type of power supply, capacitance, and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable supply voltage ripple
- Type of motor (brushed DC, brushless DC, stepper)
- The motor start-up and braking methods

The inductance between the power supply and motor drive system can limit the current rate from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet provides a recommended minimum value, but system level testing is required to determine the appropriate sized bulk capacitor.

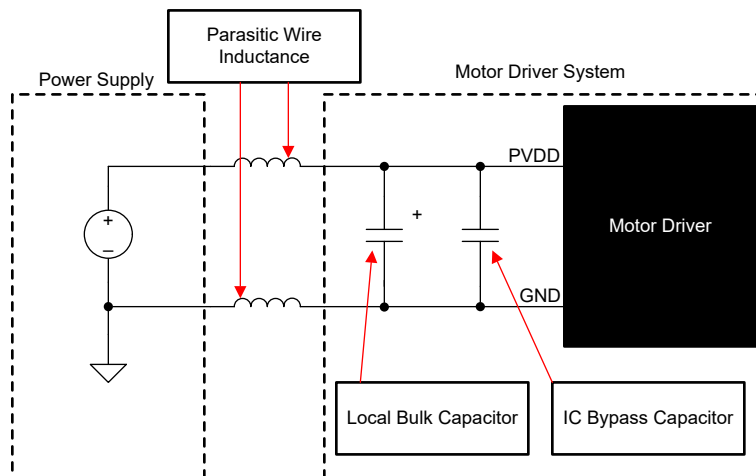


Figure 9-2. Motor Driver Supply Parasitics Example

9.5 Layout

9.5.1 Layout Guidelines

Bypass the PVDD pin to the GND pin using a low-ESR ceramic bypass capacitor C_{PVDD1} . Place this capacitor as close to the PVDD pin as possible with a thick trace or ground plane connected to the GND pin. Additionally, bypass the PVDD pin using a **bulk capacitor** C_{PVDD2} rated for PVDD. This component can be electrolytic. This capacitance must be at least 10 μ F. It is acceptable if this capacitance is shared with the bulk capacitance for the external power MOSFETs.

Additional bulk capacitance is required to bypass the high current path on the external power MOSFETs of the H-bridge driver. Place this bulk capacitance such that the length of any high current paths is minimized through the external MOSFETs. Keep the connecting metal traces as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

For H-bridge driver external MOSFETs, bypass the drain pin to GND plane using a low-ESR ceramic bypass capacitor with appropriate voltage rating. Place this capacitor as close to the MOSFET drain and source pins as possible, with a thick trace or plane connection to GND plane. Place the series gate resistors as close to the MOSFET gate pins as possible.

Bypass the DVDD pin to the DGND pin with C_{DVDD} . Place this capacitor as close to the pin as possible and minimize the path from the capacitor to the DGND pin. If local bypass capacitors are already present on these power supplies in close proximity of the device to minimize noise, these additional components for DVDD are not required.

For the EC driver, place both the C_{ECDRV} and C_{ECFB} bypass capacitors to GND as close to the respective pins as possible.

Minimize the loop length for the high-side and low-side gate drivers. The high-side loop is from the GHx pin of the device to the high-side power MOSFET gate, then follows the high-side MOSFET source back to the SHx pin. The low-side loop is from the GLx pin of the device to the low-side power MOSFET gate, then follows the low-side MOSFET source back to the SL pin.

9.5.2 Layout Example

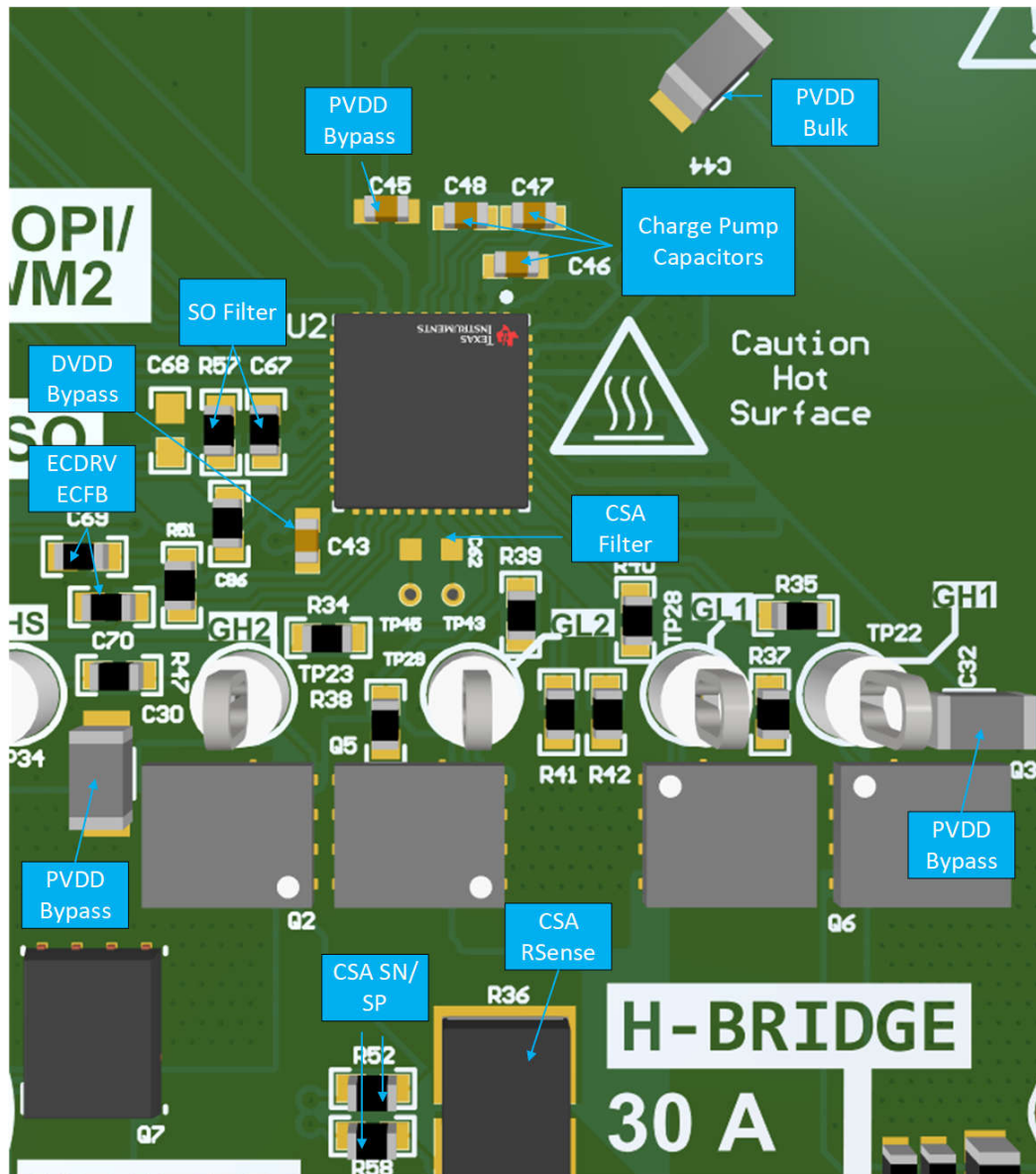


Figure 9-3. DRV8001-Q1 Component Placement and Layout

The layout screen shot above shows the device component and layout relative to the device. This layout screen shot comes from the device evaluation module. Note that all power supply decoupling capacitors, especially smaller values, and charge pump capacitors are placed as closed to the pins as possible and are placed on the same layer of the device. All general guidelines outlined in the previous section were followed in the evaluation module layout design when possible.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop designs are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.3 Trademarks

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10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

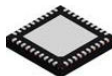
11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2025	*	Initial release.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

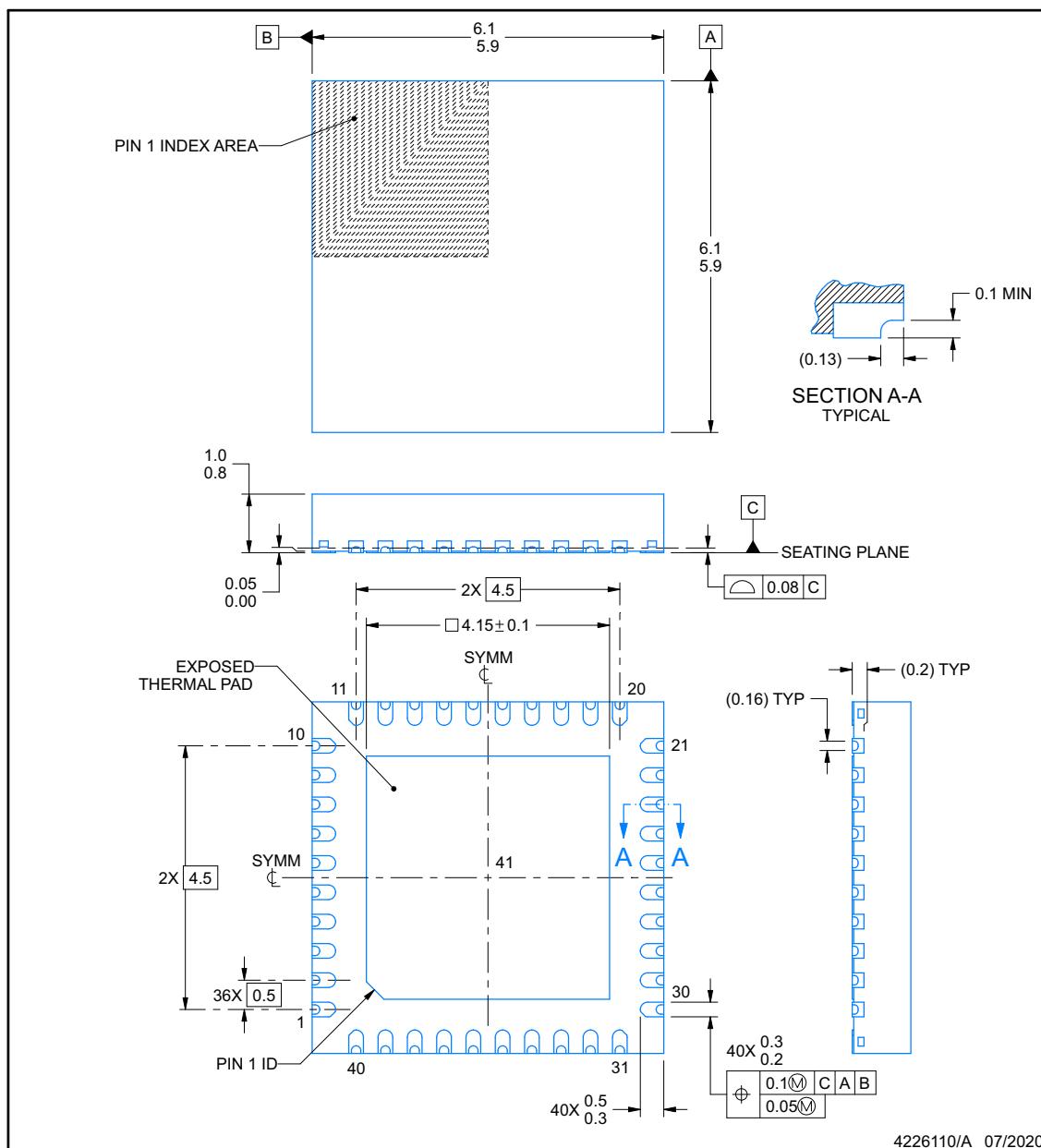


RHA0040M

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



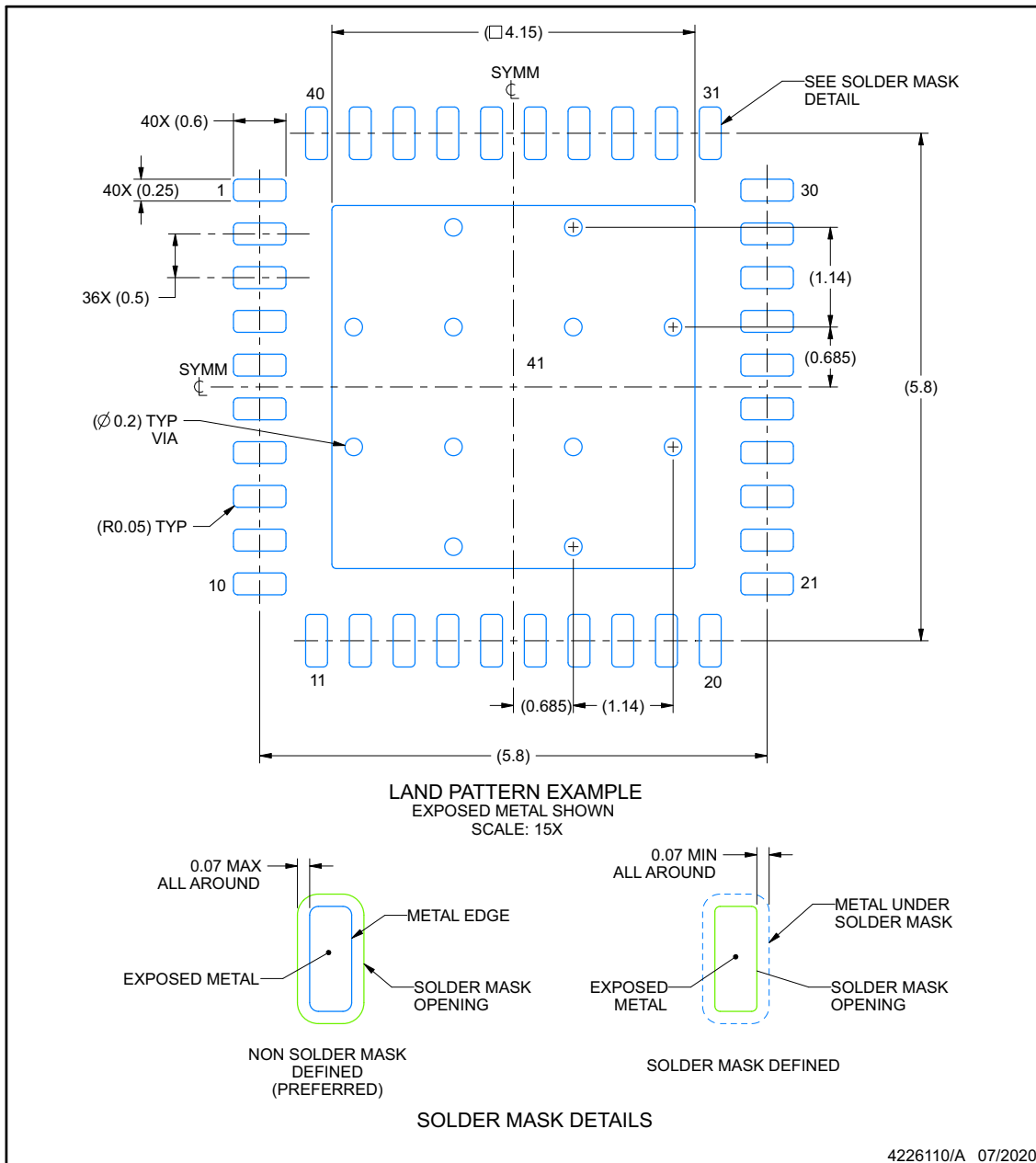
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

RHA0040M

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

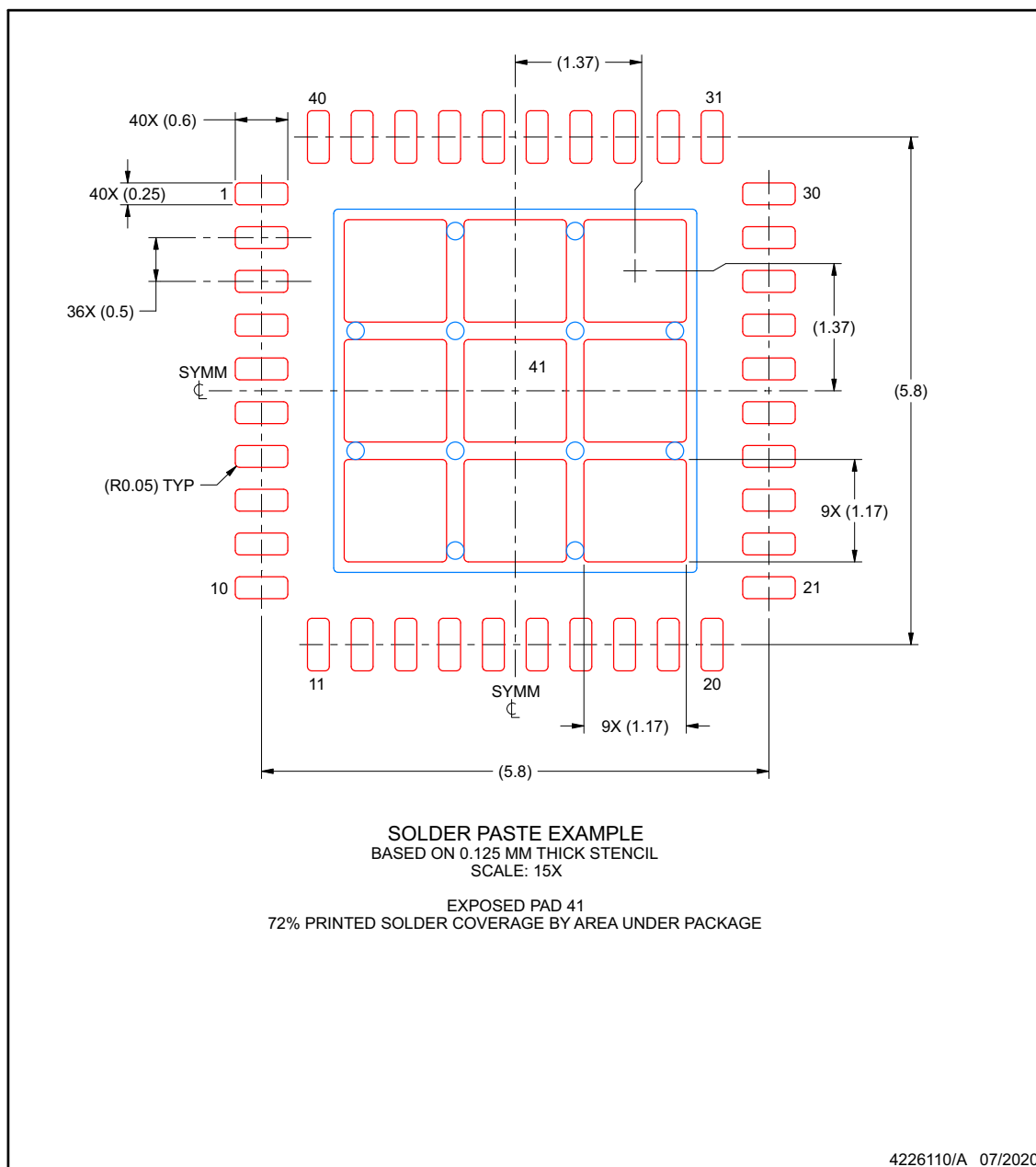
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHA0040M

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

12.1 Package Option Addendum

Packaging Information

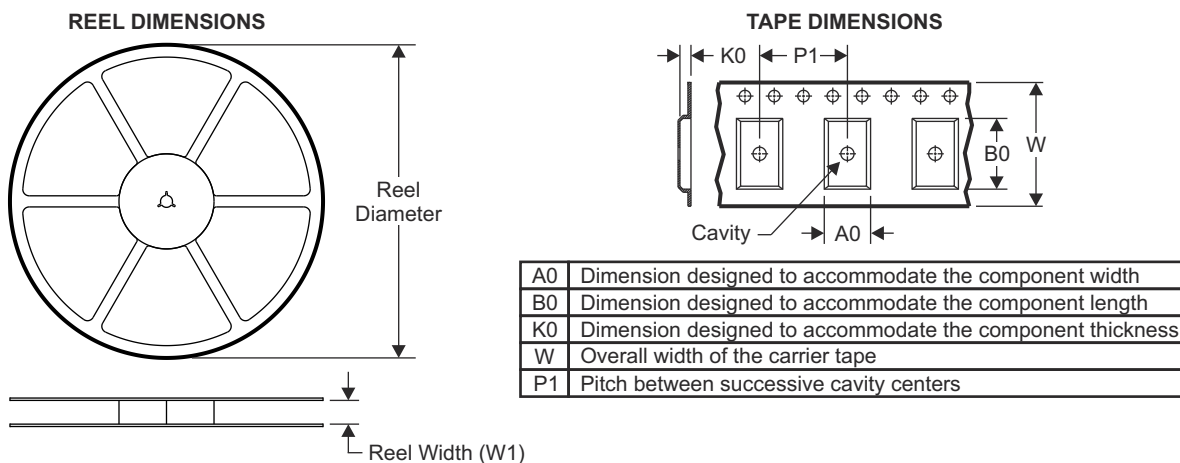
Orderable Device	Status	Package Type ⁽¹⁾	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish ⁽⁶⁾	MSL Peak Temp ⁽³⁾	Op Temp (°C)	Device Marking ^{(4) (5)}
DRV8001QWR HARQ1	PREVIEW	VQFN	RHA	40	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PDRV8001-Q1

- (1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).
- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

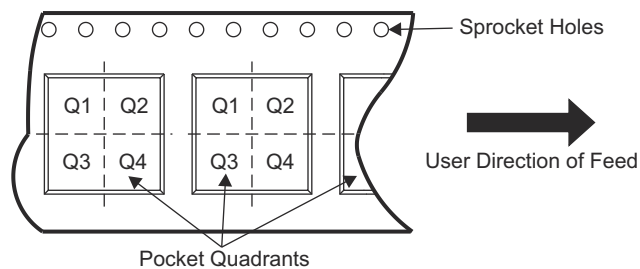
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12.2 Tape and Reel Information

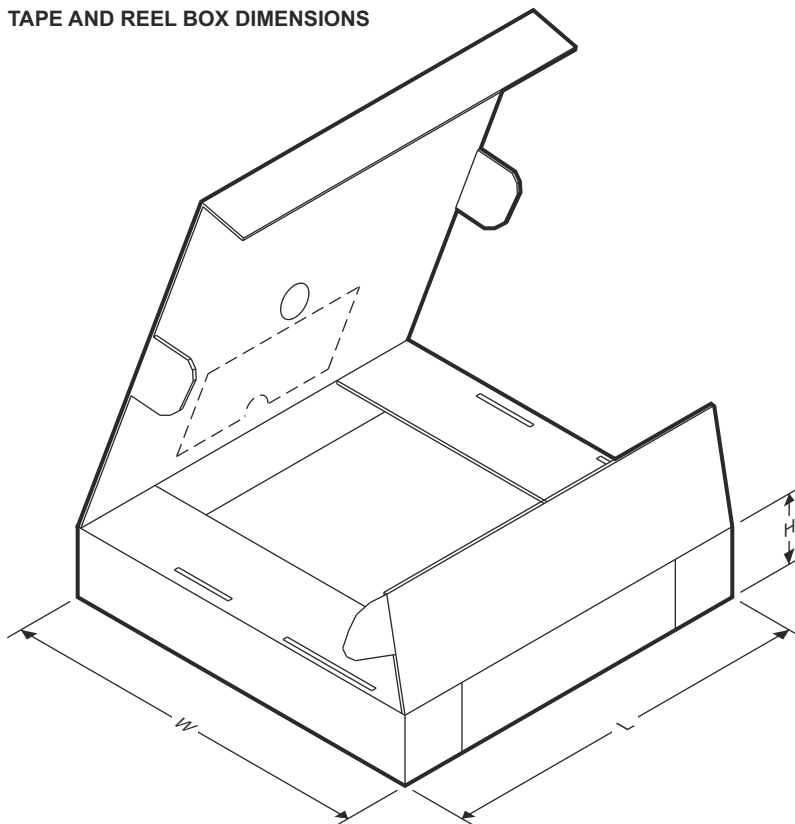


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8001QWRHARQ1	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12	16	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8001QWRHARQ1	VQFN	RHA	40	2500	367	367	35

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PDRV8001QWRHARQ1	Active	Preproduction	VQFN (RHA) 40	2500 LARGE T&R	-	Call TI	Call TI	-40 to 125	
PDRV8001QWRHARQ1.A	Active	Preproduction	VQFN (RHA) 40	2500 LARGE T&R	-	Call TI	Call TI	-40 to 125	

- ⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).
- ⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- ⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- ⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- ⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- ⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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GENERIC PACKAGE VIEW

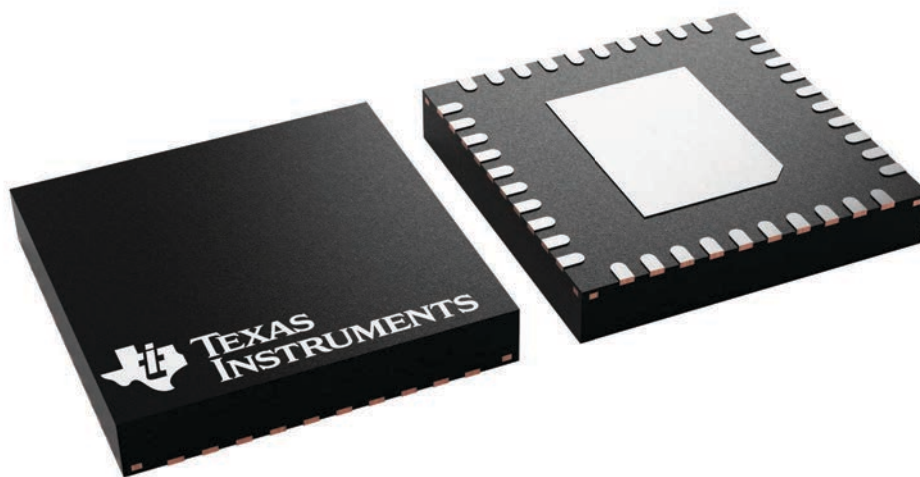
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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