











Instruments

SLIS152G - MAY 2014 - REVISED SEPTEMBER 2016

DRV5033

DRV5033 Digital-Omnipolar-Switch Hall Effect Sensor

Features

- Digital Omnipolar-Switch Hall Sensor
- Superior Temperature Stability
 - B_{OP} ±10% Over Temperature
- Multiple Sensitivity Options (B_{OP} / B_{RP}):
 - ±3.5 / ±2 mT (FA, see Device Nomenclature)
 - ±6.9 / ±3.5 mT (AJ, see Device Nomenclature)
- **Detects North and South Magnetic Field**
- Supports a Wide Voltage Range
 - 2.5 to 38 V
 - No External Regulator Required
- Wide Operating Temperature Range
 - T_A = -40 to 125°C (Q, see *Device* Nomenclature)
- Open Drain Output (30-mA Sink)
- Fast 35-µs Power-On Time
- Small Package and Footprint
 - Surface Mount 3-Pin SOT-23 (DBZ)
 - 2.92 mm × 2.37 mm
 - Through-Hole 3-Pin TO-92 (LPG)
 - $-4.00 \text{ mm} \times 3.15 \text{ mm}$

Protection Features

- Reverse Supply Protection (up to -22 V)
- Supports up to 40-V Load Dump
- **Output Short-Circuit Protection**
- Output Current Limitation

2 Applications

- **Docking Detection**
- Door Open and Close Detection
- **Proximity Sensing**
- Valve Positioning
- **Pulse Counting**

3 Description

The DRV5033 device is a chopper-stabilized Hall Effect Sensor that offers a magnetic sensing solution with superior sensitivity stability over temperature and integrated protection features.

The DRV5033 responds the same to both polarities of magnetic field direction. When the applied magnetic flux density exceeds the BOP threshold, the DRV5033 open-drain output goes low. The output stays low until the field decreases to less than B_{RP}, and then the output goes to high impedance. The output current sink capability is 30 mA. A wide operating voltage range from 2.5 to 38 V with reverse polarity protection up to -22 V makes the device suitable for a wide range of industrial applications.

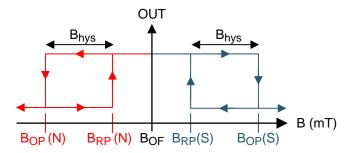
Internal protection functions are provided for reverse supply conditions, load dump, and output short circuit or over current.

Device Information⁽¹⁾

_		
PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV5033	SOT-23 (3)	2.92 mm × 1.30 mm
DK V 5033	TO-92 (3)	4.00 mm × 3.15 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Output State



Device Packages

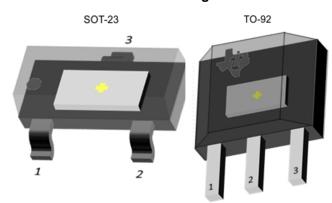




Table of Contents

1	Features 1		7.3 Feature Description	10
2	Applications 1		7.4 Device Functional Modes	15
3	Description 1	8	Application and Implementation	16
4	Revision History2		8.1 Application Information	16
5	Pin Configuration and Functions 4		8.2 Typical Applications	16
6	Specifications5	9	Power Supply Recommendations	18
	6.1 Absolute Maximum Ratings	10	Layout	. 19
	6.2 ESD Ratings		10.1 Layout Guidelines	19
	6.3 Recommended Operating Conditions		10.2 Layout Example	19
	6.4 Thermal Information5	11	Device and Documentation Support	20
	6.5 Electrical Characteristics		11.1 Device Support	20
	6.6 Switching Characteristics		11.2 Receiving Notification of Documentation Update	s 21
	6.7 Magnetic Characteristics 6		11.3 Community Resources	21
	6.8 Typical Characteristics		11.4 Trademarks	21
7	Detailed Description9		11.5 Electrostatic Discharge Caution	21
	7.1 Overview 9		11.6 Glossary	21
	7.2 Functional Block Diagram9	12	Mechanical, Packaging, and Orderable Information	21

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (May 2016) to Revision G	Page
Changed the power-on time for the FA version in the Electrical Characteristics to	able6
Added the Layout section	19
Added the Receiving Notification of Documentation Updates section	21
Changes from Revision E (February 2016) to Revision F	Page
Revised preliminary limits for the FA version	6
Changes from Revision D (December 2015) to Revision E	Page
Added the FA device option	1
Added the typical bandwidth value to the Magnetic Characteristics table	6
Changes from Revision C (May 2015) to Revision D	Page
Corrected body size of SOT-23 package and SIP package name to TO-92	1
Added B _{MAX} to Absolute Maximum Ratings	5
Removed table note from junction temperature	5
Updated package tape and reel options for M and blank	20
Added Community Resources	21
Changes from Revision B (September 2014) to Revision C	Page
Updated device status to production data	1

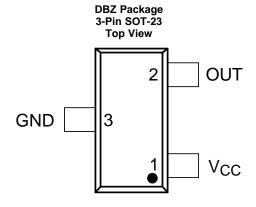


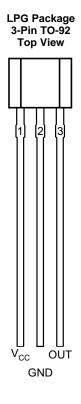
Changes from Revision A (August 2014) to Revision B	Page
Changed the maximum T _J value to 150°C	5
 Added typical rise and fall time and removed maximum value in Switching Character 	ristics6
Updated the Magnetic Characteristics values	
Updated all Typical Characteristics graphs	
Updated Equation 4	17
• Opuated Equation 4	
Changes from Original (May 2014) to Revision A	Page
Changes from Original (May 2014) to Revision A • Changed High Sensitivity Options: +6.9 / +2.3 mT (AJ) to +6.9 / +3.5 mT (AJ)	1
Changes from Original (May 2014) to Revision A Changed High Sensitivity Options: +6.9 / +2.3 mT (AJ) to +6.9 / +3.5 mT (AJ) Changed the maximum T _J value from 175°C to 150°C	
Changes from Original (May 2014) to Revision A Changed High Sensitivity Options: +6.9 / +2.3 mT (AJ) to +6.9 / +3.5 mT (AJ) Changed the maximum T _J value from 175°C to 150°C	
Changes from Original (May 2014) to Revision A Changed High Sensitivity Options: +6.9 / +2.3 mT (AJ) to +6.9 / +3.5 mT (AJ) Changed the maximum T _J value from 175°C to 150°C	



5 Pin Configuration and Functions

For additional configuration information, see *Device Markings* and *Mechanical, Packaging, and Orderable Information*.





Pin Functions

	PIN		TYPE	DESCRIPTION	
NAME DBZ LPG		LPG	ITPE	DESCRIPTION	
GND	3	2	GND	Ground pin	
OUT	OUT 2 3		Output	Hall sensor open-drain output. The open drain requires a resistor pullup.	
V _{CC}	1	1	PWR	2.5 to 38 V power supply. Bypass this pin to the GND pin with a 0.01- μ F (minimum) ceramic capacitor rated for V _{CC} .	

Product Folder Links: DRV5033

Copyright © 2014–2016, Texas Instruments Incorporated



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
	V _{cc}	-22 ⁽²⁾	40	V
Power supply voltage	Voltage ramp rate (V _{CC}), V _{CC} < 5 V	Unlir	nited	1////
	Voltage ramp rate (V _{CC}), V _{CC} > 5 V	0	2	- V/μs
Output pin voltage		-0.5	40	V
Output pin reverse current durin	g reverse supply condition	0	100	mA
Magnetic flux density, B _{MAX}		Unlir	mited	
Operating junction temperature,	T _J	-40	150	°C
Storage temperature, T _{stg}		-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
\/	Electrostatic	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2500	.,
V _{(ES}	^{SD)} discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Power supply voltage	2.5	38	٧
Vo	Output pin voltage (OUT)	0	38	٧
I _{SINK}	Output pin current sink (OUT) ⁽¹⁾	0	30	mA
T _A	Operating ambient temperature	-40	125	ô

⁽¹⁾ Power dissipation and thermal limits must be observed

6.4 Thermal Information

			DRV	5033	
	THERMAL METRIC ⁽¹⁾	DBZ (Sc	OT-23)	LPG (TO-92)	UNIT
		3 PI	NS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	333	3.2	180	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	99.	.9	98.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.	.9	154.9	°C/W
ΨЈТ	Junction-to-top characterization parameter	4.9	9	40	°C/W
ΨЈВ	Junction-to-board characterization parameter	65.	.2	154.9	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

⁽²⁾ Ensured by design. Only tested to -20 V.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER	SUPPLIES (V _{CC})					
V _{CC}	V _{CC} operating voltage		2.5		38	V
	On a mating a committee or comment	V _{CC} = 2.5 to 38 V, T _A = 25°C		2.7		Λ
I _{CC}	Operating supply current	V _{CC} = 2.5 to 38 V, T _A = 125°C		3	3.6 50 70	mA
	Davisa on time	AJ version		35		
t _{on}	Power-on time	FA version		35	70	μs
OPEN DI	RAIN OUTPUT (OUT)				•	
_	EET on vocietores	$V_{CC} = 3.3 \text{ V}, I_{O} = 10 \text{ mA}, T_{A} = 25^{\circ}\text{C}$		22		0
r _{DS(on)}	FET on-resistance	$V_{CC} = 3.3 \text{ V}, I_{O} = 10 \text{ mA}, T_{A} = 125 ^{\circ}\text{C}$		36	50	Ω
I _{lkg(off)}	Off-state leakage current	Output Hi-Z			1	μA
PROTEC	TION CIRCUITS				·	
V _{CCR}	Reverse supply voltage		-22			V
I _{OCP}	Overcurrent protection level	OUT shorted V _{CC}	15	30	45	mA

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
OPEN DRAIN OUTPUT (OUT)							
t _d	Output delay time	$B = B_{RP} - 10 \text{ mT to } B_{OP} + 10 \text{ mT in } 1 \mu\text{s}$		13	25	μs	
t _r	Output rise time (10% to 90%)	R1 = 1 k Ω , C _O = 50 pF, V _{CC} = 3.3 V		200		ns	
t _f	Output fall time (90% to 10%)	R1 = 1 k Ω , C _O = 50 pF, V _{CC} = 3.3 V		31		ns	

6.7 Magnetic Characteristics

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT ⁽¹⁾
f_{BW}	Bandwidth ⁽²⁾		20	30		kHz
DRV503	3FA: ±3.5 / ±2 mT					
B _{OP}	Operate point; see Figure 12		±1.8	±3.5	±6.8	mT
B _{RP}	Release point; see Figure 12	T 40%C += 405%C	±0.5	±2	±4.2	mT
B _{hys}	Hysteresis; $B_{hys} = (B_{OP} - B_{RP})^{(3)}$	T _A = -40°C to 125°C		±1.5		mT
B _O	Magnetic offset; $B_O = (B_{OP} + B_{RP}) / 2$			±2.8		mT
DRV503	3AJ: ±6.9 / ±3.5 mT					
B _{OP}	Operate point; see Figure 12		±3	±6.9	±12	mT
B _{RP}	Release point; see Figure 12	T 4000 to 40500	±1	±3.5	±5	mT
B _{hys}	Hysteresis; B _{hys} = (B _{OP} – B _{RP}) ⁽³⁾	$T_A = -40^{\circ}\text{C to } 125^{\circ}\text{C}$		3.4		mT
B _O	Magnetic offset; $B_O = (B_{OP} + B_{RP}) / 2$			5.2		mT

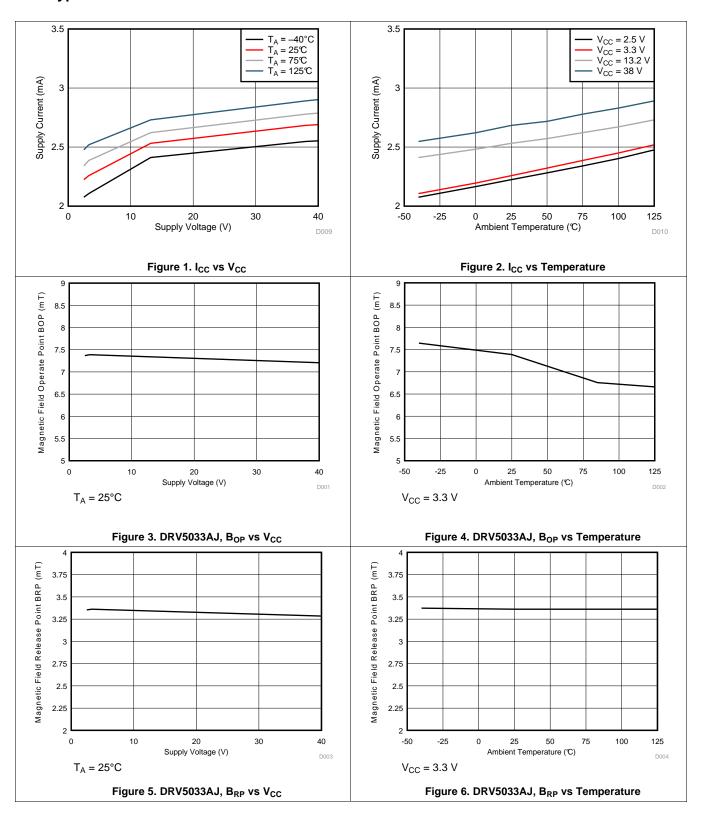
^{(1) 1} mT = 10 Gauss

⁽²⁾ Bandwidth describes the fastest changing magnetic field that can be detected and translated to the output.

^{(3) |}B_{OP}| is always greater than |B_{RP}|.



6.8 Typical Characteristics

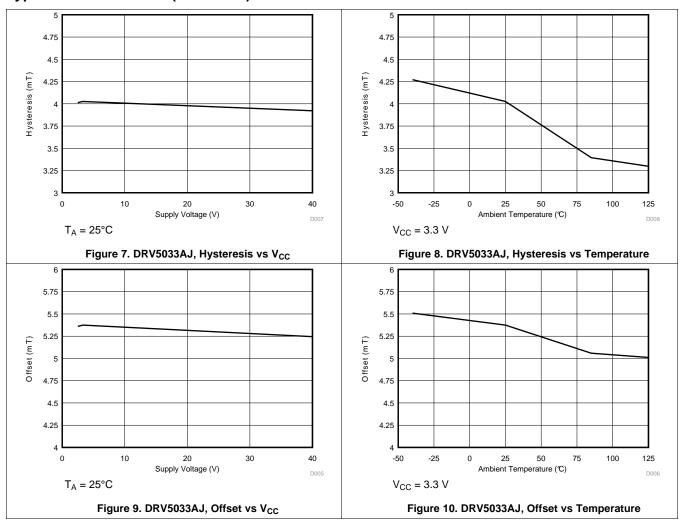


Copyright © 2014–2016, Texas Instruments Incorporated

Submit Documentation Feedback

TEXAS INSTRUMENTS

Typical Characteristics (continued)





7 Detailed Description

7.1 Overview

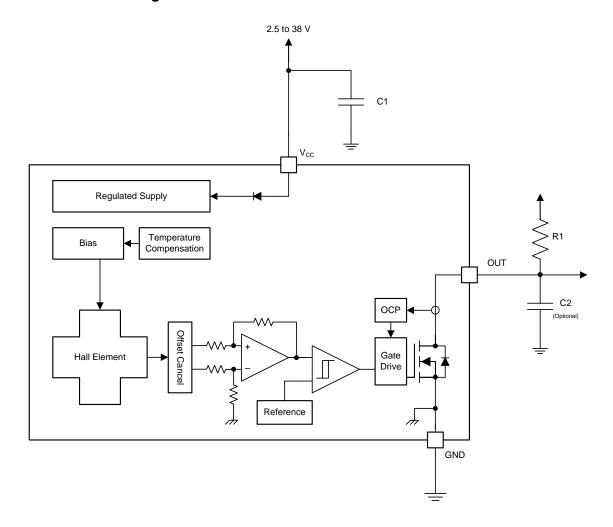
The DRV5033 device is a chopper-stabilized hall sensor with a digital omnipolar switch output for magnetic sensing applications. The DRV5033 device can be powered with a supply voltage between 2.5 and 38 V, and will survive -22 V reverse battery conditions continuously. Note that the DRV5033 device will not be operating when about -22 to 2.4 V is applied to V_{CC} (with respect to GND). In addition, the device can withstand voltages up to 40 V for transient durations.

The field polarity is defined as follows: a south pole near the marked side of the package is a positive magnetic field. A north pole near the marked side of the package is a negative magnetic field.

The omnipolar configuration allows the hall sensor to respond to either a south or north pole. A strong magnetic field of either polarity will cause the output to pull low (operate point, B_{OP}), and a weaker magnetic field will cause the output to release (release point, B_{RP}). Hysteresis is included in between the operate and release points, so magnetic field noise will not trip the output accidentally.

An external pullup resistor is required on the OUT pin. The OUT pin can be pulled up to V_{CC} , or to a different voltage supply. This allows for easier interfacing with controller circuits.

7.2 Functional Block Diagram





7.3 Feature Description

7.3.1 Field Direction Definition

A positive magnetic field is defined as a south pole near the marked side of the package as shown in Figure 11.

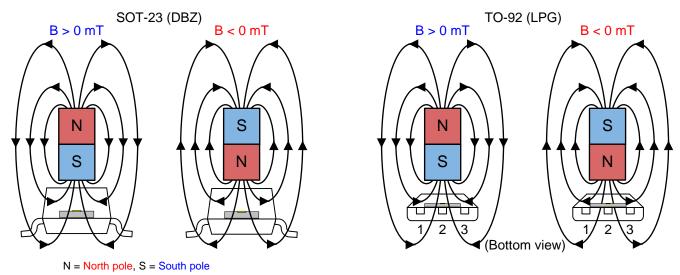


Figure 11. Field Direction Definition

7.3.2 Device Output

If the device is powered on with a magnetic field strength between B_{RP} and B_{OP} , then the device output is indeterminate and can either be Hi-Z or Low. If the field strength is greater than B_{OP} , then the output is pulled low. If the field strength is less than B_{RP} , then the output is released.

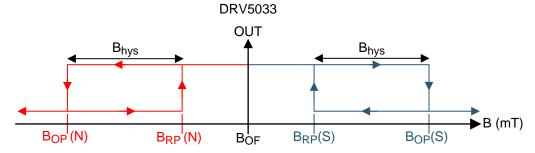


Figure 12. DRV5033— $B_{OP} > 0$

Product Folder Links: DRV5033

Submit Documentation Feedback

10



7.3.3 Power-On Time

After applying V_{CC} to the DRV5033 device, t_{on} must elapse before the OUT pin is valid. During the power-up sequence, the output is Hi-Z. A pulse as shown in Figure 13 and Figure 14 occurs at the end of t_{on} . This pulse can allow the host processor to determine when the DRV5033 output is valid after startup. In Case 1 (Figure 13) and Case 2 (Figure 14), the output is defined assuming a constant magnetic field B > B_{OP} and B < B_{RP}.

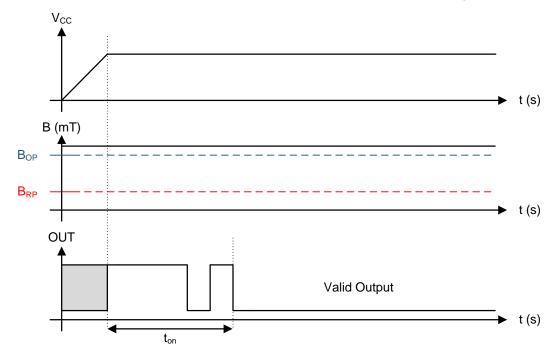


Figure 13. Case 1: Power On When $B > B_{OP}$

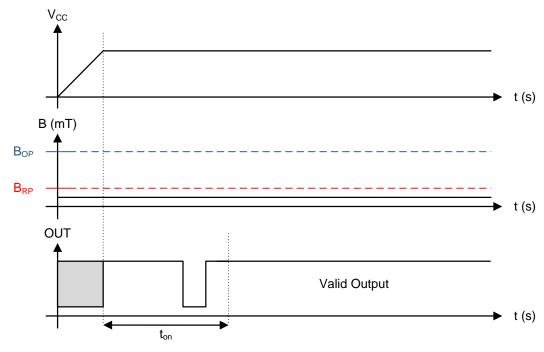


Figure 14. Case 2: Power On When $B < B_{RP}$

Copyright © 2014–2016, Texas Instruments Incorporated

Submit Documentation Feedback



If the device is powered on with the magnetic field strength $B_{RP} < B < B_{OP}$, then the device output is indeterminate and can either be Hi-Z or pulled low. During the power-up sequence, the output is held Hi-Z until t_{on} has elapsed. At the end of t_{on} , a pulse is given on the OUT pin to indicate that t_{on} has elapsed. After t_{on} , if the magnetic field changes such that $B_{OP} < B$, the output is released. Case 3 (Figure 15) and Case 4 (Figure 16) show examples of this behavior.

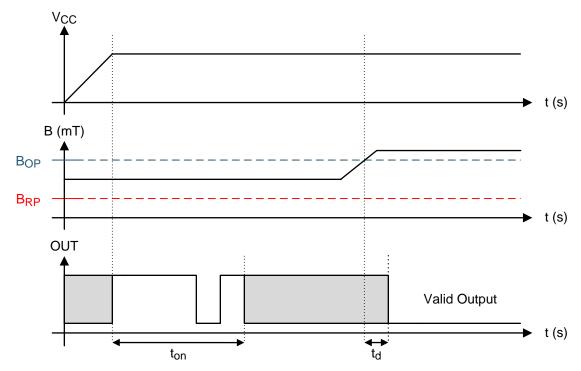


Figure 15. Case 3: Power On When $B_{RP} < B < B_{OP}$, Followed by $B > B_{OP}$

Submit Documentation Feedback

Copyright © 2014–2016, Texas Instruments Incorporated



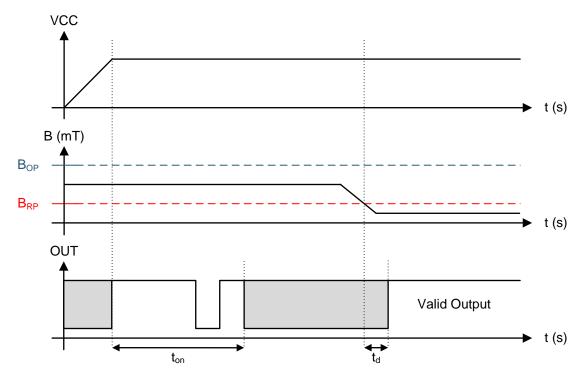


Figure 16. Case 4: Power On When $B_{RP} < B < B_{OP}$, Followed by $B < B_{RP}$

7.3.4 Output Stage

The DRV5033 output stage uses an open-drain NMOS, and it is rated to sink up to 30 mA of current. For proper operation, calculate the value of the pullup resistor R1 using Equation 1.

$$\frac{V_{ref} max}{30 mA} \le R1 \le \frac{V_{ref} min}{100 \mu A}$$
 (1)

The size of R1 is a tradeoff between the OUT rise time and the current when OUT is pulled low. A lower current is generally better, however faster transitions and bandwidth require a smaller resistor for faster switching.

In addition, ensure that the value of R1 > 500 Ω to ensure the output driver can pull the OUT pin close to GND.

NOTE

 V_{ref} is not restricted to V_{CC} . The allowable voltage range of this pin is specified in the Absolute Maximum Ratings.

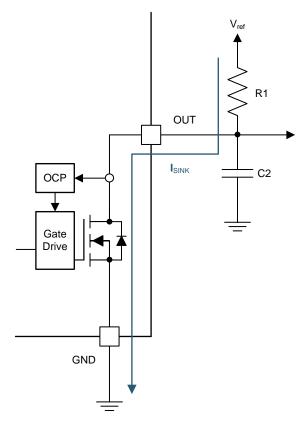


Figure 17.

Select a value for C2 based on the system bandwidth specifications as shown in Equation 2.

$$2 \times f_{\text{BW}} \text{ (Hz)} < \frac{1}{2\pi \times \text{R1} \times \text{C2}}$$
 (2)

Most applications do no require this C2 filtering capacitor.



7.3.5 Protection Circuits

The DRV5033 device is fully protected against overcurrent and reverse-supply conditions.

7.3.5.1 Overcurrent Protection (OCP)

An analog current-limit circuit limits the current through the FET. The driver current is clamped to I_{OCP} . During this clamping, the $r_{DS(on)}$ of the output FET is increased from the nominal value.

7.3.5.2 Load Dump Protection

The DRV5033 device operates at DC V_{CC} conditions up to 38 V nominally, and can additionally withstand V_{CC} = 40 V. No current-limiting series resistor is required for this protection.

7.3.5.3 Reverse Supply Protection

The DRV5033 device is protected in the event that the V_{CC} pin and the GND pin are reversed (up to -22 V).

NOTE

In a reverse supply condition, the OUT pin reverse-current must not exceed the ratings specified in the *Absolute Maximum Ratings*.

Table 1.

FAULT	CONDITION	DEVICE	DESCRIPTION	RECOVERY
FET overload (OCP)	I _{SINK} ≥ I _{OCP}	Operating	Output current is clamped to I _{OCP}	I _O < I _{OCP}
Load dump	38 V < V _{CC} < 40 V	Operating	Device will operate for a transient duration	V _{CC} ≤ 38 V
Reverse supply	-22 V < V _{CC} < 0 V	Disabled	Device will survive this condition	V _{CC} ≥ 2.5 V

7.4 Device Functional Modes

The DRV5033 device is active only when V_{CC} is between 2.5 and 38 V.

When a reverse supply condition exists, the device is inactive.



8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV5033 device is used in magnetic-field sensing applications.

8.2 Typical Applications

8.2.1 Standard Circuit

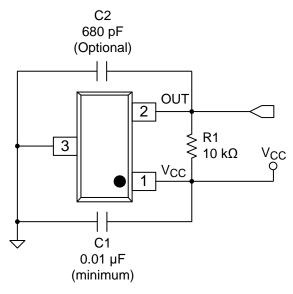


Figure 18. Typical Application Circuit

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE			
Supply voltage	V _{CC}	3.2 to 3.4 V			
System bandwidth	f_{BW}	10 kHz			

8.2.1.2 Detailed Design Procedure

Table 3. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C1	V _{CC}	GND	A 0.01-μF (minimum) ceramic capacitor rated for V _{CC}
C2	OUT	GND	Optional: Place a ceramic capacitor to GND
R1	OUT	REF ⁽¹⁾	Requires a resistor pullup

 REF is not a pin on the DRV5033 device, but a REF supply-voltage pullup is required for the OUT pin; the OUT pin may be pulled up to V_{CC}.



8.2.1.2.1 Configuration Example

In a 3.3-V system, 3.2 V \leq V_{ref} \leq 3.4 V. Use Equation 3 to calculate the allowable range for R1.

$$\frac{V_{ref} max}{30 mA} \le R1 \le \frac{V_{ref} min}{100 \mu A}$$
(3)

For this design example, use Equation 4 to calculate the allowable range of R1.

$$\frac{3.4 \text{ V}}{30 \text{ mA}} \le \text{R1} \le \frac{3.2 \text{ V}}{100 \text{ \muA}}$$
 (4)

Therefore:

$$113 \Omega \le R1 \le 32 k\Omega \tag{5}$$

After finding the allowable range of R1 (Equation 5), select a value between 500 Ω and 32 k Ω for R1.

Assuming a system bandwidth of 10 kHz, use Equation 6 to calculate the value of C2.

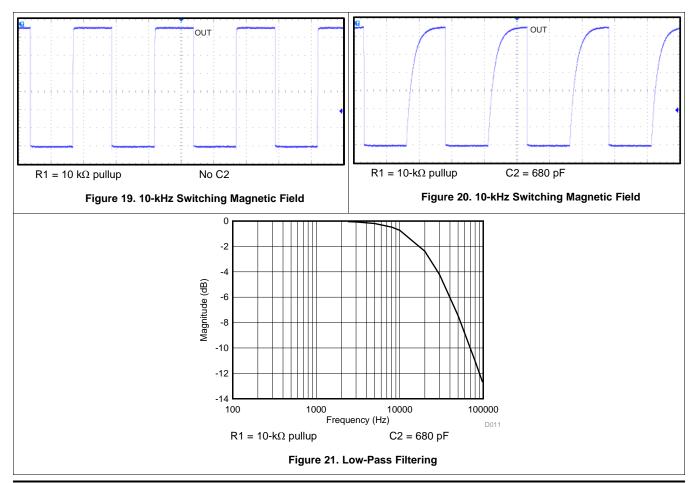
$$2 \times f_{\text{BW}} \text{ (Hz)} < \frac{1}{2\pi \times \text{R1} \times \text{C2}}$$
 (6)

For this design example, use Equation 7 to calculate the value of C2.

$$2 \times 10 \text{ kHz} < \frac{1}{2\pi \times R1 \times C2} \tag{7}$$

An R1 value of 10 k Ω and a C2 value less than 820 pF satisfy the requirement for a 10-kHz system bandwidth. A selection of R1 = 10 k Ω and C2 = 680 pF would cause a low-pass filter with a corner frequency of 23.4 kHz.

8.2.1.3 Application Curves



Copyright © 2014–2016, Texas Instruments Incorporated

Submit Documentation Feedback



8.2.2 Alternative Two-Wire Application

For systems that require minimal wire count, the device output can be connected to V_{CC} through a resistor, and the total supplied current can be sensed near the controller.

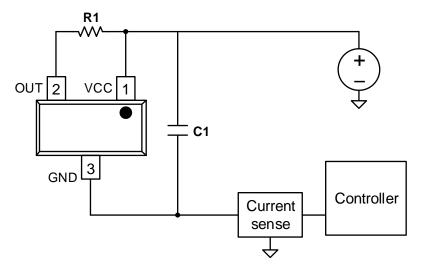


Figure 22. 2-Wire Application

Current can be sensed using a shunt resistor or other circuitry.

8.2.2.1 Design Requirements

Table 4 lists the related design parameters.

 DESIGN PARAMETER
 REFERENCE
 EXAMPLE VALUE

 Supply voltage
 V_{CC} 12 V

 OUT resistor
 R1
 1 k Ω

 Bypass capacitor
 C1
 0.1 μ F

 Current when B < B_RP</td>
 I_RELEASE
 About 3 mA

IOPERATE

Table 4. Design Parameters

8.2.2.2 Detailed Design Procedure

Current when B > BOP

When the open-drain output of the device is high-impedance, current through the path equals the I_{CC} of the device (approximately 3 mA).

When the output pulls low, a parallel current path is added, equal to V_{CC} / (R1 + $r_{DS(on)}$). Using 12 V and 1 k Ω , the parallel current is approximately 12 mA, making the total current approximately 15 mA.

The local bypass capacitor C1 should be at least 0.1 μ F, and a larger value if there is high inductance in the power line interconnect.

9 Power Supply Recommendations

The DRV5033 device is designed to operate from an input voltage supply (VM) range between 2.5 and 38 V. A 0.01- μ F (minimum) ceramic capacitor rated for V_{CC} must be placed as close to the DRV5033 device as possible.

Product Folder Links: DRV5033

About 15 mA



10 Layout

10.1 Layout Guidelines

The bypass capacitor should be placed near the DRV5033 device for efficient power delivery with minimal inductance. The external pullup resistor should be placed near the microcontroller input to provide the most stable voltage at the input; alternatively, an integrated pullup resistor within the GPIO of the microcontroller can be used.

Generally, using PCB copper planes underneath the DRV5033 device has no effect on magnetic flux, and does not interfere with device performance. This is because copper is not a ferromagnetic material. However, If nearby system components contain iron or nickel, they may redirect magnetic flux in unpredictable ways.

10.2 Layout Example

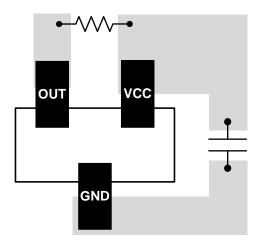


Figure 23. DRV5033 Layout Example



11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

Figure 24 shows a legend for reading the complete device name for and DRV5033 device.

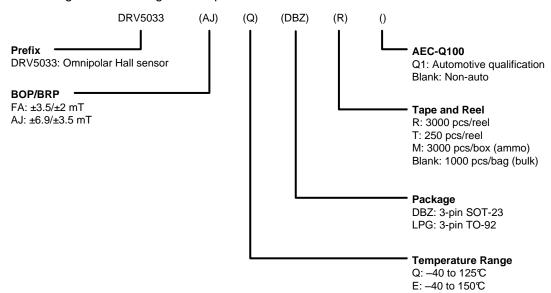


Figure 24. Device Nomenclature

11.1.2 Device Markings

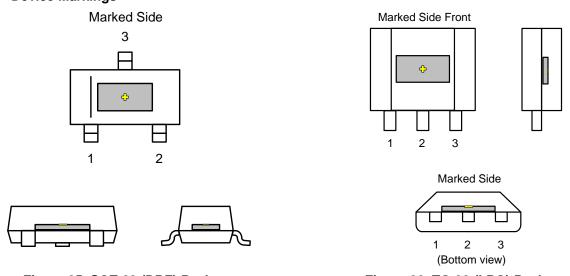


Figure 25. SOT-23 (DBZ) Package

Figure 26. TO-92 (LPG) Package

indicates the Hall effect sensor (not to scale). The Hall element is located in the center of the package with a tolerance of ±100 μm. The height of the Hall element from the bottom of the package is 0.7 mm ±50 μm in the DBZ package and 0.987 mm ±50 μm in the LPG package.



11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com 10-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
DRV5033AJQDBZR	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	NIPDAUAG SN	Level-1-260C-UNLIM	-40 to 125	(+QLAJ, 1J72)
DRV5033AJQDBZR.A	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(+QLAJ, 1J72)
DRV5033AJQDBZT	Obsolete	Production	SOT-23 (DBZ) 3	-	-	Call TI	Call TI	-40 to 125	(+QLAJ, 1J72)
DRV5033AJQLPG	Active	Production	TO-92 (LPG) 3	1000 BULK	Yes	SN	N/A for Pkg Type	-40 to 125	+QLAJ
DRV5033AJQLPG.A	Active	Production	TO-92 (LPG) 3	1000 BULK	Yes	SN	N/A for Pkg Type	-40 to 125	+QLAJ
DRV5033AJQLPGM	Active	Production	TO-92 (LPG) 3	3000 AMMO	Yes	SN	N/A for Pkg Type	-40 to 125	+QLAJ
DRV5033AJQLPGM.A	Active	Production	TO-92 (LPG) 3	3000 AMMO	Yes	SN	N/A for Pkg Type	-40 to 125	+QLAJ
DRV5033FAQDBZR	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(+QLFA, 1J8W)
DRV5033FAQDBZR.A	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(+QLFA, 1J8W)

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

www.ti.com 10-Nov-2025

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF DRV5033:

Automotive : DRV5033-Q1

NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

www.ti.com 3-Jul-2025

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV5033AJQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.2	2.85	1.3	4.0	8.0	Q3
DRV5033AJQDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
DRV5033FAQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.2	2.85	1.3	4.0	8.0	Q3

www.ti.com 3-Jul-2025



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV5033AJQDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
DRV5033AJQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
DRV5033FAQDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0



TRANSISTOR OUTLINE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.



TRANSISTOR OUTLINE



TRANSISTOR OUTLINE





SMALL OUTLINE TRANSISTOR



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 This drawing is subject to change without notice.
 Reference JEDEC registration TO-236, except minimum foot length.

- 4. Support pin may differ or may not be present.
- 5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025