DRV2901 Single-Channel PWM-input Piezo Transducer Driver for Ultrasonic Cleaning with Wide Supply Voltage

1 Features

- Wide 12V to 48V supply voltage operation
- Supports up to 50W peak power
- High-Efficiency Power Stage with 90mΩ Output MOSFETs
- Power-On Reset for Protection on Power Up Without Any Power-Supply Sequencing
- Integrated Self-Protection Circuits Including
  - Undervoltage protection
  - Over temperature protection
  - Overload protection
  - Short Circuit protection
- Available in 44-pin HTSSOP package (DDV)

2 Applications

- Thermal Imaging Camera
- Traffic Monitoring Camera
- Machine Vision Camera
- Wireless Security Camera
- Drone Vision

3 Description

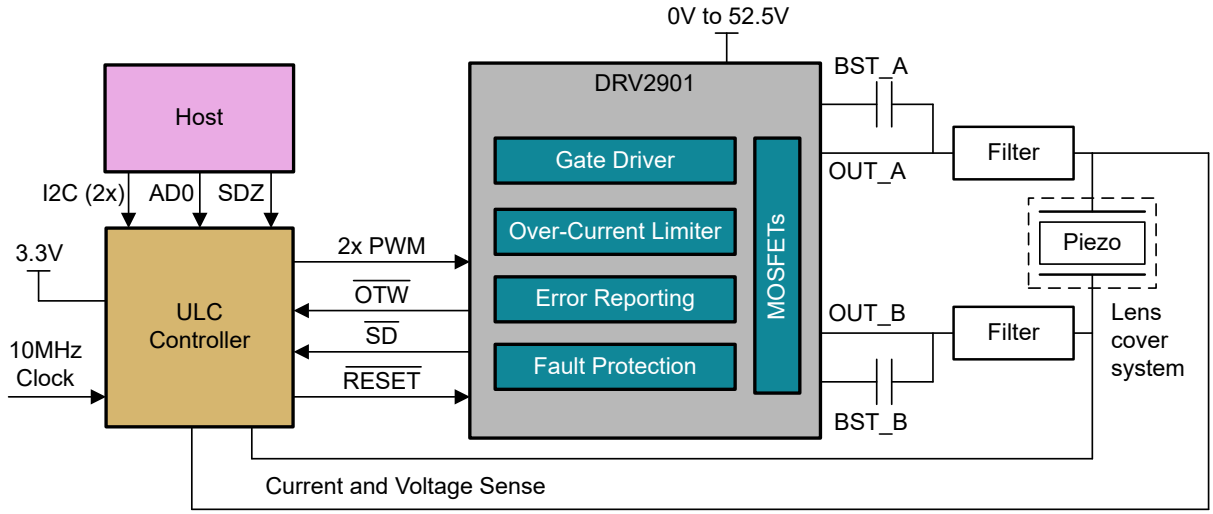
The DRV2901 is a high-performance lens cleaner transducer driver. This system only requires a simple passive LC demodulation filter to deliver high-quality, high-efficiency amplification with proven EMI compliance. This device requires two power supplies, at 12V for GVDD and VDD, and 12V to 48V for PVDD. The DRV2901 does not require power-up sequencing due to an internal power-on reset.

The DRV2901 has an remarkable protection system integrated on-chip, safeguarding the device against a wide range of fault conditions that can damage the system. These safeguards are short-circuit protection, overcurrent protection, undervoltage protection, and overtemperature protection. The DRV2901 has a new proprietary current-limiting circuit that reduces the possibility of device shutdown during high-level transients.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE (2)
DRV2901	44-pin HTSSOP	14.0mm × 8.1mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins where applicable.



DRV2901 Functional Block Diagram

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4 Pin Configuration and Functions

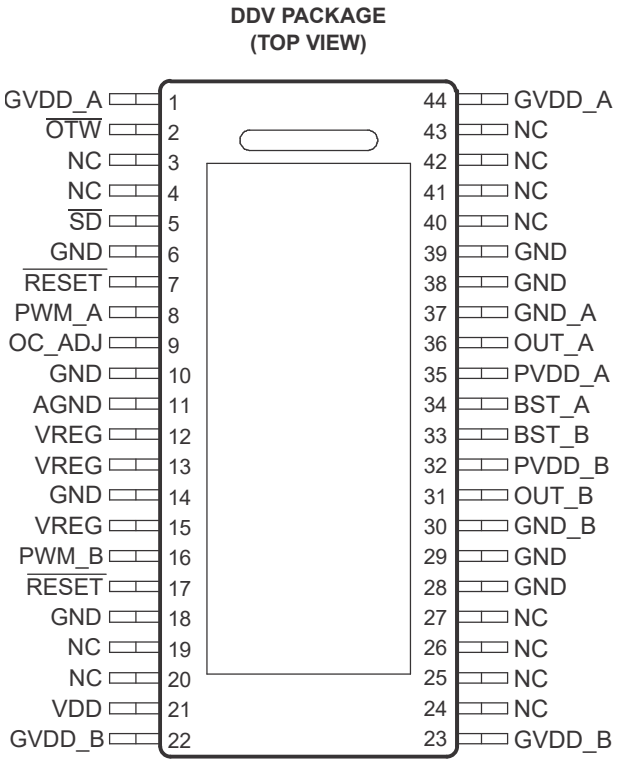


Figure 4-1. DDV Package 44-Pin HTSSOP PowerPad Top View

Table 4-1. Pin Functions

PIN		TYPE [1]	DESCRIPTION
NAME	NO.		
AGND	11	P	Analog ground
BST_A	34	P	HS bootstrap supply (BST), external 0.1µF capacitor to OUT_A required
BST_B	33	P	HS bootstrap supply (BST), external 0.1µF capacitor to OUT_B required
GND	6, 10, 14, 18, 28, 29, 38, 39	P	Ground.
GND_A	37	P	Power ground for half-bridge A
GND_B	30	P	Power ground for half-bridge B
GVDD_A	1, 44	P	Gate-drive voltage supply requires 0.1µF capacitor to AGND
GVDD_B	22, 23	P	Gate-drive voltage supply requires 0.1µF capacitor to AGND
NC	3, 4, 19, 20, 24, 25, 26, 27, 40, 41, 42, 43	—	Do not connect.
OC_ADJ	9	O	Analog overcurrent programming pin requires resistor to ground
$\overline{\text{OTW}}$	2	O	Overtemperature warning signal, open-drain, active-low
OUT_A	36	O	Output, half-bridge A
OUT_B	31	O	Output, half-bridge B
PVDD_A	35	P	Power supply input for half-bridge A requires close decoupling of 0.01µF capacitor in parallel with a 1.0µF capacitor to GND_A.
PVDD_B	32	P	Power supply input for half-bridge B requires close decoupling of 0.01µF capacitor in parallel with a 1.0µF capacitor to GND_B.
PWM_A	8	I	The input signal for half-bridge A

Table 4-1. Pin Functions (continued)

PIN		TYPE [1]	DESCRIPTION
NAME	NO.		
PWM_B	16	I	The input signal for half-bridge B
$\overline{\text{RESET}}$	7, 17	I	Reset signal for half-bridge A and B, active-low
$\overline{\text{SD}}$	5	O	Shutdown signal, open-drain, active-low
VDD	21	P	The power supply for the digital voltage regulator requires a 47µF capacitor in parallel with a 0.1µF capacitor to GND for decoupling.
VREG	12, 13, 15	P	The digital regulator supply filter pin requires 0.1µF capacitor to AGND.

(1) I = input, O = output, P = power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted (1)

VDD to AGND	–0.3 V to 13.2V
GVDD_X to AGND	–0.3 V to 13.2V
PVDD_X to GND_X (2)	–0.3 V to 71V
OUT_X to GND_X (2)	–0.3 V to 71V
BST_X to GND_X (2)	–0.3 V to 79.7V
VREG to AGND	–0.3 V to 4.2V
GND_X to GND	–0.3 V to 0.3V
GND_X to AGND	–0.3 V to 0.3V
GND to AGND	–0.3 V to 0.3V
PWM_X, OC_ADJ, M1, M2, M3 to AGND	–0.3 V to 4.2V
$\overline{\text{RESET\_X}}$, $\overline{\text{SD}}$, $\overline{\text{OTW}}$ to AGND	–0.3 V to 7V
Maximum continuous sink current ($\overline{\text{SD}}$, $\overline{\text{OTW}}$)	9mA
Maximum operating junction temperature range, T_J	0°C to 125°C
Storage temperature	–40°C to 125°C
Lead temperature, 1.6mm (1/16 inch) from case for 10 seconds	260°C
Minimum pulse duration, low	50ns

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) These voltages represent the dc voltage + peak ac waveform measured at the terminal of the device in all conditions.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
PVDD_X	Half-bridge supply	DC supply voltage	0	50	52.5	V
GVDD_X	Supply for logic regulators and gate-drive circuitry	DC supply voltage	10.8	12	13.2	V
VDD	Digital regulator input	DC supply voltage	10.8	12	13.2	V
L_{Output}	Output-filter inductance	Minimum output inductance under short-circuit condition	5	10		µH
F_{PWM}	PWM frequency		20		600	kHz
T_J	Junction temperature		0		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		DRV2901 DDV 44-PINS HTSSOP JEDEC STANDARD 4 LAYER PCB	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.7	°C/W

THERMAL METRIC(1)		DRV2901 DDV 44-PINS HTSSOP JEDEC STANDARD 4 LAYER PCB	UNIT
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.36	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.19	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics

R_L= 6Ω, F_{PWM} = 384kHz, unless otherwise noted. All performance is in accordance with recommended operating conditions unless otherwise specified.

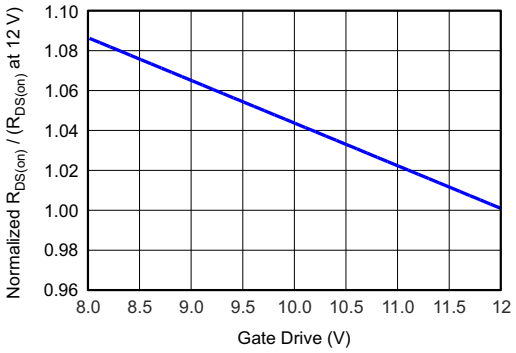
PARAMETER		TEST CONDITIONS	DRV2900 MIN	DRV2900 TYP	DRV2900 MAX	UNIT
Internal Voltage Regulator and Current Consumption						
VREG	Voltage regulator, only used as a reference node	VDD = 12V	2.95	3.3	3.65	V
IVDD	VDD supply current	Operating, 50% duty cycle		10		mA
		Idle, reset mode		6		
IGVDD_X	Gate supply current per half-bridge	50% duty cycle		8		mA
		Reset mode		0.3		
IPVDD_X	Half-bridge idle current	50% duty cycle, without output filter or load		15		mA
		Reset mode, no switching		500		µA
Output Stage MOSFETs						
$R_{DSon,LS}$	Drain-to-source resistance, LS	T_J = 25°C, includes metallization resistance, GVDD = 12V		90		mΩ
$R_{DSon,HS}$	Drain-to-source resistance, HS	T_J = 25°C, includes metallization resistance, GVDD = 12V		90		mΩ
I/O Protection						
$V_{uvp,G}$	Undervoltage protection limit, GVDD_X			8.5		V
$V_{uvp,hyst}$ (1)				400		mV
OTW(1)	Overtemperature warning		115	125	135	°C
OTW_{HYST} (1)	Temperature drop needed below OTW temp. for $\overline{OTW}$ to be inactive after the $\overline{OTW}$ event			25		°C
OTE(1)	Overtemperature error		145	155	165	°C
$OTE\text{-}OTW_{differential}$ (1)	OTE-OTW differential			25		°C
OTE_{HYST} (1)	A reset needs to occur for $\overline{SD}$ for be released following an OTE event.			25		°C
OLPC	Overload protection counter	F_{PWM} = 384kHz		1.3		ms
I_{OC}	Overcurrent limit protection	Resistor—programmable, nominal, R_{OCP} = 22 kΩ		12		A
I_{OCT}	Overcurrent response time	Time from application of short condition to Hi-Z of affected 1/2 bridge		250		ns
R_{OCP}	OC programming resistor range	Resistor tolerance = 5%	22		69	kΩ

R_L= 6Ω, F_{PWM} = 384kHz, unless otherwise noted. All performance is in accordance with recommended operating conditions unless otherwise specified.

PARAMETER		TEST CONDITIONS	DRV2900			UNIT
			MIN	TYP	MAX	
R_{PD}	Internal pulldown resistor at the output of each half-bridge	Connected when $\overline{\text{RESET}}$ is active to provide bootstrap capacitor charge. Not used in SE mode		1.0		kΩ
Static Digital Specifications						
V_{IH}	High-level input voltage	PWM_A, PWM_B, RESET_AB	2			V
V_{IL}	Low-level input voltage				0.8	V
Leakage	Input leakage current		-100		100	μA
OTW/SHUTDOWN (SD)						
R_{INT_PU}	Internal pullup resistance, $\overline{\text{OTW}}$ to VREG, $\overline{\text{SD}}$ to VREG		20	26	35	kΩ
V_{OH}	High-level output voltage	Internal pullup resistor	2.95	3.3	3.65	V
		External pullup of 4.7kΩ to 5V	4.5		5	
V_{OL}	Low-level output voltage	I_O = 4 mA		0.2	0.4	V
FANOUT	Device fanout $\overline{\text{OTW}}$, $\overline{\text{SD}}$	No external pullup		30		Devices

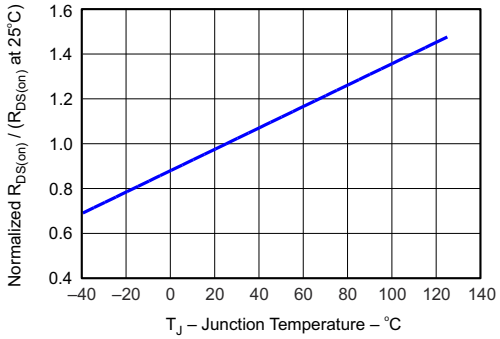
(1) Specified by design

5.6 Typical Characteristics



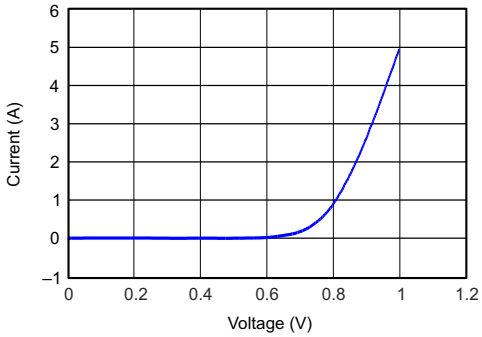
T_J = 25°C

Figure 5-1. Normalized $R_{DS(on)}$ vs Gate Drive



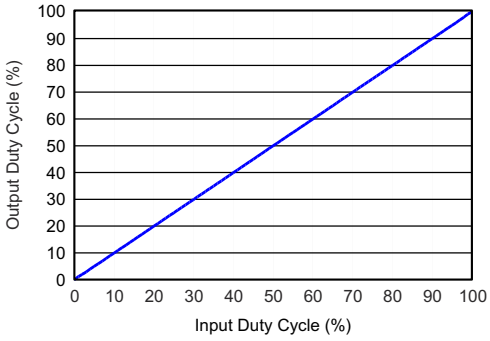
GVDD = 12 V

Figure 5-2. Normalized $R_{DS(on)}$ vs Junction Temperature



T_J = 25°C

Figure 5-3. Drain To Source Diode Forward On Characteristics



F_S = 500 kHz; T_C = 25°C

Figure 5-4. Output Duty Cycle vs Input Duty Cycle

6 Detailed Description

6.1 Block Diagrams

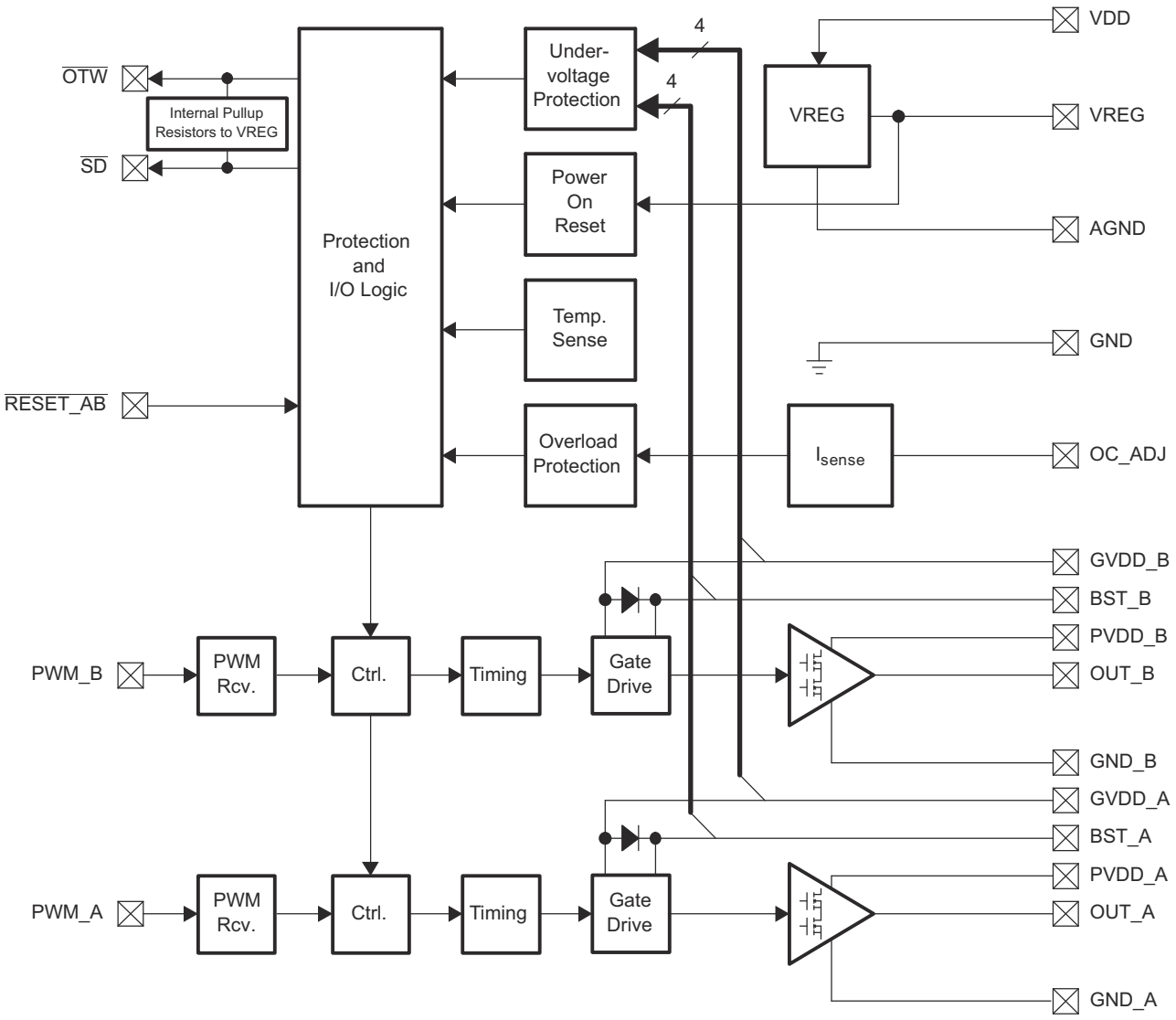


Figure 6-1. System Block Diagram

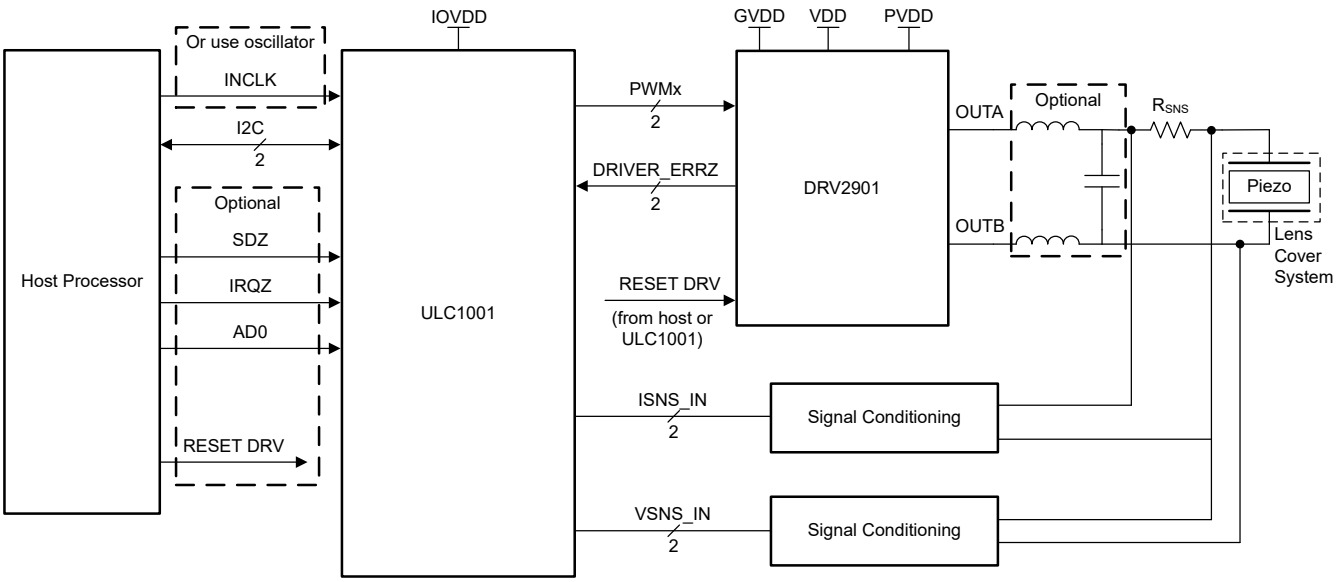


Figure 6-2. Functional Block Diagram

6.2 Feature Description

6.2.1 Error Reporting

The $\overline{SD}$ and $\overline{OTW}$ pins are both active-low, open-drain outputs. The pins purpose is protection-mode signaling to a PWM controller or other system-control device.

Any fault resulting in device shutdown, such as overtemperatue shut down, overcurrent shut-down, or undervoltage protection, is signaled by the $\overline{SD}$ pin going low. Likewise, $\overline{OTW}$ goes low when the device junction temperature exceeds 125°C (see Table 6-1).

Table 6-1. Protection Mode Signal Descriptions

$\overline{SD}$	$\overline{OTW}$	DESCRIPTION
0	0	Overtemperature warning and (overtemperature shut down or overcurrent shut down or undervoltage protection) occurred
0	1	Overcurrent shut-down or GVDD undervoltage protection occurred
1	0	Overtemperature warning
1	1	Device under normal operation

TI recommends monitoring the $\overline{OTW}$ signal using the system microcontroller and responding to an $\overline{OTW}$ signal by reducing the load current to prevent further heating of the device resulting in device overtemperature shutdown (OTSD).

To reduce external component count, an internal pullup resistor to internal VREG (3.3V) is provided on both $\overline{SD}$ and $\overline{OTW}$ outputs. Level compliance for 5V logic can be obtained by adding external pullup resistors to 5V (see the *Electrical Characteristics* section of this data sheet for further specifications).

6.2.2 Device Reset

Reset pin is provided for control of the H-bridge. When $\overline{RESET\_AB}$ is asserted low, the power-stage FETs in H-bridge are forced into a high-impedance (Hi-Z) state.

A rising-edge transition on reset input allows the device to resume operation after a shut-down fault and clears the fault and $\overline{SD}$ pin.

6.2.3 Device Protection System

6.2.3.1 Overcurrent (OC) Protection With Current Limiting and Overload Detection

The device has independent, fast-reacting current detectors with programmable trip threshold (OC threshold) on all high-side and low-side power-stage FETs. See the following table for OC-adjust resistor values. The detector outputs are closely monitored by two protection systems. The first protection system controls the power stage to prevent the output current from further increasing, for example, the first protection system performs a current-limiting function rather than prematurely shutting down during combinations of high-level transients and extreme load impedance drops. If the high-current situation persists, for example, the power stage is being overloaded, a second protection system triggers a latching shutdown, resulting in the power stage being set in the high-impedance (Hi-Z) state. Current limiting and overload protection are independent for half-bridges A and B

- For the lowest-cost bill of materials in terms of component selection, limit the OC threshold measure, considering the power output requirement and minimum load impedance. Higher-impedance loads require a lower OC threshold.
- The demodulation-filter inductor must retain at least 5µH of inductance at twice the OC threshold setting.

Unfortunately, most inductors have decreasing inductance with increasing temperature and increasing current (saturation). To some degree, an increase in temperature naturally occurs when operating at high output currents, due to core losses and the dc resistance of the copper winding in the inductor. A thorough analysis of inductor saturation and thermal properties is strongly recommended.

Setting the OC threshold too low can cause issues such as lack of enough output power and/or unexpected shutdowns due to too-sensitive overload detection.

For added flexibility, the OC threshold is programmable within a limited range using a single external resistor connected between the OC_ADJ pin and AGND. (See the *Electrical Characteristics* section of this data sheet for information on the correlation between programming-resistor value and the OC threshold.) Note that a properly functioning overcurrent detector assumes the presence of a properly designed demodulation filter at the power-stage output. Short-circuit protection is not provided directly at the output pins of the power stage but only on the transducer terminals (after the demodulation filter). Requirements dictate the need to follow certain guidelines when selecting the OC threshold and an appropriate demodulation inductor:

OC-Adjust Resistor Values (kΩ)	Max. Current Before OC Occurs (A)
22	12.2
27	10.5
47	6.4
68	4.0
100	3.0

6.2.3.2 Overtemperature Protection

The DRV2901 has a two-level temperature-protection system that asserts an active-low warning signal ($\overline{\text{OTW}}$) when the device junction temperature exceeds 125°C (nominal) and, if the device junction temperature exceeds 155°C (nominal), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and $\overline{\text{SD}}$ being asserted low. OTE is latched in this case and $\overline{\text{RESET\_AB}}$ must be asserted low.

6.2.3.3 Undervoltage Protection (UVP) and Power-On Reset (POR)

The UVP and POR circuits of the DRV2901 fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and maintains that all circuits are fully operational when the GVDD_X and VDD supply voltages reach 9.8V (typical). Although GVDD_X and VDD are independently monitored, a supply voltage drop below the UVP threshold on any VDD or GVDD_X pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and $\overline{\text{SD}}$ being

asserted low. The device automatically resumes operation when all supply voltage on the bootstrap capacitors has increased above the UVP threshold.

7 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The DRV2901 is a high-performance lens cleaner transducer driver. This device requires two power supplies, at 12V for GVDD and VDD, and 12V to 52V for PVDD. The DRV2901 does not require power-up sequencing due to an internal power-on reset.

The typical schematic is shown in Figure 7-1. The DRV2901 PWM inputs, fault outputs, and reset control are designed to be handled by the ULC1001 controller. A host processor controls ULC1001 and commands the device to drive specific PWM patterns into the DRV2901. Alternatively, the host can be used to control DRV2901 fault and reset pins.

The current and voltage feedback network, R1-R6, is described in the ULC1001 data sheet.

7.2 Typical Application

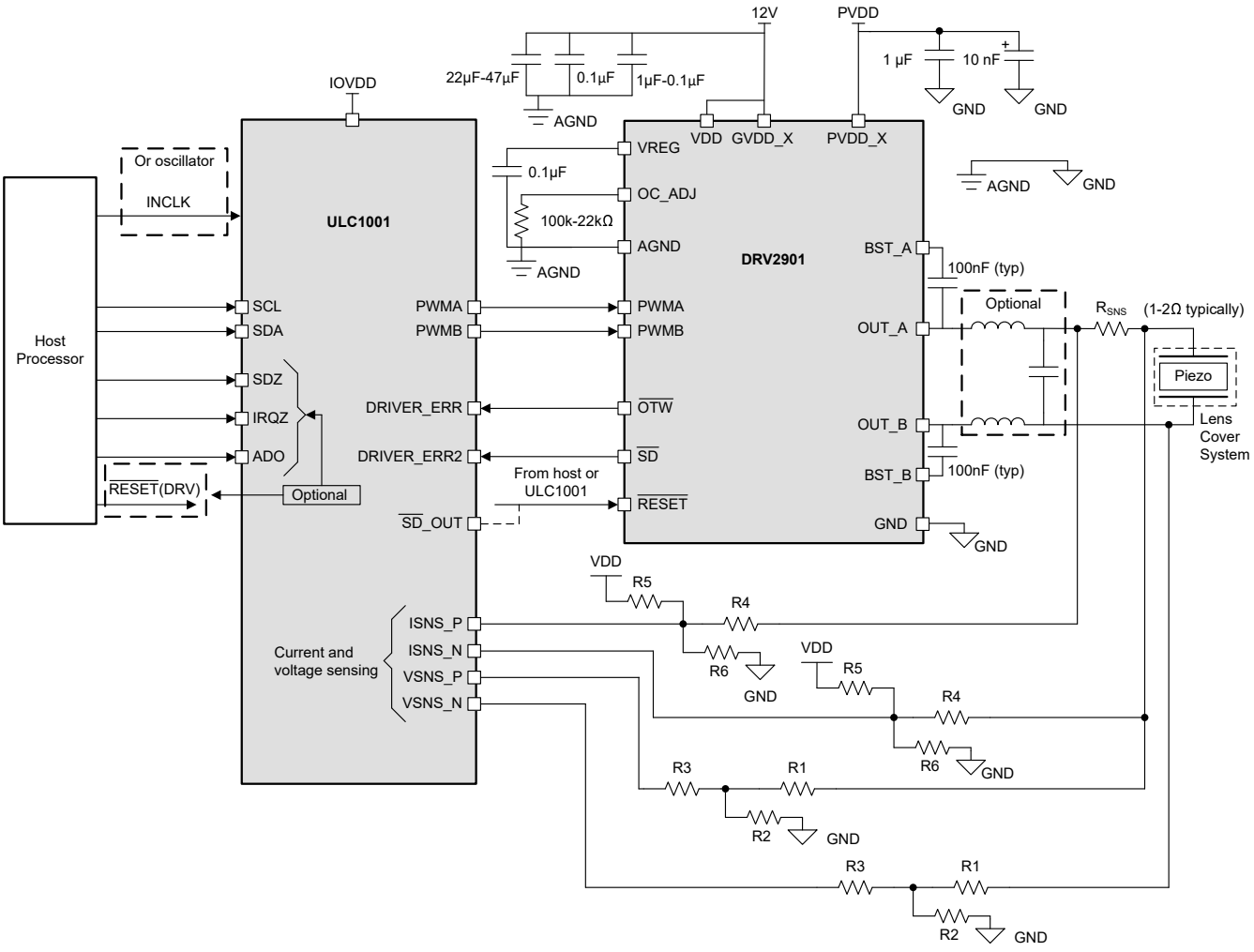


Figure 7-1. System Schematic

7.3 Power Supply Recommendations

7.3.1 System Power-up/power-down Sequence

7.3.1.1 Powering Up

The DRV2901 does not require a power-up sequence. The outputs of the H-bridges remain in a high impedance state until the gate-drive supply voltage (GVDD_X) and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, TI recommends to hold $\overline{\text{RESET\_AB}}$ in a low state while powering up the device. This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output.

7.3.1.2 Powering Down

The DRV2901 does not require a power-down sequence. The device remains fully operational as long as the gate-drive supply (GVDD_X) voltage and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, a good practice is to hold $\overline{\text{RESET\_AB}}$ low during power down, thus preventing any artifacts.

7.3.2 System Design Recommendations

7.3.2.1 VDD Pin

The transient current in the VDD pin can be significantly higher than the average current through the VDD pin. A low-resistive path to GVDD can be used. A 22µF to 47µF capacitor can be placed on the VDD pin beside the 100nF to 1µF decoupling capacitor to provide a constant voltage during the transient.

7.3.2.2 VREG Pin

The VREG pin is used for internal logic and should not be used as a voltage source for external circuitry. The capacitor on VREG pin should be connected to AGND.

7.3.2.3 OTW Pin

$\overline{\text{OTW}}$ reporting indicates the device approaching high junction temperature. This signal can be used with MCU to decrease system power when $\overline{\text{OTW}}$ is low to prevent OT shutdown at a higher temperature.

No external pull-up resistor or 3.3V power supply is needed for 3.3V logic. The $\overline{\text{OTW}}$ pin has an internal pull-up resistor connecting to an internal 3.3V to reduce external component count. For 5V logic, an external pull-up resistor to 5V is needed.

7.3.2.4 Bootstrap Capacitors

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_X) to the respective power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power supply pin (GVDD_X) and the bootstrap pin. When the power-stage output pin is high, the bootstrap capacitor provides additional voltage for the high-side gate driver. In higher frequency applications, above 300kHz, smaller 33nF bootstrap capacitors can be used. For lower frequency operation, larger bootstrap capacitors such as 100nF are recommended. The capacitor needs to be sized to maintain sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle.

7.4 Layout

Follow the EVM layout images below to achieve the best balance of design size and electrical performance for the DRV2901 device. The PVDD capacitors, C7, C6, C1 and C2, are placed on the power plane on the bottom side of the PCB to quickly supply charge to the PVDD pins. To insure stability for VDD, C21 is placed on the top of the PCB near pin 21 and C20 is directly below the device on the bottom of the PCB. The gate driver capacitors, C3 and C5, are placed on the bottom side of the PCB at each side of the device near the respective GVDD_X. These capacitor placements leave ample room for the bootstrap capacitors to be placed on the top of the PCB between the respective OUT_X and BST_X pins. For sizing the boost strap capacitors correctly, refer to Section 7.3.2.4.

To prevent any high-voltage noise on the sensitive low-voltage IV sense pins that travel to the ULC1001 device, a trench is cutout between the devices shown in the 2D layer plots.

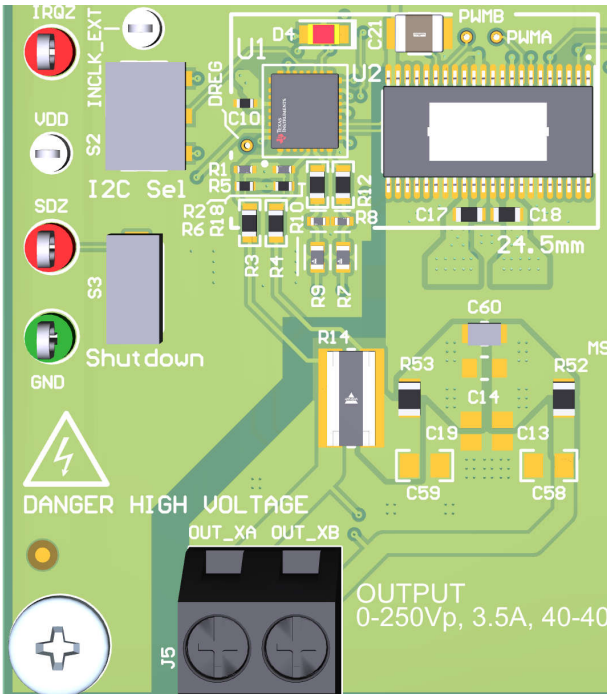


Figure 7-2. 3D Top View Layout

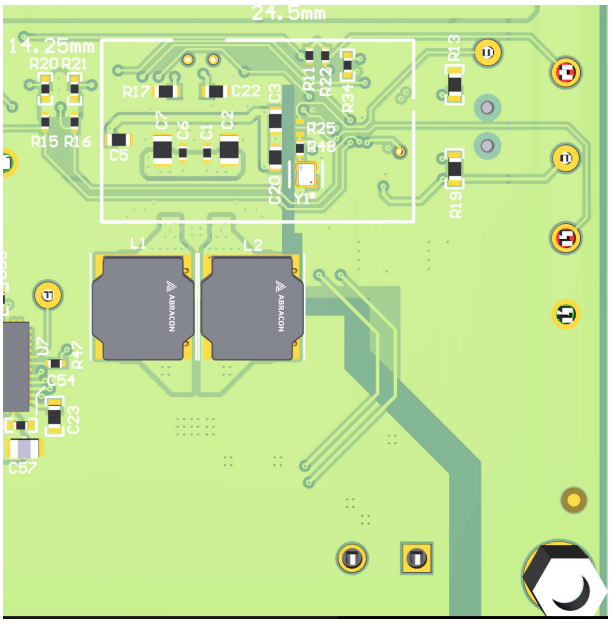


Figure 7-3. 3D Bottom View Layout

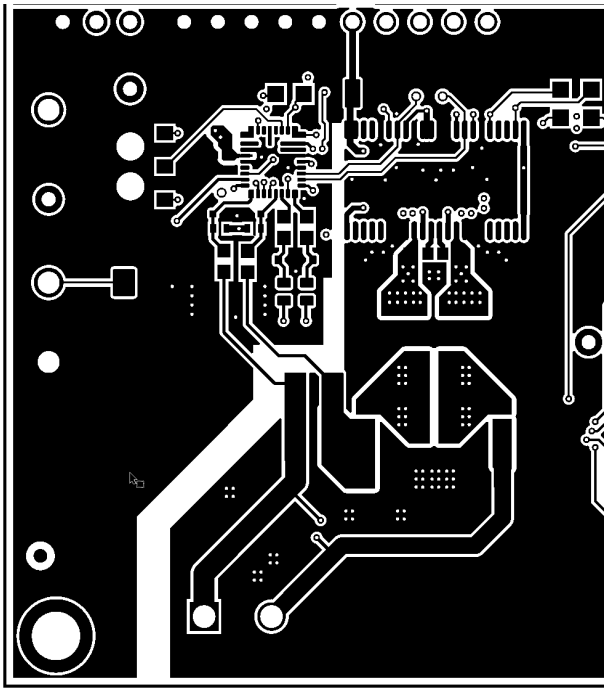


Figure 7-4. 2D Top Layer (Signal) Layout

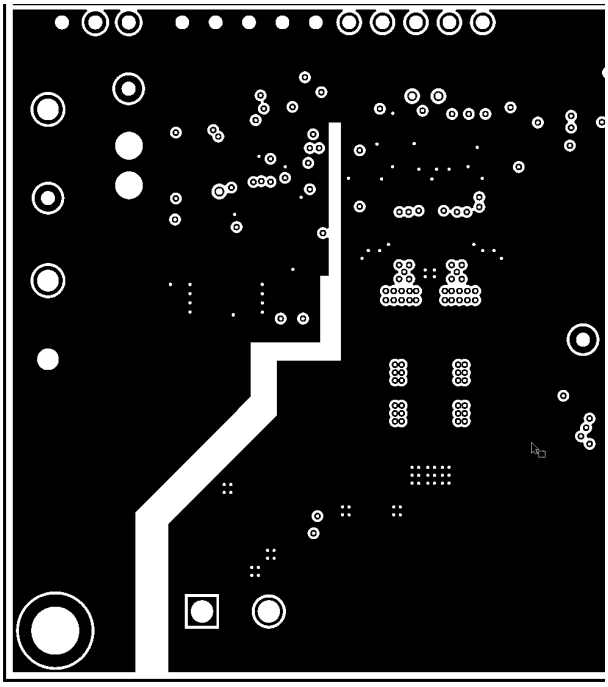


Figure 7-5. 2D Second Layer (GND) Layout

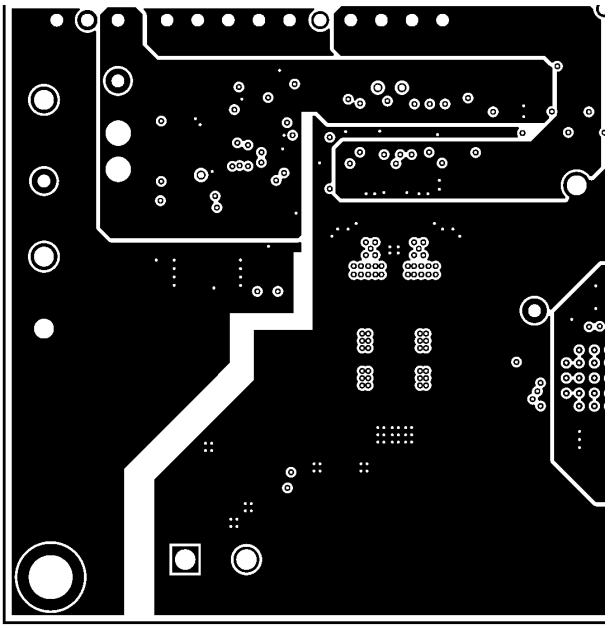


Figure 7-6. 2D Third Layer (PWR) Layout

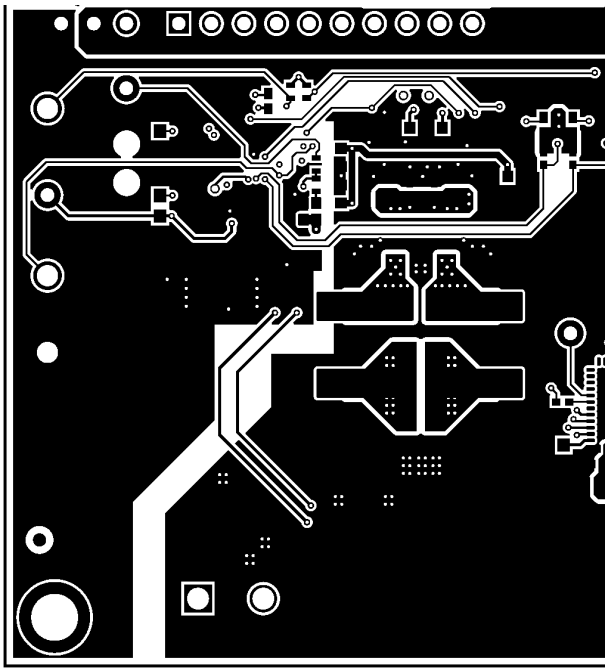


Figure 7-7. 2D Bottom Layer (Signal) Layout

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (January 2023) to Revision A (July 2025)	Page
• Updated functional block diagram	1
• Updated bootstrap capacitor recommendation	3
• Updated PWM frequency range	5
• Updated block diagram	9
• Clarifications on application circuit	13
• Updated system schematic	13
• Bootstrap section added	14
• Layout section added	14

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV2901DDVR	Active	Production	HTSSOP (DDV) | 44	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 125	DRV2901
DRV2901DDVR.A	Active	Production	HTSSOP (DDV) | 44	2000 | LARGE T&R	-	NIPDAU	Level-3-260C-168 HR	0 to 125	DRV2901

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

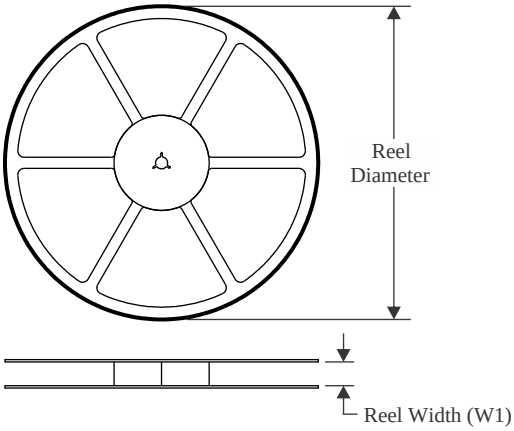
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

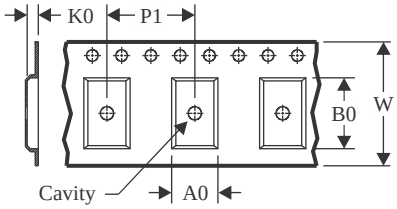
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

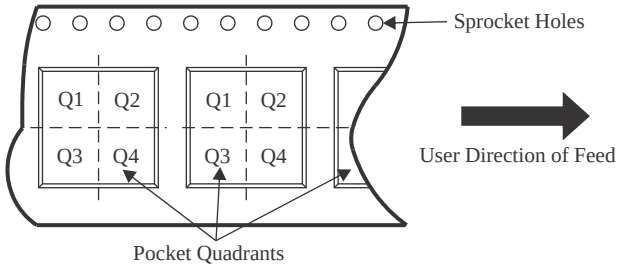


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

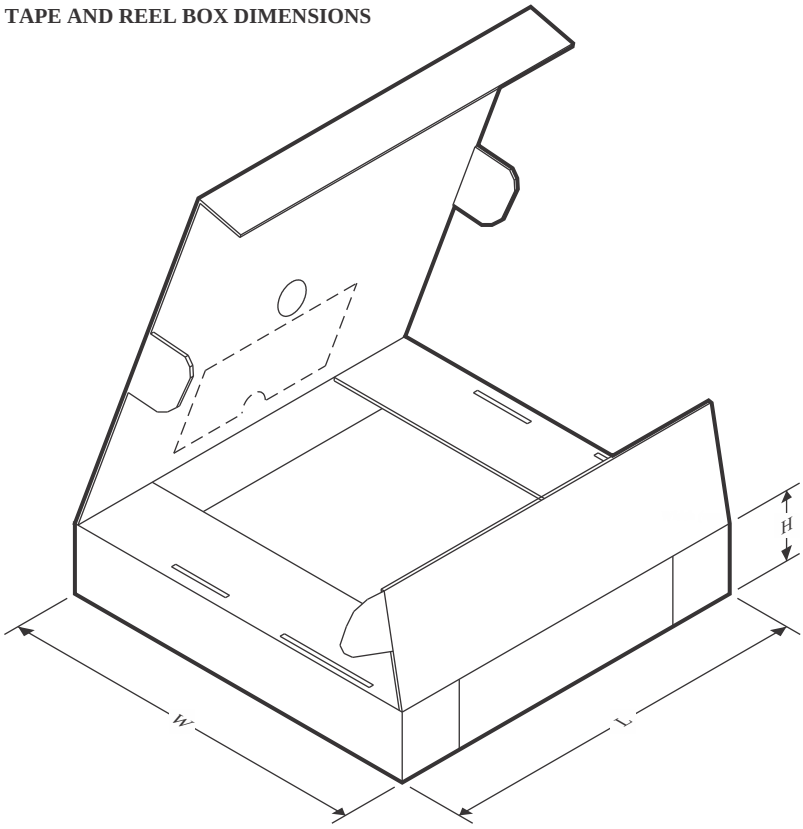
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV2901DDVR	HTSSOP	DDV	44	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

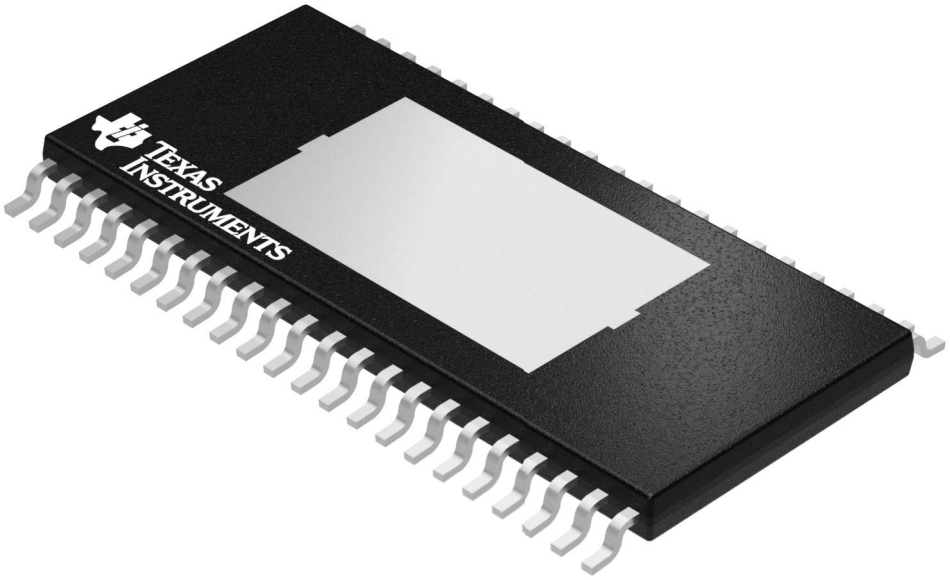


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV2901DDVR	HTSSOP	DDV	44	2000	350.0	350.0	43.0

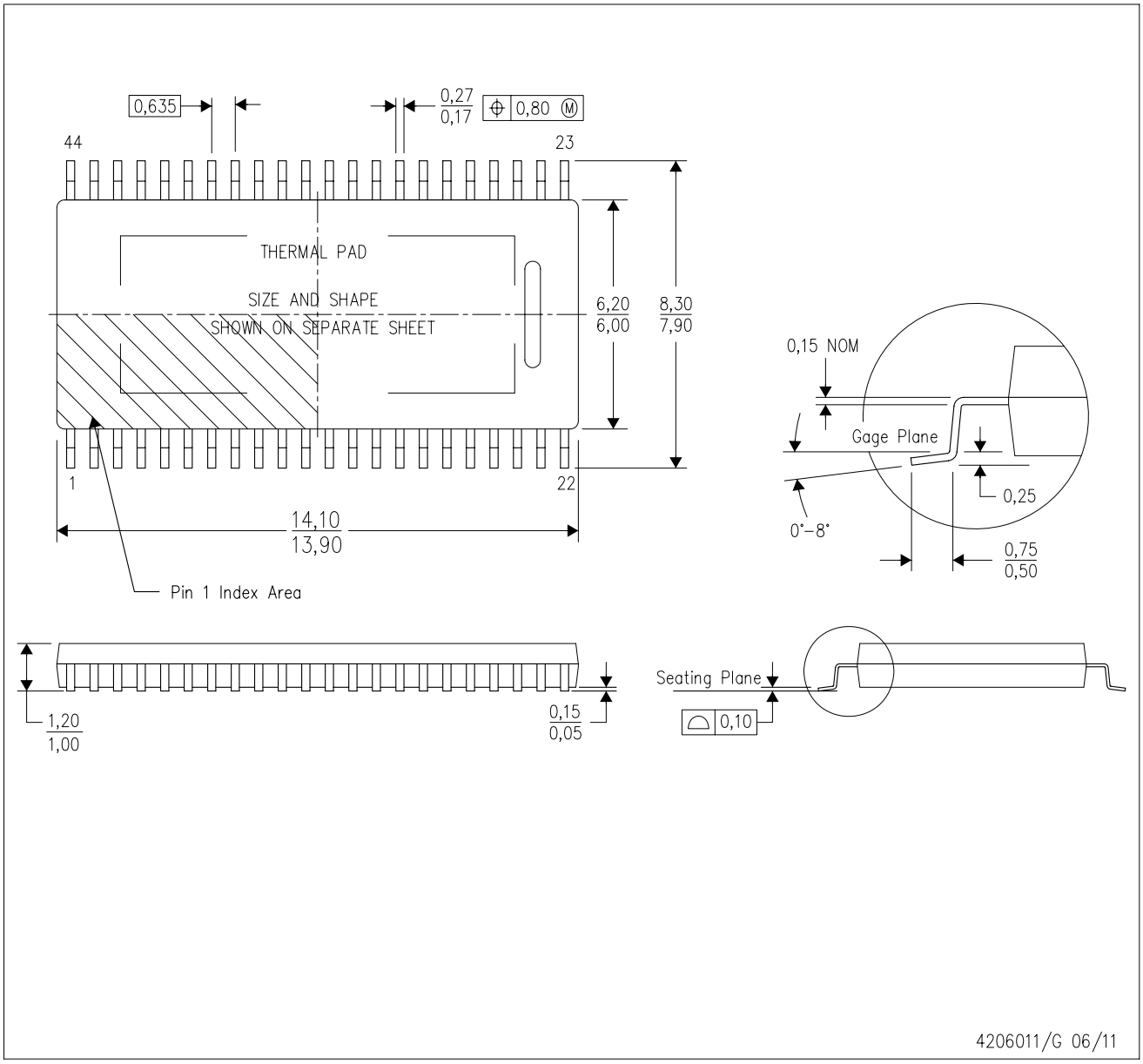
DDV 44 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDV (R–PDSO–G44) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be attached directly to an external heatsink. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.

PowerPAD is a trademark of Texas Instruments.

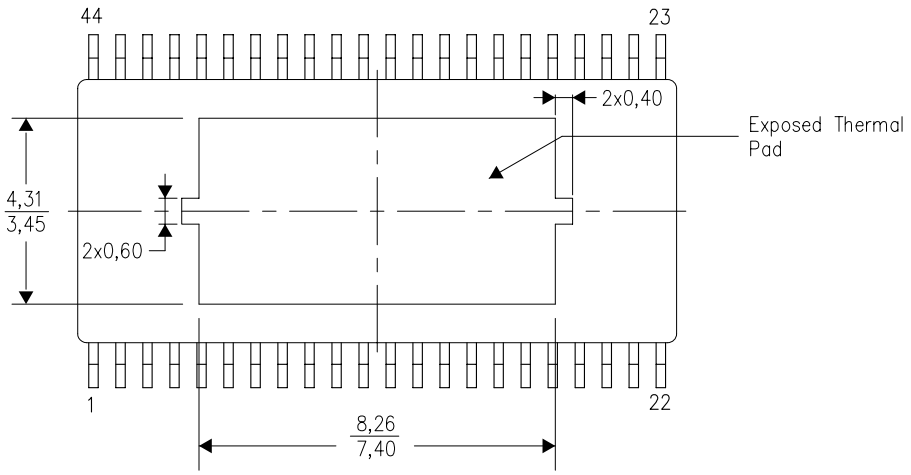
DDV (R–PDSO–G44) PowerPAD ™SMALL OUTLINE PACKAGE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206975–4/D 07/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

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