

# **DLPA3082 Power Management and High-Current Driver IC**

### 1 Features

- Generation of DMD high voltage supplies
- Two high-efficiency buck converters to generate the DLPC84xx and DMD supply
- One high-efficiency, 8-bit programmable buck converter for fan driver application or general power supply. General purpose buck2 (PWR6) is currently supported.
- Two LDOs supplying auxiliary voltages
- Analog MUX for measuring internal and external nodes such as a thermistor and reference levels
- Monitoring/protections: thermal shutdown, hot die, and undervoltage lockout (UVLO)

# 2 Applications

Portable DLP®Pico™ projectors

## 3 Description

DLPA3082 is а highly-integrated management IC optimized for DLP® Pico™ Projector systems. The DLPA3082 contains five converters, two of which are dedicated for DLPC low voltage supplies. Another dedicated regulating supply generates the three timing-critical DC supplies for the DMD: VBIAS, VRST, and VOFS.

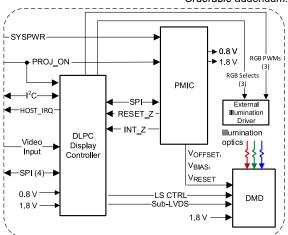
The DLPA3082 contains several auxiliary blocks which are used in a flexible way. This enables a tailor-made Pico Projector system. One 8-bit programmable buck converter isused, for instance, to make auxiliary supply line. General purpose buck2 (PWR6) is currently supported. Two LDOs are used for a lower-current supply, up to 200mA. These LDOs are predefined to 2.5V and 3.3V.

Through the SPI, all blocks of the DLPA3082 are addressed. Features included are the generation of the system reset, power sequencing, IC selfprotections, and an analog MUX for routing analog information to an external ADC.

#### **Device Information**

PART NUMBER	PACKAGE	PACKAGE SIZE
DLPA3082 <sup>(1)</sup>	HTQFP (100)	14.00mm × 14.00mm

For more information, see the Mechanical, Packaging, and Orderable addendum.



**Typical Simplified System** 



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## 4 Pin Configuration and Functions

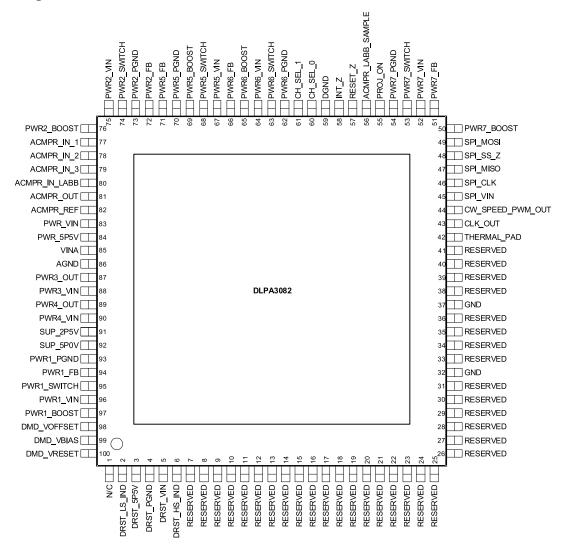


Figure 4-1. PFD Package 100-Pin HTQFP Top View

**Table 4-1. Pin Functions** 

PIN		I/O	DESCRIPTION	
NAME	NO.	1/0	DESCRIPTION	
N/C	1	_	No connect	
DRST_LS_IND	2	I/O	Connection for the DMD SMPS-inductor (low-side switch).	
DRST_5P5V	3	0	Filter pin for LDO DMD. Power supply for internal DMD reset regulator, typical 5.5V	
DRST_PGND	4	GND	ver ground for DMD SMPS. Connect to ground plane.	
DRST_VIN	5	POWER	ower supply input for LDO DMD. Connect to system power.	
DRST_HS_IND	6	I/O	onnection for the DMD SMPS-inductor (high-side switch).	
RESERVED	7	_	Connect a 10µF capacitor to ground.	
RESERVED	8	_	Connect a 1µF capacitor to ground.	
RESERVED	9	_	No connect	
RESERVED	10	_	No connect	
RESERVED	11	_	No connect	
RESERVED	12	_	No connect	



# **Table 4-1. Pin Functions (continued)**

PIN	PIN		able 4-1. Fill Functions (continueu)			
NAME	NO.	I/O	DESCRIPTION			
RESERVED	13	_	No connect			
RESERVED	14	_	No connect			
RESERVED	15	_	No connect			
RESERVED	16	_	No connect			
RESERVED	17	_	No connect			
RESERVED	18	_	No connect			
RESERVED	19	_	No connect			
RESERVED	20	_	No connect			
RESERVED	21	_	No connect			
RESERVED	22	_	No connect			
RESERVED	23	_	No connect			
RESERVED	24	_	No connect			
RESERVED	25	_	No connect			
RESERVED	26	_	No connect			
RESERVED	27	_	No connect			
RESERVED	28	_	No connect			
RESERVED	29	_	No connect			
RESERVED	30	_	No connect			
RESERVED	31	_	Connect a pull-down 1kΩ resistor to ground.			
GND	32	GND	Ground			
RESERVED	33	_	No connect			
RESERVED	34	_	No connect			
RESERVED	35	_	No connect			
RESERVED	36	_	Connect a pull-down 1kΩ resistor to ground.			
GND	37	GND	Ground			
RESERVED	38	_	No connect			
RESERVED	39	_	No connect			
RESERVED	40	_	No connect			
RESERVED	41	_	No connect			
THERMAL_PAD	42	GND	Thermal pad. Connect to a clean system ground.			
CLK_OUT	43	0	No connect. Reserved for color wheel clock output.			
CW_SPEED_PWM_OUT	44	0	No connect. Reserved for color wheel PWM output.			
SPI_VIN	45	I	Supply for SPI interface			
SPI_CLK	46	I	SPI clock input			
SPI_MISO	47	0	SPI data output			
SPI_SS_Z	48	I	SPI chip select (active low)			
SPI_MOSI	49	I	SPI data input			
PWR7_BOOST	50	I	No connect. Reserved for general purpose buck converter. Charge-pump-supply input for the high-side FET gate drive circuit. Connect a 100nF capacitor between PWR7_BOOST and PWR7_SWITCH pins.			
PWR7_FB	51	I	No connect. Reserved for general purpose buck converter. Converter feedback input. Connect to converter output voltage.			
PWR7_VIN	52	POWER	No connect. Reserved for general purpose buck converter. Power supply input for converter			
PWR7_SWITCH	53	I/O	No connect. Reserved for general purpose buck converter. Switch node connection between high-side NFET and low-side NFET			



# **Table 4-1. Pin Functions (continued)**

PIN			Table 4-1. Pin Functions (continued)			
NAME	NO.	I/O	DESCRIPTION			
PWR7_PGND	54	GND	No connect. Reserved for general purpose buck converter. Ground pin. Power ground return for switching circuit			
PROJ_ON	55	I	Input signal to enable and or disable the IC and DLP projector			
ACMPR_LABB_SAMPLE	56	I	Control signal to sample voltage at ACMPR_IN_LABB. Needs to connect a pull-down $10k\Omega$ resistor to ground when the pin is not used.			
RESET_Z	57	0	Reset output to the DLP system (active low). The pin is held low to reset DLP system.			
INT_Z	58	0	Interrupt output signal (open drain, active low). Connect to the pullup resistor.			
DGND	59	GND	Digital ground. Connect to ground plane.			
CH_SEL_0	60	I	Control signal to enable either of CH1,2,3. Needs to connect a pull-down $10k\Omega$ resistor to ground when the pin is not used.			
CH_SEL_1	61	I	Control signal to enable either of CH1,2,3. Needs to connect a pull-down $10k\Omega$ resistor to ground when the pin is not used.			
PWR6_PGND	62	GND	Ground pin. Power ground return for switching circuit			
PWR6_SWITCH	63	I/O	Switch node connection between high-side NFET and low-side NFET			
PWR6_VIN	64	POWER	ver supply input for converter			
PWR6_BOOST	65	I	arge-pump-supply input for the high-side FET gate drive circuit. Connect a 100nF acitor between PWR6_BOOST and PWR6_SWITCH pins.			
PWR6_FB	66	I	Converter feedback input. Connect to output voltage.			
PWR5_VIN	67	POWER	No connect. Reserved for general purpose buck converter. Power supply input for converter			
PWR5_SWITCH	68	I/O	No connect. Reserved for general purpose buck converter. Switch node connection betwee high-side NFET and low-side NFET			
PWR5_BOOST	69	I	No connect. Reserved for general purpose buck converter. Charge-pump-supply input for the high-side FET gate drive circuit. Connect 100nF capacitor between PWR5_BOOST and PWR5_SWITCH pins.			
PWR5_PGND	70	GND	No connect. Reserved for general purpose buck converter. Ground pin. Power ground return for switching circuit			
PWR5_FB	71	I	No connect. Reserved for general purpose buck converter. Converter feedback input. Connect to output voltage.			
PWR2_FB	72	I	Converter feedback input. Connect to output voltage.			
PWR2_PGND	73	GND	Ground pin. Power ground return for switching circuit			
PWR2_SWITCH	74	I/O	Switch node connection between high-side NFET and low-side NFET			
PWR2_VIN	75	POWER	Power supply input for converter			
PWR2_BOOST	76	I	Charge-pump-supply input for the high-side FET gate drive circuit. Connect a 100nF capacitor between PWR2_BOOST and PWR2_SWITCH pins.			
ACMPR_IN_1	77	I	Reserved. Input for analog sensor signal. No connect when the pin is not used.			
ACMPR_IN_2	78	I	Input for analog sensor signal. No connect when the pin is not used.			
ACMPR_IN_3	79	ı	Input for analog sensor signal. No connect when the pin is not used.			
ACMPR_IN_LABB	80	ı	Input for ambient light sensor, sampled input. No connect when the pin is not used.			
ACMPR_OUT	81	0	Analog comparator out. No connect when the pin is not used.			
ACMPR_REF	82	I	Reference voltage input for analog comparator. No connect when the pin is not used.			
PWR_VIN	83	POWER	Power supply input for LDO_Bucks. Connect to system power.			
PWR_5P5V	84	0	Filter pin for LDO_BUCKS. Internal analog supply for buck converters, typical 5.5V			
VINA	85	POWER	Input voltage supply pin for reference system			
AGND	86	GND	Analog ground pin			
PWR3_OUT	87	0	Filter pin for LDO_2 DMD/DLPC/AUX, typical 2.5V			
PWR3_VIN	88	POWER	Power supply input for LDO_2. Connect to system power.			
PWR4_OUT	89	0	Filter pin for LDO_1 DMD/DLPC/AUX, typical 3.3V			
PWR4_VIN	90	POWER	Power supply input for LDO_1. Connect to system power.			



# **Table 4-1. Pin Functions (continued)**

PIN		I/O	DESCRIPTION	
NAME	NO.	1/0	DESCRIPTION	
SUP_2P5V	91	0	Filter pin for LDO_V2V5. Internal supply voltage, typical 2.5V	
SUP_5P0V	92	0	er pin for LDO_V5V. Internal supply voltage, typical 5V	
PWR1_PGND	93	GND	ound pin. Power ground return for switching circuit	
PWR1_FB	94	I	onverter feedback input. Connect to output voltage.	
PWR1_SWITCH	95	I/O	vitch node connection between high-side NFET and low-side NFET	
PWR1_VIN	96	POWER	Power supply input for converter	
PWR1_BOOST	97	I	Charge-pump-supply input for the high-side FET gate drive circuit. Connect a 100nF capacitor between PWR1_BOOST and PWR1_SWITCH pins.	
DMD_VOFFSET	98	0	OFS output rail. Connect to ceramic capacitor.	
DMD_VBIAS	99	0	VBIAS output rail. Connect to ceramic capacitor.	
DMD_VRESET	100	0	VRESET output rail. Connect to ceramic capacitor.	



# **5 Specifications**

## 5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)

		MIN	MAX	UNIT
	PWR_VIN, PWR1,2,3,4,6_VIN, VINA, DRST_VIN	-0.3	22	
	PWR1,2,6_BOOST	-0.3	28	
	PWR1,2,6_BOOST (10ns transient)	-0.3	30	
	PWR1,2,6_SWITCH	-2	22	
	PWR1,2,6_SWITCH (10ns transient)	-3	27	
	PWR1,2,6_FB	-0.3	6.5	
	PWR1,2,6_BOOST vs PWR1,2,6_SWITCH	-0.3	6.5	
	DRST_LS_IND	-0.3	20	
	INT_Z, PROJ_ON	-0.3	7	
Voltage	DRST_HS_IND	-18	7	V
	ACMPR_IN_1,2,3, ACMPR_REF, ACMPR_IN_LABB, ACMPR_LABB_SAMPLE, ACMPR_OUT	-0.3	3.6	
	SPI_VIN, SPI_CLK, SPI_MOSI, SPI_SS_Z, SPI_MISO, CH_SEL_0,1, RESET_Z	-0.3	3.6	
	DGND, AGND, DRST_PGND, GND, PWR1,2,6_PGND	-0.3	0.3	
	DRST_5P5V, PWR_5P5, PWR3,4_OUT, SUP_5P0V	-0.3	7	
	SUP_2P5V	-0.3	3.6	
	DMD_VOFFSET	-0.3	12	
	DMD_VBIAS	-0.3	20	
	DMD_VRESET	-18	7	
2	RESET_Z, ACMPR_OUT		1	^
Source current	SPI_DOUT		5.5	mA
Sinds assument	RESET_Z, ACMPR_OUT		1	^
Sink current	SPI_DOUT, INT_Z		5.5	- mA
$\Gamma_{ m stg}$	Storage temperature	-65	150	°C

<sup>(1)</sup> Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

## 5.2 ESD Ratings

			VALUE	UNIT
V (1)	Electrostatic	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(2)</sup>	±2000	V
V <sub>(ESD)</sub> (1)	discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(3)</sup>	±500	v

<sup>(1)</sup> Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.

<sup>(2)</sup> JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

<sup>(3)</sup> JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.



## **5.3 Recommended Operating Conditions**

over operating free-air temperature range (unless otherwise noted)

	· · · · · · · · · · · · · · · · · · ·	MIN	MAX	UNIT
	PWR_VIN, PWR1,2,3,4,6_VIN, VINA, DRST_VIN	6	20	
	PROJ_ON	-0.1	6	
	PWR1,2,6_FB	-0.1	5	
Input voltage range	ACMPR_REF, CH_SEL_0,1, SPI_CLK, SPI_MOSI, SPI_SS_Z	-0.1	3.6	V
	RLIM_BOT_K_1,2	-0.1	0.1	
	ACMPR_IN_1,2,3, LABB_IN_LABB	-0.1	1.5	
	SPI_VIN	1.7	3.6	
Ambient temperature ra	ange	0	70	°C
Operating junction tem	perature	0	120	°C

#### 5.4 Thermal Information

		DLPA3082	
	THERMAL METRIC <sup>(1)</sup>	PFD (HTQFP)	UNIT
		100 PINS	
R <sub>0JA</sub>	Junction-to-ambient thermal resistance (2)	7.0	°C/W
R <sub>0</sub> JC(top)	Junction-to-case (top) thermal resistance (3)	0.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	N/A	°C/W
ΨЈТ	Junction-to-top characterization parameter (4)	0.6	°C/W
ΨЈВ	Junction-to-board characterization parameter (5)	3.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, but since the device is intended to be cooled with a heatsink from the top case of the package, the simulation includes a fan and heatsink attached to the DLPA3082. The heatsink is a 22mm × 22mm × 12mm aluminum pin fin heatsink with a 12 × 12 × 3mm stud. The base thickness is 2mm and the pin diameter is 1.5mm with an array of 6 × 6 pins. The heatsink is attached to the DLPA3082 with 100µm thick thermal grease with 3W/m-K thermal conductivity. The fan is 20 × 20 × 8mm with a 1.6cfm open volume flow rate and 0.22-inch water pressure at stagnation.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description is found in the ANSI SEMI standard G30-88.
- (4) The junction-to-top characterization parameter, ψ<sub>JT</sub>, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining R<sub>θJA</sub>, using a procedure described in JESD51-2a (sections 6 and 7), but modified to include the fan and heatsink described in Note 2.
- (5) The junction-to-board characterization parameter, ψ<sub>JB</sub>, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining R<sub>θJA</sub>, using a procedure described in JESD51-2a (sections 6 and 7), but modified to include the fan and heatsink described in Note 2.



### 5.5 Electrical Characteristics

Over operating free-air temperature range.  $V_{IN}$  = 12V,  $T_A$  = 0 to +70°C, typical values are at  $T_A$  = 25°C, Configuration according to Section 7.2 ( $V_{IN}$  =12V) (unless otherwise noted).

according to	Section 7.2 (V <sub>IN</sub> =12V) (unles	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	FAINAMETER	SUPPLIES	IVIIIV		IVIAA	ONIT
INPUT VOLT	AGE	SUFFLIES				
V <sub>IN</sub>	Input voltage range	VINA – pin	6(6)	12	20	V
VIN	input voitage range	VINA – pill VINA falling (through a 5-bit trim function, 0.5V	0(-7	12	20	V
V <sub>UVLO</sub> (7)	UVLO threshold	steps)	3.9	6.22	18.4	V
	Hysteresis	VINA rising		90		mV
V <sub>STARTUP</sub>	Startup voltage	DMD_VBIAS, DMD_VOFFSET, DMD_VRESET loaded with 10mA	6			V
INPUT CURR	RENT					
I <sub>IDLE</sub>	Idle current	IDLE mode, all VIN pins combined		15		μΑ
I <sub>STD</sub>	Standby current	STANDBY mode, analog, internal supplies and LDOs enabled, DMD and BUCK CONVERTERS disabled.		3.7		mA
I <sub>Q_DMD</sub>	Quiescent current (DMD)	Quiescent current DMD block (in addition to I <sub>STD</sub> ), VINA + DRST_VIN		0.49		mA
I <sub>Q_ВИСК</sub>		Quiescent current per BUCK converter (in addition to I <sub>STD</sub> ), Normal mode, VINA + PWR_VIN + PWR1,2,6_VIN, PWR1,2,6_VOUT = 1V		4.3		
	Quiescent current (per BUCK)	Quiescent current per BUCK converter (in addition to I <sub>STD</sub> ), Normal mode, VINA + PWR_VIN + PWR1,2,6_VIN, PWR1,2,6_VOUT = 5V		15		mA
		Quiescent current per BUCK converter (in addition to I <sub>STD</sub> ), Cycle-skipping mode, VINA + PWR_VIN + PWR1,2,6_VIN = 1V		0.41		
		Quiescent current per BUCK converter (in addition to I <sub>STD</sub> ), Cycle-skipping mode, VINA + PWR_VIN + PWR1,2,6_VIN = 5V		0.46		
I <sub>Q_TOTAL</sub>	Quiescent current (Total)	Typical Application: ACTIVE mode, all VIN pins combined, DMD, and PWR1,2 enabled, PWR3,4,6 disabled.		38		mA
INTERNAL S	UPPLIES				'	
V <sub>SUP_5P5V</sub>	Internal supply, analog			5		V
V <sub>SUP_2P5V</sub>	Internal supply, logic			2.5		V
		DMD — LDO DMD				
V <sub>DRST_VIN</sub>			6	12	20	V
V <sub>DRST_5P5V</sub>				5.5		V
DCOOD	Dower good DDCT EDEV	Rising		80%		
PGOOD	Power good DRST_5P5V	Falling		60%		
OVP	Overvoltage protection DRST_5P5V			7.2		V
	Regulator dropout	At 25mA, VDRST_VIN= 5.5V		56		mV
	Regulator current limit <sup>(2)</sup>		300	340	400	mA
		DMD — REGULATOR				
5	MODELLON	Switch A (from DRST_5P5V to DRST_HS_IND)		920		
R <sub>DS(ON)</sub>	MOSFET ON-resistance	Switch B (from DRST_LS_IND to DRST_PGND)		450		mΩ



Over operating free-air temperature range.  $V_{IN}$  = 12V,  $T_A$  = 0 to +70°C, typical values are at  $T_A$  = 25°C, Configuration according to Section 7.2 ( $V_{IN}$  =12V) (unless otherwise noted).

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{FW}$	Forward voltage drop	Switch C (from DRST_LS_IND to DRST_VBIAS <sup>(1)</sup> ), VDRST_LS_IND = 2V, I <sub>F</sub> = 100mA		1.21		V
V FW	r orward voltage drop	Switch D (from DRST_LS_IND to DRST_VOFFSET <sup>(1)</sup> ), VDRST_LS_IND = 2V, I <sub>F</sub> = 100mA		1.22		<b>,</b>
t <sub>DIS</sub>	Rail Discharge time	C <sub>OUT</sub> = 1µF			40	μs
$t_{PG}$	Power-good timeout	Not tested in production		15		ms
I <sub>LIMIT</sub>	Switch current limit			610		mA
VOFFSET R	EGULATOR					
V <sub>OFFSET</sub>	Output voltage			10		V
	DC output voltage accuracy	I <sub>OUT</sub> = 10mA	-0.3		0.3	V
	DC Load regulation	I <sub>OUT</sub> = 0mA to 10mA		-10		V/A
	DC Line regulation	I <sub>OUT</sub> = 10mA, DRST_VIN = 8V to 20V		-5		mV/V
V <sub>RIPPLE</sub>	Output ripple	I <sub>OUT</sub> = 10mA, C <sub>OUT</sub> = 1μF		200		mVpp
I <sub>OUT</sub>	Output current		0.1		10	mA
	Power-good threshold	VOFFSET rising		86%		
PGOOD	(fraction of nominal output voltage)	VOFFSET falling		66%		
С	Output capacitor	Recommended value <sup>(5)</sup> (use same value as output capacitor on VRESET)	1			μF
		t <sub>DISCHARGE</sub> <40μs at VIN = 8V			1	
VBIAS REGI	JLATOR					
V <sub>BIAS</sub>	Output voltage			18		V
	DC output voltage accuracy	I <sub>OUT</sub> = 10mA	-0.3		0.3	V
	DC Load regulation	I <sub>OUT</sub> = 0 to 10mA		-18		V/A
	DC Line regulation	I <sub>OUT</sub> = 10mA, DRST_VIN = 8V to 20V		-3		mV/V
V <sub>RIPPLE</sub>	Output ripple	I <sub>OUT</sub> = 10mA, C <sub>OUT</sub> = 470nF		200		mVpp
I <sub>OUT</sub>	Output current		0.1		10	mA
	Power-good threshold	VBIAS rising		86%		
PGOOD	(fraction of nominal output voltage)	VBIAS falling		66%		
С	Output capacitor	Recommended value <sup>(5)</sup> (use same or smaller value as output capacitors VOFFSET / VRESET)	470			nF
		t <sub>DISCHARGE</sub> <40µs at VIN = 8V			470	
VRESET RE	GULATOR					
V <sub>RST</sub>	Output voltage			-14		V
	DC output voltage accuracy	I <sub>OUT</sub> = 10mA	-0.3		0.3	V
	DC Load regulation	I <sub>OUT</sub> = 0 to 10mA		-4		V/A
	DC Line regulation	I <sub>OUT</sub> = 10mA, DRST_VIN = 8 to 20V		-2		mV/V
V <sub>RIPPLE</sub>	Output ripple	I <sub>OUT</sub> = 10mA, C <sub>OUT</sub> = 1μF		120		mVpp
I <sub>OUT</sub>	Output current	22	0.1		10	mA
	Power-good threshold		<u> </u>	90%		
PGOOD	rower-good uneshold					
PGOOD C	Output capacitor	Recommended value <sup>(5)</sup> (use same value as output capacitor on VOFFSET)	1			μF

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Over operating free-air temperature range.  $V_{IN}$  = 12V,  $T_A$  = 0 to +70°C, typical values are at  $T_A$  = 25°C, Configuration according to *Section 7.2* ( $V_{IN}$  =12V) (unless otherwise noted).

according to c	Section 7.2 (V <sub>IN</sub> =12V) (unless PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	I / U VIIIIE I EIX	DMD — BUCK CONVERTERS	.,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,		шда	0.411
OUTPUT VOLT	<u>Γ</u> ΔGF	DIND — BOOK CONVENTERS				
V <sub>PWR_1_VOUT</sub>	Output Voltage			0.8		V
	Output Voltage			1.8		
V <sub>PWR_2_VOUT</sub>	DC output voltage accuracy	I <sub>OUT</sub> = 0mA	-3%	1.0	3%	v
MOSFET		1001 - 01114			3 70	
R <sub>ON,H</sub>	High side switch resistance	25°C, V <sub>PWR_1,2_Boost</sub> - V <sub>PWR1,2_SWITCH</sub> = 5.5V		150		mΩ
R <sub>ON,L</sub>	Low side switch resistance <sup>(2)</sup>	25°C		85		mΩ
LOAD CURRE		20 0				11122
20/13 0011112	Allowed Load Current <sup>(3)</sup>				3	Α
I <sub>OCL</sub>	Current limit <sup>(2)</sup>	L <sub>OUT</sub> = 3.3μH	3.2	3.6	4.2	
ON-TIME TIME		2001 0.0μπ	0.2	0.0	7.2	
	On time	V <sub>IN</sub> = 12V, V <sub>O</sub> = 5V		120		ns
tossame	Minimum off time <sup>(2)</sup>	T <sub>A</sub> = 25°C, V <sub>FB</sub> = 0V		270		ns
t <sub>OFF(MIN)</sub> START-UP		. A 20 0, v <sub>FB</sub> - 0 v		210		113
START-OF	Soft start		1	2.5	4	ms
PGOOD			<u>'</u>	2.5	4	1115
	Overvoltage protection			120%		
Ratio <sub>OV</sub>	Relative power good level	Low to high		72%		
Ratio <sub>PG</sub>	Relative power good level			1270		
	Input voltage range	BUCK CONVERTERS — LDO_BUCKS				
V <sub>PWR_VIN</sub>	Input voltage range PWR1,2,6_VIN		6	12	20	V
V <sub>PWR_5P5V</sub>	PWR_5P5V			5.5		V
PGOOD	Power good PWR_5P5V	Rising		80%		
1 0002		Falling		60%		
OVP	Overvoltage Protection PWR_5P5V			7.2		٧
	Regulator dropout	At 25mA, V <sub>PWR_VIN</sub> = 5.5V		41		mV
	Regulator current limit <sup>(2)</sup>		300	340	400	mA
	BUCK CONVI	ERTER — GENERAL PURPOSE BUCK CONVER	RTER (8)			
OUTPUT VOLT	ΓAGE					
V <sub>PWR6_VOUT</sub>	Output Voltage (General Purpose Buck2)	8-bit programmable	1		5	V
	DC output voltage accuracy	I <sub>OUT</sub> = 0mA	-3.5%		3.5%	
MOSFET						
R <sub>ON,H</sub>	High side switch resistance	25°C, V <sub>PWR6_Boost</sub> – V <sub>PWR6_SWITCH</sub> = 5.5V		150		mΩ
R <sub>ON,L</sub>	Low side switch resistance <sup>(2)</sup>	25°C		85		mΩ
LOAD CURRENT						
	Allowed Load Current PWR6 <sup>(3)</sup> .			2		Α
I <sub>OCL</sub>	Current limit <sup>(2)</sup> (3)	L <sub>OUT</sub> = 3.3µH	3.2	3.6	4.2	Α
ON-TIME TIMER CONTROL						



Over operating free-air temperature range.  $V_{IN}$  = 12V,  $T_A$  = 0 to +70°C, typical values are at  $T_A$  = 25°C, Configuration according to Section 7.2 ( $V_{IN}$  =12V) (unless otherwise noted).

toff(MIN) Mir START-UP  Sof PGOOD  Ratioov Ove Ratiopg Ref  VpWR3,4_VIN Inp PGOOD Por  OVP  OVP  DC PW  Ref  ton Tur  LDO2 (PWR3)  VpWR3_VOUT Ou  LO2  DC PW  DC PW  DC PW  ARE  DC PW  DC PW  DC PW  ARE  CO PW  Ref  ARE  CO PW  ARE  CO	n time inimum off time <sup>(2)</sup> oft start  vervoltage protection elative power good level	$V_{IN} = 12V, V_O = 5V$ $T_A = 25^{\circ}C, V_{FB} = 0V$		120 270	310	ns
START-UP  Sof  PGOOD  RatioOV  RatioPG  Rel  VPWR3,4_VIN  INP  PGOOD  OVP  OVP  DC  PW  Reg  ton  LDO2 (PWR3)  VPWR3_VOUT  COP  LDO1 (PWR4)  VPWR4_VOUT  COP  COP  COP  COP  COP  COP  COP  CO	oft start vervoltage protection	T <sub>A</sub> = 25°C, V <sub>FB</sub> = 0V		270	310	
Sof PGOOD  Ratio <sub>OV</sub> Over Ratio <sub>PG</sub> Rel  V <sub>PWR3,4_VIN</sub> Inp PGOOD Por  OVP  OVP  DC PW  Rea  ton Tur  LOO2 (PWR3)  V <sub>PWR3_VOUT</sub> Our  Loa  DC PW  A  B  C  C  C  C  C  C  C  C  C  C  C  C	vervoltage protection				0.10	ns
PGOOD  Ratio <sub>OV</sub> Over Ratio <sub>PG</sub> Rel  V <sub>PWR3,4_VIN</sub> Inp PGOOD Por  OVP Over PW  Res  ton Tur  LDO2 (PWR3)  V <sub>PWR3_VOUT</sub> Our  Loa  DC PW  DC PW  DC PW  DC PW  ARE  DC PW  DC PW  DC PW  ARE  CO PW  Res  CO PW  Res	vervoltage protection					
Ratioov Over Relations Rel			1	2.5	4	ms
Ratiopg Rel  VPWR3,4_VIN Inp PGOOD Pot  OVP OVP  DC PW  Res  ton Tur  LDO2 (PWR3)  VPWR3_VOUT Ou  LO2  DC PW  DC PW  DC PW  DC PW  DC PW  DC PW  ARE  CO PW  ARE  CO PW  Res  CO PW  Res						
V <sub>PWR3,4_VIN</sub> Inp PGOOD Poi  OVP Ov. PW  DC PW  Rei ton Tur LDO2 (PWR3)  V <sub>PWR3_VOUT</sub> Ou  Loa DC PW  LDO1 (PWR4)  V <sub>PWR4_VOUT</sub> Ou  Loa DC PW  AREI AREI AREI AREI AREI AREI AREI ARE	elative power good level			120%		
PGOOD POO  OVP OVP PW  DC PW  ton Tur  LDO2 (PWR3)  VPWR3_VOUT Ou  DC PW  DC PW  LDO1 (PWR4)  VPWR4_VOUT Ou  Loa  DC PW  Rea  LABB		Low to high		72%		
PGOOD POO  OVP OVP PW  Reston Tur  LDO2 (PWR3)  VPWR3_VOUT Ou  DC PW  LDO1 (PWR4)  VPWR4_VOUT Ou  Loa  DC PW  ARE  CO PW		AUXILIARY LDOs				
PGOOD Por  PGOOD Por  OVP  OVP  PW  Reg  ton Tur  Loa  DC  PW  DC  PW  Loa  DC  PW  DC  PW  DC  PW  DC  PW  CO  DC  PW  CO  CO  CO  CO  CO  CO  CO  CO  CO  C	put voltage range	LDO1 (PWR4), LDO2 (PWR3)	3.3	12	20	V
DC PWR3_VOUT Our Loa DC PW LDO1 (PWR4_VOUT Our Loa DC PW LDO4 (PWR4_VOUT OUR LDO4 (PWR	ower good PWR3,4 VOUT	PWR3,4_VOUT rising		80%		
DC PWR3_VOUT Our Loa DC PW LDO1 (PWR4_VOUT Our Loa DC PW LDO4 (PWR4_VOUT DC PW LD04 (PWR4_VOUT DC PW		PWR3,4_VOUT falling		60%		
PW Rei ton Tur LDO2 (PWR3)  V_PWR3_VOUT Coa DC PW DC PW LDO1 (PWR4)  V_PWR4_VOUT Coa DC PW Coa DC PW Loa	vervoltage Protection WR3,4_VOUT			7		V
ton Tur LDO2 (PWR3)  VPWR3_VOUT Our Loa DC PW  DC PW  LDO1 (PWR4)  VPWR4_VOUT Our Loa DC PW  ARea  LABB	C output voltage accuracy WR3,4_VOUT	I <sub>OUT</sub> = 0mA	-3%		3%	
LDO2 (PWR3)  V <sub>PWR3_VOUT</sub> Loa  DC PW  DC PW  LDO1 (PWR4)  V <sub>PWR4_VOUT</sub> DC PW  COC PW  LOA  LOA  LOA  LOA  LOA  LOA  LOA  LO	egulator current limit <sup>(2)</sup>		300	340	400	mA
V <sub>PWR3_VOUT</sub> Our Loa DC PW DC PW LDO1 (PWR4) V <sub>PWR4_VOUT</sub> Our Loa DC PW DC PW Rea LABB	urn-on time	to 80% of V <sub>OUT</sub> = PWR3 and PWR4, C= 1µF		40		μs
Loa DC PW DC PW LDO1 (PWR4)  VPWR4_VOUT COA DC PW DC PW Rea LABB						
Loa DC PW DC PW LDO1 (PWR4)  V <sub>PWR4_VOUT</sub> Ou Loa DC PW DC PW Rea	utput Voltage PWR3_VOUT			2.5		V
PW DC PW LDO1 (PWR4)  V_PWR4_VOUT Loa DC PW DC PW Rea	pad Current capability			200		mA
PW LDO1 (PWR4)  V <sub>PWR4_VOUT</sub> Ou Loa DC PW DC PW Rea	C Load regulation WR3_VOUT	V <sub>OUT</sub> = 2.5V, I <sub>OUT</sub> = 5 to 200mA		-70		mV/A
V <sub>PWR4_VOUT</sub> Ou  Loa  DC  PW  DC  PW  Rea	C Line regulation WR3_VOUT	V <sub>OUT</sub> = 2.5V, I <sub>OUT</sub> = 5mA, PWR3_VIN = 3.3 to 20V		30		μV/V
Loa DC PW DC PW Res						
Loa DC PW DC PW Rea	utput Voltage PWR4_VOUT			3.3		V
PW DC PW Res	oad Current capability			200		mA
PW Res	C Load regulation WR4_VOUT	V <sub>OUT</sub> = 3.3V, I <sub>OUT</sub> = 5 to 200mA		-70		mV/A
LABB	C Line regulation WR4_VOUT	V <sub>OUT</sub> = 3.3V, I <sub>OUT</sub> = 5mA, PWR4_VIN= 4 to 20V		30		μV/V
	egulator dropout	At 25mA, V <sub>OUT</sub> = 3.3V, V <sub>PWR4 VIN</sub> = 3.3V		48		mV
		MEASUREMENT SYSTEM				
T <sub>RC</sub> Set						
T <sub>RC</sub> Set		To 1% of final value <sup>(2)</sup> .		4.6	6.6	
	ettling time	To 0.1% of final value <sup>(2)</sup>	<del>.</del>	7	10	μs
	put voltage range CMPR_IN_LABB		0		1.5	V
	ampling window CMPR_IN_LABB	Programmable per 7μs	7		28	μs
	DIGITAL CONTE	ROL — LOGIC LEVELS AND TIMING CHARACT	ERISTICS			
V <sub>SPI_VIN</sub> SP	DIGITAL CONTI	SPI_VIN	1.7		3.6	V

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Over operating free-air temperature range.  $V_{IN}$  = 12V,  $T_A$  = 0 to +70°C, typical values are at  $T_A$  = 25°C, Configuration according to *Section 7.2* ( $V_{IN}$  =12V) (unless otherwise noted).

	PARAMETER	TEST CONDITIONS	MIN	TYP MAX	UNIT
		RESET_Z, ACMPR_OUT, CLK_OUT. I <sub>O</sub> = 0.3mA sink current	0	0.3	
V <sub>OL</sub>	Output low-level	SPI_DOUT. I <sub>O</sub> = 5mA sink current	0	0.3 × V <sub>SPI_VIN</sub>	٧
		INT_Z. I <sub>O</sub> = 1.5mA sink current	0	$0.3 \times V_{SPI\_VIN}$	
V	Output high-level	RESET_Z, ACMPR_OUT, CLK_OUT. I <sub>O</sub> = 0.3mA source current	1.3	2.5	V
V <sub>OH</sub> Output h	Output High-level	SPI_DOUT. I <sub>O</sub> = 5mA source current	0.7 × V <sub>SPI_VIN</sub>	V <sub>SPI_VIN</sub>	V
		PROJ_ON, CH_SEL0, CH_SEL1	0	0.4	
$V_{IL}$	Input low-level	SPI_CSZ, SPI_CLK, SPI_DIN	0	0.3 × V <sub>SPI_VIN</sub>	V
V <sub>IH</sub> In		PROJ_ON, CH_SEL0, CH_SEL1	1.2		
	Input high-level	SPI_CSZ, SPI_CLK, SPI_DIN	0.7 × V <sub>SPI_VIN</sub>	V <sub>SPI_VIN</sub>	V
I <sub>BIAS</sub>	Input bias current	V <sub>IO</sub> = 3.3V, any digital input pin		0.1	μA
	SPI clock frequency <sup>(4)</sup>	Normal SPI mode, DIG_SPI_FAST_SEL = 0, $f_{OSC}$ = 9MHz	0	36	MHz
SPI_CLK		Fast SPI mode, DIG_SPI_FAST_SEL = 1, V <sub>SPI_VIN</sub> > 2.3V, f <sub>OSC</sub> = 9MHz	20	40	IVII IZ
t <sub>DEGLITCH</sub>	Deglitch time	CH_SEL0, CH_SEL1 <sup>(2)</sup> .		300	ns
		INTERNAL OSCILLATOR			
fosc	Oscillator frequency			9	MHz
	Frequency accuracy	T <sub>A</sub> = 0 to 70°C	-5%	5%	
		THERMAL SHUTDOWN			
T <sub>WARN</sub>	Thermal warning (HOT threshold)			120	°C
	Hysteresis			10	
T <sub>SHTDWN</sub>	Thermal shutdown (TSD threshold)			150	°C
- GITLDWIN	Hysteresis			15	

- (1) Including rectifying diode
- (2) Not production tested
- (3) Take care to not exceed the max power dissipation. Refer to *Thermal Considerations*.
- (4) Maximum depends linearly on oscillator frequency fosc.
- (5) Take care that the capacitor has the specified capacitance at the related voltage, that is V<sub>OFFSET</sub>, V<sub>BIAS</sub>, or V<sub>RESET</sub>.
- (6) VIN must be higher than the UVLO voltage setting, including after accounting for AC noise on VIN, for the DLPA3082 to fully operate. While 6.0V is the minimum VIN voltage supported, TI recommends that the UVLO is never set below 6.21V for a fault fast power down. 6.21V gives a margin above 6.0V to protect against the case where someone suddenly removes the VIN's power supply which causes the VIN voltage to drop rapidly. Failure to keep VIN above 6.0V before the mirrors are parked and VOFS, VRST, and VBIAS supplies are properly shut down results in permanent damage to the DMD. Since 6.21V is .21V above 6.0V, when UVLO trips there is time for the DLPA3082 and DLPC84xx to park the DMD mirrors and do a fast shutdown of supplies VOFS, VRST, and VBIAS. For whatever UVLO setting is used, if VIN's power supply is suddenly removed enough bulk capacitance can be included on VIN inside the projector to keep VIN above 6.0V for at least 100µs after UVLO trips.
- (7) UVLO cannot be used for normal power down operation, it is meant as a protection from power loss.
- (8) General purpose buck2 (PWR6) is currently supported.



# **5.6 SPI Timing Parameters**

SPI\_VIN = 3.6V  $\pm$  5%, T<sub>A</sub> = 0 to 70°C, C<sub>L</sub> = 10pF (unless otherwise noted).

		MIN	NOM MA	X UNIT
f <sub>CLK</sub>	Serial clock frequency	0	4	0 MHz
t <sub>CLKL</sub>	Pulse width low, SPI_CLK, 50% level	10		ns
t <sub>CLKH</sub>	Pulse width high, SPI_CLK, 50% level	10		ns
t <sub>t</sub>	Transition time, 20% to 80% level, all signals	0.2		4 ns
t <sub>CSCR</sub>	SPI_SS_Z falling to SPI_CLK rising, 50% level	8		ns
t <sub>CFCS</sub>	SPI_CLK falling to SPI_CSZ rising, 50% level			1 ns
t <sub>CDS</sub>	SPI_MOSI data setup time, 50% level	7		ns
t <sub>CDH</sub>	SPI_MOSI data hold time, 50% level	6		ns
t <sub>iS</sub>	SPI_MISO data setup time, 50% level	10		ns
t <sub>iH</sub>	SPI_MISO data hold time, 50% level	0		ns
t <sub>CFDO</sub>	SPI_CLK falling to SPI_MISO data valid, 50% level		13	ns
t <sub>CSZ</sub>	SPI_CSZ rising to SPI_MISO HiZ		6	ns



## **6 Detailed Description**

### 6.1 Overview

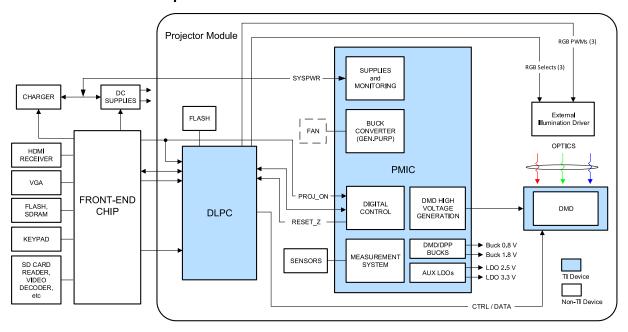
The DLPA3082 is a highly integrated power management IC optimized for DLP Pico Projector systems. The device targets accessory applications up to several hundreds of lumen. Section 6.2 shows a typical DLP Pico Projector implementation using the DLPA3082.

Part of the projector is the projector module, which is an optimized combination of components consisting of, for instance, DLPA3082, DMD, DLPC chip, memory, and optional sensors and fan. The frontend chip controls the projector module. More information about the system and projector module configuration can be found in a separate application note.

Within the DLPA3082, several blocks are distinguished. The blocks are listed below and subsequently discussed in detail:

- Supply and monitoring: Creates internal supply and reference voltages and has function such as thermal protection
- DMD: Generates voltages and specific timing for the DMD. Contains regulators and DMD/DLPC buck converters
- · Buck converter: General purpose buck converter
- Auxilairy LDOs: Fixed voltage LDOs for customer usage
- · Measurement system: Analog frontend to measure internal and external signals
- · Digital control: SPI, digital control

## **6.2 Functional Block Description**





### 6.3 Feature Description

### 6.3.1 Supply and Monitoring

This block takes care of creating several internal supply voltages and monitors correct behavior of the device.

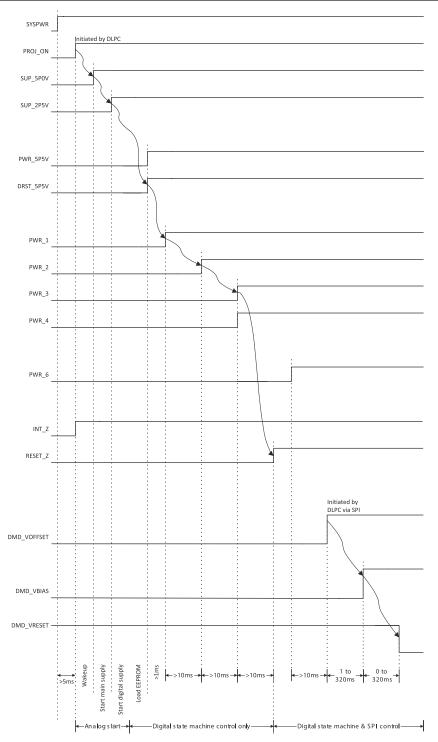
#### 6.3.1.1 Supply

SYSPWR is the main supply of the DLPA3082. It ranges from 6V to 20V, where the typical is 12V. At power-up, several (internal) power supplies are started one after the other to make the system work correctly (Figure 6-1). A sequential startup ensures that all the different blocks start in a certain order and prevent excessive startup currents. The main control to start the DLPA3082 is the control pin  $PROJ_ON$ . Once set high the *basic* analog circuitry is started that is needed to operate the digital and SPI interface. This circuitry is supplied by two LDO regulators that generate 2.5V (SUP\_2P5V) and 5V (SUP\_5P0V). These regulator voltages are for internal use only and cannot be loaded by an external application. The output capacitors of those LDOs can be  $2.2\mu F$  for the 2.5V LDO, and  $4.7\mu F$  for the 5V LDO, pin 91 and 92, respectively. Once these are up the digital core is started, and the DLPA3082 Digital State Machine (DSM) takes over.

Subsequently, the 5.5V LDOs for various blocks are started: PWR\_5P5V and DRST\_5P5V. Next, the buck converters and DMD LDOs are started (PWR\_1 to PWR\_4). The DLPA30085 is now awake and ready to be controlled by the DLPC (indicated by RESET\_Z going high).

The general purpose buck converter (PWR\_6) can be started (if used) as well as the regulator that supplies the DMD. The DMD regulator generates the timing critical VOFFSET, VBIAS, and VRESET supplies.





- Arrows indicate the sequence of events automatically controlled by the digital state machine. Other events are initiated under SPI control.
- SUP\_5P0V and SUP\_2P5V rise to a precharge level with SYSPWR, and reach the full level potential after PROJ\_ON is pulled 2. high.

Figure 6-1. Powerup Timing



#### 6.3.1.2 Monitoring

Several possible faults are monitored by the DLPA3082. If a fault occurred and the type of the fault is read in the Main Status register (0x0C). Subsequently, an interrupt could be generated if a fault occurs. The fault conditions that generate an interrupt could be configured in the Interrupt Mask register (0x0D).

#### 6.3.1.2.1 Block Faults

Fault conditions for several supplies can be observed such as the low voltage supplies SUPPLY\_FAULT (0x0C, bit 7). DMD\_FAULT (0x0C, bit 4) monitors the correct function of the DMD block. The PROJ\_ON\_INT (0x0C, bit 5) indicates if PROJ\_ON was asserted.

#### 6.3.1.2.2 Thermal Protection

The chip temperature is monitored constantly to prevent overheating of the device. There are two levels of a fault condition. The first is TS\_WARN (0x0C, bit 0) to warn of overheating. This is an indication that the chip temperature rises to a critical temperature. The next level of warning is TS\_SHUT (0x0C, bit 1). This occurs at a higher temperature than TS\_WARN (0x0C, bit 0) and shuts down the chip to prevent permanent damage. Both temperature faults have hysteresis on each level to prevent rapid switching around the temperature threshold.

### 6.3.2 DMD Supplies

This block contains all the supplies needed for the DMD and DLPC (Figure 6-2). The block comprises:

- LDO DMD: for internal supply
- DMD\_HV: regulator generates high voltage supplies
- Two buck converters: for DLPC/DMD voltages

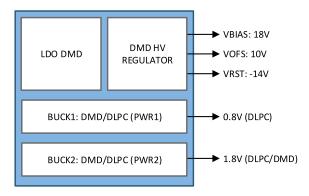


Figure 6-2. DMD Supplies Blocks

The DMD supplies block is designed to work with the DMD and the related DLPC. The DMD has a DMD-specific set of supply voltage requirements. Besides the three high voltages, two supplies are needed for the DMD and the related DLPC (DLPC84xx-family for instance). These supplies are made by two buck converters.

#### 6.3.2.1 LDO DMD

This regulator is dedicated to the DMD supplies block and provides an analog supply voltage of 5.5V to the internal circuitry. Use a  $1\mu F$  capacitor in parallel with a  $10\mu F$  capacitor on the input and a  $10\mu F$  capacitor on the output of the LDO. Make the voltage rating of the capacitor equal to or greater than two times the applied voltage across the capacitor in the application.

## 6.3.2.2 DMD HV Regulator

The DMD HV regulator generates three high-voltage supplies: DMD\_VRESET, DMD\_VBIAS, and DMD\_VOFFSET (Figure 6-3). The DMD HV regulator uses a switching regulator (switch A-D), where the inductor is time-shared between all three supplies. The inductor is charged up to a certain current value (current limit) and then discharged into one of the three supplies. If not all supplies need charging, the time available is equally shared between those that do need charging. The recommended value for the capacitors is  $1\mu F$  for  $V_{RST}$  and  $V_{OFS}$ , and 470nF for  $V_{BIAS}$ . The inductor value is  $10\mu H$ .



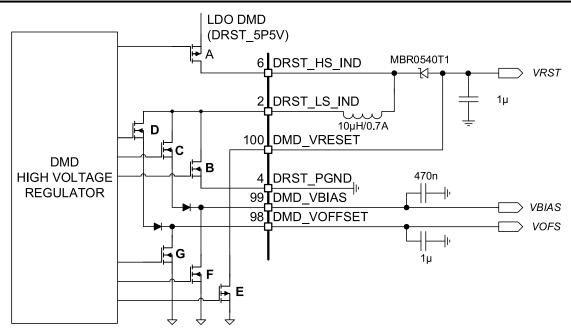


Figure 6-3. DMD High Voltage Regulator

#### 6.3.2.3 DMD/DLPC Buck Converters

Each of the two DMD buck converters creates a supply voltage for the DMD and DLPC. The values of the voltages for the DMD and DLPC used, for instance:

DMD+DLPC84xx: 0.8V (DLPC) and 1.8V (DLPC/DMD)

The topology of the buck converters is the same as the general-purpose buck converter discussed later in this document. How to configure the inductor and capacitor is discussed in Section 6.3.3.

A typical configuration is 3.3µH for the inductor and 2× 22µF for the output capacitor.



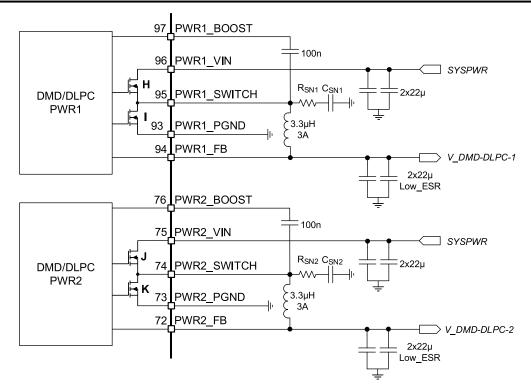


Figure 6-4. DMD/DLPC Buck Converters

### 6.3.2.4 DMD Monitoring

DOMED 000D

The DMD block is continuously monitored for failures to prevent damage to the DLPA3082 and the DMD. Several possible failures are monitored such that the DMD voltages can be ensured. Failures can be, for instance, a broken control loop or a too high or too low converter output voltage. The overall DMD fault bit is in Main Status register (0x0C), DMD\_FAULT. If any of the failures in Table 6-1 occur, the DMD\_FAULT bit is set high.

**Table 6-1. DMD FAULT Indication** 

POWER GOOD					
BLOCK	REGISTER BIT	THRESHOLD			
HV Regulator	DMD_PG_FAULT	DMD_VRESET: 90%, DMD_VOFFSET and DMD_VBIAS: 86% rising, 66% falling			
PWR1	BUCK_DMD1_PG_FAULT	Ratio: 72%			
PWR2	BUCK_DMD2_PG_FAULT	Ratio: 72%			
PWR3 (LDO_2)	LDO_GP2_PG_FAULT / LDO_DMD1_PG_ FAULT	80% rising, 60% falling			
PWR4 (LDO_1)	LDO_GP1_PG_FAULT / LDO_DMD1_PG_ FAULT	80% rising, 60% falling			
OVERVOLTAGE					
BLOCK	REGISTER BIT	THRESHOLD (V)			
PWR1	BUCK_DMD1_OV_FAULT	Ratio: 120%			
PWR2	BUCK_DMD2_OV_FAULT	Ratio: 120%			
PWR3 (LDO_2)	LDO_GP2_OV_FAULT / LDO_DMD1_OV_FAULT	7			
PWR4 (LDO_1)	LDO_GP1_OV_FAULT / LDO_DMD1_OV_FAULT	7			

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#### 6.3.2.4.1 Power Good

The DMD HV regulator, DMD buck converters, auxiliary LDOs and the LDO DMD that supports the HV regulator, all have a power good indication.

The DMD HV regulator is continuously monitored to check if the output rails DMD\_VRESET, DMD\_VOFFSET, and DMD\_VBIAS are in regulation. If either one of the output rails drops out of regulation (for example, due to a shorted output or overloading) the DMD\_PG\_FAULT bit in Detailed Status Register3 (0x29) is set. The threshold for DMD\_VRESET is 90% and the thresholds for DMD\_VOFFSET/ DMD\_VBIAS are 86% (rising edge) and 66% (falling edge).

The power good signal for the two DMD buck converters indicates if the output voltages (PWR1\_FB and PWR2\_FB) are within a defined window. The relative power good ratio is 72%. This means that if the output voltage is below 72% of the set output voltage the power good bit is asserted. The power good bits are in Detailed Status Register3 (0x29), bits BUCK DMD1 PG FAULT and BUCK DMD2 PG FAULT.

LDO\_1 and LDO\_2 output voltages are also monitored. When the power good fault of the LDO is asserted it implies that the LDO voltage is below 80% (rising edge) or 60% (falling edge) of its intended value. The power good indication for the LDOs is in <a href="Detailed Status Register3">Detailed Status Register3</a> (0x29), bits LDO\_GP1\_PG\_FAULT / LDO\_DMD1\_PG\_FAULT and LDO\_GP2\_PG\_FAULT / LDO\_DMD2\_PG\_FAULT.

#### 6.3.2.4.2 Overvoltage Fault

An overvoltage fault occurs when an output voltage rises above a pre-defined threshold. Overvoltage faults are indicated for the DMD buck converters, auxiliary LDOs, and the LDO DMD supporting the DMD HV regulator. The overvoltage faults of LDO\_1 and LDO\_2 are not incorporated in the overall DMD\_FAULT when the LDOs are used as general-purpose LDOs. Table 6-1 provides an overview of the possible DMD overvoltage faults and the faults' threshold levels.

#### 6.3.3 Buck Converters

The DLPA3082 contains one general-purpose buck converter and a supporting LDO (LDO\_BUCKS). The programmable 8-bit buck converter can generate a voltage between 1V and 5V, and have an output current limit of 3A. General purpose buck2 (PWR6) is currently supported. One buck converter and the LDO\_BUCKS are depicted in Figure 6-5.

The two DMD/DLPC buck converters discussed earlier in Section 6.3.2 have the same architecture as the buck converter and can be configured in the same way.



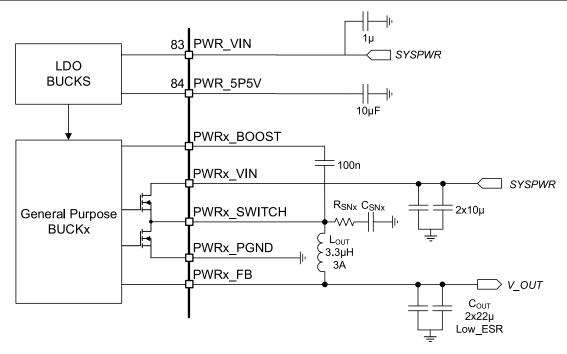


Figure 6-5. Buck Converter

#### 6.3.3.1 LDO Bucks

This regulator supports the general-purpose buck converter and the two DMD/DLPC buck converters and provides an analog voltage of 5.5V to the internal circuitry. Use a  $1\mu F$  capacitor on the input and a  $10\mu F$  capacitor on the output of the LDO.

### 6.3.3.2 General Purpose Buck Converters

The buck converter is for general-purpose use (Figure 6-5). The converter can be enabled or disabled through Enable Register (0x01): BUCK GP2 EN.

General purpose buck2 (PWR6) has a current capability of 2A.

The buck converter can operate in two switching modes: Normal, 600kHz switching frequency mode and the skip mode. The skip mode is designed to increase light load efficiency. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to the point that the current's rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the MOSFET's zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage.

#### 6.3.3.3 Buck Converter Monitoring

The buck converter block is continuously monitored for system failures to prevent damage to the DLPA3082 and peripherals. Several possible failures are monitored such as a too high or too low output voltage. The possible faults are summarized in Table 6-2.

 POWER GOOD

 BLOCK
 REGISTER BIT
 THRESHOLD (RISING EDGE)

 Gen.Buck2
 BUCK\_GP2\_PG\_FAULT
 Ratio 72%

 OVERVOLTAGE

 Gen.Buck2
 BUCK\_GP2\_OV\_FAULT
 Ratio 120%

Table 6-2. Buck Converter Fault Indication

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#### 6.3.3.3.1 Power Good

The buck converter as well as the supporting LDO\_BUCK have a power good indication. The buck converter has a separate indication.

The power good for the buck converter indicates if the output voltage (PWR6\_FB) is within a defined window. The relative power good ratio is 72%. This means that if the output voltage is below 72% of the set voltage the PG\_fault bit is set high. The power good bit of the buck converter is in Detailed Status Register1 (0x27) bit:

BUCK\_GP2\_PG\_FAULT for BUCK2 (PWR6)

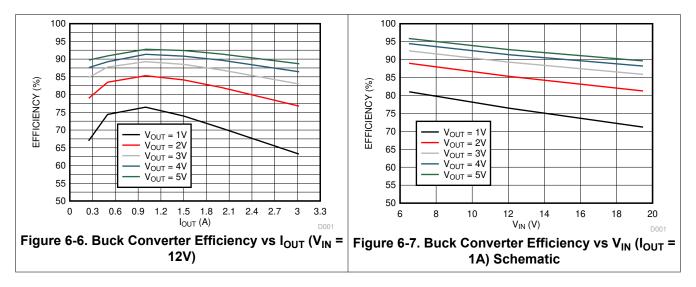
#### 6.3.3.3.2 Overvoltage Fault

An overvoltage fault occurs when an output voltage rises above a predefined threshold. Overvoltage faults are indicated for the buck converter and LDO\_BUCKS. The overvoltage fault of the LDO\_BUCKS is asserted if the LDO voltage is above 7.2V. The overvoltage of the general-purpose buck converter is 120% of the set value and can be read through Detailed Status Register2 (0x28), bit BUCK GP2 OV FAULT.

#### 6.3.3.4 Buck Converter Efficiency

Figure 6-6 shows an overview of the efficiency of the buck converter for an input voltage of 12V. The efficiency is shown for several output voltage levels where the load current is swept.

Figure 6-7 depicts the buck converter efficiency versus input voltage  $(V_{IN})$  for a load current  $(I_{OUT})$  of 1A for various output voltage levels  $(V_{OUT})$ .



### 6.3.4 Auxiliary LDOs

LDO\_1 and LDO\_2 are the two auxiliary LDOs that can be used by an additional external application. All other LDOs are for internal usage only and cannot be loaded. LDO\_1 (PWR4) is a fixed voltage of 3.3V, while LDO\_2 (PWR3) is a fixed voltage of 2.5V. Both LDOs are capable of delivering 200mA.

#### 6.3.5 Measurement System

The measurement system (Figure 6-8) is designed to sense internal and external nodes and convert them to digital by the implemented AFE comparator. The reference signal for this comparator, ACMPR\_REF, is a low-pass filtered PWM signal coming from the DLPC. To be able to cover a wide range of input signals, a variable gain amplifier (VGA) is added with three gain settings (1x, 9.5x, and 18x). The maximum input voltage of the VGA is 1.5V. However, some of the internal voltages are too large to be handled by the VGA and are divided down first.



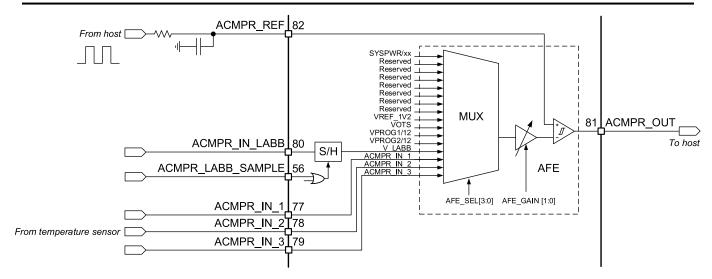


Figure 6-8. Measurement System Schematic

The system input voltage SYSPWR can be measured by selecting the SYSPWR/xx input of the MUX. Before the system input voltage is supplied to the MUX, the voltage needs to be divided. This is because the variable gain amplifier (VGA) can handle voltages up to 1.5V, whereas the system voltage can be as high as 20V. The division is done internally in the DLPA3082.

VOTS is connected to an on-chip temperature sensor. The voltage is a measure of the chip's junction temperature: Temperature ( $^{\circ}$ C) = 300 × VOTS (V) – 270.

LABB is a feature that stands for Local Area Brightness Boost. LABB locally increases the brightness while maintaining good contrast and saturation. Connect the sensor this feature to pin ACMPR\_IN\_LABB.

ACMPR\_IN\_1,2,3 can measure external signals from for instance a temperature sensor. Ensure the voltage on the input does not exceed 1.5V.

#### 6.4 Device Functional Modes

Table 6-3. Modes of Operation

MODE	DESCRIPTION
OFF	This is the lowest-power mode of operation. All power functions are turned off, registers are reset to default values, and the IC does not respond to SPI commands. RESET_Z pin is pulled low. The IC enters OFF mode whenever the PROJ_ON pin is low.
WAIT	The DMD regulators are turned off, but the IC does respond to the SPI. The device enters WAIT mode whenever PROJ_ON is set high, DMD_EN <sup>(1)</sup> bit is set to 0 or a FAULT is resolved.
STANDBY	The device also enters STANDBY mode when a fault condition is detected <sup>(2)</sup> . (See Section 6.5.2). Once the fault condition is resolved, WAIT mode is entered.
ACTIVE	The DMD supplies are enabled. PROJ_ON pin must be high, DMD_EN bit must be set to 1.

- (1) Settings can be done through Enable register, bit DMD EN.
- (2) Power-good faults, overvoltage, overtemperature shutdown, and undervoltage lockout.

Table 6-4. Device State as a Function of Control-Pin Status

PROJ_ON Pin	STATE
LOW	OFF
HIGH	WAIT STANDBY ACTIVE (Device state depends on DMD_EN bit and whether there are any fault conditions.)



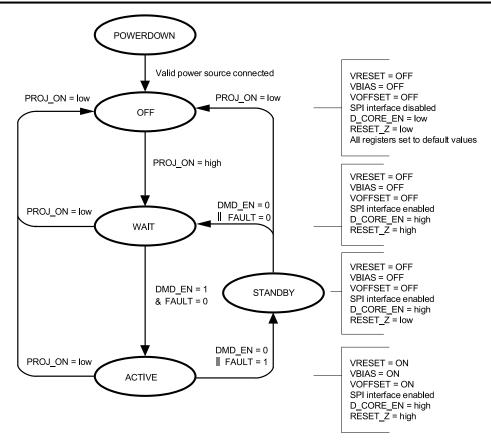


Figure 6-9. State Diagram

- A. || = OR, & = AND
- B. FAULT = Undervoltage on any supply, thermal shutdown, or UVLO detection
- C. UVLO detection, per the diagram, causes the DLPA3082 to go into the standby state. This is not the lowest power state. If lower power is desired, PROJ\_ON must be set low.
- D. DMD\_EN register bit can be reset or set by SPI writes. DMD\_EN defaults to 0 when PROJ\_ON goes from low to high and then the DLPC ASIC software automatically sets DMD\_EN to 1. Also, FAULT = 1 causes the DMD\_EN register bit to be reset.
- E. D\_CORE\_EN is a signal internal to the DLPA3082. This signal turns on the VCORE regulator.

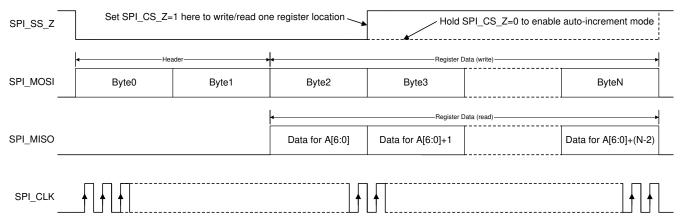
## 6.5 Programming

This section discusses the serial protocol interface (SPI) of the DLPA3082 as well as the interrupt handling, device shutdown, and register protection.

#### 6.5.1 SPI

The DLPA3082 provides a 4-wire SPI port that supports two SPI clock frequency modes: 0MHz to 36MHz and 20MHz to 40MHz. The clock frequency mode can be set in register DIG\_SPI\_FAST\_SEL. The interface supports both read and write operations. The SPI\_SS\_Z input serves as the active low chip select for the SPI port. The SPI\_SS\_Z input must be forced low for writing to or reading from registers. When SPI\_SS\_Z is forced high, the data at the SPI\_MOSI input is ignored, and the SPI\_MISO output is forced to a high-impedance state. The SPI\_MOSI input serves as the serial data input for the port; the SPI\_MISO output serves as the serial data output. The SPI\_CLK input serves as the serial data clock for both the input and output data. Data at the SPI\_MOSI input is latched on the rising edge of SPI\_CLK, while data is clocked out of the SPI\_MISO output on the falling edge of SPI\_CLK. Figure 6-10 illustrates the SPI port protocol. Byte 0 is referred to as the command byte, where the most significant bit is the write/not-read bit. For the W/nR bit, a 1 indicates a write operation, while a 0 indicates a read operation. The remaining seven bits of the command byte are the register address targeted by the write or read operation. The SPI port supports write and read operations for

multiple sequential register addresses through the implementation of an auto-increment mode. As shown in Figure 6-10, the auto-increment mode is invoked by simply holding the SPI\_SS\_Z input low for multiple data bytes. The register address is automatically incremented after each data byte transferred, starting with the address specified by the command byte. After reaching address 0x7Fh the address pointer jumps back to 0x00h.



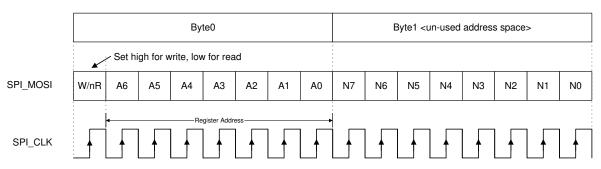


Figure 6-10. SPI Protocol

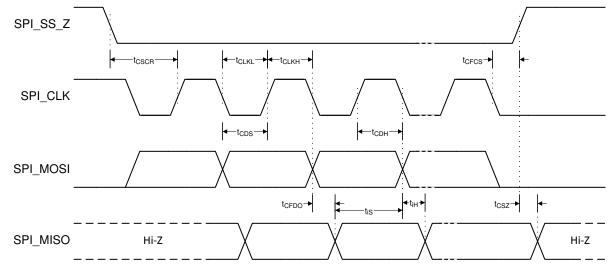


Figure 6-11. SPI Timing Diagram

### 6.5.2 Interrupt

The DLPA3082 has the capability to flag several faults in the system, such as overheating, power good, and overvoltage faults. If a certain fault condition occurs, one or more bits in the Table 6-5 are set. The setting of a bit in Main Status register (0x0C) triggers an interrupt event, which pulls down the INT\_Z pin. Interrupts can be masked by setting the respective MASK bits in Interrupt Mask register . Setting a MASK bit prevents the INT\_Z is pulled low for the particular fault condition. The high-level faults can be read in Main Status register (0x0C), while the lower-level faults can be read in Detailed status register1 (0x27) through Detailed status register4 (0x2A). Table 6-5 provides an overview of the faults and how they are related.

Table 6-5. Interrupt Registers

HIGH-LEVEL	MID-LEVEL	LOW-LEVEL		
		DMD_PG_FAULT		
		BUCK_DMD1_PG_FAULT		
		BUCK_DMD1_OV_FAULT		
		BUCK_DMD2_PG_FAULT		
	DMD_FAULT	BUCK_DMD2_OV_FAULT		
SUPPLY_FAULT		LDO_GP1_PG_FAULT / LDO_DMD1_PG_FAULT		
		LDO_GP1_OV_FAULT / LDO_DMD1_OV_FAULT		
		LDO_GP2_PG_FAULT / LDO_DMD2_PG_FAULT		
		LDO_GP2_OV_FAULT / LDO_DMD2_OV_FAULT		
	BUCK_GP2_PG_FAULT			
	BUCK_GP2_OV_FAULT			
PROJ_ON_INT				
TS_SHUT				
TS_WARN				

#### 6.5.3 Fast-Shutdown in Case of Fault

The DLPA3082 has two shutdown modes: a normal shutdown initiated after pulling PROJ\_ON level low and a fast power-down mode. The fast power-down feature can be enabled or disabled through register Main Status register (0x01), bit 7, FAST\_SHUTDOWN\_EN. By default, the mode is enabled.

When the fast power-down feature is enabled, a fast shutdown is initiated for specific faults. This shutdown happens autonomously from the DLPC. The DLPA3082 enters the fast-shutdown mode only for specific faults, thus not for all the faults flagged by the DLPA3082. The faults for which the DLPA3082 goes into fast shutdown are listed in Table 6-6.

Table 6-6. Faults that Trigger a Fast-Shutdown

HIGH-LEVEL	LOW-LEVEL	
TS_SHUT		
	DMD_PG_FAULT	
	BUCK_DMD1_PG_FAULT	
	BUCK_DMD1_OV_FAULT	
	BUCK_DMD2_PG_FAULT	
DMD_FAULT	BUCK_DMD2_OV_FAULT	
	LDO_GP1_PG_FAULT / LDO_DMD1_PG_FAULT	
	LDO_GP1_OV_FAULT / LDO_DMD1_OV_FAULT	
	LDO_GP2_PG_FAULT / LDO_DMD2_PG_FAULT	
	LDO_GP2_OV_FAULT / LDO_DMD2_OV_FAULT	



# **6.6 Register Maps**

Register Address, Default, R/W, Register name. **Boldface** settings are the hardwired defaults.

Table 6-7. Register Map

NAME	BITS	DESCRIPTION
0x00, 40, R/W, Chip Identification		
CHIPID	[7:4]	Chip identification number: 3 (hex)
REVID	[3:0]	Revision number, 0 (hex)
0x01, 82, R/W, Enable Register		
FAST_SHUTDOWN_EN	[7]	0: Fast shutdown disabled 1: Fast shutdown enabled
CW_EN	[6]	Reserved
BUCK_GP3_EN	[5]	Reserved, value default as 0
BUCK_GP2_EN	[4]	0: General purpose buck2 disabled 1: General purpose buck2 enabled
BUCK_GP1_EN	[3]	Reserved, value default as 0
Reserved	[2]	Reserved
Reserved	[1]	Reserved
DMD_EN	[0]	0: DMD regulators disabled 1: DMD regulators enabled
0x0C, 00, R, Main Status Register		
SUPPLY_FAULT	[7]	0: No PG or OV failures for any of the LV Supplies 1: PG failures for a LV Supplies
Reserved	[6]	Reserved
PROJ_ON_INT	[5]	0: PROJ_ON = HIGH 1: PROJ_ON = LOW
DMD_FAULT	[4]	0: DMD_FAULT = LOW 1: DMD_FAULT = HIGH
BAT_LOW_SHUT	[3]	Reserved
BAT_LOW_WARN	[2]	Reserved
TS_SHUT	[1]	0: Chip temperature < 132.5°C and no violation in V5V0 1: Chip temperature > 156.5°C, or violation in V5V0
TS_WARN	[0]	0: Chip temperature < 121.4°C 1: Chip temperature > 123.4°C

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**Table 6-7. Register Map (continued)** 

		Table 6-7. Register Map (continued)	
NAME	BITS	DESCRIPTION	
0x0D, F5, Interrupt Mask Register	•		
SUPPLY_FAULT_MASK	[7]	0: Not masked for SUPPLY_FAULT interrupt 1: Masked for SUPPLY_FAULT interrupt	
Reserved	[6]	Reserved	
PROJ_ON_INT_MASK	[5]	0: Not masked for PROJ_ON_INT interrupt  1: Masked for PROJ_ON_INT interrupt	
DMD_FAULT_MASK	[4]	0: Not masked for DMD_FAULT interrupt  1: Masked for DMD_FAULT interrupt	
BAT_LOW_SHUT_MASK	[3]	Reserved, value default as 0	
BAT_LOW_WARN_MASK	[2]	Reserved, value default as 1	
TS_SHUT_MASK	[1]	0: Not masked for TS_SHUT interrupt 1: Masked for TS_SHUT interrupt	
TS_WARN_MASK	[0]	0: Not masked for TS_WARN interrupt  1: Masked for TS_WARN interrupt	
0x27, 00, R, Detailed status regist	er1 (Pow	ver good failures for general purpose block)	
BUCK_GP3_PG_FAULT	[7]	Reserved, value default as 0	
BUCK_GP1_PG_FAULT	[6]	Reserved, value default as 0	
BUCK_GP2_PG_FAULT	[5]	0: No fault 1: General purpose buck2 power good failure. Does not initiate a fast shutdown.	
Reserved	[4]	Reserved	
Reserved	[3]	Reserved	
Reserved	[2]	Reserved	
Reserved	[1]	Reserved, value always 0	
Reserved	[0]	Reserved, value always 0	
0x28, 00, R, Detailed status regist	er2 (Ove	rvoltage failures for general purpose block)	
BUCK_GP3_OV_FAULT	[7]	Reserved, value default as 0	
BUCK_GP1_OV_FAULT	[6]	Reserved, value default as 0	
BUCK_GP2_OV_FAULT	[5]	0: No fault 1: General purpose buck2 overvoltage failure. Does not initiate a fast shutdown.	
Reserved	[4]	Reserved, value always 0	
Reserved	[3]	Reserved	
Reserved	[2]	Reserved	
Reserved	[1]	Reserved, value always 0	
Reserved	[0]	Reserved, value always 0	
0x29, 00, R, Detailed status regist	er3 (Pow	ver good failure for DMD related blocks)	
Reserved	[7]	Reserved, value always 0	
DMD_PG_FAULT	[6]	0: No fault 1: VBIAS, VOFS and/or VRST power good failure. Initiates a fast shutdown.	
BUCK_DMD1_PG_FAULT	[5]	0: No fault 1: Buck1 (used to create DMD voltages) power good failure. Initiates a fast shutdown.	
BUCK_DMD2_PG_FAULT	[4]	0: No fault 1: Buck2 (used to create DMD voltages) power good failure. Initiates a fast shutdown.	
Reserved	[3]	Reserved, value always 0	
Reserved	[2]	Reserved, value always 0	
LDO_GP1_PG_FAULT / LDO_DMD1_PG_FAULT	[1]	0: No fault 1: LDO1 (used as general purpose or DMD specific LDO) power good failure. Initiates a fast shutdown.	
LDO_GP2_PG_FAULT / LDO_DMD2_PG_FAULT	[0]	0: No fault 1: LDO2 (used as general purpose or DMD specific LDO) power good failure. Initiates a fast shutdown.	



**Table 6-7. Register Map (continued)** 

NAME	BITS	DESCRIPTION		
0x2A, 00, R, Detailed status register4 (Overvoltage failures for DMD related blocks and Color Wheel)				
Reserved	[7]	Reserved, value always 0		
Reserved	[6]	Reserved, value always 0		
BUCK_DMD1_OV_FAULT	[5]	0: No fault 1: Buck1 (used to create DMD voltage) overvoltage failure		
BUCK_DMD2_OV_FAULT	[4]	0: No fault 1: Buck2 (used to create DMD voltage) overvoltage failure		
Reserved	[3]	Reserved, value always 0		
Reserved	[2]	Reserved, value always 0		
LDO_GP1_OV_FAULT / LDO_DMD1_OV_FAULT	[1]	0: No fault 1: LDO1 (used as general purpose or DMD specific LDO) overvoltage failure		
LDO_GP2_OV_FAULT / LDO_DMD2_OV_FAULT	[0]	0: No fault 1: LDO2 (used as general purpose or DMD specific LDO) overvoltage failure		



# 7 Application and Implementation

#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

In display applications, using the DLPA3082 provides all needed analog functions. Each DLP application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC84xx DLP controller chips.

## 7.2 Typical Application

A common application when using DLPA3082 is to use it with a 0.47-inch 4K DMD (DLP472TP) and DLPC84xx controller for creating a small, ultra-portable projector. The DLPC84xx in the projector typically receives images from a PC or video player using HDMI or VGA analog as shown in Figure 7-1. Card readers and Wi-Fi can also receive images if the appropriate peripheral chips are added.

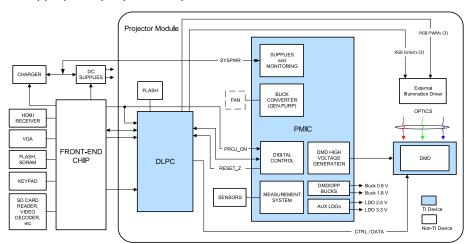


Figure 7-1. Typical Setup Using DLPA3082

#### 7.2.1 Design Requirements

An ultra-portable projector can be created by using a DLP chipset comprised of a DMD, DLPC84xx controller, and the DLPA3082 PMIC. The DLPC84xx manages the digital image processing, the DLPA3082 provides the needed analog functions for the projector, and the DMD is the display device for producing the projected image. In addition to the three DLP chips in the chipset, other chips can be included. At a minimum, a Flash part is needed to store the software and firmware to control the DLPC84xx. To connect the DLPC84xx to the frontend chip for receiving images, use the parallel interface. While using the parallel interface, connect the I<sup>2</sup>C to the frontend chip for inputting commands to the DLPC84xx.

The DLPA3082 has three built-in buck-switching regulators to serve as projector system power supplies. Two of the regulators are fixed to 0.8V and 1.8V for powering the DLP chipset. The remaining buck regulator is available for general-purpose use and its voltage is programmable. The regulator can be used to drive a variable-speed fan or to power other projector chips such as the frontend chip. The only power supply needed at the DLPA3082 input is SYSPWR from an external DC power supply. The entire projector can be turned on and off by using a single signal called PROJ ON. When PROJ ON is high, the projector turns on and begins displaying images. When PROJ ON is set low, the projector turns off and draws just microamps of current on SYSPWR.



### 7.2.2 Detailed Design Procedure

To connect the 0.47-inch 4K DMD (DLP472TP), the DLPC84xx, and the DLPA3082 devices, see the reference design schematic. When a circuit board layout is created from this schematic a very small circuit board is possible. An example small board layout is included in the reference design data base. Layout guidelines must be followed to achieve reliable projector operation. The optical engine that has the illumination package and the DMD mounted to it is typically supplied by an optical OEM who specializes in designing optics for DLP projectors.

### 7.2.2.1 Component Selection for General-Purpose Buck Converter

The theory of operation of a buck converter is explained in application note, *Understanding Buck Power Stages in Switchmode Power Supplies*, SLVA057. This section is limited to the component selection. For proper operation, selection of the external components is very important, especially the inductor  $L_{OUT}$  and the output capacitor  $C_{OUT}$ . For best efficiency and ripple performance, choose an inductor and capacitor with low equivalent series resistance (ESR).

Product Folder Links: *DLPA3082* 

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# 7.3 System Example with DLPA3082 Internal Block Diagram

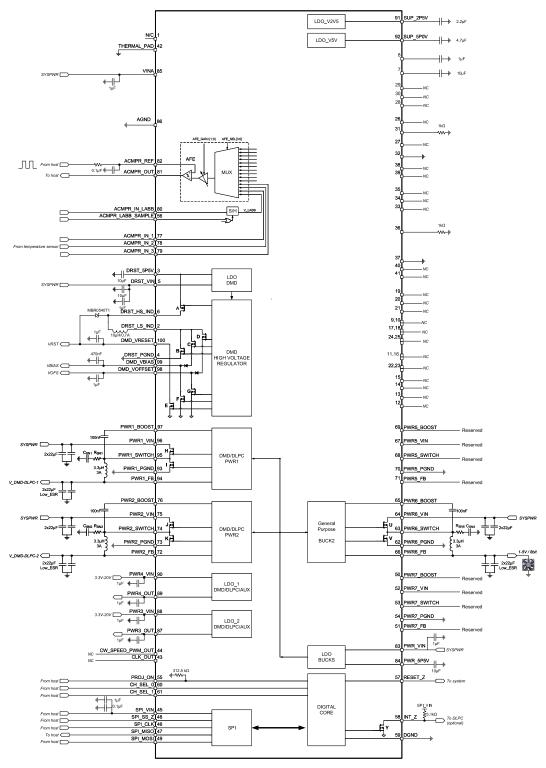


Figure 7-2. Typical Application:  $V_{IN} = 12V$ 



## 7.4 Power Supply Recommendations

The DLPA3082 is designed to operate from a 6V to 20V input voltage supply. To avoid insufficient supply current due to line drop, ringing due to trace inductance at the VIN terminals, or supply peak current limitations, additional bulk capacitance is possibly required. In the case of ringing caused by the interaction with the ceramic input capacitors, an electrolytic or tantalum-type capacitor is needed for damping.

Evaluate the amount of bulk capacitance required, such that the input voltage can remain in spec long enough for a proper fast shutdown to occur for the VOFFSET, VRESET, and VBIAS supplies. The shutdown begins when the input voltage drops below the programmable UVLO threshold such as when the external power supply is suddenly removed from the system.

## 7.4.1 Power-Up and Power-Down Timing

The power-up and power-down sequence is important to ensure the correct operation of the DLPA3082 and to prevent damage to the DMD. The DLPA3082 controls the correct sequencing of the DMD\_VRESET, DMD\_VBIAS, and DMD\_VOFFSET to ensure a reliable operation of the DMD.

The general startup sequence of the supplies is described in *Supply and Monitoring*. The power-up sequence of the high voltage DMD lines is especially important to not damage the DMD. Avoid a too large delta voltage between DMD VBIAS and DMD VOFFSET, which can cause damage.

After PROJ\_ON is pulled high, the DMD buck converters and LDOs are powered (PWR1-4) and the DMD high voltage lines (HV) are sequentially enabled. First, DMD\_VOFFSET is enabled. After a delay, DMD\_VBIAS is enabled. Finally, after another delayDMD\_VRESET is enabled. Now the DLPA3082 is fully powered and ready for starting projection.

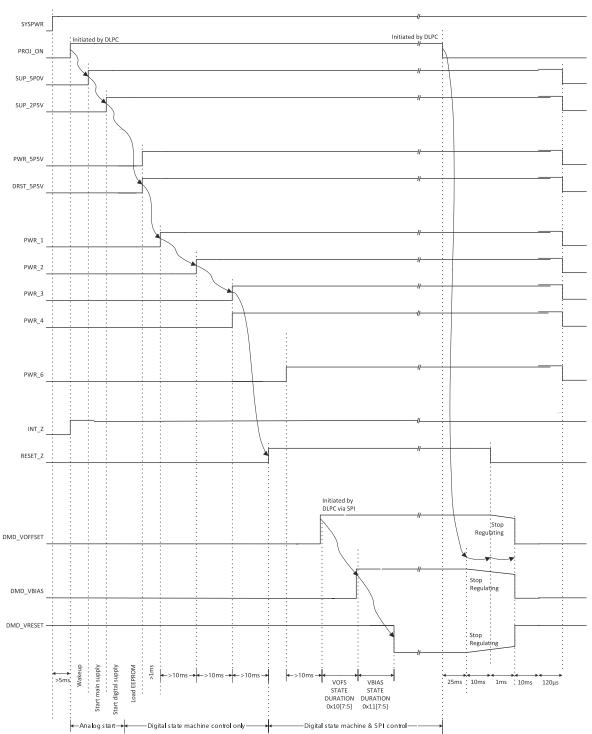
For power down there are two sequences, normal power down (Figure 7-3) and a fault fast power down used in case a fault occurs (Figure 7-4).

In normal power down mode, the power down is initiated after pulling PROJ\_ON pin low. 25ms after PROJ\_ON is pulled low, first DMD\_VBIAS and DMD\_VRESET stop regulating, 10ms later, DMD\_VOFFSET stops regulating. When DMD\_VOFFSET stopped regulating, RESET\_Z is pulled low. 1ms after the DMD\_VOFFSET stops regulating, all other supplies are turned off. INT\_Z remains high during the power down sequence since no fault occurred. During power down it is ensured that the HV levels do not violate the DMD specifications on these three lines. For this to occur, it is important to select the capacitors such that  $C_{VOFFSET}$  is equal to  $C_{VRESET}$  and  $C_{VBIAS}$  is  $\leq C_{VOFFSET}$ ,  $C_{VRESET}$ .

The fast power down mode (Figure 7-4) is started in case a fault occurs (INT\_Z is pulled low), for instance, due to overheating. The fast power down mode can be enabled or disabled through Main Status register (0x01), bit 7, FAST\_SHUTDOWN\_EN. By default, the mode is enabled. After the fault occurs, the regulation of DMD\_VBIAS and DMD\_VRESET is stopped. There is 540µs default delay time between fault and stop of regulation. After the regulation stops, there is a 4µs default delay time before all three DMD\_VRESET, DMD\_VBIAS, and DMD\_VOFFSET high voltages lines are discharged and RESET\_Z is pulled low.

Now the DLPA3082 is in a standby state. It remains in standby state until the fault resolves. In case the fault resolves a restart is initiated. It starts then by powering up PWR\_3 and follows the regular power-up as depicted

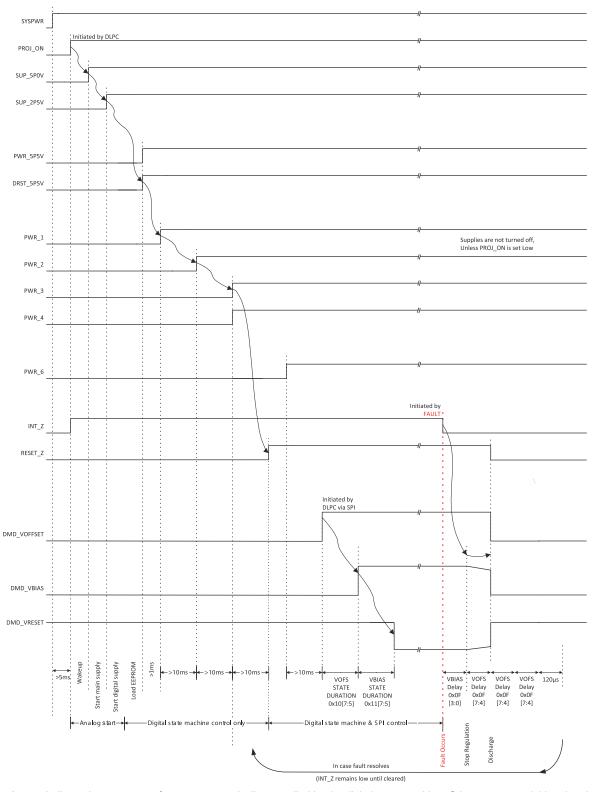
in Figure 7-4. Again, for proper discharge timing and levels, the capacitors must be selected such that  $C_{VOFFSET}$  is equal to  $C_{VRESET}$  and  $C_{VBIAS}$  is  $\leq C_{VOFFSET}$ ,  $C_{VBIAS}$ .



- 1. Arrows indicate the sequence of events automatically controlled by the digital state machine. Other events are initiated under SPI control
- 2. SUP\_5P0V and SUP\_2P5V rise to a precharge level with SYSPWR, and reach the full level potential after PROJ\_ON is pulled high.

Figure 7-3. Power Sequence Normal Shutdown Mode





- Arrows indicate the sequence of events automatically controlled by the digital state machine. Other events are initiated under SPI control.
- SUP\_5P0V and SUP\_2P5V rise to a precharge level with SYSPWR, and reach the full level potential after PROJ\_ON is pulled high.

Figure 7-4. Power Sequence Fault Fast Shutdown Mode



### 7.5 Layout

### 7.5.1 Layout Guidelines

For switching power supplies, the layout is an important step in the design, especially when it concerns high peak currents and high switching frequencies. If the layout is not done carefully, the regulator can show stability issues and EMI problems. Therefore, use wide and short traces for high current paths and the return power ground paths. For the DMD HV regulator, place the input capacitor, output capacitor, and the inductor as close as possible to the IC. To minimize ground noise coupling between different buck converters, separate the grounds and connect them at a central point under the part. For the DMD HV regulator, the recommended value for the capacitors is 1µF for VRST and VOFS, and 470nF for VBIAS. The inductor value is 10µH.

The high currents of the buck converter concentrate around pins VIN, SWITCH, and PGND (Figure 7-5). The voltage at the pins VIN, PGNDm, and FB are DC voltages while the pin SWITCH has a switching voltage between VIN and PGND. In case the FET between pins 63–4 is closed, the red line indicates the current flow while the blue line indicates the current flow when the FET between pins 62–63 is closed.

These paths carry the highest currents and must be kept as short as possible.

For the LDO DMD, use a  $1\mu$ F capacitor in parallel with a  $10\mu$ F capacitor on the input and a  $10\mu$ F capacitor on the output of the LDO. Make the voltage rating of the capacitor equal to or greater than two times the applied voltage across the capacitor in the application.

For LDO bucks, use a  $1\mu F$  capacitor on the input and a  $10\mu F$  capacitor on the output of the LDO. Make the voltage rating of the capacitor equal to or greater than two times the applied voltage across the capacitor in the application.

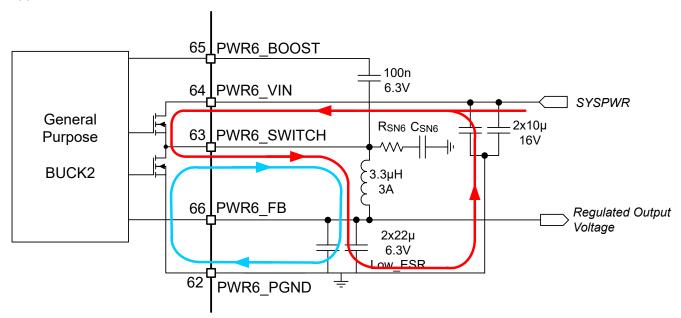


Figure 7-5. High AC Current Paths in a Buck Converter

The trace to the VIN pin carries high AC currents; therefore, the trace must be low resistive to prevent a voltage drop across the trace. Additionally, place the decoupling capacitors as close to the VIN pin as possible.

The SWITCH pin is connected alternately to the VIN or GND. This means a square wave voltage is present on the SWITCH pin with an amplitude of VIN, and containing high frequencies. This can lead to EMI problems if not properly handled. To reduce EMI problems, place a snubber network (RSN6 and CSN6) at the SWITCH pin to prevent and suppress unwanted high-frequency ringing at the moment of switching.

The PGND pin sinks high current. Connect the PGND pin to a star ground point so it does not interfere with other ground connections.



The FB pin is the sense connection for the regulated output voltage, which is a DC voltage; nothing flows through this pin. The voltage on the FB pin is compared with the internal reference voltage to control the loop. Make the FB connection at the load so that the I•R drop does not affect the sensed voltage.

#### 7.5.1.1 SPI Connections

The SPI interface consists of several digital lines and the SPI supply. If routing the interface lines is not done properly, communication errors can occur. Prevent SPI lines from picking up noise and keep other possible interfering sources from the interface.

Pickup of noise can be prevented by ensuring that the SPI ground line is routed together with the digital lines as much as possible to the respective pins. The SPI interface can be connected by a separate ground connection to the DGND of the DLPA3082 in Figure 7-6. This prevents ground noise between SPI ground references of DLPA3082 and DLPC due to the high current in the system.

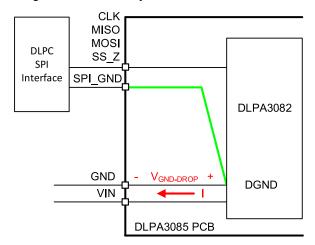


Figure 7-6. SPI Connections

Keep interfering sources away from the interface lines as much as possible. If any power lines are routed too close to the SPI CLK, it can lead to false clock pulses and thus communication errors.

### 7.5.2 Layout Example

A layout example of a buck converter is shown in Figure 7-7, illustrating the optimal routing and placement of components around the DLPA3082. This can be used as a reference for a general-purpose buck2 (PWR6). The layout example illustrates the inductor and the accompanying capacitors as close as possible to the corresponding pins using the thickest possible traces. The capacitors use multiple vias to the ground layer to ensure a low resistance path and minimize the distance between the ground connections of the output capacitors and the ground connections of the buck converter.

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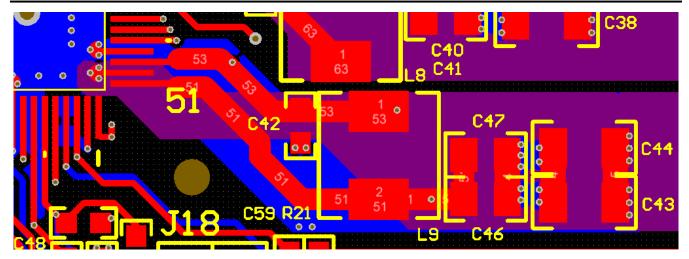


Figure 7-7. Practical Layout

A proper layout requires short traces and separate power grounds to avoid losses from trace resistance and to avoid ground shifting. Use high-quality capacitors with low ESR to keep capacitor losses minimal and to maintain an acceptable voltage ripple at the output.

Use an RC snubber network to avoid EMI that can occur when switching high currents at high frequencies. There is a possibility the EMI has a higher amplitude and frequency than the switching voltage.

### 7.5.3 Thermal Considerations

Power dissipation must be considered when implementing integrated circuits in low-profile and fine-pitch surface-mount packages. Many system-related issues affect power dissipation: thermal coupling, airflow, adding heat sinks and convection surfaces, and the presence of other heat-generating components. In general, there are three basic methods that can be used to improve thermal performance:

- Improving the heat-sinking capability of the PCB
- Reducing thermal resistance to the environment of the chip by adding or increasing heat sink capability on top of the package
- · Adding or

increasing

airflow in the system

The recommended junction temperature for the DLPA3082 is below 120°C during operation. The equation that relates junction temperature, T<sub>iunction</sub>, is given by:

$$T_{junction} = T_{ambient} + P_{diss} \times R_{\theta JA} \tag{1}$$

where  $T_{ambient}$  is the ambient temperature,  $P_{diss}$  is the total power dissipation, and  $R_{\theta JA}$  is the thermal resistance from junction to ambient.

The total power dissipation can vary depending on the application of the DLPA3082. The main contributors in the DLPA3082 are typically:

- Buck converters
- LDOs

For the buck converter, the power dissipation is given by:

$$P_{diss\_buck} = P_{in} - P_{out} = P_{out} \left( \frac{1}{\eta_{buck}} - 1 \right)$$
 (2)



where  $\eta_{buck}$  is the efficiency of the buck converter,  $P_{in}$  is the power delivered to the input of the buck converter, and  $P_{out}$  is the power delivered to the load of the buck converter. For the buck converter PWR1,2,6, the efficiency can be determined using the curves in Figure 6-6.

For the LDO, the power dissipation is given by:

$$P_{diss\_LDO} = (V_{in} - V_{out}) \times I_{load}$$
(3)

where  $V_{in}$  is the input supply voltage,  $V_{out}$  is the output voltage of the LDO, and  $I_{load}$  is the load current of the LDO. The voltage drop over the LDO ( $V_{in}$ – $V_{out}$ ) can be relatively large; a small load current can result in significant power dissipation. For this situation, a general-purpose buck converter can be a more efficient solution.

The LDO DMD provides power to the boost converter, and the boost converter provides high voltages for the DMD; that is,  $V_{BIAS}$ ,  $V_{OFS}$ , and  $V_{RST}$ . The current load on these lines can increase up to  $I_{load, max} = 10 mA$ . Assuming the efficiency of the boost converter,  $\eta_{boost}$  is 80%, the maximum boost converter power dissipation,  $P_{diss\_DMD\_boost, max}$ , can be calculated as:

$$P_{diss\_DMD\_boost,max} = I_{load,max} \left( V_{BIAS} + V_{OFS} + |V_{RST}| \right) \times \left( \frac{1}{\eta_{boost}} - 1 \right) \approx 0.1W$$
(4)

In general, the power dissipation of the boost converter is negligible. However, the power dissipation of the LDO DMD, P<sub>diss\_LDO\_DMD</sub> must be considered in the case of a high supply voltage. The worst-case load current for the LDO is given by:

$$I_{load\_LDO,max} = \frac{1}{\eta_{boost}} \frac{\left(V_{BIAS} + V_{OFS} + \left|V_{RST}\right|\right)}{V_{DRST\_5P5V}} I_{load,max} \approx 100 \text{mA}$$
(5)

where the output voltage of the LDO is  $V_{DRST}$  5P5V = 5.5V.

The worst-case power dissipation of the LDO DMD is approximately 1.5W when the input supply voltage is 19.5V. For your specific application, check the LDO current level. Therefore, the total power dissipation of the DLPA3082 can be described as:

$$P_{\text{diss\_DLPA3082}} = \sum P_{\text{buck\_converter}} + \sum P_{\text{LDOs}}$$
 (6)

The following examples calculate the maximum ambient temperature and the junction temperature based on known information.

If it is assumed that the total dissipation  $P_{diss\_DLPA3082}$ = 2.5W,  $T_{junction,max}$ = 120°C, and  $R_{\theta JA}$ = 7°C/W (refer to Section 5.4), then the maximum ambient temperature can be calculated using Equation 1.

$$T_{ambient,max} = T_{junction,max} - P_{diss} \times R_{t, JA} = 120^{\circ}C - 2.5W \times 7^{\circ}C/W = 102.5^{\circ}C$$

$$(7)$$

If the total power dissipation and the ambient temperature are known as:

$$T_{ambient} = 50^{\circ}C, R_{\theta JA} = 7^{\circ}C/W, P_{diss} D_{LPA3082} = 4W.$$
 (8)

the junction temperature can be calculated:

$$T_{junction} = T_{ambient} + P_{diss} \times R_{\theta JA} = 50^{\circ}C + 4W \times 7^{\circ}C/W = 78^{\circ}C$$
(9)

If the combination of ambient temperature and the total power dissipation of the DLPA3082 does not produce an acceptable junction temperature, that is, <120°C, there are two approaches:

Product Folder Links: DLPA3082



- 1. Use a larger heat sink or more airflow to reduce  $R_{\theta JA}$ .
- 2. Reduce power dissipation in DLPA3082:
  - Use an external buck converter instead of an internal general-purpose buck converter.
  - Reduce load current for the buck converter.

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## 8 Device and Documentation Support

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### 8.2 Device Support

### 8.2.1 Device Nomenclature

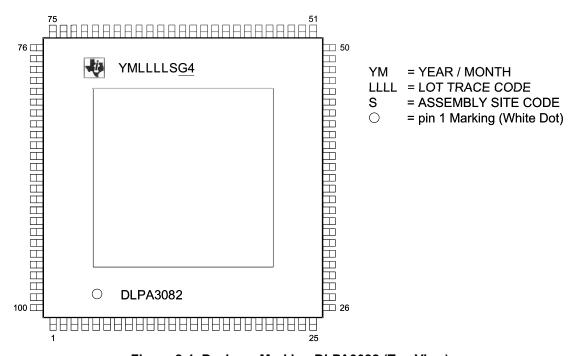


Figure 8-1. Package Marking DLPA3082 (Top View)

### 8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.4 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.7 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES				
October 2024 *		Initial Release				

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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#### PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
DLPA3082PFDR	Active	Production	HTQFP (PFD)   100	1000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	DLPA3082
DLPA3082PFDR.B	Active	Production	HTQFP (PFD)   100	1000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	DLPA3082

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

# **PACKAGE MATERIALS INFORMATION**

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### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DLPA3082PFDR	HTQFP	PFD	100	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2

# PACKAGE MATERIALS INFORMATION

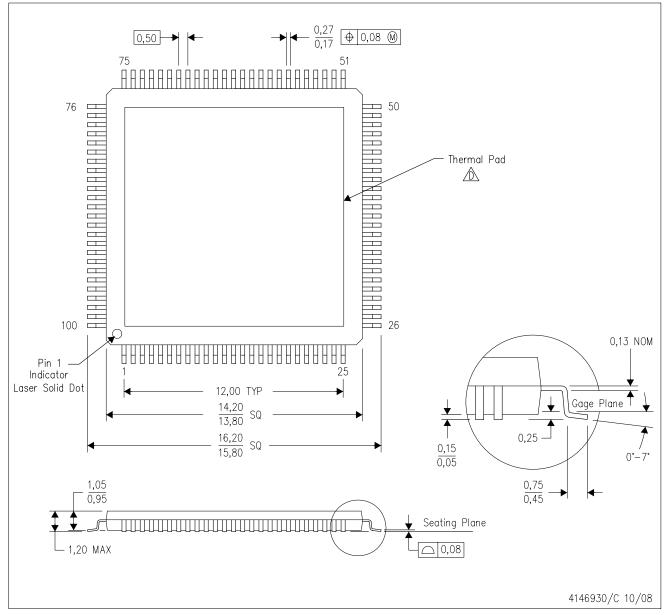
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### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
DLPA3082PFDR	HTQFP	PFD	100	1000	350.0	350.0	43.0	

# PFD (S-PQFP-G100) PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- This package is designed to be attached directly to an external heatsink. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <a href="https://www.ti.com">http://www.ti.com</a>. See the product data sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MS-026

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# PFD (S-PQFP-G100)

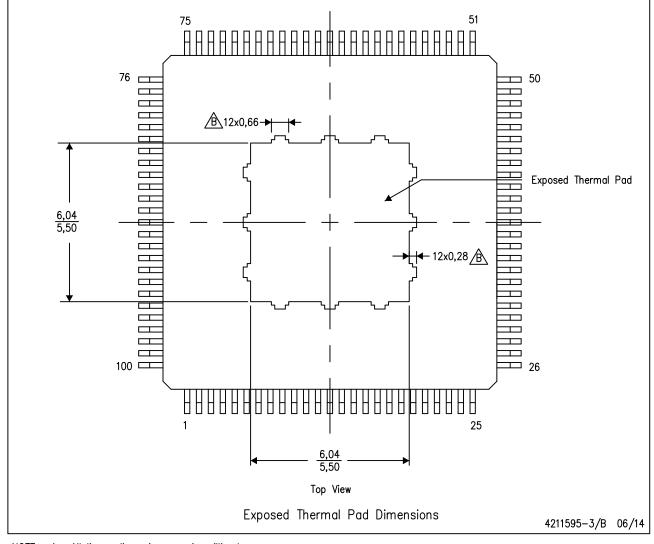
PowerPAD™ PLASTIC QUAD FLATPACK

### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: A. All linear dimensions are in millimeters

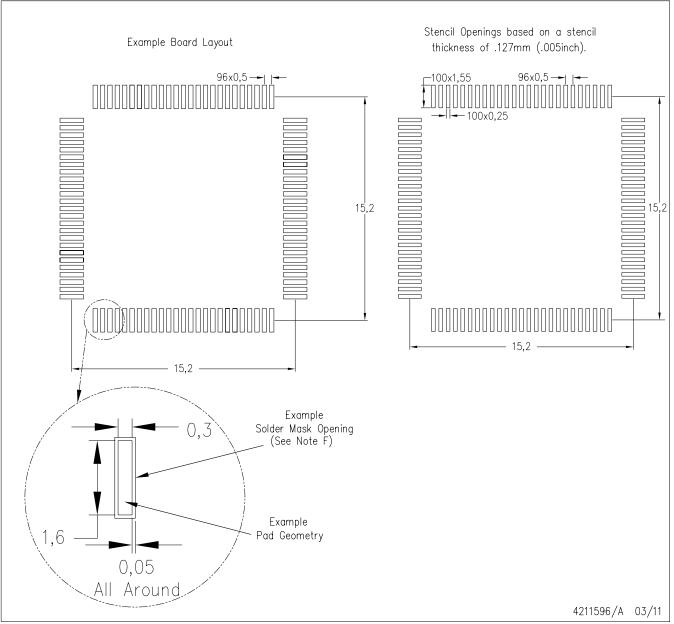
B Tie strap features may not be present.

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# PFD (S-PQFP-G100)

# PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:

- All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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