

DLP78TUV 0.78-Inch 4K UHD Digital Micromirror Device for 3D Printers

1 Features

- 0.78-inch diagonal micromirror array
 - 1920×1080 array of aluminum micrometer-sized mirrors, in an orthogonal layout
 - 8.2 Megapixels, 3840 × 2160 pixels on the resin
 - 9.0-micron mirror pitch
 - ±14.5° micromirror tilt (relative to flat surface)
 - Corner illumination for optimal efficiency and contrast
- 2xLVDS input data bus
- Dedicate DLPC6422 3D print light controller and DLPA100 and DLPA300 power management for reliable operation

2 Applications

- TI DLP® 3D Printer
 - Additive manufacturing
 - Vat polymerization
 - Masked stereolithography (mSLA 3D printer)
- Laser manufacturing
- Light exposure: programmable spatial and temporal light exposure

3 Description

The DLP78TUV digital micromirror device (DMD) is a digitally controlled micro-opto-electromechanical system (MOEMS) spatial light modulator (SLM) that enables 1080p and 4K UHD imaging systems. When coupled to an appropriate optical system, the DMD displays a very crisp and high-quality image. This DMD is a component of the chipset comprising DLP78TUV DMD, DLPC6422 light Controller, DLPA300 micromirror driver, and DLPA100 power supply. The compact physical size of the chipset provides a complete system that enables small form factor 4K UHD or 1080p HD imaging with high power output, high contrast optical engines for fast, high resolution, reliable DLP 3D Printers.

To help accelerate the design cycle, the DMD ecosystem includes established resources, which include [production ready optical modules](#), [optical module manufacturers](#), and [design houses](#).

Package Information

PART NUMBER ⁽¹⁾	PACKAGE	PACKAGE SIZE
DLP78TUV	FYU (350)	35.0mm × 32.2mm

(1) For more information, see the *Mechanical, Packaging, and Orderable* addendum.

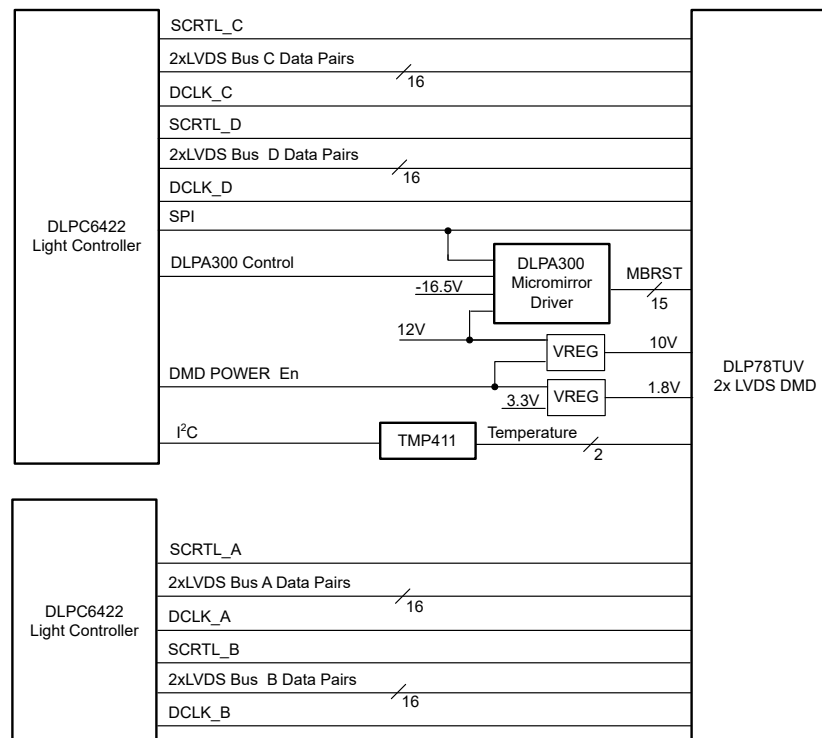


Figure 3-1 Simplified Application for 4K System



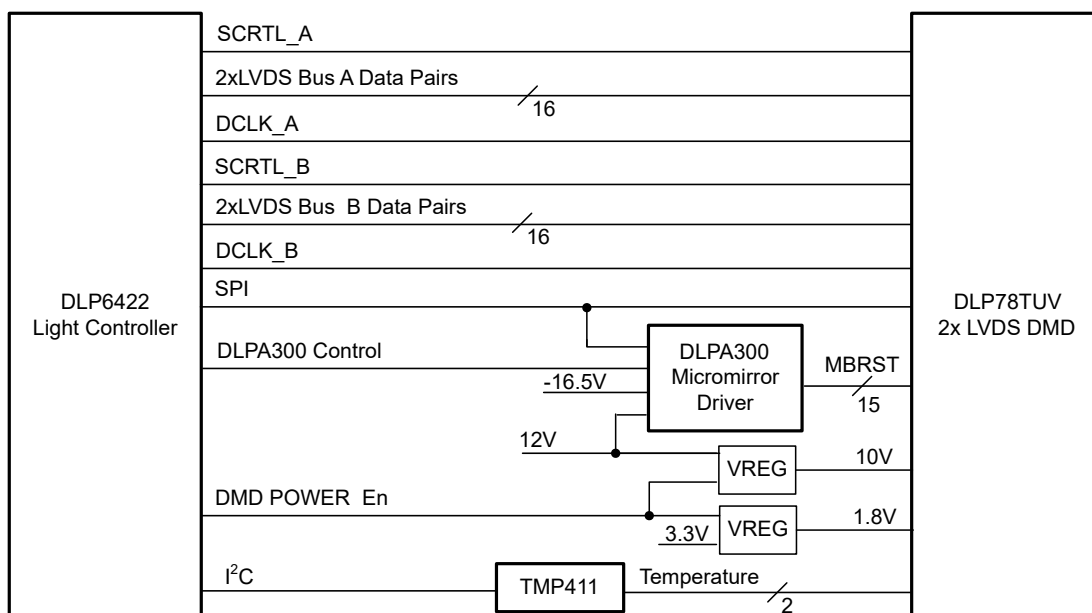


Figure 3-2 Simplified Application for 1080p System

Table of Contents

1 Features	1	6.6 Micromirror Array Temperature Calculation.....	30
2 Applications	1	6.7 Micromirror Power Density Calculation.....	31
3 Description	1	6.8 Window Aperture Illumination Overfill Calculation....	32
4 Pin Configuration and Functions	4	6.9 Micromirror Landed-On/Landed-Off Duty Cycle.....	33
5 Specifications	11	7 Application and Implementation	37
5.1 Absolute Maximum Ratings.....	11	7.1 Application Information.....	37
5.2 Storage Conditions.....	11	7.2 Typical Application.....	37
5.3 ESD Ratings.....	11	7.3 Temperature Sensor Diode.....	40
5.4 Recommended Operating Conditions.....	12	7.4 Power Supply Recommendations.....	41
5.5 Thermal Information.....	15	7.5 Layout.....	42
5.6 Electrical Characteristics.....	15	8 Device and Documentation Support	45
5.7 Timing Requirements.....	15	8.1 Third-Party Products Disclaimer.....	45
5.8 System Mounting Interface Loads.....	20	8.2 Device Support.....	45
5.9 Micromirror Array Physical Characteristics.....	22	8.3 Device Markings.....	45
5.10 Micromirror Array Optical Characteristics.....	23	8.4 Documentation Support.....	46
5.11 Window Characteristics.....	24	8.5 Receiving Notification of Documentation Updates....	46
5.12 Chipset Component Usage Specification.....	24	8.6 Support Resources.....	46
6 Detailed Description	26	8.7 Trademarks.....	46
6.1 Overview.....	26	8.8 Electrostatic Discharge Caution.....	46
6.2 Functional Block Diagram.....	27	8.9 Glossary.....	46
6.3 Feature Description.....	28	9 Revision History	46
6.4 Device Functional Modes.....	29	10 Mechanical, Packaging, and Orderable	
6.5 Optical Interface and System Image Quality		Information	46
Considerations.....	29		

4 Pin Configuration and Functions

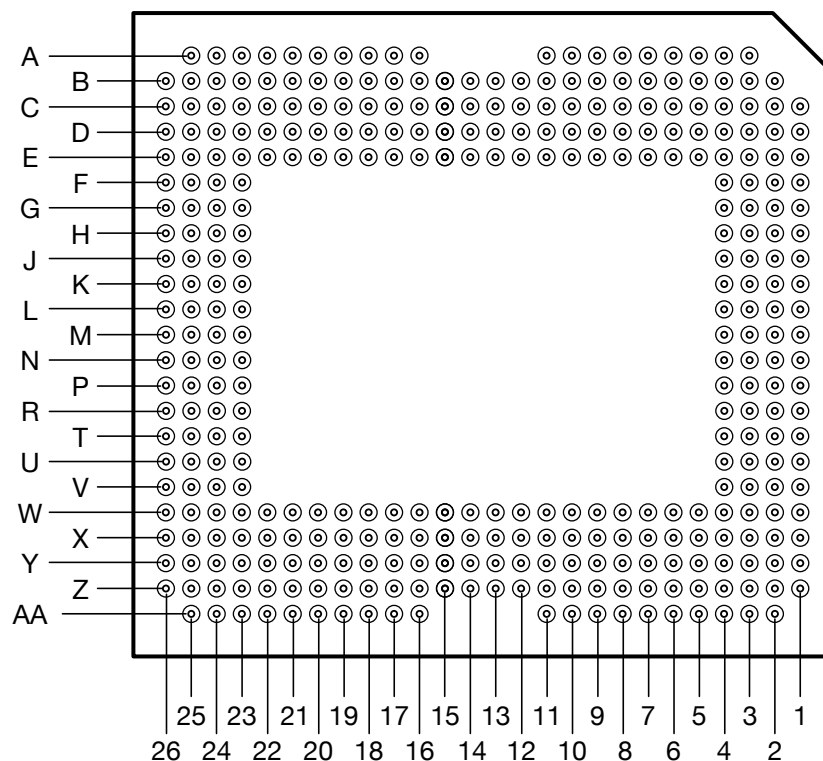


Figure 4-1. FYU Package (350-Pin) Bottom View

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	PIN DESCRIPTION	SIGNAL TYPE	TERMINATION
SIGNAL	PGA_PAD				
LVDS BUS A					
D_AN(0)	E10	I	High-speed differential pair	LVDS	Differential 100Ω
D_AP(0)	E11	I			
D_AN(1)	D6	I	High-speed differential pair		Differential 100Ω
D_AP(1)	C6	I			
D_AN(2)	E3	I	High-speed differential pair		Differential 100Ω
D_AP(2)	D3	I			
D_AN(3)	C7	I	High-speed differential pair		Differential 100Ω
D_AP(3)	C8	I			
D_AN(4)	D8	I	High-speed differential pair		Differential 100Ω
D_AP(4)	D7	I			
D_AN(5)	E6	I	High-speed differential pair		Differential 100Ω
D_AP(5)	E5	I			
D_AN(6)	C5	I	High-speed differential pair		Differential 100Ω
D_AP(6)	C4	I			
D_AN(7)	B8	I	High-speed differential pair		Differential 100Ω
D_AP(7)	B9	I			
D_AN(8)	B6	I	High-speed differential pair		Differential 100Ω
D_AP(8)	B5	I			
D_AN(9)	C10	I	High-speed differential pair		Differential 100Ω
D_AP(9)	B10	I			
D_AN(10)	A9	I	High-speed differential pair		Differential 100Ω
D_AP(10)	A10	I			
D_AN(11)	C13	I	High-speed differential pair		Differential 100Ω
D_AP(11)	C14	I			
D_AN(12)	B12	I	High-speed differential pair		Differential 100Ω
D_AP(12)	B13	I			
D_AN(13)	C17	I	High-speed differential pair		Differential 100Ω
D_AP(13)	C16	I			
D_AN(14)	B15	I	High-speed differential pair		Differential 100Ω
D_AP(14)	B16	I			
D_AN(15)	D15	I	High-speed differential pair		Differential 100Ω
D_AP(15)	E15	I			
DCLK_AN	B3	I	High-speed differential pair		Differential 100Ω
DCLK_AP	C3	I			
SCTRL_AN	E4	I	High-speed differential pair		Differential 100Ω
SCTRL_AP	D4	I			
LVDS BUS B					

Table 4-1. Pin Functions (continued)

PIN		TYPE ⁽¹⁾	PIN DESCRIPTION	SIGNAL TYPE	TERMINATION
SIGNAL	PGA_PAD				
D_BN(0)	W10	I	High-speed differential pair	LVDS	Differential 100Ω
D_BP(0)	W11	I			
D_BN(1)	Z3	I	High-speed differential pair		Differential 100Ω
D_BP(1)	Y3	I			
D_BN(2)	W4	I	High-speed differential pair		Differential 100Ω
D_BP(2)	X4	I			
D_BN(3)	Y7	I	High-speed differential pair		Differential 100Ω
D_BP(3)	Y8	I			
D_BN(4)	X8	I	High-speed differential pair		Differential 100Ω
D_BP(4)	X7	I			
D_BN(5)	Y6	I	High-speed differential pair		Differential 100Ω
D_BP(5)	X6	I			
D_BN(6)	X3	I	High-speed differential pair		Differential 100Ω
D_BP(6)	W3	I			
D_BN(7)	Z8	I	High-speed differential pair		Differential 100Ω
D_BP(7)	Z9	I			
D_BN(8)	Z6	I	High-speed differential pair		Differential 100Ω
D_BP(8)	Z5	I			
D_BN(9)	Y10	I	High-speed differential pair		Differential 100Ω
D_BP(9)	Z10	I			
D_BN(10)	AA9	I	High-speed differential pair		Differential 100Ω
D_BP(10)	AA10	I			
D_BN(11)	Y13	I	High-speed differential pair		Differential 100Ω
D_BP(11)	Y14	I			
D_BN(12)	Z12	I	High-speed differential pair		Differential 100Ω
D_BP(12)	Z13	I			
D_BN(13)	Y17	I	High-speed differential pair		Differential 100Ω
D_BP(13)	Y16	I			
D_BN(14)	Z15	I	High-speed differential pair		Differential 100Ω
D_BP(14)	Z16	I			
D_BN(15)	X15	I	High-speed differential pair		Differential 100Ω
D_BP(15)	W15	I			
DCLK_BN	Y4	I	High-speed differential pair		Differential 100Ω
DCLK_BP	Y5	I			
SCTRL_BN	W5	I	High-speed differential pair		Differential 100Ω
SCTRL_BP	W6	I			
LVDS BUS C					

Table 4-1. Pin Functions (continued)

PIN		TYPE ⁽¹⁾	PIN DESCRIPTION	SIGNAL TYPE	TERMINATION
SIGNAL	PGA_PAD				
D_CN(0)	B18	I	High-speed differential pair	LVDS	Differential 100Ω
D_CP(0)	B19	I			
D_CN(1)	H24	I	High-speed differential pair		Differential 100Ω
D_CP(1)	G24	I			
D_CN(2)	L23	I	High-speed differential pair		Differential 100Ω
D_CP(2)	K23	I			
D_CN(3)	C18	I	High-speed differential pair		Differential 100Ω
D_CP(3)	C19	I			
D_CN(4)	A19	I	High-speed differential pair		Differential 100Ω
D_CP(4)	A20	I			
D_CN(5)	E24	I	High-speed differential pair		Differential 100Ω
D_CP(5)	D24	I			
D_CN(6)	K25	I	High-speed differential pair		Differential 100Ω
D_CP(6)	J25	I			
D_CN(7)	C26	I	High-speed differential pair		Differential 100Ω
D_CP(7)	D26	I			
D_CN(8)	C21	I	High-speed differential pair		Differential 100Ω
D_CP(8)	B21	I			
D_CN(9)	G25	I	High-speed differential pair		Differential 100Ω
D_CP(9)	F25	I			
D_CN(10)	A24	I	High-speed differential pair		Differential 100Ω
D_CP(10)	B24	I			
D_CN(11)	J26	I	High-speed differential pair		Differential 100Ω
D_CP(11)	K26	I			
D_CN(12)	D25	I	High-speed differential pair		Differential 100Ω
D_CP(12)	C25	I			
D_CN(13)	E23	I	High-speed differential pair		Differential 100Ω
D_CP(13)	D23	I			
D_CN(14)	B23	I	High-speed differential pair		Differential 100Ω
D_CP(14)	C23	I			
D_CN(15)	K24	I	High-speed differential pair		Differential 100Ω
D_CP(15)	L24	I			
DCLK_CN	H23	I	High-speed differential pair		Differential 100Ω
DCLK_CP	G23	I			
SCTRL_CN	F26	I	High-speed differential pair		Differential 100Ω
SCTRL_CP	G26	I			
LVDS BUS D					

Table 4-1. Pin Functions (continued)

PIN		TYPE ⁽¹⁾	PIN DESCRIPTION	SIGNAL TYPE	TERMINATION
SIGNAL	PGA_PAD				
D_DN(0)	Z18	I	High-speed differential pair	LVDS	Differential 100Ω
D_DP(0)	Z19	I			
D_DN(1)	T24	I	High-speed differential pair		Differential 100Ω
D_DP(1)	U24	I			
D_DN(2)	N23	I	High-speed differential pair		Differential 100Ω
D_DP(2)	P23	I			
D_DN(3)	Y18	I	High-speed differential pair		Differential 100Ω
D_DP(3)	Y19	I			
D_DN(4)	AA19	I	High-speed differential pair		Differential 100Ω
D_DP(4)	AA20	I			
D_DN(5)	W24	I	High-speed differential pair		Differential 100Ω
D_DP(5)	X24	I			
D_DN(6)	P25	I	High-speed differential pair		Differential 100Ω
D_DP(6)	R25	I			
D_DN(7)	Y26	I	High-speed differential pair		Differential 100Ω
D_DP(7)	X26	I			
D_DN(8)	Y21	I	High-speed differential pair		Differential 100Ω
D_DP(8)	Z21	I			
D_DN(9)	U25	I	High-speed differential pair		Differential 100Ω
D_DP(9)	V25	I			
D_DN(10)	AA24	I	High-speed differential pair		Differential 100Ω
D_DP(10)	Z24	I			
D_DN(11)	R26	I	High-speed differential pair		Differential 100Ω
D_DP(11)	P26	I			
D_DN(12)	X25	I	High-speed differential pair		Differential 100Ω
D_DP(12)	Y25	I			
D_DN(13)	W23	I	High-speed differential pair		Differential 100Ω
D_DP(13)	X23	I			
D_DN(14)	Z23	I	High-speed differential pair		Differential 100Ω
D_DP(14)	Y23	I			
D_DN(15)	P24	I	High-speed differential pair		Differential 100Ω
D_DP(15)	N24	I			
DCLK_DN	T23	I	High-speed differential pair		Differential 100Ω
DCLK_DP	U23	I			
SCTRL_DN	V26	I	High-speed differential pair		Differential 100Ω
SCTRL_DP	U26	I			
SCP INTERFACE					
SCPCLK	U2	I	Serial Communications Port CLK	LVC MOS	Internal pulldown
SCPDI	T3	I	Serial Communications Data In	LVC MOS	Internal pulldown
SCPENZ	U4	I	Serial Communications Port Enable	LVC MOS	Internal pulldown
SCPDO	U3	O	Serial Communications Port Output	LVC MOS	Internal pulldown
OTHER SIGNALS					
DMD_PWRDNZ	G4	I	Chip–Level ResetZ	LVC MOS	Internal pulldown

Table 4-1. Pin Functions (continued)

PIN		TYPE ⁽¹⁾	PIN DESCRIPTION	SIGNAL TYPE	TERMINATION
SIGNAL	PGA_PAD				
N/C	G1, H1, J1, J3, J4, K3, P3, R1, R3, R4, T1, U1, V3, D17, X17, K4, P4, F3, G2, W18, G3, H3, X16	No Connect for Dual DLPC6422 4K System			
N/C	G1, H1, J1, J3, J4, K3, P3, R1, R3, R4, T1, U1, V3, D17, X17, K4, P4, F3, G2, H3, W18, G3, W6, W5, Y5, Y4, W15, X15, Z16, Z15, Y16, Y17, Z13, Z12, Y14, Y13, AA10, AA9, Z10, Y10, Z5, Z6, Z9, Z8, W3, X3, X6, Y6, X7, X8, Y8, Y7, X4, W4, Y3, Z3, W11, W10, D4, E4, C3, B3, E15, D15, B16, B15, C16, C17, B13, B12, C14, C13, A10, A9, B10, C10, B5, B6, B9, B8, C4, C5, E5, E6, D7, D8, C8, C7, D3, E3, C6, D6, E11, E10, X16	No Connect for Single DLPC6422 1080p System			
TEMP_N	W16	I/O			
TEMP_P	W17	I/O			
MICROMIRROR BIAS RESET INPUTS					
MBRST(0)	E14	I	Mirror actuation signal		
MBRST(1)	D13	I	Mirror actuation signal		
MBRST(2)	E13	I	Mirror actuation signal		
MBRST(3)	C12	I	Mirror actuation signal		
MBRST(4)	E12	I	Mirror actuation signal		
MBRST(5)	C11	I	Mirror actuation signal		
MBRST(6)	D16	I	Mirror actuation signal		
MBRST(7)	C15	I	Mirror actuation signal		
MBRST(8)	W14	I	Mirror actuation signal		
MBRST(9)	X13	I	Mirror actuation signal		
MBRST(10)	W13	I	Mirror actuation signal		
MBRST(11)	Y12	I	Mirror actuation signal		
MBRST(12)	W12	I	Mirror actuation signal		
MBRST(13)	Y11	I	Mirror actuation signal		
MBRST(14)	Y15	I	Mirror actuation signal		
POWERS AND GROUNDS					

Table 4-1. Pin Functions (continued)

PIN		TYPE ⁽¹⁾	PIN DESCRIPTION	SIGNAL TYPE	TERMINATION
SIGNAL	PGA_PAD				
VDD	A5, A6, B2, C1, D10, D12, D19, D22, E8, E19, E20, E21, E22, F1, F2, J2, K1, L1, L25, M3, M4, M25, N1, N25, P1, R2, V1, V2, W8, W19, W20, W21, W22, X10, X12, X19, X22, Y1, Z1, Z2, AA2, AA5, AA6	P	Low-voltage CMOS core supply		
VDDI	A7, A8, A11, A16, A17, A18, A21, A22, A23, AA7, AA8, AA11, AA16, AA17, AA18, AA21, AA22, AA23	P	I/O supply		
VCC2	A3, A4, A25, B26, L26, M26, N26, Z26, AA3, AA4, AA25	P	Memory array stepped-up voltage		
VSS	B4, B7, B11, B14, B17, B20, B22, B25, C2, C9, C20, C22, C24, D1, D2, D5, D9, D11, D14, D18, D20, D21, E1, E2, E7, E9, E16, E17, E18, E25, E26, F4, F23, F24, H2, H4, H25, H26, J23, J24, K2, L2, L3, L4, M1, M2, M23, M24, N2, N3, N4, P2, R23, R24, T2, T4, T25, T26, V4, V23, V24, W1, W2, W7, W9, W25, W26, X1, X2, X5, X9, X11, X14, X18, X20, X21, Y2, Y9, Y20, Y22, Y24, Z4, Z7, Z11, Z14, Z17, Z20, Z22, Z25	G	Global ground		

(1) I = Input, O = Output, P = Power, G = Ground, NC = No Connect

5 Specifications

5.1 Absolute Maximum Ratings

Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

		MIN	MAX	UNIT
SUPPLY VOLTAGES				
V_{DD}	Supply voltage for LVCMOS core logic ⁽¹⁾	−0.5	2.3	V
V_{DDI}	Supply voltage for LVDS Interface ⁽¹⁾	−0.5	2.3	V
V_{CC2}	Micromirror Electrode and HVCMOS voltage ^{(1) (2)}	−0.5	11	V
V_{MBRST}	Input voltage for MBRST pins ⁽¹⁾	−17.5	22.5	V
$ V_{DDI} - V_{DD} $	Supply voltage delta (absolute value) ⁽³⁾		0.3	V
INPUT VOLTAGES				
$ V_{ID} $	Input differential voltage for LVDS pins (absolute value)		500	mV
V_{LVCMOS}	Input voltage for all other input pins ⁽¹⁾	−0.3	$V_{DDI} + 0.3$	V
ENVIRONMENTAL				
T_{ARRAY}	Temperature, operating ⁽⁴⁾	0	90	°C
	Temperature, nonoperating ⁽⁴⁾	−40	90	°C
T_{DP}	Dew point temperature, operating and non-operating (noncondensing)		81	°C

- (1) All voltages are referenced to common ground V_{SS} . V_{DD} , V_{DDI} , and V_{CC2} power supplies are all required for all DMD operating modes.
- (2) V_{CC2} supply transients must fall within specified voltages.
- (3) Exceeding the recommended allowable voltage difference between V_{DD} and V_{DDI} may result in excessive current draw.
- (4) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1), shown in [DMD Thermal Test Point](#), using the [Micromirror Array Temperature Calculation](#).

5.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system

		MIN	MAX	UNIT
T_{DMD}	DMD storage temperature	−40	80	°C
T_{DP-AVG}	Average dew point temperature (noncondensing) ⁽¹⁾		28	°C
T_{DP-ELR}	Elevated dew point temperature range (noncondensing) ⁽²⁾	28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range		24	months

- (1) This is the average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
- (2) Exposure to dew point temperatures in the elevated range during storage and operation must be limited to less than a total cumulative time of CT_{ELR} .

5.3 ESD Ratings

SYMBOL	PARAMETER	DESCRIPTION	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±500	V
$V_{(ESD)}$	Electrostatic discharge (MBRST PINS)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±150	V

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

		MIN	NOM	MAX	UNIT
VOLTAGE SUPPLY					
V _{DD}	Supply voltage for LVCMOS core logic ⁽¹⁾	1.65	1.8	1.95	V
V _{DDI}	Supply voltage for LVDS Interface ⁽¹⁾	1.65	1.8	1.95	V
V _{CC2}	Micromirror Electrode and HVCMOS voltage ^{(1) (2)}	9.5	10	10.5	V
V _{MBRST}	Micromirror Bias / Reset Voltage ⁽¹⁾	–17		21.5	V
V _{DD} – V _{DDI}	Supply voltage delta (absolute value) ⁽³⁾		0	0.3	V
LVCMOS					
V _{IH(DC)}	Input High Voltage	0.7 × V _{DD}		V _{DD} + 0.3	V
V _{IL(DC)}	Input Low Voltage	–0.3		0.3 × V _{DD}	V
V _{IH(AC)}	Input High Voltage	0.8 × V _{DD}		V _{DD} + 0.3	V
V _{IL(AC)}	Input Low Voltage	–0.3		0.2 × V _{DD}	V
I _{OH}	High-level Output Current			2	mA
I _{OL}	Low-level Output Current	–2			mA
t _{PWRDNZ}	PWRDNZ pulse width ⁽⁴⁾	10			ns
SCP INTERFACE					
F _{SCPCLK}	SCP clock frequency	50		500	kHz
SCPCLK _{DCDIN}	SCP Clk Input duty cycle	40%		60%	
LVDS INTERFACE					
F _{CLOCK}	Clock frequency for LVDS interface (all channels), DCLK ⁽⁵⁾			400	MHz
DCD _{IN}	Input CLK Duty Cycle Distortion tolerance	44%		56%	
V _{ID}	Input differential voltage (absolute value) ⁽⁶⁾	150	300	440	mV
V _{CM}	Common mode voltage ⁽⁶⁾	1100	1200	1300	mV
V _{LVDS}	LVDS voltage ⁽⁶⁾	880		1520	mV
t _{LVDS_RSTZ}	Time required for LVDS receivers to recover from PWRDNZ	2			μs
Z _{IN}	Internal differential termination resistance	80	100	120	Ω
Z _{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
ENVIRONMENTAL					
T _{ARRAY}	Array temperature, long-term operational ^{(7) (8) (9)}	10		40 to 70 ⁽¹⁰⁾	°C
	Array temperature, short-term operational, 500 hour max ^{(8) (11)}	0		10	°C
T _{DP-AVG}	Average dew point average temperature (non-condensing) ⁽¹²⁾			28	°C
T _{DP-ELR}	Elevated dew point temperature range (non-condensing) ⁽¹³⁾	28		36	°C
CT _{ELR}	Cumulative time in elevated dew point temperature range			24	Months
Q _{AP-ILL}	Window aperture illumination overfill ^{(14) (15) (16)}			17	W/cm ²
SOLID STATE ILLUMINATION					
ILL _{UV4}	Illumination power at wavelengths < 365nm ^{(7) (17) (18)}			10	mW/cm ²
ILL _{UV3}	Illumination power at wavelengths ≥ 365nm and ≤ 385nm ^{(7) (17) (18)}			2	W/cm ²
ILL _{UV2}	Illumination power at wavelengths ≥ 385nm and ≤ 400nm ^{(7) (17) (18)}			5	W/cm ²
ILL _{UV1}	Illumination power at wavelengths ≥ 400nm < 410nm ^{(7) (17) (18)}			12	W/cm ²
ILL _{UV}	Illumination power at wavelengths ≥ 365nm and ≤ 410nm ^{(7) (17) (18)}			12	W/cm ²
ILL _{BLU}	Illumination power at wavelengths ≥ 410nm and ≤ 475nm ^{(17) (18)}			12.8	W/cm ²

5.4 Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

		MIN	NOM	MAX	UNIT
ILL _{VIS}	Illumination power at wavelengths $\geq 410\text{nm}$ and $\leq 800\text{nm}$ ⁽¹⁷⁾ ⁽¹⁸⁾			22	W/cm ²

- (1) All voltages are referenced to common ground V_{SS} . V_{DD} , V_{DDI} , and V_{CC2} power supplies are all required for proper DMD operation. V_{SS} must also be connected.
- (2) V_{CC2} supply transients must fall within specified max voltages.
- (3) To prevent excess current, the supply voltage delta $|V_{DDI} - V_{DD}|$ must be less than the specified limit. See the [DMD Power Supply Requirements](#).
- (4) PWRDNZ input pin resets the SCP and disables the LVDS receivers. The PWRDNZ input pin overrides the SCPENZ input pin and tristates the SCPDO output pin.
- (5) See LVDS clock timing requirements in [Timing Requirements](#).
- (6) See [Figure 5-5](#) for the LVDS waveform requirements.
- (7) Simultaneous exposure of the DMD to the maximum [Recommend Operating Conditions](#) for temperature and UV illumination reduces device lifetime.
- (8) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1), shown in [Figure 6-3](#) using the [Micromirror Array Temperature Calculation](#).
- (9) Long-term is defined as the usable life of the device.
- (10) Per [Figure 5-1](#), the maximum operational array temperature is derated based on the micromirror landed duty cycle that the DMD experiences in the end application. See [Micromirror Landed-on/Landed-off Duty Cycle](#) for a definition of micromirror landed duty cycle.
- (11) Short-term is the total cumulative time over the useful life of the device.
- (12) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
- (13) Exposure to dew point temperatures in the elevated range during storage and operation is limited to less than a total cumulative time of CT_{ELR} .
- (14) Applies to region defined in [Figure 5-2](#)
- (15) The active area of the DMD is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. Minimizing the light flux incident outside the active array is a design requirement of the illumination optical system. Depending on the particular optical architecture and assembly tolerances of the optical system, the amount of overfill light on the outside of the active array may cause system performance degradation.
- (16) To calculate, see [Window Aperture Illumination Overfill Calculation](#).
- (17) The maximum allowable optical power incident on the DMD is limited by the maximum optical power density for each wavelength range specified and the micromirror array temperature (T_{ARRAY}).
- (18) To calculate, see [Micromirror Power Density Calculation](#).

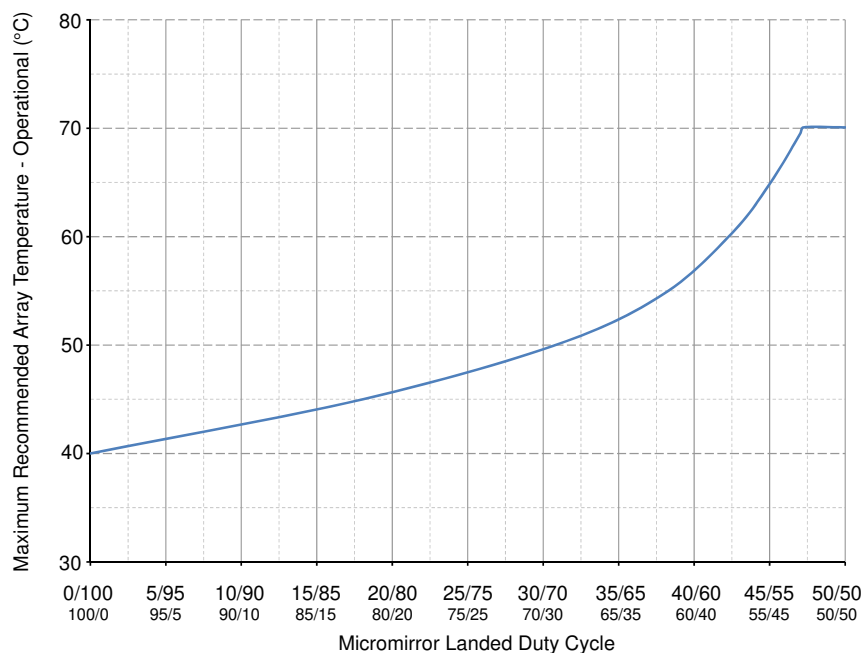


Figure 5-1. Maximum Recommended Array Temperature—Derating Curve

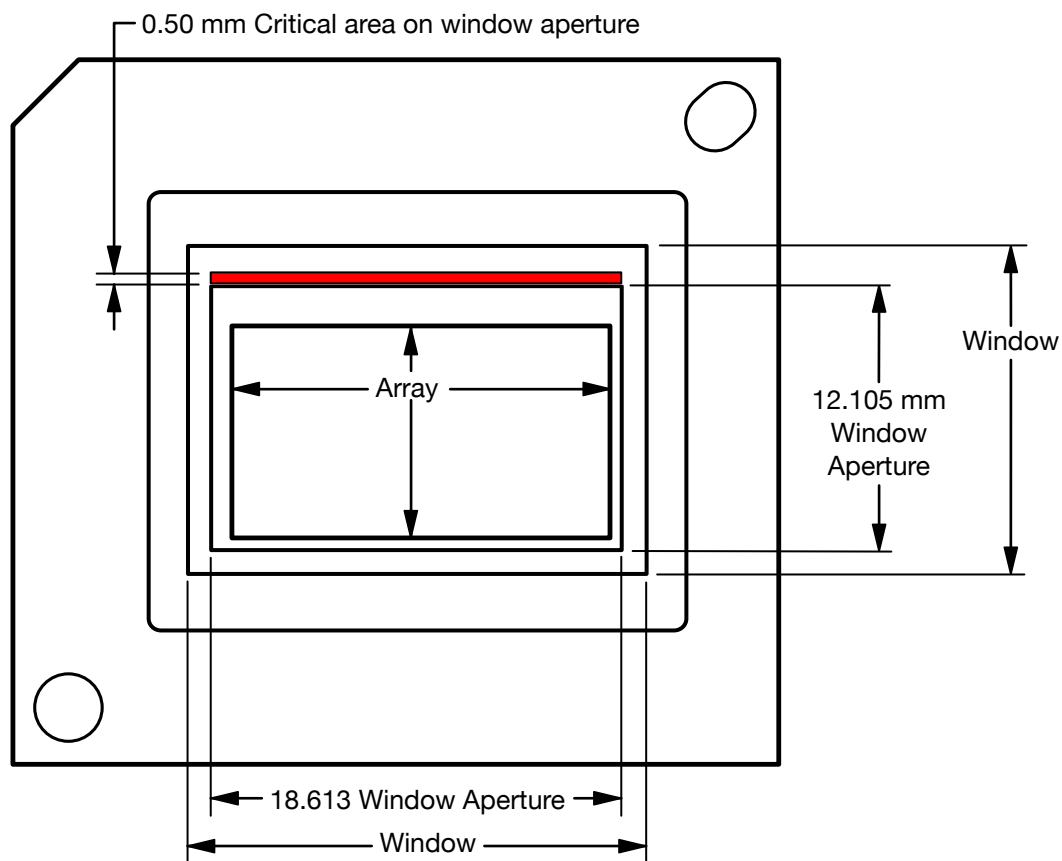


Figure 5-2. Illumination Overfill Diagram—Critical Area

5.5 Thermal Information

THERMAL METRIC	DLP78TUV	UNIT
	FYU	
	350 PINS	
Thermal resistance, active area to test point 1 (TP1) ⁽¹⁾	0.55	°C/W

- (1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the DMD within the temperature range specified in the [Recommended operating conditions](#). The total heat load on the DMD is largely driven by the incident light absorbed by the active area, although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Minimizing the light energy falling outside the window clear aperture is a design requirement of the optical system because any additional thermal load in this area can significantly degrade the reliability of the device.

5.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Information (1080p)						
I _{DD}	Supply current V _{DD} ⁽¹⁾				800	mA
I _{DDI}	Supply current V _{DDI} ⁽¹⁾				170	mA
I _{CC2}	Supply current V _{CC2}				40	mA
P _{DD}	Supply power V _{DD} ⁽¹⁾				1560	mW
P _{DDI}	Supply power V _{DDI} ⁽¹⁾				332	mW
P _{CC2}	Supply power V _{CC2} ⁽¹⁾				420	mW
Power Supply Information (4K)						
I _{DD}	Supply current V _{DD} ⁽¹⁾				1200	mA
I _{DDI}	Supply current V _{DDI} ⁽¹⁾				340	mA
I _{CC2}	Supply current V _{CC2}				40	mA
P _{DD}	Supply power V _{DD} ⁽¹⁾				2340	mW
P _{DDI}	Supply power V _{DDI} ⁽¹⁾				663	mW
P _{CC2}	Supply power V _{CC2} ⁽¹⁾				420	mW
LVCMOS						
V _{OH}	High-level output voltage	I _{OH} = 2mA	0.8			× V _{DD}
V _{OL}	Low-level output voltage	I _{OL} = 2mA			0.2	× V _{DD}
I _{OZ}	High impedance output current	V _{DD} = 1.95V			10	μA
I _{IL}	Low-level input current	V _{DD} = 1.95V, V _{in} = 0V	–60			μA
I _{IH}	High-level input current ⁽²⁾	V _{DD} = 1.95V, V _{in} = V _{DD}			200	μA
Capacitances						
C _I	Input capacitance: LVDS pins	f = 1MHz			20	pF
C _I	Input capacitance ⁽²⁾	f = 1MHz			15	pF
C _O	Output capacitance ⁽²⁾	f = 1MHz			15	pF
C _{IM}	Input capacitance for MBRST[0:14] pins	f = 75kHz	360	410	520	pF

- (1) To prevent excess current, the supply voltage delta |V_{DDI} – V_{DD}| must be less than the specified limit in [Absolute Maximum Ratings](#).
(2) Applies to LVCMOS pins only. Excludes LVDS pins and test pad pins

5.7 Timing Requirements

Over [Recommended Operating Conditions](#) (unless otherwise noted)

PARAMETER DESCRIPTION	MIN	NOM	MAX	UNIT
SCP				

5.7 Timing Requirements (continued)

Over *Recommended Operating Conditions* (unless otherwise noted)

PARAMETER DESCRIPTION		MIN	NOM	MAX	UNIT
t _{SCP_DS}	SCPD clock setup time (before SCPCLK falling-edge) ⁽¹⁾	800			ns
t _{SCP_DH}	SCPD hold time (after SCPCLK falling-edge) ⁽¹⁾	900			ns
t _{SCP_NEG_ENZ}	Time between falling edge of SCPENZ and the rising edge of SCPCLK ⁽¹⁾	1			μs
t _{SCP_POS_ENZ}	Time between falling edge of SCPCLK and the rising edge of SCPENZ ⁽¹⁾	1			μs
t _{SCP_OUT_EN}	Time required for SCP output buffer to recover after SCPENZ (from tri-state). ⁽¹⁾			960	ns
t _{SCP_PW_ENZ}	SCPENZ inactive pulse width (high-level)	1			1/F _{scpclk}
t _r	Rise time (20% to 80%). See ⁽²⁾			200	ns
t _f	Fall time (80% to 20%). See ⁽²⁾			200	ns
LVDS					
t _{R_LVDS}	Rise time (20% to 80%). See ⁽³⁾			500	ps
t _{F_LVDS}	Fall time (80% to 20%). See ⁽³⁾			500	ps
t _C	Clock Cycle Duration for DCLK_C and DCLK_D ⁽⁴⁾	2.5			ns
t _W	Pulse Duration for DCLK_C/D ⁽⁴⁾	1.19			ns
t _{SU_data}	Setup Time for High-speed data(15:0) before DCLK ⁽⁴⁾	350			ps
t _{SU_sctrl}	Setup Time for SCTRL before DCLK ⁽⁴⁾	330			ps
t _{H_data}	Hold time for High-speed data(15:0) after DCLK ⁽⁴⁾	150			ps
t _{H_sctrl}	Hold Time for SCTRL after DCLK ⁽⁴⁾	170			ps
t _{SKEW_A2B}	Skew tolerance between Channel B and Channel A ^{(6) (7) (8)}	-1.25		1.25	ns
t _{SKEW_C2D}	Skew tolerance between Channel C and Channel D ^{(5) (9) (10)}	-1.25		1.25	ns

(1) See Figure 5-3.

(2) See Figure 5-4.

(3) See Figure 5-6.

(4) See Figure 5-7.

(5) See Figure 5-8.

(6) See Figure 5-8.

(7) Channel A (Bus A) includes the following LVDS pairs: DCLK_A, SCTRL_A, and D_A.

(8) Channel B (Bus B) includes the following LVDS pairs: DCLK_B, SCTRL_B, and D_B.

(9) Channel C (Bus C) includes the following LVDS pairs: DCLK_C, SCTRL_C, and D_C.

(10) Channel D (Bus D) includes the following LVDS pairs: DCLK_D, SCTRL_D, and D_D.

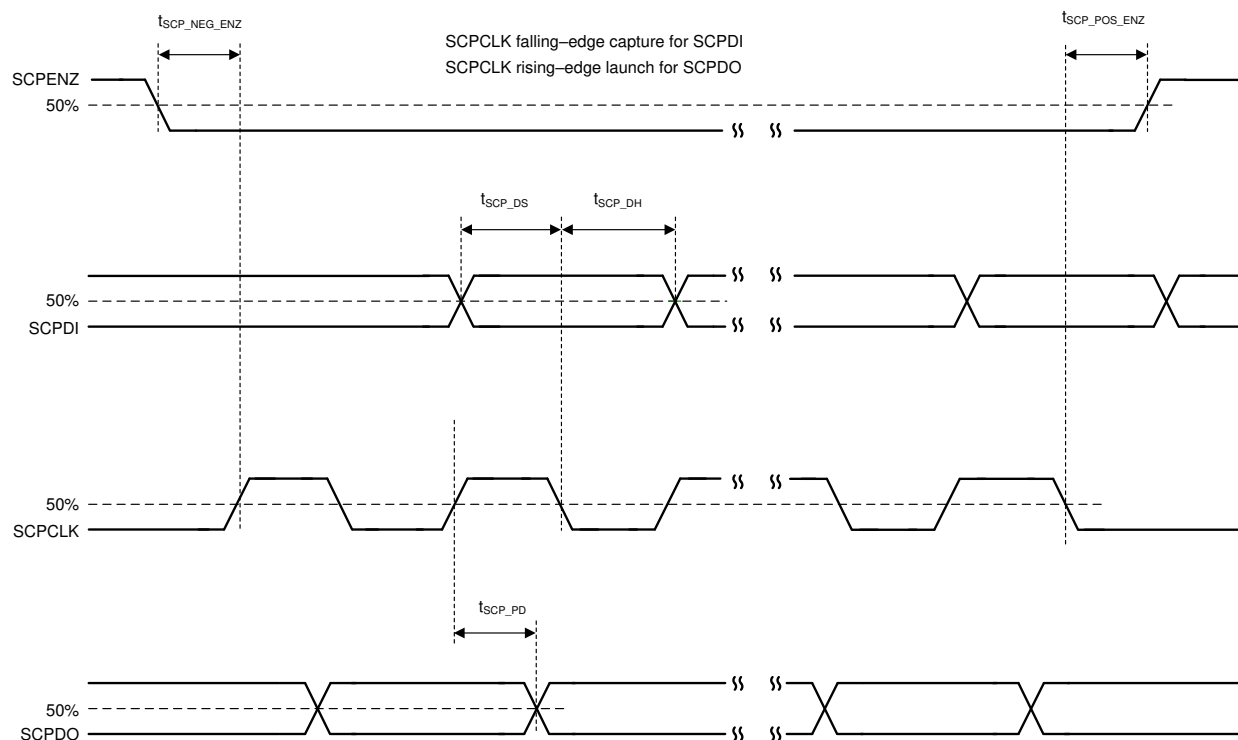


Figure 5-3. SCP Timing Parameters

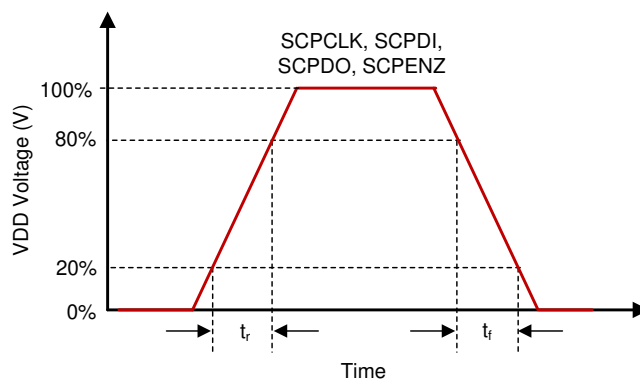


Figure 5-4. SCP Rise and Fall Times

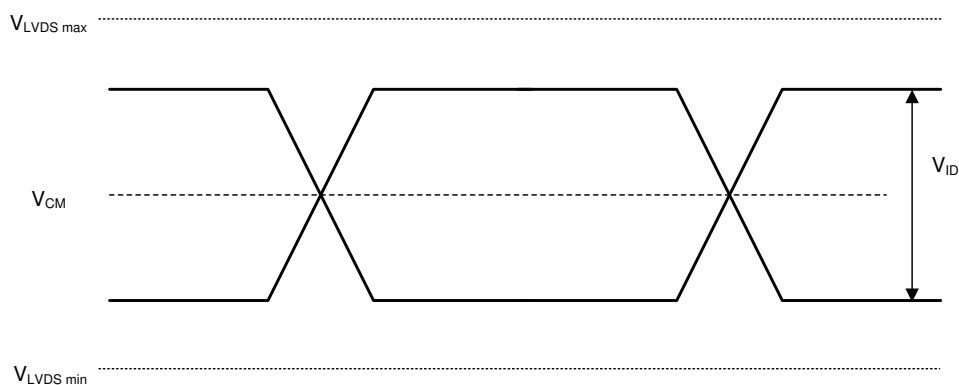


Figure 5-5. LVDS Waveform Parameters

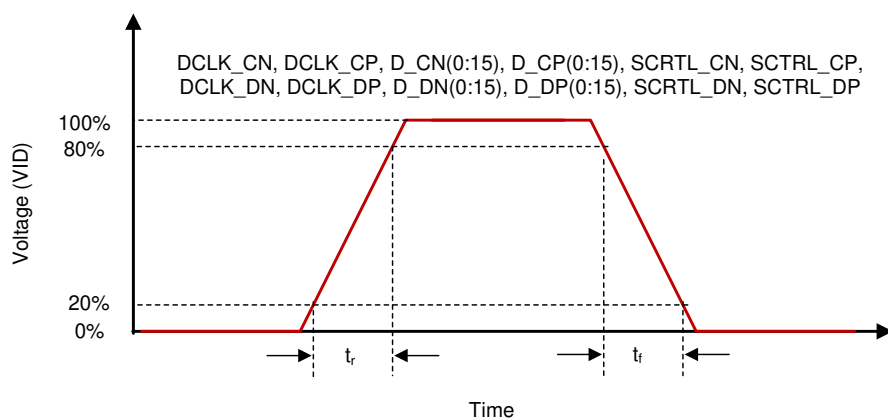


Figure 5-6. LVDS Rise and Fall Times

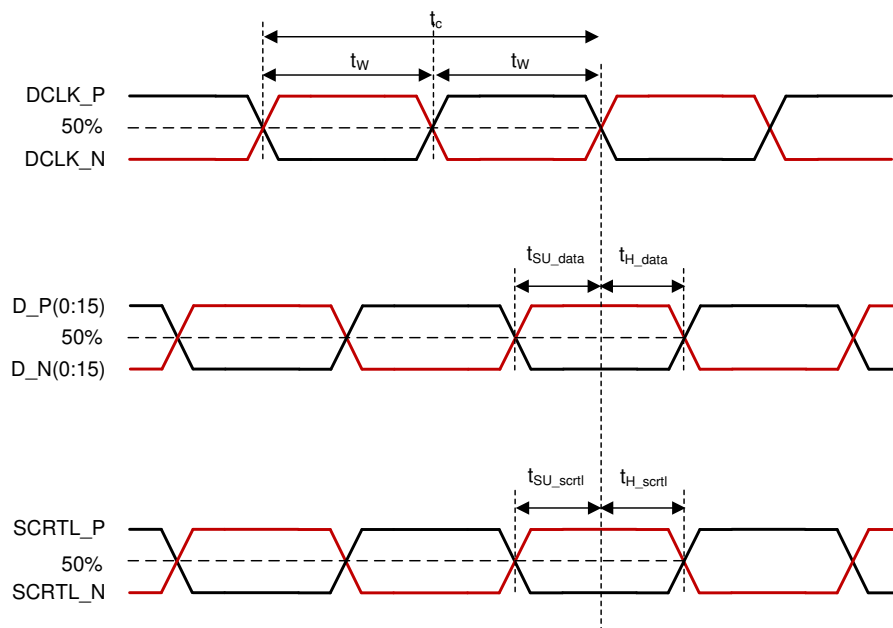


Figure 5-7. LVDS Timing Parameters

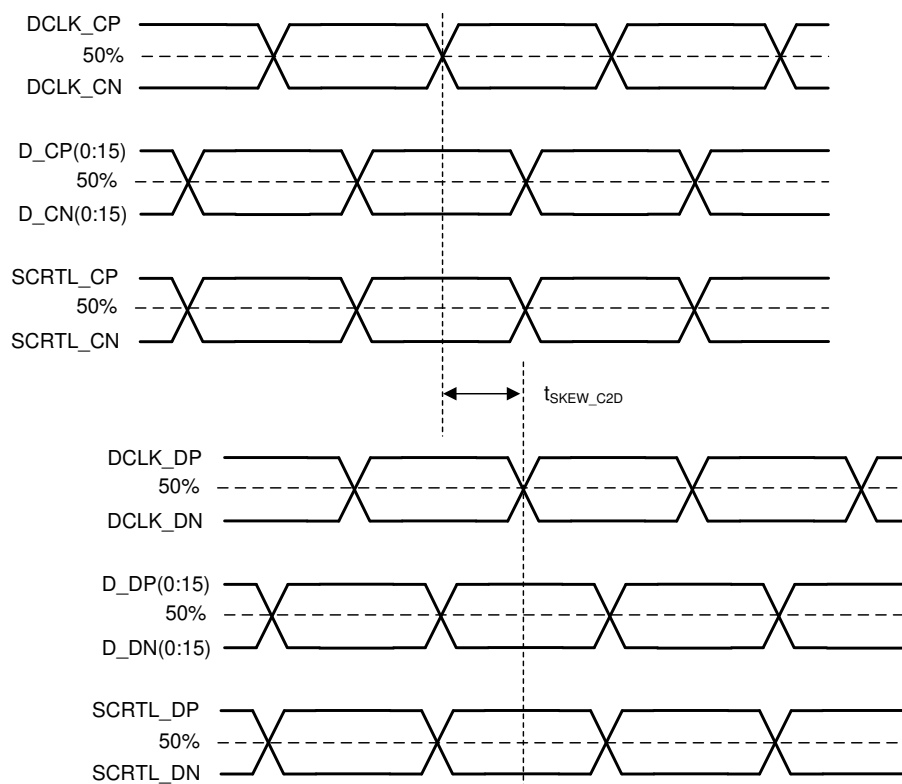


Figure 5-8. LVDS Skew Parameters

5.8 System Mounting Interface Loads

PARAMETER	MIN	NOM	MAX	UNIT
When loads are applied on both electrical and thermal interface areas				
Maximum load to be applied to the electrical interface area ⁽¹⁾			111	N
Maximum load to be applied to the thermal interface area ⁽¹⁾			111	N
When load is applied on the electrical interface area only				
Maximum load to be applied to the electrical interface area ⁽¹⁾			222	N
Maximum load to be applied to the thermal interface area ⁽¹⁾			0	N

(1) The load must be uniformly applied in the corresponding areas shown in [Figure 5-9](#).

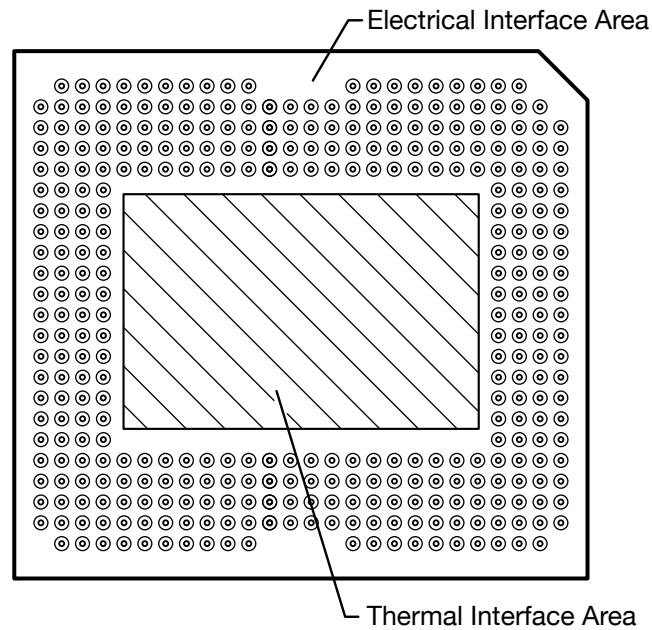


Figure 5-9. System Mounting Interface Loads

5.9 Micromirror Array Physical Characteristics

PARAMETER DESCRIPTION		VALUE	UNIT
M	Number of active columns ⁽¹⁾	1920	micromirrors
N	Number of active rows ⁽¹⁾	1080	micromirrors
P	Micromirror (pixel) pitch ⁽¹⁾	9.0	μm
Micromirror active array width ⁽¹⁾	Micromirror pitch x number of active columns	17.280	mm
Micromirror active array height ⁽¹⁾	Micromirror pitch x number of active rows	9.720	mm
Micromirror active border (top and bottom) ⁽²⁾	Pond of micromirror (POM)	12	micromirrors/side
Micromirror active border (right and left) ⁽²⁾	Pond of micromirror (POM)	12	micromirrors/side

(1) See Figure 5-10.

(2) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.

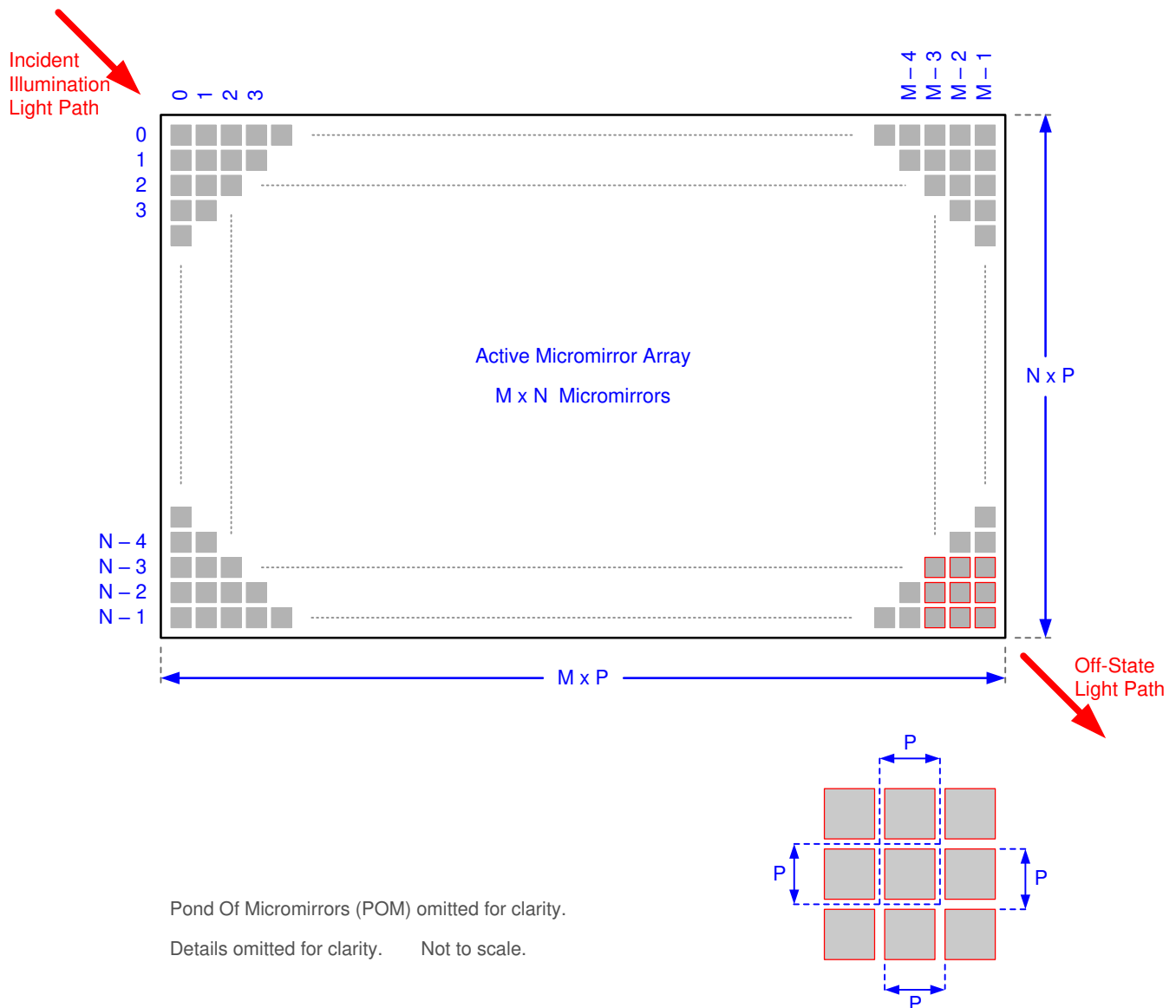


Figure 5-10. Micromirror Array Physical Characteristics

5.10 Micromirror Array Optical Characteristics

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Micromirror tilt angle ^{(2) (3) (4) (5)}		Landed state ⁽¹⁾	13.5	14.5	15.5	degrees
Image performance ⁽⁶⁾	Bright pixel(s) in active area ⁽⁷⁾	Gray 10 screen ⁽¹⁰⁾			0	micromirrors
	Bright pixel(s) in the POM ^{(7) (9)}	Gray 10 screen ⁽¹⁰⁾			1	
	Dark pixel(s) in the active area ⁽⁸⁾	White screen ⁽¹¹⁾			4	
	Adjacent pixel(s) ⁽¹⁶⁾	Any screen			0	
	Unstable pixel(s) in active area ⁽¹³⁾	Any screen			0	

- (1) Measured relative to the plane formed by the overall micromirror array.
- (2) Additional variation exists between the micromirror array and the package datums.
- (3) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
- (4) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations or system contrast variations.
- (5) Refer to [Figure 5-11](#).
- (6) Conditions of Acceptance: all DMD image performance returns are evaluated using the following projected image test conditions:
 - Test set degamma shall be linear.
 - Test set brightness and contrast shall be set to nominal.
 - The diagonal size of the projected image shall be a minimum of 60 inches.
 - The projections screen shall be 1× gain.
 - The projected image shall be inspected from an 8-foot minimum viewing distance.
 - The image shall be in focus during all image performance tests.
- (7) Bright pixel definition: a single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels
- (8) Dark pixel definition: a single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels
- (9) POM definition: rectangular border of off-state mirrors surrounding the active area
- (10) Gray 10 screen definition: a full screen with RGB values set to R = 10/255, G = 10/255, B = 10/255
- (11) White screen definition: a full screen with RGB values set to R=255/255, G = 255/255, B = 255/255
- (12) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point, also referred to as a cluster.
- (13) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image.

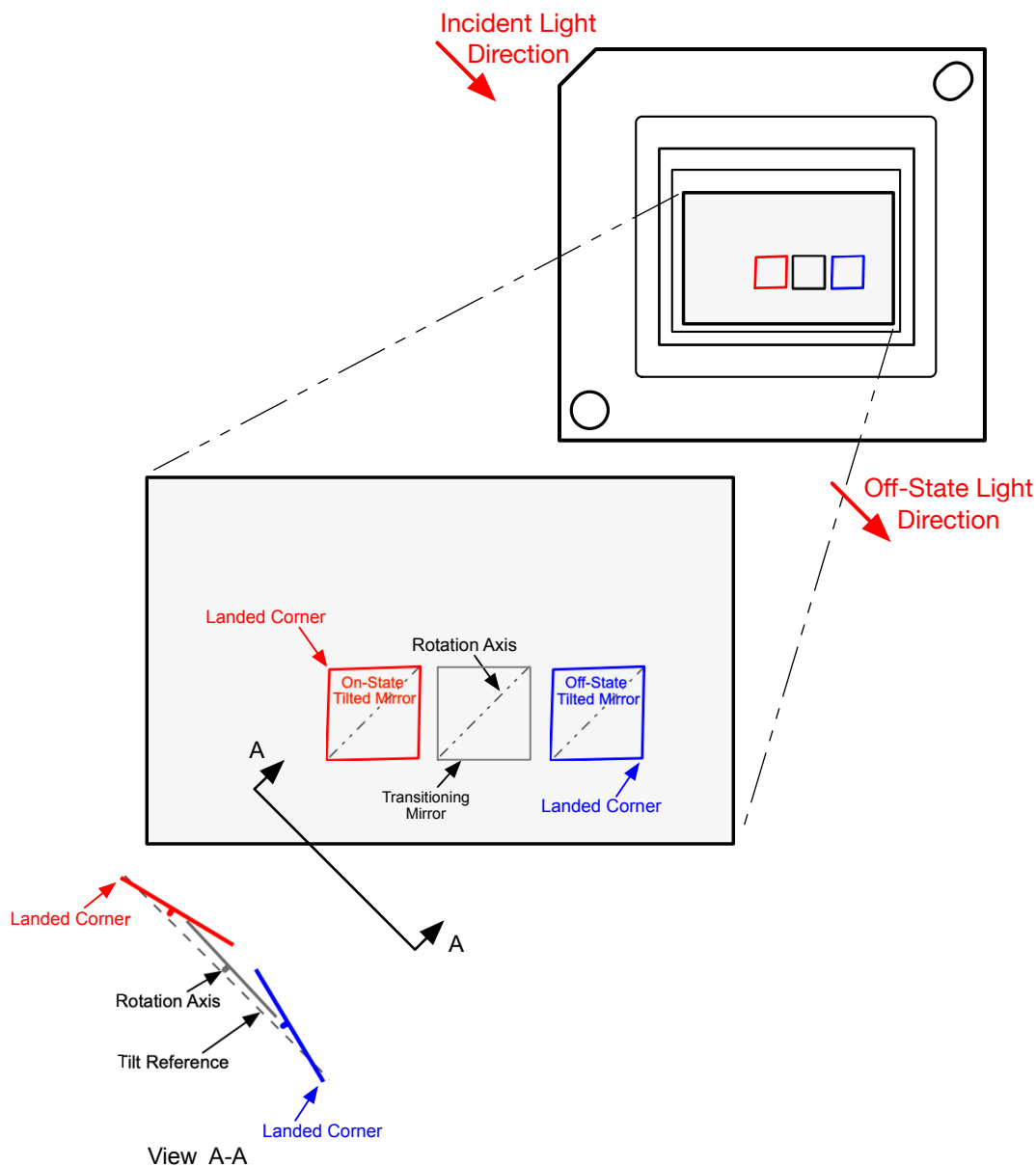


Figure 5-11. Micromirror Landed Orientation and Tilt

5.11 Window Characteristics

PARAMETER DESCRIPTION	Test Conditions	MIN	NOM	MAX	UNIT
Window Material		Corning EagleXG			
Window Refractive Index	546.1nm		1.5119		

5.12 Chipset Component Usage Specification

Reliable function and operation of the DLP78TUV DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD

control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

Note

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

6 Detailed Description

6.1 Overview

The DLP78TUV DMD is a 0.78-inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-optical-electrical-mechanical system (MOEMS). The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables the micromirror array to display a full 3840 × 2160 pixel image at a 60Hz frame rate. The electrical interface is a low voltage differential signaling (LVDS) interface. The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to the [Section 6.2](#). The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

The DLP 0.78-inch UV chipset is comprised of the DLP78TUV DMD, two or one DLPC6422 light controllers , the DLPA300 micromirror driver and the [DLPA100](#) power management and motor driver. For reliable operation, the DLP78TUV DMD must always be used with the DLPC6422 light controller and the power and motor driver specified in the chipset.

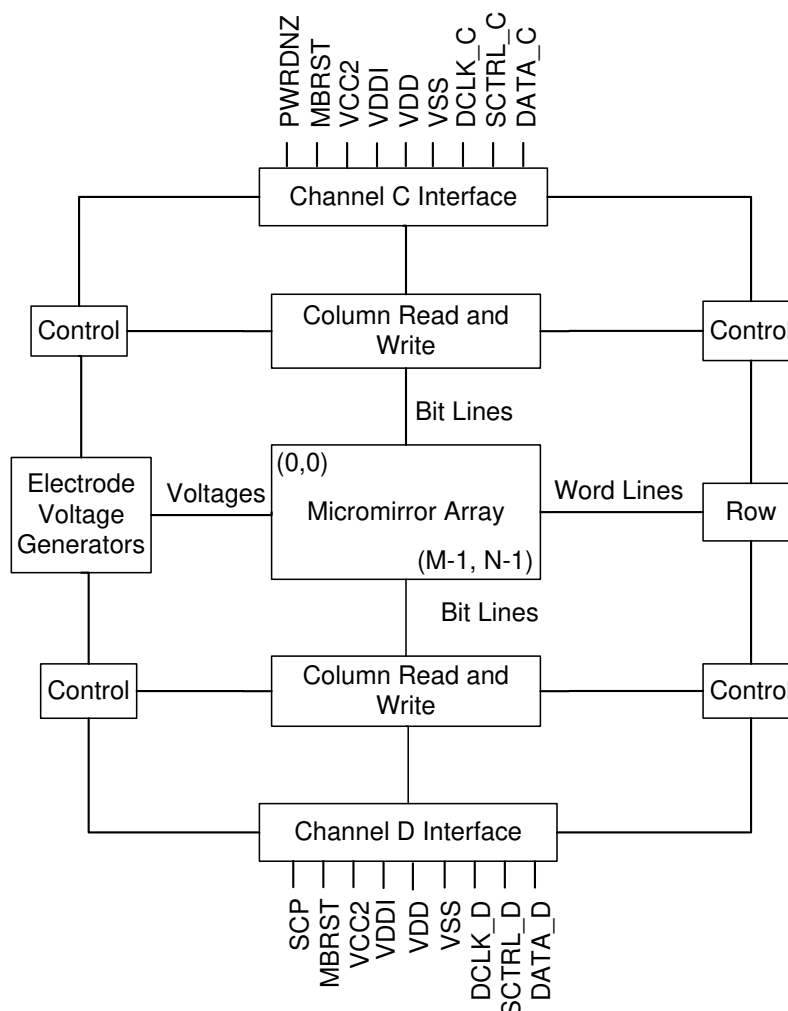


Figure 6-1. Functional Block Diagram for 1080p Single controller Syestem

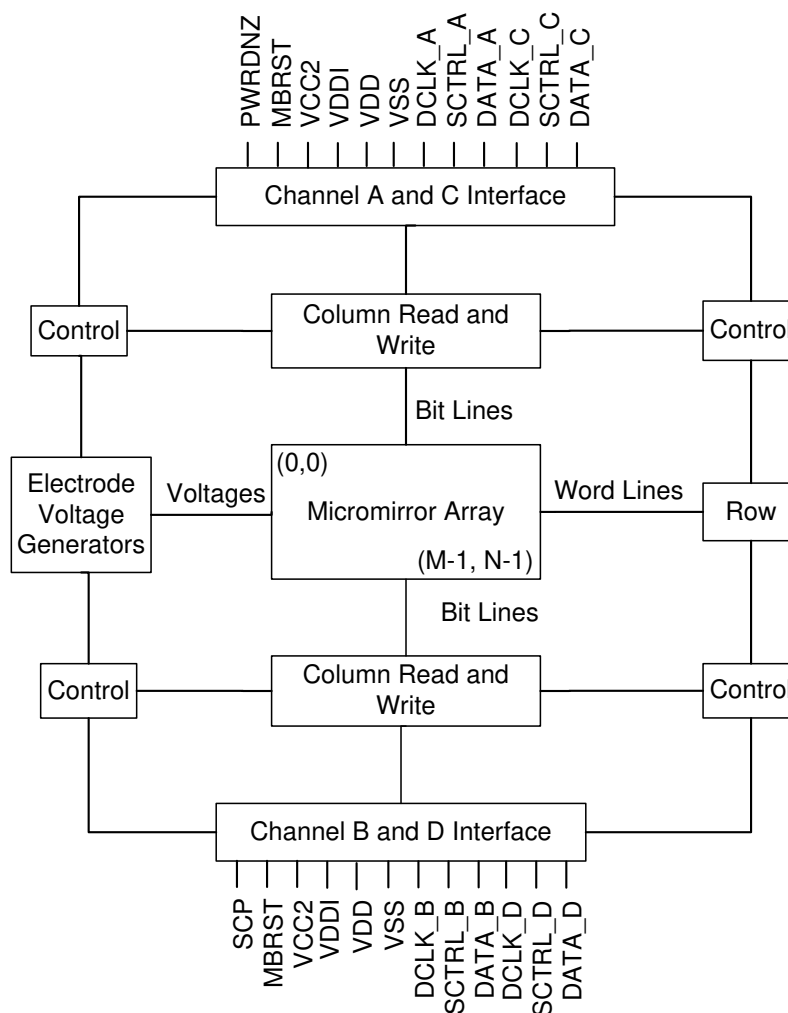


Figure 6-2. Functional Block Diagram for 4K Dual Controller System

6.3 Feature Description

6.3.1 Power Interface

The DMD requires two DC voltages: 1.8-V source for VDD and VDDI, and a 10-V supply for VCC2. In a typical configuration, 3.3V is created by the [DLPA100](#) power management and motor driver and is used on the DMD board to create the 1.8V. The [DLPA300](#) micromirror driver takes in 12V and creates the micromirror reset voltages.

6.3.2 Timing

The data sheet specifies timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be considered. Timing reference loads are not intended to be precise representations of any particular system environment or depiction of the actual load presented by a production test. TI recommends that system designers use IBIS or other simulation tools to correlate the timing reference load to a system environment. Use the specified load capacitance value for characterization and measurement of AC timing signals only. This load capacitance value does not indicate the maximum load the device is capable of driving.

6.4 Device Functional Modes

DMD functional modes are controlled by the DLPC6422 light controller. See the DLPC6422 light controller data sheet or contact a TI applications engineer.

6.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

6.5.1 Numerical Aperture and Stray Light Control

TI recommends that the light cone angle defined by the numerical aperture of the illumination optics is the same as the light cone angle defined by the numerical aperture of the projection optics. This angle must not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and projection pupils to block out flat-state and stray light from the projection lens. The DLP78TUV has a 14.5° tilt angle which corresponds to the f/2.0 numerical aperture. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than 2° larger than the illumination numerical aperture angle (and vice versa), contrast degradation and objectionable artifacts in the display border or active area are possible.

6.5.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display border and active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

6.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. Design the illumination optical system to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system optical architecture, the overfill light on the window aperture may have to be further reduced below the suggested maximum 10% level in order to be acceptable.

6.6 Micromirror Array Temperature Calculation

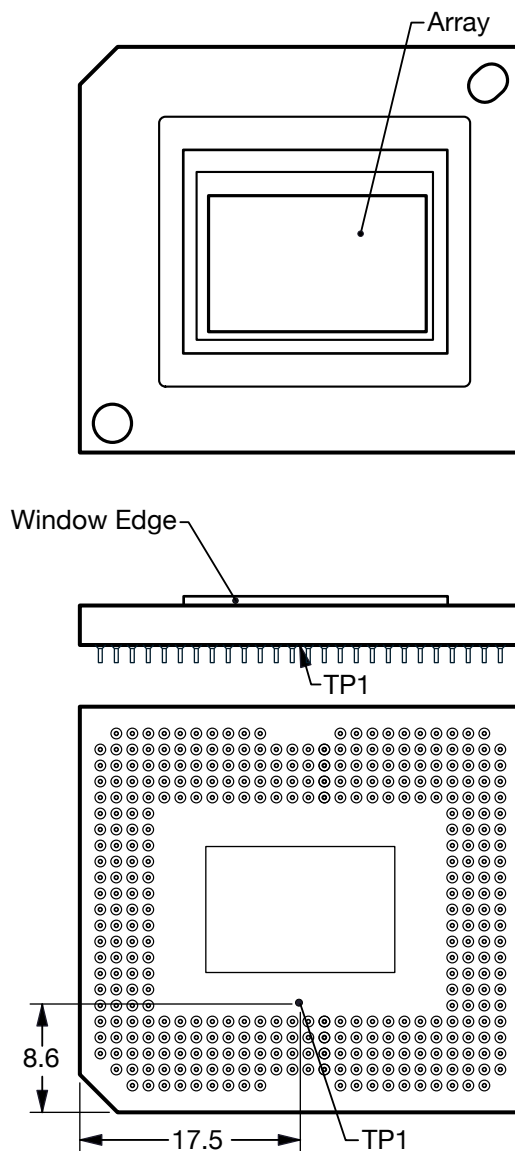


Figure 6-3. DMD Thermal Test Point

Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from a measurement point on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The following equations show the relationship between array temperature and the reference ceramic temperature, thermal test TP1, shown above:

$$T_{\text{ARRAY}} = T_{\text{CERAMIC}} + (Q_{\text{ARRAY}} \times R_{\text{ARRAY-TO-CERAMIC}}) \quad (1)$$

$$Q_{\text{ARRAY}} = Q_{\text{ELECTRICAL}} + Q_{\text{ILLUMINATION}} \quad (2)$$

where

- T_{ARRAY} = Computed array temperature (°C)
- T_{CERAMIC} = Measured ceramic temperature (°C) (TP1 location)

- $R_{\text{ARRAY-TO-CERAMIC}}$ = Thermal resistance of package specified in [Section 5.5](#) from array to ceramic TP1 ($^{\circ}\text{C}/\text{Watt}$)
- Q_{ARRAY} = Total DMD power on the array (W) (electrical + absorbed)
- $Q_{\text{ELECTRICAL}}$ = Nominal electrical power (W)
- Q_{INCIDENT} = Incident illumination optical power (W)
- $Q_{\text{ILLUMINATION}}$ = (DMD average thermal absorptivity $\times Q_{\text{INCIDENT}}$) (W)
- DMD average thermal absorptivity = 0.55

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 1.4W. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a single chip or multichip DMD system. It assumes an illumination distribution of 83.7% on the active array, and 16.3% on the array border.

The sample calculation for a typical projection application is as follows:

$$Q_{\text{INCIDENT}} = 23.8\text{W (measured)} \quad (3)$$

$$T_{\text{CERAMIC}} = 55.0^{\circ}\text{C (measured)} \quad (4)$$

$$Q_{\text{ELECTRICAL}} = 1.4\text{W} \quad (5)$$

$$Q_{\text{ARRAY}} = 1.4\text{W} + (0.55 \times 23.8\text{W}) = 14.49\text{W} \quad (6)$$

$$T_{\text{ARRAY}} = 55.0^{\circ}\text{C} + (14.49\text{W} \times 0.55^{\circ}\text{C/W}) = 63^{\circ}\text{C} \quad (7)$$

6.7 Micromirror Power Density Calculation

The calculation of the optical power density of the illumination on the DMD in the different wavelength bands uses the total measured optical power on the DMD, percent illumination overfill, area of the active array, and ratio of the spectrum in the wavelength band of interest to the total spectral optical power.

- $ILL_{\text{UV4}} = [OP_{\text{UV4-RATIO}} \times Q_{\text{INCIDENT}}] \times 1000 \text{ (mW/W)} \div A_{\text{ILL}} \text{ (mW/cm}^2\text{)}$
- $ILL_{\text{UV3}} = [OP_{\text{UV3-RATIO}} \times Q_{\text{INCIDENT}}] \div A_{\text{ILL}} \text{ (W/cm}^2\text{)}$
- $ILL_{\text{UV2}} = [OP_{\text{UV2-RATIO}} \times Q_{\text{INCIDENT}}] \div A_{\text{ILL}} \text{ (W/cm}^2\text{)}$
- $ILL_{\text{UV1}} = [OP_{\text{UV1-RATIO}} \times Q_{\text{INCIDENT}}] \div A_{\text{ILL}} \text{ (W/cm}^2\text{)}$
- $ILL_{\text{UV}} = [OP_{\text{UV-RATIO}} \times Q_{\text{INCIDENT}}] \div A_{\text{ILL}} \text{ (W/cm}^2\text{)}$
- $ILL_{\text{VIS}} = [OP_{\text{VIS-RATIO}} \times Q_{\text{INCIDENT}}] \div A_{\text{ILL}} \text{ (W/cm}^2\text{)}$
- $A_{\text{ILL}} = A_{\text{ARRAY}} \div (1 - OV_{\text{ILL}}) \text{ (cm}^2\text{)}$

where:

- ILL_{UV4} = UV4 illumination power density on the DMD (mW/cm^2)
- ILL_{UV3} = UV3 illumination power density on the DMD (W/cm^2)
- ILL_{UV2} = UV2 illumination power density on the DMD (W/cm^2)
- ILL_{UV1} = UV1 illumination power density on the DMD (W/cm^2)
- ILL_{UV} = UV illumination power density on the DMD (W/cm^2)
- ILL_{VIS} = VIS illumination power density on the DMD (W/cm^2)
- A_{ILL} = illumination area on the DMD (cm^2)
- Q_{INCIDENT} = total incident optical power on DMD (W) (measured)
- A_{ARRAY} = area of the array (cm^2) (data sheet)
- OV_{ILL} = percent of total illumination on the DMD outside the array (%) (optical model)
- $OP_{\text{UV4-RATIO}}$ = ratio of the optical power for wavelengths $<365\text{nm}$ to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{\text{UV3-RATIO}}$ = ratio of the optical power for wavelengths $\geq 365\text{nm}$ and $<385\text{nm}$ to the total optical power in the illumination spectrum (spectral measurement)

- $OP_{UV2-RATIO}$ = ratio of the optical power for wavelengths $\geq 385\text{nm}$ and $< 400\text{nm}$ to the total optical power in the illumination spectrum (spectral measurement)
 $OP_{UV1-RATIO}$ = ratio of the optical power for wavelengths $\geq 400\text{nm}$ and $< 410\text{nm}$ to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{UV-RATIO}$ = ratio of the optical power for wavelengths $\geq 365\text{nm}$ and $< 410\text{nm}$ to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{VIS-RATIO}$ = ratio of the optical power for wavelengths ≥ 410 and $\leq 800\text{nm}$ to the total optical power in the illumination spectrum (spectral measurement)

The illumination area varies and depends on the illumination overfill. The total illumination area on the DMD is the array area and overfill area around the array. The optical model is used to determine the percent of the total illumination on the DMD that is outside the array (OV_{ILL}) and the percent of the total illumination that is on the active array. From these values the illumination area (A_{ILL}) is calculated. The illumination is assumed to be uniform across the entire array.

From the measured illumination spectrum, the ratio of the optical power in the wavelength bands of interest to the total optical power is calculated.

Sample calculation — Illumination 405nm

$$Q_{INCIDENT} = 23.8\text{W (measured)} \quad (8)$$

$$A_{ARRAY} = (17.280\text{mm} \times 9.72\text{mm}) \div 100 = 1.6796\text{cm}^2 \text{ (data sheet)} \quad (9)$$

$$OV_{ILL} = 16.3\% \text{ (optical model)} \quad (10)$$

$$OP_{UV1-RATIO} = 0.99876 \text{ (spectral measurement)} \quad (11)$$

$$OP_{UV2-RATIO} = 0.00062 \text{ (spectral measurement)} \quad (12)$$

$$A_{ILL} = 1.6796\text{cm}^2 \div (1 - 0.163) = 2.0067\text{cm}^2 \quad (13)$$

$$ILL_{UV1} = [0.99876 \times 23.8\text{W}] \div 2.0067\text{cm}^2 = 11.85 \text{ W/cm}^2 \quad (14)$$

$$ILL_{UV2} = [0.00062 \times 23.8\text{W}] \div 2.0067\text{cm}^2 = 0.0074 \text{ W/cm}^2 \quad (15)$$

6.8 Window Aperture Illumination Overfill Calculation

The amount of optical overfill on the critical area of the window aperture cannot be measured directly. For systems with uniform illumination on the array the amount is determined using the total measured incident optical power on the DMD, and the ratio of the total optical power on the DMD that is on the defined critical area. The optical model is used to determine the percent of optical power on the window aperture critical area and estimate the size of the area.

$$Q_{AP-ILL} = [Q_{INCIDENT} \times OP_{AP_ILL_RATIO}] \div A_{AP_ILL} \text{ (W/cm}^2\text{)}$$

where:

- Q_{AP-ILL} = window aperture illumination overfill (W/cm^2)
- $Q_{INCIDENT}$ = total incident optical power on the DMD (Watts) (measured)
- $OP_{AP_ILL_RATIO}$ = ratio of the optical power on the critical area of the window aperture to the total optical power on the DMD (optical model)
- A_{AP-ILL} = size of the window aperture critical area (cm^2) (datasheet)
- OP_{CA_RATIO} = percent of the window aperture critical area with incident optical power (%) (optical model)

Sample calculation:

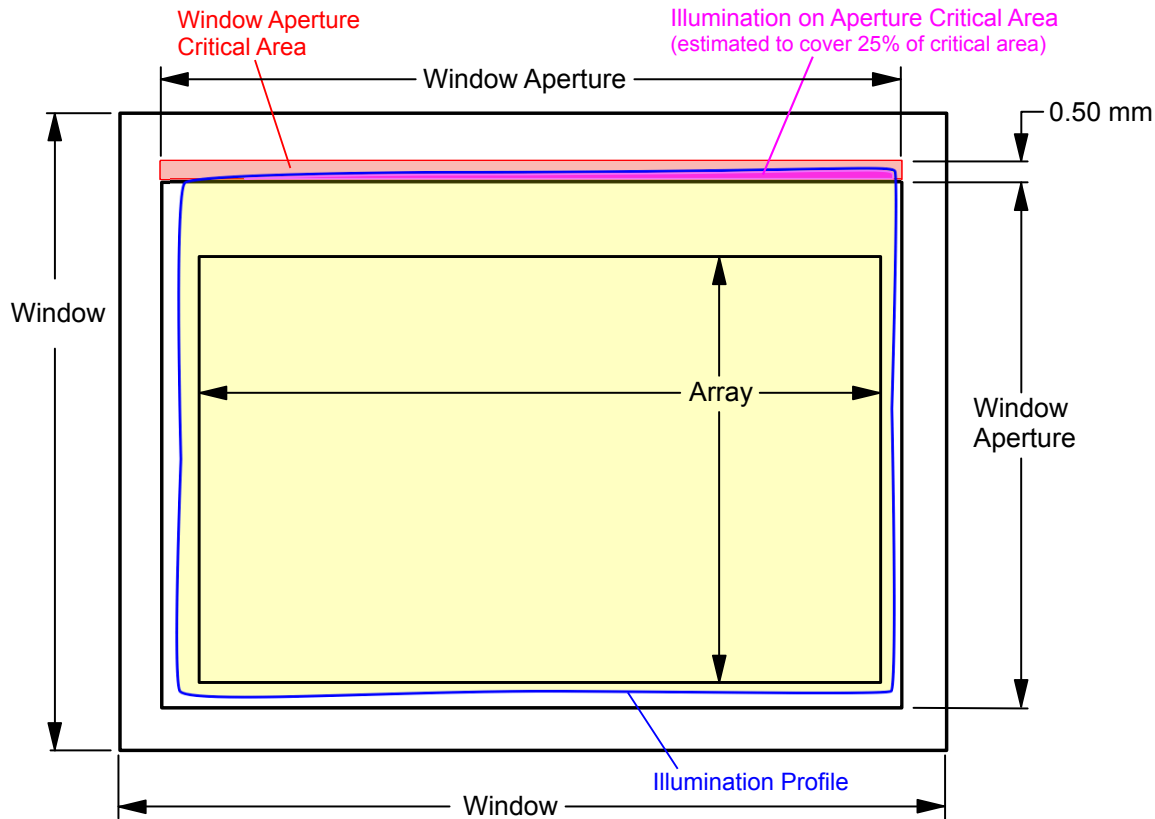


Figure 6-4. Window Aperture Overfill Example

See the figure for the length of the critical aperture.

$$Q_{\text{INCIDENT}} = 23.8\text{W (measured)} \quad (16)$$

$$OP_{\text{AP_ILL_RATIO}} = 0.312\% \text{ (optical model)} \quad (17)$$

$$OV_{\text{CA_RATIO}} = 25\% \text{ (optical model)} \quad (18)$$

$$\text{Length of the window aperture for critical area} = 1.8613\text{cm (data sheet)} \quad (19)$$

$$\text{Width of critical area} = 0.050\text{cm (data sheet)} \quad (20)$$

$$A_{\text{AP-ILL}} = 1.8613\text{cm} \times 0.050\text{cm} = 0.093065 \text{ (cm}^2\text{)} \quad (21)$$

$$Q_{\text{AP-ILL}} = (23.8\text{W} \times 0.00312) \div (0.093065\text{cm}^2 \times 0.25) = 3.2 \text{ (W/cm}^2\text{)} \quad (22)$$

6.9 Micromirror Landed-On/Landed-Off Duty Cycle

6.9.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the percentage of time that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

For example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the ON state 100% of the time (and in the OFF state 0% of the time); whereas 0/100 indicates that the pixel is in the OFF state 100% of the time. Likewise, 50/50 indicates that the pixel is ON for 50% of the time (and OFF for 50% of the time).

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

6.9.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD useful life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

6.9.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect DMD useful life, and this interaction can be exploited to reduce the impact that an asymmetrical landed duty cycle has on the DMD useful life. This is quantified in the derating curve shown in [Figure 5-1](#).

The importance of this curve is that:

- All points along this curve represent the same useful life.
- All points above this curve represent lower useful life (and the further away from the curve, the lower the useful life).
- All points below this curve represent higher useful life (and the further away from the curve, the higher the useful life).

In practice, this curve specifies the maximum operating DMD temperature for a given long-term average landed duty cycle.

6.9.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the landed duty cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel operates under a 100/0 landed duty cycle during that time period. Likewise, when displaying pure-black, the pixel operates under a 0/100 landed duty cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the gray scale value, as shown in [Table 6-1](#).

Table 6-1. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30

**Table 6-1. Grayscale Value and Landed Duty Cycle
(continued)**

GRAYSCALE VALUE	LANDED DUTY CYCLE
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

Use [Equation 23](#) to calculate the landed duty cycle of a given pixel during a given time period.

$$\text{Landed Duty Cycle} = (\text{Red_Cycle_}\% \times \text{Red_Scale_Value}) + (\text{Green_Cycle_}\% \times \text{Green_Scale_Value}) + (\text{Blue_Cycle_}\% \times \text{Blue_Scale_Value}) \quad (23)$$

where

- Red_Cycle_% represents the percentage of the frame time that red is displayed to achieve the desired white point.
- Green_Cycle_% represents the percentage of the frame time that green is displayed to achieve the desired white point.
- Blue_Cycle_% represents the percentage of the frame time that blue is displayed to achieve the desired white point.

For example, assume that the red, green, and blue color cycle times are 30%, 50%, and 20% respectively (to achieve the desired white point), then the landed duty cycle for various combinations of red, green, blue color intensities are shown in [Table 6-2](#) and [Table 6-3](#).

Table 6-2. Example Landed Duty Cycle for Full-Color, Color Percentage

CYCLE PERCENTAGE		
RED	GREEN	BLUE
30%	50%	20%

Table 6-3. Example Landed Duty Cycle for Full-Color

SCALE VALUE			LANDED DUTY CYCLE
RED	GREEN	BLUE	
0%	0%	0%	0/100
100%	0%	0%	30/70
0%	100%	0%	50/50
0%	0%	100%	20/80
0%	12%	0%	6/94
0%	0%	35%	7/93
60%	0%	0%	18/82
0%	100%	100%	70/30
100%	0%	100%	50/50
100%	100%	0%	80/20
0%	12%	35%	13/87
60%	0%	35%	25/75
60%	12%	0%	24/76
100%	100%	100%	100/0

The last factor to account for in estimating the landed duty cycle is any applied image processing. Within the DLPC6422 light controller, the gamma function affects the landed duty cycle.

Gamma is a power function of the form $\text{Output_Level} = A \times \text{Input_Level}^{\text{Gamma}}$, where A is a scaling factor that is typically set to 1.

In the DLPC6422 light controller gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in [Figure 6-5](#).

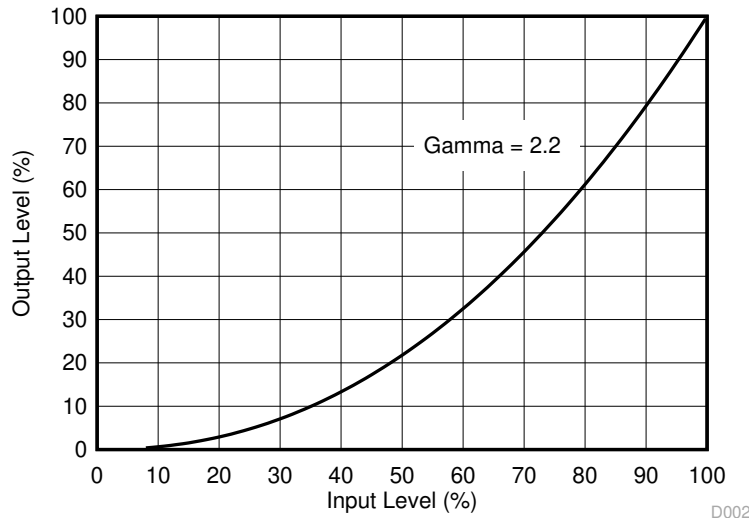


Figure 6-5. Example of Gamma = 2.2

From [Figure 6-5](#), if the gray scale value of a given input pixel is 40% (before gamma is applied), then gray scale value is 13% after gamma is applied. Therefore, it can be seen that since gamma has a direct impact displayed gray scale level of a pixel, it also has a direct impact on the landed duty cycle of a pixel.

Consideration must also be given to any image processing that occurs before the DLPC6422 light controller.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into DLPC6422 Controller. Typical applications using the DLP78TUV DMD include 3D print and other laser manufacture application

DMD power-up and power-down sequencing is strictly controlled by the DLPC6422 Controller through the DLPA300. Refer to [Section 7.4.2](#) for power-up and power-down specifications. For reliable operation, the DLP78TUV DMD must always be used with DLPC6422 Controller a [DLPA100](#) PMIC/Motor driver and a DLPA300 Micromirror Driver.

7.2 Typical Application

The DLP78TUV DMD combined with two DLPC6422 light controller and a power management device provides 4K UHD 3840x2160 resolution image on resin. When DLP78TUV is used with single DLPC6422 light controller, the system will provide 1920x1080 resolution image on resin. A typical 3D Print system using LED illumination combines the DLP78TUV DMD, two or one DLPC6422 light controllers, DLPA300 micromirror driver and [DLPA100](#) PMIC. [Figure 7-1](#) and [Figure 7-2](#) show a system block diagram for this configuration of the DLP .78 chipset and additional system components needed for 1080p and 4K System.

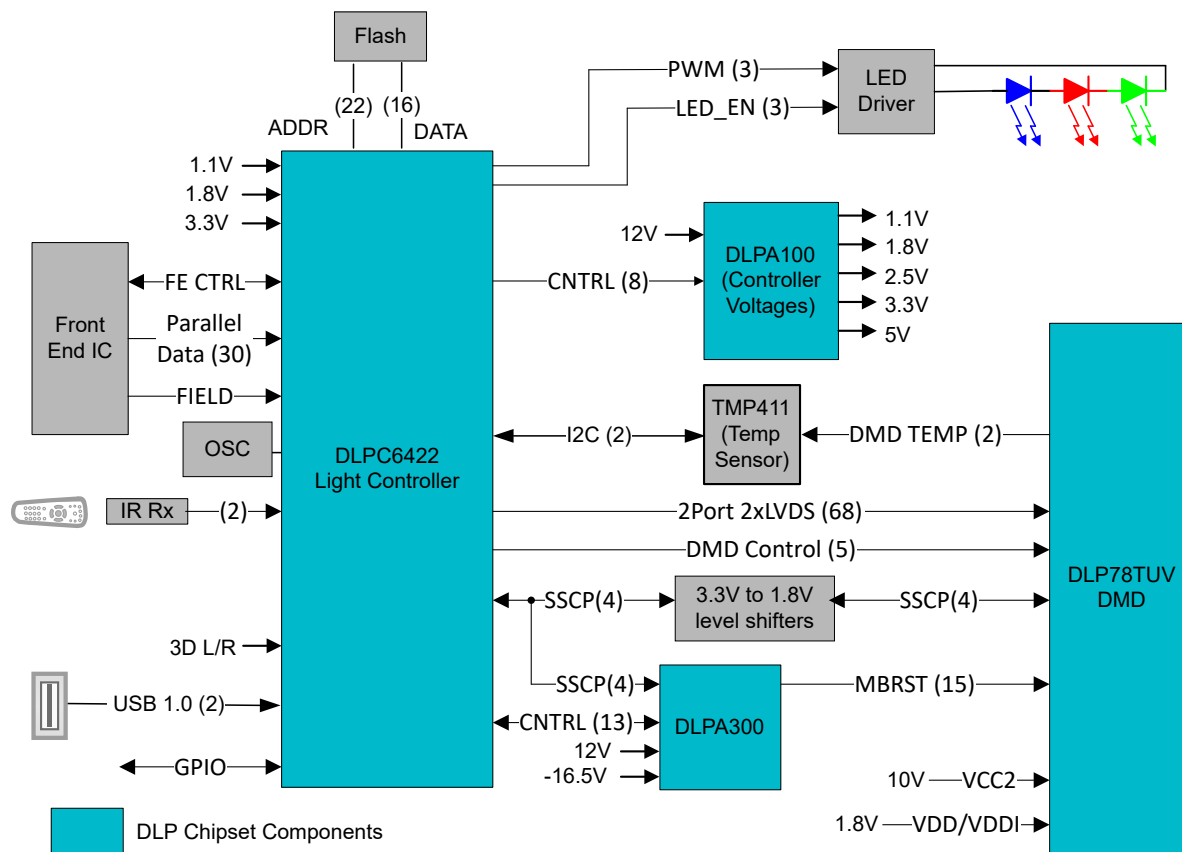


Figure 7-1. Typical Full HD LED Application



Other core components of the display system include an illumination source, an optical engine for the illumination and projection optics, other electrical and mechanical components, and software. The type of illumination used and desired brightness has a major effect on the overall system design and size.

Copyright © 2025 Texas Instruments Incorporated

7.2.2 Detailed Design Procedure

For a complete DLP system, an optical module or light engine is required that contains the DLP78TUV DMD, associated illumination sources, optical elements, and necessary mechanical components.

For reliable operation, the DMD must always be used with two or one DLPC6422 light controllers, the DLPA300 micromirror driver and the [DLPA100](#) PMIC and motor driver.

7.2.3 Application Curve

In a typical 3D print and imaging application, the light output from the DMD depends on the optical design of the system. The efficiency and total power of the illumination optical system and the projection optical system determines the overall light output of the projector. The DMD is inherently a linear spatial light modulator, so its efficiency just scales the light output. Figure 7-3 describes the relationship of illumination input optical power to light output for a led/laser system, where the light power is within DMD power density specification.

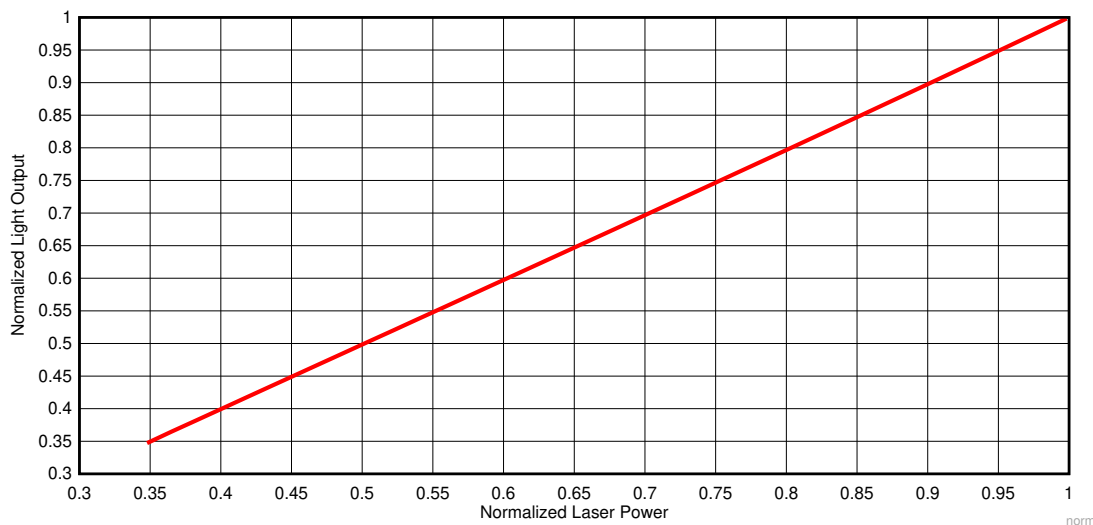
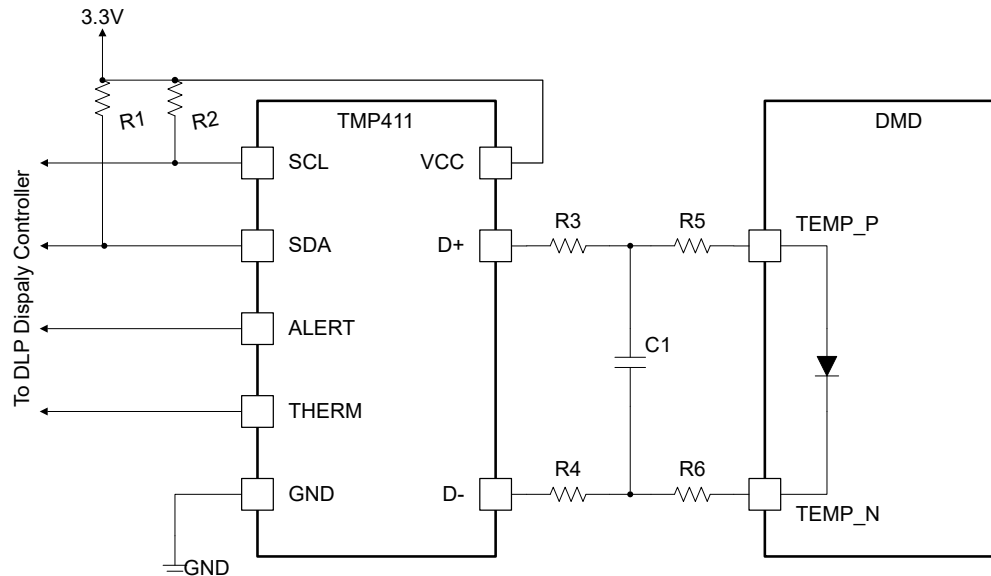


Figure 7-3. Normalized Light Output vs Normalized LED/Laser Power as Illumination

7.3 Temperature Sensor Diode

The DMD features a built-in thermal diode that measures the temperature at one corner of the die outside the micromirror array. The thermal diode can be interfaced with the TMP411 temperature sensor as shown in [Figure 7-4](#). The software application contains functions to configure the [TMP411](#) to read the DLP78TUV DMD temperature sensor diode. This data can be leveraged by the customer to incorporate additional functionality in the overall system design such as adjusting illumination, fan speeds, etc. All communication between the TMP411 and the DLPC6422 light controller happens over the I²C interface. The TMP411 connects to the DMD through pins outlined in [Section 4](#).

Leave TEMP_N and TEMP_P pins unconnected (NC) if the temp sensor is not used.



- A. Details omitted for clarity.
 B. See the TMP411 datasheet for system board layout recommendation.
 C. See the TMP411 datasheet and the TI reference design for suggested component values for R1, R2, R3, R4, and C1.
 D. R5 = 0Ω. R6 = 0Ω. Place 0Ω resistors close to the DMD package pins.

Figure 7-4. TMP411 Sample Schematic

7.4 Power Supply Recommendations

7.4.1 DMD Power Supply Requirements

The following power supplies are all required to operate the DMD: VDD, VDDI, and VCC2. VSS must also be connected. DMD power-up and power-down sequencing is strictly controlled by the DLPC6422 light controller.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability. VDD, VDDI and VCC2 power supplies have to be coordinated during power-up and power-down operations. VSS must also be connected. Failure to meet any of the below requirements results in a significant reduction in the reliability and lifetime of the DMD. Refer to [Figure 7-5](#).

7.4.2 DMD Power Supply Power-Up Procedure

- During power-up, VDD and VDDI must always start and settle before VCC2 is applied to the DMD.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements listed in [Section 5.1](#) and in [Section 5.4](#).
- During power-up, LVCMOS input pins must not be driven high until after VDD and VDDI have settled at operating voltages listed in [Section 5.4](#) table.

7.4.3 DMD Power Supply Power-Down Procedure

- During power-down, VDD and VDDI must be supplied until after VCC2 is discharged to within the specified limit of ground. Refer to [Section 5.4](#).
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements listed in [Section 5.1](#) and in [Section 5.4](#).
- During power-down, LVCMOS input pins must be less than specified in [Section 5.4](#).

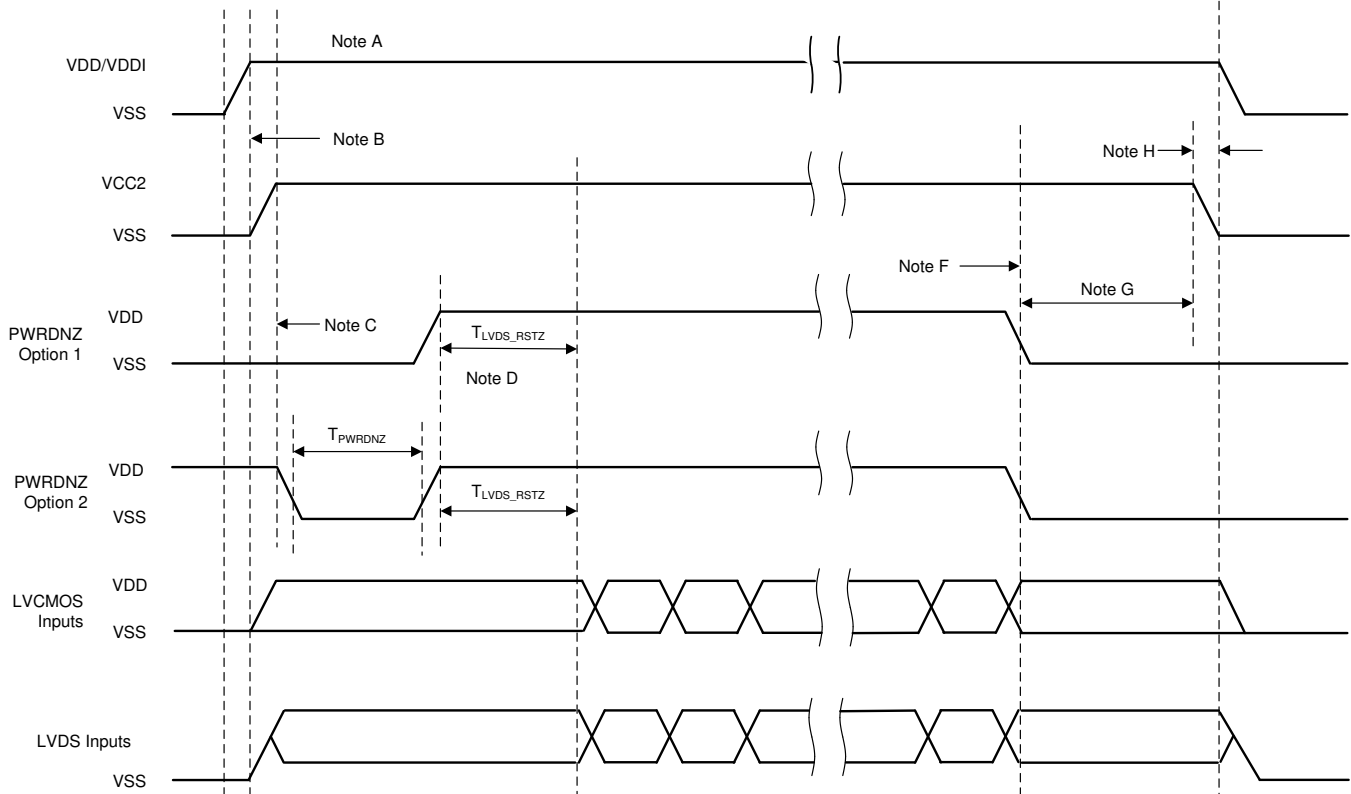


Figure 7-5. DMD Power Supply Sequencing Requirements

- A. See *Pin Configuration and Functions* for pin functions.
- B. VDD must be up and stable prior to VCC2 powering up.
- C. PWRDNZ has two turn on options. Option 1: PWRDNZ does not go high until VDD and VCC2 are up and stable, or Option 2: PWRDNZ must be pulsed low for a minimum of T_{PWRDNZ} , or 10ns after VDD and VCC2 are up and stable.
- D. There is a minimum of T_{LVDS_ARSTZ} , or 2 μ s, wait time from PWRDNZ going high for the LVDS receiver to recover.
- E. After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates the PWRDNZ and disables VCC2.
- F. Under power-loss conditions, where emergency DMD micromirror park procedures are being enacted by the DLP controller hardware, PWRDNZ goes low.
- G. VDD must remain high until after VCC2 goes low.
- H. To prevent excess current, the supply voltage delta $|VDDI - VDD|$ must be less than specified limit in [Section 5.4](#).

7.5 Layout

7.5.1 Layout Guidelines

The DLP78TUV DMD is part of a chipset that is controlled by the two or one DLPC6422 light controllers in conjunction with the DLP300 micromirror driver and the DLPA100 power and motor driver. These guidelines are targeted at designing a PCB board with the DLP78TUV DMD. The DLP78TUV DMD board is a high-speed multi-layer PCB, with primarily high-speed digital logic utilizing dual edge clock rates up to 400MHz for DMD LVDS signals. The remaining traces are comprised of low speed digital LVTTTL signals. Solid planes are required for DMD_P1P8V and Ground. The target impedance for the PCB is $50\Omega \pm 10\%$ with the LVDS traces being $100\Omega \pm 10\%$ differential. TI recommends using an 8-layer stack-up as described in [Table 7-1](#).

7.5.2 Layout Example

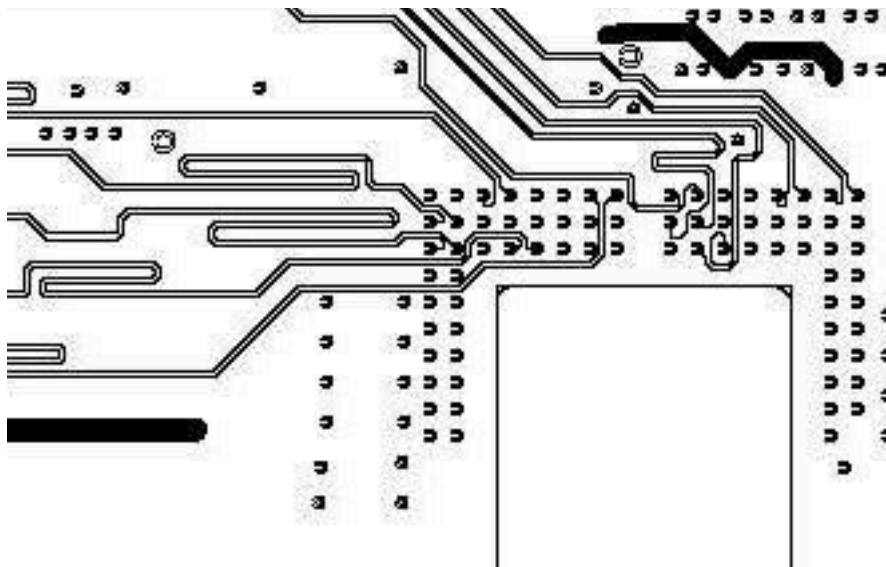


Figure 7-6. Typical example for matching LVDS signal lengths by serpentine sections

7.5.2.1 Layers

The layer stack-up and copper weight for each layer is shown in [Table 7-1](#). Small subplanes are allowed on signal routing layers to connect components to major subplanes on top and bottom layers if necessary.

Table 7-1. Layer Stack-Up

LAYER NO.	LAYER NAME	COPPER WT. (oz.)	COMMENTS
1	Side A—DMD only	1.5	DMD, escapes, low frequency signals, power subplanes
2	Ground	1	Solid ground plane (net GND)
3	Signal	0.5	50Ω and 100Ω differential signals
4	Ground	1	Solid ground plane (net GND)
5	VDD and VDDI	1	+1.8V power plane
6	Signal	0.5	50Ω and 100Ω differential signals
7	Ground	1	Solid ground plane (net GND)
8	Side B—All other Components	1.5	Discrete components, low frequency signals, power subplanes

7.5.2.2 Impedance Requirements

TI recommends that the board has matched impedance of 50Ω ±10% for all signals. The exceptions are listed in [Table 7-2](#).

Table 7-2. Special Impedance Requirements

SIGNAL TYPE	SIGNAL NAME	IMPEDANCE (Ω)
A channel LVDS differential pairs	DDAP(0:15), DDAN(0:15)	100 ±10% differential across each pair
	DCLKA_P, DCLKA_N	
	SCTRL_AP, SCTRL_AN	

Table 7-2. Special Impedance Requirements (continued)

SIGNAL TYPE	SIGNAL NAME	IMPEDANCE (Ω)
B channel LVDS differential pairs	DDBP(0:15), DDBN(0:15)	100 $\pm$ 10% differential across each pair
	DCLKB_P, DCLKB_N	
	SCTRL_BP, SCTRL_BN	
C channel LVDS differential pairs	DDCP(0:15), DDCN(0:15)	100 $\pm$ 10% differential across each pair
	DCLKC_P, DCLKC_N	
	SCTRL_CP, SCTRL_CN	
D channel LVDS differential pairs	DDDP(0:15), DDDN(0:15)	100 $\pm$ 10% differential across each pair
	DCLKD_P, DCLKD_N	
	SCTRL_DP, SCTRL_DN	

7.5.2.3 Trace Width, Spacing

Unless otherwise specified, TI recommends that all signals follow the 0.005"/0.005" design rule. Minimum trace clearance from the ground ring around the PWB has a 0.1" minimum. An analysis of impedance and stack-up requirements determine the actual trace widths and clearances.

7.5.2.3.1 Voltage Signals**Table 7-3. Special Trace Widths, Spacing Requirements**

SIGNAL NAME	MINIMUM TRACE WIDTH TO PINS (MIL)	LAYOUT REQUIREMENT
GND	15	Maximize trace width to connecting pin
3.3-V Supply Rail	15	Maximize trace width to connecting pin
VDD, VDDI	15	Maximize trace width to connecting pin
MBRST(0,14)	15	Use 10mil etch to connect all signals/voltages from DLPA300 to DLP78TUV
VCC2	15	Create mini plane from Voltage regulator to DLP78TUV

8 Device and Documentation Support

8.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

8.2 Device Support

8.2.1 Device Nomenclature

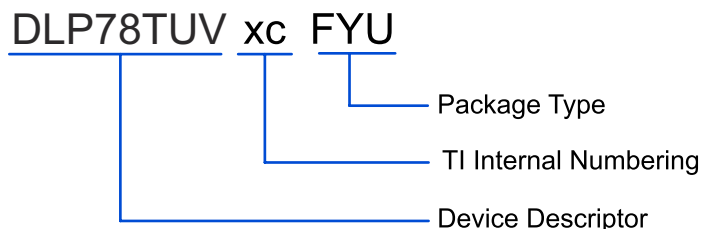


Figure 8-1. Part Number Description

8.3 Device Markings

The device marking includes both human-readable information and a 2-dimensional matrix code. The human-readable information is described in [Figure 8-2](#). The 2-dimensional matrix code is an alpha-numeric string that contains the DMD part number, Part 1 and Part 2 of the serial number.

Example:

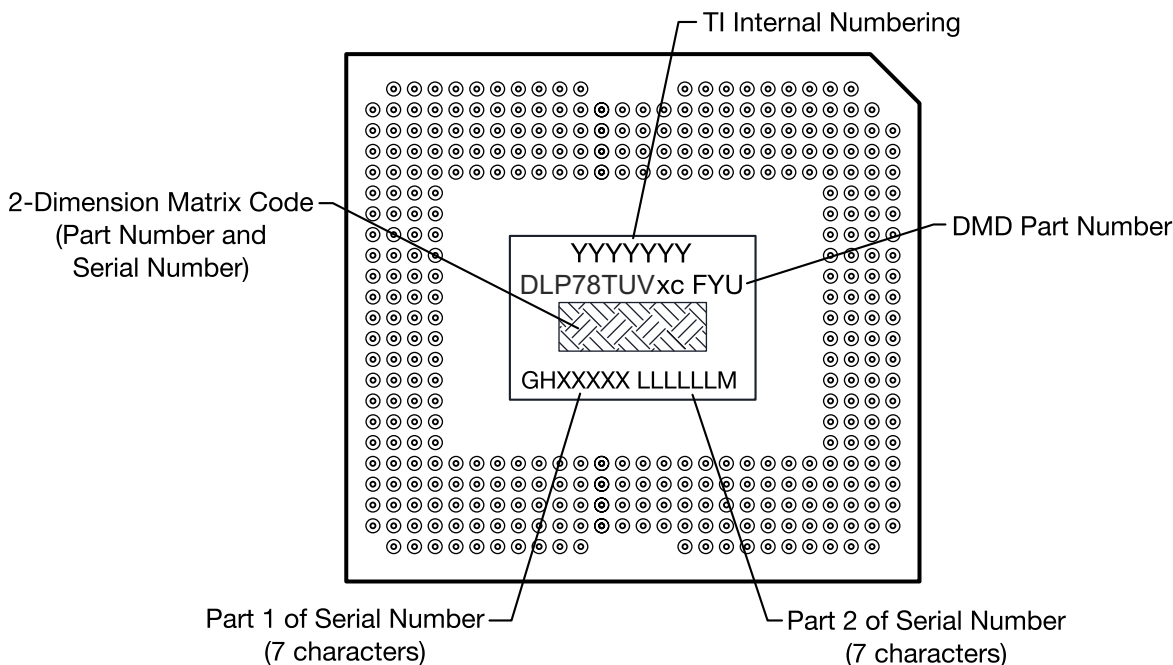


Figure 8-2. DMD Marking Locations

8.4 Documentation Support

8.4.1 Related Documentation

- [DLPC6422 DLP light Controller Data Sheet](#)
- [DLPA100 Power and Motor Driver Data Sheet](#)
- [DLPA300 DMD Micromirror Driver Data Sheet](#)

8.5 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.6 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.7 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

8.8 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.9 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2025) to Revision A (November 2025)	Page
• First public release of the data sheet.....	1

DATE	REVISION	NOTES
September 2025	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLP78TUV A0FYU	Active	Production	null (null)	21 JEDEC TRAY (5+1)	Yes	NIAU	N/A for Pkg Type	0 to 70	

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025